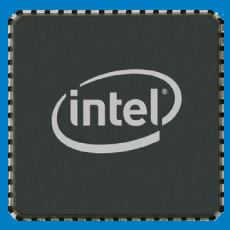
Product Brief

Intel® Ethernet Controller I210



Low-power, small-footprint, single-port gigabit network controller

Key Features

- IEEE 802.1Qav Audio-Video Bridging (AVB) for tightly controlled media stream synchronization, buffering and reservation
- Hardware-based timestamping of IEEE 1588 and 802.1AS packets
- Innovative power management features including Energy Efficient Ethernet (EEE) and DMA Coalescing
- Supports commercial and industrial temperature applications
- MDI (Copper) standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, 10BASE-T connections (IEEE 802.3, 802.3u, 802.3ab)
- Supports a SerDes interface for 1000BASE-SX/LX fiber connections as well as an SGMII interface for SFP and external PHY connections

Overview

The Intel® Ethernet Controller I210 provides a full-featured Gigabit Ethernet Media Access Control (MAC) and Physical-Layer (PHY) for Desktop, Server, and Embedded Applications. This controller is ideal for embedded applications such as industrial automation, in-vehicle infotainment, medical, print imaging, telecommunications infrastructure, and for military.

The I210 supports advanced features such as Audio-Video Bridging (AVB), IEEE 802.1AS precision timestamping, Error Correcting Code (ECC) Packet Buffers, and Enhanced Management Interface options.

The fully integrated GbE MAC/PHY capabilities can be configured for either 1000 Mb/s or 10/100 Mb/s modes of operation. The I210 enables a quick migration from custom interconnects to Ethernet.

Performance Optimization Capabilities

The Intel® Ethernet Controller I210 contains four transmit and four receive queues for the single port. These queues offer Error Correcting Memory (ECC) protection for improved data reliability. The controller efficiently manages packets with minimum latency by combining parallel and pipelined logic architectures optimized for these independent transmit and receive queues.

These queues, combined with Receive Side Scaling (RSS) and Message Signal Interrupt Extension (MSI-X) support, provide a toolset for optimizing the performance on multi-core processor designs.

Advanced interrupt-handling features to manage multiple interrupts simultaneously, combined with intelligent filtering, ordering, and directing of packets to specific queues and cores, enables load-balancing the network traffic flows to improve throughput in Multi-core platforms.

Other performance-enhancing features include IPv4 and IPv6 checksum offload, TCP/UDP checksum offload, extended Tx descriptors for more offload capabilities, up to 256 KB TCP segmentation (TSO v2), header splitting, 40 KB packet buffer size, and 9.5 KB Jumbo Frame support.

Advanced Features

Audio-Video Bridging (AVB)
Supports IEEE 802.1Qav Audio-Video Bridging (AVB) for customers that require tightly controlled media stream synchronization, buffering, and reservation. The 802.1Qav is part of the AVB specification that provides a way to guarantee bounded latency and latency variation for time-sensitive traffic and includes:

- Timing and Synchronization for time-specific applications (802.1AS)
- Stream Reservation (SR) protocol to guarantee the resources needed for Audio/Video (AV) streams (802.1Qat)
- Forwarding and queueing enhancements for time-sensitive streams (802.1Qav)

IEEE 1588/802.1AS Timestamping
Supports IEEE 1588/802.1AS for precision timestamping of packets. IEEE 1588 provides a mechanism for clock synchronization requirements of measurement and control systems. The protocol supports system-wide synchronization accuracy in the submicrosecond range with minimal network and local clock computing resources. The protocol is spatially localized and allows simple systems to be installed and operate. The IEEE 802.1AS standard specifies the protocol used to ensure that synchronization requirements are met for time-sensitive applications, such as audio and video, across bridged and Virtual Bridged Local Area Networks (VBLAN) consisting of LAN media where the transmission delays are essentially fixed and symmetrical.

Flexible Filters
Supports a total of eight individually configurable flexible filters. Filters can be used for wake-up or proxying when in D3 state or for queueing when in D0 state.

Secure Flexible Firmware Architecture
Flexible Firmware Architecture with Secure NVM Update protects the flash from external unauthorized software programming. The I210-AT/IT/AS/IS implement a signed firmware authentication capability to verify the firmware and critical device settings with built-in corruption detection. The Intel® Ethernet Controller I210-AT/IT/AS/IS also supports dynamic firmware updating that enables firmware updates without the need for a system reboot. For I210-CL/CS an immutable firmware code is built into the ROM that eliminates firmware tampering or firmware replacement.

Software Definable Pins
Four Software Definable Pins (SDPs) enable additional design customization for embedded platforms. SDPs can be used for IEEE 1588 auxiliary device connections, to enable/disable the device, and for other miscellaneous hardware or software-control purposes. These pins can be individually configured to act as either standard inputs, General-Purpose Interrupt (GPI) input or output pins, as well as the default value of all pins configured as outputs.

Energy Efficient Ethernet (EEE)
Supports the IEEE 802.3az EEE standard so that during periods of low network activity, EEE reduces the power consumption of an Ethernet connection by negotiating with the switch port to transition to a low power idle (LPI) state.

This capability reduces power up to 50 percent of its normal operating power, saving power on both the network and the switch ports. When increased traffic is detected, the controller and the switch quickly come back to full power to handle the increased traffic. EEE is supported for both 1000BASE-T and 100BASE-TX.

Multiple Interface Options

The Intel Ethernet Controller I210 provides a fully integrated GbE MAC/PHY, which has integrated power control components that can reduce board component cost and board layout space. The small 9 mm x 9 mm package size increases board layout flexibility for all types of client, server, and embedded designs.

The I210-AT and I210-IT provide MDI (Copper), a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab).

The I210-IS, I210-CS, and I210-CL provide a SerDes interface to connect over a 1000BASE-BX or 1000BASE-KX backplane to another SerDes-compliant device or to an optical module. The I210-IS, I210-CS, and I210-CL can also support an SGMII interface for SFP and external PHY connections for even greater design flexibility.

The I210CS and I210-CL provide a SerDes or SGMII interface for Automotive applications supporting AEC-Q100 Grade 3.

Flexible Design Configurations

The I210 can be used for server system configurations such as rack-mounted or pedestal servers, in an add-on NIC, in LAN on Motherboard (LOM) designs and for blade servers. In the latter case, the I210-IS can support a SerDes port in a LOM design or on a blade mezzanine card.

For customers needing extended temperature ranges, the I210-AT supports commercial temperature ranges of 0 °C to 70 °C. The I210-IT, 1210-IS, I210-CS, and I210-CL support -40 °C to 85 °C for industrial applications.

Interfaces for Network Manageability

The I210 provides OS2BMC, SMBus and DMTF-defined Network Controller Sideband Interface (NC-SI) for BMC manageability. In addition, it introduces support for Management Component Transport Protocol (MCTP), a new DMTF standard, enabling a BMC to gather information about Intel Ethernet Controllers that use the data rate, link speed, and error counts.

Features	Description
External Interfaces	
PCI Express 2.1	• 2.5 GT/s Support for x1 width (Lane)
Network Interfaces	• MDI (Copper) standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab) • Serializer-Deserializer (SerDes) to support 1000BASE-SX/LX (optical fiber - IEEE 802.3) • Serializer-Deserializer (SerDes) to support 1000BASE-KX (IEEE 802.3ap) and 1000BASE-BX (PICMIG 3.1) for Gigabit backplane applications • SGMII (Serial-GMII Specification) interface for SFP (SFP MSA INF-8074i)/external PHY connections
BOM Cost Reduction	
On-chip integrated Switched Voltage Regulator (iSVR)	• Removes need for a higher cost onboard voltage regulator
Ethernet Features	
IEEE 802.3 autonegotiation	• Automatic link configuration for speed duplex and flow control
1Gb/s Ethernet IEEE 802.3, 802.3u, 802.3ab PHY specifications compliant	• Robust operation over installed base of Cat5 twisted-pair cabling
Integrated PHY for 10/100/1000 Mb/s for multi-speed, full, and half-duplex	• Smaller footprint and lower power dissipation compared to multiple discreet MAC and PHYs
IEEE 802.3x and IEEE 802.3z compliant flow control support with software-controllable Rx thresholds and Tx pause frames	• Local control of network congestion levels
Automatic cross-over detection function (MDI/ MDI-X)	• Frame loss reduced from receive overruns
IEEE 1588 protocol and 802.1AS implementation	• The PHY automatically detects which application is being used and configures itself accordingly • Timestamping and synchronization of time sensitive applications • Distribute common time to media devices
Audio-Video Bridging (AVB) Support (802.1Qav)	• Dedicated Tx and Rx Queues for AVB traffic • Supports Forwarding and Queuing Enhancements for Time-Sensitive Streams • Supports Time-based transmission
Power Management Features	
Controller is designed for low power consumption	• <750 mW S0-Max (state) 1000BASE-T Active 70 °C (Intel® Ethernet Controller I210-AT) • <800 mW S0-Max (state) 1000BASE-T Active 85 °C (Intel® Ethernet Controller I210-IT, I210-CS, I210-CL) • <550 mW S0-Max (state) 1GbE SerDes/SGMII Active 85 °C (Intel® Ethernet Controller I210-IS, I210-CS, I210-CL)
IEEE 802.3az - Energy Efficient Ethernet (EEE)	• Power consumption by the PHY is reduced by approximately 50%; link transitions to low power Idle (LPI) state as defined in the IEEE 802.3az (EEE) standard
Smart power down (SPD) at S0 no link/Sx no link	• PHY powers down circuits and clocks that are not required for detection of link activity
Active State Power Management (ASPM)	• Optionality Compliance bit enables ASPM or runs ASPM compliance tests to support entry to L0s
LAN disable function	• Option to disable the LAN Port and/or PCIe Function. Disabling just the PCIe function but keeping the LAN port that resides on it fully active (for manageability purposes and BMC pass-through traffic).
Full wake up support:	• Advanced Power Management (APM) Support–[formerly Wake on LAN] - APM: Designed to receive a broadcast or unicast packet with an explicit data pattern (Magic Pack) and assert a signal to wake up the system • Advanced Configuration and Power Interface (ACPI) specification v2.0c - ACPI: PCIe power management based wake-up that can generate system wake-up events from a number of sources • Magic Packet wake-up enable with unique MAC address
ACPI register set and power down functionality supporting D0 and D3 states	• Power-managed speed control lowers link speed/power when highest link performance is not required
MAC Power Management controls	• Power management controls in the MAC /PHY enable the device to enter a low-power state
Low Power Link Up - Link Speed Control	• Enables a link to come up at the lowest possible speed in cases where power is more important than performance
Power Management Protocol Offload (Proxying)	• Enables a link to come up at the lowest possible speed in cases where power is more important than performance
Latency Tolerance Reporting (LTR)	• Reports service latency requirements for memory reads and writes to the Root Complex

Features	Description
Stateless Offloads and Performance Features	
Connections	• Reports service latency requirements for memory read and write to the Root Complex
TCP/UDP, IPv4 checksum offloads (Rx/ Tx/Large- send); Extended Tx descriptors)	• More offload capabilities and improved CPU usage • Checksum and segmentation capability extended to new standard packet type
Transmit Segmentation Offloading (TSO) (IPv4, IPv6)	• Increased throughput and lower processor usage
Interrupt throttling control	• Limits maximum interrupt rate and improves CPU usage
Legacy and Message Signal Interrupt (MSI)	• Interrupt mapping.
Message Signal Interrupt Extension (MSI-X)	• Dynamic allocation of up to 5 vectors per port
Intelligent interrupt generation	• Enhanced software device driver performance
Network Standard Physical Layer Interfaces	• Reports service latency requirements for memory reads and writes to the Root Complex
Receive Side Scaling (RSS) for Windows	• Up to four queues per port
Scalable I/O for Linux environments (IPv4, IPv6, TCP/UDP)	• Improves the system performance related to handling of network data on multiprocessor systems
Support for packets up to 9.5 KB (Jumbo Frames)	• Enables faster and more accurate throughput of data
Low-Latency Interrupts	• Based on the sensitivity of the incoming data, the controller can bypass the automatic moderation of time intervals between the interrupts
Header/packet data split in receive	• Helps the driver to focus on the relevant part of the packet without the need to parse it
PCIe 2.1 TLP Processing Hint Requester	• Provides hints on a per transaction basis to facilitate optimized processing
Descriptor ring management hardware for Transmit and Receive	• Optimized descriptor fetch and write-back for efficient system memory and PCIe bandwidth usage
Remote Boot Options	
Preboot Execution Environment (PXE) flash interface support	• Enables system boot via the EFI (32-bit and 64-bit) • Flash interface for PXE 2.1 option ROM
Intel® Boot Agent software--Linux boot via PXE or BOOTP, Windows Deployment Services, or UEFI	• Enables networked computer to boot using a program code image supplied by a remote server • Complies with the Preboot Execution Environment (PXE) Version 2.1 Specification
Manageability Features	
DMTF Network Controller Sideband Interface (NC-SI) Pass-through	• Supports pass through traffic between BMC and Controller's LAN functions • Meets RMII Spec, Rev. 1.2 as a PHY-side device
Intel® System Management Bus (SMBus) Pass-through	• Enables BMC to configure the Controller's filters and management related capabilities.
Management Component Transport Protocol (MCTP) over SMBus and PCIe	• Used for baseboard management controller (BMC) communication between add-in devices
OS2BMC Traffic support	• Transmission and reception of traffic internally to communicate between the OS and local BMC
Private OS2BMC Traffic Flow	• BMC may have its own private connection to the network controller and network flows are blocked
Firmware Based Thermal Management	• Can be programmed via the BMC to initiate Thermal actions and report thermal occurrences
IEEE 802.3 MII Management Interface	• Enables the MAC and software to monitor and control the state of the PHY
MAC/PHY Control and Status	• Enhanced control capabilities through PHY reset, link status, duplex indication, and MAC Dx power state
Watchdog timer	• Defined by the FLASHT register to minimize Flash updates
Extended error reporting	• Messaging support to communicate multiple types/severity of errors
Controller Memory Protection	• Main internal memories are protected by error-correcting code (ECC) or parity bits
Vital Product Data (VPD) Support	• Support for VPD memory area

Supported Operating Systems

The Feature Support Matrix for Intel® Ethernet Controllers includes a complete list of supported network operating systems.

Product Order Code

MM#	Brand Name	Description	Media	Product Order Code
925131	Intel® Ethernet Controller I210-AT	1000Base-T Commercial Temp	tape and reel	WGI210AT
925132	Intel® Ethernet Controller I210-AT	1000Base-T Commercial Temp	tray	WGI210AT
937549	Intel® Ethernet Controller I210-CS	SerDes/SGMII Automotive AEC-Q100 grade 3	tape and reel	WGI210CS
937548	Intel® Ethernet Controller I210-CS	SerDes/SGMII Automotive AEC-Q100 grade 3	tray	WGI210CS
958497	Intel® Ethernet Controller I210-CL	SerDes/SGMII Automotive AEC-Q100 grade 3 (<20 DPM)	tape and reel	WGI210CL
958496	Intel® Ethernet Controller I210-CL	SerDes/SGMII Automotive AEC-Q100 grade 3 (<20 DPM)	tray	WGI210CL

Product Order Code (continued)

MM#	Brand Name	Description	Media	Product Order Code
925133	Intel® Ethernet Controller I210-IT	1000Base-T Industrial Temp	tape and reel	WGI210IT
925138	Intel® Ethernet Controller I210-IT	1000Base-T Industrial Temp	tray	WGI210IT
925142	Intel® Ethernet Controller I210-IS	SerDes/SGMII Industrial Temp	tape and reel	WGI210IS
925143	Intel® Ethernet Controller I210-IS	SerDes/SGMII Industrial Temp	tray	WGI210IS

Warranty

Standard Intel limited warranty, one year. See Intel terms and conditions of sale for more details.

Product Information

For information about Intel® Ethernet Products and technologies, visit: intel.com/ethernetproducts

Customer Support

For customer support options in North America visit:
intel.com/content/www/us/en/support/contact-support.html

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