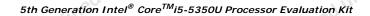
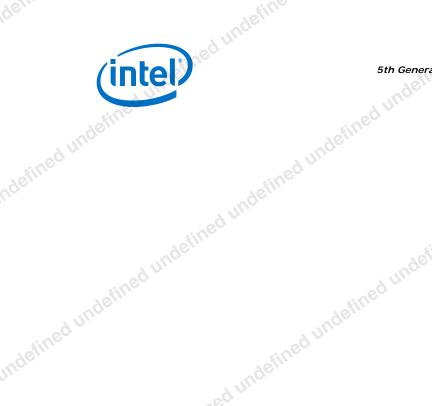


5th Generation Intel® CoreTM i55350U Processor Evaluation Kit Based on Intel® ISX Form Reference Design oduct User Guide ## 2016 undefined undefi 5350U Processor Evaluation Kit Based on Intel® ISX Form Factor undefined undefi

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Available on select Intel® processors. Requires an Intel® HT Technology-enabled system. Your performance varies depending on the specific hardware and software you use. Learn more by visiting: http://www.intel.com/info/hyperthreading.

Requires 3D glasses and a 3D-capable display. Physical risk factors may be present when viewing 3D material.

Requires a system with a 64-bit enabled processor, chipset, BIOS and software. Performance varies depending on the specific hardware and software you use. Check with your manufacturer for more information. Learn more at http://www.intel.com/info/em64t.

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Introduction

1.1 **About this Evaluation Kit**

The 5th Generation Intel[®] CoreTM i5-5350U Processor Evaluation Kit Based on Intel[®] Intelligent System Extended (ISX) Form Factor Reference Design is an Internet-of-Things (IoT) evaluation platform that can be used as-is by end-customers or can be customized by software vendors, driver developers, and system integrators.

The evaluation kit is based on the Intel® Intelligent System Extended (ISX) Form Factor Reference Design. It's a fanless design in a small form factor, made possible through process optimization, performance improvements, dynamic power, and thermal framework enhancements in the 5th generation Intel® CoreTM (U series) processor.

The evaluation kit is a dual-channel DDR3L mobility platform that uses a new 4.4 × 6.1 inch board form factor. It's a full performance computing platform in the smallest form factor possible that supports the 5th generation Intel[®] CoreTM (U series) processor in the BGA-type package. The Modular Board Design (MBD) of the Intel[®] ISX completes the critical signal paths for the processor and the supporting components according to Intel Design Guidelines.

This evaluation kit provides you with the necessary items to enable you to customize the board design to suit your requirements. Alternatively, for faster time to market, the board design can be used as-is out of the box.

Note:

The 5th generation Intel[®] CoreTM (U series) processor was formerly known as the Broadwell-U CPU.

1.2 **Terminology**

Table 1. **Terminology**

ind	Term	Definition
edu	APS	Automated Power Switch
istine	BIOS	Basic Input Output System
inde	CMOS	Refers to the non-volatile configuration memory in the PCH
	CPU	Central Processing Unit
undefined undefined und	DDR3L	Double Data Rate Synchronous Dynamic Random Access Memory third generation (low power)
Y OIL	GND	Signal Ground
	HDD	Hard disk drive
	HDMI	High Definition Multimedia Interface
nu .	LAN	Local Area Network
ined .	LED	Light Emitting Diode
defill	LPC	Low Pin Count
, uno	LVDS	Low-Voltage Differential Signaling
ined.	ME	Intel Management Engine
defill	OS	Operating System
d undefined undefined un	PCI	Peripheral Component Interface
	PCIe*	Peripheral Component Interface Express*

5th Generation Intel[®] CoreTM i5-5350U Processor Evaluation Kit Based on Intel[®] ISX Form Factor Reference Design April 2016 Document Number: 334089-001US



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defined under	Term	Definition	
inea	POST	Power-On Self Test	
defil	RTC	Real Time Clock	d undefined und
.Co.	S3	"Save to RAM" Sleep State	
	S5	"Soft Off" Sleep State	
	SATA	Serial - Advanced Technology Attachment	4 UM
inc	SIO	Super Input Output	
ndefined undefined un	SLP	Sleep	
ighthe	SO-DIMM	Small Outline Dual In-line Memory Module	
inde	SSD	Solid State Drive	
edu	USB	Universal Serial Bus	
iefine	VCC	Used to signify circuit logic voltage	.117
Inde	VDDQ	Used to signify DIMM logic supply voltage	
	VGA	Video Graphics Array	48fille
	VID	Voltage Identification	Inor
	VTT	Used to signify signal termination voltage	

Evaluation Board Parts

The evaluation board includes the following parts listed in Table 2 unless stated otherwise.

Table 2. **List of Evaluation Board Parts**

	sined under		
Evaluation Board Parts	Model	Quantity	refill,
4 GB 204-PIN DDR3L SDRAM Unbuffered SODIMM	Apacer (78.B2GCY.4000C)	2	defined u
mSATA SSD-64 G (half-size mPCIe*)	SANDISK (SDSA5FK-064 G)	1	
MA 2.4 G Terminal antenna (external)	UNI LINK (TLB-2400-2.5B L)	2	
Power adapter: Input: 100-240 V, AC 50/60 Hz Output:12 VDC, 4000 mA	KUANTECH (KSAH1200400W1UK)	ined 1	
Intel WiFi* module	Intel (6300 633AN.HMWG)	1	
mPCIe* half to full-size extender bracket	SC2MPCIEEXTOB1100P	1	- 61
3G/WiFi* Mini PCIe* card (half-size mPCIe*)‡	Option (GTM671W)	1	definee
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2.0 Getting Started

Before using the evaluation kit, verify that all the items listed in this section are received, and that the evaluation board is functioning by going through the following:

- · Check the contents of the evaluation kit
- Inspect the evaluation board for any defects
- · Power-on the evaluation board and verify that it is functioning correctly.

2.1 Before You Begin

Verify the contents of the evaluation kit and the condition of the evaluation board. If any of the items are missing or if the evaluation board is damaged, contact Intel before you proceed.

2.1.1 Check the Contents of the Evaluation Kit

The 5th Generation Intel[®] CoreTM i5-5350U Processor Evaluation Kit Based on Intel[®] Intelligent System Extended (ISX) Form Factor Reference Design contains the following items:

- 5th Generation Intel[®] CoreTM i5-5350U Processor Evaluation Kit Based on Intel[®] Intelligent System Extended (ISX) Form Factor Reference Design System
- 12 V@4 A DC Power Adapter
- System Drivers + User Guide (CD)
- · Safety Flyer
- · China RoHS Declaration
- WCI
- Intel[®] Evaluation Vehicles Terms and Conditions

2.1.2 Inspect the Evaluation Board

To check the evaluation board for damages, set it on an anti-static surface and inspect the evaluation board to ensure that the components are not missing, bent, or cracked.

Caution: The evaluation board may be damaged if it is not placed on an anti-static surface.

2.1.3 Power-on the Evaluation Board

Once the evaluation board is free from any visible defects, power-on the evaluation board and verify that the evaluation board is functioning correctly using the following steps:

1. Connect the supplied DC power adapter to the evaluation board.

Note: Only use the DC power adapter supplied with the evaluation kit.

- 2. Press the **POWER BUTTON**.
- 3. Select the **Del** key as the system boots to enter the BIOS setup screen.
- 4. Check the time, date, and configuration settings. The default settings should be sufficient for most users with the exception of Intel SpeedStep[®] Technology. This feature is disabled by default and can be enabled in setup.
- 5. Save and exit the BIOS setup.

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Based on Intel® ISX Form Factor Reference Design
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6. The system will reboot and would then be ready for use.

Note: The evaluation board can be powered down with the following methods:

- Use the Windows* Start menu (or equivalent) shutdown option
- Press the **POWER BUTTTON** to begin the power-down process
- If the above does not work, hold down the POWER BUTTON for four seconds to asynchronously shut down the system (not recommended).

Reference Documents

Table 3. **Technical Reference Documents**

raed III	Document Description	Document Number/Location	2
ndefined un	5th Generation Intel® Core™ Processor Family and Intel® Core™ M Processor Family (Broadwell U/Y) – External Design Specification (EDS) Volume 1 of 2	514405	undefined und
	Broadwell Mobile U-Processor and Y-Processor External Design Specification (EDS) Volume 2 of 2	514525	indeill
الله الله	5th Generation Intel [®] Core [™] i5-5350u Processor Evaluation kit based on Intel [®] ISX Reference Design – System Reference Design Schematic and Board File	556749	
lefined	5th Generation Intel [®] Core [™] i5-5350u Processor Evaluation Kit Based on Intel [®] ISX Reference Design BIOS Image – BIOS Reference Code	557335	
od unoe	5th Generation Intel [®] Core [™] i5-5350u Processor Evaluation kit based on Intel ISX Reference Design - Mechanical Reference Design Files	557242	
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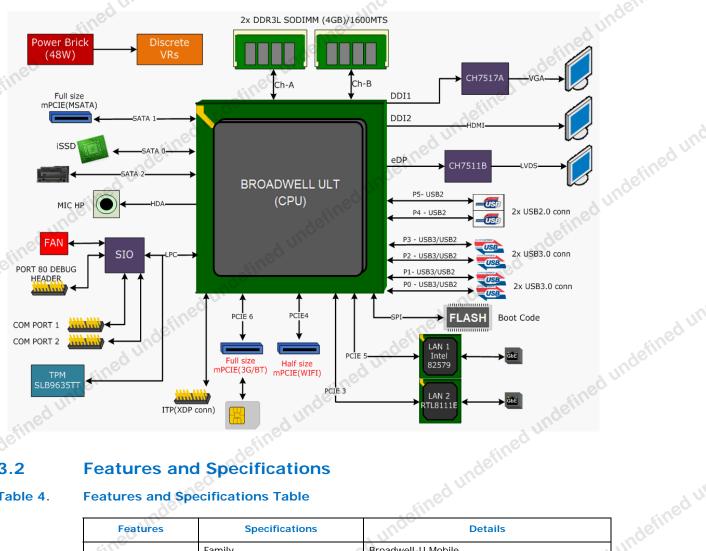




Evaluation Kit Overview

Block Diagram

Block Diagram of the Evaluation Kit Figure 1.



3.2 **Features and Specifications**

Table 4. **Features and Specifications Table**

ined	3.2	reatures and	Specifications	inge	
undefil	Table 4.	Features and Spe	ecifications Table	is fined L	ined v
2.		Features	Specifications	Details	defill
	ned un	СРИ	Family Model Package type TDP	Broadwell-U Mobile 5th Generation Intel [®] Core™ i7/i5/i3 Processor BGA 1168 Maximum up to 15 W	un
ined !	Indetili.	Memory	RAM type Maximum RAM size Maximum RAM speed RAM slot	DDR3L (1.35 V) 16GB ¹ 1600MT/s 2	
undein.		BIOS	SPI model	W25Q128FV; 128 M-bit SOIC-8 serial flash memory	, sed
30		EC/SIO	LPC-IO	IT8728F	defille

ned undefined 5th Generation Intel[®] CoreTM i5-5350U Processor Evaluation Kit Based on Intel[®] ISX Form Factor Reference Design April 2016 Document Number: 334089-001US



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4 unc	Features	Specifications	Details	
defined under.	Display	Graphic type Integrated audio Maximum resolution Display option Others	Integrated Supported 3840 × 2160 at 60 Hz 1 × VGA connector 1 × Standard HDMI connector 1 × Dual-channel LVDS header 3 Display supported	Indefined und
ndefined undefined und	Storage	mSATA (default) HDD/SSD iSSD (optional) ²	Full-size Mini PCIe* slot Standard SATA 3.0 connector Soldered down iSSD (optional) ²	
red under	Audio	Integrated HD Audio Codec Codec model Port	Supported Realtek ALC662 1 × 3.5 mm jack with line out and mic	
ndefil.	USB	USB 3.0 USB 2.0	4 × USB 3.0 port 2 × USB 2.0 port	ed nu
	Network	Gigabit LAN port Intel LAN controller model 2nd LAN controller model 3G + WiFi* WiFi*	2 × RJ45 port Clarksville (i218-LM) with Intel [®] AMT support Realtek (RTL8111E) 1 × Full-size Mini PCIe slot + 1 × Micro SIM slot 1 × Half-size Mini PCIe slot	undefined uni
ined	Serial Port	COM port header	2 × RS232 header	
indefili	Power Supply	Mobile mode 48 W power adapter	12V @4 A input DC power	
undefined undefined und	Others	Clocks RTC Processor VR TPM LPC ITP	Fully integrated clocking Battery-backed real-time clock ISL95812; Intel VR12.5 Serial VID (SVID) compliant SLB9635TT; TPM ver 1.2 1 × LPC debug header 1 × XDP debug port	undefined ur
ed ur	System Form Factor Dimension	System Form Factor (W × L × H)	4.6" × 7.2" × 1.7"	
Jefined undefineo	PCB Dimensions	Board Form Factor Board Z-height PCB layer count	4.4" × 6.1" 1.61" 10 layers	
d undefined undefined u	1. The evaluation kit ne 2. This feature's part is	eds 64-bit Windows* installed to sunot populated on the system evaluated on the system evaluated for the system evaluated for the system evaluation evalua	April 2016 Document Number: 334089-001US	ed undefined u
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12		defill	Document Number: 334089-001US	
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^{1.} The evaluation kit needs 64-bit Windows* installed to support 16 GB memory.

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Power Management States

Table 5 lists the power management states that have been defined for the platform. The Controller Link (CL) operates at various power levels called M-states.

Power Management States Description Table 5.

	State	Description
inde	G0/S0	Full on mode. Display on.
ed u.	G0/S0	Connected standby mode. Display off.
adefine	G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory (S3-Hot is not supported by the processor).
d ull	G1/S4	Suspend-to-Disk (STD). All power lost (except wakeup on PCH).
adefined	G2/S5	Soft off. All power lost (except wakeup on PCH). Total system reboot.
ider.	G3	Mechanical off. All power source (AC and battery) removed from the system.
71.	The voltage of the ev	aluation board power nets at different activity states is shown in

The voltage of the evaluation board power nets at different activity states is shown in Table 6.

Table 6. **Evaluation Board Power States**

undefined undefined	POWER NET	VOLTAGE	POWER WELL	ACTIVITY STATES
adelli	+VDCIN	12 V	ALWAYS ON	S0-S5
ed ull	+V5 A	5 V	ALWAYS ON	S0-S5
"inec	+V3.3 A	3.3 V	ALWAYS ON	S0-S5
nder	18/11		eineo.	
O.	LAN1_V3P3	3.3 V	LAN	S0-S5
	+V3.3 M	3.3 V	ME	S0-S5
	+V1.05 M	1.05 V	ME	S0-S5
d undefined undefined und		deli		istine
ned	+VSM	1.355 V	DDR3L	S0-S3
defill	+VSM_VTT	0.675 V	DDR3L	S0
unc		"yde"		efille
ineo	+V12S	12 V	CORE	S0
deill	+V5S	5 V	CORE	S0
A Uluc	+V3.3S	3.3 V	CORE	S0
	+V1.05S	1.05 V	CORE	S0
	+VCORE	1.5 V-1.85 V	CORE	S0
771	+V1.8S	1.8 V	EDP to LVDS	SO STORY
edu	+V1.5S	1.5 V	CORE	S0
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5th Generation Intel[®] CoreTM i5-5350U Processor Evaluation Kit Based on Intel[®] ISX Form Factor Reference Design User Guide April 2016 Document Number: 334089-001US



4.0 Evaluation Kit Setup

This section provides the following details:

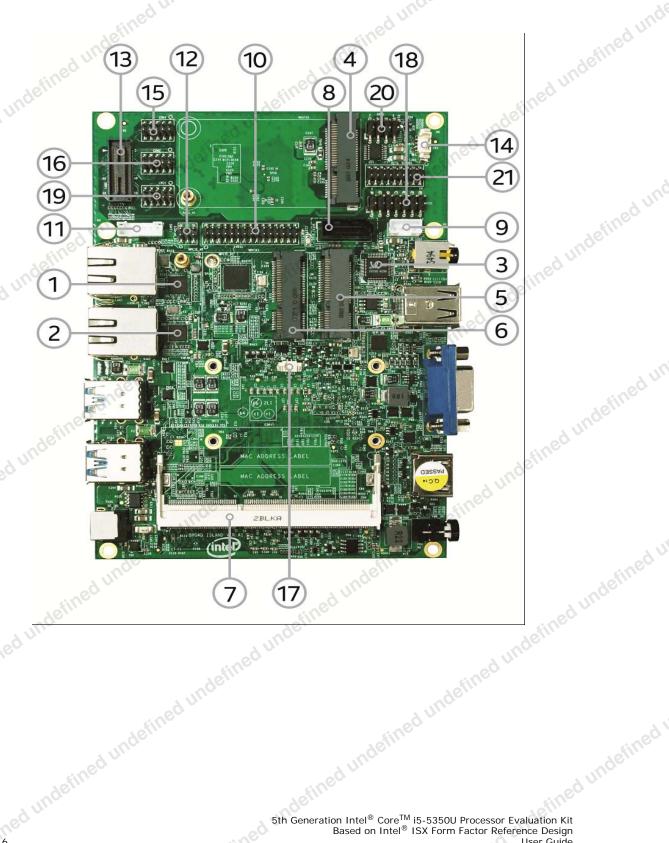
- Lists the major components and their locations on the evaluation board, front panel and back panel
- · Describes the pinouts of the headers
- Lists the LED indicator location and colors for different power states
- · Provides the configuration settings to clear the BIOS.

4.1 Layout of the Board, Front Panel, and Back Panel

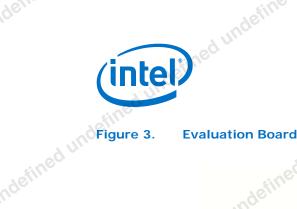
The following figures show the evaluation board, front panel, back panel layout, and the location of each major component.



Figure 2. **Evaluation Board Top Layer**



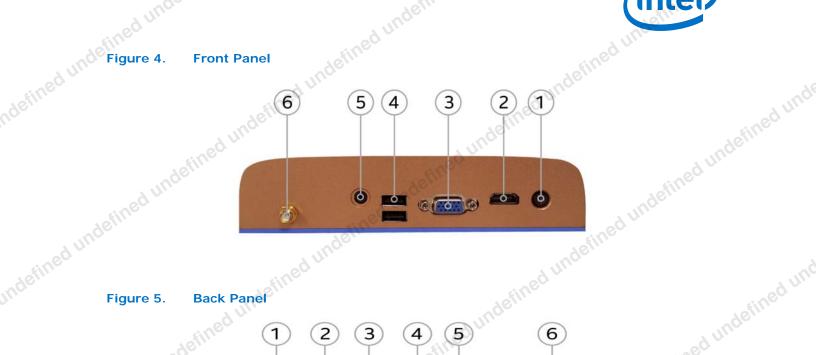
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Evaluation Board Bottom Layer





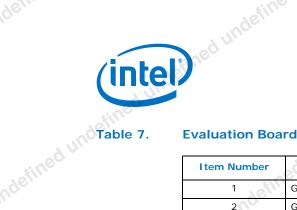




List of Components 4.2

The following tables list the major components and the reference designator of the

5th Generation Intel[®] CoreTM i5-5350U Processor Evaluation Kit Based on Intel[®] ISX Form Factor Reference Design User Guide April 2016 Document Number: 334089-001US



Evaluation Board Top Layer

4 um		1000000		
adefined une	Item Number	Description	Reference Designator	offined unde
	1 10111	GbE controller 2 (RTL8111E)	U5	od uli.
	2	GbE controller 1 (Clarkville- i128LM)	U32	Fine
	3	Audio Codec (ALC662)	U4	uge.
A	4	Mini PCIe connector (full size) - MSATA	MSATA1	
, une	5	3G + WiFi*	MPCIE2	
Indefined undefined und	6	Mini PCIe connector (half size)	MPCIE1	
defill	7	Non-ECC DDR3 sodimm connector (CH A)	J1	
June	8	SATA 3.0 connector	SATA1	
	9	SATA power header	SATA_PWR1	
deill	10	LVDS signals header	LVDS1	4 nu
	11 000	LVDS inverter power	INVT1	
	12	LVDS VDD selection power jumper	LCDPWR_SEL1	gell.
	13	XDP connector	XDP1	Ullia
	14	Fan 4-pin header	FAN1	
ed di	15	Serial port header (COM 1)	COM1	
istine	16	Serial port header (COM 2)	COM2	
undefined undefined un	17	RTC header	J_RTC1	
	18	APS header	APS1	
iefille	19	Port 80 LPC header	LPC1	711
III	20	SPI flash header	SPI1	
	21	Debug header	DEBUG1	defill.
Table 8.	Evaluation Boa	rd Bottom Layer	ine	Juna
ed u	Item Number	Description	Reference Designator	

Table 8. **Evaluation Board Bottom Layer**

			CANA	
d undefined undefined ut	Item Number	Description	Reference Designator	
18 file	1	CPU (Broadwell U)	U1	
11000	2	EC/SIO (IT8728F)	U11	
raed to	3	Non-ECC DDR3 sodimm connector (CH B)	J2	
defill.	4	SPI chip (W25Q128FV)	U3	
Uno	5 26	TPM (SLB9635TT)	U2	ed
	6	Micro SIM slot	SIM1	4efill.
	4109	ISSD (optional)	U29	NUC.
5th Generation Int	Indefille	Non-ECC DDR3 sodimm connector (CH B) SPI chip (W25Q128FV) TPM (SLB9635TT) Micro SIM slot ISSD (optional) Processor Evaluation Kit ence Design	indefined under	d undefined f
Based on Intel [®] IS User Guide	X Form Factor Refere	Processor Evaluation Kit ence Design	April 2016	
18		Docume	April 2016 ent Number: 334089-001US	
sined b		ence Design Docume	nuger.	
76/		410		



Table 9. **Front Panel**

	.000		
Item Number	Description	Reference Designator	
1	Power button	PWR_SW1	ed m.
2	HDMI connector	HDMI1	
3	VGA connector	VGA1	
4	Dual USB 2.0 stacked connector	USB3	
5	Single port audio jack	AUD1	
6	Antenna SMA connector 1	1100	
Back Panel	indefine	efined	
Item Number	Description	Reference Designator	

undefined und Table 10. **Back Panel**

			YO.
lefined b	Item Number	Description	Reference Designator
ie.	1 10	DC power jack Dual USB 3.0 stacked connector 1	DC_IN1
	2	Dual USB 3.0 stacked connector 1	USB2
.0.	3	Dual USB 3.0 stacked connector 2	USB1
76/	4	Single LAN RJ45 connector 1	LAN1
4 Unc.	5	Single LAN RJ45 connector 2	LAN2
"ingo	6	Antenna SMA connector 2	1100
defined undefined under	ined undefi	defined undefi	ne ^c
idefined undefined	d undef	Single LAN RJ45 connector 2 Antenna SMA connector 2	ined undefined under
d undefined unde	afineu.	indefined undefined un	defined undefine
Indefined	efined unde	Fined under	Fined unoe

theed underineed under 5th Generation Intel[®] CoreTM i5-5350U Processor Evaluation Kit Based on Intel[®] ISX Form Factor Reference Design User Guide 19 April 2016 Document Number: 334089-001US



ndefined und 4.3 **Header Pinout Configuration**

4.3.1 **Evaluation Board Header Pinout**

The following tables list the pinout configuration for the headers, and their corresponding signal names, on the evaluation board.

Table 11. **Evaluation Board Connector Functions**

indefined undefined und	Label	Function
	XDP1	XDP Debug Port
ade.	COM1	COM1
ad uli	COM2	COM2
	LPC1	Low Pin Count Bus interface
inde.	INVT1	Inverter Power
	LCDPWR_SEL1	LVDS Operating VDD Selection
	LVDS1	LVDS Connector
	J_RTC1	RTC Battery Connector
July 1	SATA_PWR1	SATA Power
	APS1	APS Debug Port
deill	Debug1	Debug Port
4 Unic	SPI1	SPI Flash Programming Connector
	FAN1	System Fan Connector
undefined undefined un	Jundefine	ndefined



Table 12.

5th Generation I	Intel [®] Core TM i5-5350U Pro	ocessor Evaluation Kit		(intel)	
4 une		inder		elli	
		ed un		Un	
Table 12.	XDP Debug Port (XI	OP1)			
Table 12.		96.	dell		1
	Pin	Signal Name	Pin	Signal Name	
	13/11/1	GND	2	GND	60
	3	PREQ	4	CFG17	defined
	5	PRDY	6	CFG16	19e.
	7	GND	8	GND	
ined undefined undef	9	CFG0	10	CFG8	
aneo.	11	CFG1	12	CFG9	
defil.	13	GND	14	GND	
unc	15	CFG2	16	CFG10	
	17	CFG3	18	CFG11	
	19	GND	20	GND	definer
	21	BPM0	22	CFG19	ine
	23	BPM1	24	CFG18	Yelli.
		GND	26	GND	W.
296	27	CFG4	28	CFG12	
d ui.	29	CFG5	30	CFG13	
	31	GND	32	GND	
efined undefined unde	33	CFG6	34	CFG14	
dull,	35	CFG7	36	CFG14	
	35	GND	38		
811.	39		-00	GND	ndefine
	39	VCCST_PWRGD	40	CLK_P	SINE
		PWRBTN	42	CLK_N	"ger.
	43	1.05V	44	1.05V	011.
undefined und	45	PWR_DEBUG	46	PLT_RESET	
ed	47	SYS_PWROK	48	PM_RESET	
Sine	49	GND	50	GND	
"uge"	51	SMB_DATA	52	TDO	
Jefined unden	53	SMB_CLK	54	TRST	
	55	NC	56	TDI	
ie.	57	TCK	58	TMS	
	59	GND	60	GND	717
idefined undefined un	defined	tefined undefi	ned un	eined undefined	unde
defined un	59 59	Junde	54 56 58 60 seration Intel® Core TM i5-538 Based on Intel® ISX Fo	defi	d undefi
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Serial Port (COM1/COM2)

Pin	Signal Name	Pin UITO	Signal Name
1.6	DCD	2	SIN
3	SOUT	4	DTR
5	GND	d Ull 6	DSR
7	RTS	8	CTS
9	NC	10	NC

Table 14. **Low Pin Count Bus (LPC1)**

Pin	Signal Name	Pin	Signal Name	
1	AD0	2	RESET	
3	AD1	4,000	FRAME	iefined un
5	AD2	6	3.3 V	Gine
7	AD3	8	GND	INOIS
9	CLK	10	NC	
Inverter Power (IN	VT1)	_	ined undefill.	
Pin	Signal Name			
1	BKL_PWR 12 V	defined ur	delli	
2	BKL_PWR 12 V	9 11		
3	BKL_ENABLE	sinec		
4	BKL_CONTROL	inge.		define

Inverter Power (INVT1)

	60.	
Pin	Signal Name	sined undefined undefined us
1	BKL_PWR 12 V	aden.
2	BKL_PWR 12 V	- dulle
3	BKL_ENABLE	sinet ed
4	BKL_CONTROL	nder.
5	GND	od uli
6	GND	and a sed to
LVDS Operating VD Pin	D Selection Power	(LCDPWR_SEL1)
1-2	+3.3 V (Default)	- defil's
3-4	+5 V	- d unit
5-6	+12 V	- sineo
	d undefined uni	Jefin defined undefinee
el® Cora™ i5-5250U Proce	esor Evaluation Kit	(LCDPWR_SEL1) April 2016 Document Number: 334089-001US
SX Form Factor Reference D	esign	April 2014
		April 2010 Document Number: 334089-001US

Table 16.

Jundefined undefin	Pin	Signal Name	sineo
edu	1-2	+3.3 V (Default)	nder.
defille	3-4	+5 V	ad ull
uno	5-6	+12 V	ine ined
d undefined undefined v	sined ull		sined underined and a second underined under und
40	nder.	,nde	ine defined
ie fine c		ined u.	ad uno
, unae			Leftinee
fine o		ed uli.	4 Unac
inder	defin		sineo
300	d unit		inder.
	Stines		red II.
	Inge	6	efin.
5th Generation Int	rel [®] Core TM i5-5350U Proces SX Form Factor Reference De	sor Evaluation Kit	inge,
	SX FORTH FACTOR Reference De	sign	April 2016 Document Number: 334089-001US
22/11		inde.	Document Number: 334089-00105
User Guide 22		sor Evaluation Kit esign	4 Unic
76,	410		20



LVDS Connector (LVDS1) Table 17.

	Pin	Signal Name	Pin Ulho	Signal Name
	1	VDD	2	VDD
	3	VDD	4	NC
	5	GND	6	GND
	7	DATA0-	8	DATA0+
indefined undefined unde	9	DATA1-	10	DATA1+
	11	DATA2-	12	DATA2+
defill	13	GND	14	GND
4 Unce	15	CLK1-	16	CLK1+
	17	DATA3-	18	DATA3+
detti	19	DATA4-	20	DATA4+
	21	DATA5-	22	DATA5+
	23	DATA6-	24	DATA6+
	25	GND	26	GND
ind	27	CLK2-	28	CLK2+
edu	29	DATA7-	30	DATA7+
4	·			· · · · · · · · · · · · · · · · · · ·

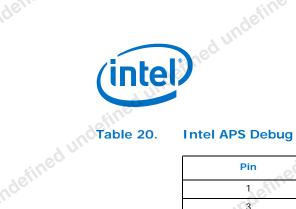
undefined und Table 18. RTC Battery Connector (J_RTC1)

Pin	Signal Name
1 6	Battery +
2	Battery -

Table 19.

~()	Signal Name	inde
1 41118	Battery +	1269 C
2	Battery -	defill
SATA Power (SATA	_PWR1)	ed undefined undefined sined undefi
Pin	Signal Name	18 tinec
1	+12 V	, unoc
2	GND	:ned
3	GND	defill
4	+5 V	unc
	4 under	indefine
		sined U.
dundefine	Jundefined	neration Intel® Core™ i5-5350U Processor Evaluation Kit Based on Intel® ISX Form Factor Reference Design User Guide 23

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Intel APS Debug Port (APS1)

	nois	26		_
Pin	Signal Name	Pin Juno.	Signal Name	ind ⁹
1	+3.3 A	2	SLP_S3	ed u.
3	+3.3 A	4	+3.3 A	Sine
5	SLP_S4	4 Ull 6	SLP_A	"uge"
7	NC	8	GND	J
9	RTC_RST	10	GND	
11	PWRBTN	12	GND	
13	RSTBTN	14	GND	

indefined undefined und **Debug Port (Debug1)**

Pin	Signal Name	Pin	Signal Name
UT	SPI_MISO	2062	SPI_MOSI
3	SPI_CS	4	SPI_CLK
5	GND	6	GPIO0
7	NC	8	GPIO1
9	I2C_SDA	10	I2C_SCL
11	SMB_ALERT	12	GND
13	SMB_DATA	14	SMB_CLK
15	NC	16	GND
17	+3.3A	18	+5A

undefined undefined uni Table 22. **SPI Programming Connector (SPI1)**

17	+3.3A	18	+5A
SPI Programming	Connector (SPI1)	4 undefin	
Pin	Signal Name	Pin	Signal Name
1	+3.3 V	2	GND
3	SPI_CS	4	SPI_CLK
5	SPI_MISO	6	SPI_MOSI
7	NC	8	DETECT

Jundefined undefined **System Fan Connector (FAN1)**

			_		
ed nii.	7	NC	8	DETECT	
Table 23.	System Fan Connec	tor (FAN1)	d undefined i	undefined undefin	<u>,</u> V
unc	Pin	Signal Name	4efine		
	Pill	Signal Name	1100		4611.
	ein ^e 1	GND	ed a		i nuo.
	2	+12 V	lin		
A.V	3	FAN_FB		defill.	
	4	FAN_PWM		4 Uno	
d undefined undefined t	·	defille			
ed m.		, uno		dell	
Sine			A		
	ofined undefin				69,
900	und		dell		istine
	ed		4 Ullie		
	defil.				eg n.
4.	UNC		le,,		16
5th Generation In	tel [®] Core TM i5-5350U Proces SX Form Factor Reference De	ssor Evaluation Kit		"uge,	
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		INO		der	
fine				nu	
767.					



Push-Buttons and LED Indicators

4.4.1 **Power-On Button**

The evaluation kit system has a single push-button POWER button. The POWER button enables or disables power to the entire evaluation kit system causing it to boot or shut down.

The location of the POWER button is shown in Table 24.

Table 24. **Push-Buttons Location Table**

Description	Reference Designator
Power button	PWR_SW1

4.4.2 **LED Indicators**

There are two LED indicators in the evaluation kit system: power button LED and standby LED. The power button LED is located at the POWER button (PWR_SW1) while the standby LED is located at LED1.

The location, power state, and color of the LED indicators are shown in Table 25.

Table 25. **LED Indicators Table**

Description	Reference Designator	Power State	Color
Standby LED	LED1	S4/S5	Red
Power button LED	PWR_SW1	S0	Blue

Configuration Settings 4.5

J_RTC1 — Clear CMOS or ME Settings

Clearing the contents of all BIOS or ME settings will restore the evaluation kit system to factory default values.

Note: J_RTC1 is connected to a coin battery by default.

To restore the BIOS settings:

- 1. Turn off the evaluation kit system, and unplug the power cord.
- 2. Remove the 3.3 V coin battery from J RTC1 for a few seconds, and then install the 3.3 V coin battery.
- 3. Turn on the evaluation kit system

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5.0 Thermal and Mechanical Design Information for the Evaluation Kit System

The evaluation Kit based on Intel[®] Intelligent System Extended (ISX) Reference Design offers a powerful computing performance in a compact chassis measuring 4.6×7.2 inch \times 1.7 inch.

Inside the chassis is a 4.4×6.1 inch motherboard. To meet the thermal requirements of the 5th generation ${\sf Intel}^{\circledR}$ CoreTM (U series) processor, the chassis is designed to ensure adequate airflow in order to support the thermal solution for the processor and critical components.

The evaluation board is enclosed in a full metal chassis. As this is a fanless system, the heat generated by the Intel[®] CoreTM i5-5350u Processor is dissipated to the chassis by means of conduction. The metal chassis acts as a heat sink.

Warning:

The surface of the chassis may get hot when the processor is operating in a high workload. The chassis surface is hot enough to burn when it comes into contact with human touch.

The evaluation kit system is designed to meet the 35? C ambient temperature.

As part of the Intel[®] ISX Form Factor Reference Design program, the mechanical design files for the chassis are mass production ready. The program also gives the flexibility for embedded design houses to modify the mechanical design according to their requirements, which provides opportunities to incorporate the reference design into their custom designs, gain the benefits that Intel[®] architecture provides, and accelerate their time-to-market.

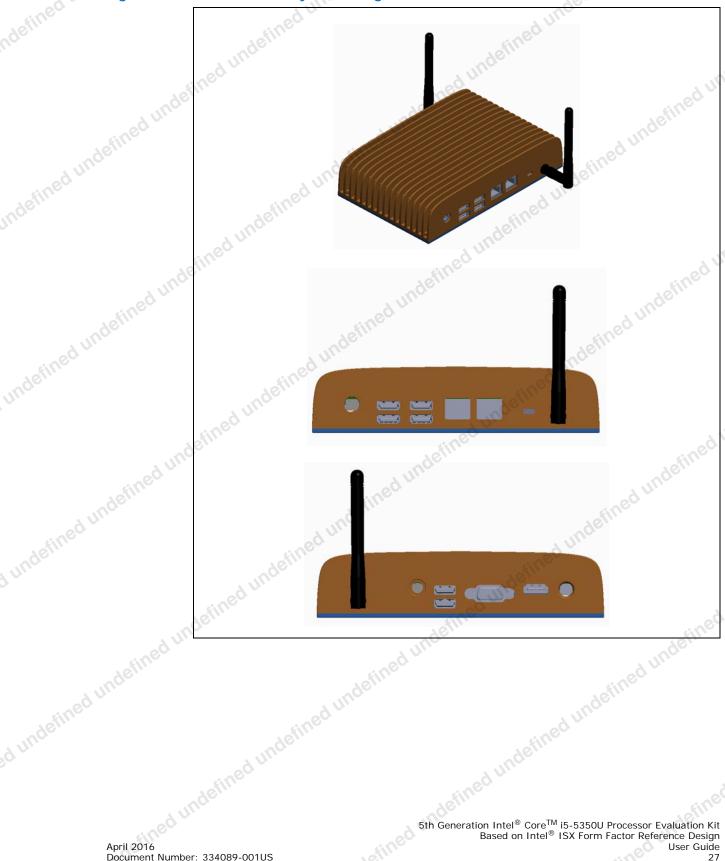
Note: For the 2D drawings and 3D design files, kindly refer to Table 3, CDI #557242.

5.1 Evaluation Kit System Design and Specification

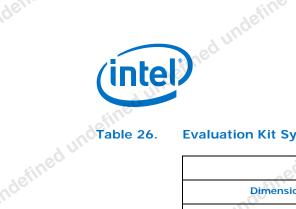
Figure 6 shows the design of the evaluation kit system while Table 26 shows its specification.



Figure 6. **Evaluation Kit System Design**



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Evaluation Kit System Specification

Table 26.	Evaluation Kit System Specific	cation	afine
ndefined un Table 26.	SYST	EM	Je.
uge,	Dimensions	4.6 × 7.2 × 1.7 inch	ed un
	Thickness	1.7 inch	d undefined unde
2	Weight	~760 g	ad une
4 Uno	TOP COVER		18 fine
Fined	Material	Aluminum	ined undefined un
inde.	Color	Copper brown (Pantone 876)	fined
ined to	Finishing	Sandblast	ge.
andefined undefined und	BOTTOM COVER		sined undefined und
71.	Material	Aluminum	de fine
	Color	Blue (Pantone 2727)	d uno
110	Finishing	Sandblast	Hined
sined to	FEATL	IRES	inde.
d undefined un	Security	Kensington lock slot	ined to
raed ur	VESA Mount	>19" Displays	ider.

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Disassembly and Reassembly Procedure

This section provides details regarding the following:

- Precautions and safety handling of the evaluation kit system
- Disassembly and Reassembly of the evaluation kit system

Precautions and Safety Handling of the evaluation Kit **System**

The evaluation kit system contains components that are static-sensitive. Electrostatic can cause underlying damages to the system, resulting in failures occurring weeks or months later. Therefore, Electrostatic Discharge (ESD) prevention is important when handling the system.

Observe the following precautions and safety handling before disassembling the evaluation kit system:

- Ensure that the working area is properly grounded using the highest level of ESD protection available. It is recommended to use a wrist strap, ground cords, a table mat, a floor mat, ESD shoes, and an ESD chair.
- Do not wear nylon clothing when handling the system.
- Before touching the system, touch an electrical ground to remove any electrostatic charge from the body that may have accumulated.
- If possible, handle the system's components by holding on to the package and not by the leads.
- Use ESD protection bags when storing or moving the system's components.
- Ensure that all power source is removed from the system.

Warning: Failing to comply with the proper grounding and handling procedures may cause damage to the evaluation kit system.

Evaluation Kit System Disassembly and Reassembly

It is not recommended to disassemble the evaluation kit system for repair purposes. If the system is faulty and requires repair, send it to the nearest Intel Service Center.

The following disassembly procedure should only be performed if necessary.

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Evaluation Kit Completed Assembly





Figure 8. **Evaluation Kit Exploded View**



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Evaluation Board Removal

1. Remove the four M3×6 screws from the bottom cover as shown in Figure 9.

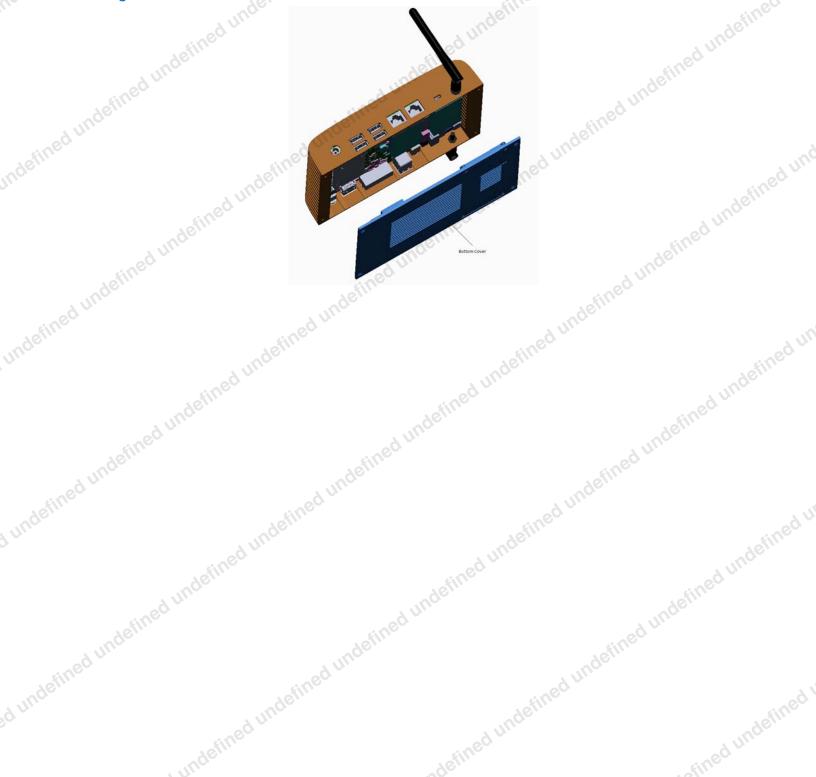
Figure 9. **Bottom Cover Screws Removal** undefined undefined undefined





2. Gently remove the bottom cover from the chassis.

Figure 10. **Bottom Cover Removal**



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3. Remove the six M3×4 screws from the evaluation board as shown in Figure 11.

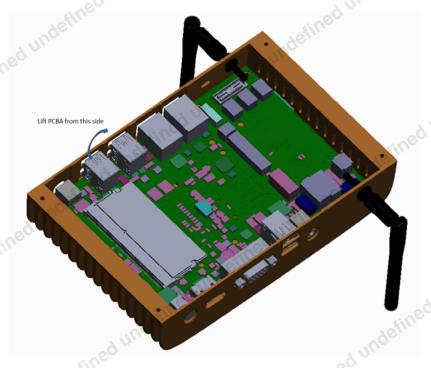
Figure 11. **Evaluation Board Screws Removal**





4. Remove the evaluation board by lifting it up at an angle as shown in Figure 12.

Figure 12. **Evaluation Board Removal**



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5th Generation Intel[®] CoreTM i5-5350U Processor Evaluation Kit Based on Intel[®] ISX Form Factor Reference Design User Guide April 2016 Document Number: 334089-001US



6.2.2 **Debug Ports Access**

The debug ports can be easily accessed without having to remove the bottom cover. Note:

1. Remove the four M2×4 screws as shown in Figure 13.

Figure 13. Remove the four screws



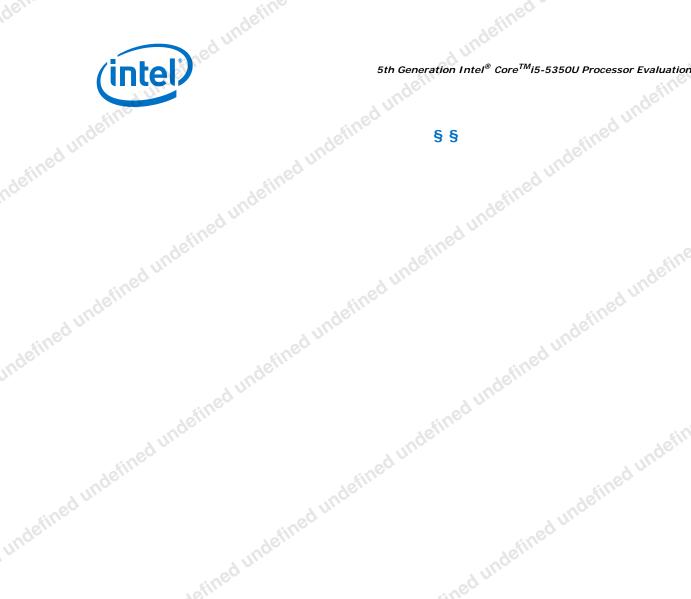


2. Gently remove the debug port access window from the chassis.

Figure 14. **Debug Port Access Window Removal**



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