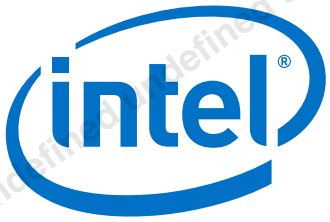

5th Generation Intel® Core™ i5-5350U Processor Evaluation Kit Based on Intel® ISX Form Factor Reference Design

Product User Guide

April 2016

Document Number: 334089-001US

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Revision History

Date	Revision	Description
April 2016	001	Initial release

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1.0 Introduction

1.1 About this Evaluation Kit

The 5th Generation Intel® Core™ i5-5350U Processor Evaluation Kit Based on Intel® Intelligent System Extended (ISX) Form Factor Reference Design is an Internet-of-Things (IoT) evaluation platform that can be used as-is by end-customers or can be customized by software vendors, driver developers, and system integrators.

The evaluation kit is based on the Intel® Intelligent System Extended (ISX) Form Factor Reference Design. It's a fanless design in a small form factor, made possible through process optimization, performance improvements, dynamic power, and thermal framework enhancements in the 5th generation Intel® Core™ (U series) processor.

The evaluation kit is a dual-channel DDR3L mobility platform that uses a new 4.4 × 6.1 inch board form factor. It's a full performance computing platform in the smallest form factor possible that supports the 5th generation Intel® Core™ (U series) processor in the BGA-type package. The Modular Board Design (MBD) of the Intel® ISX completes the critical signal paths for the processor and the supporting components according to Intel Design Guidelines.

This evaluation kit provides you with the necessary items to enable you to customize the board design to suit your requirements. Alternatively, for faster time to market, the board design can be used as-is out of the box.

Note: The 5th generation Intel® Core™ (U series) processor was formerly known as the Broadwell-U CPU.

1.2 Terminology

Table 1. Terminology

Term	Definition
APS	Automated Power Switch
BIOS	Basic Input Output System
CMOS	Refers to the non-volatile configuration memory in the PCH
CPU	Central Processing Unit
DDR3L	Double Data Rate Synchronous Dynamic Random Access Memory third generation (low power)
GND	Signal Ground
HDD	Hard disk drive
HDMI	High Definition Multimedia Interface
LAN	Local Area Network
LED	Light Emitting Diode
LPC	Low Pin Count
LVDS	Low-Voltage Differential Signaling
ME	Intel Management Engine
OS	Operating System
PCI	Peripheral Component Interface
PCIe*	Peripheral Component Interface Express*

Term	Definition
POST	Power-On Self Test
RTC	Real Time Clock
S3	“Save to RAM” Sleep State
S5	“Soft Off” Sleep State
SATA	Serial - Advanced Technology Attachment
SIO	Super Input Output
SLP	Sleep
SO-DIMM	Small Outline Dual In-line Memory Module
SSD	Solid State Drive
USB	Universal Serial Bus
VCC	Used to signify circuit logic voltage
VDDQ	Used to signify DIMM logic supply voltage
VGA	Video Graphics Array
VID	Voltage Identification
VTT	Used to signify signal termination voltage

1.3 Evaluation Board Parts

The evaluation board includes the following parts listed in Table 2 unless stated otherwise.

Table 2. List of Evaluation Board Parts

Evaluation Board Parts	Model	Quantity
4 GB 204-PIN DDR3L SDRAM Unbuffered SODIMM	Apacer (78.B2GCY.4000C)	2
mSATA SSD-64 G (half-size mPCIe*)	SANDISK (SDSA5FK-064 G)	1
MA 2.4 G Terminal antenna (external)	UNI LINK (TLB-2400-2.5B L)	2
Power adapter: Input: 100-240 V, AC 50/60 Hz Output:12 VDC, 4000 mA	KUANTECH (KSAH1200400W1UK)	1
Intel WiFi* module	Intel (6300 633AN.HMWG)	1
mPCIe* half to full-size extender bracket	SC2MPCIEEXT0B1100P	1
3G/WiFi* Mini PCIe* card (half-size mPCIe*)‡	Option (GTM671W)	1

Note: ‡ Optional and would require a separate order

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2.0 Getting Started

Before using the evaluation kit, verify that all the items listed in this section are received, and that the evaluation board is functioning by going through the following:

- Check the contents of the evaluation kit
- Inspect the evaluation board for any defects
- Power-on the evaluation board and verify that it is functioning correctly.

2.1 Before You Begin

Verify the contents of the evaluation kit and the condition of the evaluation board. If any of the items are missing or if the evaluation board is damaged, contact Intel before you proceed.

2.1.1 Check the Contents of the Evaluation Kit

The 5th Generation Intel® Core™ i5-5350U Processor Evaluation Kit Based on Intel® Intelligent System Extended (ISX) Form Factor Reference Design contains the following items:

- 5th Generation Intel® Core™ i5-5350U Processor Evaluation Kit Based on Intel® Intelligent System Extended (ISX) Form Factor Reference Design System
- 12 V@4 A DC Power Adapter
- System Drivers + User Guide (CD)
- Safety Flyer
- China RoHS Declaration
- WCL
- Intel® Evaluation Vehicles Terms and Conditions

2.1.2 Inspect the Evaluation Board

To check the evaluation board for damages, set it on an anti-static surface and inspect the evaluation board to ensure that the components are not missing, bent, or cracked.

Caution: The evaluation board may be damaged if it is not placed on an anti-static surface.

2.1.3 Power-on the Evaluation Board

Once the evaluation board is free from any visible defects, power-on the evaluation board and verify that the evaluation board is functioning correctly using the following steps:

1. Connect the supplied DC power adapter to the evaluation board.

   Note: Only use the DC power adapter supplied with the evaluation kit.
2. Press the **POWER BUTTON**.
3. Select the **Del** key as the system boots to enter the BIOS setup screen.
4. Check the time, date, and configuration settings. The default settings should be sufficient for most users with the exception of Intel SpeedStep® Technology. This feature is disabled by default and can be enabled in setup.
5. Save and exit the BIOS setup.

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6. The system will reboot and would then be ready for use.

Note: The evaluation board can be powered down with the following methods:

- Use the Windows* Start menu (or equivalent) shutdown option
- Press the **POWER BUTTTON** to begin the power-down process
- If the above does not work, hold down the **POWER BUTTON** for four seconds to asynchronously shut down the system (not recommended).

2.2 Reference Documents

Table 3. Technical Reference Documents

Document Description	Document Number/Location
5th Generation Intel® Core™ Processor Family and Intel® Core™ M Processor Family (Broadwell U/Y) – External Design Specification (EDS) Volume 1 of 2	514405
Broadwell Mobile U-Processor and Y-Processor External Design Specification (EDS) Volume 2 of 2	514525
5th Generation Intel® Core™ i5-5350u Processor Evaluation kit based on Intel® ISX Reference Design – System Reference Design Schematic and Board File	556749
5th Generation Intel® Core™ i5-5350u Processor Evaluation Kit Based on Intel® ISX Reference Design BIOS Image – BIOS Reference Code	557335
5th Generation Intel® Core™ i5-5350u Processor Evaluation kit based on Intel ISX Reference Design - Mechanical Reference Design Files	557242

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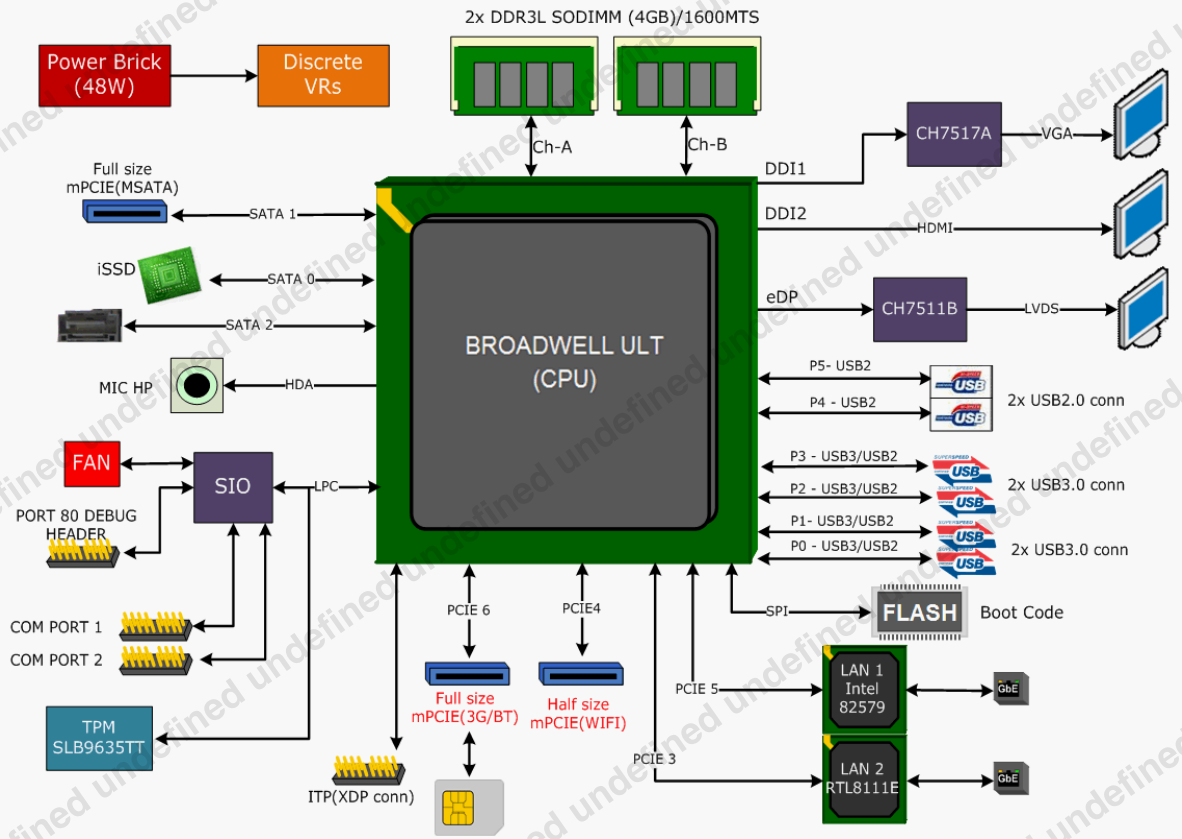
3.0 Evaluation Kit Overview

3.1 Block Diagram

Figure 1. Block Diagram of the Evaluation Kit



3.2 Features and Specifications

Table 4. Features and Specifications Table

Features	Specifications	Details
CPU	Family Model Package type TDP	Broadwell-U Mobile 5th Generation Intel® Core™ i7/i5/i3 Processor BGA 1168 Maximum up to 15 W
Memory	RAM type Maximum RAM size Maximum RAM speed RAM slot	DDR3L (1.35 V) 16GB[1] 1600MT/s 2
BIOS	SPI model	W25Q128FV; 128 M-bit SOIC-8 serial flash memory
EC/SIO	LPC-IO	IT8728F

Features	Specifications	Details
Display	Graphic type Integrated audio Maximum resolution Display option Others	Integrated Supported 3840 × 2160 at 60 Hz 1 × VGA connector 1 × Standard HDMI connector 1 × Dual-channel LVDS header 3 Display supported
Storage	mSATA (default) HDD/SSD iSSD (optional)[2]	Full-size Mini PCIe* slot Standard SATA 3.0 connector Soldered down iSSD (optional)[2]
Audio	Integrated HD Audio Codec Codec model Port	Supported Realtek ALC662 1 × 3.5 mm jack with line out and mic
USB	USB 3.0 USB 2.0	4 × USB 3.0 port 2 × USB 2.0 port
Network	Gigabit LAN port Intel LAN controller model 2nd LAN controller model 3G + WiFi* WiFi*	2 × RJ45 port Clarksville (i218-LM) with Intel® AMT support Realtek (RTL8111E) 1 × Full-size Mini PCIe slot + 1 × Micro SIM slot 1 × Half-size Mini PCIe slot
Serial Port	COM port header	2 × RS232 header
Power Supply	Mobile mode 48 W power adapter	12V @4 A input DC power
Others	Clocks RTC Processor VR TPM LPC ITP	Fully integrated clocking Battery-backed real-time clock ISL95812; Intel VR12.5 Serial VID (SVID) compliant SLB9635TT; TPM ver 1.2 1 × LPC debug header 1 × XDP debug port
System Form Factor Dimension	System Form Factor (W × L × H)	4.6” × 7.2” × 1.7”
PCB Dimensions	Board Form Factor Board Z-height PCB layer count	4.4” × 6.1” 1.61” 10 layers

1. The evaluation kit needs 64-bit Windows* installed to support 16 GB memory.
2. This feature's part is not populated on the system evaluation kits.

3.3 Power Management States

Table 5 lists the power management states that have been defined for the platform. The Controller Link (CL) operates at various power levels called M-states.

Table 5. Power Management States Description

State	Description
G0/S0	Full on mode. Display on.
G0/S0	Connected standby mode. Display off.
G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory (S3-Hot is not supported by the processor).
G1/S4	Suspend-to-Disk (STD). All power lost (except wakeup on PCH).
G2/S5	Soft off. All power lost (except wakeup on PCH). Total system reboot.
G3	Mechanical off. All power source (AC and battery) removed from the system.

The voltage of the evaluation board power nets at different activity states is shown in Table 6.

Table 6. Evaluation Board Power States

POWER NET	VOLTAGE	POWER WELL	ACTIVITY STATES
+VDCIN	12 V	ALWAYS ON	S0–S5
+V5 A	5 V	ALWAYS ON	S0–S5
+V3.3 A	3.3 V	ALWAYS ON	S0–S5
LAN1_V3P3	3.3 V	LAN	S0–S5
+V3.3 M	3.3 V	ME	S0–S5
+V1.05 M	1.05 V	ME	S0–S5
+VSM	1.355 V	DDR3L	S0–S3
+VSM_VTT	0.675 V	DDR3L	S0
+V12S	12 V	CORE	S0
+V5S	5 V	CORE	S0
+V3.3S	3.3 V	CORE	S0
+V1.05S	1.05 V	CORE	S0
+VCORE	1.5 V-1.85 V	CORE	S0
+V1.8S	1.8 V	EDP to LVDS	S0
+V1.5S	1.5 V	CORE	S0

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4.0 Evaluation Kit Setup

This section provides the following details:

- Lists the major components and their locations on the evaluation board, front panel and back panel
- Describes the pinouts of the headers
- Lists the LED indicator location and colors for different power states
- Provides the configuration settings to clear the BIOS.

4.1 Layout of the Board, Front Panel, and Back Panel

The following figures show the evaluation board, front panel, back panel layout, and the location of each major component.

Figure 2. Evaluation Board Top Layer

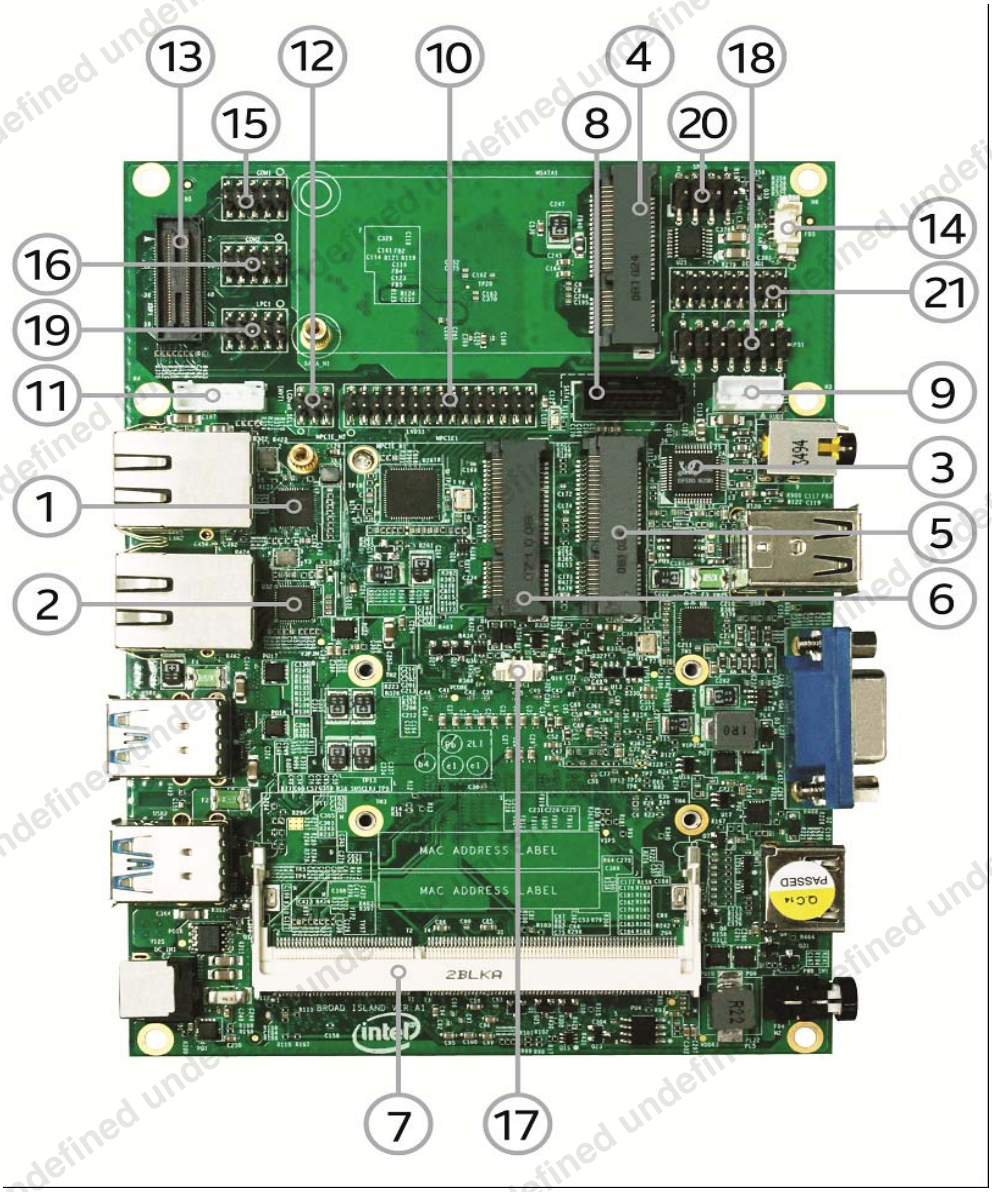


Figure 3. Evaluation Board Bottom Layer

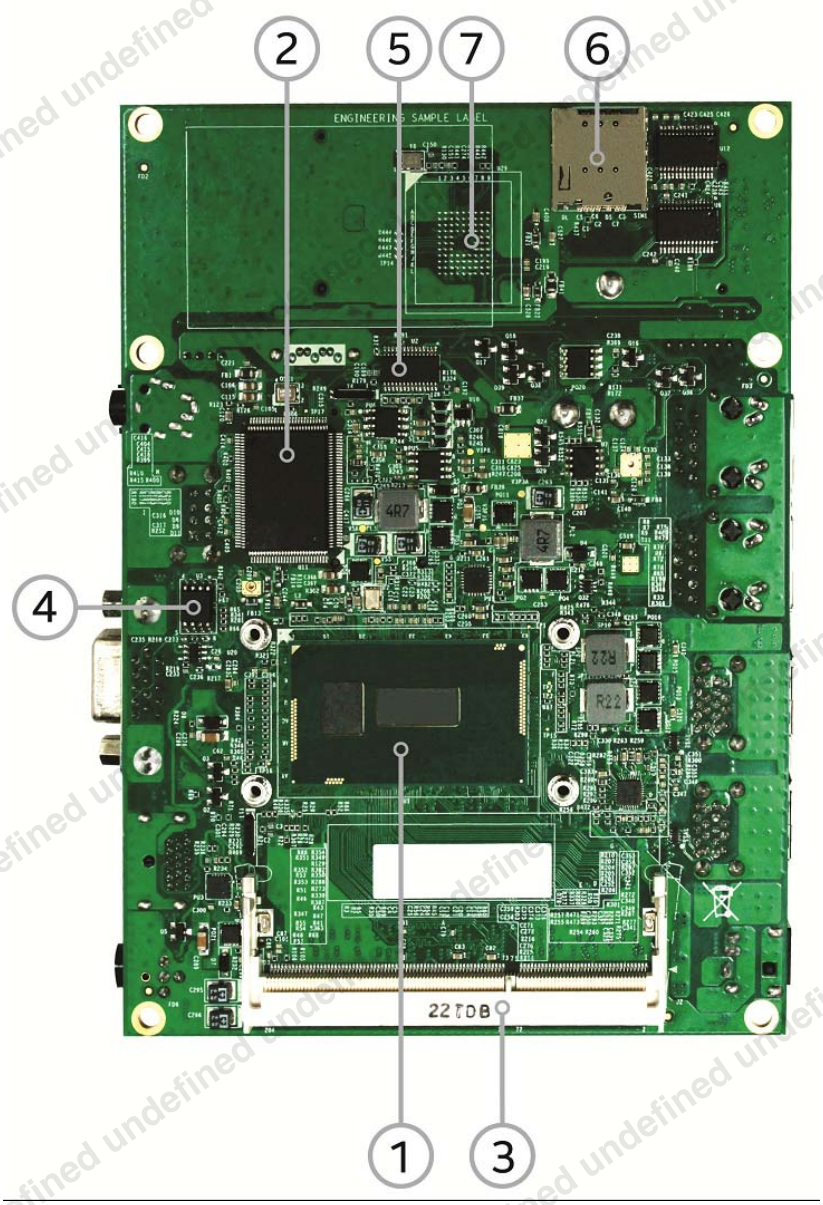


Figure 4. Front Panel

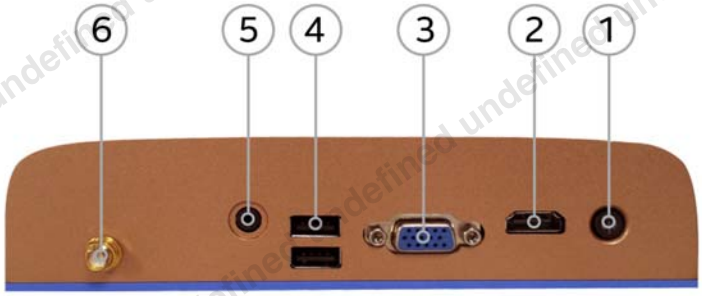
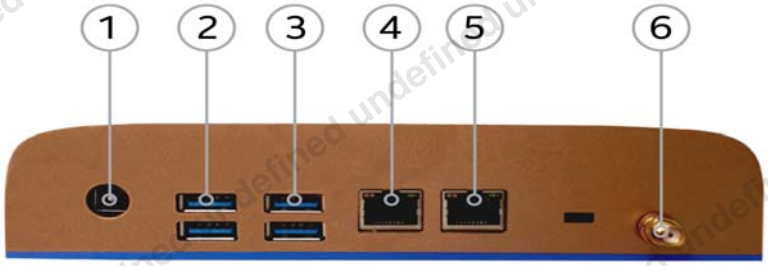


Figure 5. Back Panel



4.2 List of Components

The following tables list the major components and the reference designator of the evaluation board, front panel, and back panel.

Table 7. Evaluation Board Top Layer

Item Number	Description	Reference Designator
1	GbE controller 2 (RTL8111E)	U5
2	GbE controller 1 (Clarkville- i128LM)	U32
3	Audio Codec (ALC662)	U4
4	Mini PCIe connector (full size) - MSATA	MSATA1
5	3G + WiFi*	MPCIE2
6	Mini PCIe connector (half size)	MPCIE1
7	Non-ECC DDR3 sodimm connector (CH A)	J1
8	SATA 3.0 connector	SATA1
9	SATA power header	SATA_PWR1
10	LVDS signals header	LVDS1
11	LVDS inverter power	INVT1
12	LVDS VDD selection power jumper	LCDPWR_SEL1
13	XDP connector	XDP1
14	Fan 4-pin header	FAN1
15	Serial port header (COM 1)	COM1
16	Serial port header (COM 2)	COM2
17	RTC header	J_RTC1
18	APS header	APS1
19	Port 80 LPC header	LPC1
20	SPI flash header	SPI1
21	Debug header	DEBUG1

Table 8. Evaluation Board Bottom Layer

Item Number	Description	Reference Designator
1	CPU (Broadwell U)	U1
2	EC/SIO (IT8728F)	U11
3	Non-ECC DDR3 sodimm connector (CH B)	J2
4	SPI chip (W25Q128FV)	U3
5	TPM (SLB9635TT)	U2
6	Micro SIM slot	SIM1
7	ISSD (optional)	U29

Table 9. Front Panel

Item Number	Description	Reference Designator
1	Power button	PWR_SW1
2	HDMI connector	HDMI1
3	VGA connector	VGA1
4	Dual USB 2.0 stacked connector	USB3
5	Single port audio jack	AUD1
6	Antenna SMA connector 1	-

Table 10. Back Panel

Item Number	Description	Reference Designator
1	DC power jack	DC_IN1
2	Dual USB 3.0 stacked connector 1	USB2
3	Dual USB 3.0 stacked connector 2	USB1
4	Single LAN RJ45 connector 1	LAN1
5	Single LAN RJ45 connector 2	LAN2
6	Antenna SMA connector 2	-

4.3 Header Pinout Configuration

4.3.1 Evaluation Board Header Pinout

The following tables list the pinout configuration for the headers, and their corresponding signal names, on the evaluation board.

Table 11. Evaluation Board Connector Functions

Label	Function
XDP1	XDP Debug Port
COM1	COM1
COM2	COM2
LPC1	Low Pin Count Bus interface
INVT1	Inverter Power
LCDPWR_SEL1	LVDS Operating VDD Selection
LVDS1	LVDS Connector
J_RTC1	RTC Battery Connector
SATA_PWR1	SATA Power
APS1	APS Debug Port
Debug1	Debug Port
SPI1	SPI Flash Programming Connector
FAN1	System Fan Connector

Table 12. XDP Debug Port (XDP1)

Pin	Signal Name	Pin	Signal Name
1	GND	2	GND
3	PREQ	4	CFG17
5	PRDY	6	CFG16
7	GND	8	GND
9	CFG0	10	CFG8
11	CFG1	12	CFG9
13	GND	14	GND
15	CFG2	16	CFG10
17	CFG3	18	CFG11
19	GND	20	GND
21	BPM0	22	CFG19
23	BPM1	24	CFG18
25	GND	26	GND
27	CFG4	28	CFG12
29	CFG5	30	CFG13
31	GND	32	GND
33	CFG6	34	CFG14
35	CFG7	36	CFG15
37	GND	38	GND
39	VCCST_PWRGD	40	CLK_P
41	PWRBTN	42	CLK_N
43	1.05V	44	1.05V
45	PWR_DEBUG	46	PLT_RESET
47	SYS_PWROK	48	PM_RESET
49	GND	50	GND
51	SMB_DATA	52	TDO
53	SMB_CLK	54	TRST
55	NC	56	TDI
57	TCK	58	TMS
59	GND	60	GND

Table 13. Serial Port (COM1/COM2)

Pin	Signal Name	Pin	Signal Name
1	DCD	2	SIN
3	SOUT	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	NC	10	NC

Table 14. Low Pin Count Bus (LPC1)

Pin	Signal Name	Pin	Signal Name
1	AD0	2	RESET
3	AD1	4	FRAME
5	AD2	6	3.3 V
7	AD3	8	GND
9	CLK	10	NC

Table 15. Inverter Power (INVT1)

Pin	Signal Name
1	BKL_PWR 12 V
2	BKL_PWR 12 V
3	BKL_ENABLE
4	BKL_CONTROL
5	GND
6	GND

Table 16. LVDS Operating VDD Selection Power (LCDPWR_SEL1)

Pin	Signal Name
1-2	+3.3 V (Default)
3-4	+5 V
5-6	+12 V

Table 17. LVDS Connector (LVDS1)

Pin	Signal Name	Pin	Signal Name
1	VDD	2	VDD
3	VDD	4	NC
5	GND	6	GND
7	DATA0-	8	DATA0+
9	DATA1-	10	DATA1+
11	DATA2-	12	DATA2+
13	GND	14	GND
15	CLK1-	16	CLK1+
17	DATA3-	18	DATA3+
19	DATA4-	20	DATA4+
21	DATA5-	22	DATA5+
23	DATA6-	24	DATA6+
25	GND	26	GND
27	CLK2-	28	CLK2+
29	DATA7-	30	DATA7+

Table 18. RTC Battery Connector (J_RTC1)

Pin	Signal Name
1	Battery +
2	Battery -

Table 19. SATA Power (SATA_PWR1)

Pin	Signal Name
1	+12 V
2	GND
3	GND
4	+5 V

Table 20. Intel APS Debug Port (APS1)

Pin	Signal Name	Pin	Signal Name
1	+3.3 A	2	SLP_S3
3	+3.3 A	4	+3.3 A
5	SLP_S4	6	SLP_A
7	NC	8	GND
9	RTC_RST	10	GND
11	PWRBTN	12	GND
13	RSTBTN	14	GND

Table 21. Debug Port (Debug1)

Pin	Signal Name	Pin	Signal Name
1	SPI_MISO	2	SPI_MOSI
3	SPI_CS	4	SPI_CLK
5	GND	6	GPIO0
7	NC	8	GPIO1
9	I2C_SDA	10	I2C_SCL
11	SMB_ALERT	12	GND
13	SMB_DATA	14	SMB_CLK
15	NC	16	GND
17	+3.3A	18	+5A

Table 22. SPI Programming Connector (SPI1)

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	2	GND
3	SPI_CS	4	SPI_CLK
5	SPI_MISO	6	SPI_MOSI
7	NC	8	DETECT

Table 23. System Fan Connector (FAN1)

Pin	Signal Name
1	GND
2	+12 V
3	FAN_FB
4	FAN_PWM

4.4 Push-Buttons and LED Indicators

4.4.1 Power-On Button

The evaluation kit system has a single push-button POWER button. The POWER button enables or disables power to the entire evaluation kit system causing it to boot or shut down.

The location of the POWER button is shown in Table 24.

Table 24. Push-Buttons Location Table

Description	Reference Designator
Power button	PWR_SW1

4.4.2 LED Indicators

There are two LED indicators in the evaluation kit system: power button LED and standby LED. The power button LED is located at the POWER button (PWR_SW1) while the standby LED is located at LED1.

The location, power state, and color of the LED indicators are shown in Table 25.

Table 25. LED Indicators Table

Description	Reference Designator	Power State	Color
Standby LED	LED1	S4/S5	Red
Power button LED	PWR_SW1	S0	Blue

4.5 Configuration Settings

4.5.1 J_RTC1 — Clear CMOS or ME Settings

Clearing the contents of all BIOS or ME settings will restore the evaluation kit system to factory default values.

Note: J_RTC1 is connected to a coin battery by default.

To restore the BIOS settings:

1. Turn off the evaluation kit system, and unplug the power cord.
2. Remove the 3.3 V coin battery from J_RTC1 for a few seconds, and then install the 3.3 V coin battery.
3. Turn on the evaluation kit system.

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5.0 Thermal and Mechanical Design Information for the Evaluation Kit System

The evaluation Kit based on Intel® Intelligent System Extended (ISX) Reference Design offers a powerful computing performance in a compact chassis measuring 4.6 × 7.2 inch × 1.7 inch.

Inside the chassis is a 4.4 × 6.1 inch motherboard. To meet the thermal requirements of the 5th generation Intel® Core™ (U series) processor, the chassis is designed to ensure adequate airflow in order to support the thermal solution for the processor and critical components.

The evaluation board is enclosed in a full metal chassis. As this is a fanless system, the heat generated by the Intel® Core™ i5-5350u Processor is dissipated to the chassis by means of conduction. The metal chassis acts as a heat sink.

Warning: The surface of the chassis may get hot when the processor is operating in a high workload. The chassis surface is hot enough to burn when it comes into contact with human touch.

The evaluation kit system is designed to meet the 35? C ambient temperature.

As part of the Intel® ISX Form Factor Reference Design program, the mechanical design files for the chassis are mass production ready. The program also gives the flexibility for embedded design houses to modify the mechanical design according to their requirements, which provides opportunities to incorporate the reference design into their custom designs, gain the benefits that Intel® architecture provides, and accelerate their time-to-market.

Note: For the 2D drawings and 3D design files, kindly refer to Table 3, CDI #557242.

5.1 Evaluation Kit System Design and Specification

Figure 6 shows the design of the evaluation kit system while Table 26 shows its specification.

Figure 6. Evaluation Kit System Design

Table 26. Evaluation Kit System Specification

SYSTEM	
Dimensions	4.6 × 7.2 × 1.7 inch
Thickness	1.7 inch
Weight	~760 g
TOP COVER	
Material	Aluminum
Color	Copper brown (Pantone 876)
Finishing	Sandblast
BOTTOM COVER	
Material	Aluminum
Color	Blue (Pantone 2727)
Finishing	Sandblast
FEATURES	
Security	Kensington lock slot
VESA Mount	>19” Displays

Note: Embedded design houses have the flexibility to modify the mechanical design specifications according to their requirements.

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6.0 Disassembly and Reassembly Procedure

This section provides details regarding the following:

- Precautions and safety handling of the evaluation kit system
- Disassembly and Reassembly of the evaluation kit system

6.1 Precautions and Safety Handling of the evaluation Kit System

The evaluation kit system contains components that are static-sensitive. Electrostatic can cause underlying damages to the system, resulting in failures occurring weeks or months later. Therefore, Electrostatic Discharge (ESD) prevention is important when handling the system.

Observe the following precautions and safety handling before disassembling the evaluation kit system:

- Ensure that the working area is properly grounded using the highest level of ESD protection available. It is recommended to use a wrist strap, ground cords, a table mat, a floor mat, ESD shoes, and an ESD chair.
- Do not wear nylon clothing when handling the system.
- Before touching the system, touch an electrical ground to remove any electrostatic charge from the body that may have accumulated.
- If possible, handle the system's components by holding on to the package and not by the leads.
- Use ESD protection bags when storing or moving the system's components.
- Ensure that all power source is removed from the system.

Warning: Failing to comply with the proper grounding and handling procedures may cause damage to the evaluation kit system.

6.2 Evaluation Kit System Disassembly and Reassembly

It is not recommended to disassemble the evaluation kit system for repair purposes. If the system is faulty and requires repair, send it to the nearest Intel Service Center.

The following disassembly procedure should only be performed if necessary.

Figure 7. Evaluation Kit Completed Assembly

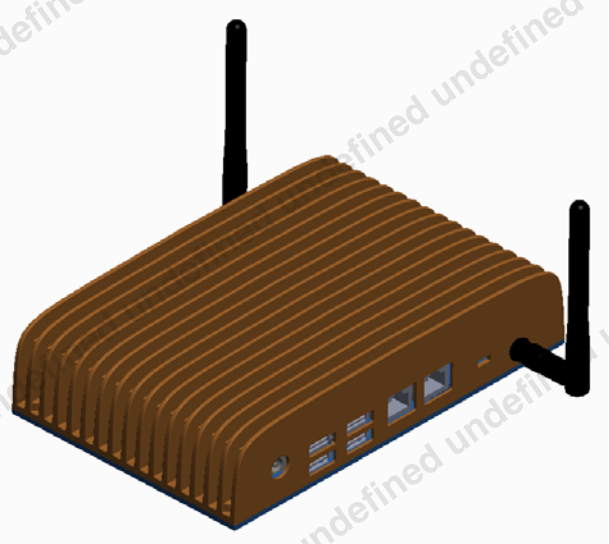
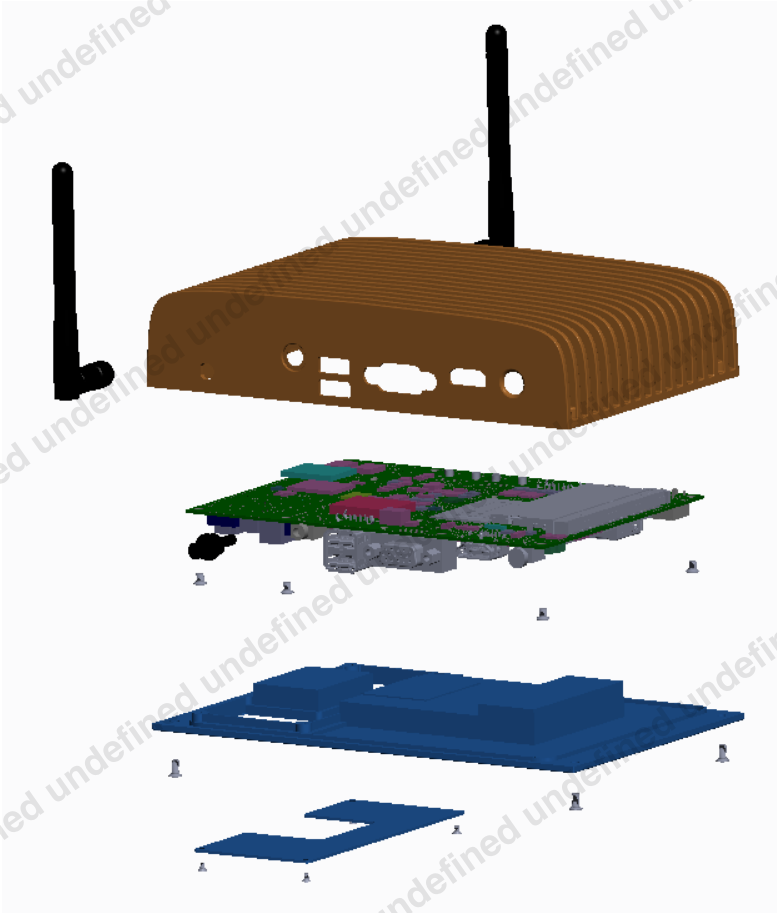


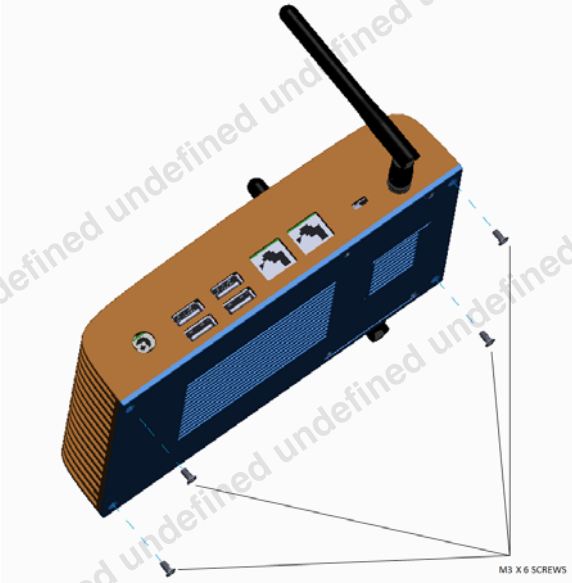
Figure 8. Evaluation Kit Exploded View



6.2.1 Evaluation Board Removal

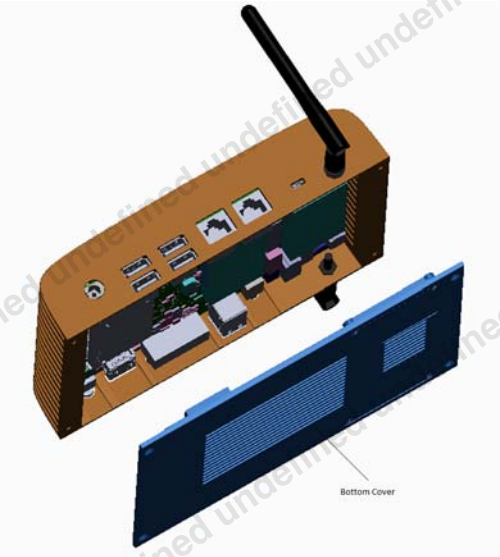
1. Remove the four M3×6 screws from the bottom cover as shown in Figure 9.

Figure 9. Bottom Cover Screws Removal



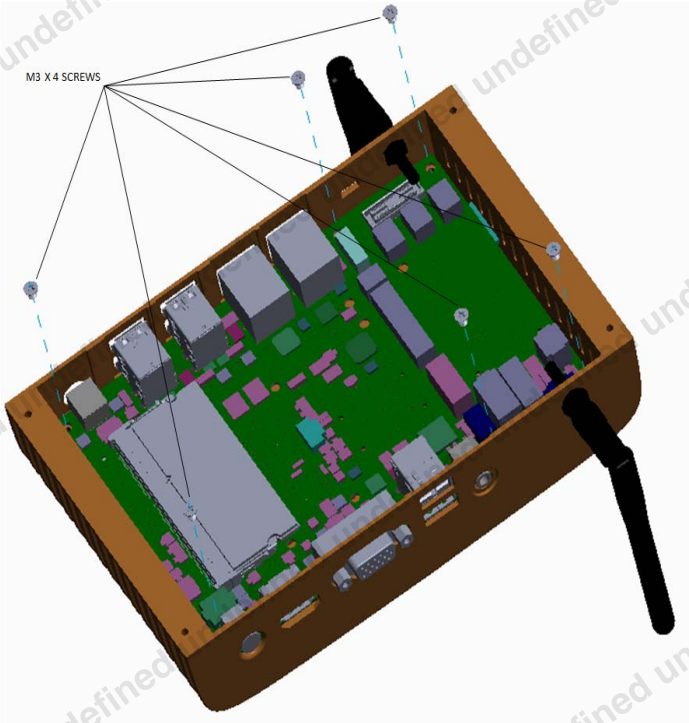
2. Gently remove the bottom cover from the chassis.

Figure 10. Bottom Cover Removal



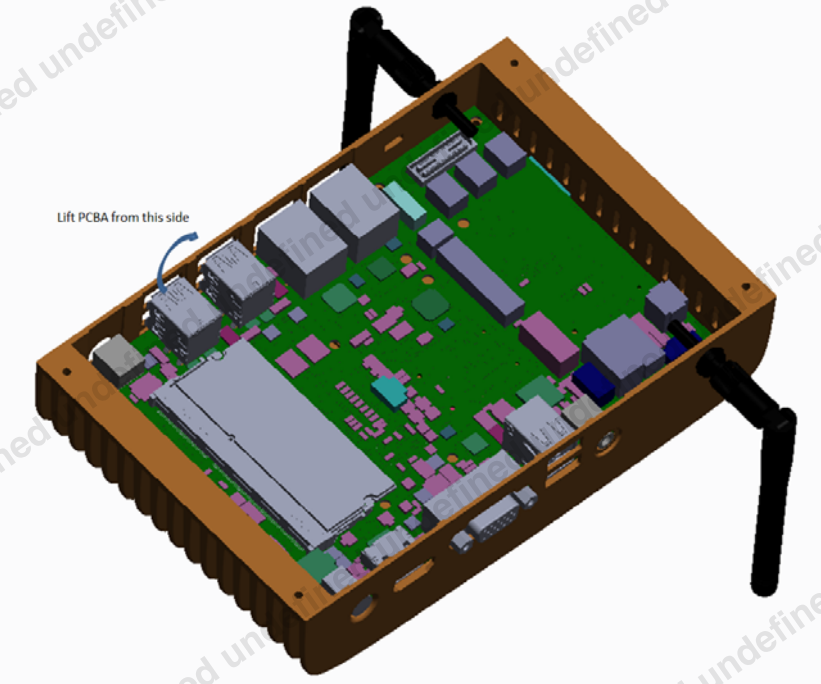
3. Remove the six M3×4 screws from the evaluation board as shown in Figure 11.

Figure 11. Evaluation Board Screws Removal



4. Remove the evaluation board by lifting it up at an angle as shown in Figure 12.

Figure 12. Evaluation Board Removal



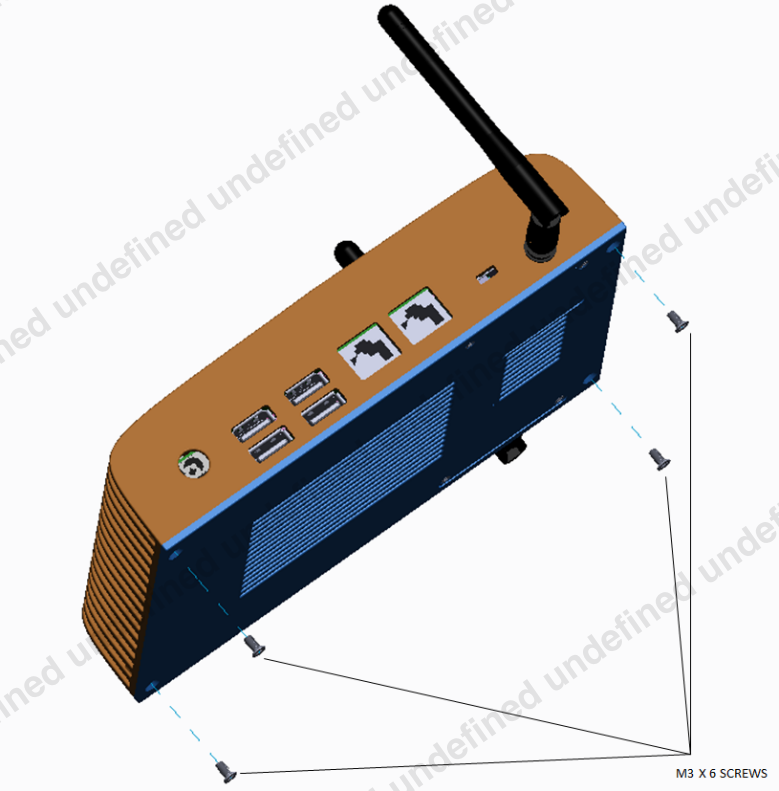
Note: This concludes the disassembly portion of the evaluation kit system. To assemble the evaluation kit system, follow the above disassembly procedure in reverse order.

6.2.2 Debug Ports Access

Note: The debug ports can be easily accessed without having to remove the bottom cover.

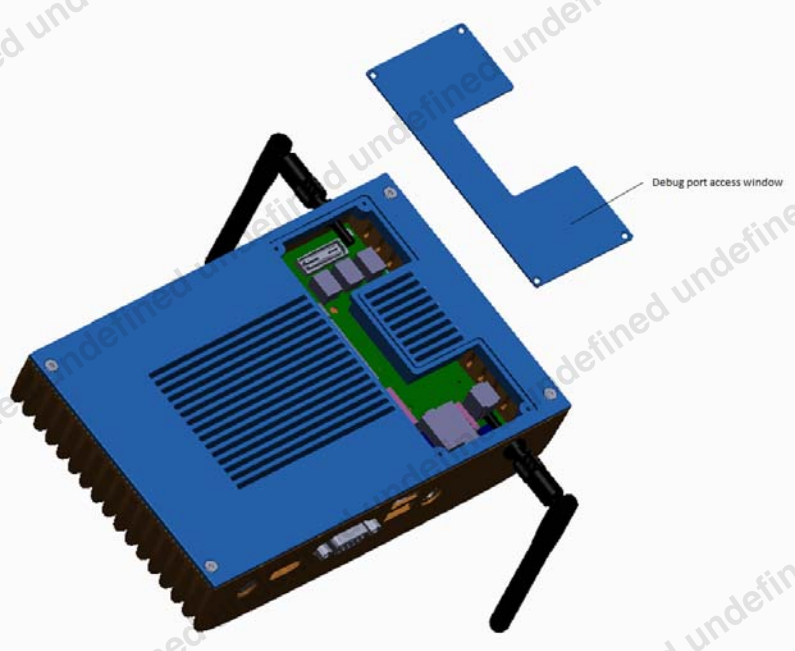
1. Remove the four M2×4 screws as shown in Figure 13.

Figure 13. Remove the four screws



2. Gently remove the debug port access window from the chassis.

Figure 14. Debug Port Access Window Removal



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