

Intel® Pentium® and Celeron® Processor N- and J- Series

Datasheet - Volume 1 of 3

For Volume 2 of 3 refer to Document ID: 334818

For Volume 3 of 3 refer to Document ID: 334819

September 2021

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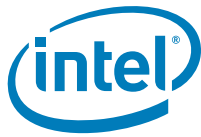
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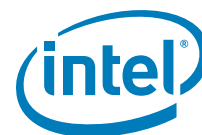
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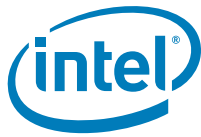


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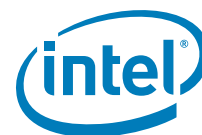
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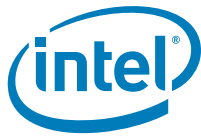
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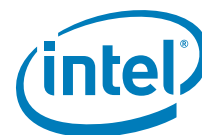
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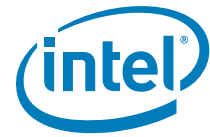


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Revision History

Document Number	Revision	Description	Date
334817	001	Initial release	August 2016



Document Number	Revision	Description	Date
334817	002	Chapter 1 - Introduction - Updated CSI D-PHY1.2 speed to 1.5Gb/s. - Updated Table 1-1 for SDR104 from 104MB/s to 100MB/s, to match Table 3-25 - Updated Figure 1-1 to further clarify processor architecture - Added Intel Legacy Block to in Section 1.2 Terminology Chapter 2- Physical Interface - Removed OSC_CLK_OUT4 - Added DEBUG_PORT description - Updated RTX_X1 Vih max value to 1.5V - Added note for GPIO degradation - Updated Table 2-35 and removed Community Offset column - Added note for Table 2-35 - Updated Table 2-2 Function from EXI to Intel® DCI - Corrected Table 2-35 to remove any GPIOs incorrectly shown as Fn1 and add any missing RSVD functions - Updated Table 2-35 - Buffer Type, Fn1, Fn4, Fn5, and Default Mode. - Updated Table 2-4 Platform Power Well Definitions. - Added GPIO_119 in Table 2-34 Hardware Straps - Updated Note 8 in Section 2.32 GPIO Multiplexing Chapter 3- Functional Description - Changed OSC_CLK_OUT[0:3] Clock frequency support. - Updated DMIC Clock Frequency - Updated Table 3-4 - Updated note 6 in Figure 3-4 - Updated Table 3-4 Channel Operating Rules - Updated Table 3-8 LPDDR4 x32 Configuration Support - Added note for Summary of Clock Signal - Updated and added note for SoC Clock Mapping - Updated Table 3-10 - Updated Table 3-23 - Updated Section 3.19 Thermal Management - Updated Table 3-26 eMMC Working Modes - Updated Table 3-31 - Updated section 3.31 - Updated Table 3-32Updated Table 3-36 Summary of Clock Signals Chapter 4- Reset and Power Sequence - Added Platform Initiated Shutdown section - Updated THERMTRIP Sequencing figure - Updated Table 4.1 Timing Requirement - Added Timing Label t5 in Table 4-1 - Added notes 6 and 7 under Table 4-1 - Removed EMMC_RST# from all timing diagram - Updated section 4.3.4 statement - Added note for 4.3.4 Platform Initiated Shutdown - Added Note in Figure 4-6 Chapter 5- Electrical Specification - Change SoC VID range as 450mV to 1.3V - Added Table with Absolute Max and min Values - Updated USB2 High-speed squelch detection threshold to 200mV - Added 3.3V GPIO Specification - Updated Table 5.33 - Added PCIE_CLKOUT in Section 5.6.17.1 - Added VOH and VOL for 3.3V in Section 5.6.19.1 - Added VOH and VOL for 3.3V in Table 5-37 and Table 5-41 - Updated Table 5-4 SoC Power Rail DC Specification and Iccmax - Updated Table 5-60 I2C SIO/PMIC/ISH/MIPI/DDI_DDC Signals DC	April 2020



Document Number	Revision	Description	Date
334817	003	Chapter 3- Functional Description - Updated Table 3-13. USB xHCI Controller Features Chapter 6- Ball Map and SoC Pin - Updated Figure 6-7. Ball Map LPDDR4—Left (63-42)	December 2020
334817	004	Chapter 2 - Physical Interfaces - Updated Table 2-28. SoC RTC Interface (Sheet 2 of 2) - Updated Table 2-33. Hardware Straps (Sheet 2 of 2) Chapter 3 - Functional Description - Updated Table 3-7. LPDDR4 Memory Configurations	September 2021

§ §



1 Introduction

Intel® Pentium® and Celeron® Processor N- and J- Series is the Intel Architecture (IA) SoC that integrates the next generation Intel processor Core, Graphics, Memory Controller, and I/O interfaces into a single System-on-Chip (SoC) solution.

Table 1-1 shows the system level features supported on SoC.

Refer to the subsequent chapters for detailed information on the functionality of the different interface blocks.

1.1 SoC Features

Table 1-1. SoC Features (Sheet 1 of 3)

Interface	Category	SoC
CPU	Number of Cores	4
	Burst Speed	Up to 2.6 GHz
	ULFM/LFM/HFM	400 MHz/800 MHz/Up to 2.0 GHz
Package	Type	31x24 mm ² Type-3
	I/O count	682
	Ball count	1296
	Minimum Ball pitch	0.593 mm
	Z-height	1.318 mm +/-0.092
Graphics	Gen	Gen9-LP
	Frequency	Up to 800 MHz
	Execution Units	Up to 18
Display	MIPI*-DSI ports	1x4 and 2x4 supported (D-PHY 1.1)
	Maximum MIPI*-DSI Resolution	1920x1080 @ 60 Hz (1x4) (No Compression) 2560x1600 @ 60 Hz (2 x4) (No compression)
	Maximum DSI Data rate	1.0 Gb/s
	DDI ports (external)	2x (DP 1.2 and HDMI 1.4b)
	Maximum DDI (external) Resolution	DP 1.2: Upto 4096x2160 @ 60 Hz HDMI 1.4b: Upto 3840x2160 @ 30 Hz
	eDP ports	1 (x4 eDP 1.3)
	Maximum eDP Resolution	Up to 3840x2160 @ 60 Hz
	Maximum DDI Data Rate	5.4 Gb/s (DP/eDP) 2.9Gb/s (HDMI)
Memory	Interface	2x64 DDR3L (non ECC) 4x32 LPDDR3 and LPDDR4 (non ECC)
	Supported transfer data rates (MT/s)	DDR3L and LPDDR3: 1333, 1600, and 1866 LPDDR4: 1600, 2133, 2400

Table 1-1. SoC Features (Sheet 2 of 3)

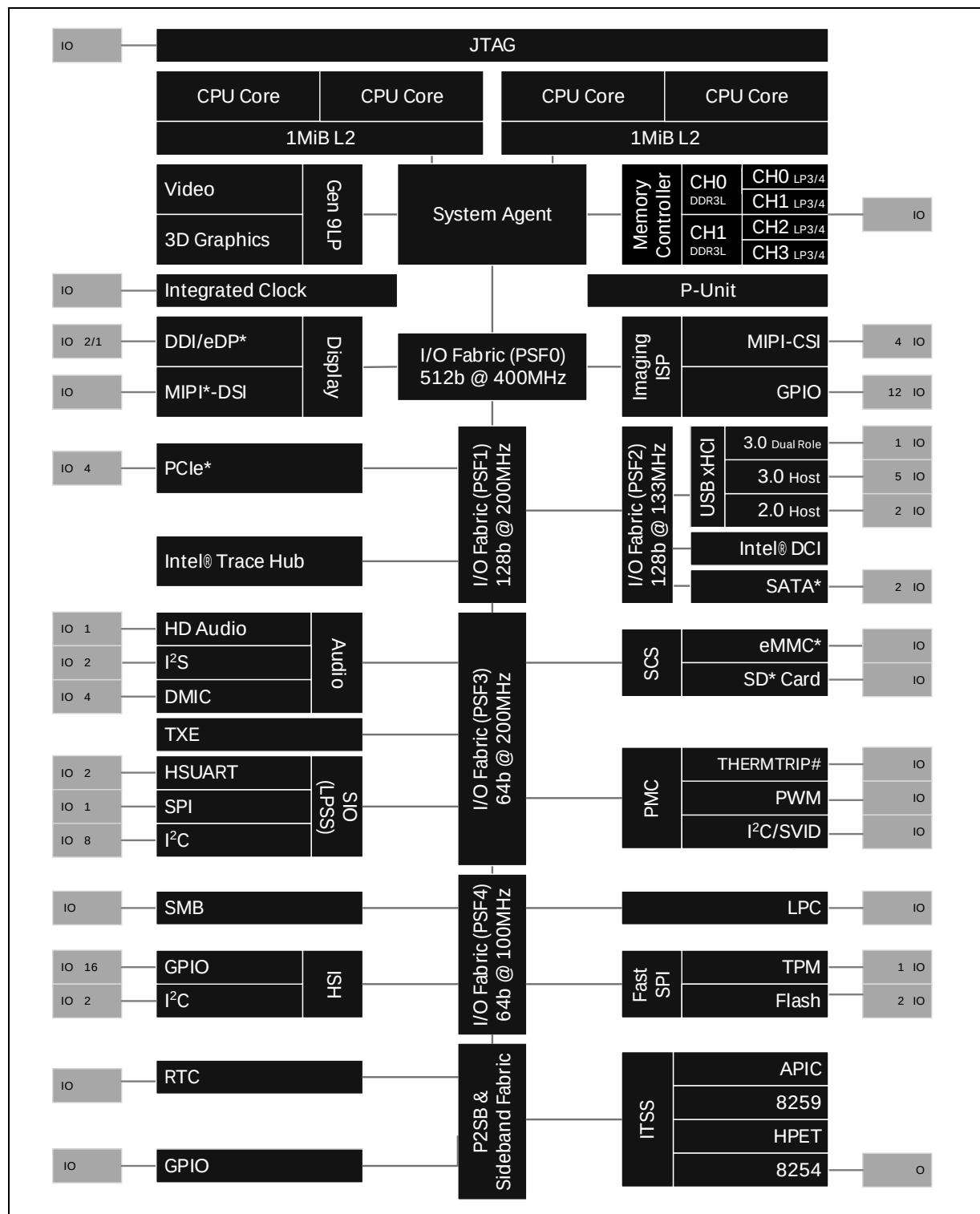
Interface	Category	SoC
Imaging [CSI D-PHY 1.1]	Number of lanes	4
	Speed	Up to 1.5Gb/s
	Still Capture	13MP @ 30fps
	Video Capture	1920x1080 @ 60fps
	Video HDR	1920x1080 @ 30fps
	Maximum Vector Unit	4
Imaging [CSI D-PHY1.2]	Number of Lanes	4
	Speed	Up to 1.5Gb/s
	Still Capture	13MP @ 30fps
	Video Capture	1920x1080 @ 60fps
	Video HDR	1920x1080 @ 30fps
	Maximum Vector Unit	4
Audio	Number of Ports	2x I ² S 4x DMIC 1x HD Audio (HDA/mHDA Codec)
	Maximum I ² S Speed	Master Clock: 19.2 MHz, Bit Clock: 12.28 MHz
USB	USB 3.0 Port	6 (1x USB Dual Role, 1 dedicated port, 3x multiplex with PCIe* 2.0, 1x multiplexed with SATA 3.0) Note: All Ports are backward compatible with USB 2.0
	Maximum USB 3.0 Speed	5Gb/s
	USB 2.0 Ports	2
	Maximum USB 2.0 Speed	480Mb/s
PCIe* Gen2	Ports	Up to 4 ports 6 Lanes (3x dedicated lanes and 3x multiplexed with USB 3.0)
	Maximum Speed	5 GT/s
SATA Gen3	Ports	2
	Maximum Speed	Gen 3 (6.0Gb/s)
Storage	SD Card	1x Port (SD3.01, SDR104/50/25/12 and DDR50)
	Maximum SD Card speed	Default Speed Mode=2.5MB/s High Speed Mode=25MB/s SDR50/DDR50 = 50MB/s SDR104 = 100MB/s
	eMMC	5.0 (HS400 DDR Mode) 4.5 (HS200 SDR Mode)
	Maximum eMMC speed	HS400 @ 400MB/s HS200 @ 200MB/s

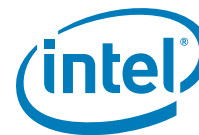


Table 1-1. SoC Features (Sheet 3 of 3)

Interface	Category	SoC
LPSS	I ² C Ports	8 3rd Party NFC is supported on this interface
	Maximum I ² C Maximum Speed	3.1 MHz
	HSUART	3 [1x Discrete GNSS(UART1), 1x Host OS Debug (UART2) and 1XGPIO(UART0))]
	Maximum HSUART speed	115.200kb/s (standard-speed 16550) 3.6864Mb/s (high-speed 16750)
	SPI	Controller: 1 Device supported: 1
	Maximum SPI Speed	25Mb/s
ISH	I ² C	3 (Sensors)
	Maximum I ² C Speed	1.7 MHz
	GPIO	16
iLB	Fast SPI	Controller: 1 Devices supported: 3 (FST_SPI supports upto 3 loads)
	Maximum Fast SPI Frequency	FST SPI = 50 MHz
PMC	I ² C (PMIC)	1
	Maximum I ² C speed	1.7 MHz
LPC	Ports	Devices Supported: 2
	Maximum Speed	25 MHz
SMBus	Ports	1
	Maximum Speed	100 KHz

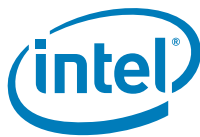
Figure 1-1. SoC Block Diagram





1.2 Terminology

Term	Description
AHCI	Advanced Host Controller Interface
ACPI	Advanced Configuration and Power Interface
CCM	Closely Coupled Memory
CCI	Camera Control Interface
CRU	Clock Reset Unit
CSI	Camera Serial Interface
CMOS	Complementary MOS
CSE	Converged Security Engine Note: This is the same as TXE3.0 - Trusted Execution Technology
DP*	DisplayPort*
DTS	Digital Thermal Sensor
DVS	Descriptive Video Services
DMIC	Digital Microphone
DnX	Download and Execute
EIOB	Electronic In/Out Board
EMI	Electro Magnetic Interference
eMMC	embedded Multi Media Card
eDP*	embedded DisplayPort*
HDCP	High-Bandwidth Digital Content Protection
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable. HDMI transmits all Advanced Television Systems Committee (ATSC) HDTV standards and supports 8-channel digital audio, with bandwidth to spare for future requirements and enhancements (additional details available at http://www.hdmi.org/).
HPET	High Precision Event Timer
HSMV	High Speed Medium Voltage
IGD	Internal Graphics Unit
ILB	Intel Legacy Block Note: This contains the ITSS (Interrupt Timer Subsystem), RTC & GPIO controllers
Intel® TXE	Intel® Trusted Execution Engine 3.0 Note: This is also called CSE - Converged Security Engine
IPC	Inter-Processor Communication
ISH	Integrated Sensor Hub
ISP	Image Signal Processor
LCD	Liquid Crystal Display
LPC	Low Pin Count
LPDDR	Low Power Dual Data Rate memory technology
LPE	Low Power Engine
LSMV	Low Speed Medium Voltage
MIPI*-CSI	MIPI*-Camera Serial Interface
MIPI*-DSI	MIPI*-Display Serial Interface
MPO	Multi Plane Overlay
MPEG	Motion Picture Experts Group



Term	Description
MSI	Message Signaled Interrupt. MSI is a transaction initiated outside the host, conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.
MSR	Model Specific Register, as the name implies, is model-specific and may change from processor model number (n) to processor model number (n+1). An MSR is accessed by setting ECX to the register number and executing either the RDMSR or WRMSR instruction. The RDMSR instruction will place the 64-bits of the MSR in the EDX: EAX register pair. The WRMSR writes the contents of the EDX: EAX register pair into the MSR.
MSHV	Medium Speed High Voltage
PCIe*	PCI Express*
PMC	Power Management Controller
PMU	Power Management Unit
PSP	Programmable Serial Protocol
Rank	A unit of DRAM corresponding to the set of SDRAM devices that are accessed in parallel for a given transaction. For a 64-bit wide data bus using 8-bit (x8) wide SDRAM devices, a rank would be eight devices. Multiple ranks can be added to increase capacity without widening the data bus, at the cost of additional electrical loading.
RTC	Real Time Clock
SATA	Serial ATA
SCI	System Control Interrupt—SCI is used in the ACPI protocol.
SDRAM	Synchronous Dynamic Random Access Memory
SERR	System Error. SERR is an indication that an unrecoverable error has occurred on an I/O bus.
SIO (LPSS)	Serial I/O (also called LPSS—Low Power Sub System)
SMBus	System Management Bus
SMC	System Management Controller or External Controller refers to a separate system management controller that handles reset sequences, sleep state transitions, and other system management tasks.
SMI	System Management Interrupt is used to indicate any of several system conditions (such as thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state related activity).
SPI	Serial Peripheral Interface
SSP	Synchronous Serial Protocol
TMDS	Transition-Minimized Differential Signaling. TMDS is a serial signaling interface used in HDMI to send visual data to a display. TMDS is based on low-voltage differential signaling with 8/10b encoding for DC balancing.
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator



1.3 SKU Information

Table 1-2. SoC SKU List

S-Spec	MM #	Stepping	Processor Number	Functional Core	Core Speed		Integrated Graphics Core Speed		TDP (W)
					Burst Frequency Mode (BFM) 2C/1C	High Frequency Mode (HFM)	Burst Frequency	Base Frequency	
R2Y9	951483	B-0	Pentium® N4200	4	2.4 GHz/2.5 GHz	1.1 GHz	750 MHz	200 MHz	6
R2YA	951484	B-0	Celeron® N3450	4	2.1 GHz/2.2 GHz	1.1 GHz	700 MHz	200 MHz	6
R2YB	951485	B-0	Celeron® N3350	2	2.3 GHz/2.4 GHz	1.1 GHz	650 MHz	200 MHz	6
R2ZA	951843	B-1	Pentium® J4205	4	2.5 GHz/2.6 GHz	1.5 GHz	800 MHz	250 MHz	10
R2Z9	951842	B-1	Celeron® J3455	4	2.2 GHz/2.3 GHz	1.5 GHz	750 MHz	250 MHz	10
R2Z8	951841	B-1	Celeron® J3355	2	2.4 GHz/2.5 GHz	2.0 GHz	700 MHz	250 MHz	10
R2Z5	951830	B-1	Pentium® N4200	4	2.4 GHz/2.5 GHz	1.1 GHz	750 MHz	200 MHz	6
R2Z6	951833	B-1	Celeron® N3450	4	2.1 GHz/2.2 GHz	1.1 GHz	700 MHz	200 MHz	6
R2Z7	951834	B-1	Celeron® N3350	2	2.3 GHz/2.4 GHz	1.1 GHz	650 MHz	200 MHz	6

§ §

2 Physical Interfaces

Many interfaces contain physical pins. These groups of pins make up the physical interfaces. Because of the large number of interfaces and the small size of the package, some interfaces share their pins with GPIOs, while others use dedicated physical pins. This chapter summarizes the physical interfaces, including the diversity in GPIO multiplexing options.

2.1 PCI Device ID

Table 2-1. PCI Configuration Matrix (Sheet 1 of 2)

Device ID	Device Description	Device	Function	Comments
0x5AF0	Host Bridge	0	0	
0x5A8C	DPTF	0	1	
0x5A84	Graphics and Display controller [18 EU]	2	0	
0x5A85	Graphics and Display controller [12 EU]	2	0	
0x5A88	Imagining Control Unit	3	0	
0x5A92	Primary to SideBand Bridge	13	0	
0x5A94	PMC (Power Management Controller)	13	1	
0x5A96	Fast SPI	13	2	
0x5AEC	Shared SRAM	13	3	
0x5A98	High Definition Audio	14	0	
0x5A9A	TXE HECI1	15	0	
0x5A9C	TXE HECI2	15	1	
0x5A9E	TXE HECI3	15	2	
0x5AA2	Integrated Sensor Hub (ISH)	17	0	
0x5AE0	SATA	18	0	
0x5AD8	PCIe*-A 0	19	0	
0x5AD9	PCIe*-A 1	19	1	
0x5ADA	PCIe*-A 2	19	2	
0x5ADB	PCIe*-A 3	19	3	
0x5AD6	PCIe*-B 0	20	0	
0x5AD7	PCIe*-B 1	20	1	
0x5AA8	USB-Host (xHCI)	21	0	
0x5AAA	USB-Device (xDCI)	21	1	
0x5AAC	I ² C 0	22	0	SIO/LPSS
0x5AAE	I ² C 1	22	1	SIO/LPSS
0x5AB0	I ² C 2	22	2	SIO/LPSS
0x5AB2	I ² C 3	22	3	SIO/LPSS

**Table 2-1. PCI Configuration Matrix (Sheet 2 of 2)**

Device ID	Device Description	Device	Function	Comments
0x5AB4	I ² C 4	23	0	SIO/LPSS
0x5AB6	I ² C 5	23	1	SIO/LPSS
0x5AB8	I ² C 6	23	2	SIO/LPSS
0x5ABA	I ² C 7	23	3	SIO/LPSS
0x5ABC	UART 0	24	0	SIO/LPSS
0x5ABE	UART 1	24	1	SIO/LPSS
0x5AC0	UART 2	24	2	SIO/LPSS
0x5AEE	UART 3	24	3	SIO/LPSS
0x5AC2	SPI 0	25	0	SIO/LPSS
0x5AC4	SPI 1	25	1	SIO/LPSS
0x5AC6	SPI 2	25	2	SIO/LPSS
0x5ACA	SD Card	27	0	
0x5ACC	eMMC*	28	0	
0x5AE8	LPC	31	0	
0x5AD4	SMBus	31	1	

2.2 Buffer Type Definitions

Table 2-2. Buffer Type Definitions

Buffer Type	Buffer Description
MIPI-PHY	1.05V tolerant buffer type
MOD PHY	1.24V tolerant buffer type (USB3, PCIe* and SATA)
Display PHY	1.05V tolerant buffer type
MIPI-DPHY	1.24V tolerant buffer type
USB2 PHY	3.3V tolerant buffer type
PCIe* PHY	1.0V tolerant PCIe* PHY buffer type
RTC PHY	3.3V tolerant RTC PHY buffer type
DDR3L PHY	1.35V tolerant buffer type
LPDDR3	1.2V tolerant buffer type
CLK PHY	1.0V tolerant buffer type
Analog	Analog pins that do not have specific digital requirements. Often used for circuit calibration or monitoring
GPIO	1.8V and 3.3V tolerant GPIO Buffer type

2.3 Power Well Definitions

Table 2-3. Platform Power Well Definitions

Power Type	Voltage Range (V)	Power Well Description	Power System States
VCC_VCGI	0.45–1.3	Variable voltage supply to CPU and Graphics Core and ISP logic	S0
VNN_SVID	0.45–1.3	Variable voltage supply to other (non core) logic	S0
VCCIOA	0.45–1.3	Variable voltage supply to DDR PHY logic	S0
VCCRAM_1P05	1.05	Fixed voltage rail for SRAM Logic	S0
VCCRAM_1P05_IO	1.05	Fixed voltage rail for I/O Logic	S0
VCC_1P05_INT	1.05	Fixed voltage rail for Internal Logic	S0
VDD2_1P24_CPU	1.24	Fixed voltage rail for SoC L2	S0–S5
VDD2_1P24_AUD_ISH_PLL	1.24	Fixed voltage rail for Audio & ISH I/O Logic and PLLs	S0–S5
VDD2_1P24_USB2	1.24	Fixed voltage rail for USB2 I/O	S0–S5
VDD2_V1P24_DSI_CSI	1.24	Fixed voltage rail for MIPI I/Os	S0–S5
VCC_1P8V_A	1.8	Fixed voltage rail for all GPIOs	S0–S5
VDDQ	1.35	Fixed voltage rail for DDR3 IO	S0–S3
	1.2	Fixed voltage rail for LPDDR3 IO	S0–S3
	1.1	Fixed voltage rail for LPDDR4 IO	S0–S3
VCC_3P3V_A	3.3	Fixed voltage rail for GPIO, I/O logic, and USB2 PHY	S0–S5
VCC_RTC_3P3V	3.3	Fixed Voltage rail for RTC (Real Time Clock)	S0–G3

2.4 Memory Interface Signals

2.4.1 DDR3L Interface Signals

Table 2-4. DDR3L System Memory Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
MEM_CH0/CH1_DQ[63:0]	I/O	VDDQ	DDR3L PHY	Data Buses: Data signals interface to the SDRAM data buses.
MEM_CH0/CH1_DQSP[7:0] MEM_CH0/CH1_DQSN[7:0]	I/O	VDDQ	DDR3L PHY	Data Strobes: Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.
MEM_CH0/CH1_CLKP[1:0] MEM_CH0/CH1_CLKN[1:0]	I/O	VDDQ	DDR3L PHY	SDRAM Differential Clock: Differential clocks signal pairs, pair per rank. The crossing of the positive edge of MEM_CH0/CH1_CLKP and the negative edge of their complement MEM_CH0/CH1_CLKN are used to sample the command and control signals on the SDRAM.
MEM_CH0/CH1_CKE[1:0]	O	VDDQ	DDR3L PHY	Clock Enable: (1 per rank). These signals are used to: - Initialize the SDRAMs during power-up. - Power-down SDRAM ranks. - Place all SDRAM ranks into and out of self-refresh during STR (Suspend to RAM).

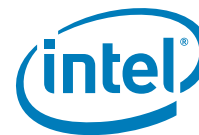


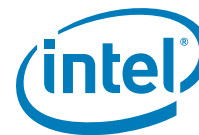
Table 2-4. DDR3L System Memory Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
MEM_CH0/CH1_CS[1:0]_N	O	VDDQ	DDR3L PHY	Chip Select: (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.
MEM_CH0/CH1_ODT[1:0]	O	VDDQ	DDR3L PHY	On Die Termination: (1 per rank). Active SDRAM Termination Control.
MEM_CH0/CH1_MA[15:0]	O	VDDQ	DDR3L PHY	Memory Address: These signals are used to provide the multiplexed row and column address to the SDRAM. - A10 is sampled during Read/Write commands to determine whether Auto pre-charge should be performed to the accessed bank after the Read/Write operation. HIGH: Auto pre-charge LOW: No Auto pre-charge. - A10 is sampled during a Pre-charge command to determine whether the Pre-charge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be pre-charged, the bank is selected by bank addresses. - A12 is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. HIGH: no burst chop
MEM_CH0_BA[2:0] MEM_CH1_BA[2:0]	O	VDDQ	DDR3L PHY	Bank Select: These signals define which banks are selected within each SDRAM rank.
MEM_CH0_CAS_N MEM_CH1_CAS_N	O	VDDQ	DDR3L PHY	CAS Control Signal: Column Address Select command signal
MEM_CH0_RAS_N MEM_CH1_RAS_N	O	VDDQ	DDR3L PHY	RAS Control Signal: Row Address Select command signal
MEM_CH0_VREFCA MEM_CH1_VREFCA	O	VDDQ	DDR3L PHY	Memory Reference Voltage for Command & Address
MEM_CH0_VREFDQ MEM_CH1_VREFDQ	O	VDDQ	DDR3L PHY	Memory Reference Voltage for DQ
MEM_CH0_RESET_N MEM_CH1_RESET_N	O	VDDQ	DDR3L PHY	Channel Reset Signal
MEM_CH0_WE_N MEM_CH1_WE_N	O	VDDQ	DDR3L PHY	Wake Enable signals
MEM_CH0_RCOMP MEM_CH1_RCOMP	N/A	VDDQ	DDR3L PHY	Channel Compensation

2.4.2 LPDDR3 Interface Signals

Table 2-5. LPDDR3 System Memory Signals

Signal Name	Dir.	I/O Voltage	Type	Description
MEM_CH0/CH1_DQA[31:0] MEM_CH0/CH1_DQB[31:0]	I/O	VDDQ	LPDDR3 PHY	Data Buses: Data signals interface to the SDRAM data buses.
MEM_CH0/CH1_DQSA[3:0]_P/N MEM_CH0/CH1_DQSB[3:0]_P/N	I/O	VDDQ	LPDDR3 PHY	Data Strokes: Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.
MEM_CH0_CLKA/B_P/N MEM_CH1_CLKA/B_P/N	I/O	VDDQ	LPDDR3 PHY	SDRAM Differential Clock: Differential clocks signal pairs, pair per rank. The crossing of the positive edge of MEM_CH0/CH1_CLKP and the negative edge of their complement MEM_CH0/CH1_CLKN are used to sample the command and control signals on the SDRAM.
MEM_CH0/CH1_CKE0A MEM_CH0/CH1_CKE1A MEM_CH0/CH1_CKE0B MEM_CH0/CH1_CKE1B	I	VDDQ	LPDDR3 PHY	Clock Enable: (1 per rank) These signals are used to: - Initialize the SDRAMs during power-up. - Power-down SDRAM ranks. - Place all SDRAM ranks into and out of self-refresh during STR.
MEM_CH0/CH1_CS[1:0]A_N MEM_CH0/CH1_CS[1:0]B_N	I	VDDQ	LPDDR3 PHY	Chip Select: (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.
MEM_CH0/CH1_CAA[9:0]	I/O	VDDQ	LPDDR3 PHY	Command Address: These signals are used to provide the multiplexed command and address to the SDRAM.
MEM_CH0/CH1_CAB[9:0]	I/O	VDDQ	LPDDR3 PHY	Command Address: These signals are used to provide the multiplexed command and address to the SDRAM.
MEM_CH0_VREFCA MEM_CH1_VREFCA	I/O	VDDQ	LPDDR3 PHY	Memory Reference Voltage for Command & Address
MEM_CH0_VREFDQ MEM_CH1_VREFDQ	I	VDDQ	LPDDR3 PHY	Memory Reference Voltage for DQ
MEM_CH0_RCOMP MEM_CH1_RCOMP	N/A	VDDQ	LPDDR3 PHY	Channel Compensation
MEM_CH0/CH1_ODT[A:B]	O	VDDQ	LPDDR3 PHY	On Die Termination: (1 per rank). Active SDRAM Termination Control.



2.4.3 LPDDR4 Interface Signals

Table 2-6. LPDDR4 System Memory Signals

Signal Name	Dir.	I/O Voltage	Type	Description
MEM_CH0/CH1_DQA[31:0] MEM_CH0/CH1_DQB[31:0]	I/O	VDDQ	LPDDR4 PHY	Data Buses: Data signals interface to the SDRAM data buses.
MEM_CH0/CH1_DQSA[3:0]_P/N MEM_CH0/CH1_DQSB[3:0]_P/N	I/O	VDDQ	LPDDR4 PHY	Data Strobes: Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.
MEM_CH0_CLKA/B_P/N MEM_CH1_CLKA/B_P/N	I/O	VDDQ	LPDDR4 PHY	SDRAM Differential Clock: Differential clocks signal pairs, pair per rank. The crossing of the positive edge of MEM_CH0/CH1_CLKP and the negative edge of their complement MEM_CH0/CH1_CLKN are used to sample the command and control signals on the SDRAM.
MEM_CH0/CH1_CKE[1:0]A MEM_CH0/CH1_CKE[1:0]B	I	VDDQ	LPDDR4 PHY	Clock Enable: (1 per rank) These signals are used to: • Initialize the SDRAMs during power-up. • Power-down SDRAM ranks. • Place all SDRAM ranks into and out of self-refresh during STR.
MEM_CH0/CH1_CS[1:0]A MEM_CH0/CH1_CS[1:0]B	I	VDDQ	LPDDR4 PHY	Chip Select: (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.
MEM_CH0/CH1_CAA[5:0]	I/O	VDDQ	LPDDR4 PHY	Command Address: These signals are used to provide the multiplexed command and address to the SDRAM.
MEM_CH0/CH1_CAB[5:0]	I/O	VDDQ	LPDDR4 PHY	Command Address: These signals are used to provide the multiplexed command and address to the SDRAM.
MEM_CH0_RCOMP MEM_CH1_RCOMP	N/A	VDDQ	LPDDR4 PHY	Channel Compensation
MEM_CH0/CH1_RESET_N	I	VDDQ	LPDDR4 PHY	Channel Reset: This signal is used to reset the individual channels

2.5 Digital Display Interface (DDI) Signals

Table 2-7. Digital Display Interface Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
DDIO_TXP[3:0]	O	V1P05	Display PHY	Port 0: Transmit Signals for DP/HDMI
DDIO_TXN[3:0]	O	V1P05	Display PHY	Port 0: Transmit Complement Signals for DP/HDMI
DDIO_AUXP	I/O	V1P05	Display PHY	Port 0: Display Port Auxiliary Channel for DP
DDIO_AUXN	I/O	V1P05	Display PHY	Port 0: Display Port Auxiliary Channel Complement for DP

Table 2-7. Digital Display Interface Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
DDIO_RCOMP_P/N	O	V1P05	Display PHY	Port 0/1: This signal is used for pre-driver slew rate compensation. Note: The SoC will use the eDP_RCOMP value for DDI Port 0/1 as well. Ensure that the eDP_RCOMP pin is populated with the correct value. There is no need to have this DDIO_RCOMP on the platform.
DDIO_DDC_SCL	I/O	V1P8	GPIO	Port 0: I ² C Clock for HDMI*
DDIO_DDC_SDA	I/O	V1P8	GPIO	Port 0: I ² C Data for HDMI*
DDI1_TXP[3:0]	O	V1P05	Display PHY	Port 1: Transmit Signals for DP/HDMI
DDI1_TXN[3:0]	O	V1P05	Display PHY	Port 1: Transmit Complement Signals for DP/HDMI
DDI1_AUXP	I/O	V1P05	Display PHY	Port 1: Display Port Auxiliary Channel for DP
DDI1_AUXN	I/O	V1P05	Display PHY	Port 1: Display Port Auxiliary Channel Complement for DP
DDI1_DDC_SCL	I/O	V1P8	GPIO	Port 1: I ² C Clock for HDMI
DDI1_DDC_SDA	I/O	V1P8	GPIO	Port 1: I ² C Data for HDMI
EDP_TXP[3:0]	O	V1P05	Display PHY	Transmit Signals for eDP*
EDP_TXN[3:0]	O	V1P05	Display PHY	Transmit Complement Signals for eDP*
EDP_AUXP	I/O	V1P05	Display PHY	Display Port Auxiliary Channel for eDP*
EDP_AUXN	I/O	V1P05	Display PHY	Display Port Auxiliary Channel Complement for eDP*
EDP_RCOMP_P/N	O	V1P05	Display PHY	This signal is used for pre-driver slew rate compensation.
PNL[0,1]_BKLCTL	I/O	V1P8	GPIO	Panel Backlight Brightness Control (for eDP/MDSI)
PNL[0,1]_BKLTEN	I/O	V1P8	GPIO	Panel Backlight Enable (for eDP/MDSI)
PNL[0,1]_VDDEN1	I/O	V1P8	GPIO	Panel Power Enable (for eDP/MDSI)
DDI[2:0]_HPD	I/O	V1P8	GPIO	Digital Display Interface Hot Plug Detect Note: These are multiplexed signals and need to be enabled through GPIO programming Note: DDI2 is a dedicated eDP port. Note: A logic inversion circuit with a mandatory pull up resistor is required on the platform

2.6 MIPI*-DSI Interface Signals

Table 2-8. MIPI*-DSI Interface Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
MDSI_A_CLKN	O	V1P24	MIPI*-DPHY	MIPI* Clock output for pipe A
MDSI_A_CLKP	O	V1P24	MIPI*-DPHY	MIPI* Clock complement output for pipe A
MDSI_A_DN[3:0]	I/O	V1P24	MIPI*-DPHY	MIPI* Data Lane 3:0 for Pipe A
MDSI_A_DP[3:0]	I/O	V1P24	MIPI*-DPHY	MIPI* Data Lane 3:0 complement for Pipe A
MDSI_C_CLKN	O	V1P24	MIPI*-DPHY	MIPI* Clock output for pipe C

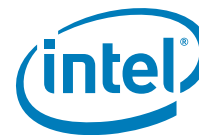


Table 2-8. MIPI*-DSI Interface Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
MDSI_C_CLKP	O	V1P24	MIPI*-DPHY	MIPI* Clock complement output for Pipe C
MDSI_C_DN[3:0]	I/O	V1P24	MIPI*-DPHY	MIPI* Data Lane 3:0 for Pipe C
MDSI_C_DP[3:0]	I/O	V1P24	MIPI*-DPHY	MIPI* Data Lane 3:0 complement for Pipe C
MDSI_RCOMP	I/O	V1P24	MIPI*-DPHY	This signal is used for pre-driver slew rate compensation. An external precision resistor of $150\ \Omega \pm 1\%$ should be connected between MDSI_RCOMP and GND.
MDSI_A_TE	I	V1P8	GPIO	MIPI*-DSI tearing effect signal (Port A)
MDSI_C_TE	I	V1P8	GPIO	MIPI*-DSI tearing effect signal (Port C)
MIPI_I ² C_SDA	I/O	V1P8	GPIO	I ² C Serial Data for MIPI Port
MIPI_I ² C_SCL	I/O	V1P8	GPIO	I ² C Serial Clock for MIPI Port

2.7 MIPI*-CSI2 (DPHY1.1) Signals

Table 2-9. MIPI*-CSI2 (DPHY1.1) Interface Signals

Signal Name	Dir.	I/O Voltage	Type	Description
MCSI_DN/P[0:3]	I	V1P24	MIPI*-DPHY	Four MIPI*-CSI Data Lanes
MCSI_CLKP_0 MCSI_CLKN_0 MCSI_CLKP_2 MCSI_CLKN_2	I	V1P24	MIPI*-DPHY	Two MIPI*-CSI Input clock lanes
MCSI_DPHY1.1_RCOMP	I/O	V1P24	MIPI*-DPHY	Resistor Compensation (D-PHY1.1): This signal is used for pre-driver slew rate compensation.

2.8 MIPI*-CSI2 (DPHY1.2) Signals

Table 2-10. SoC MIPI*-CSI2 (DPHY1.2) Interface Signals

Signal Name	Dir.	I/O Voltage	Type	Description
MCSI_RX_DATA[3:0]_P MCSI_RX_DATA[3:0]_N	I	V1P24	MIPI*-DPHY	Data: Four MIPI*-CSI Data Lanes
MCSI_RX_CLK[1:0]_P MCSI_RX_CLK[1:0]_N	I	V1P24	MIPI*-DPHY	Clocks: Two MIPI*-CSI Input clock lanes
MCSI_DPHY1.2_RCOMP	I/O	V1P24	MIPI*-DPHY	Resistor Compensation (D-PHY1.2): This signal is used for pre-driver slew rate compensation.

2.9 MIPI * Camera Sideband Signals

Table 2-11. SoC Camera Sideband Signals

Signal Name	Dir.	I/O Voltage	Type	Description
GP_CAMERASB0	I/O	V1P8	GPIO	Output from shutter switch when its pressed halfway. This switch state is used to trigger the Auto focus LED for Xenon Flash or Torch mode for LED Flash.
GP_CAMERASB1	I/O	V1P8	GPIO	Output from shutter switch when its pressed full way. This switch state is used to trigger Xenon flash or LED Flash.
GP_CAMERASB2	I/O	V1P8	GPIO	Active high control signal to Xenon Flash to start charging the capacitor
GP_CAMERASB3	I/O	V1P8	GPIO	Active low output from Xenon Flash to indicate that the capacitor is fully charged and is ready to be triggered
GP_CAMERASB4	I/O	V1P8	GPIO	Active high Xenon Flash trigger/Enables Torch Mode on LED Flash IC
GP_CAMERASB5	I/O	V1P8	GPIO	Enables Red Eye Reduction LED for Xenon/ Triggers STROBE on LED Flash IC
GP_CAMERASB6	I/O	V1P8	GPIO	Camera Sensor 0 Strobe Output to SoC to indicate beginning of capture/Active high signal to still camera to power down the device.
GP_CAMERASB7	I/O	V1P8	GPIO	Camera Sensor 1 Strobe Output to SoC to indicate beginning of capture/Active high signal to still camera to power down the device
GP_CAMERASB8	I/O	V1P8	GPIO	Active high signal to video camera to power down the device.
GP_CAMERASB9	I/O	V1P8	GPIO	Active low output signal to reset digital still camera #0
GP_CAMERASB10	I/O	V1P8	GPIO	Active low output signal to reset digital still camera #1
GP_CAMERASB11	I/O	V1P8	GPIO	Active low output signal to reset digital video camera
Note: These signals are also part of the SoC GPIOs and designers can use them based on design implementation.				

2.10 SVID Signals

Table 2-12. SVID Interface Signals

Signal Name	Dir.	I/O Voltage	Type	Description
SVID_CLK	O, OD	V1P05	GPIO	SVID Clock signal
SVID_DATA	I/O, OD	V1P05	GPIO	SVID Data signal
SVID_ALERT_N	I	V1P05	GPIO	SVID Alert signal



2.11 eMMC* Signals

Table 2-13. SoC eMMC* Interface Signals

Signal Name	Dir.	I/O Voltage	Type	Description
EMMC_CLK	O	V1P8	GPIO	eMMC* Clock
EMMC_D[7:0]	I/O	V1P8	GPIO	eMMC* Port Data bits 0 to 7: Bi-directional port used to transfer data to and from eMMC* device.
EMMC_CMD	I/O	V1P8	GPIO	eMMC* Port Command: This signal is used for card initialization and transfer of commands.
EMMC_PWR_EN_N	O	V1P8/ V3P3	GPIO	eMMC Power Enable: This signal is used to power cycle the eMMC Card
EMMC_RCLK	I	V1P8	GPIO	eMMC Return Clock: Return Clock/Data Strobe signal
EMMC_RCOMP	I	V1P8	GPIO	eMMC* RCOMP: This signal is used for pre-driver slew rate compensation.

2.12 SD Card Signals

Table 2-14. SoC SD Card Interface Signals

Signal Name	Dir.	I/O Voltage	Type	Description
SDCARD_CLK	O	V1P8/V3P3	GPIO	SD Card Clock: Port Clock
SDCARD_D[3:0]	I/O	V1P8/V3P3	GPIO	SD Card Data bits 0 to 3: Bi-directional port used to transfer data to and from SD/MMC card. By default, after power up or reset, only D[0] is used for data transfer. A wider data bus can be configured for data transfer, using D[0]-D[3].
SDCARD_CD_N	I	V1P8	GPIO	SD Card Detect: Active low when a card is present. Floating (pulled high with external PU) when a card is not present.
SDCARD_CMD	I/O	V1P8/V3P3	GPIO	SD Card Command: This signal is used for card initialization and transfer of commands.
SDCARD_LVL_WP	I	V1P8	GPIO	SD Card Port Write Protect: Active High pin when High, a card does not want to accept writes. This signal must be pulled up on the platform using an external pull up resistor.
SDCARD_LVL_CLK_FB	I/O	V1P8	-	Clock feedback signal for aligning the SD Card data from level shifter. There is a loop back through the level shifter that drives this signal. This is connected to the controller. Note: This is not a physical GPIO that can be used. This Signal is not Ball out on the SoC. Only the buffer exists.
Notes: - These signals will default to 3.3V during initial power-up and depending on the type of SD Card used, it can be negotiated down to 1.8V. User needs to know the GPIO Configuration Registers to enable the 1.8V Mode. - The above signals have internal PU and PD. Refer to the Table 2-34 for more information.				

2.13 System Management Bus (SMBus)

Table 2-15. SoC SMBus Interface Signals

Signal Name	Dir.	I/O Voltage	Type	Description
SMB_ALERT_N	I/O	V1P8/V3P3	GPIO	SMBus Alert: This signal is used to wake the system or generate SMI#. External pull-up resistor is required.
SMB_CLK	I/O	V1P8/V3P3	GPIO	SMBus Clock: External pull-up is required.
SMB_DATA	I/O	V1P8/P3V3	GPIO	SMBus Data: External pull-up resistor is required.
Note: The I/O voltage selection is done by using Hardware Strap GPIO_78.				

2.14 USB 2.0 Interface Signals

Table 2-16. USB 2.0 Interface Signals

Signal Name	Dir.	I/O Voltage	Type	Description
USB2_DN[7:0]	I/O	V3P3	USB2 PHY	USB2 Data: High speed serialized data I/O.
USB2_DP[7:0]	I/O	V3P3	USB2 PHY	
USB2_RCOMP	O	V3P3	USB2 PHY	Resistor Compensation: This signal is used for pre-driver slew rate compensation.
USB2_DUALROLE_ID	I/O	V1P8		USB Dual Role Support
USB2_VBUS_SNS	I	V1P8		USB VBus Sense line
USB_OC[1:0]_N	I/O	V1P8	GPIO	Used by the controller to disable I/O in case of overcurrent Note: USB_OC[1:0]_N can be individually configured for the USB ports.
Note: There are 8x HS ports available. 6x of these can be used towards USB 3.0 ports. By default USB2_DP/DN [7:6] are dedicated HS ports.				

2.15 USB 3.0 Interface Signals

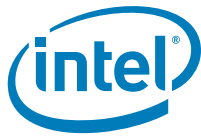
Table 2-17. SoC USB 3.0 Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
USB3_P[1:0]_TXP/N	O	V1P24	MOD-PHY	Differential Transmitter serial data outputs (Port0 and Port1): SuperSpeed Serialized data outputs.
USB3_P[1:0]_RXP/N	I	V1P24	MOD-PHY	Differential Receiver serial data inputs (Port0 and Port1): SuperSpeed serialized data inputs.
PCIE_P5_USB3_P2_TXP/N	O	V1P24	MOD-PHY	Differential Transmitter serial data outputs (Port2): Multiplexed PCIe*2/Super-Speed Serialized data outputs.
PCIE_P5_USB3_P2_RXP/N	I	V1P24	MOD-PHY	Differential Receiver serial data inputs (Port2): Multiplexed PCIe*2/SuperSpeed serialized data inputs.
PCIE_P4_USB3_P3_TXP/N	O	V1P24	MOD-PHY	Differential Transmitter serial data outputs (Port3): Multiplexed PCIe*2/Super-Speed Serialized data outputs.



Table 2-17. SoC USB 3.0 Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
PCIE_P4_USB3_P3_RXP/N	I	V1P24	MOD-PHY	Differential Receiver serial data inputs (Port3): Multiplexed PCIE*2/SuperSpeed serialized data inputs.
PCIE_P3_USB3_P4_TXP/N	O	V1P24	MOD-PHY	Differential Transmitter serial data outputs (Port4): Multiplexed PCIE*2/Super-Speed Serialized data outputs.
PCIE_P3_USB3_P4_RXP/N	I	V1P24	MOD-PHY	Differential Receiver serial data inputs (Port4): Multiplexed PCIE*2/SuperSpeed serialized data inputs.
SATA_P1_USB3_P5_TXP/N	O	V1P24	MOD-PHY	Differential Transmitter serial data outputs (Port5): Multiplexed SATA3/Super-Speed Serialized data outputs.
SATA_P1_USB3_P5_RXP/N	I	V1P24	MOD-PHY	Differential Receiver serial data inputs (Port5): Multiplexed SATA3/SuperSpeed serialized data inputs.
PCIE2_USB3_SATA3_RCOMP_N	O	V1P24	MOD-PHY	Resistor Compensation: This signal is used for pre-driver slew rate compensation. This signal is common for PCI2, USB3, and SATA3 compensation.
PCIE2_USB3_SATA3_RCOMP_P	O	V1P24	MOD-PHY	



2.16 PCIe* Interface Signals

Table 2-18. SoC PCIe*2 Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
PCIE_P[2:0]_TXP/N	O	V1P24	MOD-PHY	Differential Transmitter serial data outputs: PCIe*2 data outputs. Tied to PCIe* x4 controller.
PCIE_P[2:0]_RXP/N	I	V1P24	MOD-PHY	Differential Receiver serial data inputs: PCIe*2 data input. Tied to PCIe x4 controller.
PCIE_P3_USB3_P4_TXP/N	O	V1P24	MOD-PHY	Differential Transmitter serial data outputs: Multiplexed PCIe*2/USB3 Super-Speed Serialized data outputs. Tied to PCIe x4 controller.
PCIE_P3_USB3_P4_RXP/N	I	V1P24	MOD-PHY	Differential Receiver serial data inputs: Multiplexed PCIe*2/USB3 Super-Speed serialized data inputs. Tied to PCIe x4 controller.
PCIE_P4_USB3_P3_TXP/N	O	V1P24	MOD-PHY	Differential Transmitter serial data outputs: Multiplexed PCIe*2/USB3 Super-Speed Serialized data outputs. Tied to PCIe x2 controller.
PCIE_P4_USB3_P3_RXP/N	I	V1P24	MOD-PHY	Differential Receiver serial data inputs: Multiplexed PCIe*2/USB3 Super-Speed serialized data inputs. Tied to PCIe* x2 controller.
PCIE_P5_USB3_P2_TXP/N	O	V1P24	MOD-PHY	Differential Transmitter serial data outputs: Multiplexed PCIe*2/USB3 Super-Speed Serialized data outputs. Tied to PCIe* x2 Controller
PCIE_P5_USB3_P2_RXP/N	I	V1P24	MOD-PHY	Differential Receiver serial data inputs: Multiplexed PCIe*2/USB3 Super-Speed serialized data inputs. Tied to PCIe x2 Controller.
PCIE_CLKOUT[3:0]P/N	I/O	V1P05	CLK PHY	PCIe* Output Clocks
PCIE_WAKE[3:0]_N	I	V1P8	GPIO	PCIe* Wake Signals
PCIE_CLKREQ[3:0]_N	I/O	V1P8	GPIO	PCIe Clock Request: Used for devices that need to request one of the four output clocks. Note: Each CLKREQ signal must be associated with the corresponding PCIE_CLKOUT to enable the clocks for each port.
PCIE2_USB3_SATA3_RCOMP_N	O	V1P24	MOD-PHY	Resistor Compensation: This signal is used for pre-driver slew rate compensation. This signal is common for PCI*2, USB3 and SATA3 compensation
PCIE2_USB3_SATA3_RCOMP_P	O	V1P24	MOD-PHY	
PCIE_REF_CLK_RCOMP	O	V1P24	MOD-PHY	Resistor Compensation: PCI reference clock compensation resistor signal.



Table 2-18. SoC PCIE*2 Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
PCIE_PERST[3:0]_N	O	V1P8	GPIO	PCie Reset Note: Operates in GPIO Mode. These signals need to be assigned by BIOS based on design implementation
PCIE_PFET[3:0]	O	V1P8	GPIO	PCie Power FET (OPTIONAL) Note: Operates in GPIO Mode. These signals are optional and need to be assigned by BIOS based on design implementations
Notes: 1. PCIE_WAKE and PCIECLKREQ can be paired with any port. These signals are not tied to a particular port usage. 2. Note that each CLKREQs signal must be associated with the corresponding PCIE_REFCLK to enable the clocks for each port.				

2.17 SATA Interface Signals

Table 2-19. SoC SATA3 Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
SATA_P0_TXP/N	O	V1P24	MOD-PHY	Serial ATA Differential Transmit Pair 0: These outbound SATA Port 0 high-speed differential signals support 1.5Gb/s, 3Gb/s and 6Gb/s.
SATA_P0_RXP/N	I	V1P24	MOD-PHY	Serial ATA Differential Receive Pair 0: These inbound SATA Port 0 high-speed differential signals support 1.5Gb/s, 3Gb/s, and 6Gb/s.
SATA_P1_USB3_P5_TXP/N	O	V1P24	MOD-PHY	Serial ATA Differential Transmit Pair 1: These outbound SATA Port 1 high-speed differential signals support 1.5Gb/s, 3Gb/s and 6Gb/s. The signals are multiplexed with USB3, Port 5 signals.
SATA_P1_USB3_P5_RXP/N	I	V1P24	MOD-PHY	Serial ATA Differential Receive Pair 1: These inbound SATA Port 1 high-speed differential signals support 1.5Gb/s, 3Gb/s, and 6Gb/s. The signals are multiplexed with USB3 Port 5 signals.
SATA_GP0/GPIO_22	I/O	V1P8	GPIO	Serial ATA Port [0] General Purpose Inputs: When configured as SATA_GP0, this is an input pin that issued as an interlock switch status indicator for SATA Port 0. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open.
SATA_GP1/GPIO_23	I/O	V1P8	GPIO	Serial ATA Port [1] General Purpose Inputs: When configured as SATA_GP1, this is an input pin that issued as an interlock switch status indicator for SATA Port 1. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open.
SATA_DEVSLP0/GPIO_24	I/O	V1P8	GPIO	Serial ATA Port [0] Device Sleep: This is an open-drain pin on the SoC side. SoC will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that is internal to the SATA device, per DEVSLP specification). SoC will drive pin low to signal an exit from DEVSLP state. Note: This pin can be mapped to SATA Port 0.
SATA_DEVSLP1/GPIO_25	I/O	V1P8	GPIO	Serial ATA Port [1] Device Sleep: This is an open-drain pin on the SOC side. SoC will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). SoC will drive pin low to signal an exit from DEVSLP state. Design Constraint: No external pull-up or pull-down termination required when used as DEVSLP. Note: This pin can be mapped to SATA Port 1.

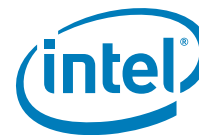


Table 2-19. SoC SATA3 Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
SATA_LED_N/GPIO_26	I/O	V1P8	GPIO	Serial ATA LED: This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off.
PCIE2_USB3_SATA3_RCOMP_N	O	V1P24	MOD-PHY	Compensation Resistor: This signal is used for pre-driver slew rate compensation. Note: This signal is common for PCIe*2, USB3 and SATA3 compensation
PCIE2_USB3_SATA3_RCOMP_P	O	V1P24	MOD-PHY	

2.18 FAST SPI Interface

2.18.1 Fast Serial Peripheral Interface (SPI) Signals

Table 2-20. Fast Serial Peripheral Interface (SPI) Signals

Signal Name	Dir.	I/O Voltage	Type	Description
FST_SPI_MOSI_IO0	I/O	V1P8	GPIO	Fast SPI Data Pad: Data Input/output pin for the SoC.
FST_SPI_MISO_IO1	I/O	V1P8	GPIO	
FST_SPI_IO2	I/O	V1P8	GPIO	
FST_SPI_IO3	I/O	V1P8	GPIO	
FST_SPI_CLK	I/O	V1P8	GPIO	Fast SPI Clock: When the bus is idle, the owner will drive the clock signal low.
FST_SPI_CS0_N	I/O	V1P8	GPIO	Fast SPI Chip Select 0: Used as the SPI bus request signal for the first SPI Flash devices.
FST_SPI_CS1_N	I/O	V1P8	GPIO	Fast SPI Chip Select 1: Used as the SPI bus request signal for the second SPI Flash devices.
FST_SPI_CS2_N	I/O	V1P8	GPIO	Fast SPI Chip Select 2: Used as the SPI bus request signal for the TPM device.
FST_SPI_CLK_FB	I/O	V1P8	-	Clock feedback signal for aligning the FST SPI data from level shifter. This is connected to the controller. Note: This is not a physical GPIO that can be used. This Signal is not Ball out on the SoC. Only the buffer exists.
Notes: 1. These signals will be tri-stated when SoC is in Sx state (will need RSMRST_N to be asserted). 2. RSMRST_N based Flash sharing between SoC and EC is allowed when coming out of G3. Flash access in G3 will not work without isolating the SoC using external components. For Windows* platform, TXE3.0 supports verified boot flow in which the firmware from SPI device is authenticated.				

2.19 SIO (LPSS) Serial Peripheral Interface (SPI) Signals

Table 2-21. SIO (LPSS) Serial Peripheral Interface (SPI) Signals

Signal Name	Dir.	I/O Voltage	Type	Description
SIO_SPI_0_TXD	I/O	V1P8	GPIO	SIO SPI 0 Data Pad: Data Input/Output pin for the SoC.
SIO_SPI_0_RXD	I/O	V1P8	GPIO	
SIO_SPI_0_FS0	I/O	V1P8	GPIO	SIO SPI 0 Frame Select: Used as the SPI bus request signal
SIO_SPI_0_CLK	I/O	V1P8	GPIO	SIO SPI 0 Clock: SPI Clock signal
SIO_SPI_[1:2]_TXD	I/O	V1P8	GPIO	These signals can be used as GPIOs ONLY
SIO_SPI_[1:2]_RXD	I/O	V1P8	GPIO	
SIO_SPI_[1:2]_FS0	I/O	V1P8	GPIO	
SIO_SPI_[1:2]_FS1	I/O	V1P8	GPIO	
SIO_SPI_[1:2]_CLK	I/O	V1P8	GPIO	
Notes: 1. The SIO_SPI_0 is dedicated SPI to support Finger Print Sensor. This set of signals is part of the GPIO pins and need to be configured in the BIOS to enabled SPI functionality.				

2.20 JTAG Interface Signals

Table 2-22. JTAG Interface Signals

Signal Name	Dir.	I/O Voltage	Type	Description
JTAG_TCK	I/O	V1P8	GPIO	JTAG Test Clock: Provides the clock input for the SoC Test Bus (also known as, Test Access Port).
JTAG_TDI	I/O	V1P8	GPIO	JTAG Test Data Input: Transfers serial test data into the processor.
JTAG_TDO	I/O, OD	V1P8	GPIO	JTAG Test Data Output: Transfers serial test data out of the processor.
JTAG_TMS	I/O	V1P8	GPIO	JTAG Test Mode Select: A JTAG specification support signal used by debug tools.
JTAG_TRST_N	I/O	V1P8	GPIO	JTAG Test Reset: Asynchronously resets the Test Access Port (TAP) logic.
JTAG_PRDY_N	I/O, OD	V1P8	GPIO	Probe Mode Ready: SoC response to PREQ_B assertion. Indicates SoC is in probe mode.
JTAG_PREQ_N	I/O	V1P8	GPIO	Probe Mode Request: Requests the SoC to enter probe mode. SoC will response with PRDY_B assertion once it has entered.
JTAG_PMODE	I/O	V1P8	GPIO	Power Mode: This signal serially encodes the virtual system-state
JTAGX	I/O	V1P8	GPIO	Tap master control



2.21 Audio Interface Signals

Table 2-23. SoC Audio Interface Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O voltage	Type	Description
AVS_I ² S[1:2]_MCLK	I/O	V1P8	GPIO	MCLK for Master Mode operation or GPIO.
AVS_I ² S[1:2]_BCLK	I/O	V1P8	GPIO	Analog microphone I ² S Bit Clock – bi-directional. In master mode the BCLK is supplied by the SoC, in slave mode serves as an input
AVS_I ² S[1:2]_WS_SYNC	I/O	V1P8	GPIO	Word Select or SYNC input – marks the beginning of serial sample
AVS_I ² S[1:2]_SDI	I/O	V1P8	GPIO	Analog microphone I ² S Data in – serial data input
AVS_I ² S[1:2]_SDO	I/O	V1P8	GPIO	Audio Codec I ² S Data out – serial data out
AVS_I ² S3_BCLK	I/O	V1P8	GPIO	Audio Codec I ² S Bit Clock – bi-directional. In master mode the BCLK is supplied by the SoC, in slave mode serves as an input
AVS_I ² S3_WS_SYNC	I/O	V1P8	GPIO	Audio Codec frame synchronization or Word select signal. Bi-directional – may be configured for master or slave
AVS_I ² S3_SDI	I/O	V1P8	GPIO	Audio Codec I ² S Data in – serial data in
AVS_I ² S3_SDO	I/O	V1P8	GPIO	Audio Codec I ² S Data out – serial data out
AVS_I ² S[4:6]_BCLK	I/O	V1P8	GPIO	Audio Codec I ² S Bit Clock – bi-directional. In master mode the BCLK is supplied by the SoC, in slave mode serves as an input This signal is a part of the GPIO pins and needs to be configured in the BIOS to enable there functionality
AVS_I ² S[4:6]_WS_SYNC	I/O	V1P8	GPIO	Audio Codec frame synchronization or Word select signal. Bi-directional – may be configured for master or slave This signal is a part of the GPIO pins and needs to be configured in the BIOS to enable there functionality
AVS_I ² S[4:6]_SDI	I/O	V1P8	GPIO	Audio Codec I ² S Data in – serial data in This signal is a part of the GPIO pins and needs to be configured in the BIOS to enable there functionality
AVS_I ² S[4:6]_SDO	I/O	V1P8	GPIO	Audio Codec I ² S Data out – serial data out This signal is a part of the GPIO pins and needs to be configured in the BIOS to enable there functionality This signal is a part of the GPIO pins and needs to be configured in the BIOS to enable there functionality
AVS_DMIC_CLK_A1	I/O	V1P8	GPIO	DMIC Clock: Digital Microphone Clock for channel A (Voice trigger microphone)
AVS_DMIC_CLK_B1	I/O	V1P8	GPIO	DMIC Clock: Digital Microphone Clock for channel B (Secondary microphone)
AVS_DMIC_DATA_1	I/O	V1P8	GPIO	DMIC Data: First microphone pair data input
AVS_DMIC_CLK_AB2	I/O	V1P8	GPIO	DMIC Data: Second microphone pair Clock (common for the second pair)

Table 2-23. SoC Audio Interface Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O voltage	Type	Description
AVS_DMIC_DATA_2	I/O	V1P8	GPIO	DMIC Data: Second microphone pair Data (Common for the second pair)
Notes: 1. SoC supports two I ² S interfaces. AVS_I ² S2 and AVS_I ² S6. 2. The other I ² S interfaces can be used as GPIO.				

Table 2-24. SoC HDA Interface Signals

Signal Name	Dir.	I/O Voltage	Type	Description
AVS_HDA_BCLK	O	V1P8	GPIO	HD Audio Bit Clock: Up to 24-MHz serial data clock generated by the Intel HD Audio controller.
AVS_HDA_WS_SYNC	O	V1P8	GPIO	HD Audio Word Select or SYNC: 48 KHz fixed rate frames sync to the codec. Also used to encode the stream number.
AVS_HDA_SDI	I	V1P8	GPIO	HD Audio Serial Data In: Serial TDM data input from the codec. The serial input is single-pumped for a bit rate of up to 24Mb/s. The signal contains integrated pull-down resistors, which are enabled while the primary well is powered.
AVS_HDA_SDO	O	V1P8	GPIO	HD Audio Serial Data Out: Serial TDM data output to the codecs. The serial output is double-pumped for a bit rate of up to 48Mb/s.
AVS_HDA_RST_N	O	V1P8	GPIO	HD Audio Reset: Master H/W Reset to internal/external codec.
Note: This set of signals is part of the GPIO pins and need to be configured in the BIOS to enabled HDA functionality.				

2.22 High Speed UART Interface Signals

These signals are part of the GPIO. Refer to [Table 2-34](#) for more details.

Table 2-25. SoC UART Interface Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
LPSS_UART1_RXD	I/O	V1P8	GPIO	UART1 data send
LPSS_UART1_TXD	I/O	V1P8	GPIO	UART1 data output
LPSS_UART1_RTS_N	I/O	V1P8	GPIO	UART1 Ready to Send
LPSS_UART1_CTS_N	I/O	V1P8	GPIO	UART1 Clear to Send
LPSS_UART2_RXD	I/O	V1P8	GPIO	UART2 data input
LPSS_UART2_TXD	I/O	V1P8	GPIO	UART2 data output
LPSS_UART2_RTS_N	I/O	V1P8	GPIO	UART2 Ready to Send
LPSS_UART2_CTS_N	I/O	V1P8	GPIO	UART2 Clear to Send
LPSS_UART0_RXD	I/O	V1P8	GPIO	These signals can be used as GPIOs
LPSS_UART0_TXD	I/O	V1P8	GPIO	These signals can be used as GPIOs
LPSS_UART0_RTS_N	I/O	V1P8	GPIO	These signals can be used as GPIOs
LPSS_UART0_CTS_N	I/O	V1P8	GPIO	These signals can be used as GPIOs



Table 2-25. SoC UART Interface Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
Notes: 1. LPSS_UART1 should be dedicated for discrete GNSS. 2. LPSS_UART2 should be dedicated for Host OS Debug				

2.23 I²C Interface Signals

Table 2-26. SoC I²C Interface Signals

Signal Name	Dir.	I/O Voltage	Type	Description
LPSS_I ² C[7:0]_SDA	I/O	V1P8	GPIO	I ² C Serial Data
LPSS_I ² C[7:0]_SCL	I/O	V1P8	GPIO	I ² C Serial Clock
ISH_I ² C[2:0]_SDA	I/O	V1P8	GPIO	I ² C Serial Data
ISH_I ² C[2:0]_SCL	I/O	V1P8	GPIO	I ² C Serial Clock
DDI[1:0]_DDC_SDA	I/O	V1P8	GPIO	I ² C Serial Data for Display
DDI[1:0]_DDC_SCL	I/O	V1P8	GPIO	I ² C Serial Clock for Display
MIPI_I ² C_SDA	I/O	V1P8	GPIO	I ² C Serial Data for MIPI Port
MIPI_I ² C_SCL	I/O	V1P8	GPIO	I ² C Serial Clock for MIPI Port
PMIC_I ² C_SDA	I/O	V1P8	GPIO	I ² C Serial Data for PMIC
PMIC_I ² C_SCL	I/O	V1P8	GPIO	I ² C Serial Clock for PMIC
Note: These signals are part of the GPIO. Refer to Table 2-34 for more details.				

2.24 Power Management Signals

Table 2-27. SoC PM Interface Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
PMU_BATLOW_N	I/O	V1P8/V3P3	GPIO	Battery Low: This signal indicates that there is insufficient power to boot the system. Assertion will prevent wake from S3-S5 state. This signal can also be enabled to cause an SMI# when asserted.
PMU_PLTRST_N	I/O	V1P8/V3P3	GPIO	Platform Reset: This signal is used to reset devices on the platform (such as SIO, LAN, processor, and so forth.). This signal is asserted during power-up and when S/W initiates a hard reset sequence through the Reset Control register (I/O port CF9h). The SoC drives PLTRST# active a minimum of 1 ms when initiated through the Reset Control register (I/O port CF9h)
PMU_PWRBTN_N	I	V1P8/V3P3	GPIO	Power Button: Power button input signal. Used to wake the SoC from power button press. The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S3- S4 states. This signal has an internal 16 ms de-bounce on the input.

Table 2-27. SoC PM Interface Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
PMU_RSTBTN_N	I	V1P8/V3P3	GPIO	Reset Button: Reset button input signal.
PMU_SLP_S0_N	O	V1P8/V3P3	GPIO	S0 Sleep Control: Controls power delivery subsystem. Asserted low in S0ix
PMU_SLP_S3_N	O	V1P8/V3P3	GPIO	S3 Sleep Control: Controls power delivery subsystem. Asserted low in S3 and lower
PMU_SLP_S4_N	O	V1P8/V3P3	GPIO	S4 Sleep Control: Controls power delivery subsystem. Asserted low in S4 and lower
PMU_SUSCLK	O	V1P8/V3P3	GPIO	Suspend Clock: Primary RTC clock output.
PMU_RCOMP	O	V1P8/V3P3	GPIO	Resistor Compensation
SUS_STAT_N	O	V1P8/V3P3	GPIO	Suspend Status: Asserted to indicate that the system will be entering a Sx state.
SUSPWRDNACK	O	V1P8/V3P3	GPIO	Sus Power Down Ack: Indicator from SoC that "always on" rails can be shut down.
SOC_PWROK	I	VCC_RTC_3P3V	PHY	SoC Power OK: When asserted, this signal is an indication to the SoC that all of its core power rails have been stable for at least 5 ms. This signal can be driven asynchronously. Then this signal is negated, the SoC asserts PLTRST#. Note: This signal was previously called PCH_PWROK
Notes: 1. These signals are part of the GPIO. Refer to Table 2-34 for more details. 2. The I/O voltage selection is done by using Hardware Strap GPIO_88.				

2.25 Real Time Clock (RTC) Interface Signals

Table 2-28. SoC RTC Interface (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
INTRUDER_N	I	VCC_RTC_3P3V	RTC PHY	Intruder Detect: This signal can be set to disable system if box detected open.
RSM_RST_N	I	VCC_RTC_3P3V	RTC PHY	Resume Well Reset Used for resetting the resume well. An external RC circuit is required to guarantee that the resume well power is valid prior to this signal going high.
RTC_TEST_N	I	VCC_RTC_3P3V	RTC PHY	RTC Battery Test An external RC circuit creates a time delay for the signal such that it will go high (de-assert) sometime after the battery voltage is valid. If the battery is missing/weak, this signal appears low (asserted) at boot just after the suspend power rail (V3P3) is up since it will not have time to meet Vih (Voltage input high) when V3P3A is high. When asserted, BIOS may clear the RTC CMOS RAM. Note: Unless CMOS is being cleared (only to be done in the G3 power state) or the battery is low, the signal input must always be high when all other RTC power planes are on.

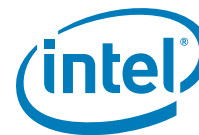


Table 2-28. SoC RTC Interface (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
RTC_RST_N	I	VCC_RTC_3P3V	RTC PHY	RTC Reset An external RC circuit creates a time delay for the signal such that it will go high (de-assert) sometime after the battery voltage is valid. When asserted, this signal resets all register bits in the RTC well. Notes: - Unless registers are being cleared (only to be done in the G3 power state), the signal input must always be high when all other RTC power planes are on. - In the case where the RTC battery is dead or missing on the platform, the signal should be de-asserted before the RSM_RST_N signal is de-asserted.
RTC_X1	I	V3P3	RTC PHY	Crystal Input 1: This signal is connected to a 32.768 KHz crystal (max 50K ESR). If using an external oscillator, the RTCX1 Vih must be within the range of 0.8V to 1.2V (1.2V max).
RTC_X2	O	V3P3	RTC PHY	Crystal Input 2: This signal is connected to a 32.768 KHz crystal (Max 50K ESR). If using an external oscillator, RTCX2 should be left floating.
VCC_RTC_EXTPAD	O	V3P3	RTC PHY	External Pad for voltage supply

2.26 Integrated Clock Interface Signals

Table 2-29. Integrated Clock Interface Signals (Sheet 1 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
MEM_CH[1:0]_CLKP/N[1:0]	O	VDDQ	DDR3L	DDR3L Memory Clocks
MEM_CH[1:0]_CLKP/N[1:0]A/B	O	VDDQ	LPDDR3	LPDDR3 Memory Clocks
MEM_CH[1:0]_CLKP/N[1:0]A/B	O	VDDQ	LPDDR4	LPDDR4 Memory Clocks
PCIE_CLKOUT[3:0]P/N	O	V1P05	CLOCK	PCIe* Clocks
eMMC_CLK	O	V1P8	GPIO	eMMC* Clock
eMMC_RCLK	I	V1P8	GPIO	eMMC* Return Clock
SDCARD_CLK	O	V1P8/V3P3	GPIO	SD Card Clock
DDI[1:0]_DDC_SCL	O	V1P8	GPIO	DDI Port Clocks
MDSI_[A, C]_CLKP/N	O	V1P24	D-PHY	MDSI Port Clocks
MCSI_CLKP/N[0,2]	O	V1P24	D-PHY1.1	MCSI Port Clocks (D-PHY1.1)
MCSI_RX_CLK[0,1]_P/N	O	V1P24	D-PHY1.2	MCSI Ports Clocks (D-PHY1.2)
AVS_HDA_BCLK	O	V1P8	GPIO	HD Audio Clock
AVS_I ² S[3:1]_BCLK AVS_I ² S[2:1]_MCLK AVS_I ² S[5:6]_BCLK	O	V1P8	GPIO	AVS I ² S clocks
AVS_DMIC_CLK_[A/B]1 AVS_DMIC_CLK-AB2	O	V1P8	GPIO	Digital Microphone Clocks
MIPI_I ² C_SCL	O	V1P8	GPIO	MIPI I ² C Clock
PMIC_I ² C_SCL	O	V1P8	GPIO	PMIC I ² C Clock

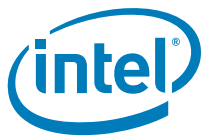


Table 2-29. Integrated Clock Interface Signals (Sheet 2 of 2)

Signal Name	Dir.	I/O Voltage	Type	Description
ISH_I ² C[2:0]_SCL	O	V1P8	GPIO	PMIC I ² C Clock
SVID_CLK	O	V1P05	GPIO	Serial VID Clock
LPC_CLKOUT[0,1]	O	V1P8/V3P3	GPIO	LPC Clock
SMB_CLK	O	V1P8/V3P3	GPIO	SMBus Clock
SIO_SPI_[2:0]_CLK	O	V1P8	GPIO	SIO (LPSS) Clock
FST_SPI_CLK	O	V1P8	GPIO	Fast SPI Clock (SPI NOR)
PMU_SUSCLK	O	V1P8/V3P3	GPIO	RTC clock Output to platform
SUS_CLK[3:1]	O	V1P8	GPIO	RTC clock output (GPIOs)
RTC_X[1,2]	I	V3P3	RTC	RTC Crystal Input
OSC_CLK_OUT[3:0]	O	V1P8	GPIO	Oscillator Clocks
OSCIN	I	V1P05	CLKPHY	Interface to attached crystal oscillator on the platform
OSCOUT	O	V1P05	CLKPHY	
DDI[1:0]_TXP/N[3]	O	V1P05	Display PHY	DDI Clock for HDMI
JTAG_TCK	I/O	V1P8	GPIO	JTAG Test Clock
LPSS_I2C[7:0]_SCL	I/O	V1P8	GPIO	I2C Serial Clock



2.27 Integrated Sensor Hub Interface Signals

Table 2-30. SoC Integrated Sensor Hub Interface Signals

Signal Name	Dir.	I/O Voltage	Type	Description
ISH_I ² C[2:0]_SDA	I/O	V1P8	GPIO	I ² C Data
ISH_I ² C[2:0]_SCL	I/O	V1P8	GPIO	I ² C Clock
ISH_GPIO_[15:0]	I/O	V1P8	GPIO	GPIO for wake, interrupt, alert from sensors

2.28 Low Pin Count (LPC) Bus

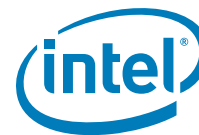
Table 2-31. SoC LPC Interface

Signal Name	Dir.	I/O Voltage	Type	Description
LPC_AD[3:0]	I/O, OD	V1P8/V3P3	GPIO	LPC Multiplexed Command, Address, Data
LPC_CLKOUT[1:0]	O	V1P8/V3P3	GPIO	Clock Out: 25 MHz output clock
LPC_CLKRUN_N	I/O, OD	V1P8/V3P3	GPIO	LPC Clock Run: Control LPC Clock Signals
LPC_FRAME_N	O	V1P8/V3P3	GPIO	LPC Frame: LFRAME# indicates the start of an LPC cycle, or an abort.
LPC_SERIRQ	I/O	V1P8/V3P3	GPIO	LPC SERIRQ: Serial Interrupt Request
Note: The I/O voltage selection is done by using Hardware Strap GPIO_110.				

2.29 Miscellaneous Signals

Table 2-32. Miscellaneous Signals

Signal Name	Dir.	I/O Voltage	Type	Description
PROCHOT_N	I, OD	V1P8	GPIO	Processor Hot: Indicates when the processor die temperature has reached its maximum operating temperature.
THERMTRIP_N	O	V1P8	GPIO	Thermal Trip: THERMTRIP_N will be asserted/driven by the SoC under the following conditions: - In case of a catastrophic thermal event as seen by the SoC. - To indicate that a 'force shutdown' event has occurred. If user presses the power button for the override length (4 seconds), SoC will assert THERMTRIP_N to force a platform G2. - If SOC_PWROK de-asserts unexpectedly during normal platform operation (while PMU_SLP_S3_N or PMU_SLP_S4_N) are de-asserted), then the SOC considers this as an unrecoverable condition and will be asserted THERMTRIP_N to take the system into G2. Note: In the event of a catastrophic thermal failure (such as failure of cooling system), each thermal sensor can detect that die temperature exceeds thermal specification limits (typically 24-28C above Tjmax) and assert its CAT sensor output. Assertion of CAT must automatically trigger a thermal shut-down of all CPU PLLs, and platform voltage regulators within 500 ms and also trigger the soc thermtrip# I/O pin to be asserted.
GPIO_RCOMP	I/O	V1P8	GPIO	Resistor Compensation: This signal is used for pre-driver slew rate compensation.
VNN_SENSE	I/O	N/A	PWR	VNN Sense signal for voltage feedback to the Voltage Regulator
VCC_VCGI_SENSE_P/N	I/O	N/A	PWR	Differential sense line for the VCC VCGI rail Voltage Regulator
PWM[3:0]	I/O	V1P8	GPIO	PWM Signals



2.30 Hardware Straps

Notes:

1. All the straps are sampled at ~95ms after RSM_RST_N de-assertion, where a stable RTC clock is used to count the duration. In cases where the RTC clock is not stable when boot starts, the strap sampling may deviate significantly above ~95ms.
2. The internal termination values listed in this table will be in effect from 3 RTC clock cycles before the strap sampling event until 3 RTC clock cycles after the strap sampling event. The external signal input to each strap must be glitch-free during this time. At 4 RTC clock cycles after the strap sampling event, the termination value will change to the GPIO termination as shown in [Table 2-33](#).
3. If the RTC Clock Timer Bypass strap is enabled, all the straps are sampled a few RTC clock cycles after RSM_RST_N de-assertion.

Table 2-33. Hardware Straps (Sheet 1 of 2)

GPIO #	Purpose	Internal Termination	Pin Strap Usage / Description / Polarity
GPIO_34	RSVD	20K PD	Ensure that this strap is always pulled low for normal platform operation.
GPIO_35	RSVD	20K PD	Ensure that this strap is always pulled low for normal platform operation.
GPIO_36	RSVD	20K PD	Ensure that this strap is always pulled low for normal platform operation.
GPIO_39	Enable CSE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) Notes: 1. SoC supports TXE3.0 (this is also called CSE) 2. This strap tells CSE (TXE3.0) to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of CSE (TXE3.0) before the first patch point this strap enabled the platform tell CSE (TXE3.0) to bypass the ROM causing the issue and go to the patch space instead.
GPIO_40	RTC Clock Timer Bypass	20K PD	1 =enable bypass 0 =disable bypass (Default) Note: This strap shall only be used when an external oscillator is used to supply a 32.768kHz clock to RTC_X1.
GPIO_43	RSVD	20K PU	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_44	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable
GPIO_47	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) Notes: 1. DnX: Download and Execute. 2. This strap is a recovery strap for corrupted FW image. This strap will force CSE (TXE3.0) to execute a "Download and Execute" (DnX) flow, where it would fetch firmware from a USB stick and re-flash a eMMC device. CSE (TXE3.0) can do it for BIOS part of FW, but if CSE FW itself is corrupted, this strap is needed.
GPIO_48	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_78	SMBus 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_82	RSVD	20K PD	Ensure that this strap is always pulled low for normal platform operation.

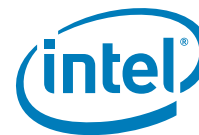
Table 2-33. Hardware Straps (Sheet 2 of 2)

GPIO #	Purpose	Internal Termination	Pin Strap Usage / Description / Polarity
GPIO_88	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_92	RSVD	20K PD	Ensure that this strap is pulled either HIGH or LOW when RSM_RST_N deasserts
GPIO_104	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N deasserts for normal platform operation.
GPIO_105	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N deasserts for normal platform operation.
GPIO_106	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N deasserts for normal platform operation.
GPIO_110	LPC 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_111	Allow SPI as a boot source	20K PU	- Pull LOW when RSM_RST_N deasserts to map these regions to the boot SPI - Pull HIGH when RSM_RST_N deasserts to leave these regions unmapped by the System Agent Note: Pull LOW for designs that boot from SPI and HIGH otherwise
GPIO_112	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N deasserts for normal platform operation.
GPIO_113	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N deasserts for normal platform operation.
GPIO_117	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N deasserts for normal platform operation.
GPIO_118	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override Note: This strap enables the platform to override security features in the SPI.
GPIO_119	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N deasserts for normal platform operation.
GPIO_120	Top swap override	20K PD	1 = Enable 0 = Disable (default) Note: Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_121	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N deasserts for normal platform operation.
GPIO_123	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N deasserts for normal platform operation.

2.31 GPIO Multiplexing

Notes:

- All GPIOs are available during the Sx and S0ix Standby state. The default I/O Standby State is programmable through BIOS.
- As mentioned in previous sections, not all the signals listed are supported on SoC but these signals can be used as GPIO functionality.



3. The operating I/O voltage of some GPIO with native functionality of SD_CARD will default to 3.3V and cannot be operated in 1.8V mode.
4. The operating I/O Voltage for GPIOs with native functionality of SMBus, LPC, and PMU will be based on the Hardware Strap selection as listed in [Table 2-33](#).
5. PMC-SPI pins are only for PMC debug and not general purpose SPI devices.
6. PCIE_CLKREQ signals can only be used as GPIO when the corresponding PCIE* slots or a PCIE* device is NOT in use. For example, if you are using PCIE_CLKREQ0 for PCIE* Port0, then you cannot use PCIE_CLKREQ0 as GPIO and it should be driven low to enable REFCLK0.
7. The state of the signal should be considered to be indeterminate until RSM_RST_N is de-asserted
8. GPIO_168, GPIO_174 and GPIO_219 are not usable as GPIO mode.

Table 2-34. SoC GPIO Multiplexing (Sheet 1 of 14)

GPIO No.	Signal Name	SoC Pin No.	Community	IO Voltage	Default Termination	Buffer Type	Default Mode	Fn 1	Fn 2	Fn 3	Fn 4	Fn 5	Fn 6
GPIO_79	AVS_DMIC_CLK_A1	P54	NW	1.8V	20K PD	HSMV	GP-In	AVS_DMIC_CLK_A1	AVS_I2S4_BCLK	0	0	0	0
GPIO_82	AVS_DMIC_CLK_AB2	M55	NW	1.8V	20K PD	HSMV	GP-In	AVS_DMIC_CLK_AB2	AVS_I2S4_SDO	0	0	0	0
GPIO_80	AVS_DMIC_CLK_B1	P52	NW	1.8V	20K PD	HSMV	GP-In	AVS_DMIC_CLK_B1	AVS_I2S4_WS_SYNC	0	0	0	0
GPIO_81	AVS_DMIC_DATA_1	M54	NW	1.8V	20K PD	HSMV	GP-In	AVS_DMIC_DATA_1	AVS_I2S4_SDI	0	0	0	0
GPIO_83	AVS_DMIC_DATA_2	M52	NW	1.8V	20K PD	HSMV	GP-In	AVS_DMIC_DATA_2		0	0	0	0
GPIO_75	AVS_I2S1_BCLK	H63	NW	1.8V	20K PD	HSMV	GP-In	AVS_I2S1_BCLK	0	0	0	0	0
GPIO_74	AVS_I2S1_MCLK	G62	NW	1.8V	20K PD	HSMV	GP-In	AVS_I2S1_MCLK	0	0	0	0	0
GPIO_77	AVS_I2S1_SDI	K61	NW	1.8V	20K PD	HSMV	GP-In	AVS_I2S1_SDI	0	0	0	0	0
GPIO_78	AVS_I2S1_SDO	K62	NW	1.8V	20K PD	HSMV	GP-In	AVS_I2S1_SDO	0	0	0	0	0
GPIO_76	AVS_I2S1_WS_SYNC	J62	NW	1.8V	20K PD	HSMV	GP-In	AVS_I2S1_WS_SYNC	0	0	0	0	0
GPIO_85	AVS_I2S2_BCLK	H59	NW	1.8V	20K PD	HSMV	GP-In	AVS_I2S2_BCLK	0	0	0	0	0
GPIO_84	AVS_I2S2_MCLK	K58	NW	1.8V	20K PD	HSMV	GP-In	AVS_I2S2_MCLK	AVS_HDA_RST_N	0	0	0	0

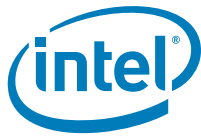


Table 2-34. SoC GPIO Multiplexing (Sheet 2 of 14)

GPIO No.	Signal Name	SoC Pin No.	Community	IO Voltage	Default Termination	Buffer Type	Default Mode	Fn 1	Fn 2	Fn 3	Fn 4	Fn 5	Fn 6
GPIO _87	AVS_I2S2_SDI	K59	NW	1.8V	20K PD	HSMV	GP-In	AVS_I2S2_SDI	0	0	0	0	0
GPIO _88	AVS_I2S2_SDO	M58	NW	1.8V	20K PD	HSMV	GP-In	AVS_I2S2_SDO	0	0	0	0	0
GPIO _86	AVS_I2S2_WS_SYNC	M57	NW	1.8V	20K PD	HSMV	GP-In	AVS_I2S2_WS_SYNC	0	0	0	0	0
GPIO _89	AVS_I2S3_BCLK	M62	NW	1.8V	20K PD	HSMV	GP-In	AVS_I2S3_BCLK	0	0	0	0	0
GPIO _91	AVS_I2S3_SDI	L62	NW	1.8V	20K PD	HSMV	GP-In	AVS_I2S3_SDI	0	0	0	0	0
GPIO _92	AVS_I2S3_SDO	L63	NW	1.8V	20K PD	HSMV	GP-In	AVS_I2S3_SDO	0	0	0	0	0
GPIO _90	AVS_I2S3_WS_SYNC	M61	NW	1.8V	20K PD	HSMV	GP-In	AVS_I2S3_WS_SYNC	0	0	0	0	0
GPIO _188	DDI0_DDC_SCL	B49	NW	1.8V	20K PU	MSMV	Fn 1	DDI0_DDC_SCL	0	0	0	0	0
GPIO _187	DDI0_DDC_SDA	C49	NW	1.8V	20K PU	MSMV	Fn 1	DDI0_DDC_SDA	0	0	0	0	0
GPIO _190	DDI1_DDC_SCL	A54	NW	1.8V	20K PU	MSMV	Fn 1	DDI1_DDC_SCL	0	0	0	0	0
GPIO _189	DDI1_DDC_SDA	C54	NW	1.8V	20K PU	MSMV	Fn 1	DDI1_DDC_SDA	0	0	0	0	0
GPIO _156	EMMC_CLK	Y58	SW	1.8V	20K PD	HSMV	Fn 1	EMMC_CLK	RSVD	0	0	0	0
GPIO _165	EMMC_CMD	Y51	SW	1.8V	20K PU	HSMV	Fn 1	EMMC_CMD	RSVD	0	0	0	0
GPIO _157	EMMC_D0	V58	SW	1.8V	20K PU	HSMV	Fn 1	EMMC_D0	RSVD	0	0	0	0
GPIO _158	EMMC_D1	T58	SW	1.8V	20K PU	HSMV	Fn 1	EMMC_D1	RSVD	0	0	0	0
GPIO _159	EMMC_D2	T59	SW	1.8V	20K PU	HSMV	Fn 1	EMMC_D2	RSVD	0	0	0	0
GPIO _160	EMMC_D3	V51	SW	1.8V	20K PU	HSMV	Fn 1	EMMC_D3	RSVD	0	0	0	0
GPIO _161	EMMC_D4	V52	SW	1.8V	20K PU	HSMV	Fn 1	EMMC_D4	RSVD	0	0	0	0
GPIO _162	EMMC_D5	Y49	SW	1.8V	20K PU	HSMV	Fn 1	EMMC_D5	RSVD	0	0	0	0



Table 2-34. SoC GPIO Multiplexing (Sheet 3 of 14)

GPIO No.	Signal Name	SoC Pin No.	Community	IO Voltage	Default Termination	Buffer Type	Default Mode	Fn 1	Fn 2	Fn 3	Fn 4	Fn 5	Fn 6
GPIO _163	EMMC_D6	V55	SW	1.8V	20K PU	HSMV	Fn 1	EMMC _D6	RSVD	0	0	0	0
GPIO _164	EMMC_D7	V57	SW	1.8V	20K PU	HSMV	Fn 1	EMMC _D7	RSVD	0	0	0	0
GPIO _221	EMMC_PWR_EN_N	AG55	W	1.8V/ 3.3V	20K PU	MSHV	GP-In	EMMC _PWR _EN _N	0	0	0	0	0
GPIO _182	EMMC_RCLK	V54	SW	1.8V	20K PD	HSMV	Fn 1	EMMC _RCL K	RSVD	0	0	0	0
GPIO _103	FST_SPI_CLK	C56	NW	1.8V	Native	HSMV	Fn 1	FST _SPI _C LK	0	0	0	0	0
GPIO _97	FST_SPI_CS0_N	B57	NW	1.8V	Native	HSMV	Fn 1	FST _SPI _C S0 _N	0	0	0	0	0
GPIO _98	FST_SPI_CS1_N	C57	NW	1.8V	Native	HSMV	Fn 1	FST _SPI _C S1 _N	0	0	0	0	0
GPIO _101	FST_SPI_IO2	B60	NW	1.8V	Native	HSMV	Fn 1	FST _SPI _I O2	0	0	0	0	0
GPIO _102	FST_SPI_IO3	B61	NW	1.8V	Native	HSMV	Fn 1	FST _SPI _I O3	0	0	0	0	0
GPIO _100	FST_SPI_MISO_IO1	B58	NW	1.8V	Native	HSMV	Fn 1	FST _SPI _MISO _IO1	0	0	0	0	0
GPIO _99	FST_SPI_MOSI_IO0	A58	NW	1.8V	Native	HSMV	Fn 1	FST _SPI _MOSI _IO0	0	0	0	0	0
GPIO _62	GP_CAMERASB0	L37	N	1.8V	20K PD	LSMV	GP-In	GP _C AMER ASB0	RSVD	0	0	0	0
GPIO _63	GP_CAMERASB1	P34	N	1.8V	20K PD	LSMV	GP-In	GP _C AMER ASB1	0	0	0	0	0
GPIO _72	GP_CAMERASB10	R34	N	1.8V	20K PD	LSMV	GP-In	GP _C AMER ASB10	0	0	0	0	0
GPIO _73	GP_CAMERASB11	E30	N	1.8V	20K PD	LSMV	GP-In	GP _C AMER ASB11	0	0	0	0	0
GPIO _64	GP_CAMERASB2	J34	N	1.8V	20K PD	LSMV	GP-In	GP _C AMER ASB2	0	0	0	0	0
GPIO _65	GP_CAMERASB3	H30	N	1.8V	20K PD	LSMV	GP-In	GP _C AMER ASB3	0	0	0	0	0

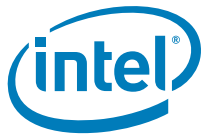


Table 2-34. SoC GPIO Multiplexing (Sheet 4 of 14)

GPIO No.	Signal Name	SoC Pin No.	Community	IO Voltage	Default Termination	Buffer Type	Default Mode	Fn 1	Fn 2	Fn 3	Fn 4	Fn 5	Fn 6
GPIO _66	GP_CAMERASB4	M37	N	1.8V	20K PD	LSMV	GP-In	GP_C AMER ASB4	0	0	0	0	0
GPIO _67	GP_CAMERASB5	F30	N	1.8V	20K PD	LSMV	GP-In	GP_C AMER ASB5	0	0	0	0	0
GPIO _68	GP_CAMERASB6	R35	N	1.8V	20K PD	LSMV	GP-In	GP_C AMER ASB6	0	0	0	0	0
GPIO _69	GP_CAMERASB7	L34	N	1.8V	20K PD	LSMV	GP-In	GP_C AMER ASB7	0	0	0	0	0
GPIO _70	GP_CAMERASB8	M34	N	1.8V	20K PD	LSMV	GP-In	GP_C AMER ASB8	0	0	0	0	0
GPIO _71	GP_CAMERASB9	M35	N	1.8V	20K PD	LSMV	GP-In	GP_C AMER ASB9	0	0	0	0	0
GPIO _0	GPIO_0	A38	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	RSVD
GPIO _1	GPIO_1	B33	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	RSVD
GPIO _10	GPIO_10	L39	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	0
GPIO _11	GPIO_11	C34	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	0
GPIO _12	GPIO_12	E39	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	0
GPIO _13	GPIO_13	C30	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	0
GPIO _14	GPIO_14	C38	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	0
GPIO _15	GPIO_15	F39	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	0
GPIO _16	GPIO_16	C36	N	1.8V	20K PU	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	0
GPIO _166	GPIO_166	P58	SW	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	0	0	0	0
GPIO _167	GPIO_167	T52	SW	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	0	0	0	0
GPIO _168	GPIO_168	P57	SW	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	0	0	0	0
GPIO _169	GPIO_169	T54	SW	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	0	0	0	0
GPIO _17	GPIO_17	C35	N	1.8V	20K PU	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	0
GPIO _170	GPIO_170	T55	SW	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	0	0	0	0
GPIO _171	GPIO_171	T57	SW	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	0	0	0	0



Table 2-34. SoC GPIO Multiplexing (Sheet 5 of 14)

GPIO No.	Signal Name	SoC Pin No.	Community	IO Voltage	Default Termination	Buffer Type	Default Mode	Fn 1	Fn 2	Fn 3	Fn 4	Fn 5	Fn 6
GPIO_18	GPIO_18	J39	N	1.8V	20K PU	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	0
GPIO_183	GPIO_183	P51	SW	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	0	0	0	0
GPIO_19	GPIO_19	C33	N	1.8V	20K PU	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	0
GPIO_199	GPIO_199	A50	NW	1.8V	20K PD	LSMV	GP-In	RSVD	DDI1_HPDP	0	0	0	0
GPIO_2	GPIO_2	C39	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	RSVD
GPIO_20	GPIO_20	B27	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	RSVD	0
GPIO_200	GPIO_200	C50	NW	1.8V	20K PD	LSMV	GP-In	RSVD	DDI0_HPDP	0	0	0	0
GPIO_21	GPIO_21	C26	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	RSVD	0
GPIO_213	GPIO_213	M47	NW	1.8V	None	LSMV	GP-In	RSVD	0	0	0	0	0
GPIO_214	GPIO_214	L47	NW	1.8V	20K PD	LSMV	GP-In	RSVD	0	0	0	0	0
GPIO_215	GPIO_215	P47	NW	1.8V	20K PD	LSMV	GP-In	RSVD	0	0	0	0	0
GPIO_216	GPIO_216	P30	N	1.8V	20K PD	HSMV	Fn1	RSVD	RSVD	0	0	0	0
GPIO_217	GPIO_217	M29	N	1.8V	20K PD	HSMV	Fn1	RSVD	RSVD	0	0	0	0
GPIO_218	GPIO_218	M30	N	1.8V	20K PD	HSMV	Fn1	RSVD	RSVD	0	0	0	0
GPIO_219	GPIO_219	L30	N	1.8V	20K PD	HSMV	Fn1	RSVD	RSVD	0	0	0	0
GPIO_242	GPIO_242	AF6_2	N	1.8V	20K PD	HSMV	Fn1	RSVD	0	0	0	0	0
GPIO_22	GPIO_22	A26	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	SATA_GP0	0
GPIO_223	GPIO_223	F48	NW	1.8V	None	LSMV	Fn1	RSVD	0	0	0	0	0
GPIO_224	GPIO_224	J45	NW	1.8V	20K PD	LSMV	Fn1	RSVD	0	0	0	0	0
GPIO_23	GPIO_23	B25	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	SATA_GP1	0
GPIO_24	GPIO_24	C25	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	SATA_DEV_SLP0	0
GPIO_25	GPIO_25	C27	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	SATA_DEV_SLP1	0
GPIO_26	GPIO_26	C31	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	SATA_LED_N	0

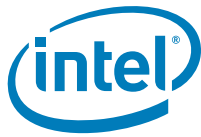


Table 2-34. SoC GPIO Multiplexing (Sheet 6 of 14)

GPIO No.	Signal Name	SoC Pin No.	Community	IO Voltage	Default Termination	Buffer Type	Default Mode	Fn 1	Fn 2	Fn 3	Fn 4	Fn 5	Fn 6
GPIO_27	GPIO_27	C29	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	RSVD
GPIO_28	GPIO_28	B37	N	1.8V	20K PD	HSMV	GP-In	RSVD	ISH_GPIO_10	RSVD	RSVD	0	RSVD
GPIO_29	GPIO_29	H35	N	1.8V	20K PD	HSMV	GP-In	RSVD	ISH_GPIO_11	RSVD	RSVD	0	RSVD
GPIO_3	GPIO_3	B39	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	RSVD
GPIO_30	GPIO_30	C37	N	1.8V	20K PD	HSMV	GP-In	ISH_GPIO_12	0	RSVD	RSVD	0	RSVD
GPIO_31	GPIO_31	H34	N	1.8V	20K PD	HSMV	GP-In	ISH_GPIO_13	0	RSVD	RSVD	SUSC LK1	0
GPIO_32	GPIO_32	F35	N	1.8V	20K PD	HSMV	GP-In	ISH_GPIO_14	0	RSVD	RSVD	SUSC LK2	0
GPIO_33	GPIO_33	F34	N	1.8V	20K PD	HSMV	GP-In	ISH_GPIO_15	0	RSVD	RSVD	SUSC LK3	0
GPIO_4	GPIO_4	B35	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	0
GPIO_5	GPIO_5	A34	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	0
GPIO_6	GPIO_6	B31	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	0
GPIO_7	GPIO_7	H39	N	1.8V	20K PD	HSMV	Fn5	RSVD	RSVD	RSVD	RSVD	RSVD	0
GPIO_8	GPIO_8	B29	N	1.8V	20K PD	HSMV	Fn5	RSVD	RSVD	RSVD	RSVD	RSVD	0
GPIO_9	GPIO_9	A30	N	1.8V	20K PD	HSMV	GP-In	RSVD	RSVD	RSVD	RSVD	0	0
GPIO_146	ISH_GPIO_0	AM48	W	1.8V	20K PD	HSMV	GP-In	ISH_GPIO_0	AVS_I2S6_BCLK	AVS_HDA_BCLK	0	0	0
GPIO_147	ISH_GPIO_1	AK58	W	1.8V	20K PD	HSMV	GP-In	ISH_GPIO_1	AVS_I2S6_WS_SYNC	AVS_HDA_WS_SYNC	0	0	0
GPIO_148	ISH_GPIO_2	AK51	W	1.8V	20K PD	HSMV	GP-In	ISH_GPIO_2	AVS_I2S6_SDI	AVS_HDA_SDI	0	0	0
GPIO_149	ISH_GPIO_3	AM54	W	1.8V	20K PD	HSMV	GP-In	ISH_GPIO_3	AVS_I2S6_SDO	AVS_HDA_SDO	0	0	0



Table 2-34. SoC GPIO Multiplexing (Sheet 7 of 14)

GPIO No.	Signal Name	SoC Pin No.	Community	IO Voltage	Default Termination	Buffer Type	Default Mode	Fn 1	Fn 2	Fn 3	Fn 4	Fn 5	Fn 6
GPIO_150	ISH_GPIO_4	AM51	W	1.8V	20K PD	HSMV	GP-In	ISH_GPIO_4	AVS_I2S5_BCLK	LPSS_UAR_T2_RXD	0	0	0
GPIO_151	ISH_GPIO_5	AM49	W	1.8V	20K PD	HSMV	GP-In	ISH_GPIO_5	AVS_I2S5_WS_SYNC	LPSS_UAR_T2_TXD	0	0	0
GPIO_152	ISH_GPIO_6	AM57	W	1.8V	20K PD	HSMV	GP-In	ISH_GPIO_6	AVS_I2S5_SDI	LPSS_UAR_T2_RXTS_B	0	0	0
GPIO_153	ISH_GPIO_7	AM55	W	1.8V	20K PD	HSMV	GP-In	ISH_GPIO_7	AVS_I2S5_SDO	LPSS_UAR_T2_CTS_B	0	0	0
GPIO_154	ISH_GPIO_8	AM52	W	1.8V	20K PD	HSMV	GP-In	ISH_GPIO_8	RSVD	0	0	0	0
GPIO_155	ISH_GPIO_9	AK57	W	1.8V	20K PD	HSMV	GP-In	ISH_GPIO_9	SPKR	0	0	0	0
JTAG_PMODE	JTAG_PMODE	B19	N	1.8V	None	HSMV	Fn 1	JTAG_PMODE	0	0	0	0	0
JTAG_PRDY_N	JTAG_PRDY_N	C21	N	1.8V	20K PU	MSMV	Fn 1	JTAG_PRDY_N	0	0	0	0	0
JTAG_PREQ_N	JTAG_PREQ_N	C20	N	1.8V	20K PU	HSMV	Fn 1	JTAG_PREQ_N	0	0	0	0	0
JTAG_TCK	JTAG_TCK	B23	N	1.8V	20K PD	HSMV	Fn 1	JTAG_TCK	0	0	0	0	0
JTAG_TDI	JTAG_TDI	C22	N	1.8V	20K PU	HSMV	Fn 1	JTAG_TDI	0	0	0	0	0
JTAG_TDO	JTAG_TDO	A22	N	1.8V	20K PU	MSMV	Fn 1	JTAG_TDO	0	0	0	0	0
JTAG_TMS	JTAG_TMS	C23	N	1.8V	20K PU	HSMV	Fn 1	JTAG_TMS	0	0	0	0	0
JTAG_TRST_N	JTAG_TRST_N	C24	N	1.8V	20K PD	HSMV	Fn 1	JTAG_TRST_N	0	0	0	0	0
JTAGX	JTAGX	B21	N	1.8V	20K PU	HSMV	Fn 1	JTAGX	0	0	0	0	0
LPC_AD0	LPC_AD0	Y61	SW	1.8V/ 3.3V	20K PU	MSHV	GP-In	LPC_AD0	0	0	0	0	0
LPC_AD1	LPC_AD1	Y62	SW	1.8V/ 3.3V	20K PU	MSHV	GP-In	LPC_AD1	0	0	0	0	0
LPC_AD2	LPC_AD2	W62	SW	1.8V/ 3.3V	20K PU	MSHV	GP-In	LPC_AD2	0	0	0	0	0
LPC_AD3	LPC_AD3	W63	SW	1.8V/ 3.3V	20K PU	MSHV	GP-In	LPC_AD3	0	0	0	0	0

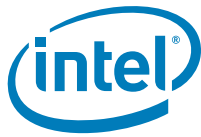


Table 2-34. SoC GPIO Multiplexing (Sheet 8 of 14)

GPIO No.	Signal Name	SoC Pin No.	Community	IO Voltage	Default Termination	Buffer Type	Default Mode	Fn 1	Fn 2	Fn 3	Fn 4	Fn 5	Fn 6
LPC_CLKOUT0	LPC_CLKOUT0	AB61	SW	1.8V/3.3V	None	MSHV	GP-In	LPC_CLKOUT0	0	0	0	0	0
LPC_CLKOUT1	LPC_CLKOUT1	AA62	SW	1.8V/3.3V	None	MSHV	GP-In	LPC_CLKOUT1	0	0	0	0	0
LPC_CLKRUN_N	LPC_CLKRUN_N	V62	SW	1.8V/3.3V	20K PU	MSHV	GP-In	LPC_CLKRUN_N	0	0	0	0	0
LPC_FRAME_N	LPC_FRAME_N	V61	SW	1.8V/3.3V	20K PU	MSHV	GP-In	LPC_FRAME_N	0	0	0	0	0
LPC_SERIRQ	LPC_SERIRQ	AB62	SW	1.8V/3.3V	20K PU	MSHV	GP-In	LPC_ILB_SERIRQ	0	0	0	0	0
GPIO_125	LPSS_I2C0_SCL	AR63	W	1.8V	20K PU	MSMV	GP-In	LPSS_I2C0_SCL	0	0	0	0	0
GPIO_124	LPSS_I2C0_SDA	AR62	W	1.8V	20K PU	MSMV	GP-In	LPSS_I2C0_SDA	0	0	0	0	0
GPIO_127	LPSS_I2C1_SCL	AM61	W	1.8V	20K PU	MSMV	GP-In	LPSS_I2C1_SCL	0	0	0	0	0
GPIO_126	LPSS_I2C1_SDA	AN62	W	1.8V	20K PU	MSMV	GP-In	LPSS_I2C1_SDA	0	0	0	0	0
GPIO_129	LPSS_I2C2_SCL	AP58	W	1.8V	20K PU	MSMV	GP-In	LPSS_I2C2_SCL	0	0	0	0	0
GPIO_128	LPSS_I2C2_SDA	AP59	W	1.8V	20K PU	MSMV	GP-In	LPSS_I2C2_SDA	0	0	0	0	0
GPIO_131	LPSS_I2C3_SCL	AL62	W	1.8V	20K PU	MSMV	GP-In	LPSS_I2C3_SCL	0	0	0	0	0
GPIO_130	LPSS_I2C3_SDA	AM62	W	1.8V	20K PU	MSMV	GP-In	LPSS_I2C3_SDA	0	0	0	0	0
GPIO_133	LPSS_I2C4_SCL	AP54	W	1.8V	20K PU	MSMV	GP-In	LPSS_I2C4_SCL	0	0	0	0	0
GPIO_132	LPSS_I2C4_SDA	AP52	W	1.8V	20K PU	MSMV	GP-In	LPSS_I2C4_SDA	0	0	0	0	0
GPIO_135	LPSS_I2C5_SCL	AP51	W	1.8V	20K PU	MSMV	GP-In	LPSS_I2C5_SCL	ISH_I2C0_SCL	0	0	0	0
GPIO_134	LPSS_I2C5_SDA	AP49	W	1.8V	20K PU	MSMV	GP-In	LPSS_I2C5_SDA	ISH_I2C0_SDA	0	0	0	0

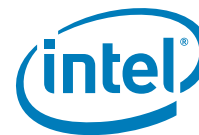


Table 2-34. SoC GPIO Multiplexing (Sheet 9 of 14)

GPIO No.	Signal Name	SoC Pin No.	Community	IO Voltage	Default Termination	Buffer Type	Default Mode	Fn 1	Fn 2	Fn 3	Fn 4	Fn 5	Fn 6
GPIO _137	LPSS_I2C6_SCL	AK6 1	W	1.8V	20K PU	MSMV	GP-In	LPSS_I2C6_SCL	ISH_I2C1_SCL	0	0	0	0
GPIO _136	LPSS_I2C6_SDA	AL6 3	W	1.8V	20K PU	MSMV	GP-In	LPSS_I2C6_SDA	ISH_I2C1_SDA	0	0	0	0
GPIO _139	LPSS_I2C7_SCL	AP6 1	W	1.8V	20K PU	MSMV	GP-In	LPSS_I2C7_SCL	ISH_I2C2_SCL	0	0	0	0
GPIO _138	LPSS_I2C7_SDA	AP6 2	W	1.8V	20K PU	MSMV	GP-In	LPSS_I2C7_SDA	ISH_I2C2_SDA	0	0	0	0
GPIO _41	LPSS_UART0_CTS_N	C44	N	1.8V	20K PU	LSMV	GP-In	LPSS_UAR T0_C TS_N	RSVD	0	0	0	0
GPIO _40	LPSS_UART0_RTS_N	A46	N	1.8V	20K PU	LSMV	GP-Out	LPSS_UAR T0_R TS_N	RSVD	0	0	0	0
GPIO _38	LPSS_UART0_RXD	C45	N	1.8V	20K PU	LSMV	GP-In	LPSS_UAR T0_R XD	RSVD	0	0	0	0
GPIO _39	LPSS_UART0_TXD	B45	N	1.8V	20K PU	LSMV	GP-Out	LPSS_UAR T0_T XD	RSVD	0	0	0	0
GPIO _45	LPSS_UART1_CTS_N	C42	N	1.8V	20K PU	LSMV	GP-In	LPSS_UAR T1_C TS_N	RSVD	0	0	0	0
GPIO _44	LPSS_UART1_RTS_N	A42	N	1.8V	20K PU	LSMV	GP-Out	LPSS_UAR T1_R TS_N	RSVD	0	0	0	0
GPIO _42	LPSS_UART1_RXD	C43	N	1.8V	20K PU	LSMV	GP-In	LPSS_UAR T1_R XD	RSVD	0	0	0	0
GPIO _43	LPSS_UART1_TXD	B43	N	1.8V	20K PU	LSMV	GP-Out	LPSS_UAR T1_T XD	RSVD	0	0	0	0
GPIO _49	LPSS_UART2_CTS_N	M41	N	1.8V	20K PU	LSMV	GP-In	LPSS_UAR T2_C TS_N	RSVD	0	0	0	0
GPIO _48	LPSS_UART2_RTS_N	L41	N	1.8V	20K PU	LSMV	GP-Out	LPSS_UAR T2_R TS_N	RSVD	0	0	0	0
GPIO _46	LPSS_UART2_RXD	J41	N	1.8V	20K PU	LSMV	GP-In	LPSS_UAR T2_R XD	RSVD	0	0	0	0

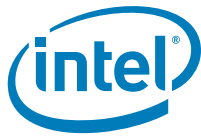


Table 2-34. SoC GPIO Multiplexing (Sheet 10 of 14)

GPIO No.	Signal Name	SoC Pin No.	Community	IO Voltage	Default Termination	Buffer Type	Default Mode	Fn 1	Fn 2	Fn 3	Fn 4	Fn 5	Fn 6
GPIO_47	LPSS_UART2_TXD	H41	N	1.8V	20K PU	LSMV	GP-Out	LPSS_UART2_TXD	RSVD	0	0	0	0
GPIO_201	MDSI_A_TE	M45	NW	1.8V	20K PD	LSMV	Fn 1	MDSI_A_TE	0	0	0	0	0
GPIO_202	MDSI_C_TE	M43	NW	1.8V	20K PD	LSMV	Fn 1	MDSI_C_TE	0	0	0	0	0
GPIO_192	MIPI_I2C_SCL	C51	NW	1.8V	20K PD	MSMV	Fn 1	MIPI_I2C_SCL	0	0	0	0	0
GPIO_191	MIPI_I2C_SDA	B51	NW	1.8V	20K PD	MSMV	Fn 1	MIPI_I2C_SDA	0	0	0	0	0
NCTF	NCTF	H48	NW	1.8V	None	LSMV	Fn 1	RSVD	0	0	0	0	0
OSC_CLK_OUT_0	OSC_CLK_OUT_0	AG62	W	1.8V	20K PD	HSMV	Fn 1	OSC_CLK_OUT_0	0	0	0	0	0
OSC_CLK_OUT_1	OSC_CLK_OUT_1	AF61	W	1.8V	20K PD	HSMV	Fn 1	OSC_CLK_OUT_1	0	0	0	0	0
OSC_CLK_OUT_2	OSC_CLK_OUT_2	AG63	W	1.8V	20K PD	HSMV	Fn 1	OSC_CLK_OUT_2	0	0	0	0	0
OSC_CLK_OUT_3	OSC_CLK_OUT_3	AE60	W	1.8V	20K PD	HSMV	Fn 1	OSC_CLK_OUT_3	0	0	0	0	0
GPIO_209	PCIE_CLKREQ0_N	AK62	W	1.8V	20K PU	HSMV	Fn 1	PCIE_CLKREQ0_N	RSVD	0	0	0	0
GPIO_210	PCIE_CLKREQ1_N	AH62	W	1.8V	20K PU	HSMV	Fn 1	PCIE_CLKREQ1_N	0	0	0	0	0
GPIO_211	PCIE_CLKREQ2_N	AH61	W	1.8V	20K PU	HSMV	Fn 1	PCIE_CLKREQ2_N	0	0	0	0	0
GPIO_212	PCIE_CLKREQ3_N	AJ62	W	1.8V	20K PU	HSMV	Fn 1	PCIE_CLKREQ3_N	RSVD	0	0	0	0
GPIO_205	PCIE_WAKE0_N	R62	SW	1.8V	20K PU	HSMV	GP-In	PCIE_WAKE0_N	RSVD	0	0	0	0
GPIO_206	PCIE_WAKE1_N	P62	SW	1.8V	20K PU	HSMV	GP-In	PCIE_WAKE1_N	RSVD	0	0	0	0



Table 2-34. SoC GPIO Multiplexing (Sheet 11 of 14)

GPIO No.	Signal Name	SoC Pin No.	Community	IO Voltage	Default Termination	Buffer Type	Default Mode	Fn 1	Fn 2	Fn 3	Fn 4	Fn 5	Fn 6
GPIO_207	PCIE_WAKE2_N	P61	SW	1.8V	20K PU	HSMV	GP-In	PCIE_WAKE2_N	RSVD	0	0	0	0
GPIO_208	PCIE_WAKE3_N	N62	SW	1.8V	20K PU	HSMV	GP-In	PCIE_WAKE3_N	RSVD	0	0	0	0
PMC_SPI_CLK	PMC_SPI_CLK	E52	NW	1.8V	20K PD	LSMV	Fn 1	PMC_SPI_CLK	0	0	0	0	0
PMC_SPI_FS0	PMC_SPI_FS0	L48	NW	1.8V	20K PU	LSMV	Fn 1	PMC_SPI_FS0	0	0	0	0	0
PMC_SPI_FS1	PMC_SPI_FS1	P48	NW	1.8V	20K PU	LSMV	Fn 1	PMC_SPI_FS1	DDI2_HPDP	0	0	0	0
PMC_SPI_FS2	PMC_SPI_FS2	M48	NW	1.8V	20K PU	LSMV	Fn 1	PMC_SPI_FS2	FST_SPI_CS2_N	0	0	0	0
PMC_SPI_RXD	PMC_SPI_RXD	J50	NW	1.8V	20K PD	LSMV	Fn 1	PMC_SPI_RXD	0	0	0	0	0
PMC_SPI_TXD	PMC_SPI_TXD	H50	NW	1.8V	20K PD	LSMV	Fn 1	PMC_SPI_TXD	0	0	0	0	0
PMIC_I2C_SCL	PMIC_I2C_SCL	H45	NW	1.8V	1K PU	MSMV	Fn 1	PMIC_I2C_SCL	0	0	0	0	0
PMIC_I2C_SDA	PMIC_I2C_SDA	F47	NW	1.8V	1K PU	MSMV	Fn 1	PMIC_I2C_SDA	0	0	0	0	0
GPIO_220	PMU_AC_PRESENT	AK49	W	1.8V/3.3V	20K PD	MSHV	GP-In	PMU_AC_PRESENT	0	0	0	0	0
PMU_BATLOW_N	PMU_BATLOW_N	AH51	W	1.8V/3.3V	20K PU	MSHV	Fn 1	PMU_BATLOW_N	0	0	0	0	0
PMU_PLTRST_N	PMU_PLTRST_N	AG57	W	1.8V/3.3V	None	MSHV	Fn 1	PMU_PLTRST_N	0	0	0	0	0
PMU_PWRBTN_N	PMU_PWRBTN_N	AK55	W	1.8V/3.3V	20K PU	MSHV	Fn 1	PMU_PWRBTN_N	0	0	0	0	0
PMU_RSTBTN_N	PMU_RSTBTN_N	AD62	W	1.8V/3.3V	None	MSHV	Fn 1	PMU_RSTBTN_N	0	0	0	0	0
PMU_SLP_S0_N	PMU_SLP_S0_N	AD61	W	1.8V/3.3V	None	MSHV	Fn 1	PMU_SLP_S0_N	0	0	0	0	0
PMU_SLP_S3_N	PMU_SLP_S3_N	AC62	W	1.8V/3.3V	None	MSHV	Fn 1	PMU_SLP_S3_N	0	0	0	0	0

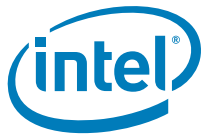


Table 2-34. SoC GPIO Multiplexing (Sheet 12 of 14)

GPIO No.	Signal Name	SoC Pin No.	Community	IO Voltage	Default Termination	Buffer Type	Default Mode	Fn 1	Fn 2	Fn 3	Fn 4	Fn 5	Fn 6
PMU_SLP_S4_N	PMU_SLP_S4_N	AK54	W	1.8V/3.3V	None	MSHV	Fn 1	PMU_SLP_S4_N	0	0	0	0	0
PMU_SUSCLK	PMU_SUSCLK	AE62	W	1.8V/3.3V	None	MSHV	Fn 1	PMU_SUSCLK	0	0	0	0	0
GPIO_195	PNL0_BKLCTL	C46	NW	1.8V	20K PD	LSMV	Fn 1	PNL0_BKLCTL	0	0	0	0	0
GPIO_194	PNL0_BKLTEN	B47	NW	1.8V	20K PD	LSMV	Fn 1	PNL0_BKLTEN	0	0	0	0	0
GPIO_193	PNL0_VDDEN	C47	NW	1.8V	20K PD	LSMV	Fn 1	PNL0_VDDEN	0	0	0	0	0
GPIO_198	PNL1_BKLCTL	C53	NW	1.8V	20K PD	LSMV	Fn 1	PNL1_BKLCTL	0	0	0	0	0
GPIO_197	PNL1_BKLTEN	B53	NW	1.8V	20K PD	LSMV	Fn 1	PNL1_BKLTEN	0	0	0	0	0
GPIO_196	PNL1_VDDEN	C52	NW	1.8V	20K PD	LSMV	Fn 1	PNL1_VDDEN	0	0	0	0	0
PROC_HOT_N	PROC_HOT_N	E47	NW	1.8V	20K PU	LSMV	Fn 1	PROC_HOT_N	0	0	0	0	0
GPIO_34	PWM0	B41	N	1.8V	20K PD	LSMV	GP-In	PWM0	0	0	0	0	0
GPIO_35	PWM1	C41	N	1.8V	20K PD	LSMV	GP-In	PWM1	0	0	0	0	0
GPIO_36	PWM2	F41	N	1.8V	20K PD	LSMV	GP-In	PWM2	0	0	0	0	0
GPIO_37	PWM3	E41	N	1.8V	20K PD	LSMV	GP-In	PWM3	0	0	0	0	0
GPIO_177	SDCARD_CD_N	AB54	SW	1.8V	20K PD	HSMV	GP-In	SDCARD_CD_N	RSVD	0	0	0	0
GPIO_172	SDCARD_CLK	AB58	SW	1.8V/3.3V	20K PD	HSHV	GP-In	SDCARD_CLK	RSVD	0	0	0	0
GPIO_178	SDCARD_CMD	AC52	SW	1.8V/3.3V	20K PD	HSHV	GP-In	SDCARD_CMD	RSVD	0	0	0	0
GPIO_173	SDCARD_D0	AC49	SW	1.8V/3.3V	20K PD	HSHV	GP-In	SDCARD_D0	RSVD	0	0	0	0
GPIO_174	SDCARD_D1	AC48	SW	1.8V/3.3V	20K PD	HSHV	GP-In	SDCARD_D1	RSVD	0	0	0	0
GPIO_175	SDCARD_D2	AC51	SW	1.8V/3.3V	20K PD	HSHV	GP-In	SDCARD_D2	RSVD	0	0	0	0



Table 2-34. SoC GPIO Multiplexing (Sheet 13 of 14)

GPIO No.	Signal Name	SoC Pin No.	Community	IO Voltage	Default Termination	Buffer Type	Default Mode	Fn 1	Fn 2	Fn 3	Fn 4	Fn 5	Fn 6
GPIO _176	SDCARD_D3	AB5 1	SW	1.8V/ 3.3V	20K PD	HSBV	GP-In	SDCA RD_D 3	RSVD	0	0	0	0
GPIO _186	SDCARD_LVL_WP	AB5 5	SW	1.8V	20K PD	HSMV	GP-In	SDCA RD_L VL_W P	RSVD	0	0	0	0
GPIO _104	SIO_SPI_0_CLK	F54	NW	1.8V	20K PD	HSMV	GP-In	SIO_ SPI_0 _CLK	RSVD	0	0	0	0
GPIO _105	SIO_SPI_0_FS0	F52	NW	1.8V	20K PD	HSMV	GP-Out	SIO_ SPI_0 _FS0	RSVD	0	0	0	0
GPIO _106	SIO_SPI_0_FS1	H52	NW	1.8V	20K PD	HSMV	GP-Out	SIO_ SPI_0 _FS1	RSVD	FST_ SPI_ CS2_ N	0	0	0
GPIO _109	SIO_SPI_0_RXD	H54	NW	1.8V	20K PD	HSMV	GP-In	SIO_ SPI_0 _RXD	RSVD	0	0	0	0
GPIO _110	SIO_SPI_0_TXD	J52	NW	1.8V	20K PD	HSMV	GP-In	SIO_ SPI_0 _TXD	RSVD	0	0	0	0
GPIO _111	SIO_SPI_1_CLK	F58	NW	1.8V	20K PD	HSMV	GP-In	SIO_ SPI_1 _CLK	0	0	0	0	0
GPIO _112	SIO_SPI_1_FS0	K55	NW	1.8V	20K PD	HSMV	GP-Out	SIO_ SPI_1 _FS0	RSVD	0	0	0	0
GPIO _113	SIO_SPI_1_FS1	F61	NW	1.8V	20K PD	HSMV	GP-Out	SIO_ SPI_1 _FS1	RSVD	0	0	0	0
GPIO _116	SIO_SPI_1_RXD	H57	NW	1.8V	20K PD	HSMV	GP-In	SIO_ SPI_1 _RXD	RSVD	0	0	0	0
GPIO _117	SIO_SPI_1_TXD	H58	NW	1.8V	20K PD	HSMV	GP-In	SIO_ SPI_1 _TXD	RSVD	0	0	0	0
GPIO _118	SIO_SPI_2_CLK	F62	NW	1.8V	20K PD	HSMV	GP-In	SIO_ SPI_2 _CLK	RSVD	RSVD	0	0	0
GPIO _119	SIO_SPI_2_FS0	D61	NW	1.8V	20K PD	HSMV	GP-Out	SIO_ SPI_2 _FS0	RSVD	RSVD	0	0	0
GPIO _120	SIO_SPI_2_FS1	E56	NW	1.8V	20K PD	HSMV	GP-Out	SIO_ SPI_2 _FS1	RSVD	RSVD	0	0	0
GPIO _121	SIO_SPI_2_FS2	D59	NW	1.8V	20K PD	HSMV	GP-In	SIO_ SPI_2 _FS2	RSVD	RSVD	0	0	0
GPIO _122	SIO_SPI_2_RXD	C62	NW	1.8V	20K PD	HSMV	GP-In	SIO_ SPI_2 _RXD	RSVD	RSVD	0	0	0

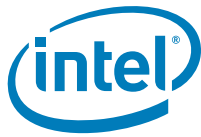
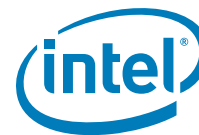


Table 2-34. SoC GPIO Multiplexing (Sheet 14 of 14)

GPIO No.	Signal Name	SoC Pin No.	Community	IO Voltage	Default Termination	Buffer Type	Default Mode	Fn 1	Fn 2	Fn 3	Fn 4	Fn 5	Fn 6
GPIO_123	SIO_SPI_2_TXD	E62	NW	1.8V	20K PD	HSMV	GP-In	SIO_SPI_2_TXD	RSVD	RSVD	0	0	0
SMB_ALERT_N	SMB_ALERT_N	R63	SW	1.8V/ 3.3V	20K PU	MSHV	GP-In	SMB_ALERT_N	0	0	0	0	0
SMB_CLK	SMB_CLK	T62	SW	1.8V/ 3.3V	20K PU	MSHV	GP-In	SMB_CLK	LPSS_I2C7_SCL	0	0	0	0
SMB_DATA	SMB_DATA	T61	SW	1.8V/ 3.3V	20K PU	MSHV	GP-In	SMB_DATA	LPSS_I2C7_SDA	0	0	0	0
SUS_STAT_N	SUS_STAT_N	AG58	W	1.8V/ 3.3V	None	MSHV	Fn 1	SUS_STAT_B	0	0	0	0	0
SUSP_WRD_NACK	SUSP_WRD_NACK	AC63	W	1.8V/ 3.3V	None	MSHV	Fn 1	SUSP_WRD_NACK	0	0	0	0	0
SVID0_ALERT_N	SVID0_ALERT_N	B17	N	1.05V	None	MSMV	Fn 1	SVID0_ALERT_N	0	0	0	0	0
SVID0_CLK	SVID0_CLK	C17	N	1.05V	20K PU	MSMV	Fn 1	SVID0_CLK	0	0	0	0	0
SVID0_DATA	SVID0_DATA	C18	N	1.05V	20K PU	MSMV	Fn 1	SVID0_DATA	0	0	0	0	0
THERMTRIP_N	THERMTRIP_N	J47	NW	1.8V	20K PU	LSMV	Fn 1	THERMTRIP_N	0	0	0	0	0
GPIO_203	USB_OC0_N	B55	NW	1.8V	20K PU	LSMV	Fn 1	USB_OC0_N	RSVD	0	0	0	0
GPIO_204	USB_OC1_N	C55	NW	1.8V	20K PU	LSMV	Fn 1	USB_OC1_N	RSVD	RSVD	0	0	0



2.32 Wake Events

Table 2-35. Wake Events (Sheet 1 of 2)

Wake Event	Interrupt Type	Windows* OS Wake Requirements				SoC Implementation		Comments
		SoC	C-MS	D-MS	S3	Interrupt Type	Description	
Timers								
RTC	N/A	Y	N	N	N/A	Timer Interrupt	N/A	
Always On Times/Watch Dog Time	N/A	Y	N	N	N/A	Timer Interrupt	N/A	Note: No AONT (Always On Timer) in Win10
Buttons								
Power Button	SCI	Y	Y	Y	Y	SCI/EC	N/A	Note: HID event filter/ Virtual Button Driver
Home Button	GPIO	Y	Y	Y	N	SCI/EC	N/A	
LID SWTCH	GPIO	Y	Y	Y	N	SCI/EC	N/A	
Communication Devices								
Wi-Fi Radio	GPIO	Y	Y (See Notes)	N	N	Direct Wake	GPIO_111 (WAKE_TO_HOST)	Notes: 1. NDIS 6.3 compliant for WOL patterns, protocol off-loads and D0 packet coalescing 2. On critical alert or activity detection
MBB Radio	USB PME	Y	Y (See Notes)	N	N	PME	In band	Note: On critical alert or activity detection
Bluetooth* Radio	GPIO	Y	Y (See note)	N/A	N	Direct Wake	GPIO_10 (BT_HOST_WAKE)	Note: CS wake for Keyboard/ Mouse only (see below)
Wired LAN	PCIe* WAKE#	Y	Y (See Note)	N	Y	N/A	GPIO	Note: Pattern match offload to device
Input Devices								
Keyboard (USB)	USB PME	Y	Y	Y	Y	PME	SCI	Note: All keys generate INT (including VUP and VDN)
Keyboard Bluetooth*	GPIO	Y	Y	Y	N	Direct Wake	GPIO_10 (BT_HOST_WAKE)	
TrackPad (HID ² C)	GPIO	Y	Y	Y	N	DIRQ/ Direct Wake/GPE	GPIO_18	Note: BIOS changes to SCI when entering S3 state
TrackPad (USB)	USB PME	Y	Y	Y	Y	PME	SCI	
Mouse (USB)	USB PME	Y	Y	Y	Y	PME	SCI	
Mouse (Bluetooth*)	GPIO	Y	Y	Y	N	Direct Wake	GPIO_10 (BT_HOST_WAKE)	

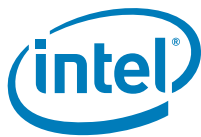
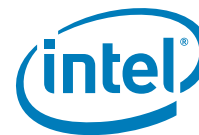


Table 2-35. Wake Events (Sheet 2 of 2)

Wake Event	Interrupt Type	Windows* OS Wake Requirements				SoC Implementation		Comments
Devices Insertion / Removal								
Insert USB Device	USB PME	Y	N	N	N	PME	SCI	
Remove USB Device	USB PME	Y	N	N	N	PME	SCI	
Insert SDC	USB PME	Y	N	N	N	PME	SCI	Note: USB attached
Insert SDC	GPIO	Y	N	N	N			
Remove SDC	USB PME	Y	N	N	N	PME	SCI	Note: USB attached
Remove SDC	GPIO	Y	N	N	N			
Attach to Dock	Varies	Y	See Note	See Note	N/A	USB PME	SCI	Note: Depends on device in dock and their state (USB Dock support ONLY)
Remove from Dock	Varies	Y	See Note	See Note	N/A	USB PME	SCI	Note: Depends on device in dock and their state (USB Dock support ONLY)
Environmental Context Changes								
Power Source change	GPIO	Y	Y	N	N	EC (GPIO_11)	SOC_RUNTIME_SCI_N	
Thermal event	GPIO	Y	N	N	N	EC (GPIO_11)	SOC_RUNTIME_SCI_N	
Battery charge complete	GPIO	Y	N	N	N	EC (GPIO_11)	SOC_RUNTIME_SCI_N	
BATT LOW	GPIO	Y	Y	N	N	EC (GPIO_11)	SOC_RUNTIME_SCI_N	
Audio Interrupt	Audio_INT	Y	Y	Y	N	Direct Wake	GPIO_116	Note: DMIC powered on for VT
Notes: 1. The SoC may not go into S0ix depending on, on-going back ground activities and actions 2. C-MS - Connected Modern Standby 3. D-MS - Disconnected Modern Standby 4. S3 -Platform S3 Power State 5. HID - Human Interface Device 6. NDIS - Network Driver Interface Specification 7. PME - Power Management Event 8. SCI - System Control Interrupt 9. EC - Embedded Controller 10. MBB - Mobile Broadband 11. DMIC - Digital Microphone 12. VT - Virtualization Technology								



3 Functional Description

3.1 Processor Core Overview

Table 3-1. Processor Core Overview

Category	Feature Description
CPU Cores	Quad/Dual IA Processor Core 2 modules of 2 cores each for Quad Core - Supporting Out of Order Execution (OOE) 14 nm processor Technology
Modules/Caches	2 Modules 2 Cores grouped per Module (Dual-Core Module) - On-die, 32KiB 8-way L1 instruction cache and 24KiB 6-way L1 data cache per core - On-die, 1MiB, 16-way L2 unified cache, shared per two core (module)
Architecture	Intel® 64 Bit
Virtualization architecture	Intel's full virtualization architecture support - VTx-2 with Extended Page Table - VT-d
Burst Technology	1/2/3/4 Core Burst Technology
Thermal Management	Supported by means of Intel® Thermal Monitor (TM1 and TM2)
Power Management	- Support Connected Standby, Modern Standby and Lucid Sleep - Support system states: S0, S0ix, S3, S4/S5, and RTD3 - Uses Power Aware Interrupt Routing (PAIR)
Boot feature	Support boot from SPI (secure and non-secure)
Other features	- Support for a Digital Random Number Generator (DRNG) - Support for Intel Carry-Less Multiplication Instruction (PCLMULQDQ)

3.2 System Memory Controller

3.2.1 Supported Memory Overview

The SoC Memory Controller supports the following Memory Technologies on two independent 64-bit channels.

Table 3-2. Specifics of Supported Memory Technologies (Sheet 1 of 2)

Technology Attributes	LPDDR4	LPDDR3	DDR3L
Channels	4 (x32)	4 (x32)	2 (x64)
Peak Bandwidth (GB/s)	38.4	29.86	29.86
Maximum Data Transfer Rate (MT/s)	1600/2133/2400	1333/1600/1867	1333/1600/1867
Maximum Total System Capacity	8GB	8GB	8GB
Raw Card Support	N/A	N/A	A(2Rx16) B(1Rx8) C(1Rx16) F(2Rx8)
Densities (Gb)	8, 12, 16	4, 8	4, 8

Table 3-2. Specifics of Supported Memory Technologies (Sheet 2 of 2)

Technology Attributes	LPDDR4	LPDDR3	DDR3L
CMD/Adds pins per channel	6	10	22
DQ pins per channel	32	32	64
Voltage Rail (V)	1.1	1.24	1.35
Scrambling	Yes		
On Die Termination Control	Yes		
Rank Interleaving	Yes		
Refresh	No per bank-refresh, only at rank level		
Power Saving Features	Fast Exit Power Down, Self Refresh plus extra features, Power/trunk gating		

3.2.2 Memory Configurations

SoC supports different configurations for channel population, SO-DIMM and Memory Down (DRAM) configurations. The tables below list the configurations and limitations for platform design.

Table 3-4. Channel Operating Rules (Sheet 1 of 2)

Channel Configurations (Applies to All Speeds)	SoC
Mixed Capacity Rules	
Channel 1 capacity $\geq$ Channel 0 capacity (Memory Down or SO-DIMM, if both channels are populated)	Supported Notes: 1. This applies to DDR3L. 2. Configurations with a capacity imbalance across channels are not recommended as it leads to performance imbalance. Adding capacity to one channel will result in unpredictable performance losses relative to matching the smaller capacity on both channels. Applications which are allocated performance critical pages in the unmatched region will experience half memory bandwidth. 3. CH0 devices or raw cards need not be the same as CH1. Mixing different speeds will result in all channels running at the slowest common speed. 4. For LPDDR3/LPDDR4, all populated channels need to be identical in capacity.
Channel 0 capacity $\geq$ Channel 1 capacity (Memory Down or SO-DIMM, if both channels are populated)	Supported Notes: 1. This applies to DDR3L. 2. Configurations with a capacity imbalance across channels are not recommended as it leads to performance imbalance. Adding capacity to one channel will result in unpredictable performance losses relative to matching the smaller capacity on both channels. Applications which are allocated performance critical pages in the unmatched region will experience half memory bandwidth. 3. CH0 devices or raw cards need not be the same as CH1. Mixing different speeds will result in all channels running at the slowest common speed. 4. For LPDDR3/LPDDR4, all populated channels need to be identical in capacity.
Mixed Configuration Rules	

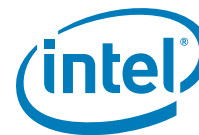


Table 3-4. Channel Operating Rules (Sheet 2 of 2)

Channel Configurations (Applies to All Speeds)	SoC
Support mixture of DRAM vendors in Memory Down configuration across channels	Supported Notes: 1. For SO-DIMM this will be taken care by the specific SPD. But for DRAMs the BIOS will need to include the DRAM identification. 2. Applies to DDR3L. 3. For LPDDR3/LPDDR4, all populated channels need to be identical in configuration.
Mixed Technology / Speed / Rank Rules	
Support for Mixed speeds across channels	Supported Notes: 1. Mixing different speeds will result in all channels running at the slowest common speed. 2. For LPDDR3/LPDDR4, all populated channels need to be identical in technology and speed.
Single Rank and Dual Rank Devices across channels	Supported Notes: 1. Configurations with a capacity imbalance across channels are not recommended as it leads to performance imbalance. Adding capacity to one channel will result in unpredictable performance losses relative to matching the smaller capacity on both channels. Applications which are allocated performance critical pages in the unmatched region will experience half memory bandwidth. 2. For LPDDR3/LPDDR4, all populated channels need to be identical in ranks.

Table 3-5. DDR3L Channel Configuration Support

DRAM Package	Ranks per Package	Density per DRAM Die (Gb)	DQ Width per DRAM	Number of DRAM Die per Package	DRAM Package Capacity (GB)	Number of Packages to Form a x64 Non-ECC Channel
SDP	1	4	16	1	0.5	4
DDP	2	4	16	2	1	4
SDP	1	4	8	1	0.5	8
DDP	2	4	8	2	1	8
SDP	1	8	16	1	1	4
DDP	2	8	16	2	2	4
SDP	1	8	8	1	1	8

Table 3-6. LPDDR3 Memory Configurations

Devices per Package	DQs per Package	Ranks	Device Density (Gb)	DQ Width per Device	DRAM Package Capacity (GB)
SDP	x32	1	4	32	0.5
DDP	x32	2	4	32	1
SDP	x32	1	6	32	0.75
DDP	x32	2	6	32	1.5

Table 3-6. LPDDR3 Memory Configurations

Devices per Package	DQs per Package	Ranks	Device Density (Gb)	DQ Width per Device	DRAM Package Capacity (GB)
QDP	x32	2	6	16	3
SDP	x32	1	8	32	1
DDP	x32	2	8	32	2
QDP	x32	2	8	16	4

Table 3-7. LPDDR4 Memory Configurations

Devices per Package	DQs per Package	Ranks	Device Density (Gb)	DQ Width per Device	DRAM Package Capacity (GB)
SDP	x32	1	8	2x16	1
DDP	x32	2	8	2x16	2
SDP	x32	1	12	2x16	1.5
DDP	x32	2	12	2x16	3
SDP	x32	1	16	2x16	2
DDP	x32	2	16	2x16	4
QDP	x32	2	8	2x16	4

Table 3-8. LPDDR4 x32 Configuration Support

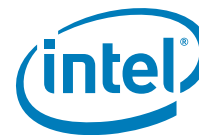
CH0 (CH0_DQB)	CH1 (CH0_DQA)	CH2 (CH1_DQB)	CH3 (CH1_DQA)	Restrictions
x32 BGA	x32 BGA	x32 BGA	x32 BGA	All Channels Identical
x32 BGA	Unpopulated	Unpopulated		Only on CH0
x32 BGA	x32 BGA	Unpopulated		CH0 identical to CH1

3.3 Display Controller

The Gen9 Display Engine (DE) provides the ability to connect up to three displays to the SoC using MIPI-DSI, eDP, and DP/HDMI. When only a single internal display is used (MIPI-DSI or eDP), DE can employ power optimizations to reduce power.

3.3.1 Features of Display Controller

- Support 3 Display pipes, simultaneous multi-streaming on all three display pipes (1x Internal and 2x External Displays)
- Support 2 MIPI-DSI 1.1 ports
- Support 3 DDI ports to enable eDP 1.3, DP 1.2, or HDMI 1.4b
 - Supports 1x Internal Display (eDP 1.3). DDI2 port is dedicated to eDP
 - Supports 2x External Display (DP 1.2, HDMI 1.4b). DDI0 and DDI1 can be used for external displays
- Supports Audio on DP and HDMI
- Supports Multi Plane Overlay (MPO)



- Supports Intel® Display Power Saving Technology (DPST) 6.3, Panel Self Refresh (PSR) and Display Refresh Rate Switching Technology (DRRS)

Table 3-9. Display Features

Feature	MIPI-DSI	eDP	DP	HDMI
Number of Ports	2 (x4)	1 (x4) (DDI-2)	1 (x4) DDI[1:0]	1 (x4) DDI[1:0]
Maximum Resolution	1x4: 1920x1200 @ 60 Hz (without compression) 2x4: 2560x1600 @ 60 Hz (without compression)	3840x2160 @ 60 Hz, with SSC	4096x2160 @ 60 Hz, with SSC	3840x2160@ 30 Hz
Data Rate	1.0 Gb/s	5.4 Gb/s	5.4 Gb/s	2.9 Gb/s
Standard	DPHY1.1	eDP 1.3	DP 1.2	HDMI 1.4b
Power gated during S0ix w/display off	Yes	Yes	Yes	Yes
DRRS (Refresh reduction)	Yes (M/N pair)	Yes (Panel command)	N/A	N/A
Self-Refresh with Frame buffer in Panel	Yes (Command Mode)	Yes (PSR)	No	No
Content-Based back light control	DPST6.0	DPST6/CABC	N/A	N/A
HDCP wired display	N/A	N/A (ASSR support)	1.4	1.4
PAVP	AES-encrypted buffer, plane control, panic attack			
SEC	All display registers can be accessed by CEC			
HD-Audio	N/A	N/A	Yes	Yes
LPE Audio	N/A	N/A	Yes	Yes
Compressed Audio	N/A	N/A	Yes	Yes

3.4 Graphics and Media Engine

- Intel 9th generation (Gen 9) LP graphics and media encode/decode engine
- Three slices of 6 EUs each (3x6); each slice supports 6 threads resulting in a total of 108 available threads
- Supports 3-D rendering, media compositing, and video encoding.
- Graphics Burst enabled through energy counters.
- Supports DX* (9.3, 10, 11.1, 12), OpenGL* 4.4, OGL ES 3.0, OpenCL* 2.0
- 4x anti-aliasing
- Supports Content protection using PAVP 2.0 and HDCP 1.4/2.0.

Table 3-10. Hardware Accelerated Video Decode/Encode Codec Support (Sheet 1 of 2)

Codec Format	Decode Level	Encode Level
HEVC (H.265)	MP L5.1: Up to 4kx2kp (3840x2160) @ 60Hz (8b/10b) MP L5: Up to 4kx2kp (3840x2160) @ 30Hz (8b/10b)	MP L5: 4kx2kp (3840x2160) @ 30Hz (8b, Up to 100Mbps)

Table 3-10. Hardware Accelerated Video Decode/Encode Codec Support (Sheet 2 of 2)

Codec Format	Decode Level	Encode Level
H.264	CBP, MP, HP L5.2: Up to 1080p (1920x1080) @ 240Hz, 4kx2kp (3840x2160) @ 60Hz	CBP, MP HP L5.2: Up to 1080p (1920x1080) @ 240Hz, 4kx2kp (3840x2160) @ 60Hz
MVC	CBP, MP, HP L5.2: Up to 4kx2kp (3840x2160) @ 60Hz	CBP, MP, HP L5.1: Up to 4kx2kp (3840x2160) @ 30Hz
VP8	Up to 4kx2kp (3840x2160) @ 60Hz	Up to 4kx2kp (3840x2160) @ 30Hz
VP9	Up to 4kx2kp (3840x2160) @ 60Hz	Up to 480p30 Note: Software based only
MPEG2	HD, MP, HL: Up to 1080p (1920x1080) @ 60Hz	N/A
VC-1	AP L4: Up to 1080p (1920x1080) @ 60Hz	N/A
WMV9	MP, HL: Up to 1080p (1920x1080) @ 30Hz	N/A
JPEG/MJPEG	1067 Mpps (420), 800 Mpps (422), 533 Mpps (444)	1067 Mpps (420), 800 Mpps (422), 533 Mpps (444)

Note: Table above describes the hardware accelerated video decode/encode CODEC support capability of the processor. Software support of these capabilities may vary depending on the version of operating system and driver.

3.5 Imaging

The SoC consists of the Processing Subsystem (PS), which is an advanced Image Signal Processor (ISP), and the Input Subsystem (IS), which contains the MIPI*-CSI2 controllers.

Supports four concurrent streams from four operating sensors.

3.5.1 Camera Configurations

SoC supports CSI2 image sensors connected using both D-PHY 1.1 and D-PHY 1.2. There are two input blocks. One input block supports two sensors on D-PHY 1.1 lanes, and the other input block supports two sensors on D-PHY 1.2 lanes.

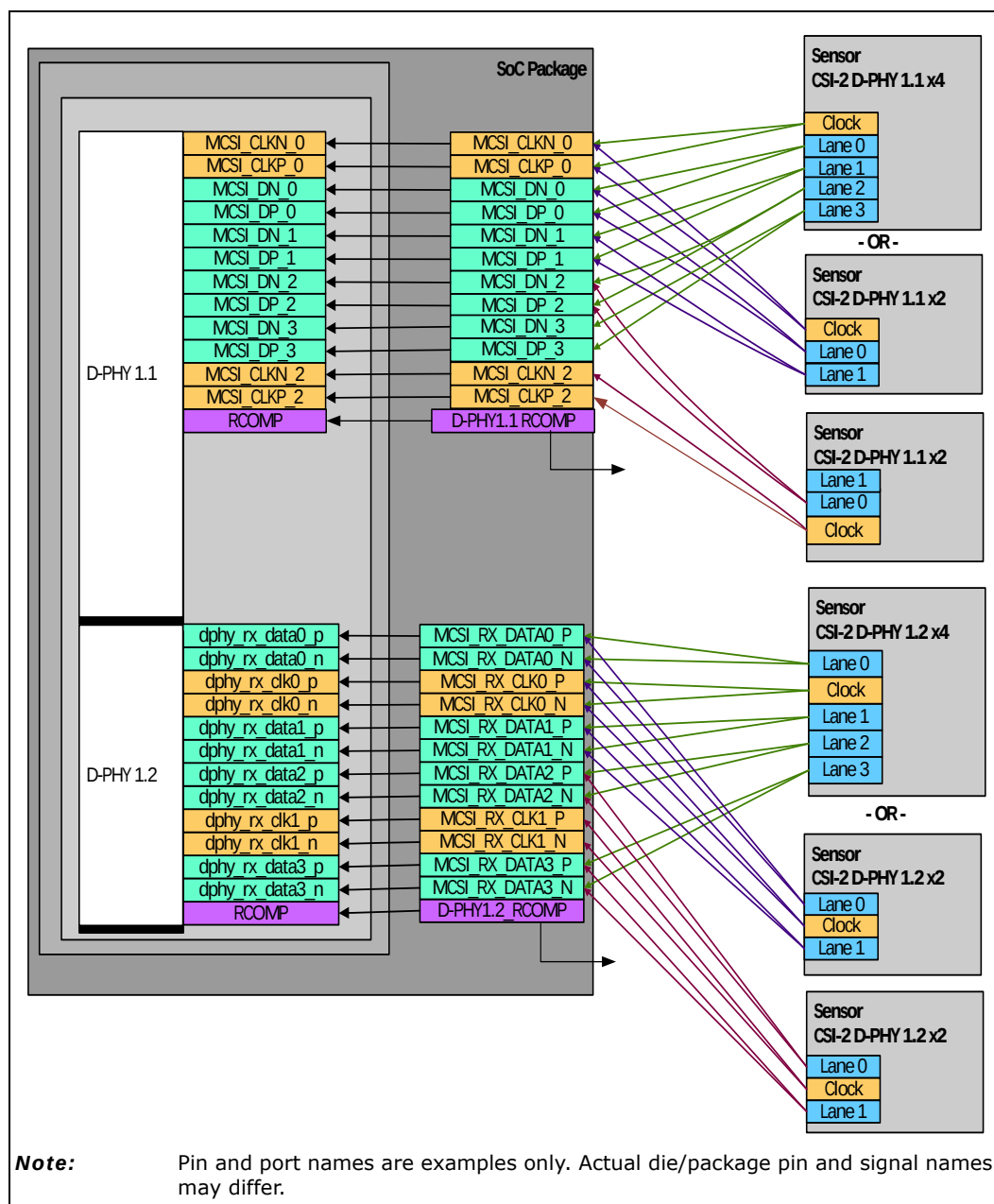
3.5.1.1 CSI2 D-PHY 1.1 / 1.2 Sensor Configurations

The SoC has four dedicated DPHY 1.1 lanes and two differential clock lanes, running at a maximum frequency of 1.5 GHz and supporting a peak MIPI*-DPHY transfer rate of 1.5 Gb/s per lane. Similarly, SoC has four dedicated DPHY 1.2 lanes and two differential clock lanes, supporting peak transfer rate of 1.5Gb/s per lane. The four clock lanes (two on D-PHY 1.1 and two on D-PHY 1.2) enable supporting of maximum of four sensors. The eight DPHY lanes can be used in any of the following configurations, to support up to four sensors.

1. Single sensor up to x4 configurations
2. Two sensors up to x4 and x4 configurations
3. Four sensors up to x2, x2, x2, and x2



Figure 3-1. CSI2 D-PHY 1.1/1.2 Sensor Configurations



3.6 Audio Controller

Table 3-11. Audio Controller Features

Category	Description
I ² S/SSP Interfaces	Two I ² S/SSP Interfaces for platform peripherals
DSPs	Two high-performance DSPs configured with: 32kB 4-way set associative L1 Instruction Cache 64kB 4-way set associative L1 Data Cache
L2	- L2 Memory controller with the local high-performance interconnect fabric - L2 Cache Controller with cacheing and prefetch capabilities
ROM Size	8kB ROM
DMA Interfaces	Two, 8-channel universal DMA interfaces for transferring data between memory buffers and peripherals and between memories
DMIC Interfaces	Two, dual-channel D igital M icrophone interfaces
HD Audio and LPE Audio	Supports HD-Audio and LPE Audio for DDI [1:0] (DisplayPort and HDMI)
CODEC	Supports one external CODEC for attaching audio peripherals
Burst Mode	Local power sequencer for burst-mode data processing in micropower modes (S0ix)
Debug Interface	DSP On-chip Debug interface with two JTAG ports

3.7 Power Management

The SoC supports different power modes providing significant power optimization.

Table 3-12. Power Management Supported Features

Category	Description		
ACPI	Support ACPI 5.0		
Core C-States	CC0, CC1 and CC6		
Core C-State OS definition	Core C-State	C0, C1, C1E, C6, C6L	C7, C7L, C8, C9, and C10
	Deepest Module C-State	MC0	MC7
	Deepest S0ix state	S0	S0i3
Processor Module States	MC0-CC0, MC0-CC6, MC7		
Graphics States	RC0, RC1, RC6		
System Sleep States	S0, S0ix, S3, S4, S5		
Power States Management	• Active-state power management — Performance control inputs received from platform firmware and software — Physical constraints observed through sensors in the package — Operating points determined to maximize power performance and energy efficiency • Idle-state power management • Flexible platform states to support phone and tablet usage models • Supports minimal device-to-device operations while most of the package is quiesced • Autonomous power gating		
Other Power Features	• Support thermal management • Integrated Sensor Hub (ISH) — Supports “always on” sensing in S0ix modes		



3.8 USB Controller

Table 3-13. USB xHCI Controller Features

USB Interface	
Category	Description
USB 3.0 Port	6 (1x USB Dual Role, 1 dedicated port, 3x multiplexed with PCIe* 2.0, 1x multiplexed with SATA 3.0) Note: All Ports are backward compatible with USB 2.0
Peak USB 3.0 Speed	5Gb/s
USB 2.0 Port	2
Direct Connect Interface (DCI)	USB Port0 and Port 1 only
Peak USB 2.0 Speed	480Mb/s
Number of Supported Endpoints	32 per port

Figure 3-2. USB3/PCIe*/SATA Port Mapping

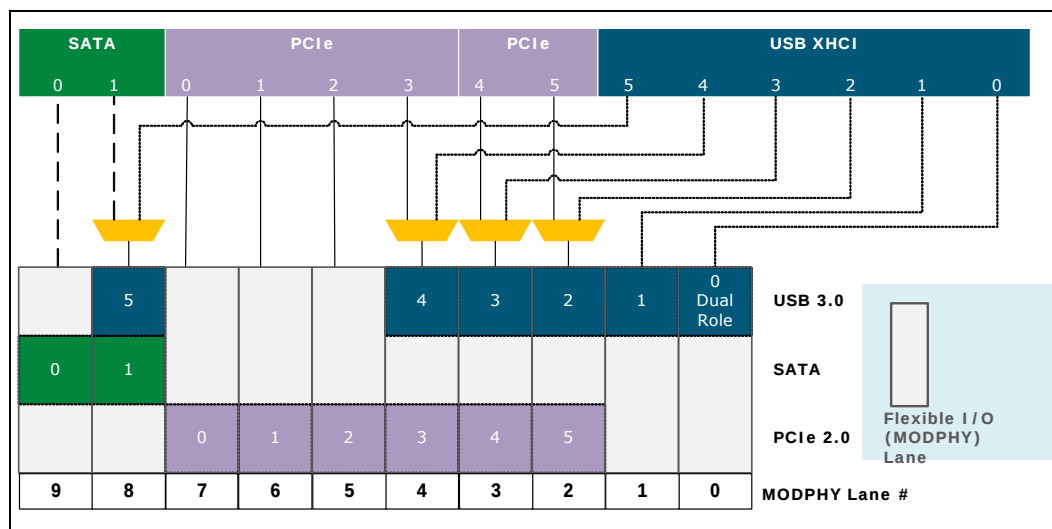
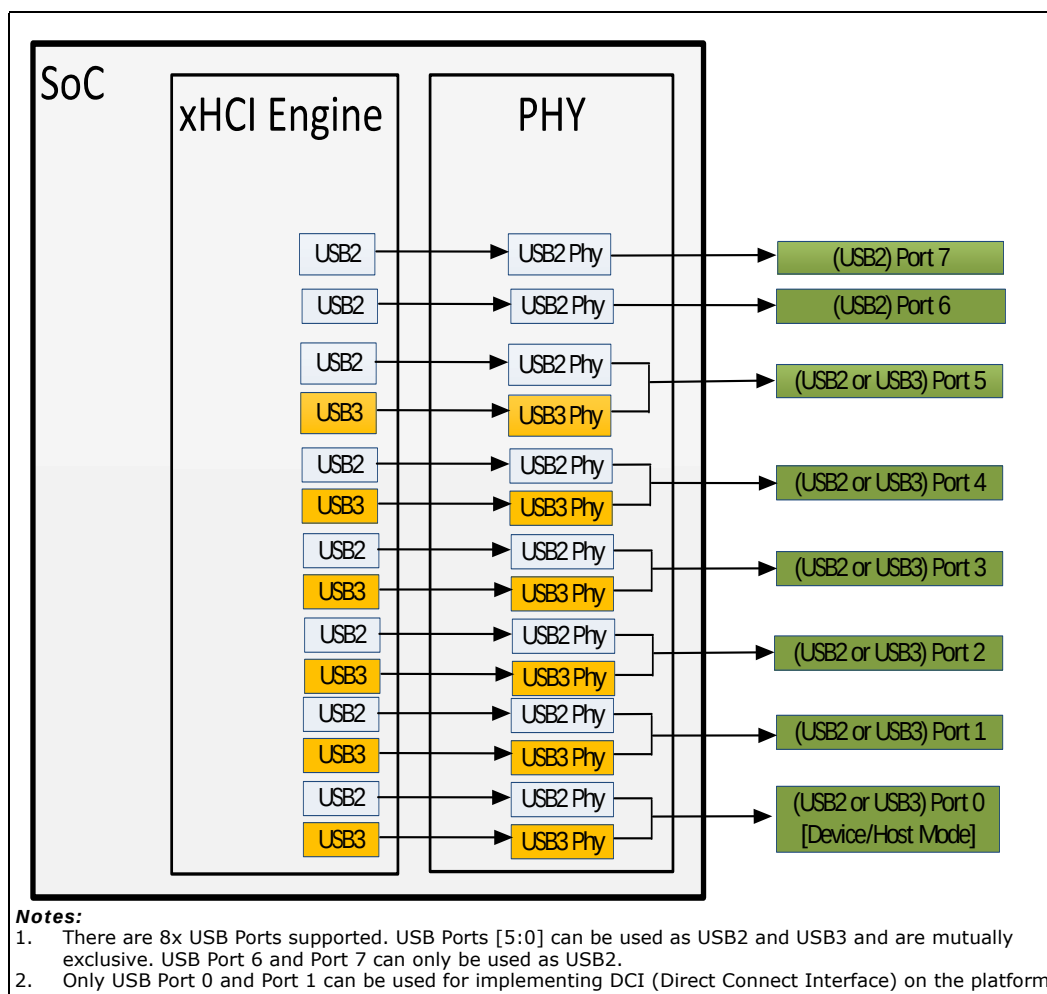


Figure 3-3. USB2 and USB3 Port Mapping


3.9 PCI Express*

SoC has integrated PCIe* interface with following features:

Note: PCIe* Lanes 3, 4, and 5 are multiplexed with USB3 Ports 4, 3, and 2, respectively. Refer to [Figure 3-2](#) for more information.

Table 3-15. PCIe* Features (Sheet 1 of 2)

Category	Description
PCIe* Interface	PCIe* Gen2 and PCIe* Gen1
PCIe* number of lanes	6 lanes (x3 dedicated and x3 multiplexed with USB 3.0)
PCIe* Maximum Supported Devices	Up to 4 root ports/external device
PCIe* Signal Transfer Rate	PCIe* Gen2: 5.0 GT/s and PCIe* Gen1: 2.5 GT/s per root port
PCIe* Clock Frequency	100 MHz (SSC/NSSC Type) Supports 4 reference Clocks (REF CLK)

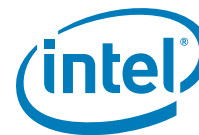


Table 3-15. PCIe* Features (Sheet 2 of 2)

Category	Description
PCIe* Supported Configuration	Flexible Configuration Supported with any combination of 4 root ports (should not exceed 6 lanes). Example of some common configurations: — (1) x4 + (1) x2 — (4) x1 — (2) x1 + (1) x2 + (1) x2 x1, x2, x4 lane widths (auto negotiated)
Supported Interrupt and Events	• Legacy (INTx) and MSI Interrupts • General Purpose Events • System Error Event
Power Management	• Link State support for L0s, L1, and L2 • L1 Sub-states support • Powered Down in ACPI S3state - L3
PCIe* Compliance	
Reference	Revision
PCI Express* Base Specification	Revision 2.0

3.9.1 PCIe* Port Mapping

Table 3-16. PCIe* Port Mapping

PCIe* Config.	Dev.	Func.	Device ID	BIOS ASL (Root Port)	Signal Names	Bifurcation
x2	20	0	0x5AD6	0/Device(RP01)	PCIE_P4_USB3_P3_TX/RX [N/P]	1 x2, 2 x1
	20	1	0x5AD7	1/Device (RP02)	PCIE_P5_USB3_P2_TX/RX [N/P]	
x4	19	0	0x5AD8	2/Device (RP03)	PCIE_P0_TX/RX [N/P]	1 x4, 2 x2, 1 x2, 2 x1, 4 x1
	19	1	0x5AD9	3/Device(RP04)	PCIE_P1_TX/RX [N/P]	
	19	2	0x5ADA	4/Device (RP05)	PCIE_P2_TX/RX [N/P]	
	19	3	0x5ADB	5/Device(RP06)	PCIE_P3_USB3_P4_TX/RX [N/P]	
Note: For proper functionality of the PCIe ports each CLKREF signal must be associated with the corresponding CLKREQ signal to enable the clocks. Ensure that the BIOS assigns the valid number for the CLKREQ.						

Table 3-17. Supported Configurations for x4 Root Port

Configuration	PCIe* x4			
	Port 0	Port 1	Port 2	Port 3
1 x4	x4	Disabled	Disabled	Disabled
2 x2	x2	Disabled	x2	Disabled
1 x2, 2 x1	x2	Disabled	x1	x1
4 x1	x1	x1	x1	x1

Table 3-18. Supported Configuration for x2 Root Port

Configuration	Port 0	Port 1
1x 2	x2	Disable
2 x1	x1	x1

3.10 Serial ATA (SATA)

The SoC has an integrated Serial ATA (SATA) host controller with independent DMA operation on up to 2 SATA ports.

Note: SATA Port 0 is dedicated for SATA, while SATA Port 1 is multiplexed with USB3, Port 5 and can be configured to be used for either interface. Refer to [Figure 3-2](#) for more information.

Table 3-19. SATA Interface

SATA Interface	
SATA Interface	SATA Gen3, Gen2, and Gen1
SATA number of ports	2 SATA Ports
SATA Signaling Transfer Rate	SATA Gen3: 6Gbps - Gen2: 3Gbps - Gen1: 1.5Gbps
SATA Data Speed	SATA Gen3: 600MB/second - Gen2: 300MB/second - Gen1: 150MB/second
SATA Clock Frequency	100 MHz (SSC/NSSC Type)
SATA Compliance	
SATA Specification Compliance	Revision 3.2 (Also supports optional sections of the SATA Revision 2.6/2.0 Specification.)
AHCI Specification Compliance	Revision 1.3.1
SATA II: Extensions to SATA 1.0	Revision 1.0 (AHCI support is required for some elements)

Table 3-20. SATA Supported Features (Sheet 1 of 2)

Supported Features	
Native Command Queuing (NCQ)	Allows the device to reorder commands for more efficient data transfers
Auto Activate for DMA	Collapses a DMA Setup then DMA Activate sequence into a DMA Setup only
Asynchronous Signal Recovery	Provides a recovery from a loss of signal or establishing communication after hot-plug
ATAPI Asynchronous Notification	A mechanism for a device to send a notification to the host that the device requires attention
Host and Link Initiated Power Management	Capability for the host controller or device to request Partial and Slumber interface power states
Staggered Spin-Up	Enables the host to spin up hard drives sequentially to prevent power load problems on boot
DEVSLP	Device Sleep (DEVSLP) is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state

**Table 3-20. SATA Supported Features (Sheet 2 of 2)**

Supported Features	
AHCI DMA PRD format	Allows software to communicate between system memory and SATA devices
AHCI Mode Support	The application layer operates in AHCI Host Bus Adaptor (HBA) mode
Dynamic clock gating and dynamic trunk gating	Enables automatic gating off of peripherals that are not being used until CPU or a DMA engine needs to use.

Table 3-21. SATA Non-Supported Features

Non-Supported Features
Port Multiplier
FIS Based Switching
Command Based Switching
IDE Mode
Cold Presence Detect
Function Level Reset (FLR)
Command Completion Coalescing
Enclosure Management

3.11 Storage

The following interfaces are part of the Storage subsystem:

Table 3-22. Storage Interface Usage

Interface	Type	Use
eMMC*	Storage	Internal storage device
SD-Card	Storage	Removable storage device

Table 3-23. SD Card Features

Category	Feature Supported
Specification	SD Memory Card Specification Version 3.01
SD Signalling	SD 3.01 Signaling (UHS-1@ SDR 104/50/25/12 and DDR50)
SD Clock Frequency	25, 50, 100, and 200 MHz
Data Rate	Up to 100MB/s using 4 parallel data lines (SDR104 mode)
Transfer Modes	Support transfer the data in 1-bit and 4-bit SD modes
Mode of Operation	Support both ADMA2/DMA and Non-DMA Modes
Cyclic Redundancy Check	Support CRC7 for command and CRC16 for data integrity
Others	- Supports both Wi-Fi and Modem devices - Support Card Detection (Insertion/Removal) for SD Card only - Support Async Interrupt Cards

Table 3-24. eMMC* Features

Category	Feature Supported
eMMC* Specification	embedded Multi-Media Card* Product Standard v5.0, JESD84-B50
eMMC* Signalling	- eMMC* v5.0: HS400 DDR Mode - eMMC* v4.5: HS200 SDR Mode
Transfer Modes	Support transfer the data in 1-bit, 4-bit, and 8-bit modes
Mode of Operation	Support both ADMA2/DMA and Non-DMA Modes
Boot Modes	Support both eMMC* Secure and Non-Secure Boot
Cyclic Redundancy Check	Support CRC7 for command and CRC16 for data integrity
Others	Support Interrupt Coalescing

Table 3-25. SD Card Working Modes

SD Card Mode	Data Rate	Maximum Clock Frequency	Maximum Data Throughput
Default Speed/SDR12 ¹	Single	25 MHz	12.5MB/s
High Speed/SDR25 ²	Single	50 MHz	25MB/s
SDR50	Single	100 MHz	50MB/s
DDR50	Dual	50 MHz	50MB/s
SDR104	Single	200 MHz	100MB/s
Notes: 1. Default-Speed means 3.3V signaling, SDR12 means 1.8V signaling. 2. High-Speed means 3.3V signaling, SDR25 means 1.8V signaling.			

Table 3-26. eMMC* Working Modes

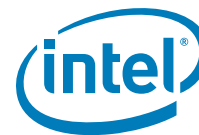
eMMC* Mode	Data Rate	Maximum Clock Frequency	Maximum Data Throughput
Compatibility	Single	25 MHz	25MB/s
High Speed SDR	Single	50 MHz	50MB/s
High Speed DDR	Dual	50 MHz	100MB/s
HS200	Single	200 MHz	200MB/s
HS400	Dual	200 MHz	400MB/s

3.12 Serial I/O (SIO) (LPSS)

SIO (LPSS) is a collection of slow I/Os used to interface various external devices in the platform.

Table 3-28. SoC Serial I/O Supported Interfaces

Interface	Number of Ports	Maximum Speed
[SIO] I ² C	8	3.1Mb/s
[SIO] HSUART	3	115.200kb/s (standard 16550) 3.6864Mb/s (high-speed 16750)
[SIO] SPI	1	25 Mb/s

Table 3-29. SIO—I²C Features

Category	Feature Supported
SIO - I ² C Interface	Two-wire, I ² C serial interface comprising a Serial Data line (SDA) and a Serial Clock (SCL)
Loading Range	Limited to 400 pF maximum
Addressing	7b or 10b addressing Note: Ignores CBUS addresses (an older ancestor of I ² C that used to share the I ² C bus)
Operation Modes	- Master I²C operation only - Interrupt or polled-mode operation - Handles Bit and Byte waiting at all bus speeds Notes: - I²C Multi Masters are not supported - I²C Slave Mode is not supported - I²C Generic Call is not supported
Maximum bit rate	High-speed mode supporting a maximum bit rate of 3.1Mb/s Note: Simultaneous configuration of FM or FM+ is not supported in Fast-mode Plus
Data Transfer	64B transmit (TX) and receive (RX) Host Controller FIFOs 64B iDMA FIFO per channel with up to 32B Burst capability Notes: - IDMA handshaking interface compatible with the DW_OCP_IDMAc handshaking interface - DMA mode is not supported when Slice is assigned to TXE (Trusted Execution Engine)
Driver/SW Support	- Component parameters for configurable software driver support - SW Controlled serial data line (SDA) and a serial clock (SCL) - Programmable SDA hold time (tHD; DAT)

Table 3-30. SIO—HSUART Features (Sheet 1 of 2)

Category	Feature Supported
SIO—HSUART Interface	Four-Wire HSUART signal Interface using RTS/CTS Control only
Addressing	Programmable character properties, such as number of data bits per character (5b to 8b), optional parity bit (even or odd parity) and number of stop bits (1b, 1.5b, or 2b)
Operation Modes	- Functionality based on the 16550 and 16750 industry standards - Transmitter Holding Register Empty (THRE) interrupt mode - Prioritized interrupt identification Note: HSUART Slave Mode is not supported
Max bit rate	- Up to 3.6864 MT/s Auto Flow Control mode as specified in the 16750 standard - Programmable serial data baud rate - Programmable baud supported [baud rate = (serial clock frequency)/(16× divisor)]
Data Transfer	64B transmit (TX) and receive (RX) Host Controller FIFOs 64B iDMA FIFO per channel with up to 32B Burst capability - DMA signaling with two programmable modes - Programmable FIFO enable/disable - Line break generation and detection Notes: - DMA mode is not supported when Slice is assigned to TXE - UART 16550 8b Legacy mode is not required when Slice is assigned to TXE - There is no external read enable signal for RAM wake-up when using external RAMs

Table 3-30. SIO—HSUART Features (Sheet 2 of 2)

Driver/SW Support	- Software-controlled CTS overwrite (for 2-wire interface there is no flow control operation) - Loopback mode enables greater testing of Modem Control and Auto Flow Control features Notes: - Modem and status lines are independently controlled - Serial Infrared (SIR) per the Infrared Data Association (IrDA) 1.0 is not supported
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Table 3-31. SIO—SPI Features

Category	Feature Supported
SIO—SPI Interface	Receive Without Transmit (RWOT) half duplex mode
Addressing	Supports data sizes from 4-bit to 32-bit in length and FIFO depths of 64 entries
Operation Modes	- Master SPI operation only - Operates as Motorola SPI Notes: - SPI Slave Mode is not supported - Network modes from one to eight time slots are not supported with independent transmit and receive (TX and RX)
Maximum bit rate	Support Programmable baud rate
Data Transfer	256B Transmit (TX) and Receive (RX) Host Controller FIFOs 128B iDMA FIFO per channel with up to 64B Burst capability Notes: - Single DMA transactions are supported - DMA mode is not supported when Slice is assigned to TXE
Driver/SW Support	- Software control for chip-select override - Programmable Polarity for clock and chip selects signals - Up to two chip selects per host controller

3.13 Fast SPI

- The SPI controller supports up to two SPI Flash devices using two separate chips select pins.
- Each SPI Flash device can be up to 16 MB.
- Communication on the SPI bus is done with a Master – Slave protocol. The Slave is connected to the SoC and is implemented as a tri-state bus
- The SPI controller has one operational mode Descriptor. Volume 4 confirms that only Descriptor Mode is supported.
- Supports TPM

3.14 Power Management Controller (PMC)

- The Power Management Controller subsystem is one of the first subsystem to be functional after reset. It is responsible for the following functionality:
- Conducting system boot flow
- Conducting Warm/Cold/Global resets
- Conducting Sleep state entry (S3/S4/S5—cold off)



- Collecting all wake events and Conducting system wake from sleep states (wake architecture)
- Maintain Timers
- Conducting S0ix entry/exit and wake from S0ix state
- Managing Power Rails
- Handling SMI (System Management Interrupt)
- Handling SCI events (System Control Interrupt)
- PMC uses SVID or I²C interfaces for communication with PMIC (Power Management IC) or discrete IMVP8 voltage regulators

3.15 Intel™ Legacy Block

Intel™ Legacy Block (iLB) supports the following features:

Table 3-32. iLB Features

Interrupt and Timer SubSystem
• 8259 Controllers — Registers mapped to fixed I/O locations — Uses Messages to CPU to indicate interrupt — 15 total interrupts • I/O APIC — Registers mapped to fixed I/O locations — Uses Messages to CPU to indicate interrupt • 8254 timers — Registers mapped to fixed I/O locations — Has 3 internal timers — Timer 0 - used for OS timer tick — Timer 1 - Unused — Timer 2 - used for “beep” speaker • HPET - High Performance Event Timers — Includes one periodic timer, seven one-shots (total eight comparators) — Improved resolution, reduced overhead — Results in fewer interrupts to CPU

Table 3-32. iLB Features

GPIO
- Total of 243 GPIO capable pins. 1.05V, 1.8V, 3.3V signaling available on GPIO signals Note: Check the GPIO Multiplexing Table 2-34 for more details. - Each GPIO pad can be configured as an input or output signal - Most pads are multiplexed between GPIO mode and native mode function(s) - Configurable GPIO pad ownership by TXE to TXE itself, ISH or host. - SCI/GPE and IOxAPIC interrupt capable on many GPIOs - GPI GPE Status and GPE Enable registers in GPIO Community - Direct IOxAPIC interrupts available on select GPIO 32 pins from two communities can be selected as direct interrupt wake events. - Eight pins from two communities can be selected as TXE wake events. - SMI capable on selected GPIOs (NMI not implemented on SoC). - GPIO registers accessible thru IOSF-SB.
Real Time Clock (RTC)
- SoC has an integrated Real-Time Clock (RTC), a Motorola MC146818B-compatible RTC with 242 bytes of battery-backed RAM. - The RTC operates on a 32.768 KHz crystal and a 3.3V battery. - The RTC performs two key functions—keeping track of the time of day and storing system data, even when the system is powered down. - The RTC supports two lockable memory ranges. By setting bits in the configuration space two, 8-byte ranges can be locked to read and write accesses. This prevents unauthorized reading of passwords or other system security information.

3.16 Integrated Sensor Hub

Integrated Sensor Hub (ISH) serves as the connection point for many of the sensors on a platform. The ISH is designed with the goal of “Always On, Always Sensing” and it provides the following functions to support this goal:

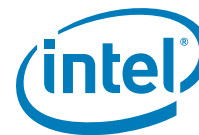
Table 3-33. Integrated Sensor Hub Supported Functions and Components

ISH Supported Functions
- Acquisition/sampling of sensor data. - Low power Sensor Fusion. - The ability to combine data from individual sensors to create a more complex virtual sensor that can be directly used by the firmware/OS. - Low power operation through clock and power gating of the ISH blocks together with the ability to manage the power state of the external sensors. - The ability to operate independently when the host platform is in a low power state (S0ix only).
ISH Key Components
- A combined cache for instructions and data. —ROM space intended for the boot loader. —SRAM space for code and data. - Interfaces to sensor peripherals (I²C and GPIO). - An interface to main memory. - Out of Band signals for clock and wake-up control. - Part of the PCI tree on the host.

3.17 SMBus

SoC provides a System Management Bus (SMBus) 2.0 host controller.

The SoC is capable of communicating with I²C compatible devices.



3.18 Security Architecture

The Security involves:

- Trusted Execution Engine 3.0 (TXE3.0)
- Basic SoC security Architecture
 - Layered SoC Security
 - Security principles like CIA triad (confidentiality, integrity, and availability)
 - SoC Trusted Computing Base (TCB)
 - Adversary Model and Adversary Capabilities
- Access Control Architecture
- SoC IP security
- SoC Assets
- Debug Security

Table 3-34. SoC TXE 3.0 Interaction

Flow	SoC Logic Blocks
Secure Boot and DnX (Download and Execute)	SoC Power Management Controller (PMC), PMIC (by means of PMC), USB (USB2 and USB3), SPI, Memory Controller, I/O Subsystem, Goldmont Core, GPIO, LPSS, System Agent, C-unit
Firmware Authentication	cAVS, ISH, Imaging, PMC
Content Protection (PAVP, HDCP 2.2, WiDi, Play Ready3 DRM)	Graphics and Display Controller
Fingerprint Reader	LPSS
Provisioning flows	SPI
Secure timer	PMC (PMIC), Protected RTC
NFC Support (reader and secure element)	LPSS

Note: It is recommended that TXE should **NOT** own Function 0 unless TXE needs to do all functions of a device. When TXE owns Function 0 of a multi-function device, the host software that enumerates PCI will not be able to see Function 0 and hence will **not** look for other functions in this case. Due to this the other functions will not be usable by the host. If TXE does not own Function 0 then the host software enumerating PCI will continue to look for additional Devices 1-7 and would enumerate the functions not owned by TXE. This is the normal operation of the SoC and there is no hardware or software requirement for the above to occur and this restriction can't be changed.

This also applies to instances where there are multiple devices (with respect to Bus: Device: Function) for one type of usage/interface that results in 2x (two) "Function 0" controllers, one under each Device number. For eg. I²C, which has 8x controllers, and uses 2x Device numbers, each with 4x Functions. This results in 2x "Function 0" controllers - 1x under each device number. In this case, it is recommended that TXE does not own "I²C0" and "I²C4" as they both are "Function 0" under different "Devices"

3.19 Thermal Management

There are four main categories of Thermal Management:

- SoC thermal area
- Memory thermal area
- Thermal Interrupt
- Running Average Power Limit algorithm

The SoC thermal area includes SoC thermal sensing, thermal control algorithms, reporting SoC temperature and supporting thermal interrupts.

The Memory thermal area includes memory thermal sensors, control algorithms, reporting memory thermal status, and generating thermal interrupts. The interaction with the DRAM varies depending on the memory type: LPDDR3/4 or DDR3L. For LPDDR3/4, the MR4 register is read in order to monitor DRAM temperature and take appropriate action that could include changes to memory timing, refresh rate and bandwidth throttling. For DDR3L, only Byte 31, Bit 2 of the SPD ROM is read to detect support for ASR (Auto Self Refresh).

The Running Average Power Limit (RAPL) algorithm is a package-level feature for Tskin control which provides energy status reporting, power-limit configuration, and control algorithms.

3.19.1 SoC Features

There are four main SoC features:

- PROCHOT Support
- DPTF – Thermal Interrupt support
- Thermal Control Algorithm
- Cross Throttling

3.19.2 Thermal Sensors

SoC Sensors are based on DTS (Digital Thermal Sensor) to provide more accurate measure of system thermals.

The SoC has 5 DTSS. DTS outputs are adjusted for silicon variations. For a given temperature the output from DTS is always the same irrespective of silicon.

Table 3-35. Temperature Reading Based on DTS (Sheet 1 of 2)

DTS Counter Value [8:0]	Temperature Reading (If $T_{J-MAX} = 90^{\circ}\text{C}$)
127	90°C
137	80°C
147	70°C
157	60°C
167	50°C
177	40°C

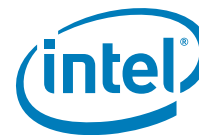


Table 3-35. Temperature Reading Based on DTS (Sheet 2 of 2)

DTS Counter Value [8:0]	Temperature Reading (If $T_{J-MAX} = 90^{\circ}\text{C}$)
187	30°C
197	20°C
207	10°C
217	0°C
227	-10°C
237	-20°C
247	-30°C
255	-38°C

- DTS encoding of 127 always represents T_{jmax} at 90°C, the encoding 137 from DTS indicates 80°C and so forth
- The DTS value 255 represents the minimum temperature and thus -38°C is the lowest temperature will be reported by the SoC.

3.20 Clocking

SoC contain variable frequency, multiple clock domains and multiple power plane clocking schemes with determinism and synchronization requirements in some areas. The architecture also supports various PLL clocking requirements with bypass options to save power.

Table 3-36. Summary of Clock Signals

Interface	Clock Signal	Clock Frequency
Memory - DDR3L	MEM_CH[0:1]_CLKP/N[0:1]	Upto 933 MHz
Memory - LPDDR3	MEM_CH[0:1]_CLKP/N[0:1]A/B	Upto 933MHz
Memory - LPDDR4	MEM_CH[0:1]_CLKP/N[0:1]A/B	Upto 1200 MHz
PCIe*	PCIe_CLKOUT[0:3]P/N	100 MHz
Storage - eMMC* 4.51 and 5.0	eMMC_CLK	2, 50, 200 MHz
Storage - SD Card	SDCARD_CLK	25, 50, 100, 200 MHz
Display - HDMI*	DDI[0,1]_DDC_SCL	100 kHz
Display - MIPI*-DSI	MDSI_[A,C]_CLKP/N	19.2 MHz ref (CLK Frequency 300-1600 MHz)
Camera - MIPI*-CSI	On DPHY1.1 MCSI_CLKP/N_[0,2]	1.5Gb/s
	On DPHY1.2 MCSI_RX_CLK[0,1]_P/N	1.5Gb/s
Audio - HD Audio	AVS_HDA_BCLK (multiplexed)	6, 12, 24 MHz
Audio Codec/Analog Microphone- I ² S	AVS_I ² S2_BCLK AVS_I ² S2_MCLK AVS_I ² S6_BCLK (multiplexed)	BCLK = 12.28 MHz MCLK = 19.2 MHz
Audio - Digital Microphone	AVS_DMIC_CLK_[A/B]1 AVS_DMIC_CLK_AB2	1.2-4.8 MHz

Table 3-36. Summary of Clock Signals

Interface	Clock Signal	Clock Frequency
SIO (LPSS) I ² C	LPSS_I ² C[0:7]_SCL	100 KHz, 400 KHz, 1 MHz, 3.1 MHz
PMIC	PMIC_I ² C_SCL	100 KHz, 400 KHz, 1 MHz, 3.1 MHz
SVID	SVID0_CLK	19.2 MHz
LPC	LPC_CLKOUT[0,1]	25 MHz
PCIe	PCIe_CLKOUT[0:3]P/N	100 MHz
SMBus	SMB_CLK	Maximum 100 KHz
SIO (LPSS) SPI	SIO_SPI_0_CLK	25 MHz
FAST SPI - SPI NOR and TPM	FST_SPI_CLK	14, 25, 40, 50 MHz
Platform - OSC_CLK_OUT	OSC_CLK_OUT_[0:2]	6.7, 8, 9.6, 13.6, 14.4, 19.2, 24, 26 MHz
	OSC_CLK_OUT_[3]	19.2 MHz
Platform - PMU_SUSCLK, SUSCLK	SUS_CLK[3:1]	32.768 KHz
XTAL Source - RTC Clock	RTC_X[1,2]	32.768 KHz
XTAL Source - SoC Clock - as default	OSCOUT OSCIN	19.2 MHz
MIPI	MIPI_I2C_SCL	400 KHz
ISH	ISH_I2C[2:0]_SCL	1.7 MHz
DDI	DDI[1:0]_TXP/N[3]	100 MHz
JTAG	JTAG_TCK	340 MHz

Note: Refer to Figure 3-4 for SSC/NSSC support clocks.

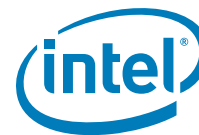
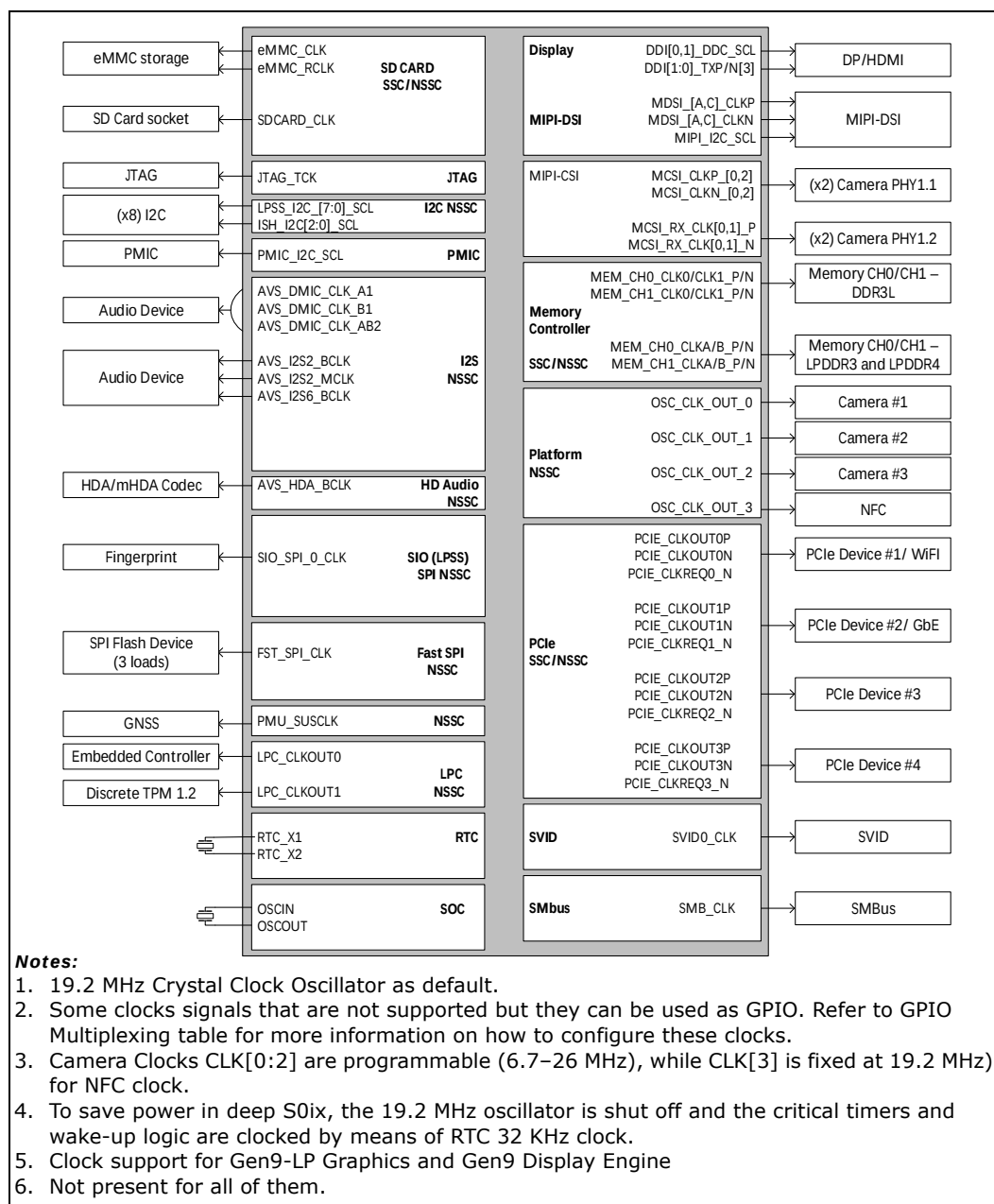


Figure 3-4. SoC Clock Mapping



4 Reset and Power Sequences

This chapter provides information about SoC reset and power sequencing.

Notes:

1. All timings shown in this chapter apply to DVR and/or PMIC design. Timing should be measured from end of the ramp to beginning of the subsequent ramp rather than the mid ramp (unless other wise specified).
2. In this section, the term DVR is synonymous with Discrete Voltage Regulator.
3. "A" rail: Always on rail. Voltage rails that do not lose power at any platform S-state (S0ix/S3/S4/S5).
4. "S" rail: Core voltage rails. These rails lose power in S3/S4/S5/Cold Reset. SoC S rails lose power during S0Ix state but not platform S rails.
5. Only one significant rail name is shown in the timing diagram for each voltage group. Refer to [Chapter 2, "Physical Interfaces"](#) section for other associated voltage rails in the same group.

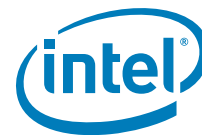
4.1 Reset Flows

Three main types of resets are supported by SoC; Cold Boot from Mechanical OFF, Cold Reset, and Warm Reset. Cold Boot G3 is defined as when first time battery install or system bring-up. Cold Boot G2 is executed any time power is reapplied while the RTC well is valid. Cold Reset is normally initiated by software starting in S0 transitions through the common reset preparation flow then through the reset stages. Warm Reset is either initiated by an internal restart (if DVR present).

4.1.1 System Sleeping States Control (S-States)

The SoC supports the S0, S0Ix S3, S4, and S5 sleep states. S4 and S5 states are identical from a hardware and power perspective. The differentiation is software determined (S4 = Suspend to Disk).

The SoC platform architecture assumes the usage of an external power management controller (for example, CPLD or PMIC) or a discrete power delivery sub-system (DVR). Some flows in this section refer to the power management controller for support of the S-states transitions.



4.2 SoC Power-Up / Down Sequences

4.2.1 RTC Power Well Transition (G5 to G3 States Transition)

When VCCRTC_3P3V (Real Time Clock power) is applied by means of RTC battery, the following occurs (refer [Figure 4-1](#) for timing):

1. VCCRTC_3P3V ramps. RTC_RST_N and RTC_TEST_N should be low.
2. The system starts the real time clock oscillator.
3. A minimum of t0 units after VCCRTC_3P3V ramps, the external RTC RC circuit de-asserts RTC_RST_N and RTC_TEST_N. The system is now in the G3 state. RTC oscillator is unlikely to be stable at this point.

4.2.2 Cold Boot [G3 Mechanical Off]

Cold Boot is executed the first time power is applied to SoC from a Mechanical Off. The Cold Boot is executed when power is completely lost, for example battery is dead or removed and no coin cell exists for the RTC. System starts completely fresh and without any previously saved state. During this state transition, the SoC rails are sequenced in an order critical to both SoC and memory operation.

Notes:

1. Platform will ignore PMU_SLP_Sx_N and THERMTRIP_N signals when RSM_RST_N is asserted.
2. VNN_SVID rail is required to sequence along with other A rails before RSM_RST_N.
3. VCC_3P3V_A voltage ramp without VCC_V1P8V_A ramps should not exceed 500 ms.
4. VCC_VCGI rail ramps at first SETVID, after the assertion of SOC_PWROK. Vboot is defined as 0V.

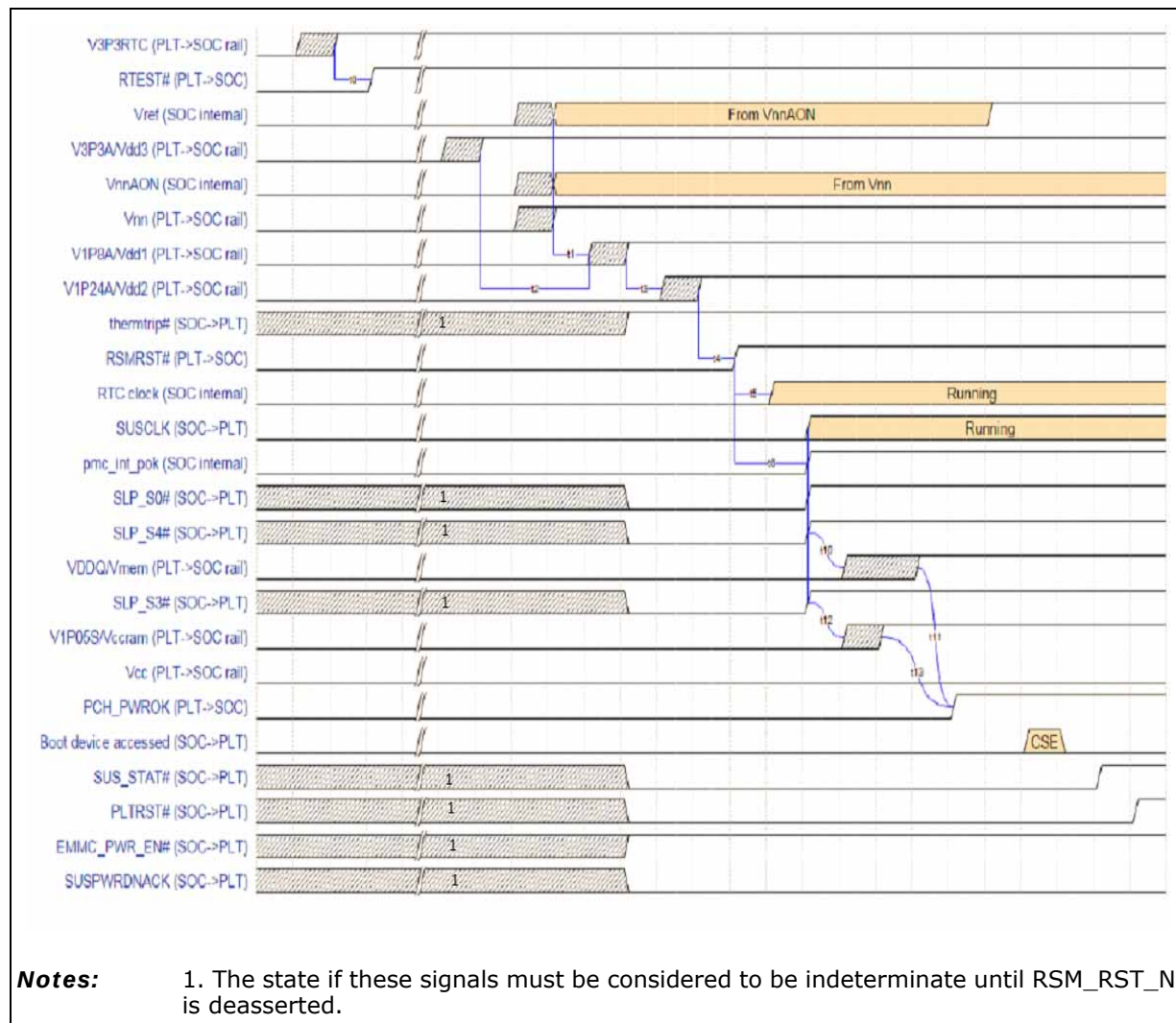
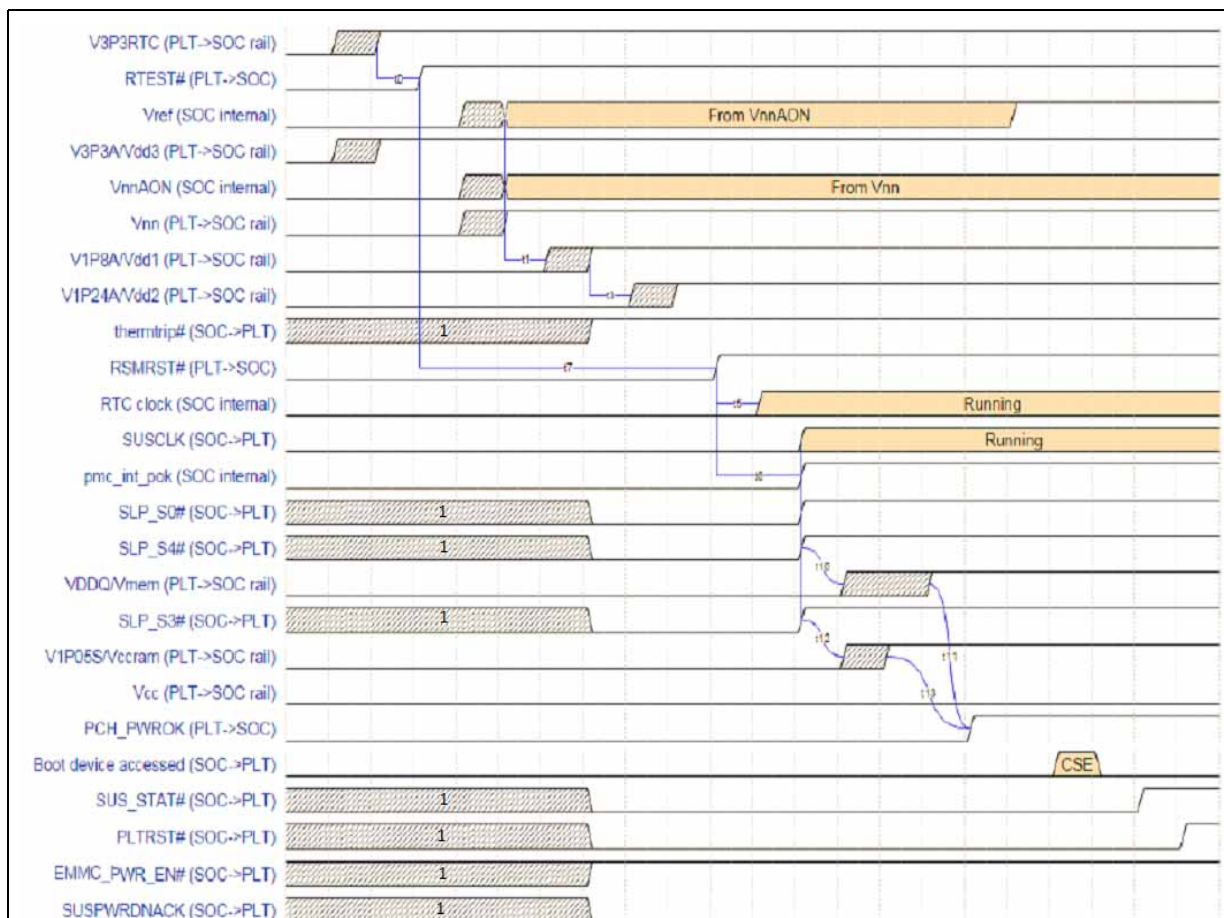
Figure 4-1. SoC G3 Cold Boot Power-Up




Figure 4-2. SoC G3 Cold Boot Power-Up No Coin Cell

**Notes:**

1. The state of these signals must be considered to be indeterminate until RSM_RST_N is deasserted

4.2.3 Cold Boot [G2]

Cold Boot G2 is executed any time power is reapplied while the RTC well is valid. Flow is the same as above G3 sequence, except that VCCRTC_3P3V would start at around 3V from the battery (note there is still a transition to V3P3A) rather than zero volts and the RTC_TEST_N is never asserted in the flow (meaning RTC was not reset).

Notes:

1. Platform shall ignore PMU_SLP_Sx_N and THERMTRIP_N signals when RSM_RST_N is asserted.
2. VNN_SVID rail is required to sequence along with other A rails before RSM_RST_N.
3. VCC_3P3V_A voltage ramp without VCC_V1P8V_A ramps should not exceed 500 ms.
4. VCC_VCGI rail ramps at first SETVID, after the assertion of SOC_PWROK. Vboot is defined as 0V.

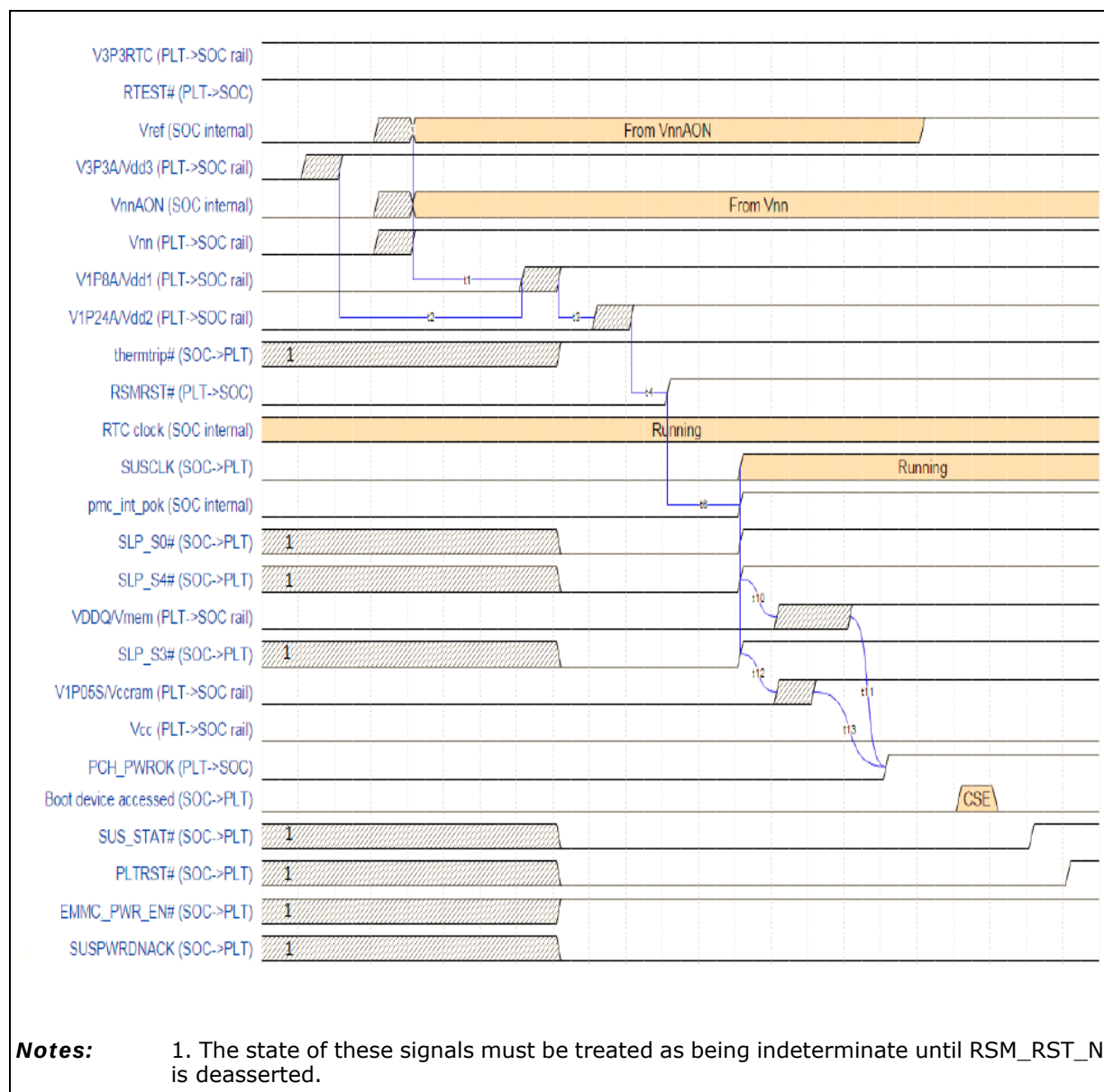
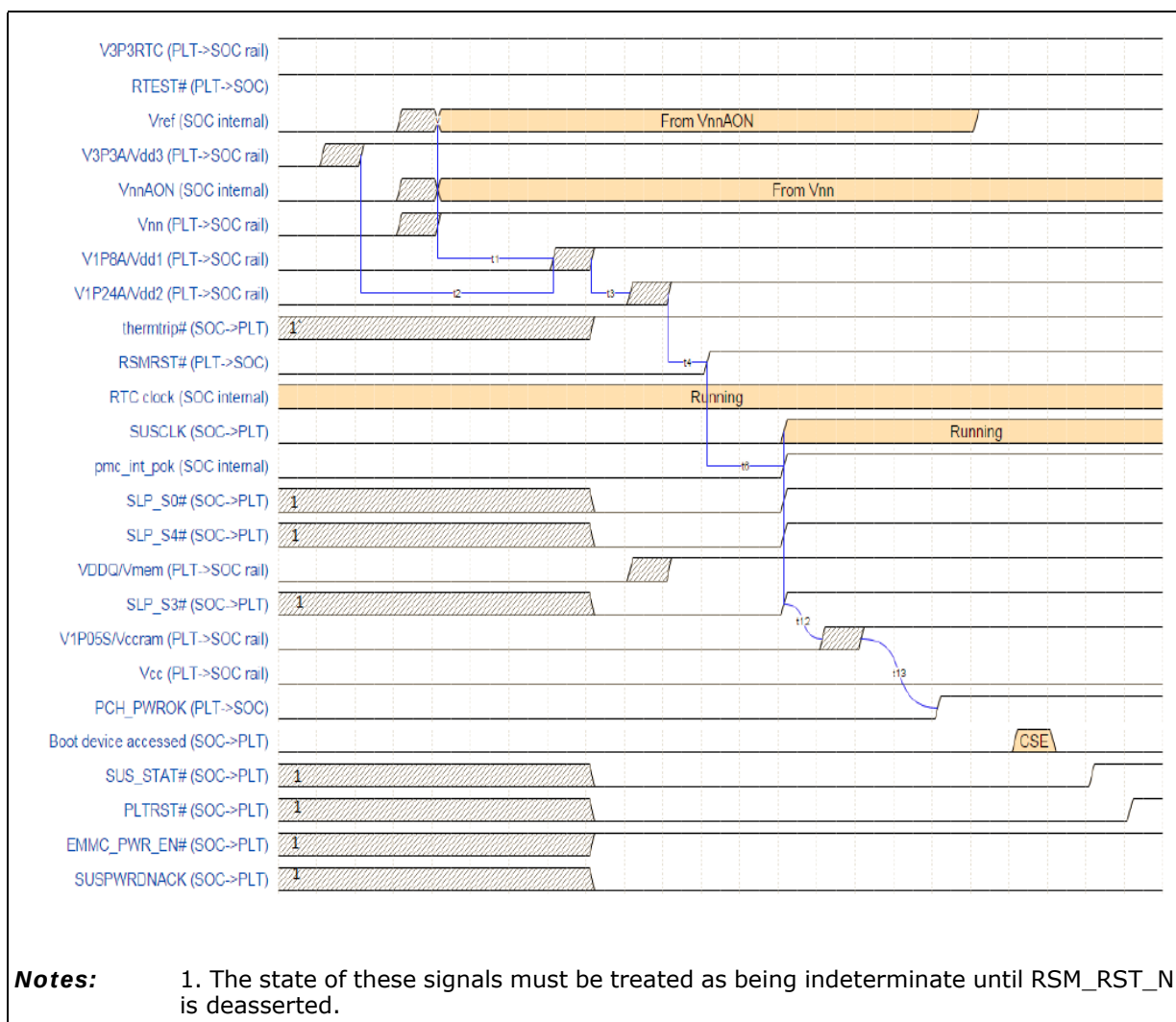
Figure 4-3. SoC G2 Cold Boot Power-Up



Figure 4-4. SoC G2 Cold Boot Power-Up VDDQ V1P24 Rail Merge


4.2.4 Cold Off [S4 / S5 Without Wakes]

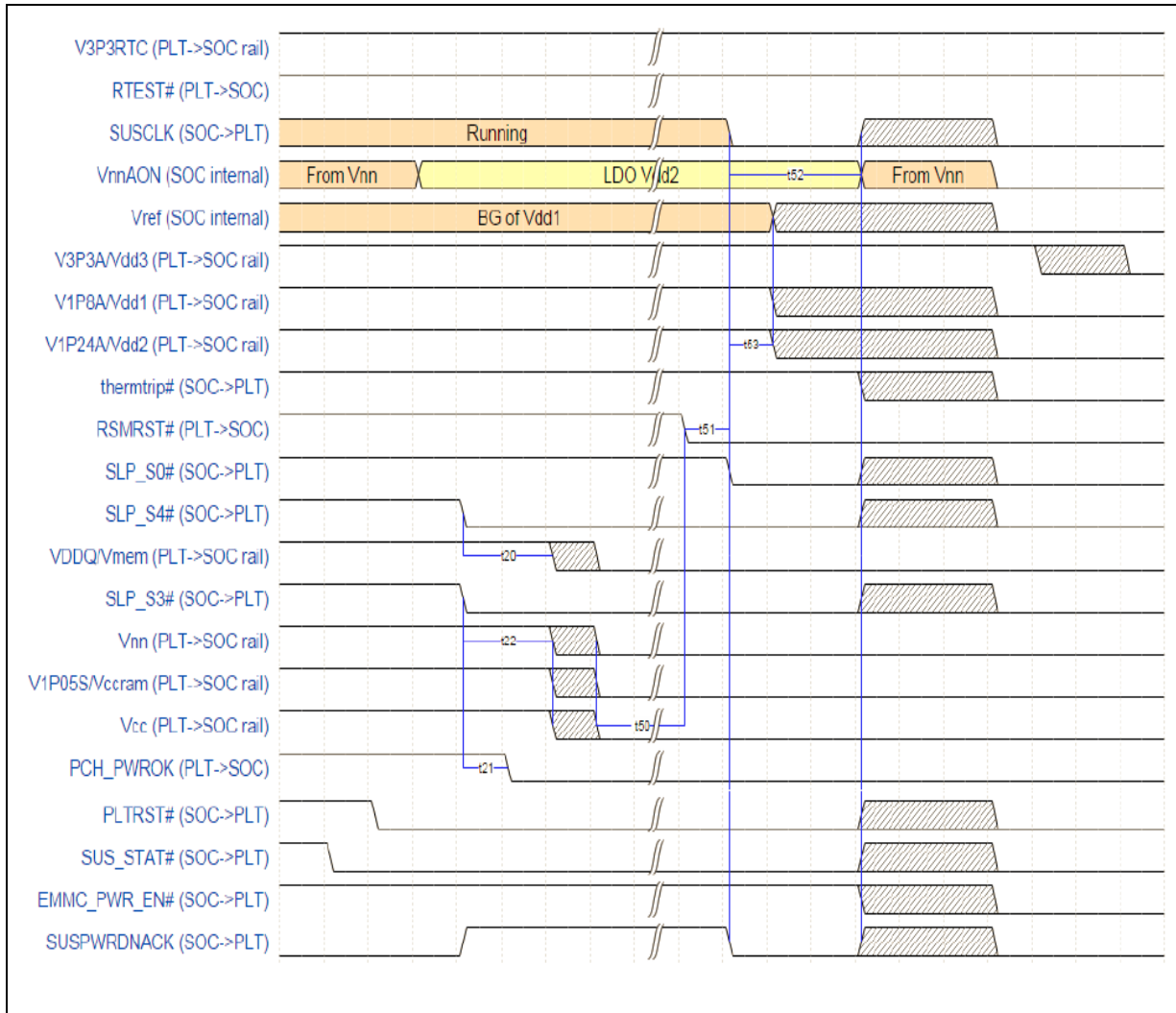
SUSPWRDNACK is asserted on S3/S4/S5. This tells the platform that it can drop power if it does not want to honor the wake requests software has set up. If this is done then the resume is a cold boot as far as the SoC is concerned.

SOC_PWROK drops will result in Thermtrip_N

- If SOC_PWROK drops outside of when SOC is asserting SLP_S3_N or SLP_S4_N SOC treats this as an unrecoverable condition and asserts Thermtrip_N to take the system into G2.
- SoC can drop from 0 to 7us after SLP_S0_N asserts without triggering a Thermtrip_N

Note: In case of forced shut down, RSM_RST_N has to be asserted first before VNN_SVID being de-asserted.

Figure 4-5. SoC S4/S5 Cold Off



4.2.5 G3->S5

When SoC does a cold boot and FW finds that there was no valid wake condition (SX_WAKE) and GEN_PMCON1.AG3E is set. FW will kick off a G3->S5 flow.

Note: When exiting G3, SoC will at least briefly go to S0 in order to complete its reset sequence. If SoC needs to go to S5 at this point, it will do so before taking the platform out of reset or running any BIOS code.

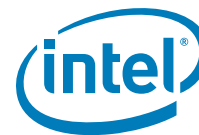
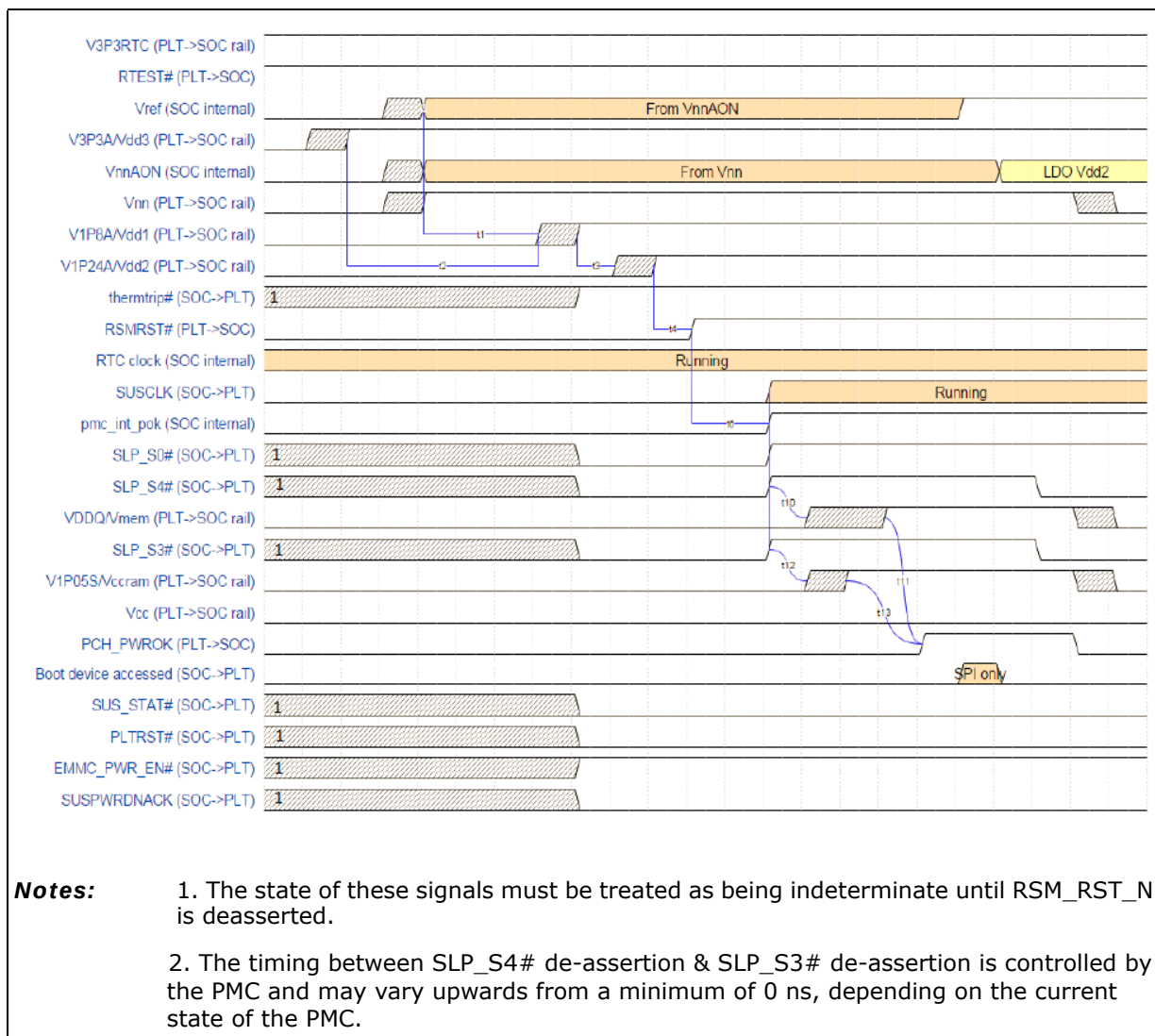


Figure 4-6. G3 -> S5 Sequencing



4.3 Reset Sequences

4.3.1 Cold Reset

Cold Reset, the basic reset, is the expected form of request coming from production software to do the most complete reset possible.

Notes:

1. Since VCC_VCGI is lower to a minimum level in the reset flow, it is very likely that VCC_VCGI will drain off well before VNN_SVID/VCCRAM_V1P05.
2. VCC_VCGI rail ramps at first SETVID, after the assertion of SOC_PWROK. Vboot is defined as 0V.

V3P3RTC (PLT->SOC rail)

RTEST# (PLT->SOC)

SUSCLK (SOC->PLT) Running

Vref (SOC internal) BG of Vdd1

V3P3A/Vdd3 (PLT->SOC rail)

VnnAON (SOC internal) From Vnn LDO Vdd2 From Vnn

V1P8A/Vdd1 (PLT->SOC rail)

V1P24A/Vdd2 (PLT->SOC rail)

thermtrip# (SOC->PLT)

RSMRST# (PLT->SOC)

SLP_S0# (SOC->PLT)

SLP_S4# (SOC->PLT)

VDDQ/Vmem (PLT->SOC rail)

SLP_S3# (SOC->PLT)

Vnn (PLT->SOC rail)

V1P05S/Vccram (PLT->SOC rail)

Vcc (PLT->SOC rail)

PCH_PWROK (PLT->SOC)

Boot device accessed (SOC->PLT) CSE

PLTRST# (SOC->PLT)

SUS_STAT# (SOC->PLT)

EMMC_PWR_EN# (SOC->PLT)

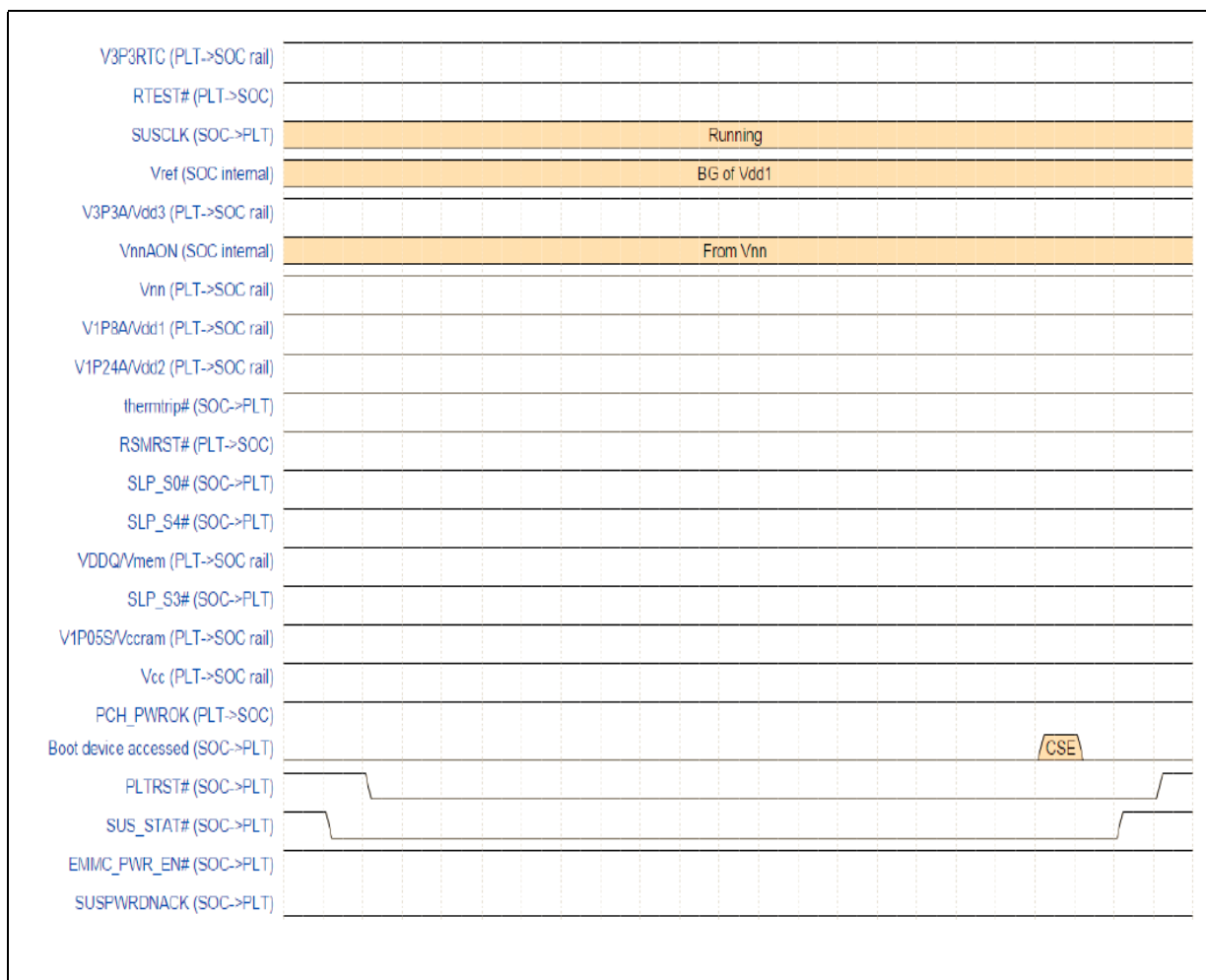
SUSPWRDNACK (SOC->PLT)



4.3.2 Warm Reset

In Warm Reset flow there is no power domain cycled from the PMIC/VR.

Figure 4-8. SoC Warm Reset



4.3.3 Sx Reset

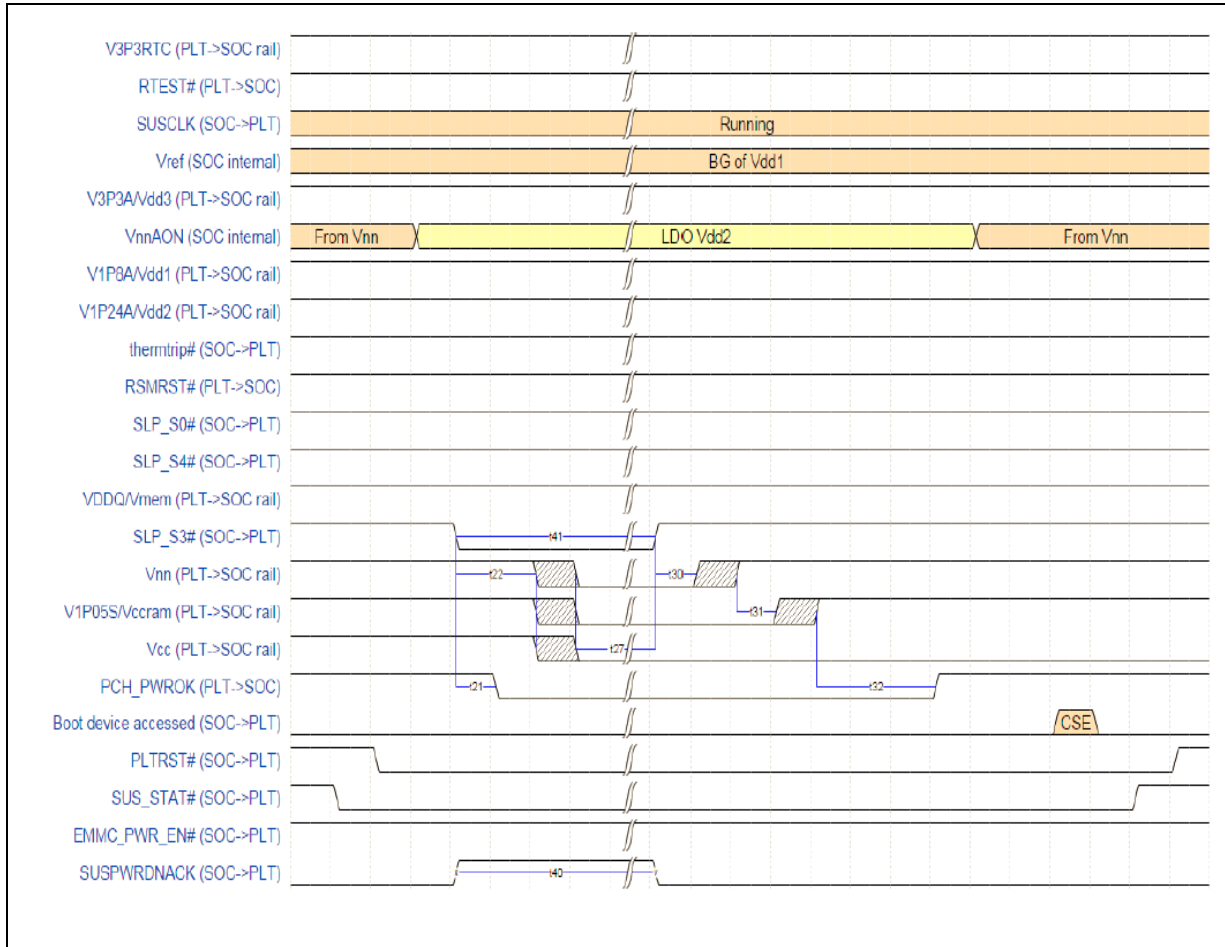
Note: VNN_SVID power states are different during boot and after boot. It starts as an A rail prior to RSM_RST_N assertion. On first transition to S0 state with SOC_PWROK from L to H, VNN_SVID switches from A rail to S rail. As such, it will be turned off during S0Ix/S3/S4 states. SOC_PWROK transition from L to H can be used as the signal to switch VNN over to S rail and assertion of RSM_RST_N from H to L to switch it back to A rail.

4.3.3.1 S3

S3 is very similar to a cold reset with a large exception being that wake events are programmed into the part and the SoC does not come back up right away. In addition, VDDQ is not removed.

Notes:

1. VNN_SVID, VCCRAM_V1P05 and VCC_VCGI are not necessary discharged to 0V during S3. These rails may or may not decay to 0V by the next transition to S0 (i.e. the VR are in the off/not regulating stage).
2. VCCRAM_V1P05 strictly required to be ramped after VNN_SVID is stable during S3 exit (timing requirement not specified).
3. VCC_VCGI rail ramps at first SETVID, after the assertion of SOC_PWROK. Vboot is defined as 0V.

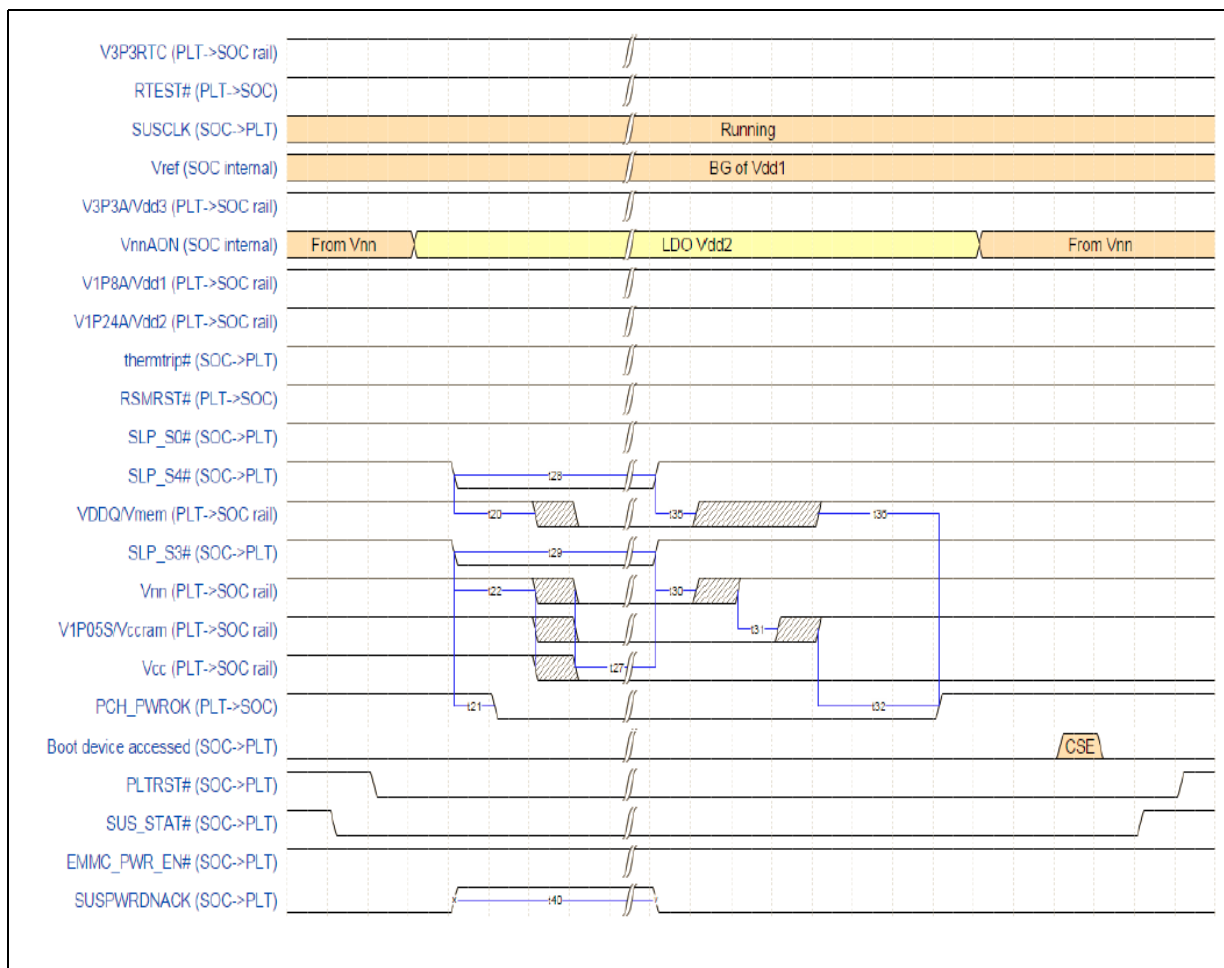
Figure 4-9. SoC S3 Power Sequencing (S0-S3-S0)

4.3.3.2 S4/S5 (With Wakes)

S4/S5 is very similar to a cold reset with a large exception being that wake events are programed into the part and the SoC does not come back up right away. In addition, memory power might have lot in S4.

Notes:

1. VNN_SVID, VCCRAM_V1P05 and VCC_VCGI are not necessary discharged to 0V during S4. These rails may or may not decay to 0V by the next transition to S0 (i.e. the VR are in the off/not regulating stage).
2. VCCRAM_V1P05 strictly required to be ramped after VNN_SVID is stable during S4 exit (timing requirement not specified).
3. VCC_VCGI rail ramps at first SETVID, after the assertion of SOC_PWROK. Vboot is defined as 0V.

Figure 4-10. SoC S4 Power Sequencing (S0-S4-S0)



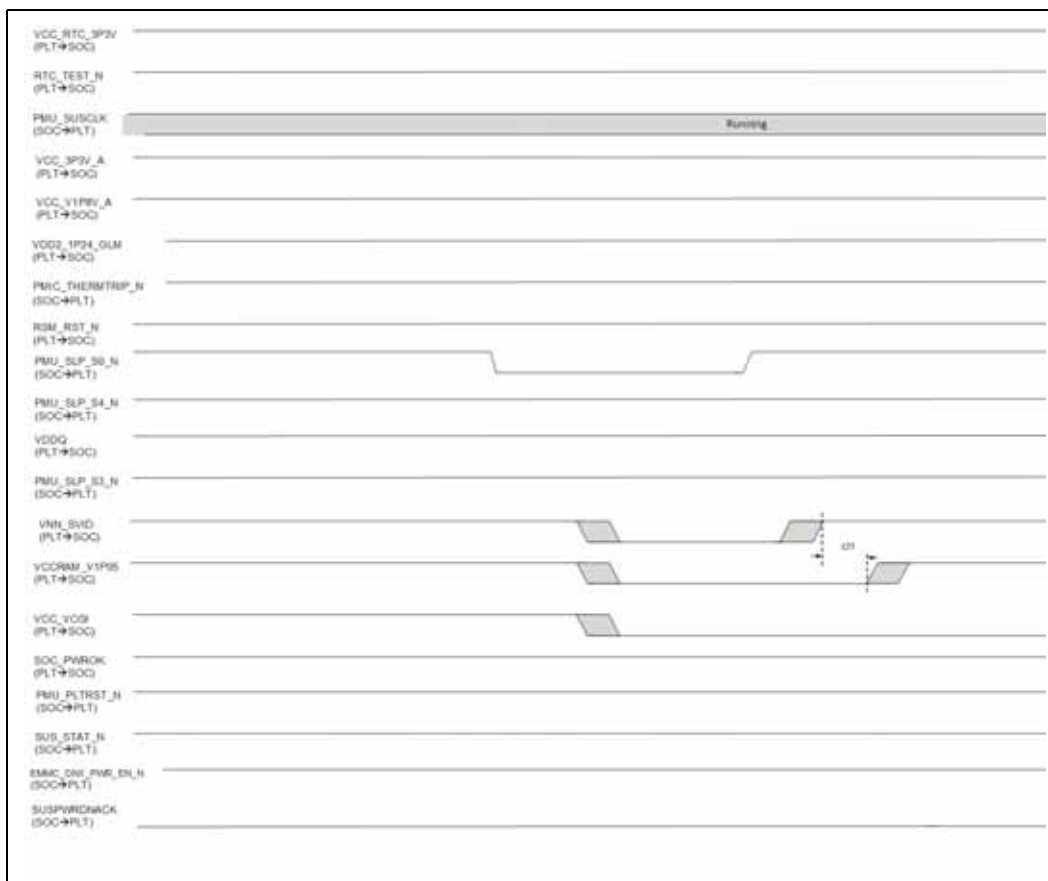
4.3.3.3 S0Ix

S0Ix is the low power state where VNN_SVID and VCCRAM_1P05V are lost.

Notes:

1. SOC_PWROK is not required to be de-asserted but it is allowed to be de-asserted during S0Ix state. In case of SOC_PWROK de-assertion, THERMTRIP_N event will not be triggered, if SOC_PWROK is being de-assert within 1us after the assertion of PMU_SLP_S0_N.
2. VNN_SVID, VCCRAM_V1P05 and VCC_VCGI are not necessary discharged to 0V during S0Ix. These rails may or may not decay to 0V by the next transition to S0 (i.e. the VR are in the off/not regulating stage).
3. VCCRAM_V1P05 strictly required to be ramped after VNN_SVID is stable during S0Ix exit (timing requirement not specified).
4. VCC_VCGI rail ramps at first SETVID, after the assertion of SOC_PWROK. Vboot is defined as 0V.

Figure 4-11. SoC S0Ix Power Sequencing (S0-S0Ix)



4.3.4 Platform Initiated Shutdown

Platform initiated shutdown to take power away from the SOC may be implemented by one of 3 methods, namely:

1. Graceful S5 shutdown
2. Emergency Shutdown of dropping all rails simultaneously
3. Reverse order of Cold Boot with Vnn dropping last but one i.e. before the last rail V3P3.

Notes:

If SOC_PWROK is unexpectedly removed, the SOC will issue a THERMTRIP_N and expect all rails to fall using Emergency Shutdown sequence.

Figure 4-12. Platform Initiated Graceful Shutdown While in S0

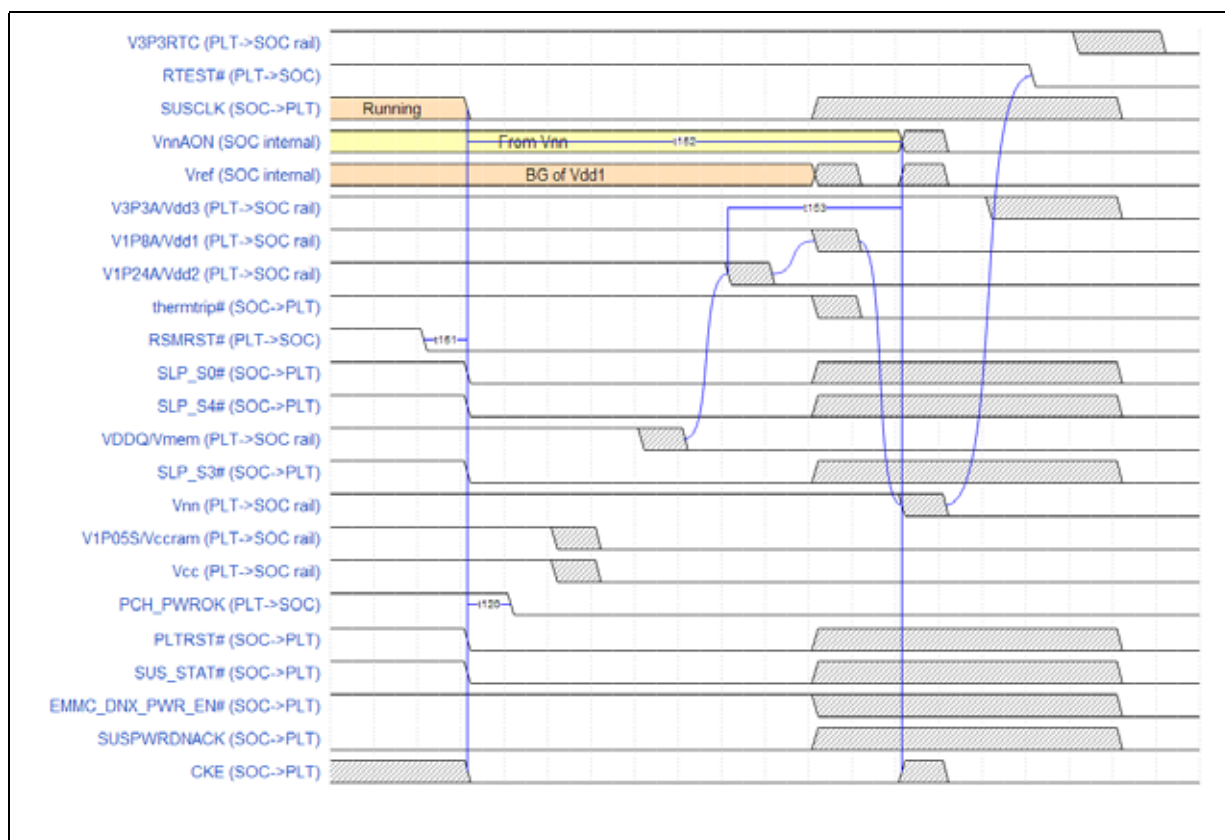
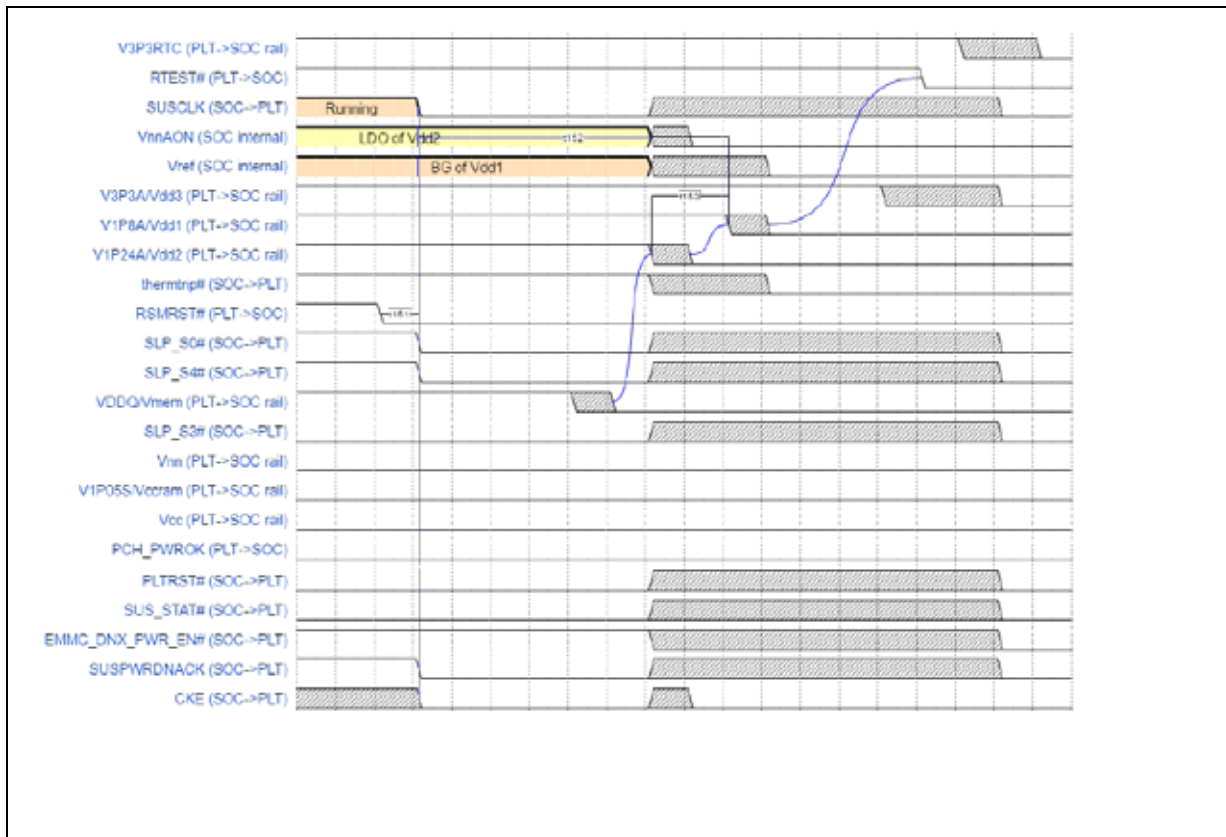


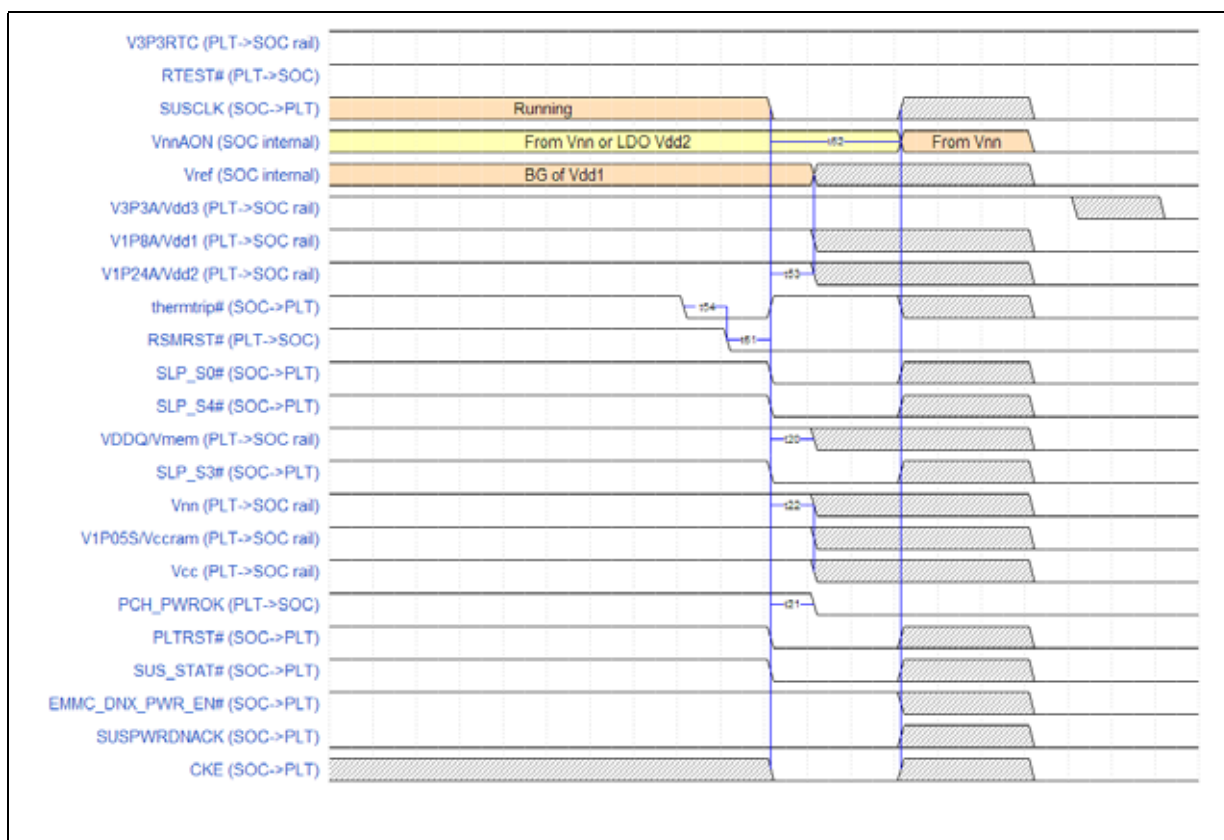
Figure 4-13. Platform Initiated Graceful Shutdown While in S3



4.3.5 Emergency Shutdown (Global Reset)

When THERMTRIP_N asserts, the platform must shutdown. The platform must immediately assert RSM_RST_N and power off all SOC rails (with an exception given to VCC_3P3V_A).

Figure 4-14.THERMTRIP Sequencing



4.4 Timing Requirements

Table 4-1 shows the timing requirement during the reset/power sequence flows.

Table 4-1. Timing Requirements During Reset Flows (Sheet 1 of 3)

Timing Label	Description	Min	Max
t0	VCCRTC_3P3V power to RTC_TEST_N/RTC_RST_N ramped	9 ms ^{1,6,7}	-
t1	VNN ramped to VCC_1P8V_A start of ramp	0 ms	-
t2	VCC_3P3V_A ramped to VCC_1P8V_A start of ramp	0 ms	-
t3	VCC_1P8V_A ramped to VCC_1P24V_A start of ramp	0 ms	-
t4	"A" rails ramped to RSM_RST_N start of ramp	10 ms	-
t5	RSMRST# to RTC clock Running	Platform dependent (i.e. crystal type used). This time can be negative (RTC clock starts before RSMRST#), but when it is positive, it extends to t6.	-
t6	RSM_RST_N to PMU_SUSCLK starts running	95 ms	-

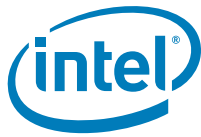


Table 4-1. Timing Requirements During Reset Flows (Sheet 2 of 3)

Timing Label	Description	Min	Max
t7	RTC_TEST_N to RSM_RST_N start of ramp	1 μ s	-
t10	PMU_SLP_S4_N de-assertion to VDDQ ramp start	no requirement	-
t11, t13, t32, t36	All rails stable to SOC_PWROK assertion	5 ms	-
t12	PMU_SLP_S3_N de-assertion to VCC_1P05V start of ramp for G3/G2 exit	no requirement	-
t20	PMU_SLP_S4_N assertion to VDDQ stop regulation	no requirement	-
t21	PMU_SLP_S3_N assertion to SOC_PWROK de-assertion	no requirement	-
t22	PMU_SLP_S3_N assertion to "S" rails stop regulation	no requirement	-
t22-t21	SOC_PWROK deassertion to rails reach (-5%) tolerance	0 μ s	
t25	PMU_SLP_S4_N assertion to PMU_SLP_S4_N de-assertion (cold reset)	Programmable ²	-
t26	PMU_SLP_S3_N assertion to PMU_SLP_S3_N de-assertion (cold reset)	Programmable ²	-
t27	"S" rails 0v to PMU_SLP_S3_N de-assertion	no requirement	
t28	PMU_SLP_S4_N assertion to PMU_SLP_S4_N de-assertion during S4	Programmable ³	
t29	PMU_SLP_S3_N assertion to PMU_SLP_S3_N de-assertion during S4	Programmable ³	
t30	PMU_SLP_S3_N de-assertion to VNN ramp start	no requirement	
t31	VNN ramped to VCC_1P05V ramp start	0 ms	
t35	PMU_SLP_S4_N de-assertion to VDDQ ramp start	no requirement	
t40	SUSPWRDNACK assertion to de-assertion	0 ms (does not stretched with other SLP signals)	
t41	PMU_SLP_S3_N assertion to PMU_SLP_S3_N de-assertion during S3	Programmable ⁴	
t50	"S" rails 0V to RSM_RST_N for G2 entry	no requirement (can be negative)	
t51	RSM_RST_N assertion to SoC output defaults	0 ns	
t52	RSM_RST_N assertion to "x" on all SoC outputs	2048 RTC clocks ⁵	
t54	THERMTRIP_N assertion to RSM_RST_N asserted	-	200 μ s
t51+t53	RSM_RST_N assertion to "A" rails stop regulation	1 μ s	
t51+t53/ t151+t152	RSM_RST_N assertion to "A" rails stop regulation (other than V3P3A)		5 ms
t153	Any "A" rail or (Vnn when RSM_RSTN will be asserted) out of spec to all "A" rails stop regulation		100 μ s
	VCC_3P3V_A ramped without VCC_V1P8_A ramped		500 ms
	RSM_RST_N assertion to starting regulation of Vnn (cold off/ Thermtrip to exiting G3)	100ms, or RTEST_N deassertion then assertion	
t51 / t151	CKE low after RSM_RST_N assertion		100ns

**Table 4-1. Timing Requirements During Reset Flows (Sheet 3 of 3)**

Timing Label	Description	Min	Max
	SLP_S0_N assertion to SOC_PWROK deassertion	Signal might be masked and does not have to deassert	7 us

Notes:

1. Measured from VCCRTC_3P3V-10% to RTC_TEST_N/RTC_RST_N reaching 55%*VCCRTC_3P3V. VCCRTC_3P3V is defined as the final settling voltages that the rail ramps to.
2. Programmable through PMC_CFG.PWR_CYC_DUR register.
3. Programmable through GEN_PMCON3.S4MAW register.
4. Programmable through GEN_PMCON3.SLP_S3_MIN_ASST_WIDTH register.
5. VDD2_1P24_CPU will be lost if SoC is in Sx on assertion. VNN_SVID will be lost if SoC is not in Sx on assertion
6. Capacitors used in the RC delay circuit for each signal should be evaluated with regards to aging, voltage and temperature characteristics to ensure reliable operation in the intended operating environment.

§ §

5 Electrical Specifications

5.1 Absolute Maximum and Minimum Specifications

The absolute maximum and minimum specifications are used to specify conditions allowable outside of the functional limits of the SoC, but with possible reduced life expectancy once returned to function limits.

At conditions exceeding absolute specifications, neither functionality nor long term reliability can be expected. Parts may not function at all once returned to functional limits.

Although the processor contains protective circuitry to resist damage from Electrostatic discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

Table 5-1. Absolute Max and Min values

Supply Name	Description	Min ^{1,2}	Nominal ¹	Max ¹	Unit
vcca_1p8	1.8V IO supply ²	1.66	1.8	1.89	volt
vcca3p3	3.3V IO Supply ²	3.00	3.30	3.45	volt

Notes:

1. Voltages are as measured at the transistor junction including all AC+DC components.
2. Voltage specifications must be met at the transistor junction. Typical bump voltages are 15-25 mV higher and typical pin voltages are 10-20 mV higher than at the bump for IO supplies.

5.2 Thermal Specifications

The following table specifies the thermal limits of SoC operation. Thermal solutions not designed to provide the following level of thermal capability may affect the long-term reliability of the processor and system and more likely result in performance throttling to ensure silicon junction temperatures within Specification.

TjMax defines the maximum operating silicon junction temperature. This is the temperature needed to ensure TDP specifications when running at guaranteed Processor and Graphics frequencies.

“TDP” defines the thermal dissipated power for a worse case estimated real world thermal scenario. “SDP”, or scenario dissipated power, defines the thermal dissipated power under a lighter workload specific to a user scenario and at a lower thermal junction temperature than TjMax. Tj SDP is 80°C and Ti TDP is Tj Max from the below table.

5.2.1 Temperature Requirements [Tsystem]

- For PC SKU's, the SoC must be functional from 0°C to 105°C.
- For IOTG SKU's, the SoC must be functional from -40 to 110C

Note:

TSystem. It is the temperature range of soldered to the board SoC, which is “0 to 105 for PC SKU's and -40 to 110C for IOTG SKU's”. TSystem applies to all system power states, including power off scenario.



Note: TStorage. It is the temperature range at which the SoC can be stored before soldered to the board, which is "-25 to 125C".

Table 5-2. Identification Table for Processor Series

S-Spec	MM #	Stepping	Processor Number	Functional Core	Core Speed		Integrated Graphics Core Speed		TDP (W)
					Burst Frequency Mode (BFM) 2C/1C	High Frequency Mode (HFM)	Burst Frequency	Base Frequency	
R2Y9	951483	B-0	Pentium® N4200	4	2.4 GHz/2.5 GHz	1.1 GHz	750 MHz	200 MHz	6
R2YA	951484	B-0	Celeron® N3450	4	2.1 GHz/2.2 GHz	1.1 GHz	700 MHz	200 MHz	6
R2YB	951485	B-0	Celeron® N3350	2	2.3 GHz/2.4 GHz	1.1 GHz	650 MHz	200 MHz	6
R2ZA	951843	B-1	Pentium® J4205	4	2.5 GHz/2.6 GHz	1.5 GHz	800 MHz	250 MHz	10
R2Z9	951842	B-1	Celeron® J3455	4	2.2 GHz/2.3 GHz	1.5 GHz	750 MHz	250 MHz	10
R2Z8	951841	B-1	Celeron® J3355	2	2.4 GHz/2.5 GHz	2.0 GHz	700 MHz	250 MHz	10
R2Z5	951830	B-1	Pentium® N4200	4	2.4 GHz/2.5 GHz	1.1 GHz	750 MHz	200 MHz	6
R2Z6	951833	B-1	Celeron® N3450	4	2.1 GHz/2.2 GHz	1.1 GHz	700 MHz	200 MHz	6
R2Z7	951834	B-1	Celeron® N3350	2	2.3 GHz/2.4 GHz	1.1 GHz	650 MHz	200 MHz	6

5.3 Storage Conditions

This section specifies absolute maximum and minimum storage temperature and humidity limits for given time durations. Failure to adhere to the specified limits could result in physical damage to the component. If this is suspected, Intel recommends a visual inspection to determine possible physical damage to the silicon or surface components.

Table 5-3. Storage Conditions Prior to Board Attach

Symbol	Parameter	Minimum	Maximum
Tabsolute storage	Device storage temperature range should not exceed for any length of time	-25 °C	125 °C
Tshort term storage	The ambient storage temperature and time for up to 72 hours.	-20 °C	85 °C

Table 5-3. Storage Conditions Prior to Board Attach

Symbol	Parameter	Minimum	Maximum
Tsustained storage	The ambient storage temperature and time for up to 30 months.	-5 °C	40 °C
RHsustained storage	The maximum device storage relative humidity for up to 30 months.	N/A	60% RH @ 24°C
Notes: - Specified temperatures are not to exceed values based on data collected. Exceptions for surface mount re-flow are specified by the applicable JEDEC* standard. Non-adherence may affect processor reliability. - Component product device storage temperature qualification methods may follow JESD22-A119 (low temperature) and JESD22-A103 (high temperature) standards when applicable for volatile memory. - Component stress testing is conducted in conformance with JESD22-A104. - The JEDEC* J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.			

5.4 Post Board-Attach

The storage condition limits for the component once attached to the application board are not specified. Intel does not conduct component-level certification assessments post board-attach given the multitude of attach methods, socket types, and board types used by customers.

Provided as general guidance only, board-level Intel-branded products are specified and certified to meet the following temperature and humidity limits:

- Non-Operating Temperature Limit: -40 °C to 70 °C
- Humidity: 50% to 90%, non-condensing with a maximum wet-bulb of 28 °C

5.5 Voltage, Current, and Crystal Specifications

Note: The specifications listed below are preliminary and subject to change.

5.5.1 Voltage and Current Specifications

Table 5-4. SoC Power Rail DC Specification and Iccmax (Sheet 1 of 2)

Power Type	Voltage Range (V)	Voltage Tolerance (AC+DC+Ripple)	Power Well Description	Iccmax (A)
VCC_VCGI	0, 0.45-1.3 ²	With AVP¹: DC Load Line (DCLL) = 6 mOhms Ripple at Iccmax = +/-15mV TOB ² _Iccmax = +/-20mV	Variable voltage supply to CPU and Graphics Core and ISP logic. SVID and I ² C VID are voltage control interface supported.	21
		Without AVP¹: Voltage Tolerance = +35mV/-161mV		
VNN_SVID	0, 0.45-1.3 ²	+/-50mV	Variable voltage supply to other (non core) logic	3.3
VCCIOA	0, 0.45-1.3	+/-50mV	Notes: - Please tie VCCIOA to VNN_SVID for DDR3L and LPDDR3 designs - Please tie VCCIOA to VDDQ for LPDDR4 designs	1.5

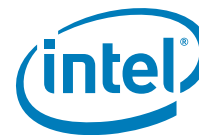


Table 5-4. SoC Power Rail DC Specification and Iccmax (Sheet 2 of 2)

Power Type	Voltage Range (V)	Voltage Tolerance (AC+DC+Ripple)	Power Well Description	Iccmax (A)
VCCRAM_1P05	1.05	+/-5%	Fixed voltage rail for SRAM and I/O Logic	2.7
VCCRAM_1P05_IO	1.05	+/-5%	Fixed voltage rail for SRAM and I/O Logic	
VCC_1P05_INT	1.05	+/-5%	Fixed voltage rail for SRAM and I/O Logic	
VDD2_1P24_CPU	1.24	+/-5%	Fixed voltage rail for SoC L2	1.3
VDD2_1P24_AUD_ISH_PLL	1.24	+/-5%	Fixed voltage rail for Audio & ISH I/O Logic and PLLs	
VDD2_1P24_USB2	1.24	+/-5%	Fixed voltage rail for USB2 I/O	
VDD2_V1P24_DSI_CSI	1.24	+/-5%	Fixed voltage rail for MIPI I/Os	
VCC_1P8V_A	1.8	+/-5%	Fixed voltage rail for all GPIOs	0.4
VDDQ	1.35 (DDR3L)	+/-5%	Fixed voltage rail for DDR3L PHY	2.8 (excluding DRAM)
	1.2 (LPDDR3)	+8.3%/-5%	Fixed voltage rail for LPDDR3 PHY	
	1.1 (LPDDR4)	+6/-4% ³	Fixed voltage rail for LPDDR4 PHY	
VCC_3P3V_A	3.3	+/-5%	Fixed voltage rail for GPIO, I/O logic and USB 2 PHY	0.15
VCC_RTC_3P3V	2-3.47	N/A	Fixed Voltage rail for RTC (Real Time Clock)	6 μ
Notes: 1. AVP: Active Voltage Positioning (this is the same as DC Load Line). 2. The SoCs are capable of issuing VIDs in the range of 450mV to 1.3V. The actual VIDs issued by the SoC in any given power state will dependent on the VR type (IMVP vs I2C) as selected by the platform designer. 3. Iccmax numbers assume top bin SKU and platform supports 4K display and DDR3L/LPDDR3 1866 2x64				

5.5.2 Crystal Specifications

Table 5-5. Integrated Clock Crystal Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
TPPM	Crystal frequency tolerance and stability	-30	30	ppm	1
PDRIVE	Crystal drive load	100		μ W	1, Typical
RESR	ESR		80	Ohm	1
CLOAD	Crystal load capacitance		12	pF	1
CSHUNT	Crystal shunt capacitance		3	pF	1
Note: These are the specifications needed to select a crystal for the Integrated clock oscillator circuit. Crystal must be AT cut, at fundamental frequency, parallel resonance mode.					

Table 5-6. Integrated Clock Oscillation Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
FPLT	Frequency	19.2 - ppm	19.2 + ppm	MHz	Typical= 19.2

Table 5-6. Integrated Clock Oscillation Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
TDC	Duty Cycle	45	55	%	1
TPEAKJIT	Cycle-to-Cycle Jitter (Peak)		300	ps	
TPERJIT	Period Jitter		550	ps	
Note: Measured @50% of 1.8V					

Table 5-7. ILB RTC Crystal Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
FRTC	Frequency		32.768	KHz	Nominal
TPPM	Crystal frequency tolerance	-100	100	ppm	
PDRIVE	Crystal drive load	0.1		μW	Nominal
CLOAD	Crystal Load Capacitance		12.5	pF	12 pF Nominal
CSHUNT	Crystal shunt Capacitance		1.3	pF	
C1/C2	Load Capacitance tolerance	-10	10	%	

5.6 Processor DC Specifications

Platform reference voltages are specified at DC only. VCC measurements should be made with respect to the supply voltages specified in [Table 5-4, "SoC Power Rail DC Specification and Iccmax"](#).

Note: $V_{IH/OH}$ Max and $V_{IL/OL}$ Minimum values are bounded by VCC and VSS.

Note: Care should be taken to read all notes associated with each parameter.

Note: SoC output timing spec, T_{co} , is measured in a tester environment with a test load. Customer should validate and ensure SoC output signal is meeting device's input setup/hold spec, probing at device's pin



5.6.1 DISPLAY

5.6.1.1 Display DC Specification

5.6.1.1.1 Display Port* DC Specification

Table 5-8. Display Port* DC Specification

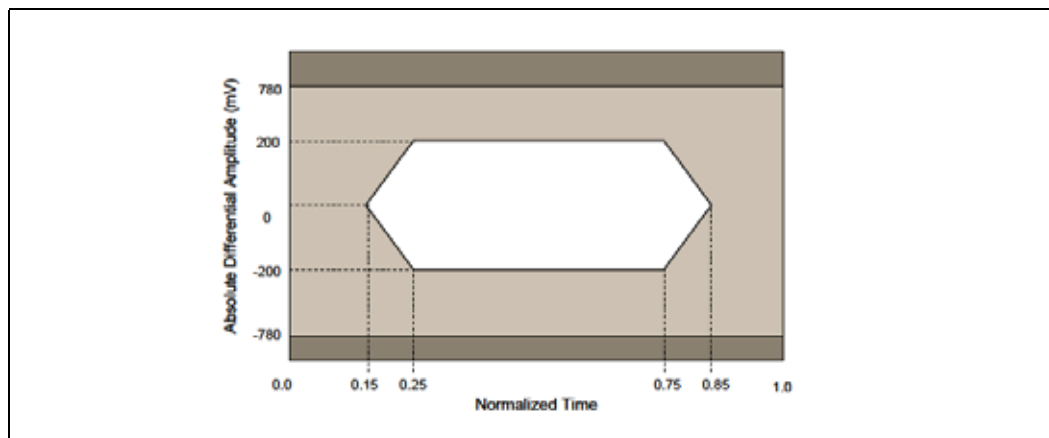
Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VTX-DIFFp-p-Level0	Differential Peak-to-peak Output Voltage Level 0	0.35	0.46	V	
VTX-DIFFp-p-Level1	Differential Peak-to-peak Output Voltage Level 1	0.51	0.68	V	
VTX-DIFFp-p-Level2	Differential Peak-to-peak Output Voltage Level 2	0.69	0.92	V	
VTX-DIFFp-p-Level3	Differential Peak-to-peak Output Voltage Level 3	0.85	1.38	V	
VTX-PREEMP-RATIO	No Pre-emphasis	0	0	dB	
VTX-PREEMP-RATIO	3.5 dB Pre-emphasis	2.8	4.2	dB	
VTX-PREEMP-RATIO	6.0 dB Pre-emphasis	4.8	7.2	dB	
VTX-PREEMP-RATIO	9.5 dB Pre-emphasis	7.5	11.4	dB	
VTX-DC-CM	Tx DC Common Mode Voltage	0	2	V	
RLTX-DIFF	Differential Return Loss at 0.675GHz at Tx Package pins	12		dB	1
RLTX-DIFF	Differential Return Loss at 1.35 GHz at Tx Package pins	9	1.6	dB	1
CTX	TX Output Capacitance	0	1.5	pF	for HBR 2
Notes: 1. Straight loss line between 0.675 GHz and 1.35 GHz. 2. Represents only the effective lump capacitance seen at the SoC interface that shunts the TX termination.					

5.6.1.1.2 HDMI* DC Specification

Table 5-9. HDMI* DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
Voff	Single Ended Standby (off), output voltage	-10	10	mV	1
Vswing	Single Ended output swing voltage	400	600	mV	
VOH (<=165 MHz)	Single Ended high level, output voltage	-10	10	mv	1
VOH (>165 MHz)	Single Ended high level, output voltage	-200	10	mV	1
VOL (<=165 MHz)	Single Ended low level, output voltage	-600	-400	mV	1
VOL (>165 MHz)	Single Ended low level, output voltage	-700	-400	mV	1
Note: The Minimum/Maximum values are with reference to VCC_VCGI.					

Figure 5-1. Eye Diagram Mask for HDMI*



5.6.1.1.3 Embedded Display Port* DC Specification

Table 5-10. Embedded Display Port* DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VTX-DIFFp-p-Level0	Differential Peak-to-peak Output Voltage Level 0	0.18	0.22	V	1,2
VTX-DIFFp-p-Level1	Differential Peak-to-peak Output Voltage Level 1	0.2	0.275	V	1,2
VTX-DIFFp-p-Level2	Differential Peak-to-peak Output Voltage Level 2	0.27	0.33	V	1,2
VTX-DIFFp-p-Level3	Differential Peak-to-peak Output Voltage Level 3	0.315	0.385	V	1,2
VTX-DIFFp-p-Level4	Differential Peak-to-peak Output Voltage Level 4	0.36	0.44	V	1,2
VTX-DIFFp-p-Level5	Differential Peak-to-peak Output Voltage Level 5	0.405	0.495	V	1,2
VTX-DIFFp-p-MAX	Maximum Allowed Differential Peak-to-peak Output Voltage		1.38	V	3
VTX-DC-CM	Tx DC Common Mode Voltage	0	2	V	1
VTX-PREEMP-RATIO	No Pre-emphasis	0	0	dB	1
VTX-PREEMP-RATIO	3.5 dB Pre-emphasis	2.8	4.2	dB	1
VTX-PREEMP-RATIO	6.0 dB Pre-emphasis	4.8	7.2	dB	1
VTX-PREEMP-RATIO	9.5 dB Pre-emphasis	7.5	11.4	dB	1
RLTX-DIFF	Differential Return Loss at 0.675GHz at Tx Package pins	12		dB	4
RLTX-DIFF	Differential Return Loss at 1.35 GHz at Tx Package pins	9		dB	4
CTX	TX Output Capacitance		1.5	pF	5



Table 5-10. Embedded Display Port* DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
Notes: - Steps between VTX-DIFFP-P voltages must be monotonic. The actual VTX-DIFFP-P-1 voltage must be equal to or greater than the actual VTX-DIFFP-P-0 voltage; the actual VTX-DIFFP-P-2 voltage must be greater than the actual VTX-DIFFP-P-1 voltage; and so forth. - The recommended minimum VTX-DIFFP-P delta between adjacent voltages is in mV. - Allows eDP* Source devices to support differential signal voltages compatible with eDP* v1.3 (and lower) devices and designs. - Straight loss line between 0.675 GHz and 1.35 GHz. - Represents only the effective lump capacitance seen at the SoC interface that shunts the TX termination.					

5.6.1.1.4 Display Port* AUX Channel DC Specification

Table 5-11. DDI AUX Channel DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
V _{AUX-DIFFP-p}	AUX Peak-to-peak Voltage at a transmitting Device	0.29	1.38	V	1
V _{AUX-TERM_R}	AUX CH termination DC resistance		100	Ω	
V _{AUX-DC-CM}	AUX DC Common Mode Voltage	0	2	V	2
V _{AUX-TURN-CM}	AUX turn around common mode voltage		0.3	V	3
I _{AUX_SHORT}	AUX Short Circuit Current Limit		90	mA	4
C _{AUX}	AC Coupling Capacitor	75	200	nF	5
Notes: $V_{AUX-DIFFP-p} = 2 * V_{AUXP} - V_{AUXN}$ - Common mode voltage is equal to V_{bias_Tx} (or V_{bias_Rx}) voltage. - Steady-state common mode voltage shift between transmit and receive modes of operation. - Total drive current of the transmitter when it is shorted to its ground. - All Display Port Main Link lanes as well as AUX CH must be AC coupled. AC coupling capacitors must be placed on the transmitter side. Placement of AC coupling capacitors on the receiver side is optional.					

5.6.1.2 Embedded Display Port* AUX Channel DC Specification

Table 5-12. Embedded Display Port* AUX Channel DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
V _{AUX-DIFFp-p}	AUX Peak-to-peak Voltage at a transmitting Device	0.29	1.38	V	1
V _{AUX-TERM_R}	AUX CH termination DC resistance		100	Ω	
V _{AUX-DC-CM}	AUX DC Common Mode Voltage	0	1.2	V	2
V _{AUX-TURN-CM}	AUX turn around common mode voltage		0.3	V	3
I _{AUX_SHORT}	AUX Short Circuit Current Limit		90	mA	4
C _{AUX}	AC Coupling Capacitor	75	200	nF	5
Notes: 1. $V_{AUX-DIFFp-p} = 2 * V_{AUXP} - V_{AUXN} $ 2. Common mode voltage is equal to V _{bias_Tx} (or V _{bias_Rx}) voltage. 3. Steady state common mode voltage shift between transmit and receive modes of operation. 4. Total drive current of the transmitter when it is shorted to its ground. 5. All Display Port Main Link lanes as well as AUX CH must be AC coupled. AC coupling capacitors must be placed on the transmitter side. Placement of AC coupling capacitors on the receiver side is optional.					

5.6.1.3 DDI Panel GPIO DC Specification

[PNL0_BKLTCTL, PNL0_BKLTEN, PNL0_VDDEN, PNL1_BKLTCTL, PNL1_BKLTEN, PNL1_VDDEN/DDI_HPDI]

Table 5-13. DDI Panel GPIO Signals DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
V _{IH}	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
V _{IL}	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
V _{OH}	Output High voltage	1.35		V	@1.80V nominal (Vcc- 0.45), @ 1.5mA load
V _{OL}	Output Low Voltage		0.45	V	@ -1.5mA load.
I _{PAD}	Pad Leakage Current	-5	5	μA	
Z _{UP}	Driver Pull-up Impedance	160	240	Ohm	200 Ohm nominal
Z _{DN}	Driver Pull-down Impedance	160	240	Ohm	200 Ohm nominal
W _{pup20K}	Weak Pull-up Impedance 20K	8	50	kOhm	20 kOhm nominal
W _{pdn20K}	Weak Pull-down Impedance 20K	8	50	kOhm	20 kOhm nominal
V _{hys}	RX hysteresis	100		mV	
C _{in}	Pad Capacitance		5	pF	



5.6.1.4 MIPI*-DSI DC Specification

Table 5-14. MIPI*-DSI DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
ILEAK	Pin Leakage current	-10	28	μA	
VCMTX	HS transmit static common-mode voltage	150	250	mV	
VCMTX(1,0)	VCMTX mismatch when output is differential-1 or differential-0		5	mV	
VOD	HS transmit differential voltage	140	270	mV	
ΔVOD	VOD mismatch when output is Differential-1 or Differential-0		14	mV	
VOHHS	HS output high voltage		360	mV	
ZOS	Single-ended output impedance	40	62.5	Ohm	
ΔZOS	Single-ended output impedance mismatch		10	%	
VOH	Thevenin output high level	1.1	1.3	V	
VOL	Thevenin output low level	-50	50	mV	
ZOLP	Output impedance of LP transmitter	110		Ohm	1
VIH	Logic 1 input voltage	880		mV	
VIL	Logic 0 input voltage, not in ULP state		550	mV	
VHYS	Input hysteresis	25		mV	
VIHCD	Logic 1 Contention threshold	450		mV	
VILCD	Logic 0 Contention threshold		200	mV	
Note: Deviates from MIPI* D-PHY specification Rev 1.1, which has minimum ZOLP of 110 Ohm.					

5.6.1.5 MIPI*-DSI GPIO DC Specification [MDSI_A_TE, MDSI_C_TE]

Table 5-15. MIPI*-DSI GPIO Signals DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VOH	Output High Voltage	1.35		V	@1.80V nominal (Vcc-0.45), @1.5mA Load
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
VIH	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
VIL	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
VOL	Output Low Voltage		0.45	V	@-1.5mA Load
IPAD	Pad Leakage Current	-5	5	uA	
ZUP	Driver Pull-up Impedance	160	240	Ohm	200 Ohm nominal
ZDN	Driver Pull-down Impedance	160	240	Ohm	200 Ohm nominal
Wpup20K	Weak Pull-up Impedance 20K	8	50	kOhm	20 kOhm nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	50	kOhm	20 kOhm nominal

Table 5-15. MIPI*-DSI GPIO Signals DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
V _{hys}	RX hysteresis	100		mV	
C _{in}	Pad Capacitance		5	pF	

5.6.2 MIPI*-CSI

5.6.2.1 MIPI*-CSI DC Specification

Table 5-16. MIPI HS-RX/MIPI LP-RX Minimum, Nominal, and Maximum Voltage Parameters

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
I _{LEAK}	Pin Leakage current [MCSI_DN[0:3]/MCSI_CLKN_0/2]]	-20	75	μA	
	Pin Leakage current[MCSI_DN[0:3]/MCSI_CLKN_0/2]]	-10	32	μA	
	Pin Leakage current[MCSI_RX_DATA[3:0]_P/N / MCSI_RX_CLK[1:0]_P/n]	-30	30	μA	
V _{CMRX(DC)}	Common-mode voltage HS receive mode	70	330	mV	1
V _{IDTH}	Differential input high threshold		70	mV	
V _{IDTL}	Differential input low threshold	-70		mV	
V _{IHHS}	Single-ended input high voltage		460	mV	
V _{ILHS}	Single-ended input low voltage	-40		mV	
V _{TERM-EN}	Single-ended threshold for HS termination enable		450	mV	
Z _{ID}	Differential input impedance	80	125	Ω	
V _{IH}	Logic 1 input voltage	880		mV	
V _{IL}	Logic 0 input voltage, not in ULP state		550	mV	
V _{IL-ULPS}	Logic 0 input voltage, ULP state		300	mV	
V _{HYST}	Input hysteresis	25		mV	
Note: Setup/hold violation will be seen for a VCM higher than 250mv.					

Table 5-17. MIPI*-CSI Clock Signal Specification

Symbol	Clock Parameter	Minimum	Typical	Maximum	Unit	Notes
U _{IINST}	UI Instantaneous (In 1 or 2 or 3 or 4 Lane configuration)			12.5	ns	1, 2



Table 5-17. MIPI *-CSI Clock Signal Specification

Symbol	Clock Parameter	Minimum	Typical	Maximum	Unit	Notes
ΔUI	UI Variation	-10%		10%	UI	3
		-5%		5%	UI	4
Notes: 1. This value corresponds to a minimum 80 Mbps data rate. 2. The minimum UI shall not be violated for any single bit period. The allowed instantaneous UI variation can cause instantaneous data rate variations. Therefore, slave devices should be able to accommodate these instantaneous variations of the UI interval. 3. When $UI \geq 1$ ns, within a single burst. 4. When $UI < 1$ ns, within a single burst. The minimum UI shall not be violated for any single bit period, that is, any DDR half cycle within a data burst.						

5.6.2.2 MIPI *-CSI Camera Side Band Signals

Table 5-18. MIPI *-CSI Camera Side Band DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VCC	I/O Voltage	1.66	1.89	V	1.80V nominal
V _{IH}	Input High Voltage	1.17		V	@1.80V nominal (0.65*V _{CC})
V _{IL}	Input Low Voltage		0.63	V	@1.80V nominal (0.35*V _{CC})
V _{OH}	Output High Voltage	1.35		V	@1.80V nominal (V _{CC} -0.45), @ 1.5mA load.
V _{OL}	Output Low Voltage		0.45	V	@ -1.5mA load.
I _{PAD}	Pad Leakage Current	-5	5	uA	
Z _{UP}	Driver Pull-up Impedance	160	240	Ohm	200 Ohm nominal
Z _{DN}	Driver Pull-down Impedance	160	240	Ohm	200 Ohm nominal
W _{pup20K}	Weak Pull-up Impedance 20K	8	50	kOhm	20 kOhm nominal
W _{pdn20K}	Weak Pull-down Impedance 20K	8	50	kOhm	20 kOhm nominal
V _{hys}	RX hysteresis	100		mV	
C _{in}	Pad Capacitance		5	pF	

5.6.3 Memory Specifications

5.6.3.1 DDR3L DC Specification

Table 5-19. DDR3L DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
V _{DDQ}	Nominal Voltage	1.2825	1.4175	V	@1.35V Nominal
V _{IL}	Input Low Voltage		0.55	V	@ v _{ref} = 0.675
V _{IH}	Input High Voltage	0.8		V	1
V _{OL}	Output Low Voltage		0.4		
V _{OH}	Output High Voltage	0.95		V	1
I _{IL}	Input Leakage Current	-37.5	37.5	uA	

Table 5-19. DDR3L DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
C _{IO}	DQ/DQS/DQS# DDR3L IO Pin Capacitance		2	pF	
Note: V _{OH} and V _{IH} measurements are taken at R _{on} = 40 Ohms and I _{Load} = 10mA					

5.6.3.2 LPDDR3 Memory Controller DC Specification

Table 5-20. LPDDR3 DC Specifications

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VDDQ	I/O Supply Voltage	1.188	1.302	V	@1.24V Nominal
V _{IL}	Input Low Voltage		0.855	V	@Vref = 0.98
V _{IH}	Input High Voltage	1.105		V	1, @Vref = 0.98
V _{OL}	Output Low Voltage		0.4	V	
V _{OH}	Output High Voltage	0.84		V	1
I _{IL}	Input Leakage Current	-20	20	μA	
C _{IO}	I/O Pin Capacitance		2	pF	
Note: V _{OH} and V _{IH} measurements are taken at R _{on} = 40 Ohms and I _{Load} = 10mA					

5.6.3.3 LPDDR4 DC Specifications

Table 5-21. LPDDR4 DC Specifications

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VDDQ	I/O Supply Voltage	1.064	1.176	V	@1.1V Nominal
V _{IL}	Input Low Voltage		0.175	V	@RxVref=0.3
V _{IH}	Input High Voltage	0.425		V	@RxVref=0.3
V _{OL}	Output Low Voltage		0.4	V	
V _{OH}	Output High Voltage	0.72		V	@ Ron = 40 Ohms/Iload = 10mA
I _{IL}	Input Leakage Current	-20	20	μA	
C _{IO}	I/O Pin Capacitance		2	pF	



5.6.4 SD Card

5.6.4.1 SD Card DC Specification

Table 5-22. SD Card Signal Group DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VCC(3.3)	I/O Voltage (3.3V)	3.05	3.45		@3.3V nominal
VCC(1.8)	I/O Voltage (1.8V)	1.66	1.89	V	@1.8V nominal
VOH	Output High Voltage	1.62		V	@1.8V nominal (Vcc-0.18), 3mA test load
VOL	Output Low Voltage		0.18	V	@-3mA test load
VIH (3.3)	Input High Voltage (3.3 V)	1.442		V	
VIL (3.3)	Input Low Voltage (3.3 V)		0.771	V	
VIH (1.8)	Input High Voltage (1.8 V)	1.251		V	
VIL (1.8)	Input Low Voltage (1.8 V)		0.609	V	
IPAD	Pad Leakage	-11	32	uA	
CPAD	PAD Capacitance		9	pF	
ZUP	Driver Pull Up Impedance	32	48	Ohm	20 Ohm nominal
ZDN	Driver Pull down Impedance	32	48	Ohm	20 Ohm nominal
Wpup20K	Weak Pull-up Impedance 20K	10	30	kOhm	20k Ohm nominal
Wpdn20K	Weak Pull Down Impedance 20K	10	30	kOhm	20k Ohm nominal
Vhys (1.8)	RX hysteresis (1.8V)	116		mV	
Vhys (3.3)	RX hysteresis (3.3V)	125		mV	

5.6.5 eMMC*

5.6.5.1 eMMC* DC Specification

Table 5-23. eMMC* Signal Group DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
VOH	Output HIGH voltage	1.35		V	@1.80V nominal (Vcc- 0.45), @ 3mA load.
VOI	Output LOW voltage		0.45	V	@ -3mA load
VIH	Input HIGH voltage	1.17		V	@1.80V nominal (0.65*Vcc)
VIL	Input LOW voltage		0.63	V	@1.80V nominal (0.35*Vcc)
CL	Bus Signal Line capacitance		5	pF	
IPAD	Pad Leakage Current	-5	5	uA	
ZUP	Driver Pull-up Impedance	32	48	Ohm	40 Ohm nominal
ZDN	Driver Pull-down Impedance	32	48	Ohm	40 Ohm nominal

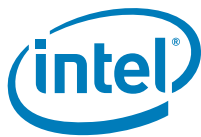


Table 5-23. eMMC* Signal Group DC Specification (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
Wpup20K	Weak Pull-up Impedance 20K	8	44	kOhm	20kOhm nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	44	kOhm	20kOhm nominal
Vhys	RX hysteresis	100		mV	
Cin	Pad Capacitance		5	pF	

5.6.6 JTAG

5.6.6.1 JTAG DC Specification

5.6.6.1.1 JTAG Signals [JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TRST_N, JTAG_PMODE, JTAG_PRDY_N, JTAG_TDO]

Table 5-24. JTAG DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figures
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
VIH	Input High Voltage	1.17		V	@ 1.80V nominal (0.65*Vcc)
VIL	Input Low Voltage		0.63	V	@ 1.80V nominal (0.35*Vcc)
VOH	Output High Voltage	1.35		V	@ 3mA load
VOL	Output Low Voltage		0.45	V	@ -3mA load
Wwpu-20K	Weak Pull-up Impedance 20K	8	44	kOhm	20 kOhm nominal
Wwpd-20K	Weak Pull-down Impedance 20K	8	44	kOhm	20 kOhm nominal
Zup	Driver Pull-up Impedance	40	60	Ohm	Nominal=50 Ohm
Zdn	Driver Pull-down Impedance	40	60	Ohm	Nominal=50 Ohm
Vhys	RX hysteresis	100		mV	
Ipad	Pad Current	-5	5	μA	

**Table 5-25. JTAG AC Specification****5.6.6.2 JTAG DC Signals [JTAG_PREQ_N, JTAGX]****Table 5-26. JTAG DC Specification**

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
VIH	Input High Voltage	1.17		V	@1.80V nominal(0.65*Vcc)
VIL	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
VOL	Output Low Voltage		0.45	V	@ -3mA load. Open Drain.
Wwpu-1K	Weak Pull-up Impedance 1K	0.65	1.35	kOhm	1 kOhm nominal
Wwpu-2K	Weak Pull-up Impedance 2K	1.3	2.7	kOhm	2 kOhm nominal
Wwup-20K	Weak Pull-up Impedance 20K	8	50	kOhm	20 kOhm nominal
Wwpd-20K	Weak Pull-down Impedance 20K	8	50	kOhm	20 kOhm nominal
Zdn	Driver Pull-down Impedance	23	43	Ohm	33 Ohm nominal
Vhys	RX hysteresis	100		mV	
Ipad	Pad Current	-5	5	μA	

5.6.7 USB**5.6.7.1 USB 2.0 DC Specification****Table 5-27. USB 2.0 Host DC Specification (Sheet 1 of 3)**

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VBUS	High-power Port	4.75	5.25	V	2
VBUS	Low-power Port	4.2	5.25		
ICCPRT	High-power Hub Port (out)	500		mA	
ICCUPT	Low-power Hub Port (out)	100		mA	
ICCHPF	High-power Function (in)		500	mA	
ICCLPF	Low-power Function (in)		100	mA	
ICCINIT	Unconfigured Function/Hub (in)		100	mA	
ICCSH	Suspended High-power Device		2.5	mA	15
ICCSL	Suspended Low-power Device		500	μA	
VIH	High (driven)	2		V	4
VIHZ	High (floating)	2.7	3.6	V	4
VIL	Low		0.8	V	4
VDI	Differential Input Sensitivity	0.2		V	4
VCM	Differential Common Mode Range	0.8	2.5	V	4

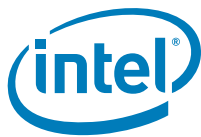


Table 5-27. USB 2.0 Host DC Specification (Sheet 2 of 3)

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VHSSQ	High-speed squelch detection threshold (differential signal amplitude)	100	200	mV	
VHSDSC	High speed disconnect detection threshold (differential signal amplitude)	525	625	mV	
VHSCM	High-speed data signaling common mode voltage range (guideline for receiver)	-50	500	mV	
VOL	Low	0	0.3	V	4,5
VOH	High (Driven)	2.8	3.6	V	4,6
VOSE1	SE1	0.8		V	
VCRS	Output Signal Crossover Voltage	1.3	2	V	10
VHSOI	High-speed idle level	-10	10	mV	
VHSOH	High-speed data signaling high	360	440	mV	
VHSOL	High-speed data signaling low	-10	10	mV	
VCHIRPJ	Chirp J level (differential voltage)	700	1100	mV	
VCHIRPK	Chirp K level (differential voltage)	-900	-500	mV	
CHPB	Downstream Facing Port Bypass Capacitance (per hub)	120		μF	
CRPB	Upstream Facing Port Bypass Capacitance	1	10	μF	9
CIND	Downstream Facing Port		150	pF	2
CINUB	Upstream Facing Port (w/o cable)		100	pF	3
CEDGE	Transceiver edge rate control capacitance		75	pF	
RPU	Bus Pull-up Resistor on Upstream Facing Port	1.425	1.575	kOhm	1.5 kOhm ±5%
RPD	Bus Pull-down Resistor on Downstream Facing Port	14.25	15.75	kOhm	1.5 kOhm ±5%
ZINP	Input impedance exclusive of pull- up/pull-down (for low/full speed)	300		kOhm	
VTERM	Termination voltage for upstream facing port pull-up (RPU)	3	3.6	V	
VHSTER M	Termination voltage in high speed	-10	10	mV	
RTERM	High Speed Termination	40.5	49.5	Ohm	
VBUSD	VBUS Voltage drop for detachable cables		125	mV	Should be 125mV max.



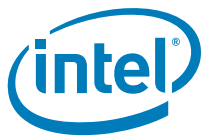
Table 5-27. USB 2.0 Host DC Specification (Sheet 3 of 3)

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
Notes: 1. Measured at A plug 2. Measured at A receptacle 3. Measured at B receptacle 4. Measured at A or B connector 5. Measured with RL of 1.425 kOhm to 3.6V. 6. Measured with RL of 14.25 kOhm to GND. 7. Timing difference between the differential data signals. 8. Measured at crossover point of differential data signals. 9. The maximum load specification is the maximum effective capacitive load allowed that meets the target VBUS drop of 330mV. 10. Excluding the first transition from the Idle state. 11. The two transitions should be a (nominal) bit time apart. 12. For both transitions of differential signaling. 13. Must accept as valid EOP 14. Single-ended capacitance of D+ or D- is the capacitance of D+/D- to all other conductors and, if present, shield in the cable. That is, to measure the single-ended capacitance of D+, short D-, VBUS, GND, and the shield line together and measure the capacitance of D+ to the other conductors. 15. For high power devices (non-hubs) when enabled for remote wakeup					

5.6.7.2 USB 3.0 DC Specification

Table 5-28. USB 3.0 Interface DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
UI	Unit Interval	199.94	200.06	ps	1
V _{TX-DIFF-PP}	Differential peak-peak Tx voltage swing	0.9	1.05	V	
V _{TX-DIFF-PP-LOW}	Low-Power Differential peak-peak Tx voltage swing	0.4	1.2	V	2
V _{TX-DE-RATIO}	Tx De-Emphasis	3	4	dB	
R _{TX-DIFF-DC}	DC differential impedance	68	92	Ohm	
V _{TX-RCV-DETECT}	The amount of voltage change allowed during Receiver Detection		0.6	V	3
C _{AC-COUPLING}	AC Coupling Capacitor	75	200	nF	4
t _{CDR_SLEW_MAX}	Maximum slew rate		10	mV/s	
Notes: 1. The specified UI is equivalent to a tolerance of 300 ppm for each device. Period does not account for SSC induced variations. 2. There is no de-emphasis requirement in this mode. De-emphasis is implementation specific for this mode. 3. Detect voltage transition should be an increase in voltage on the pin looking at the detect signal to avoid a high impedance requirement when an "off" receiver's input goes below output. 4. All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.					



5.6.7.3 USB GPIO DC Specification [USB_OC0_N, USB_OC1_N]

Table 5-29. USB GPIO Signals DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
VIH	Input High Voltage	1.17		V	@1.80V nominal(0.65*Vcc)
VIL	Input Low Voltage		0.63	V	@1.80V nominal(0.35*Vcc)
VOH	Output High Voltage	1.35		V	@1.80V nominal(Vcc-0.45), @ 1.5mA load.
VOL	Output Low Voltage		0.45	V	@ -1.5mA load.
IPAD	Pad Leakage Current	-5	5	μA	
ZUP	Driver Pull-up Impedance	160	240	Ohm	200 Ohm nominal
ZDN	Driver Pull-down Impedance	160	240	Ohm	200 Ohm nominal
Wpup20K	Weak Pull-up Impedance 20K	8	50	kOhm	20 kOhm nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	50	kOhm	20 kOhm nominal
Vhys	RX hysteresis	100		mV	
Cin	Pad Capacitance		5	pF	

5.6.8 SPI

5.6.8.1 SIO SPI DC Specification

Table 5-30. SIO SPI Signal Group DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
VIH	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
VIL	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
VOH	Output High Voltage	1.35		V	@1.80V nominal (Vcc- 0.45), @ 3mA load.
VOL	Output Low Voltage		0.45	V	@ -3mA load.
IPAD	Pad Leakage Current	-5	5	uA	
ZUP	Driver Pull-up Impedance	40	60	Ohm	50 Ohm nominal
ZDN	Driver Pull-down Impedance	40	60	Ohm	50 Ohm nominal
Wpup20K	Weak Pull-up Impedance 20K	8	44	kOhm	20 kOhm nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	44	kOhm	20 kOhm nominal
Vhys	RX hysteresis	100		mV	
Cin	Pad Capacitance		5	pF	



5.6.8.2 FAST SPI DC Specification

Table 5-31. FAST SPI Signal Group DC Specification

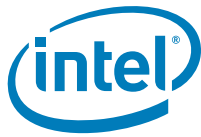
Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
V _{IH}	Input High Voltage	1.17		V	@1.80V nominal (0.65*V _{CC})
V _{IL}	Input Low Voltage		0.63	V	@1.80V nominal (0.35*V _{CC})
V _{OH}	Output High Voltage	1.35		V	@1.80V nominal (V _{CC} - 0.45), @ 3mA load.
V _{OL}	Output Low Voltage		0.45	V	@ -3mA load.
I _{PAD}	Pad Leakage Current	-5	5	μA	
Z _{UP}	Driver Pull-up Impedance	27	40	Ohm	33.5 Ohm nominal
Z _{DN}	Driver Pull-down Impedance	27	40	Ohm	33.5 Ohm nominal
W _{pup20K}	Weak Pull-up Impedance 20K	8	44	kOhm	20 kOhm nominal
W _{pdn20K}	Weak Pull-down Impedance 20K	8	44	kOhm	20 kOhm nominal
V _{hys}	RX hysteresis	100		mV	
C _{in}	Pad Capacitance		5	pF	

5.6.9 SVID

5.6.9.1 SVID DC Specification

Table 5-32. SVID Signal Group DC Specification (SVID_DATA, SVID_CLK, SVID_ALERT_N)

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1	1.1	V	1.05V Nominal
V _{IH}	Input High Voltage	0.6825		V	@1.05V nominal (0.65*V _{CC})
V _{IL}	Input Low Voltage		0.3675	V	@1.05V nominal (0.35*V _{CC})
V _{OL}	Output Low Voltage		0.45	V	@3mA Load
I _{PAD}	Pad Leakage Current	-5	5	μA	
Z _{DN}	Driver Pull-down Impedance	15	26	Ohm	20 Ohm Nominal
W _{pup20K}	Weak Pull-up Impedance 20K	8	50	kOhm	20 kOhm nominal
W _{pdn20K}	Weak Pull-down Impedance 20K	8	50	kOhm	20 kOhm nominal
V _{hys}	RX hysteresis	100		mV	
C _{in}	Pad Capacitance		5	pF	



5.6.10 LPSS UART

5.6.10.1 LPSS UART DC Specification

Table 5-33. LPSS UART Signals DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
V _{IH}	Input High Voltage	1.17		V	@1.80V nominal (0.65*V _{CC})
V _{IL}	Input Low Voltage		0.63	V	@1.80V nominal (0.35*V _{CC})
V _{OH}	Output High Voltage	1.35		V	@1.80V nominal (V _{CC} - 0.45), @ 1.5mA load.
V _{OL}	Output Low Voltage		0.45	V	@ -1.5mA load.
I _{PAD}	Pad Leakage Current	-5	5	uA	
Z _{UP}	Driver Pull-up Impedance	160	240	Ohm	200 Ohm nominal
Z _{DN}	Driver Pull-down Impedance	160	240	Ohm	200 Ohm nominal
W _{pup20K}	Weak Pull-up Impedance 20K	8	50	kOhm	20 kOhm nominal
W _{pdn20K}	Weak Pull-down Impedance 20K	8	50	kOhm	20 kOhm nominal
V _{hys}	RX hysteresis	100		mV	
C _{in}	Pad Capacitance		5	pF	

5.6.11 I²S (Audio)

5.6.11.1 I²S (Audio) DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
V _{IH}	Input High Voltage	1.17		V	@1.80V nominal (0.65*V _{CC})
V _{IL}	Input Low Voltage		0.63	V	@1.80V nominal (0.35*V _{CC})
V _{OH}	Output High Voltage	1.35		V	@1.80V nominal (V _{CC} - 0.45), @ 3mA load
V _{OL}	Output Low Voltage		0.45	V	@ -3mA load
I _{PAD}	Pad Leakage Current	-5	5	μA	
Z _{UP}	Driver Pull-up Impedance	54	80	Ohm	67 Ohm nominal
Z _{DN}	Driver Pull-down Impedance	54	80	Ohm	67 Ohm nominal
W _{pup20K}	Weak Pull-up Impedance 20K	8	44	kOhm	20 kOhm nominal
W _{pdn20K}	Weak Pull-down Impedance 20K	8	44	kOhm	20 kOhm nominal
V _{hys}	RX hysteresis	100		mV	
C _{in}	Pad Capacitance		5	pF	



5.6.12 AVS DMIC

5.6.12.1 AVS DMIC DC Specification

Table 5-34. AVS DMIC Signals DC Specification

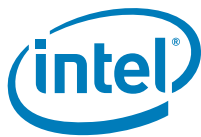
Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
VIH	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
VIL	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
VOH	Output High Voltage	1.35		V	@1.80V nominal (Vcc- 0.45), @ 3mA load.
VOL	Output Low Voltage		0.45	V	@ -3mA load.
IPAD	Pad Leakage Current	-5	5	uA	
ZUP	Driver Pull-up Impedance	54	80	Ohm	67 Ohm nominal
ZDN	Driver Pull-down Impedance	54	80	Ohm	67 Ohm nominal
Wpup20K	Weak Pull-up Impedance 20K	8	50	kOhm	20 kOhm nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	50	kOhm	20 kOhm nominal
Vhys	RX hysteresis	100		mV	
Cin	Pad Capacitance		5	pF	

5.6.13 I²C

5.6.13.1 I²C SIO/PMIC/ISH/MIPI/DDI_DDC DC Specification

Table 5-35. I²C SIO/PMIC/ISH/MIPI/DDI_DDC Signals DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
VIH	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
VIL	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
VOL	Output Low Voltage		0.45	V	@ -3mA load.
IPAD	Pad Leakage Current	-5	5	uA	
ZDN	Driver Pull-down Impedance	10	300	Ohm	
Wpup1K	Weak Pull-up Impedance 1K	0.65	1.35	kOhm	1 kOhm nominal
Wpup2K	Weak Pull-up Impedance 2K	1.3	2.7	kOhm	2 kOhm nominal
Wpup20K	Weak Pull-up Impedance 20K	8	50	kOhm	20 kOhm nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	50	kOhm	20 kOhm nominal
Vhys	RX hysteresis	100		mV	
Cin	Pad Capacitance		5	pF	



5.6.14 HDA

5.6.14.1 HDA DC Specification

Table 5-36. HDA Signal Group DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
VIH	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
VIL	Input Low Voltage		0.63	V	@1.80V nominal (0.65*Vcc)
VOH	Output High Voltage	1.35		V	@1.80V nominal (Vcc-0.45), @ 1.5mA load.
VOL	Output Low Voltage		0.45	V	@ -1.5mA load.
IPAD	Pad Leakage Current	-5	5	uA	
ZUP	Driver Pull-up Impedance	40	60	Ohm	50 Ohm nominal
ZDN	Driver Pull-down Impedance	40	60	Ohm	50 Ohm nominal
Wpup20K	Weak Pull-up Impedance 20K	8	44	kOhm	20 kOhm nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	44	kOhm	20 kOhm nominal
Vhys	RX hysteresis	100		mV	
Cin	Pad Capacitance		5	pF	

5.6.15 LPC

5.6.15.1 LPC DC Specification

Table 5-37. LPC Signals DC Specification (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VCC (3.3)	I/O Voltage (3.3)	3.05	3.45	V	3.3V nominal
VCC(1.8)	I/O Voltage (1.8)	1.66	1.89	V	1.8V nominal
VIH (3.3)	Input high Voltage (3.3)	1.442		V	
VIL (3.3)	Input Low Voltage (3.3)		0.771	V	
VIH (1.8)	Input High Voltage (1.8)	1.251		V	
VIL (1.8)	Input Low Voltage (1.8)		0.609	V	
VOH (3.3)	Output High Voltage (3.3)	2.85		V	@3.3V nominal (Vcc-0.45), @ 3mA load.
VOL (3.3)	Output Low Voltage (3.3)		0.45	V	@ -3mA load.
VOH (1.8)	Output High Voltage (1.8)	1.62		V	@1.80V nominal (Vcc- 0.18), @ 3mA load.
VOL (1.8)	Output Low Voltage (1.8)		0.18	V	@ -3mA load.
IPAD	Pad Leakage Current	-11	32	μA	

**Table 5-37. LPC Signals DC Specification (Sheet 2 of 2)**

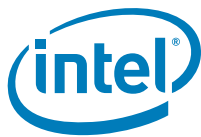
Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
ZUP	Driver Pull-up Impedance	40	60	Ohm	50 Ohm nominal
ZDN	Driver Pull-down Impedance	40	60	Ohm	50 Ohm nominal
Wpup20K	Weak Pull-up Impedance 20K	10	30	kOhm	20 kOhm nominal
Wpdn20K	Weak Pull-down Impedance 20K	10	30	kOhm	20 kOhm nominal
Vhys (3.3)	RX Hysteresis (3.3)	125		mV	
Vhys (1.8)	RX hysteresis (1.8)	116		mV	
Cin	Pad Capacitance		9	pF	

5.6.16 Platform Clock

5.6.16.1 Platform Clock DC Specification

Table 5-38. Platform Clock GPIO

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V Nominal
V _{IH}	Input High Voltage	1.17		V	@1.80V nominal (0.65*V _{CC})
V _{IL}	Input Low Voltage		0.63	V	@1.80V nominal (0.35*V _{CC})
V _{OH}	Output High Voltage	1.35		V	@1.80V nominal (V _{CC} - 0.45), @ 1.5mA load.
V _{OL}	Output Low Voltage		0.45	V	@ -1.5mA load
IPAD	Pad Leakage Current	-5	5	μA	
ZUP	Driver Pull-up Impedance	40	60	Ohm	50 Ohm nominal
ZDN	Driver Pull-down Impedance	40	60	Ohm	50 Ohm nominal
W _{pup20K}	Weak Pull-up Impedance 20K	8	50	kOhm	20 kOhm nominal
W _{pdn20K}	Weak Pull-down Impedance 20K	8	50	kOhm	20 kOhm nominal
V _{hys}	RX hysteresis	100		mV	
Cin	Pad Capacitance		5	pF	



5.6.17 PCIe* Specification

5.6.17.1 PCIe* DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VCC	I/O Voltage	1.66	1.89	V	
VIH	Input High Voltage	1.22		V	
VIL	Input Low Voltage		0.581	V	
VTXDIFF	Differential TX Peak to Peak	800	1200	mV	
VTXDIFF-LP	Differential TX Peak to Peak (Low power mode)	400	1200	mV	
VRXDIFF	Differential RX Peak to Peak	175	1200	mV	
VRXDIFF-LP	Differential RX Peak to Peak (Low power mode)	100	1200	mV	
PCIE_CLKOUT	PCIE_CLKOUT peak to peak voltage		1.05	V	

5.6.18 SATA Specification

Table 5-39. General Specifications

Parameters	Limit	Gen1	Gen2	Units
Channel Speed	Nom	1.5	3.0	Gbps
Fbaud	Nom	1.5	3.0	GHz
FER, Frame Error Rate	Max	8.2e-8 at 95 % confidence level	8.2e-8 at 95 % confidence level	
TUI, Unit Interval	Min	666.433 3	333.216 7	Ps
	Nom	666.666 7	333.333 3	
	Max	670.233 3	335.116 7	
ftol, Tx Frequency Long Term Accuracy	Min	-350	-350	ppm of Fbaud
	Max	+350	+350	
fSSC, Spread-Spectrum Modulation Frequency	Min	30	30	kHz
	Max	33	33	

**Table 5-39. General Specifications**

Parameters	Limit	Gen1	Gen2	Units
SSCtol, Spread-Spectrum Modulation Deviation	Min	-5 350	-5 350	ppm of Fbaud
	Max	+350	+350	
SSCtol, Spread-Spectrum Modulation Rate	Max	1 250	1 250	ppm/us
Vcm,ac coupled, AC Coupled Common Mode Voltage	Min	0	-	mV
	Max	2 000	-	
Zdiff, Nominal Differential Impedance	Nom	100	-	Ohm
Cac coupling AC Coupling Capacitance	Max	12	12	nF
tsettle,cm, Common Mode Transient Settle Time	Max	10	-	ns
Vtrans, Sequencing Transient Voltage	Min	-2.0	-2.0	V
	Max	2.0	2.0	

Table 5-40. Transmitted Signal Requirements

Parameter	Units	Limit	Gen1i	Gen2i
VdiffTxdevice, Tx Differential Device Output Voltage	mVppd	Min	400	400
		Min	-	-
		Nom	500	-
		Max	600	700
		Max	-	-

Table 5-40. Transmitted Signal Requirements

VdiffTxhost, Tx Differential Host Output Voltage	mVppd	Min	400	400
		Min	-	-
		Nom	500	-
		Max	600	700
		Max	-	-
UIVminTx, Tx Minimum Voltage Measurement Interval	UI		0.45 to 0.55	0.45 to 0.55
			-	-
t20-80Tx, Tx Rise/Fall Time	ps (UI)	Min 20 % to 80 %	50 (0.075)	50 (0.15)
		Max 20 % to 80 %	273 (0.41)	136 (0.41)
tskewTx, Tx Differential Skew	ps	Max	20	20

5.6.19 SMBus Specification

5.6.19.1 SMBus DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
VCC (3.3)	I/O Voltage (3.3)	3.05	3.45	V	3.3V Nominal
VCC(1.8)	I/O Voltage (1.8)	1.66	1.89	V	1.8V nominal
VIH (3.3)	Input High voltage (3.3)	1.442		V	
VIL (3.3)	Input Low Voltage (3.3)		0.771	V	
VIH (1.8)	Input High Voltage (1.8)	1.26		V	
VIL (1.8)	Input Low Voltage (1.8)		0.609	V	
VOH (3.3)	Output High Voltage (3.3)	2.85		V	@3.3V nominal (Vcc-0.45), @3mA load
VOL (3.3)	Output Low Voltage (3.3)		0.45	V	@ -3mA load
VOH (1.8)	Output High Voltage (1.8)	1.62		V	@1.80V(Vcc- 0.18), @ 3mA load
VOL (1.8)	Output Low Voltage (1.8)		0.18	V	@ -3mA load.
IPAD	Pad Leakage Current	-11	32	uA	
ZUP	Driver Pull-up Impedance	40	60	Ohm	50 Ohm nominal
ZDN	Driver Pull-down Impedance	40	60	Ohm	50 Ohm nominal
Wpup20K	Weak Pull-up Impedance 20K	10	30	kOhm	20 kOhm nominal



Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
Wpdn20K	Weak Pull-down Impedance 20K	10	30	kOhm	20 kOhm nominal
Vhys (3.3)	RX Hysteresis (3.3)	125		mV	
Vhys(1.8)	RX hysteresis(1.8)	116		mV	
Cin	Pad Capacitance		9	pF	

5.6.20 PMU (Power Management Signals) / GPIO 3.3V

5.6.20.1 PMU DC Specification

Table 5-41. PMU Signals DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VCC (3.3)	I/O Voltage (3.3)	3.05	3.45	V	3.3V nominal
VCC(1.8)	I/O Voltage (1.8)	1.66	1.89	V	1.8V nominal
VIH (3.3)	Input high Voltage (3.3)	1.442		V	
VIL (3.3)	Input Low Voltage (3.3)		0.771	V	
VIH (1.8)	Input High Voltage (1.8)	1.251		V	
VIL (1.8)	Input Low Voltage (1.8)		0.609	V	
VOH (3.3)	Output High Voltage (3.3)	2.85		V	@3.3V nominal (Vcc-0.45), @3mA load
VOL (3.3)	Output Low Voltage (3.3)		0.45	V	@ -3mA load
VOH (1.8)	Output High Voltage (1.8)	1.62	1.8	V	@1.80V nominal (Vcc- 0.18), @ 3mA load.
VOL (1.8)	Output Low Voltage (1.8)		0.18	V	@ -3mA load.
IPAD	Pad Leakage Current	-11	32	μA	
ZUP	Driver Pull-up Impedance	40	60	Ohm	50 Ohm nominal
ZDN	Driver Pull-down Impedance	40	60	Ohm	50 Ohm nominal
Wpup20K	Weak Pull-up Impedance 20K	10	30	kOhm	20 kOhm nominal
Wpdn20K	Weak Pull-down Impedance 20K	10	30	kOhm	20 kOhm nominal
Vhys (3.3)	RX Hysteresis (3.3)	125		mV	
Vhys (1.8)	RX hysteresis (1.8)	116		mV	
Cin	Pad Capacitance		9	pF	

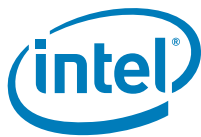
5.6.21 ISH GPIO / PROCHOT_N / PCIe Wake / PCIe CLKREQ / GPIO / THERMTRIP_N Specification

Table 5-42. DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VCC	I/O Voltage	1.66	1.89	V	1.8V nominal
VIH	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
VIL	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
VOH	Output High Voltage	1.35		V	@1.80V nominal (Vcc- 0.45), @ 1.5mA load.
VOL	Output Low Voltage		0.45	V	@ -1.5mA load.
IPAD	Pad Leakage Current	-5	5	uA	
ZUP	Driver Pull-up Impedance [PROCHOT_N]	160	240	Ohm	200 Ohm nominal

**Table 5-42. DC Specification**

Symbol	Parameter	Minimum	Maximum	Units	Notes/Figure
ZDN	Driver Pull-down Impedance [PROCHOT_N]	160	240	Ohm	200 Ohm nominal
ZUP	Driver Pull-up Impedance [ISH GPIO/PCIe WAKE/PCIe CLKREQ/GPIO]	40	60	Ohm	50 Ohm nominal
ZDN	Driver Pull-down Impedance [ISH GPIO/PCIe WAKE/PCIe CLKREQ/GPIO]	40	60	Ohm	50 Ohm nominal
Wpup20K	Weak Pull-up Impedance 20K	8	50	kOhm	20 kOhm nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	50	kOhm	20 kOhm nominal
Vhys	RX hysteresis	100		mV	
Cin	Pad Capacitance		5	pF	



5.6.22 RTC Signal Specification

5.6.22.1 RTC Specification

Table 5-43. RTC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VCC	I/O Voltage	2	3.47	V	3.3V nominal
VIH	Input High Voltage	2		V	@3.3V nominal (0.65*Vcc)
VIL	Input Low Voltage		0.78	V	@3.3V nominal (0.35*Vcc)

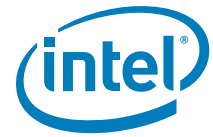
5.6.23 PWM Signal Specification

5.6.23.1 PWM DC Specification

Table 5-44. PWM DC Specification

Symbol	Parameter	Minimum	Maximum	Units	Notes / Figure
VCC	I/O Voltage	1.66	1.89	V	1.80V nominal
VIH	Input High Voltage	1.17		V	@1.80V nominal (0.65*Vcc)
VIL	Input Low Voltage		0.63	V	@1.80V nominal (0.35*Vcc)
VOH	Output High Voltage	1.35		V	@1.80V nominal (Vcc-0.45), @ 1.5mA load.
VOL	Output Low Voltage		0.45	V	@ -1.5mA load.
IPAD	Pad Leakage Current	-5	5	uA	
ZUP	Driver Pull-up Impedance	160	240	Ohm	200 Ohm nominal
ZDN	Driver Pull-down Impedance	160	240	Ohm	200 Ohm nominal
Wpup20K	Weak Pull-up Impedance 20K	8	50	kOhm	20 kOhm nominal
Wpdn20K	Weak Pull-down Impedance 20K	8	50	kOhm	20 kOhm nominal
Vhys	RX hysteresis	100		mV	
Cin	Pad Capacitance		5	pF	

§ §



6 Ball Map and SoC Pin Locations

6.1 SoC Ball Map - DDR3L



	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42
BJ		RSD	RSD	VSS		NCTF		VSS		VSS		MEM_CH 0_MAS		VSS		MEM_CH 0_BAO		VSS		MEM_CH 0_DQ40		MEM_CH 0_DQ35
BH	VSS	VSS	MEM_CH 0_CK0	MEM_CH 0_CK0E		NCTF		MEM_CH 0_BA2		MEM_CH 0_MA11		MEM_CH 0_MA9		MEM_CH 0_MA2		MEM_CH 0_MA10		MEM_CH 0_CAI_N		MEM_CH 0_DQ46		VSS
BG	RSD	MEM_CH 0_DQ3						MEM_CH 0_MA15	MEM_CH 0_MA14	MEM_CH 0_MA12	MEM_CH 0_MA6	MEM_CH 0_MA3	MEM_CH 0_MA1	MEM_CH 0_MA0	MEM_CH 0_MA5	MEM_CH 0_MA6	MEM_CH 0_MA13	VSS	MEM_CH 0_DQ45		MEM_CH 0_DQ44	
BF			VSS			MEM_CH 0_DQ18	MEM_CH 0_DQ26															
BE	VSS	MEM_CH 0_DQ2						MEM_CH 0_DQ24		VSS		VSS		MEM_CH 0_DQ27		VSS	VSS		MEM_CH 0_CLK0_N			VSS
BD	MEM_C H0_DQ4	MEM_CH 0_DQ7	VSS			MEM_CH 0_DQ18	MEM_CH 0_DQ23		VSS		MEM_CH 0_DQ25		MEM_CH 0_DQ31_2		MEM_CH 0_DQ28		MEM_CH 0_CLK1_N	MEM_CH 0_DQ38		MEM_CH 0_CLK0_P		MEM_CH 0_CB6
BC		MEM_CH 0_DQ10_N																				
BB	MEM_C H0_DQ1		VSS			MEM_CH 0_DQ11_P	MEM_CH 0_DQ17			MEM_CH 0_DQ35		MEM_CH 0_DQ31_N		MEM_CH 0_DQ29		MEM_CH 0_CLK1_P	MEM_CH 0_DQ39		VSS			MEM_CH 0_CB2
BA	VSS	VSS										VSS		MEM_CH 0_DQ30		VSS	VSS		MEM_CH 0_CB3			VSS
AY		MEM_CH 0_DQ0				MEM_CH 0_DQ15	VSS	MEM_CH 0_DQ16		MEM_CH 0_DQ21	VSS											
AW	MEM_C H0_DQ6	MEM_CH 0_DQ8												VSS		MEM_CH 0_CB0	MEM_CH 0_CB1			MEM_CH 0_CB3		MEM_CH 0_DQ70
AV		VSS	VSS			MEM_CH 0_DQ8	MEM_CH 0_DQ11	MEM_CH 0_DQ12		VSS	MEM_CH 0_DQ20		MEM_CH 0_DQ22		VDDQ		MEM_CH 0_CB4	MEM_CH 0_CB5		VSS		VSS
AU	MEM_C H0_DQ0	MEM_CH 0_DQ26																				
AT		VSS	VSS			MEM_CH 0_DQ11_P	MEM_CH 0_DQ11_N	VSS		MEM_CH 0_DQ23	MEM_CH 0_DQ14		VSS	VDDQ			VSS	VDDQ		VSS		NCTF
AR	LPSS_I2C 0_SCL	LPSS_I2C 0_SDA											LPSS_I2C 0_SDA	LPSS_I2C 0_SCL				VDDQ		VSS		MEM_CH 0_CLK0_N
AP			LPSS_I2C 0_SCL			LPSS_I2C 0_SDA	LPSS_I2C 0_SCL	NCTF		VSS	LPSS_I2C 0_SCL		LPSS_I2C 0_SDA	LPSS_I2C 0_SCL		LPSS_I2C 0_SDA						
AN	VSS	LPSS_I2C 0_SDA				VSS		VSS	VSS		VSS	VSS		VSS	VSS		VSS	VSS	VDDQ		VDDQ	VDDQ
AM		LPSS_I2C 0_SDA	LPSS_I2C 0_SCL			NCTF	NCTF	ISH_GPIO 0_A		ISH_GPIO 0_T	ISH_GPIO 0_3	ISH_GPIO 0_6	ISH_GPIO 0_4		ISH_GPIO 0_5	ISH_GPIO 0_0		VSS		VNN_SVI 0		VCCIOA
AL	LPSS_I2C 0_SDA																					
AK		PMU_CLK 0_FQZ0_N	LPSS_I2C 0_SCL			VSS	ISH_GPIO 0_9	ISH_GPIO 0_3		PMU_PW 0_RTN_N	PMU_SLP 0_14_N		VSS	ISH_GPIO 0_2		PMU_CLK 0_FQZ0_N	VSS		VNN_SVI 0		VNN_SVI 0	VNN_SVI 0
AJ	VSS	PMU_CLK 0_FQZ0_N												VSS	PMU_CLK 0_FQZ0_N				VNN_SVI 0		RSD	VNN_SVI 0
AH		PMU_CLK 0_FQZ0_N	PMU_CLK 0_FQZ0_N			VSS	VSS	VSS		VSS	VSS		VSS	PMU_CLK 0_FQZ0_N		RTC_TEST 0_N	VSS					
AG	PMU_CLK 0_FQZ0_N	PMU_CLK 0_FQZ0_N	PMU_CLK 0_FQZ0_N			PMU_CLK 0_FQZ0_N	SUS_STA 0_T_N	PMU_CLK 0_FQZ0_N		RSD			RSD	VCC_RTC 0_EXTAP		SDC_PW 0_R0A	VNN_SE 0_N0E		VSS		VSS	VSS
AF		PMU_CLK 0_FQZ0_N																				
AE	VSS	PMU_CLK 0_FQZ0_N				SDC_CLK 0_OUT_3	VSS	VSS	VSS													

Figure 6-2. Ball Map DDR3L—Center (41–20)

	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	
BJ	MEM_CH 6_DQ43			MEM_CH 6_DQ46		VSS		MEM_CH 6_DQ43		VSS		MEM_CH 1_DQ1		VSS		MEM_CH 1_DQ1		MEM_CH 1_DQ18		MEM_CH 1_DQ12		MEM_CH 1_DQ17	
BH	MEM_C 6_DQ47		VSS		MEM_CH 6_DQ46		MEM_CH 6_DQ47		MEM_CH 6_DQ48		MEM_CH 1_DQ2		MEM_CH 1_DQ10		MEM_CH 1_DQ4		VSS		MEM_CH 1_DQ18		VSS		
BG	VSS	MEM_CH 6_DQ42	MEM_CH 6_DQ41	MEM_CH 6_DQ40	MEM_CH 6_DQ42	MEM_CH 6_DQ37	VSS	MEM_CH 6_DQ37	MEM_CH 6_DQ38	VSS	MEM_CH 1_DQ3	MEM_CH 1_DQ1	VSS	MEM_CH 1_DQ15	MEM_CH 1_DQ5	MEM_CH 1_DQ8	MEM_CH 1_DQ23	MEM_CH 1_DQ16	VSS	MEM_CH 1_DQ12	MEM_CH 1_DQ21	MEM_CH 1_DQ20	
BF										VSS													
BE	MEM_C 6_DQ43		MEM_CH 6_DQ43		VSS		VSS	MEM_CH 6_DQ48				MEM_CH 1_DQ10	VSS		VSS		MEM_CH 1_DQ12		NCTF		VSS		
BD	MEM_C 6_DQ43		MEM_CH 6_DQ44		MEM_CH 6_DQ38		MEM_CH 6_DQ38	MEM_CH 6_DQ38	MEM_CH 6_DQ38		VSS		MEM_CH 1_DQ11	MEM_CH 1_DQ11		MEM_CH 1_DQ15	MEM_CH 1_DQ14		NCTF		MEM_CH 1_DQ11		
BC										VSS													
BB	NCTF		VSS		MEM_CH 6_DQ42		MEM_CH 6_DQ39	MEM_CH 6_DQ35				MEM_CH 1_DQ9	MEM_CH 1_DQ13		MEM_CH 1_DQ13		VSS		MEM_CH 1_C87		MEM_CH 1_C141		
BA	MEM_C 6_DQ41		VSS		VSS		VSS	MEM_CH 6_DQ48		VSS		MEM_CH 1_DQ8	VSS		VSS		VSS		MEM_CH 1_C88		VSS		
AY										VSS													
AW	MEM_C 6_DQ41		MEM_CH 6_DQ44		MEM_CH 6_DQ34		MEM_CH 6_DQ39	VSS				VSS	MEM_CH 1_DQ25		MEM_CH 1_DQ31		MEM_CH 1_DQ13		MEM_CH 1_C82		MEM_CH 1_C83		
AV	VSS		MEM_CH 6_DQ44		MEM_CH 6_DQ38		VSS	MEM_CH 6_DQ38		VSS		MEM_CH 1_DQ38	VSS		MEM_CH 1_DQ28		MEM_CH 1_DQ13		VSS		VSS		
AU										VSS													
AT	MEM_C 6_DQ43		VSS		MEM_CH 6_DQ38		VSS	MEM_CH 6_VREF0				MEM_CH 1_VREF0	VSS		MEM_CH 1_DQ24		VSS		MEM_CH 1_DQ27		MEM_CH 1_C81		
AR	MEM_C 6_DQ43		MEM_CH 6_DQ32		MEM_CH 6_DQ38		MEM_CH 6_DQ38	MEM_CH 6_VREF0	MEM_CH 6_VREF0		VSS	MEM_CH 1_VREF0	MEM_CH 1_VREF0		MEM_CH 1_DQ28		MEM_CH 1_DQ28		MEM_CH 1_DQ28		MEM_CH 1_C88		
AP																							
AN	VDDQ		VSS		VSS	VSS		VSS		RSVD		VSS		VSS	VSS		VSS		VDDQ	VDDQ		VDDQ	
AM	VCCDIA		VSS		VDD2_IP 24_GLM		VSS			RSVD		VCC_VCB 1	VDD2_IP 24_GLM	VSS		VCCDIA		VCCDIA	VSS		VDD2_IP 24_GLM		
AL																							
AK	VNN_SV 0		VNN_SV 0		VNN_SV 0	VSS	VCC_VCB 1		VCC_VCB 1		VCC_VCB 1	VCC_VCB 1	VSS		VCC_VCB 1		VCC_VCB 1		VSS		VDD2_IP 24_GLM		
AJ	VNN_SV 0		VNN_SV 0		VNN_SV 0	VSS		VSS		VCC_VCB 1		VCC_VCB 1	VSS		VCC_VCB 1		VCC_VCB 1		VSS		VDD2_IP 24_GLM		
AH																							
AG	VSS		VSS		VSS	VCC_VCB 1		VSS		VCC_VCB 1		VCC_VCB 1	VSS		VCC_VCB 1		VCC_VCB 1		VSS	VDD2_IP 24_MPHY		VDD2_IP 24_USB2	
AF																							
AE	VSS		VSS		VCC_VCB VCC_VCB 1		VSS		VCC_VCB 1		VCC_VCB 1	VCC_VCB 1	VSS		VCC_VCB 1		VCCRAM 1P05		VSS	VDD2_IP 24_MPHY		VDD2_IP 24_MPHY	
AD																							
AC	VCC3P 3V_A		VSS		VCC_VCB VCC_VCB 1		VSS		VCC_VCB 1		VCC_VCB 1	VCC_VCB 1	VSS		VCC_VCB 1		VCCRAM 1P05		VCCRAM 1P05	RSVD		RSVD	
AB																							
AA	VSS		VCC_VCB 1		VCC_VCB VCC_VCB 1		VSS		VCC_VCB 1		VCC_VCB 1	VCC_VCB 1	VSS		VCC_VCB 1		VCCRAM 1P05		VCCRAM 1P05	VCCRAM 1P05		VDD2_IP 24_GLM	
Y	VCC_VCB 1		VCC_VCB 1		VCC_VCB VCC_VCB 1		VSS		VCC_VCB 1		VCC_VCB 1	VCC_VCB 1	VSS		VCC_VCB 1		VCCRAM 1P05		VCCRAM 1P05	VSS		VCCRAM 1P05	
W																							
V	VCC_VCB 1		VCC_VCB 1		VCC_VCB VCC_VCB 1		VSS		VCC_VCB 1		VCC_VCB 1	VCC_VCB 1	VSS		VCC_VCB 1		VCCRAM 1P05		VCCRAM 1P05	VCCRAM 1P05		VSS	
U	VCC_VCB 1		VCC_VCB 1		VCC_VCB VCC_VCB 1		VSS		VCC_VCB 1		VCC_VCB 1	VCC_VCB 1	VSS		VCC_VCB 1		VCCRAM 1P05		VCCRAM 1P05	VCCRAM 1P05		VCCRAM 1P05	
T	VCC_VCB 1		VCC_VCB 1		VCC_VCB VCC_VCB 1		VSS		VCC_VCB 1		VCC_VCB 1	VCC_VCB 1	VSS		VCC_VCB 1		VCCRAM 1P05		VCCRAM 1P05	VCCRAM 1P05		VCCRAM 1P05	
R	VCC_VCB 1		VCC_VCB 1		VCC_VCB VCC_VCB 1		VSS		VCC_VCB 1		VCC_VCB 1	VCC_VCB 1	VSS		VCC_VCB 1		VCCRAM 1P05		VCCRAM 1P05	VCCRAM 1P05		VCCRAM 1P05	
P	VSS		NCTF		VSS		VSS	GP_CAM ERASB1		VSS		GPIO_21 6	DISCUT		NCTF		NCTF		VSS		MEM_CH 1_DQ11		
N	VSS		NCTF		VSS		VSS	GP_CAM ERASB1		VSS		GPIO_21 8	DISCUT		NCTF		NCTF		VSS		MEM_CH 1_DQ11		
M	VSS		NCTF		VSS		VSS	GP_CAM ERASB1		VSS		GPIO_21 7	DISCUT		NCTF		NCTF		VSS		MEM_CH 1_DQ11		
L	VSS		NCTF		VSS		VSS	GP_CAM ERASB1		VSS		GPIO_21 7	DISCUT		NCTF		NCTF		VSS		MEM_CH 1_DQ11		
K	VSS		NCTF		VSS		VSS	GP_CAM ERASB1		VSS		GPIO_21 7	DISCUT		NCTF		NCTF		VSS		MEM_CH 1_DQ11		
J	VSS		NCTF		VSS		VSS	GP_CAM ERASB1		VSS		GPIO_21 7	DISCUT		NCTF		NCTF		VSS		MEM_CH 1_DQ11		
H	VSS		NCTF		VSS		VSS	GP_CAM ERASB1		VSS		GPIO_21 7	DISCUT		NCTF		NCTF		VSS		MEM_CH 1_DQ11		
G	VSS		NCTF		VSS		VSS	GP_CAM ERASB1		VSS		GPIO_21 7	DISCUT		NCTF		NCTF		VSS		MEM_CH 1_DQ11		
F	VSS		NCTF		VSS		VSS	GP_CAM ERASB1		VSS		GPIO_21 7	DISCUT		NCTF		NCTF		VSS		MEM_CH 1_DQ11		
E	VSS		NCTF		VSS		VSS	GP_CAM ERASB1		VSS		GPIO_21 7	DISCUT		NCTF		NCTF		VSS		MEM_CH 1_DQ11		
D	VSS		NCTF		VSS		VSS	GP_CAM ERASB1		VSS		GPIO_21 7	DISCUT		NCTF		NCTF		VSS		MEM_CH 1_DQ11		
C	VSS		NCTF		VSS		VSS	GP_CAM ERASB1		VSS		GPIO_21 7	DISCUT		NCTF		NCTF		VSS		MEM_CH 1_DQ11		
B	VSS		NCTF		VSS		VSS	GP_CAM ERASB1		VSS		GPIO_21 7	DISCUT		NCTF		NCTF		VSS		MEM_CH 1_DQ11		
A	VSS		NCTF		VSS		VSS	GP_CAM ERASB1		VSS		GPIO_21 7	DISCUT		NCTF		NCTF		VSS		MEM_CH 1_DQ11		

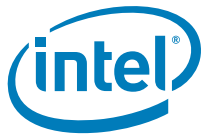


Figure 6-3. Ball Map DDR3L—Right (19–1)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
BJ	MEM_C H1_DQ2	VSS	NCTF		MEM_CH 1_MA2	MEM_CH 1_MA11	MEM_CH 1_MA9	MEM_CH 1_MA2	MEM_CH 1_MA2	MEM_CH 1_MA2	MEM_CH 1_MA2	MEM_CH 1_MA2	MEM_CH 1_MA2	MEM_CH 1_MA2	MEM_CH 1_MA2	VSS	RSVD	NCTF	
BH	MEM_CH 1_CK0	MEM_CH 1_CK0	MEM_CH 1_MA15	MEM_CH 1_MA14	MEM_CH 1_MA7	MEM_CH 1_MA12	MEM_CH 1_MA8	MEM_CH 1_MA5	MEM_CH 1_MA1	MEM_CH 1_MA0	MEM_CH 1_MA1	MEM_CH 1_MA10	MEM_CH 1_MA10	MEM_CH 1_MA10	MEM_CH 1_MA10	MEM_CH 1_MA10	MEM_CH 1_MA10	MEM_CH 1_MA10	MEM_CH 1_MA10
BG	VSS	MEM_CH 1_CK0	MEM_CH 1_CK0	MEM_CH 1_MA15	MEM_CH 1_MA14	MEM_CH 1_MA7	MEM_CH 1_MA12	MEM_CH 1_MA8	MEM_CH 1_MA5	MEM_CH 1_MA1	MEM_CH 1_MA0	MEM_CH 1_MA1	MEM_CH 1_MA10	MEM_CH 1_MA10	MEM_CH 1_MA10	MEM_CH 1_MA10	MEM_CH 1_MA10	MEM_CH 1_MA10	MEM_CH 1_MA10
BF	MEM_C H1_CLK0																		
BE	MEM_C H1_CLK0																		
BD	MEM_C H1_CLK0																		
BC	MEM_C H1_CLK0																		
BB	VSS	NCTF	MEM_CH 1_MA4		MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37
BA	MEM_C H1_CLK0																		
AY	MEM_C H1_CLK0																		
AW	MEM_C H1_CLK0																		
AV	VSS	NCTF	MEM_CH 1_DQ37		VDDQ	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37
AU																			
AT	VSS	VDDQ	VSS		VDDQ	VSS	VDDQ	VSS	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37	MEM_CH 1_DQ37
AR	VSS	VDDQ																	
AP																			
AN	VDDQ	VSS	VSS		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AM	VSS																		
AL																			
AK	VSS																		
AJ	VSS																		
AH																			
AG	VSS																		
AF																			
AE	VDDQ	VSS	VSS		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AD																			
AC	VSS																		
AB																			
AA	VDDQ	VSS	VSS		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
Y	VDDQ	VSS	VSS		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
W																			
V	VDDQ	VSS	VSS		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
U	VSS	VSS	VSS		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
T																			
R	NCTF																		
P	VSS																		
N																			
M	MEM_C H1_CLK0																		
L	MEM_C H1_CLK0																		
K																			
J	VSS																		
H	MEM_C H1_CLK0																		
G																			
F	MEM_C H1_CLK0																		
E	VSS																		
D																			
C	RSVD																		
B	RSVD																		
A	RSVD																		



6.2 SoC Ball Map—LPDDR3

Figure 6-4. Ball Map LPDDR3—Left (63–42)

	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42
BJ		RSVD	RSVD	VSS		MEM_CH 0_CKE15	VSS		VSS		MEM_CH 0_CAA2	VSS		MEM_CH 0_CAB2	VSS	MEM_CH 0_CAB2	VSS		MEM_CH 0_DQ06		MEM_CH 0_DQ06	
BH	VSS	VSS	MEM_CH 0_CKE16	MEM_CH 0_CKE16		MEM_CH 0_CKE16	MEM_CH 0_CAA7		MEM_CH 0_CAB6		MEM_CH 0_CAB1		MEM_CH 0_CAB1		MEM_CH 0_CAB6		MEM_CH 0_CAB2		MEM_CH 0_DQ014		VSS	
BG	RSVD	MEM_CH 0_DQ043					MEM_CH 0_CAA8		MEM_CH 0_CAB8		MEM_CH 0_CAB8		MEM_CH 0_CAB8		MEM_CH 0_CAB8		MEM_CH 0_CAB8		MEM_CH 0_CAB8	VSS	MEM_CH 0_DQ013	MEM_CH 0_DQ013
BF		VSS			MEM_CH 0_DQ019	MEM_CH 0_DQ019																
BE	VSS	MEM_CH 0_DQ042					MEM_CH 0_DQ042		VSS		VSS		MEM_CH 0_DQ042		VSS	VSS			MEM_CH 0_CKE15		VSS	
BD	MEM_CH 0_DQ047	VSS			MEM_CH 0_DQ018	MEM_CH 0_DQ018		VSS		MEM_CH 0_DQ018		MEM_CH 0_DQ018		MEM_CH 0_DQ018		MEM_CH 0_CKE15	NCTF			MEM_CH 0_CKE15		NCTF
BC	MEM_CH 0_DQ043																					
BB	MEM_CH 0_DQ047	VSS			MEM_CH 0_DQ018	MEM_CH 0_DQ018		MEM_CH 0_DQ018		MEM_CH 0_DQ018		MEM_CH 0_DQ018		MEM_CH 0_DQ018		MEM_CH 0_CKE15	NCTF		VSS		NCTF	
BA	VSS	VSS																				
AY	MEM_CH 0_DQ045	MEM_CH 0_DQ045			MEM_CH 0_DQ018	VSS	MEM_CH 0_DQ018		MEM_CH 0_DQ018	VSS												
AW	MEM_CH 0_DQ045	VSS																				
AV	VSS	VSS			MEM_CH 0_DQ048	MEM_CH 0_DQ048		VSS	MEM_CH 0_DQ048		MEM_CH 0_DQ048		VSS		VDDQ		NCTF	NCTF		VSS		VSS
AU	MEM_CH 0_DQ048	MEM_CH 0_DQ048																				
AT	VSS	VSS			MEM_CH 0_DQ041	MEM_CH 0_DQ041		VSS		MEM_CH 0_DQ041		VSS	VDDQ						VSS	VDDQ		MEM_CH 0_CKE15
AR	LPSS_I2C 0_SDA	LPSS_I2C 0_SDA																	VSS			
AP	LPSS_I2C 0_SDA	LPSS_I2C 0_SDA			LPSS_I2C 0_SDA	LPSS_I2C 0_SDA		VSS		LPSS_I2C 0_SDA		LPSS_I2C 0_SDA	LPSS_I2C 0_SDA	LPSS_I2C 0_SDA	LPSS_I2C 0_SDA				VSS		VDDQ	VDDQ
AN	VSS	LPSS_I2C 0_SDA			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQ		VDDQ	VDDQ
AM	LPSS_I2C 0_SDA	LPSS_I2C 0_SDA			NCTF	NCTF	SH_SPI 0_SDA		SH_SPI 0_SDA		SH_SPI 0_SDA		SH_SPI 0_SDA		SH_SPI 0_SDA		SH_SPI 0_SDA		VSS		VSS	VSS
AL	LPSS_I2C 0_SDA	LPSS_I2C 0_SDA																				
AK	SH_SPI 0_SDA	LPSS_I2C 0_SDA			VSS	SH_SPI 0_SDA																
AJ	VSS	SH_SPI 0_SDA																				
AH	SH_SPI 0_SDA	SH_SPI 0_SDA			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AG	SH_SPI 0_SDA	SH_SPI 0_SDA			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AF	SH_SPI 0_SDA	SH_SPI 0_SDA			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AE	VSS	PMU_SW 0_SDA			VSS		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AD	PMU_SW 0_SDA	PMU_SW 0_SDA																				
AC	SUSPWR 0_SDA	PMU_SW 0_SDA			RTC_X1	RTC_X2		RSM_RST_N	RTC_RST_N	INTRUDE_P_N		SDCARD_CMD	SDCARD_CMD	SDCARD_CMD	SDCARD_CMD	SDCARD_CMD	SDCARD_CMD	SDCARD_CMD	VCC_3P3	VCC_3P3	VCC_3P3	VCC_3P3
AB	LPC_SERI 0_SDA	LPC_CLK 0_SDA			VSS	SDCARD_CMD		SDCARD_CMD	SDCARD_CMD	SDCARD_CMD		VSS	SDCARD_CMD	SDCARD_CMD	SDCARD_CMD	SDCARD_CMD	SDCARD_CMD	SDCARD_CMD	VCC_3P3	VCC_3P3	VCC_3P3	VCC_3P3
AA	VSS	LPC_CLK 0_SDA																				
Y	LPC_AD3	LPC_AD2			VSS	EMMC_C 0_SDA	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
W	LPC_AD3	LPC_AD2																				
V	LPC_CLK 0_SDA	LPC_CLK 0_SDA			EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	VCC_3P3	VCC_3P3	VCC_3P3	VSS
U	VSS	VSS			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
T	EMMC_C 0_SDA	EMMC_C 0_SDA			EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	VCC_3P3	VCC_3P3	VCC_3P3	VSS
R	EMMC_C 0_SDA	EMMC_C 0_SDA																				
P	EMMC_C 0_SDA	EMMC_C 0_SDA			VSS	SDIO_CLK		VSS	SDIO_CLK		VSS	SDIO_CLK		VSS	SDIO_CLK		VSS	SDIO_CLK	VCC_VDD	VCC_VDD	VCC_VDD	VCC_VDD
N	VSS	EMMC_C 0_SDA																				
M	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA			VSS	AVS_I2S3 0_SDA		AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA
L	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA																				
K	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA			AVS_I2S3 0_SDA	AVS_I2S3 0_SDA		AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA
J	VSS	AVS_I2S3 0_SDA																				
H	AVS_I2S3 0_SDA	VSS			AVS_I2S3 0_SDA	AVS_I2S3 0_SDA		AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA
G	AVS_I2S3 0_SDA	VSS																				
F	VSS	AVS_I2S3 0_SDA			VSS	AVS_I2S3 0_SDA		VSS	AVS_I2S3 0_SDA		VSS	AVS_I2S3 0_SDA		VSS	AVS_I2S3 0_SDA		VSS	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA	AVS_I2S3 0_SDA
E	NCTF	AVS_I2S3 0_SDA																				
D	NCTF	AVS_I2S3 0_SDA																				
C	NCTF	AVS_I2S3 0_SDA																				
B	VSS	AVS_I2S3 0_SDA																				
A	VSS	AVS_I2S3 0_SDA																				

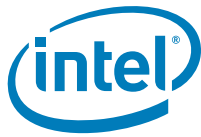


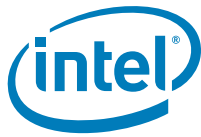
Figure 6-5. Ball Map LPDDR3—Middle (41–20)

	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21
BJ	MEM_CH 0_DQ43		MEM_CH 0_DQ56	VSS		MEM_CH 0_DQ63	VSS		MEM_CH 1_DQ7	VSS		MEM_CH 1_DQ0	VSS		MEM_CH 1_DQ0		MEM_CH 1_DQ18		MEM_CH 1_DQ32		MEM_CH 1_DQ31
BH	MEM_C HD_Q04 7	VSS		MEM_CH 0_DQ43	MEM_CH 0_DQ57	MEM_CH 0_DQ58		MEM_CH 0_DQ58		MEM_CH 1_DQ2	MEM_CH 1_DQ0	MEM_CH 1_DQ0		MEM_CH 1_DQ4	VSS		MEM_CH 1_DQ18		VSS		20
BG	VSS	MEM_CH 0_DQ42	MEM_CH 0_DQ41	MEM_CH 0_DQ40	MEM_CH 0_DQ37	VSS	MEM_CH 0_DQ37	MEM_CH 0_DQ38	VSS	MEM_CH 1_DQ3	MEM_CH 1_DQ1	VSS	MEM_CH 1_DQ35	MEM_CH 1_DQ5	MEM_CH 1_DQ4	MEM_CH 1_DQ23	MEM_CH 1_DQ16	VSS	MEM_CH 1_DQ32	MEM_CH 1_DQ21	MEM_CH 1_DQ20
BF									VSS												
BE	MEM_C HD_M44		MEM_CH 0_DQ49	VSS		VSS	MEM_CH 0_DQ49				MEM_CH 1_DQ10	VSS		VSS		MEM_CH 1_DQ12		NCTF		VSS	
BD	MEM_C HD_M43		MEM_CH 0_DQ56	MEM_CH 0_DQ55	MEM_CH 0_DQ56	MEM_CH 0_DQ56			VSS		MEM_CH 1_DQ31	MEM_CH 1_DQ31		MEM_CH 1_DQ35		MEM_CH 1_DQ14		NCTF		MEM_CH 1_CLK1 N	
BC									VSS												
BB	NCTF	VSS		MEM_CH 0_DQ52	MEM_CH 0_DQ56	MEM_CH 0_DQ55					MEM_CH 1_DQ9	MEM_CH 1_DQ51 N		MEM_CH 1_DQ13	VSS		MEM_CH 1_C87		MEM_CH 1_C87		MEM_CH 1_CLK1 P
BA	MEM_C HD_C11 N	VSS		VSS		VSS	MEM_CH 0_DQ48		VSS		MEM_CH 1_DQ8	VSS		VSS		VSS		MEM_CH 1_C86		VSS	
AY									VSS												
AW	MEM_C HD_Q01 1	MEM_CH 0_DQ44 N		MEM_CH 0_DQ34	MEM_CH 0_DQ35	VSS					VSS	MEM_CH 1_DQ25		MEM_CH 1_DQ31		MEM_CH 1_DQ31		MEM_CH 1_C82		MEM_CH 1_C83	
AV	VSS	MEM_CH 0_DQ54 P		MEM_CH 0_DQ28	VSS	MEM_CH 0_PCOM P			VSS		MEM_CH 1_PCOM P	VSS		MEM_CH 1_DQ28		MEM_CH 1_DQ13 P		VSS		VSS	
AU									VSS												
AT	MEM_C HD_Q03 7	VSS		MEM_CH 0_DQ38	VSS	MEM_CH 0_VREFD Q					MEM_CH 1_VREFD Q	VSS		MEM_CH 1_DQ24		VSS		MEM_CH 1_DQ27		MEM_CH 1_C81	
AR	MEM_C HD_Q03 8	MEM_CH 0_DQ32		MEM_CH 0_DQ38	MEM_CH 0_VREFC A	MEM_CH 0_VREFC N			VSS		MEM_CH 1_VREFC A	MEM_CH 1_VREFC N		MEM_CH 1_DQ28		MEM_CH 1_DQ29		MEM_CH 1_DQ30		MEM_CH 1_C80	
AP																					
AN	VDDQ	VSS		VSS	VSS		VSS		RSVD		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQ	VDDQ	VDDQ	VDDQ
AM	VDDQ	VSS		VDD2_IP 24_GLM	VSS		VSS		RSVD		VCC_VCG I	VDD2_IP 24_GLM	VSS	VCCIOA	VCCIOA	VSS	VCCIOA	VSS	VDD2_IP 24_GLM	VDD2_IP 24_GLM	VDD2_IP 24_GLM
AL																					
AK	VNN_SV ID	VNN_SV D		VNN_SV D	VSS		VCC_VCG I		VCC_VCG I		VCC_VCG I	VCC_VCG I	VSS	VCC_VCG I	VSS	VCC_VCG I	VSS	VDD2_IP 24_AUD SH_PIL	VSS	VDD2_IP 24_AUD SH_PIL	VDD2_IP 24_AUD SH_PIL
AJ	VNN_SV ID	VNN_SV D		VNN_SV D	VSS		VCC_VCG I		VCC_VCG I		VCC_VCG I	VCC_VCG I	VSS	VCC_VCG I	VSS	VCC_VCG I	VSS	VDD2_IP 24_AUD SH_PIL	VSS	VDD2_IP 24_AUD SH_PIL	VDD2_IP 24_AUD SH_PIL
AH																					
AG	VSS	VSS		VSS	VCC_VCG I		VSS		VCC_VCG I		VCC_VCG I	VCC_VCG I	VSS	VCC_VCG I	VSS	VCC_VCG I	VSS	VDD2_IP 24_MPHY	VSS	VDD2_IP 24_MPHY	VDD2_IP 24_MPHY
AF																					
AE	VSS	VSS		VCC_VCG I	VCC_VCG I		VSS		VCC_VCG I		VCC_VCG I	VCC_VCG I	VSS	VCC_VCG I	VSS	VCC_VCG I	VSS	VDD2_IP 24_MPHY	VSS	VDD2_IP 24_MPHY	VDD2_IP 24_MPHY
AD																					
AC	VCC_IP 3V_A	VSS		VCC_VCG I	VCC_VCG I		VSS		VCC_VCG I		VCC_VCG I	VCC_VCG I	VSS	VCC_VCG I	VSS	VCC_VCG I	VSS	VDD2_IP 24_MPHY	VSS	VDD2_IP 24_MPHY	VDD2_IP 24_MPHY
AB																					
AA	VSS	VCC_VCG I		VCC_VCG I	VCC_VCG I		VSS		VCC_VCG I		VCC_VCG I	VCC_VCG I	VSS	VCC_VCG I	VSS	VCC_VCG I	VSS	VDD2_IP 24_MPHY	VSS	VDD2_IP 24_MPHY	VDD2_IP 24_MPHY
Y	VCC_VCG I	VCC_VCG I		VCC_VCG I	VCC_VCG I		VSS		VCC_VCG I		VCC_VCG I	VCC_VCG I	VSS	VCC_VCG I	VSS	VCC_VCG I	VSS	VDD2_IP 24_MPHY	VSS	VDD2_IP 24_MPHY	VDD2_IP 24_MPHY
W																					
V	VCC_VCG I	VCC_VCG I		VCC_VCG I	VCC_VCG I		VSS		VCC_VCG I		VCC_VCG I	VCC_VCG I	VSS	VCC_VCG I	VSS	VCC_VCG I	VSS	VDD2_IP 24_MPHY	VSS	VDD2_IP 24_MPHY	VDD2_IP 24_MPHY
U	VCC_VCG I	VCC_VCG I		VCC_VCG I	VCC_VCG I		VSS		VCC_VCG I		VCC_VCG I	VCC_VCG I	VSS	VCC_VCG I	VSS	VCC_VCG I	VSS	VDD2_IP 24_MPHY	VSS	VDD2_IP 24_MPHY	VDD2_IP 24_MPHY
T																					
R	VCC_VCG I	NCTF		NCTF		GP_CAM ERASB6	GP_CAM ERASB10		VSS		NCTF	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
P	VSS	NCTF		VSS		GP_CAM ERASB1			VSS		GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S
N	LPSS_U ART2_C TS_N	NCTF		GP_CAM ERASB4	GP_CAM ERASB9	GP_CAM ERASB8			VSS		GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S
M	LPSS_U ART2_R TS_N	GPIO_18		GP_CAM ERASB0		VSS	GP_CAM ERASB7		VSS		GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S
K	LPSS_U ART2_R XD	GPIO_18		VSS		VSS	GP_CAM ERASB2		VSS		GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S
J	LPSS_U ART2_T XD	GPIO_18		VSS		VSS	GP_CAM ERASB2		VSS		GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S	GPIO_21 S
H									VSS												
G									VSS												
F	PWM2	GPIO_19		VSS		GPIO_32	GPIO_33		VSS		GPIO_26	GPIO_13	GPIO_27	VSS	GPIO_25	GPIO_21	GPIO_24	GPIO_24	GPIO_24	GPIO_24	GPIO_24
E	PWM3	GPIO_12		VCC_VCG I		VCC_VCG I	GPIO_32		VSS		GPIO_26	GPIO_13	GPIO_27	VSS	GPIO_25	GPIO_21	GPIO_24	GPIO_24	GPIO_24	GPIO_24	GPIO_24
D									VSS												
C	PWM1	VSS		GPIO_2	GPIO_14	GPIO_38	GPIO_16	GPIO_17	GPIO_11	GPIO_19	VSS	GPIO_26	GPIO_13	GPIO_27	VSS	GPIO_25	GPIO_21	GPIO_24	GPIO_24	GPIO_24	GPIO_24
B	PWM0			GPIO_3		GPIO_28		GPIO_4		GPIO_1		GPIO_6		GPIO_8		GPIO_20		GPIO_23		GPIO_23	GPIO_23
A		VSS		GPIO_0		VSS		GPIO_5		VSS		GPIO_9		VSS		GPIO_22		VSS		GPIO_22	GPIO_22



Figure 6-6. Ball Map LPDDR3—Right (19–1)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
BJ		VSS		MEM_CH 1_CKE1B		VSS		MEM_CH 1_CAA0		VSS		VSS		MEM_CH 1_CAB3		VSS	RSVD	NCTF	
BH	MEM_C H1_DQA 22		MEM_CH 1_CKE0B		MEM_CH 1_CAA7		MEM_CH 1_CAA6		MEM_CH 1_CAA4		MEM_CH 1_CAB5		MEM_CH 1_CAB4		MEM_CH 1_CAB2		MEM_CH 1_CAB1	MEM_CH 1_CAB0	VSS
BG	VSS	MEM_CH 1_CKE0A	MEM_CH 1_CKE1A	MEM_CH 1_CAA9	MEM_CH 1_CAA8	MEM_CH 1_CAA3	MEM_CH 1_CAA5	MEM_CH 1_CAA1	MEM_CH 1_CAA2	MEM_CH 1_CAB9	MEM_CH 1_CAB7	MEM_CH 1_CAB8	MEM_CH 1_CAB6					MEM_CH 1_DQB31	NCTF
BF														MEM_CH 1_DQB0	MEM_CH 1_DQB15		VSS		
BE	MEM_C H1_CLK 8_N MEM_C H1_CLK 8_P		VSS	VSS		MEM_CH 1_DQB2		VSS		VSS		MEM_CH 1_DQB7						MEM_CH 1_DQB27	VSS
BD			MEM_CH 1_CS0A_N	NCTF		MEM_CH 1_DQB6		MEM_CH 1_DQS80_N		MEM_CH 1_DQB1		VSS		MEM_CH 1_DQB9	MEM_CH 1_DQB10		VSS	MEM_CH 1_DQB25	MEM_CH 1_DQB26
BC																		MEM_CH 1_DQS83_P	
BB	VSS		MEM_CH 1_CS1A_N	NCTF		MEM_CH 1_DQB5		MEM_CH 1_DQS80_P		MEM_CH 1_DQB3			MEM_CH 1_DQB11	MEM_CH 1_DQS81_N	MEM_CH 1_DQS81_P		VSS		MEM_CH 1_DQS83_N
BA	NCTF		VSS	VSS		MEM_CH 1_DQB4		VSS										VSS	VSS
AY										VSS	MEM_CH 1_DQB13		MEM_CH 1_DQB14	VSS	MEM_CH 1_DQB20		MEM_CH 1_DQB30	MEM_CH 1_DQB24	
AW	NCTF		MEM_CH 1_CS1B_N	MEM_CH 1_ODTA		VSS												MEM_CH 1_DQB29	MEM_CH 1_DQB28
AV	VSS		MEM_CH 1_CS0B_N	MEM_CH 1_ODTB		VDDQ		MEM_CH 1_DQB8		MEM_CH 1_DQB12	VSS		MEM_CH 1_DQB23	MEM_CH 1_DQB22	MEM_CH 1_DQB21		VSS	VSS	
AU																		MEM_CH 1_DQB16	MEM_CH 1_DQB19
AT	VSS		VDDQ	VSS			VDDQ	VSS		MEM_CH 1_DQB17	MEM_CH 1_DQB18		VSS	MEM_CH 1_DQS82_N	MEM_CH 1_DQS82_P		VSS	VSS	
AR	VSS		VDDQ																
AP					MSI_A_ DP_2		MSI_A_ DN_2	MSI_A_ DP_0		MSI_A_ DN_0	VSS		MSI_RC OMP	MSI_A_ DP_3	MSI_A_ DN_3		MSI_A_ CLKN	MSI_A_ DP_1	MSI_A_ DN_1
AN		VDDQ	VSS	VSS		VSS	VSS	MSI_C_ DN_3	VSS	VSS	MSI_C_ DN_2	MSI_C_ CLKP		VSS	VSS	VSS		VSS	VSS
AM		VSS		DDIO_AU XP	DDIO_AU XN		MSI_C_ DN_3	MSI_C_ DP_2		VSS	MSI_C_ DN_2	MSI_C_ CLKP		MSI_C_ CLKN	MSI_C_ DN_1	MSI_C_ DP_1		DDIO_TX P_1	DDIO_TX N_1
AL																		DDIO_TX P_3	DDIO_TX N_3
AK		VSS		DDIO_AU XP	DDIO_AU XN		MSI_C_ DP_3	VSS		VSS	VSS		MSI_C_ DP_0	MSI_C_ DN_0	VSS		DDIO_TX P_0	DDIO_TX N_0	
AJ		VSS																VSS	VSS
AH				VSS	VSS		USB_SSIC 0_TX_P_0_TX_N	USB_SSIC 0_TX_P_0_TX_N		EDP_AUX P	EDP_AUX N		VSS	VSS	VSS		DDIO_TX P_2	DDIO_TX N_2	
AG		VSS		USB_SSIC 0_RX_P_0_RX_N	USB_SSIC 0_RX_P_0_RX_N		VSS	EDP_TXP _1		EDP_TXN _1	EDP_TXN _0		EDP_TXP _0	EDP_RCO MP_P	EDP_RCO MP_N		DDIO_RC OMP_P	DDIO_RC OMP_N	
AF																	DDIO_TX P_0	DDIO_TX N_0	
AE	VDD2_IP 24_MPHY	VSS	VSS			VSS	VSS		VSS	VSS		VSS	VSS		VSS	VSS		VSS	VSS
AD																	DDIO_TX P_1	DDIO_TX N_1	DDIO_TX P_2
AC		VSS		USB2_VB DS_EN0_G_ID	USB2_DT G_ID		NCTF	USB2_DP 6		USB2_DN _3	EDP_TXN _3		EDP_TXP _3	EDP_TXP _2	EDP_TXN _2		DDIO_TX P_3	DDIO_TX N_3	DDIO_TX P_2
AB				VSS	USB_SSIC RCOMP		NCTF	VSS		VSS	VSS		USB2_DN _5	USB2_DP _5	VSS		DDIO_TX P_3	DDIO_TX N_3	VSS
AA	VDD2_IP 24_DSIC _2																	VSS	VSS
Y	VCCRAM IP05_IO		VSS	USB2_RC OMP		USB2_DP 2	VSS		USB2_DN _4	USB2_DP _4			VSS	VSS	VSS		SATA_P0 TXP	SATA_P0 TXN	SATA_P1 USB3_P 5_TXN
W																			
V	VCCRAM IP05_IO		USB2_DP 1	USB2_DN _1		USB2_DN _0	USB2_DP _0		USB2_DN _3	USB2_DP _3			USB2_DN _2	USB2_DP _2	USB2_DP _7		PCIE_P0 TXP	PCIE_P0 TXN	
U		VSS	VSS	VSS		VSS	VSS		VSS	VSS		VSS	VSS		VSS		VSS	VSS	VSS
T				VCC_IP0 5_INT		VCC_IP0 5_INT	PCIE_P1 RXN		PCIE_P1 SATA_P0 RXP	SATA_P0 RXP		SATA_P1 SATA_P1 S_RXN	SATA_P1 S_RXN	SATA_P1 S_RXP			PCIE_P2 TXN	PCIE_P2 TXP	PCIE_P1 TXN
R	NCTF		NCTF														PCIE_P1 TXN	PCIE_P1 TXP	PCIE_P1 TXN
P	VSS		MCISL_DP 0	VCC_IP0 5_INT			VSS	PCIE_P3 USB3_P4 RXP		PCIE_P3 USB3_P4 RXN	VSS		PCIE_P0 RXN	PCIE_P0 RXN	VSS		PCIE_P3 USB3_P4 TXP	PCIE_P3 USB3_P4 TXN	PCIE_P3 USB3_P4 TXN
N																			VSS
M	MCISL_CL RP_0		MCISL_DN _0	NCTF		VSS		NCTF		NCTF	VSS		PCIE_P5 USB3_P2 RXN	PCIE_P2 RXN	PCIE_P2 RXN		VSS	PCIE_P4 USB3_P3 TXN	PCIE_P4 USB3_P3 TXN
L	MCISL_CL KN_0		MCISL_DP _2	NCTF		NCTF												PCIE_P5 USB3_P2 TXP	PCIE_P5 USB3_P2 TXN
K													USB3_P0 RXN	USB3_P0 RXP			USB3_P1 TXN	USB3_P1 TXN	USB3_P0 TXN
J	VSS		MCISL_DN _2	NCTF		VSS		VSS										USB3_P0 TXN	USB3_P0 TXN
H	MCISL_CL RP_2		VSS	NCTF		NCTF		NCTF		NCTF			VSS	PCIE_P3 USB3_P3 RXN	PCIE_P3 USB3_P3 RXP		VSS		
G																		USB3_P1 RXN	VSS
F	MCISL_CL KN_2		MCISL_DP _3	NCTF		NCTF		NCTF		VSS		NCTF		PCIE2_P5 P3_SATA 3_RCOM P_P_N	PCIE2_P5 P3_SATA 3_RCOM P_P_N		VSS	USB3_P1 RXP	RSVD
E	VSS		MCISL_DN _3	NCTF		VSS		VSS		NCTF		NCTF		NCTF		VSS	NCTF		
D																		NCTF	RSVD
C	RSVD	SVIDO_D ATA	SVIDO_CL K	VSS	NCTF	NCTF	NCTF	VSS	PCIE_CLK OUT0P	PCIE_CLK OUT1P	NCTF		PCIE_CLK OUT0N	PCIE_CLK OUT1N		PCIE_CLK OUT0N	PCIE_CLK OUT1N	NCTF	RSVD
B	RTAG_P MODE			SVIDO_AL ERT_B		NCTF		NCTF			VSS		PCIE_CLK OUT0N	PCIE_CLK OUT1N		PCIE_CLK OUT0N	PCIE_CLK OUT1N	VSS	VSS
A		RSVD			VSS		NCTF	VSS					PCIE_CLK OUT2P		VSS	RSVD	NCTF		



6.3 SoC Ball Map—LPDDR4

Figure 6-7. Ball Map LPDDR4—Left (63-42)

	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42
BJ		RSVD	RSVD	VSS		MEM_CH 0_CKE10		VSS		VSS		MEM_CH 0_CAA2		VSS		MEM_CH 0_CAA4		VSS		MEM_CH 0_DQ08		MEM_CH 0_DQ081
BH	VSS	VSS	MEM_CH 0_CAA0	MEM_CH 0_CAA3		MEM_CH 0_CK00		NCTF		MEM_CH 0_CAA8		MEM_CH 0_CAA9		NCTF		MEM_CH 0_CAB5		MEM_CH 0_DQ04		VSS		
BG	RSVD	MEM_CH 0_DQ03					NCTF	MEM_CH 0_CAA8	MEM_CH 0_CAA3	NCTF	MEM_CH 0_CAA4		NCTF	NCTF	NCTF	MEM_CH 0_CAB2	MEM_CH 0_CAB3	MEM_CH 0_CAB0	VSS	MEM_CH 0_DQ03	MEM_CH 0_DQ031	MEM_CH 0_DQ081
BF			VSS		MEM_CH 0_DQA10	MEM_CH 0_DQA20																
BE	VSS	MEM_CH 0_DQA2						MEM_CH 0_DQA24		VSS		VSS		MEM_CH 0_DQA21		VSS	VSS			MEM_CH 0_CLK8		VSS
BD	MEM_CH 0_DQA2	MEM_CH 0_DQA7	VSS		MEM_CH 0_DQA18	MEM_CH 0_DQA28		VSS		MEM_CH 0_DQA25		MEM_CH 0_DQA3		MEM_CH 0_DQA28		MEM_CH 0_CLKA	NCTF			MEM_CH 0_CLK8		NCTF
BC		MEM_CH 0_DQA0																				
BB	MEM_CH 0_DQ03		VSS		MEM_CH 0_DQA2	MEM_CH 0_DQA1	MEM_CH 0_DQA17			MEM_CH 0_DQA31		MEM_CH 0_DQA1		MEM_CH 0_DQA28		MEM_CH 0_CLKA	NCTF		VSS		NCTF	
BA	VSS	VSS												VSS		MEM_CH 0_DQA28		VSS	VSS		NCTF	VSS
AY	MEM_CH 0_DQA0	MEM_CH 0_DQA5			MEM_CH 0_DQA15	MEM_CH 0_DQA16	MEM_CH 0_DQA17	VSS		MEM_CH 0_DQA1	VSS											
AW														VSS			NCTF	NCTF		NCTF		NCTF
AV		VSS	VSS		MEM_CH 0_DQA8	MEM_CH 0_DQA11	MEM_CH 0_DQA12		VSS	MEM_CH 0_DQA20		MEM_CH 0_DQA28		VDDQ			NCTF	NCTF		VSS		VSS
AU	MEM_CH 0_DQA0	MEM_CH 0_DQA10																				
AT		VSS	VSS		MEM_CH 0_DQA1	MEM_CH 0_DQA11	VSS		MEM_CH 0_DQA11	MEM_CH 0_DQA14		VSS	VDDQ			VSS	VDDQ		VSS		MEM_CH 0_CS1A	
AR	LPSS_I2C 0_SCL	LPSS_I2C 0_SDA																VDDQ		VSS		MEM_CH 0_CS1A
AP	LPSS_I2C 0_SCL	LPSS_I2C 0_SDA			LPSS_I2C 0_SCL	LPSS_I2C 0_SCL	NCTF		VSS	LPSS_I2C 0_SCL		LPSS_I2C 0_SCL	LPSS_I2C 0_SCL	LPSS_I2C 0_SDA		LPSS_I2C 0_SDA						
AN	VSS	LPSS_I2C 0_SDA			VSS		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		VSS	VSS	VDDQ		VDDQ		VDDQ
AM		LPSS_I2C 0_SCL			NCTF	NCTF	ISH_GPIOD 0	ISH_GPIOD 0	ISH_GPIOD 0	ISH_GPIOD 0	ISH_GPIOD 0	ISH_GPIOD 0	ISH_GPIOD 0	ISH_GPIOD 0		ISH_GPIOD 0	ISH_GPIOD 0		VSS	VNN_SVI 0		VCCIOA
AL	LPSS_I2C 0_SCL	LPSS_I2C 0_SCL																				
AK		PMU_CLK 0_SDA	LPSS_I2C 0_SCL		VSS	ISH_GPIOD 0	ISH_GPIOD 0	PMU_PW 0_SDA	PMU_SLP 0_SDA			VSS	ISH_GPIOD 0	PMU_SLP 0_SDA		PMU_SLP 0_SDA	VSS	VNN_SVI 0	VNN_SVI 0	VNN_SVI 0	VNN_SVI 0	VNN_SVI 0
AJ	VSS	PMU_CLK 0_SDA																				
AH		PMU_CLK 0_SDA	PMU_CLK 0_SDA		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	PMU_SLP 0_SDA	PMU_SLP 0_SDA		RTC_TEST 0	VSS					
AG	PMU_CLK 0_SDA	PMU_CLK 0_SDA			PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA		PMU_CLK 0_SDA	PMU_CLK 0_SDA					
AF		PMU_CLK 0_SDA	PMU_CLK 0_SDA		PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA		PMU_CLK 0_SDA	PMU_CLK 0_SDA					
AE	VSS	PMU_CLK 0_SDA	PMU_CLK 0_SDA		PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA		PMU_CLK 0_SDA	PMU_CLK 0_SDA					
AD		PMU_CLK 0_SDA	PMU_CLK 0_SDA		PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA	PMU_CLK 0_SDA		PMU_CLK 0_SDA	PMU_CLK 0_SDA					
AC	SUSPWR 0_SDA	PMU_CLK 0_SDA			RTC_X1	RTC_X2	RTC_X3	RTC_X4	RTC_X5	RTC_X6	RTC_X7	RTC_X8	RTC_X9	RTC_X10		RTC_X11	RTC_X12					
AB	LPC_SERI 0_SDA	LPC_CLK 0_SDA			VSS	ICARD 0_SDA	VSS	ICARD 0_SDA	ICARD 0_SDA	ICARD 0_SDA	ICARD 0_SDA	ICARD 0_SDA	ICARD 0_SDA	ICARD 0_SDA		ICARD 0_SDA	ICARD 0_SDA					
AA	VSS	LPC_CLK 0_SDA																				
Y		LPC_AD0	LPC_AD1		VSS	EMMC_C 0_SDA	VSS	VSS	VSS	VSS	VSS	VSS	EMMC_C 0_SDA	EMMC_C 0_SDA		EMMC_C 0_SDA	VSS		VSS	VCC_3P3 0_SDA	VCC_3P3 0_SDA	VCC_3P3 0_SDA
W		LPC_AD2	LPC_AD3																			
V		LPC_CLK 0_SDA	LPC_FRA 0_SDA		EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA		EMMC_C 0_SDA	VSS		VSS	VCC_3P3 0_SDA	VCC_3P3 0_SDA	VSS
U	VSS	VSS			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		VSS	VSS					
T		SMB_CLK	SMB_DA 0_SDA		EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA	EMMC_C 0_SDA		VSS	VSS					
R	SMB_CLK	SMB_DA 0_SDA																				
P		SMB_CLK	SMB_DA 0_SDA		VSS	SDIO_CLK 0_SDA	SDIO_CLK 0_SDA		VSS	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA					
N	VSS	SMB_CLK	SMB_DA 0_SDA																			
M		AVS_DM1 0_SDA	AVS_DM1 0_SDA		VSS	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA					
L	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA					
K		AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA					
J	VSS	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA					
H	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA					
G		AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA					
F	VSS	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA					
E	NCTF	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA					
D		AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA					
C	NCTF	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA					
B	VSS	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA					
A		AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA	AVS_DM1 0_SDA		AVS_DM1 0_SDA	AVS_DM1 0_SDA					



Figure 6-8. Ball Map LPDDR4—Middle (41–20)

	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20
BJ	MEM_CH 0_DQ811	MEM_CH 0_DQ824	VSS			VSS	MEM_CH 0_DQ831	VSS		MEM_CH 1_DQ47	VSS		MEM_CH 1_DQ40	VSS	MEM_CH 1_DQ49	MEM_CH 1_DQ418	MEM_CH 1_DQ5A2_P		MEM_CH 1_DQ411			
BH	MEM_CH 0_DQ815	VSS	MEM_CH 0_DQ829	MEM_CH 0_DQ833_N	MEM_CH 0_DQ827		MEM_CH 1_DQ42	MEM_CH 1_DQ5A0_N		MEM_CH 1_DQ44	VSS		MEM_CH 1_DQ45	MEM_CH 1_DQ46	MEM_CH 1_DQ423	MEM_CH 1_DQ418	VSS		MEM_CH 1_DQ418	VSS		
BG	VSS	MEM_CH 0_DQ810	MEM_CH 0_DQ828	MEM_CH 0_DQ830	MEM_CH 0_DQ833_P	VSS	MEM_CH 0_DQ825	MEM_CH 0_DQ826	VSS	MEM_CH 1_DQ43	MEM_CH 1_DQ41	VSS	MEM_CH 1_DQ5A0_P	MEM_CH 1_DQ45	MEM_CH 1_DQ46	MEM_CH 1_DQ423	MEM_CH 1_DQ418	VSS	MEM_CH 1_DQ5A2_N	MEM_CH 1_DQ421	MEM_CH 1_DQ429	
BF										VSS												
BE	NCTF	MEM_CH 0_DQ821		VSS		VSS	MEM_CH 0_DQ817			MEM_CH 1_DQ410	VSS		VSS		VSS	MEM_CH 1_DQ412		NCTF		VSS		
BD	NCTF	MEM_CH 0_DQ822		MEM_CH 0_DQ819	MEM_CH 0_DQ822_N		MEM_CH 0_DQ818		VSS		MEM_CH 1_DQ411	MEM_CH 1_DQ5A1_P		MEM_CH 1_DQ415		MEM_CH 1_DQ414		NCTF		MEM_CH 1_CLKA_N		
BC										VSS												
BB	MEM_CH 0_C50_B	VSS		MEM_CH 0_DQ820	MEM_CH 0_DQ822_P		MEM_CH 0_DQ823			MEM_CH 1_DQ49	MEM_CH 1_DQ5A1_N		MEM_CH 1_DQ413		VSS		NCTF		MEM_CH 1_CLKA_P			
BA	MEM_CH 0_C51_B	VSS		VSS			VSS	MEM_CH 0_DQ816		VSS	MEM_CH 1_DQ48	VSS		VSS		VSS		NCTF		VSS		
AY										VSS												
AW	NCTF	MEM_CH 0_DQ5B0_N		MEM_CH 0_DQ82	MEM_CH 0_DQ87	VSS				VSS	MEM_CH 1_DQ425		MEM_CH 1_DQ431		MEM_CH 1_DQ5A3_N		NCTF		NCTF			
AV	VSS	MEM_CH 0_DQ5B0_P		MEM_CH 0_DQ81		VSS	MEM_CH 0_RCOM_P		VSS	MEM_CH 1_PCOM_P	VSS		MEM_CH 1_DQ5A2		MEM_CH 1_DQ5A3_P		VSS		VSS			
AU										VSS												
AT	MEM_CH 0_DQ8	VSS		MEM_CH 0_DQ84	VSS	NCTF				NCTF	VSS		MEM_CH 1_DQ424		VSS		MEM_CH 1_DQ427		NCTF			
AR	MEM_CH 0_DQ86	MEM_CH 0_DQ80		MEM_CH 0_DQ83	NCTF	MEM_CH 0_RESET_N		VSS		MEM_CH 1_RESET_N	NCTF		MEM_CH 1_DQ426		MEM_CH 1_DQ429		MEM_CH 1_DQ430		NCTF			
AP																						
AN	VDDQ	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RSVD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ
AM	VDDQ	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RSVD	VCC_VCG 1	VDD2_1P 24_GLM	VSS	VDD2_1P 24_GLM	VSS	VCCIOA	VCCIOA	VSS	VDD2_1P 24_GLM	VDD2_1P 24_GLM	VDD2_1P 24_GLM	VDD2_1P 24_GLM	VDD2_1P 24_GLM
AL	VNN_SV D	VNN_SV D	VNN_SV D	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AK	VNN_SV D	VNN_SV D	VNN_SV D	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AJ	VNN_SV D	VNN_SV D	VNN_SV D	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AH																						
AG	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AF																						
AE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AD																						
AC	VCC_3P 3V_A	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AB																						
AA	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
Y	VCC_VG GI	VCC_VCG I	VCC_VCG I	VCC_VCG I	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
W	VCC_VG GI	VCC_VCG I	VCC_VCG I	VCC_VCG I	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
V	VCC_VG GI	VCC_VCG I	VCC_VCG I	VCC_VCG I	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
U	VCC_VG GI	VCC_VCG I	VCC_VCG I	VCC_VCG I	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
T																						
R	VCC_VG GI_SENS E_P	NCTF	NCTF	GP_CAM ERASB6	GP_CAM ERASB10	VSS	NCTF	VSS	OSCIN	NCTF	VSS	OSCIN	NCTF	NCTF	NCTF	NCTF	VSS	MCSI_RV DATA0_N	MCSI_DP 1	MCSI_DP 1	MCSI_DP 1	MCSI_DP 1
P	VSS	NCTF	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
N	LPSS_U ART2_C TS_N	NCTF	GP_CAM ERASB4	GP_CAM ERASB9	GP_CAM ERASB8	VSS	GPIO_21 8	GPIO_21 7	VSS	GPIO_21 6	GPIO_21 5	VSS	GPIO_21 4	VSS	GPIO_21 3	VSS	GPIO_21 2	VSS	GPIO_21 1	VSS	VSS	VSS
M	LPSS_U ART2_R TS_N	GPIO_10	GP_CAM ERASB0	VSS	GP_CAM ERASB7	VSS	GPIO_21 6	GPIO_21 5	VSS	GPIO_21 4	GPIO_21 3	VSS	GPIO_21 2	VSS	GPIO_21 1	VSS	GPIO_21 0	VSS	GPIO_21 0	VSS	VSS	VSS
L																						
K	LPSS_U ART2_R XD	GPIO_18	VSS	VSS	GP_CAM ERASB2	VSS	VSS	NCTF	VSS	VSS	NCTF	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
J	LPSS_U ART2_T XD	GPIO_7	VSS	GPIO_29	GPIO_31	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
H																						
G																						
F	PWM2	GPIO_15	VSS	GPIO_32	GPIO_33	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
E	PWM3	GPIO_12	VCC_VCG I	VCC_VCG I	GPIO_RC OMP	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
D																						
C	PWM1	VSS	GPIO_2	GPIO_14	GPIO_30	GPIO_17	GPIO_11	GPIO_19	VSS	GPIO_26	GPIO_13	GPIO_27	VSS	GPIO_25	GPIO_21	GPIO_24	GPIO_23	GPIO_22	GPIO_21	GPIO_20	GPIO_19	GPIO_18
B	PWM0	GPIO_3	GPIO_28	GPIO_4	GPIO_1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
A	VSS	GPIO_0	VSS	GPIO_5	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS

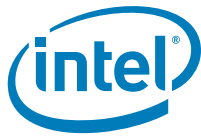


Figure 6-9. Ball Map LPDDR4—Right (19–1)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
BJ		VSS		MEM_CH 1_CKE1B		VSS		MEM_CH 1_CAA1		VSS		VSS		MEM_CH 1_CAB3		VSS	RSVD	NCTF	
BH	MEM_CH 1_DQA 22		MEM_CH 1_CKE0B		MEM_CH 1_CAA5		NCTF		MEM_CH 1_CAA4		MEM_CH 1_CAB5		MEM_CH 1_CAB2		MEM_CH 1_CAB4		MEM_CH 1_CAB1	MEM_CH 1_CAB0	VSS
BG	VSS	MEM_CH 1_CKE0A	MEM_CH 1_CKE1A		NCTF		NCTF	MEM_CH 1_CAA3		NCTF	MEM_CH 1_CAA0	MEM_CH 1_CAA2	NCTF	NCTF	NCTF			MEM_CH 1_DQB1	NCTF
BF														MEM_CH 1_DQB2	MEM_CH 1_DQB15		VSS		
BE	MEM_CH 1_DQA 22		VSS	VSS		MEM_CH 1_DQB2		VSS		VSS		MEM_CH 1_DQB7						MEM_CH 1_DQB27	VSS
BD	MEM_CH 1_DQA 22		MEM_CH 1_C50A		NCTF			MEM_CH 1_DQB6		MEM_CH 1_DQB5		MEM_CH 1_DQB1		VSS		MEM_CH 1_DQB9	MEM_CH 1_DQB10	VSS	MEM_CH 1_DQB25
BC																		MEM_CH 1_DQB26	MEM_CH 1_DQB28
BB	VSS		MEM_CH 1_C51A		NCTF			MEM_CH 1_DQB5		MEM_CH 1_DQB9		MEM_CH 1_DQB3		MEM_CH 1_DQB11	MEM_CH 1_DQB8	MEM_CH 1_DQB1	VSS		MEM_CH 1_DQB3
BA	NCTF		VSS	VSS		MEM_CH 1_DQB4		VSS										VSS	VSS
AY										VSS	MEM_CH 1_DQB13		MEM_CH 1_DQB14	VSS	MEM_CH 1_DQB20		MEM_CH 1_DQB30	MEM_CH 1_DQB24	
AW	NCTF		MEM_CH 1_C51B		NCTF		VSS											MEM_CH 1_DQB29	MEM_CH 1_DQB28
AV	VSS		MEM_CH 1_C50B		NCTF		VDDQ		MEM_CH 1_DQB8		MEM_CH 1_DQB12	VSS		MEM_CH 1_DQB23	MEM_CH 1_DQB22	MEM_CH 1_DQB21	VSS	VSS	
AU																		MEM_CH 1_DQB16	MEM_CH 1_DQB18
AT	VSS		VDDQ	VSS		VDDQ	VSS		MEM_CH 1_DQB17	MEM_CH 1_DQB18			VSS	MEM_CH 1_DQB2	MEM_CH 1_DQB2		VSS	VSS	
AR	VSS		VDDQ															MSI_A DP_1	MSI_A DN_1
AP					MSI_A DP_2		MSI_A DN_2	MSI_A DP_0		MSI_A DN_0	VSS		MSI_A DP_3	MSI_A DN_3		MSI_A CLKN		MSI_A CLKP	
AN		VDDQ	VSS	VSS		VSS	VSS		VSS	VSS		VSS		VSS	VSS			VSS	VSS
AM		VSS		DDIO_AU P_1	DDIO_AU XN		MSI_C DN_3	MSI_C DP_2		MSI_C DN_2	MSI_C CLKP		MSI_C CLKN	MSI_C DN_1	MSI_C DP_1		DDIO_TX P_1	DDIO_TX N_1	
AL																	DDIO_TX P_3	DDIO_TX N_3	
AK		VSS		DDIO_AU P_1	DDIO_AU XN		MSI_C DP_3	VSS		VSS	VSS		MSI_C DP_0	MSI_C DN_0	VSS		DDIO_TX P_0	DDIO_TX N_0	
AJ		VSS																VSS	VSS
AH				VSS	VSS		USB_SIC P_0_TX_P	USB_SIC P_0_TX_N		EDP_AUX P_0_TX_P	EDP_AUX P_0_TX_N		VSS	VSS	VSS		DDIO_TX P_2	DDIO_TX N_2	
AG		VSS		USB_SIC P_0_TX_P	USB_SIC P_0_TX_N		VSS	EDP_TXP P_1		EDP_TXN P_1	EDP_TXN P_0		EDP_TXP P_0	EDP_TXP P_0	EDP_TXP P_0		DDIO_TX P_0	DDIO_TX N_0	
AF																		DDIO_TX P_0	DDIO_TX N_0
AE		VDD2_P1 24_MPHY	VSS	VSS		VSS	VSS		VSS	VSS		VSS	VSS		VSS	VSS		VSS	VSS
AD																	DDIO_TX P_1	DDIO_TX N_1	
AC		VSS		USB2_VB P_1_TX_P	USB2_OT P_1_TX_N		NCTF	USB2_DP P_1		USB2_DN P_1	EDP_TXN P_3		EDP_TXP P_3	EDP_TXP P_2	EDP_TXN P_2		DDIO_TX P_2	DDIO_TX N_2	
AB				VSS	USB_SIC P_0_TX_P		NCTF	VSS		VSS	VSS		USB2_DN P_3	USB2_DP P_3	VSS		DDIO_TX P_3	DDIO_TX N_3	
AA		VDD2_P1 24_MPHY																VSS	VSS
Y		VCCRAM P_05_IO		VSS	USB2_RC P_0_TX_P		USB2_DP P_2	VSS		USB2_DN P_4	USB2_DP P_4		VSS	VSS	VSS		SATA_P0 TXN	SATA_P0 TXN	
W		VCCRAM P_05_IO		USB2_DP P_1	USB2_DN P_1		USB2_DN P_2	USB2_DP P_2		USB2_DN P_3	USB2_DP P_3		USB2_DN P_4	USB2_DP P_4			PCIE_P0 TXN	PCIE_P0 TXN	
V		VSS	VSS	VSS		VSS	VSS		VSS	VSS		VSS	VSS	VSS	VSS		PCIE_P0 TXN	PCIE_P0 TXN	
U		VSS	VSS	VSS		VSS	VSS		VSS	VSS		VSS	VSS	VSS	VSS		VSS	VSS	
T				VCC_P0 S_INT	VCC_P0 S_INT		VCC_P0 S_INT	PCIE_P1 RXN		PCIE_P1 RXN	SATA_P0 RXN		SATA_P0 RXN	SATA_P1 RXN	SATA_P1 RXN		PCIE_P2 TXN	PCIE_P2 TXN	
R	NCTF		NCTF														PCIE_P1 TXN	PCIE_P1 TXN	
P	VSS		MCB1_DP P_0	VCC_P0 S_INT				PCIE_P3 RXN		PCIE_P3 RXN	VSS		PCIE_P0 RXN	PCIE_P0 RXN	VSS		PCIE_P3 TXN	PCIE_P3 TXN	
N																	PCIE_P4 TXN	PCIE_P4 TXN	
M	MCB1_CL P_0		MCB1_DN P_0	NCTF		VSS		NCTF		NCTF	VSS		PCIE_P4 RXN	PCIE_P2 RXN	PCIE_P2 RXN		VSS	PCIE_P4 TXN	PCIE_P4 TXN
L	MCB1_CL P_0		MCB1_DN P_0	NCTF		NCTF							PCIE_P4 RXN	PCIE_P2 RXN	PCIE_P2 RXN		VSS	PCIE_P4 TXN	PCIE_P4 TXN
K													PCIE_P1 RXN	PCIE_P2 RXN	VSS	VSS	PCIE_P1 TXN	PCIE_P1 TXN	
J	VSS		MCB1_DN P_2	NCTF		VSS		VSS									PCIE_P1 TXN	PCIE_P1 TXN	
H	MCB1_CL P_2		VSS	NCTF		NCTF		NCTF		NCTF							PCIE_P1 TXN	PCIE_P1 TXN	
G																	PCIE_P1 TXN	PCIE_P1 TXN	
F	MCB1_CL P_2		MCB1_DP P_2	NCTF		NCTF		NCTF		VSS							PCIE_P1 TXN	PCIE_P1 TXN	
E	VSS		MCB1_DN P_2	NCTF		VSS		VSS		NCTF							PCIE_P1 TXN	PCIE_P1 TXN	
D																	PCIE_P1 TXN	PCIE_P1 TXN	
C	RSVD	SVIDO_D ATA	SVIDO_CL K	VSS	NCTF	NCTF	NCTF	VSS	PCIE_CLK OUT0P	PCIE_CLK OUT0P	NCTF						NCTF	RSVD	RSVD
B	RTAS_P MODE		SVIDO_AL ERT_B		NCTF				PCIE_CLK OUT0N	PCIE_CLK OUT0N	VSS		PCIE_CLK OUT0N	PCIE_CLK OUT0N		PCIE_CLK OUT0N	RSVD	VSS	VSS
A		RSVD		VSS		NCTF		VSS	PCIE_CLK OUT0N	PCIE_CLK OUT0N	VSS						NCTF		



6.4 SoC Pin List Numbers and Locations—DDR3L, LPDDR3, LPDDR4

Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 1 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
BB48	MEM_CH0_CLK1_P	MEM_CH0_CLKA_P	MEM_CH0_CLKA_P
BD48	MEM_CH0_CLK1_N	MEM_CH0_CLKA_N	MEM_CH0_CLKA_N
BD45	MEM_CH0_CLK0_P	MEM_CH0_CLKB_P	MEM_CH0_CLKB_P
BE45	MEM_CH0_CLK0_N	MEM_CH0_CLKB_N	MEM_CH0_CLKB_N
BB21	MEM_CH1_CLK1_P	MEM_CH1_CLKA_P	MEM_CH1_CLKA_P
BD21	MEM_CH1_CLK1_N	MEM_CH1_CLKA_N	MEM_CH1_CLKA_N
BD19	MEM_CH1_CLK0_P	MEM_CH1_CLKB_P	MEM_CH1_CLKB_P
BE19	MEM_CH1_CLK0_N	MEM_CH1_CLKB_N	MEM_CH1_CLKB_N
AR43	MEM_CH0_CS0_N	MEM_CH0_CS0A_N	MEM_CH0_CS0A
AT43	NCTF	MEM_CH0_CS1A_N	MEM_CH0_CS1A
BB41	NCTF	MEM_CH0_CS0B_N	MEM_CH0_CS0B
BA41	MEM_CH0_CS1_N	MEM_CH0_CS1B_N	MEM_CH0_CS1B
AW43	MEM_CH0_ODT0	MEM_CH0_ODTA	NCTF
AW41	MEM_CH0_ODT1	MEM_CH0_ODTB	NCTF
BH61	MEM_CH0_CKE0	MEM_CH0_CKE0A	MEM_CH0_CKE0A
BH60	MEM_CH0_CKE1	MEM_CH0_CKE1A	MEM_CH0_CKE1A
BH58	NCTF	MEM_CH0_CKE0B	MEM_CH0_CKE0B
BJ58	NCTF	MEM_CH0_CKE1B	MEM_CH0_CKE1B
BD17	MEM_CH1_CS0_N	MEM_CH1_CS0A_N	MEM_CH1_CS0A
BB17	NCTF	MEM_CH1_CS1A_N	MEM_CH1_CS1A
AV17	NCTF	MEM_CH1_CS0B_N	MEM_CH1_CS0B
AW17	MEM_CH1_CS1_N	MEM_CH1_CS1B_N	MEM_CH1_CS1B
AW16	MEM_CH1_ODT0	MEM_CH1_ODTA	NCTF
AV16	MEM_CH1_ODT1	MEM_CH1_ODTB	NCTF
BG18	MEM_CH1_CKE0	MEM_CH1_CKE0A	MEM_CH1_CKE0A
BG17	MEM_CH1_CKE1	MEM_CH1_CKE1A	MEM_CH1_CKE1A
BH17	NCTF	MEM_CH1_CKE0B	MEM_CH1_CKE0B
BJ16	NCTF	MEM_CH1_CKE1B	MEM_CH1_CKE1B
BJ52	MEM_CH0_MA5	MEM_CH0_CAA2	MEM_CH0_CAA2
BH53	MEM_CH0_MA8	MEM_CH0_CAA1	MEM_CH0_CAA0
BG53	MEM_CH0_MA6	MEM_CH0_CAA0	MEM_CH0_CAA1
BG54	MEM_CH0_MA12	MEM_CH0_CAA5	NCTF
BG52	MEM_CH0_MA9	MEM_CH0_CAA4	MEM_CH0_CAA4
BG55	MEM_CH0_MA7	MEM_CH0_CAA3	MEM_CH0_CAA3

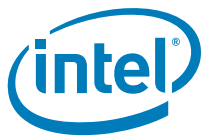


Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 2 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
BE41	MEM_CH0_MA4	NCTF	NCTF
BG56	MEM_CH0_MA14	MEM_CH0_CAA8	NCTF
BH57	MEM_CH0_BA2	MEM_CH0_CAA7	MEM_CH0_CAA5
BH55	MEM_CH0_MA11	MEM_CH0_CAA6	NCTF
BG57	MEM_CH0_MA15	MEM_CH0_CAA9	NCTF
BG11	MEM_CH1_MA5	MEM_CH1_CAA2	MEM_CH1_CAA2
BG12	MEM_CH1_MA8	MEM_CH1_CAA1	MEM_CH1_CAA0
BJ12	MEM_CH1_MA6	MEM_CH1_CAA0	MEM_CH1_CAA1
BG13	MEM_CH1_MA12	MEM_CH1_CAA5	NCTF
BH11	MEM_CH1_MA9	MEM_CH1_CAA4	MEM_CH1_CAA4
BG14	MEM_CH1_MA7	MEM_CH1_CAA3	MEM_CH1_CAA3
BB16	MEM_CH1_MA4	NCTF	NCTF
BG15	MEM_CH1_MA14	MEM_CH1_CAA8	NCTF
BH15	MEM_CH1_BA2	MEM_CH1_CAA7	MEM_CH1_CAA5
BH13	MEM_CH1_MA11	MEM_CH1_CAA6	NCTF
BG16	MEM_CH1_MA15	MEM_CH1_CAA9	NCTF
BJ48	MEM_CH0_BA0	MEM_CH0_CAB2	MEM_CH0_CAB4
BG47	MEM_CH0_RAS_N	MEM_CH0_CAB3	MEM_CH0_CAB3
BH51	MEM_CH0_MA2	MEM_CH0_CAB5	MEM_CH0_CAB5
BG50	MEM_CH0_MA0	MEM_CH0_CAB7	NCTF
BH49	MEM_CH0_MA10	MEM_CH0_CAB6	NCTF
BG49	MEM_CH0_BA1	MEM_CH0_CAB8	NCTF
BD41	MEM_CH0_MA3	NCTF	NCTF
BG51	MEM_CH0_MA1	MEM_CH0_CAB9	NCTF
BH47	MEM_CH0_CAS_N	MEM_CH0_CAB1	MEM_CH0_CAB1
BG48	MEM_CH0_WE_N	MEM_CH0_CAB4	MEM_CH0_CAB2
BG46	MEM_CH0_MA13	MEM_CH0_CAB0	MEM_CH0_CAB0
BH6	MEM_CH1_BA0	MEM_CH1_CAB2	MEM_CH1_CAB4
BJ6	MEM_CH1_RAS_N	MEM_CH1_CAB3	MEM_CH1_CAB3
BH9	MEM_CH1_MA2	MEM_CH1_CAB5	MEM_CH1_CAB5
BG9	MEM_CH1_MA0	MEM_CH1_CAB7	NCTF
BG7	MEM_CH1_MA10	MEM_CH1_CAB6	NCTF
BG8	MEM_CH1_BA1	MEM_CH1_CAB8	NCTF
BD16	MEM_CH1_MA3	NCTF	NCTF
BG10	MEM_CH1_MA1	MEM_CH1_CAB9	NCTF
BH4	MEM_CH1_CAS_N	MEM_CH1_CAB1	MEM_CH1_CAB1
BH7	MEM_CH1_WE_N	MEM_CH1_CAB4	MEM_CH1_CAB2

**Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 3 of 36)**

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
BH3	MEM_CH1_MA13	MEM_CH1_CAB0	MEM_CH1_CAB0
AR35	MEM_CH0_VREFCA	MEM_CH0_VREFCA	NCTF
AR29	MEM_CH1_VREFCA	MEM_CH1_VREFCA	NCTF
AT34	MEM_CH0_VREFDQ	MEM_CH0_VREFDQ	NCTF
AT30	MEM_CH1_VREFDQ	MEM_CH1_VREFDQ	NCTF
AR34	MEM_CH0_RESET_N	NCTF	MEM_CH0_RESET_N
AR30	MEM_CH1_RESET_N	NCTF	MEM_CH1_RESET_N
AV34	MEM_CH0_RCOMP	MEM_CH0_RCOMP	MEM_CH0_RCOMP
AV30	MEM_CH1_RCOMP	MEM_CH1_RCOMP	MEM_CH1_RCOMP
AY62	MEM_CH0_DQ0	MEM_CH0_DQA0	MEM_CH0_DQA0
AY61	MEM_CH0_DQ1	MEM_CH0_DQA1	MEM_CH0_DQA1
BE62	MEM_CH0_DQ2	MEM_CH0_DQA2	MEM_CH0_DQA2
BG62	MEM_CH0_DQ3	MEM_CH0_DQA3	MEM_CH0_DQA3
BD63	MEM_CH0_DQ4	MEM_CH0_DQA4	MEM_CH0_DQA4
AW62	MEM_CH0_DQ5	MEM_CH0_DQA5	MEM_CH0_DQA5
AW63	MEM_CH0_DQ6	MEM_CH0_DQA6	MEM_CH0_DQA6
BD62	MEM_CH0_DQ7	MEM_CH0_DQA7	MEM_CH0_DQA7
AV59	MEM_CH0_DQ8	MEM_CH0_DQA8	MEM_CH0_DQA8
AU63	MEM_CH0_DQ9	MEM_CH0_DQA9	MEM_CH0_DQA9
AU62	MEM_CH0_DQ10	MEM_CH0_DQA10	MEM_CH0_DQA10
AV58	MEM_CH0_DQ11	MEM_CH0_DQA11	MEM_CH0_DQA11
AV57	MEM_CH0_DQ12	MEM_CH0_DQA12	MEM_CH0_DQA12
AT55	MEM_CH0_DQ13	MEM_CH0_DQA13	MEM_CH0_DQA13
AT54	MEM_CH0_DQ14	MEM_CH0_DQA14	MEM_CH0_DQA14
AY59	MEM_CH0_DQ15	MEM_CH0_DQA15	MEM_CH0_DQA15
AY57	MEM_CH0_DQ16	MEM_CH0_DQA16	MEM_CH0_DQA16
BB57	MEM_CH0_DQ17	MEM_CH0_DQA17	MEM_CH0_DQA17
BD59	MEM_CH0_DQ18	MEM_CH0_DQA18	MEM_CH0_DQA18
BF59	MEM_CH0_DQ19	MEM_CH0_DQA19	MEM_CH0_DQA19
AV54	MEM_CH0_DQ20	MEM_CH0_DQA20	MEM_CH0_DQA20
AY55	MEM_CH0_DQ21	MEM_CH0_DQA21	MEM_CH0_DQA21
AV52	MEM_CH0_DQ22	MEM_CH0_DQA22	MEM_CH0_DQA22
BD58	MEM_CH0_DQ23	MEM_CH0_DQA23	MEM_CH0_DQA23
BE56	MEM_CH0_DQ24	MEM_CH0_DQA24	MEM_CH0_DQA24
BD54	MEM_CH0_DQ25	MEM_CH0_DQA25	MEM_CH0_DQA25
BF58	MEM_CH0_DQ26	MEM_CH0_DQA26	MEM_CH0_DQA26
BE50	MEM_CH0_DQ27	MEM_CH0_DQA27	MEM_CH0_DQA27

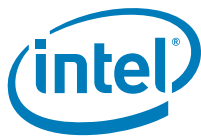


Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 4 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
BD50	MEM_CH0_DQ28	MEM_CH0_DQA28	MEM_CH0_DQA28
BB50	MEM_CH0_DQ29	MEM_CH0_DQA29	MEM_CH0_DQA29
BA50	MEM_CH0_DQ30	MEM_CH0_DQA30	MEM_CH0_DQA30
BB54	MEM_CH0_DQ31	MEM_CH0_DQA31	MEM_CH0_DQA31
BJ26	MEM_CH1_DQ0	MEM_CH1_DQA0	MEM_CH1_DQA0
BG30	MEM_CH1_DQ1	MEM_CH1_DQA1	MEM_CH1_DQA1
BH31	MEM_CH1_DQ2	MEM_CH1_DQA2	MEM_CH1_DQA2
BG31	MEM_CH1_DQ3	MEM_CH1_DQA3	MEM_CH1_DQA3
BH27	MEM_CH1_DQ4	MEM_CH1_DQA4	MEM_CH1_DQA4
BG27	MEM_CH1_DQ5	MEM_CH1_DQA5	MEM_CH1_DQA5
BG26	MEM_CH1_DQ6	MEM_CH1_DQA6	MEM_CH1_DQA6
BJ30	MEM_CH1_DQ7	MEM_CH1_DQA7	MEM_CH1_DQA7
BA30	MEM_CH1_DQ8	MEM_CH1_DQA8	MEM_CH1_DQA8
BB30	MEM_CH1_DQ9	MEM_CH1_DQA9	MEM_CH1_DQA9
BE30	MEM_CH1_DQ10	MEM_CH1_DQA10	MEM_CH1_DQA10
BD30	MEM_CH1_DQ11	MEM_CH1_DQA11	MEM_CH1_DQA11
BE25	MEM_CH1_DQ12	MEM_CH1_DQA12	MEM_CH1_DQA12
BB27	MEM_CH1_DQ13	MEM_CH1_DQA13	MEM_CH1_DQA13
BD25	MEM_CH1_DQ14	MEM_CH1_DQA14	MEM_CH1_DQA14
BD27	MEM_CH1_DQ15	MEM_CH1_DQA15	MEM_CH1_DQA15
BG24	MEM_CH1_DQ16	MEM_CH1_DQA16	MEM_CH1_DQA16
BJ20	MEM_CH1_DQ17	MEM_CH1_DQA17	MEM_CH1_DQA17
BH23	MEM_CH1_DQ18	MEM_CH1_DQA18	MEM_CH1_DQA18
BJ24	MEM_CH1_DQ19	MEM_CH1_DQA19	MEM_CH1_DQA19
BG20	MEM_CH1_DQ20	MEM_CH1_DQA20	MEM_CH1_DQA20
BG21	MEM_CH1_DQ21	MEM_CH1_DQA21	MEM_CH1_DQA21
BH19	MEM_CH1_DQ22	MEM_CH1_DQA22	MEM_CH1_DQA22
BG25	MEM_CH1_DQ23	MEM_CH1_DQA23	MEM_CH1_DQA23
AT27	MEM_CH1_DQ24	MEM_CH1_DQA24	MEM_CH1_DQA24
AW29	MEM_CH1_DQ25	MEM_CH1_DQA25	MEM_CH1_DQA25
AR27	MEM_CH1_DQ26	MEM_CH1_DQA26	MEM_CH1_DQA26
AT23	MEM_CH1_DQ27	MEM_CH1_DQA27	MEM_CH1_DQA27
AV27	MEM_CH1_DQ28	MEM_CH1_DQA28	MEM_CH1_DQA28
AR25	MEM_CH1_DQ29	MEM_CH1_DQA29	MEM_CH1_DQA29
AR23	MEM_CH1_DQ30	MEM_CH1_DQA30	MEM_CH1_DQA30
AW27	MEM_CH1_DQ31	MEM_CH1_DQA31	MEM_CH1_DQA31
BJ44	MEM_CH0_DQ40	MEM_CH0_DQB8	MEM_CH0_DQB8



Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 5 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
BG39	MEM_CH0_DQ41	MEM_CH0_DQB9	MEM_CH0_DQB9
BG40	MEM_CH0_DQ42	MEM_CH0_DQB10	MEM_CH0_DQB10
BJ40	MEM_CH0_DQ43	MEM_CH0_DQB11	MEM_CH0_DQB11
BG43	MEM_CH0_DQ44	MEM_CH0_DQB12	MEM_CH0_DQB12
BG44	MEM_CH0_DQ45	MEM_CH0_DQB13	MEM_CH0_DQB13
BH45	MEM_CH0_DQ46	MEM_CH0_DQB14	MEM_CH0_DQB14
BH41	MEM_CH0_DQ47	MEM_CH0_DQB15	MEM_CH0_DQB15
AR39	MEM_CH0_DQ32	MEM_CH0_DQB0	MEM_CH0_DQB0
AV37	MEM_CH0_DQ33	MEM_CH0_DQB1	MEM_CH0_DQB1
AW37	MEM_CH0_DQ34	MEM_CH0_DQB2	MEM_CH0_DQB2
AR37	MEM_CH0_DQ35	MEM_CH0_DQB3	MEM_CH0_DQB3
AT37	MEM_CH0_DQ36	MEM_CH0_DQB4	MEM_CH0_DQB4
AT41	MEM_CH0_DQ37	MEM_CH0_DQB5	MEM_CH0_DQB5
AR41	MEM_CH0_DQ38	MEM_CH0_DQB6	MEM_CH0_DQB6
AW35	MEM_CH0_DQ39	MEM_CH0_DQB7	MEM_CH0_DQB7
BJ38	MEM_CH0_DQ56	MEM_CH0_DQB24	MEM_CH0_DQB24
BG34	MEM_CH0_DQ57	MEM_CH0_DQB25	MEM_CH0_DQB25
BG33	MEM_CH0_DQ58	MEM_CH0_DQB26	MEM_CH0_DQB26
BH33	MEM_CH0_DQ59	MEM_CH0_DQB27	MEM_CH0_DQB27
BG38	MEM_CH0_DQ60	MEM_CH0_DQB28	MEM_CH0_DQB28
BH37	MEM_CH0_DQ61	MEM_CH0_DQB29	MEM_CH0_DQB29
BG37	MEM_CH0_DQ62	MEM_CH0_DQB30	MEM_CH0_DQB30
BJ34	MEM_CH0_DQ63	MEM_CH0_DQB31	MEM_CH0_DQB31
BA34	MEM_CH0_DQ48	MEM_CH0_DQB16	MEM_CH0_DQB16
BE34	MEM_CH0_DQ49	MEM_CH0_DQB17	MEM_CH0_DQB17
BD34	MEM_CH0_DQ50	MEM_CH0_DQB18	MEM_CH0_DQB18
BD37	MEM_CH0_DQ51	MEM_CH0_DQB19	MEM_CH0_DQB19
BB37	MEM_CH0_DQ52	MEM_CH0_DQB20	MEM_CH0_DQB20
BE39	MEM_CH0_DQ53	MEM_CH0_DQB21	MEM_CH0_DQB21
BD39	MEM_CH0_DQ54	MEM_CH0_DQB22	MEM_CH0_DQB22
BB34	MEM_CH0_DQ55	MEM_CH0_DQB23	MEM_CH0_DQB23
AV12	MEM_CH1_DQ40	MEM_CH1_DQB8	MEM_CH1_DQB8
BD6	MEM_CH1_DQ41	MEM_CH1_DQB9	MEM_CH1_DQB9
BD5	MEM_CH1_DQ42	MEM_CH1_DQB10	MEM_CH1_DQB10
BB7	MEM_CH1_DQ43	MEM_CH1_DQB11	MEM_CH1_DQB11
AV10	MEM_CH1_DQ44	MEM_CH1_DQB12	MEM_CH1_DQB12
AY9	MEM_CH1_DQ45	MEM_CH1_DQB13	MEM_CH1_DQB13



Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 6 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
AY7	MEM_CH1_DQ46	MEM_CH1_DQB14	MEM_CH1_DQB14
BF5	MEM_CH1_DQ47	MEM_CH1_DQB15	MEM_CH1_DQB15
BF6	MEM_CH1_DQ32	MEM_CH1_DQB0	MEM_CH1_DQB0
BD10	MEM_CH1_DQ33	MEM_CH1_DQB1	MEM_CH1_DQB1
BE14	MEM_CH1_DQ34	MEM_CH1_DQB2	MEM_CH1_DQB2
BB10	MEM_CH1_DQ35	MEM_CH1_DQB3	MEM_CH1_DQB3
BA14	MEM_CH1_DQ36	MEM_CH1_DQB4	MEM_CH1_DQB4
BB14	MEM_CH1_DQ37	MEM_CH1_DQB5	MEM_CH1_DQB5
BD14	MEM_CH1_DQ38	MEM_CH1_DQB6	MEM_CH1_DQB6
BE8	MEM_CH1_DQ39	MEM_CH1_DQB7	MEM_CH1_DQB7
AY2	MEM_CH1_DQ56	MEM_CH1_DQB24	MEM_CH1_DQB24
BD2	MEM_CH1_DQ57	MEM_CH1_DQB25	MEM_CH1_DQB25
BD1	MEM_CH1_DQ58	MEM_CH1_DQB26	MEM_CH1_DQB26
BE2	MEM_CH1_DQ59	MEM_CH1_DQB27	MEM_CH1_DQB27
AW1	MEM_CH1_DQ60	MEM_CH1_DQB28	MEM_CH1_DQB28
AW2	MEM_CH1_DQ61	MEM_CH1_DQB29	MEM_CH1_DQB29
AY3	MEM_CH1_DQ62	MEM_CH1_DQB30	MEM_CH1_DQB30
BG2	MEM_CH1_DQ63	MEM_CH1_DQB31	MEM_CH1_DQB31
AU2	MEM_CH1_DQ48	MEM_CH1_DQB16	MEM_CH1_DQB16
AT10	MEM_CH1_DQ49	MEM_CH1_DQB17	MEM_CH1_DQB17
AT9	MEM_CH1_DQ50	MEM_CH1_DQB18	MEM_CH1_DQB18
AU1	MEM_CH1_DQ51	MEM_CH1_DQB19	MEM_CH1_DQB19
AY5	MEM_CH1_DQ52	MEM_CH1_DQB20	MEM_CH1_DQB20
AV5	MEM_CH1_DQ53	MEM_CH1_DQB21	MEM_CH1_DQB21
AV6	MEM_CH1_DQ54	MEM_CH1_DQB22	MEM_CH1_DQB22
AV7	MEM_CH1_DQ55	MEM_CH1_DQB23	MEM_CH1_DQB23
BJ42	MEM_CH0_DQS5_P	MEM_CH0_DQSB1_P	MEM_CH0_DQSB1_P
BG42	MEM_CH0_DQS5_N	MEM_CH0_DQSB1_N	MEM_CH0_DQSB1_N
AV39	MEM_CH0_DQS4_P	MEM_CH0_DQSB0_P	MEM_CH0_DQSB0_P
AW39	MEM_CH0_DQS4_N	MEM_CH0_DQSB0_N	MEM_CH0_DQSB0_N
BG36	MEM_CH0_DQS7_P	MEM_CH0_DQSB3_P	MEM_CH0_DQSB3_P
BH35	MEM_CH0_DQS7_N	MEM_CH0_DQSB3_N	MEM_CH0_DQSB3_N
BB35	MEM_CH0_DQS6_P	MEM_CH0_DQSB2_P	MEM_CH0_DQSB2_P
BD35	MEM_CH0_DQS6_N	MEM_CH0_DQSB2_N	MEM_CH0_DQSB2_N
BB63	MEM_CH0_DQS0_P	MEM_CH0_DQSA0_P	MEM_CH0_DQSA0_P
BC62	MEM_CH0_DQS0_N	MEM_CH0_DQSA0_N	MEM_CH0_DQSA0_N
AT59	MEM_CH0_DQS1_P	MEM_CH0_DQSA1_P	MEM_CH0_DQSA1_P

**Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 7 of 36)**

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
AT58	MEM_CH0_DQS1_N	MEM_CH0_DQSA1_N	MEM_CH0_DQSA1_N
BB59	MEM_CH0_DQS2_P	MEM_CH0_DQSA2_P	MEM_CH0_DQSA2_P
BB58	MEM_CH0_DQS2_N	MEM_CH0_DQSA2_N	MEM_CH0_DQSA2_N
BD52	MEM_CH0_DQS3_P	MEM_CH0_DQSA3_P	MEM_CH0_DQSA3_P
BB52	MEM_CH0_DQS3_N	MEM_CH0_DQSA3_N	MEM_CH0_DQSA3_N
BB5	MEM_CH1_DQS5_P	MEM_CH1_DQSB1_P	MEM_CH1_DQSB1_P
BB6	MEM_CH1_DQS5_N	MEM_CH1_DQSB1_N	MEM_CH1_DQSB1_N
BB12	MEM_CH1_DQS4_P	MEM_CH1_DQSB0_P	MEM_CH1_DQSB0_P
BD12	MEM_CH1_DQS4_N	MEM_CH1_DQSB0_N	MEM_CH1_DQSB0_N
BC2	MEM_CH1_DQS7_P	MEM_CH1_DQSB3_P	MEM_CH1_DQSB3_P
BB1	MEM_CH1_DQS7_N	MEM_CH1_DQSB3_N	MEM_CH1_DQSB3_N
AT5	MEM_CH1_DQS6_P	MEM_CH1_DQSB2_P	MEM_CH1_DQSB2_P
AT6	MEM_CH1_DQS6_N	MEM_CH1_DQSB2_N	MEM_CH1_DQSB2_N
BG28	MEM_CH1_DQS0_P	MEM_CH1_DQSA0_P	MEM_CH1_DQSA0_P
BH29	MEM_CH1_DQS0_N	MEM_CH1_DQSA0_N	MEM_CH1_DQSA0_N
BD29	MEM_CH1_DQS1_P	MEM_CH1_DQSA1_P	MEM_CH1_DQSA1_P
BB29	MEM_CH1_DQS1_N	MEM_CH1_DQSA1_N	MEM_CH1_DQSA1_N
BJ22	MEM_CH1_DQS2_P	MEM_CH1_DQSA2_P	MEM_CH1_DQSA2_P
BG22	MEM_CH1_DQS2_N	MEM_CH1_DQSA2_N	MEM_CH1_DQSA2_N
AV25	MEM_CH1_DQS3_P	MEM_CH1_DQSA3_P	MEM_CH1_DQSA3_P
AW25	MEM_CH1_DQS3_N	MEM_CH1_DQSA3_N	MEM_CH1_DQSA3_N
AW48	NCTF	NCTF	NCTF
AW47	NCTF	NCTF	NCTF
BB43	NCTF	NCTF	NCTF
AW45	NCTF	NCTF	NCTF
AV48	NCTF	NCTF	NCTF
AV47	NCTF	NCTF	NCTF
BD43	NCTF	NCTF	NCTF
BA45	NCTF	NCTF	NCTF
BD47	NCTF	NCTF	NCTF
BB47	NCTF	NCTF	NCTF
AR21	NCTF	NCTF	NCTF
AT21	NCTF	NCTF	NCTF
AW23	NCTF	NCTF	NCTF
AW21	NCTF	NCTF	NCTF
BA19	NCTF	NCTF	NCTF
AW19	NCTF	NCTF	NCTF

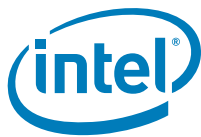


Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 8 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
BA23	NCTF	NCTF	NCTF
BB23	NCTF	NCTF	NCTF
BD23	NCTF	NCTF	NCTF
BE23	NCTF	NCTF	NCTF
AK3	DDIO_TXP_0	DDIO_TXP_0	DDIO_TXP_0
AK2	DDIO_TXN_0	DDIO_TXN_0	DDIO_TXN_0
AM3	DDIO_TXP_1	DDIO_TXP_1	DDIO_TXP_1
AM2	DDIO_TXN_1	DDIO_TXN_1	DDIO_TXN_1
AH3	DDIO_TXP_2	DDIO_TXP_2	DDIO_TXP_2
AH2	DDIO_TXN_2	DDIO_TXN_2	DDIO_TXN_2
AL2	DDIO_TXP_3	DDIO_TXP_3	DDIO_TXP_3
AL1	DDIO_TXN_3	DDIO_TXN_3	DDIO_TXN_3
AF2	DDI1_TXP_0	DDI1_TXP_0	DDI1_TXP_0
AF3	DDI1_TXN_0	DDI1_TXN_0	DDI1_TXN_0
AD3	DDI1_TXP_1	DDI1_TXP_1	DDI1_TXP_1
AD2	DDI1_TXN_1	DDI1_TXN_1	DDI1_TXN_1
AC1	DDI1_TXP_2	DDI1_TXP_2	DDI1_TXP_2
AC2	DDI1_TXN_2	DDI1_TXN_2	DDI1_TXN_2
AB3	DDI1_TXP_3	DDI1_TXP_3	DDI1_TXP_3
AB2	DDI1_TXN_3	DDI1_TXN_3	DDI1_TXN_3
AG7	EDP_TXP_0	EDP_TXP_0	EDP_TXP_0
AG9	EDP_TXN_0	EDP_TXN_0	EDP_TXN_0
AG12	EDP_TXP_1	EDP_TXP_1	EDP_TXP_1
AG10	EDP_TXN_1	EDP_TXN_1	EDP_TXN_1
AC6	EDP_TXP_2	EDP_TXP_2	EDP_TXP_2
AC5	EDP_TXN_2	EDP_TXN_2	EDP_TXN_2
AC7	EDP_TXP_3	EDP_TXP_3	EDP_TXP_3
AC9	EDP_TXN_3	EDP_TXN_3	EDP_TXN_3
AM16	DDIO_AUXP	DDIO_AUXP	DDIO_AUXP
AM15	DDIO_AUXN	DDIO_AUXN	DDIO_AUXN
AK16	DDI1_AUXP	DDI1_AUXP	DDI1_AUXP
AK15	DDI1_AUXN	DDI1_AUXN	DDI1_AUXN
AH10	EDP_AUXP	EDP_AUXP	EDP_AUXP
AH9	EDP_AUXN	EDP_AUXN	EDP_AUXN
AG1	DDIO_RCOMP_P	DDIO_RCOMP_P	DDIO_RCOMP_P
AG2	DDIO_RCOMP_N	DDIO_RCOMP_N	DDIO_RCOMP_N
AG6	EDP_RCOMP_P	EDP_RCOMP_P	EDP_RCOMP_P

**Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 9 of 36)**

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
AG5	EDP_RCOMP_N	EDP_RCOMP_N	EDP_RCOMP_N
AP3	MDSI_A_CLKN	MDSI_A_CLKN	MDSI_A_CLKN
AP2	MDSI_A_CLKP	MDSI_A_CLKP	MDSI_A_CLKP
AP10	MDSI_A_DN_0	MDSI_A_DN_0	MDSI_A_DN_0
AR1	MDSI_A_DN_1	MDSI_A_DN_1	MDSI_A_DN_1
AP13	MDSI_A_DN_2	MDSI_A_DN_2	MDSI_A_DN_2
AP5	MDSI_A_DN_3	MDSI_A_DN_3	MDSI_A_DN_3
AP12	MDSI_A_DP_0	MDSI_A_DP_0	MDSI_A_DP_0
AR2	MDSI_A_DP_1	MDSI_A_DP_1	MDSI_A_DP_1
AP15	MDSI_A_DP_2	MDSI_A_DP_2	MDSI_A_DP_2
AP6	MDSI_A_DP_3	MDSI_A_DP_3	MDSI_A_DP_3
AM7	MDSI_C_CLKN	MDSI_C_CLKN	MDSI_C_CLKN
AM9	MDSI_C_CLKP	MDSI_C_CLKP	MDSI_C_CLKP
AK6	MDSI_C_DN_0	MDSI_C_DN_0	MDSI_C_DN_0
AM6	MDSI_C_DN_1	MDSI_C_DN_1	MDSI_C_DN_1
AM10	MDSI_C_DN_2	MDSI_C_DN_2	MDSI_C_DN_2
AM13	MDSI_C_DN_3	MDSI_C_DN_3	MDSI_C_DN_3
AK7	MDSI_C_DP_0	MDSI_C_DP_0	MDSI_C_DP_0
AM5	MDSI_C_DP_1	MDSI_C_DP_1	MDSI_C_DP_1
AM12	MDSI_C_DP_2	MDSI_C_DP_2	MDSI_C_DP_2
AK13	MDSI_C_DP_3	MDSI_C_DP_3	MDSI_C_DP_3
AP7	MDSI_RCOMP	MDSI_RCOMP	MDSI_RCOMP
L19	MCSI_CLKN_0	MCSI_CLKN_0	MCSI_CLKN_0
M19	MCSI_CLKP_0	MCSI_CLKP_0	MCSI_CLKP_0
F19	MCSI_CLKN_2	MCSI_CLKN_2	MCSI_CLKN_2
H19	MCSI_CLKP_2	MCSI_CLKP_2	MCSI_CLKP_2
M17	MCSI_DN_0	MCSI_DN_0	MCSI_DN_0
P17	MCSI_DP_0	MCSI_DP_0	MCSI_DP_0
R21	MCSI_DN_1	MCSI_DN_1	MCSI_DN_1
P21	MCSI_DP_1	MCSI_DP_1	MCSI_DP_1
J17	MCSI_DN_2	MCSI_DN_2	MCSI_DN_2
L17	MCSI_DP_2	MCSI_DP_2	MCSI_DP_2
E17	MCSI_DN_3	MCSI_DN_3	MCSI_DN_3
F17	MCSI_DP_3	MCSI_DP_3	MCSI_DP_3
H27	MCSI_DPHY1.1_RCOMP	MCSI_DPHY1.1_RCOMP	MCSI_DPHY1.1_RCOMP
M23	MCSI_RX_DATA0_P	MCSI_RX_DATA0_P	MCSI_RX_DATA0_P
P23	MCSI_RX_DATA0_N	MCSI_RX_DATA0_N	MCSI_RX_DATA0_N

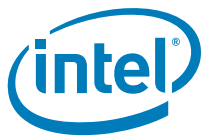


Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 10 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
L23	MCSI_RX_CLK0_P	MCSI_RX_CLK0_P	MCSI_RX_CLK0_P
J23	MCSI_RX_CLK0_N	MCSI_RX_CLK0_N	MCSI_RX_CLK0_N
J21	MCSI_RX_DATA1_P	MCSI_RX_DATA1_P	MCSI_RX_DATA1_P
H21	MCSI_RX_DATA1_N	MCSI_RX_DATA1_N	MCSI_RX_DATA1_N
M25	MCSI_RX_DATA2_P	MCSI_RX_DATA2_P	MCSI_RX_DATA2_P
L25	MCSI_RX_DATA2_N	MCSI_RX_DATA2_N	MCSI_RX_DATA2_N
F25	MCSI_RX_CLK1_P	MCSI_RX_CLK1_P	MCSI_RX_CLK1_P
E25	MCSI_RX_CLK1_N	MCSI_RX_CLK1_N	MCSI_RX_CLK1_N
H25	MCSI_RX_DATA3_P	MCSI_RX_DATA3_P	MCSI_RX_DATA3_P
J25	MCSI_RX_DATA3_N	MCSI_RX_DATA3_N	MCSI_RX_DATA3_N
F27	MCSI_DPHY1.2_RCOMP	MCSI_DPHY1.2_RCOMP	MCSI_DPHY1.2_RCOMP
AG54	RSVD	RSVD	RSVD
AG52	RSVD	RSVD	RSVD
J43	RSVD	RSVD	RSVD
H43	RSVD	RSVD	RSVD
AG15	RSVD	RSVD	RSVD
AG16	RSVD	RSVD	RSVD
AH12	RSVD	RSVD	RSVD
AH13	RSVD	RSVD	RSVD
AB15	RSVD	RSVD	RSVD
V59	EMMC_RCOMP	EMMC_RCOMP	EMMC_RCOMP
V12	USB2_DP0	USB2_DP0	USB2_DP0
V10	USB2_DN0	USB2_DN0	USB2_DN0
V16	USB2_DP1	USB2_DP1	USB2_DP1
V15	USB2_DN1	USB2_DN1	USB2_DN1
Y13	USB2_DP2	USB2_DP2	USB2_DP2
V13	USB2_DN2	USB2_DN2	USB2_DN2
V9	USB2_DP3	USB2_DP3	USB2_DP3
V7	USB2_DN3	USB2_DN3	USB2_DN3
Y9	USB2_DP4	USB2_DP4	USB2_DP4
Y10	USB2_DN4	USB2_DN4	USB2_DN4
AB6	USB2_DP5	USB2_DP5	USB2_DP5
AB7	USB2_DN5	USB2_DN5	USB2_DN5
AC12	USB2_DP6	USB2_DP6	USB2_DP6
AC10	USB2_DN6	USB2_DN6	USB2_DN6
V5	USB2_DP7	USB2_DP7	USB2_DP7
V6	USB2_DN7	USB2_DN7	USB2_DN7

**Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 11 of 36)**

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
AC15	USB2_DUALROLE_ID	USB2_DUALROLE_ID	USB2_DUALROLE_ID
AC16	USB2_VBUS_SNS	USB2_VBUS_SNS	USB2_VBUS_SNS
Y15	USB2_RCOMP	USB2_RCOMP	USB2_RCOMP
R27	OSCIN	OSCIN	OSCIN
P29	OSCOU	OSCOU	OSCOU
C11	PCIE_CLKOUT0P	PCIE_CLKOUT0P	PCIE_CLKOUT0P
B11	PCIE_CLKOUT0N	PCIE_CLKOUT0N	PCIE_CLKOUT0N
C10	PCIE_CLKOUT1P	PCIE_CLKOUT1P	PCIE_CLKOUT1P
A10	PCIE_CLKOUT1N	PCIE_CLKOUT1N	PCIE_CLKOUT1N
A7	PCIE_CLKOUT2P	PCIE_CLKOUT2P	PCIE_CLKOUT2P
B8	PCIE_CLKOUT2N	PCIE_CLKOUT2N	PCIE_CLKOUT2N
B7	PCIE_CLKOUT3P	PCIE_CLKOUT3P	PCIE_CLKOUT3P
B5	PCIE_CLKOUT3N	PCIE_CLKOUT3N	PCIE_CLKOUT3N
E21	PCIE_REF_CLK_RCOMP	PCIE_REF_CLK_RCOMP	PCIE_REF_CLK_RCOMP
V49	RSVD	RSVD	RSVD
E34	GPIO_RCOMP	GPIO_RCOMP	GPIO_RCOMP
AC54	INTRUDER_N	INTRUDER_N	INTRUDER_N
AG51	VCC_RTC_EXTPAD	VCC_RTC_EXTPAD	VCC_RTC_EXTPAD
AC59	RTC_X1	RTC_X1	RTC_X1
AC58	RTC_X2	RTC_X2	RTC_X2
AG49	SOC_PWROK	SOC_PWROK	SOC_PWROK
AC57	RSM_RST_N	RSM_RST_N	RSM_RST_N
AH49	RTC_TEST_N	RTC_TEST_N	RTC_TEST_N
AC55	RTC_RST_N	RTC_RST_N	RTC_RST_N
Y2	SATA_P0_TXN	SATA_P0_TXN	SATA_P0_TXN
Y3	SATA_P0_TXP	SATA_P0_TXP	SATA_P0_TXP
T7	SATA_P0_RXN	SATA_P0_RXN	SATA_P0_RXN
T9	SATA_P0_RXP	SATA_P0_RXP	SATA_P0_RXP
W2	SATA_P1_USB3_P5_TXN	SATA_P1_USB3_P5_TXN	SATA_P1_USB3_P5_TXN
W1	SATA_P1_USB3_P5_TXP	SATA_P1_USB3_P5_TXP	SATA_P1_USB3_P5_TXP
T6	SATA_P1_USB3_P5_RXN	SATA_P1_USB3_P5_RXN	SATA_P1_USB3_P5_RXN
T5	SATA_P1_USB3_P5_RXP	SATA_P1_USB3_P5_RXP	SATA_P1_USB3_P5_RXP
V2	PCIE_P0_TXN	PCIE_P0_TXN	PCIE_P0_TXN
V3	PCIE_P0_TXP	PCIE_P0_TXP	PCIE_P0_TXP
P6	PCIE_P0_RXN	PCIE_P0_RXN	PCIE_P0_RXN
P7	PCIE_P0_RXP	PCIE_P0_RXP	PCIE_P0_RXP
R2	PCIE_P1_TXN	PCIE_P1_TXN	PCIE_P1_TXN

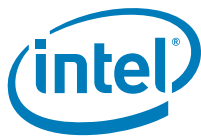


Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 12 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
R1	PCIE_P1_TXP	PCIE_P1_TXP	PCIE_P1_TXP
T12	PCIE_P1_RXN	PCIE_P1_RXN	PCIE_P1_RXN
T10	PCIE_P1_RXP	PCIE_P1_RXP	PCIE_P1_RXP
T3	PCIE_P2_TXN	PCIE_P2_TXN	PCIE_P2_TXN
T2	PCIE_P2_TXP	PCIE_P2_TXP	PCIE_P2_TXP
M6	PCIE_P2_RXN	PCIE_P2_RXN	PCIE_P2_RXN
M5	PCIE_P2_RXP	PCIE_P2_RXP	PCIE_P2_RXP
F6	PCIE2_USB3_SATA3_RC OMP_P	PCIE2_USB3_SATA3_RCO MP_P	PCIE2_USB3_SATA3_RCOM P_P
F5	PCIE2_USB3_SATA3_RC OMP_N	PCIE2_USB3_SATA3_RCO MP_N	PCIE2_USB3_SATA3_RCOM P_N
P2	PCIE_P3_USB3_P4_TXN	PCIE_P3_USB3_P4_TXN	PCIE_P3_USB3_P4_TXN
P3	PCIE_P3_USB3_P4_TXP	PCIE_P3_USB3_P4_TXP	PCIE_P3_USB3_P4_TXP
P10	PCIE_P3_USB3_P4_RXN	PCIE_P3_USB3_P4_RXN	PCIE_P3_USB3_P4_RXN
P12	PCIE_P3_USB3_P4_RXP	PCIE_P3_USB3_P4_RXP	PCIE_P3_USB3_P4_RXP
M2	PCIE_P4_USB3_P3_TXN	PCIE_P4_USB3_P3_TXN	PCIE_P4_USB3_P3_TXN
N2	PCIE_P4_USB3_P3_TXP	PCIE_P4_USB3_P3_TXP	PCIE_P4_USB3_P3_TXP
H6	PCIE_P4_USB3_P3_RXN	PCIE_P4_USB3_P3_RXN	PCIE_P4_USB3_P3_RXN
H5	PCIE_P4_USB3_P3_RXP	PCIE_P4_USB3_P3_RXP	PCIE_P4_USB3_P3_RXP
L1	PCIE_P5_USB3_P2_TXN	PCIE_P5_USB3_P2_TXN	PCIE_P5_USB3_P2_TXN
L2	PCIE_P5_USB3_P2_TXP	PCIE_P5_USB3_P2_TXP	PCIE_P5_USB3_P2_TXP
M7	PCIE_P5_USB3_P2_RXN	PCIE_P5_USB3_P2_RXN	PCIE_P5_USB3_P2_RXN
K7	PCIE_P5_USB3_P2_RXP	PCIE_P5_USB3_P2_RXP	PCIE_P5_USB3_P2_RXP
K2	USB3_P1_TXN	USB3_P1_TXN	USB3_P1_TXN
K3	USB3_P1_TXP	USB3_P1_TXP	USB3_P1_TXP
G2	USB3_P1_RXN	USB3_P1_RXN	USB3_P1_RXN
F2	USB3_P1_RXP	USB3_P1_RXP	USB3_P1_RXP
J2	USB3_P0_TXN	USB3_P0_TXN	USB3_P0_TXN
J1	USB3_P0_TXP	USB3_P0_TXP	USB3_P0_TXP
K10	USB3_P0_RXN	USB3_P0_RXN	USB3_P0_RXN
K9	USB3_P0_RXP	USB3_P0_RXP	USB3_P0_RXP
AG59	PMU_RCOMP	PMU_RCOMP	PMU_RCOMP
C19	RSVD	RSVD	RSVD
A18	RSVD	RSVD	RSVD
A4	DEBUG_PORT_A0	DEBUG_PORT_A0	DEBUG_PORT_A0
B4	DEBUG_PORT_A1	DEBUG_PORT_A1	DEBUG_PORT_A1
F1	DEBUG_PORT_B0	DEBUG_PORT_B0	DEBUG_PORT_B0
C1	DEBUG_PORT_B1	DEBUG_PORT_B1	DEBUG_PORT_B1

**Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 13 of 36)**

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
R62	PCIE_WAKE0_N	PCIE_WAKE0_N	PCIE_WAKE0_N
P62	PCIE_WAKE1_N	PCIE_WAKE1_N	PCIE_WAKE1_N
P61	PCIE_WAKE2_N	PCIE_WAKE2_N	PCIE_WAKE2_N
N62	PCIE_WAKE3_N	PCIE_WAKE3_N	PCIE_WAKE3_N
Y58	EMMC_CLK	EMMC_CLK	EMMC_CLK
V58	EMMC_D0	EMMC_D0	EMMC_D0
T58	EMMC_D1	EMMC_D1	EMMC_D1
T59	EMMC_D2	EMMC_D2	EMMC_D2
V51	EMMC_D3	EMMC_D3	EMMC_D3
V52	EMMC_D4	EMMC_D4	EMMC_D4
Y49	EMMC_D5	EMMC_D5	EMMC_D5
V55	EMMC_D6	EMMC_D6	EMMC_D6
V57	EMMC_D7	EMMC_D7	EMMC_D7
Y51	EMMC_CMD	EMMC_CMD	EMMC_CMD
P58	GPIO_166	GPIO_166	GPIO_166
T52	GPIO_167	GPIO_167	GPIO_167
P57	GPIO_168	GPIO_168	GPIO_168
T54	GPIO_169	GPIO_169	GPIO_169
T55	GPIO_170	GPIO_170	GPIO_170
T57	GPIO_171	GPIO_171	GPIO_171
AB58	SDCARD_CLK	SDCARD_CLK	SDCARD_CLK
AC49	SDCARD_D0	SDCARD_D0	SDCARD_D0
AC48	SDCARD_D1	SDCARD_D1	SDCARD_D1
AC51	SDCARD_D2	SDCARD_D2	SDCARD_D2
AB51	SDCARD_D3	SDCARD_D3	SDCARD_D3
AB54	SDCARD_CD_N	SDCARD_CD_N	SDCARD_CD_N
AC52	SDCARD_CMD	SDCARD_CMD	SDCARD_CMD
AB55	SDCARD_LVL_WP	SDCARD_LVL_WP	SDCARD_LVL_WP
V54	EMMC_RCLK	EMMC_RCLK	EMMC_RCLK
P51	GPIO_183	GPIO_183	GPIO_183
R63	SMB_ALERT_N	SMB_ALERT_N	SMB_ALERT_N
T62	SMB_CLK	SMB_CLK	SMB_CLK
T61	SMB_DATA	SMB_DATA	SMB_DATA
AB62	LPC_SERIRQ	LPC_SERIRQ	LPC_SERIRQ
AB61	LPC_CLKOUT0	LPC_CLKOUT0	LPC_CLKOUT0
AA62	LPC_CLKOUT1	LPC_CLKOUT1	LPC_CLKOUT1
Y61	LPC_AD0	LPC_AD0	LPC_AD0

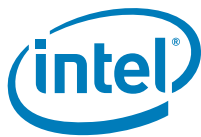
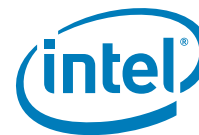


Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 14 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
Y62	LPC_AD1	LPC_AD1	LPC_AD1
W62	LPC_AD2	LPC_AD2	LPC_AD2
W63	LPC_AD3	LPC_AD3	LPC_AD3
V62	LPC_CLKRUN_N	LPC_CLKRUN_N	LPC_CLKRUN_N
V61	LPC_FRAME_N	LPC_FRAME_N	LPC_FRAME_N
AR62	LPSS_I2C0_SDA	LPSS_I2C0_SDA	LPSS_I2C0_SDA
AR63	LPSS_I2C0_SCL	LPSS_I2C0_SCL	LPSS_I2C0_SCL
AN62	LPSS_I2C1_SDA	LPSS_I2C1_SDA	LPSS_I2C1_SDA
AM61	LPSS_I2C1_SCL	LPSS_I2C1_SCL	LPSS_I2C1_SCL
AP59	LPSS_I2C2_SDA	LPSS_I2C2_SDA	LPSS_I2C2_SDA
AP58	LPSS_I2C2_SCL	LPSS_I2C2_SCL	LPSS_I2C2_SCL
AM62	LPSS_I2C3_SDA	LPSS_I2C3_SDA	LPSS_I2C3_SDA
AL62	LPSS_I2C3_SCL	LPSS_I2C3_SCL	LPSS_I2C3_SCL
AP52	LPSS_I2C4_SDA	LPSS_I2C4_SDA	LPSS_I2C4_SDA
AP54	LPSS_I2C4_SCL	LPSS_I2C4_SCL	LPSS_I2C4_SCL
AP49	LPSS_I2C5_SDA	LPSS_I2C5_SDA	LPSS_I2C5_SDA
AP51	LPSS_I2C5_SCL	LPSS_I2C5_SCL	LPSS_I2C5_SCL
AL63	LPSS_I2C6_SDA	LPSS_I2C6_SDA	LPSS_I2C6_SDA
AK61	LPSS_I2C6_SCL	LPSS_I2C6_SCL	LPSS_I2C6_SCL
AP62	LPSS_I2C7_SDA	LPSS_I2C7_SDA	LPSS_I2C7_SDA
AP61	LPSS_I2C7_SCL	LPSS_I2C7_SCL	LPSS_I2C7_SCL
AM48	ISH_GPIO_0	ISH_GPIO_0	ISH_GPIO_0
AK58	ISH_GPIO_1	ISH_GPIO_1	ISH_GPIO_1
AK51	ISH_GPIO_2	ISH_GPIO_2	ISH_GPIO_2
AM54	ISH_GPIO_3	ISH_GPIO_3	ISH_GPIO_3
AM51	ISH_GPIO_4	ISH_GPIO_4	ISH_GPIO_4
AM49	ISH_GPIO_5	ISH_GPIO_5	ISH_GPIO_5
AM57	ISH_GPIO_6	ISH_GPIO_6	ISH_GPIO_6
AM55	ISH_GPIO_7	ISH_GPIO_7	ISH_GPIO_7
AM52	ISH_GPIO_8	ISH_GPIO_8	ISH_GPIO_8
AK57	ISH_GPIO_9	ISH_GPIO_9	ISH_GPIO_9
AK62	PCIE_CLKREQ0_N	PCIE_CLKREQ0_N	PCIE_CLKREQ0_N
AH62	PCIE_CLKREQ1_N	PCIE_CLKREQ1_N	PCIE_CLKREQ1_N
AH61	PCIE_CLKREQ2_N	PCIE_CLKREQ2_N	PCIE_CLKREQ2_N
AJ62	PCIE_CLKREQ3_N	PCIE_CLKREQ3_N	PCIE_CLKREQ3_N
AG62	OSC_CLK_OUT_0	OSC_CLK_OUT_0	OSC_CLK_OUT_0
AF61	OSC_CLK_OUT_1	OSC_CLK_OUT_1	OSC_CLK_OUT_1

**Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 15 of 36)**

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
AG63	OSC_CLK_OUT_2	OSC_CLK_OUT_2	OSC_CLK_OUT_2
AE60	OSC_CLK_OUT_3	OSC_CLK_OUT_3	OSC_CLK_OUT_3
AF62	RSVD	RSVD	RSVD
AK49	PMU_AC_PRESENT	PMU_AC_PRESENT	PMU_AC_PRESENT
AH51	PMU_BATLOW_N	PMU_BATLOW_N	PMU_BATLOW_N
AG57	PMU_PLTRST_N	PMU_PLTRST_N	PMU_PLTRST_N
AK55	PMU_PWRBTN_N	PMU_PWRBTN_N	PMU_PWRBTN_N
AD62	PMU_RSTBTN_N	PMU_RSTBTN_N	PMU_RSTBTN_N
AD61	PMU_SLP_S0_N	PMU_SLP_S0_N	PMU_SLP_S0_N
AC62	PMU_SLP_S3_N	PMU_SLP_S3_N	PMU_SLP_S3_N
AK54	PMU_SLP_S4_N	PMU_SLP_S4_N	PMU_SLP_S4_N
AE62	PMU_SUSCLK	PMU_SUSCLK	PMU_SUSCLK
AG55	EMMC_PWR_EN_N	EMMC_PWR_EN_N	EMMC_PWR_EN_N
AG58	SUS_STAT_N	SUS_STAT_N	SUS_STAT_N
AC63	SUSPWRDNACK	SUSPWRDNACK	SUSPWRDNACK
C49	DDI0_DDC_SDA	DDI0_DDC_SDA	DDI0_DDC_SDA
B49	DDI0_DDC_SCL	DDI0_DDC_SCL	DDI0_DDC_SCL
C54	DDI1_DDC_SDA	DDI1_DDC_SDA	DDI1_DDC_SDA
A54	DDI1_DDC_SCL	DDI1_DDC_SCL	DDI1_DDC_SCL
B51	MIPI_I2C_SDA	MIPI_I2C_SDA	MIPI_I2C_SDA
C51	MIPI_I2C_SCL	MIPI_I2C_SCL	MIPI_I2C_SCL
C47	PNL0_VDDEN	PNL0_VDDEN	PNL0_VDDEN
B47	PNL0_BKLTEN	PNL0_BKLTEN	PNL0_BKLTEN
C46	PNL0_BKLCTL	PNL0_BKLCTL	PNL0_BKLCTL
C52	PNL1_VDDEN	PNL1_VDDEN	PNL1_VDDEN
B53	PNL1_BKLTEN	PNL1_BKLTEN	PNL1_BKLTEN
C53	PNL1_BKLCTL	PNL1_BKLCTL	PNL1_BKLCTL
A50	GPIO_199	GPIO_199	GPIO_199
C50	GPIO_200	GPIO_200	GPIO_200
M45	MDSI_A_TE	MDSI_A_TE	MDSI_A_TE
M43	MDSI_C_TE	MDSI_C_TE	MDSI_C_TE
B55	USB_OC0_N	USB_OC0_N	USB_OC0_N
C55	USB_OC1_N	USB_OC1_N	USB_OC1_N
L48	PMC_SPI_FS0	PMC_SPI_FS0	PMC_SPI_FS0
P48	PMC_SPI_FS1	PMC_SPI_FS1	PMC_SPI_FS1
M48	PMC_SPI_FS2	PMC_SPI_FS2	PMC_SPI_FS2
J50	PMC_SPI_RXD	PMC_SPI_RXD	PMC_SPI_RXD

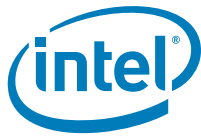


Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 16 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
H50	PMC_SPI_TXD	PMC_SPI_TXD	PMC_SPI_TXD
E52	PMC_SPI_CLK	PMC_SPI_CLK	PMC_SPI_CLK
H48	NCTF	NCTF	NCTF
F48	GPIO_223	GPIO_223	GPIO_223
M47	GPIO_213	GPIO_213	GPIO_213
L47	GPIO_214	GPIO_214	GPIO_214
P47	GPIO_215	GPIO_215	GPIO_215
J47	THERMTRIP_N	THERMTRIP_N	THERMTRIP_N
J45	GPIO_224	GPIO_224	GPIO_224
E47	PROCHOT_N	PROCHOT_N	PROCHOT_N
H45	PMIC_I2C_SCL	PMIC_I2C_SCL	PMIC_I2C_SCL
F47	PMIC_I2C_SDA	PMIC_I2C_SDA	PMIC_I2C_SDA
G62	AVS_I2S1_MCLK	AVS_I2S1_MCLK	AVS_I2S1_MCLK
H63	AVS_I2S1_BCLK	AVS_I2S1_BCLK	AVS_I2S1_BCLK
J62	AVS_I2S1_WS_SYNC	AVS_I2S1_WS_SYNC	AVS_I2S1_WS_SYNC
K61	AVS_I2S1_SDI	AVS_I2S1_SDI	AVS_I2S1_SDI
K62	AVS_I2S1_SDO	AVS_I2S1_SDO	AVS_I2S1_SDO
P54	AVS_DMIC_CLK_A1	AVS_DMIC_CLK_A1	AVS_DMIC_CLK_A1
P52	AVS_DMIC_CLK_B1	AVS_DMIC_CLK_B1	AVS_DMIC_CLK_B1
M54	AVS_DMIC_DATA_1	AVS_DMIC_DATA_1	AVS_DMIC_DATA_1
M55	AVS_DMIC_CLK_AB2	AVS_DMIC_CLK_AB2	AVS_DMIC_CLK_AB2
M52	AVS_DMIC_DATA_2	AVS_DMIC_DATA_2	AVS_DMIC_DATA_2
K58	AVS_I2S2_MCLK	AVS_I2S2_MCLK	AVS_I2S2_MCLK
H59	AVS_I2S2_BCLK	AVS_I2S2_BCLK	AVS_I2S2_BCLK
M57	AVS_I2S2_WS_SYNC	AVS_I2S2_WS_SYNC	AVS_I2S2_WS_SYNC
K59	AVS_I2S2_SDI	AVS_I2S2_SDI	AVS_I2S2_SDI
M58	AVS_I2S2_SDO	AVS_I2S2_SDO	AVS_I2S2_SDO
M62	AVS_I2S3_BCLK	AVS_I2S3_BCLK	AVS_I2S3_BCLK
M61	AVS_I2S3_WS_SYNC	AVS_I2S3_WS_SYNC	AVS_I2S3_WS_SYNC
L62	AVS_I2S3_SDI	AVS_I2S3_SDI	AVS_I2S3_SDI
L63	AVS_I2S3_SDO	AVS_I2S3_SDO	AVS_I2S3_SDO
B57	FST_SPI_CS0_N	FST_SPI_CS0_N	FST_SPI_CS0_N
C57	FST_SPI_CS1_N	FST_SPI_CS1_N	FST_SPI_CS1_N
A58	FST_SPI_MOSI_IO0	FST_SPI_MOSI_IO0	FST_SPI_MOSI_IO0
B58	FST_SPI_MISO_IO1	FST_SPI_MISO_IO1	FST_SPI_MISO_IO1
B60	FST_SPI_IO2	FST_SPI_IO2	FST_SPI_IO2
B61	FST_SPI_IO3	FST_SPI_IO3	FST_SPI_IO3

**Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 17 of 36)**

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
C56	FST_SPI_CLK	FST_SPI_CLK	FST_SPI_CLK
F54	SIO_SPI_0_CLK	SIO_SPI_0_CLK	SIO_SPI_0_CLK
F52	SIO_SPI_0_FS0	SIO_SPI_0_FS0	SIO_SPI_0_FS0
H52	SIO_SPI_0_FS1	SIO_SPI_0_FS1	SIO_SPI_0_FS1
H54	SIO_SPI_0_RXD	SIO_SPI_0_RXD	SIO_SPI_0_RXD
J52	SIO_SPI_0_TXD	SIO_SPI_0_TXD	SIO_SPI_0_TXD
F58	SIO_SPI_1_CLK	SIO_SPI_1_CLK	SIO_SPI_1_CLK
K55	SIO_SPI_1_FS0	SIO_SPI_1_FS0	SIO_SPI_1_FS0
F61	SIO_SPI_1_FS1	SIO_SPI_1_FS1	SIO_SPI_1_FS1
H57	SIO_SPI_1_RXD	SIO_SPI_1_RXD	SIO_SPI_1_RXD
H58	SIO_SPI_1_TXD	SIO_SPI_1_TXD	SIO_SPI_1_TXD
F62	SIO_SPI_2_CLK	SIO_SPI_2_CLK	SIO_SPI_2_CLK
D61	SIO_SPI_2_FS0	SIO_SPI_2_FS0	SIO_SPI_2_FS0
E56	SIO_SPI_2_FS1	SIO_SPI_2_FS1	SIO_SPI_2_FS1
D59	SIO_SPI_2_FS2	SIO_SPI_2_FS2	SIO_SPI_2_FS2
C62	SIO_SPI_2_RXD	SIO_SPI_2_RXD	SIO_SPI_2_RXD
E62	SIO_SPI_2_TXD	SIO_SPI_2_TXD	SIO_SPI_2_TXD
A38	GPIO_0	GPIO_0	GPIO_0
B33	GPIO_1	GPIO_1	GPIO_1
C39	GPIO_2	GPIO_2	GPIO_2
B39	GPIO_3	GPIO_3	GPIO_3
B35	GPIO_4	GPIO_4	GPIO_4
A34	GPIO_5	GPIO_5	GPIO_5
B31	GPIO_6	GPIO_6	GPIO_6
H39	GPIO_7	GPIO_7	GPIO_7
B29	GPIO_8	GPIO_8	GPIO_8
A30	GPIO_9	GPIO_9	GPIO_9
L39	GPIO_10	GPIO_10	GPIO_10
C34	GPIO_11	GPIO_11	GPIO_11
E39	GPIO_12	GPIO_12	GPIO_12
C30	GPIO_13	GPIO_13	GPIO_13
C38	GPIO_14	GPIO_14	GPIO_14
F39	GPIO_15	GPIO_15	GPIO_15
C36	GPIO_16	GPIO_16	GPIO_16
C35	GPIO_17	GPIO_17	GPIO_17
J39	GPIO_18	GPIO_18	GPIO_18
C33	GPIO_19	GPIO_19	GPIO_19

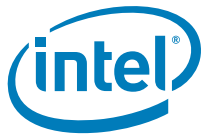


Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 18 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
B27	GPIO_20	GPIO_20	GPIO_20
C26	GPIO_21	GPIO_21	GPIO_21
A26	GPIO_22	GPIO_22	GPIO_22
B25	GPIO_23	GPIO_23	GPIO_23
C25	GPIO_24	GPIO_24	GPIO_24
C27	GPIO_25	GPIO_25	GPIO_25
C31	GPIO_26	GPIO_26	GPIO_26
C29	GPIO_27	GPIO_27	GPIO_27
B37	GPIO_28	GPIO_28	GPIO_28
H35	GPIO_29	GPIO_29	GPIO_29
C37	GPIO_30	GPIO_30	GPIO_30
H34	GPIO_31	GPIO_31	GPIO_31
F35	GPIO_32	GPIO_32	GPIO_32
F34	GPIO_33	GPIO_33	GPIO_33
B41	PWM0	PWM0	PWM0
C41	PWM1	PWM1	PWM1
F41	PWM2	PWM2	PWM2
E41	PWM3	PWM3	PWM3
C45	LPSS_UART0_RXD	LPSS_UART0_RXD	LPSS_UART0_RXD
B45	LPSS_UART0_TXD	LPSS_UART0_TXD	LPSS_UART0_TXD
A46	LPSS_UART0_RTS_N	LPSS_UART0_RTS_N	LPSS_UART0_RTS_N
C44	LPSS_UART0_CTS_N	LPSS_UART0_CTS_N	LPSS_UART0_CTS_N
C43	LPSS_UART1_RXD	LPSS_UART1_RXD	LPSS_UART1_RXD
B43	LPSS_UART1_TXD	LPSS_UART1_TXD	LPSS_UART1_TXD
A42	LPSS_UART1_RTS_N	LPSS_UART1_RTS_N	LPSS_UART1_RTS_N
C42	LPSS_UART1_CTS_N	LPSS_UART1_CTS_N	LPSS_UART1_CTS_N
J41	LPSS_UART2_RXD	LPSS_UART2_RXD	LPSS_UART2_RXD
H41	LPSS_UART2_TXD	LPSS_UART2_TXD	LPSS_UART2_TXD
L41	LPSS_UART2_RTS_N	LPSS_UART2_RTS_N	LPSS_UART2_RTS_N
M41	LPSS_UART2_CTS_N	LPSS_UART2_CTS_N	LPSS_UART2_CTS_N
L37	GP_CAMERASB0	GP_CAMERASB0	GP_CAMERASB0
P34	GP_CAMERASB1	GP_CAMERASB1	GP_CAMERASB1
J34	GP_CAMERASB2	GP_CAMERASB2	GP_CAMERASB2
H30	GP_CAMERASB3	GP_CAMERASB3	GP_CAMERASB3
M37	GP_CAMERASB4	GP_CAMERASB4	GP_CAMERASB4
F30	GP_CAMERASB5	GP_CAMERASB5	GP_CAMERASB5
R35	GP_CAMERASB6	GP_CAMERASB6	GP_CAMERASB6

**Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 19 of 36)**

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
L34	GP_CAMERASB7	GP_CAMERASB7	GP_CAMERASB7
M34	GP_CAMERASB8	GP_CAMERASB8	GP_CAMERASB8
M35	GP_CAMERASB9	GP_CAMERASB9	GP_CAMERASB9
R34	GP_CAMERASB10	GP_CAMERASB10	GP_CAMERASB10
E30	GP_CAMERASB11	GP_CAMERASB11	GP_CAMERASB11
B23	JTAG_TCK	JTAG_TCK	JTAG_TCK
C24	JTAG_TRST_N	JTAG_TRST_N	JTAG_TRST_N
C23	JTAG_TMS	JTAG_TMS	JTAG_TMS
C22	JTAG_TDI	JTAG_TDI	JTAG_TDI
B19	JTAG_PMODE	JTAG_PMODE	JTAG_PMODE
C20	JTAG_PREQ_N	JTAG_PREQ_N	JTAG_PREQ_N
B21	JTAGX	JTAGX	JTAGX
C21	JTAG_PRDY_N	JTAG_PRDY_N	JTAG_PRDY_N
A22	JTAG_TDO	JTAG_TDO	JTAG_TDO
P30	GPIO_216	GPIO_216	GPIO_216
M29	GPIO_217	GPIO_217	GPIO_217
M30	GPIO_218	GPIO_218	GPIO_218
L30	RSVD	RSVD	RSVD
B17	SVID0_ALERT_B	SVID0_ALERT_B	SVID0_ALERT_B
C18	SVID0_DATA	SVID0_DATA	SVID0_DATA
C17	SVID0_CLK	SVID0_CLK	SVID0_CLK
R29	VSS	VSS	VSS
A12	VSS	VSS	VSS
A16	VSS	VSS	VSS
A20	VSS	VSS	VSS
A24	VSS	VSS	VSS
A28	VSS	VSS	VSS
A32	VSS	VSS	VSS
A36	VSS	VSS	VSS
A40	VSS	VSS	VSS
A44	VSS	VSS	VSS
A48	VSS	VSS	VSS
A5	VSS	VSS	VSS
A52	VSS	VSS	VSS
A56	VSS	VSS	VSS
A62	VSS	VSS	VSS
A9	VSS	VSS	VSS

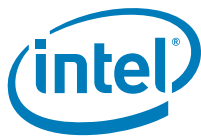


Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 20 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
AA1	VSS	VSS	VSS
AA2	VSS	VSS	VSS
AA27	VSS	VSS	VSS
AA34	VSS	VSS	VSS
AA41	VSS	VSS	VSS
AA63	VSS	VSS	VSS
AB10	VSS	VSS	VSS
AB12	VSS	VSS	VSS
AB16	VSS	VSS	VSS
AB48	VSS	VSS	VSS
AB5	VSS	VSS	VSS
AB52	VSS	VSS	VSS
AB57	VSS	VSS	VSS
AB59	VSS	VSS	VSS
AB9	VSS	VSS	VSS
AC18	VSS	VSS	VSS
AC27	VSS	VSS	VSS
AC34	VSS	VSS	VSS
AC39	VSS	VSS	VSS
AE1	VSS	VSS	VSS
AE10	VSS	VSS	VSS
AE11	VSS	VSS	VSS
AE13	VSS	VSS	VSS
AE14	VSS	VSS	VSS
AE16	VSS	VSS	VSS
AE17	VSS	VSS	VSS
AE2	VSS	VSS	VSS
AE23	VSS	VSS	VSS
AE27	VSS	VSS	VSS
AE34	VSS	VSS	VSS
AE39	VSS	VSS	VSS
AE4	VSS	VSS	VSS
AE41	VSS	VSS	VSS
AE47	VSS	VSS	VSS
AE48	VSS	VSS	VSS
AE5	VSS	VSS	VSS
AE50	VSS	VSS	VSS

**Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 21 of 36)**

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
AE51	VSS	VSS	VSS
AE53	VSS	VSS	VSS
AE54	VSS	VSS	VSS
AE56	VSS	VSS	VSS
AE57	VSS	VSS	VSS
AE59	VSS	VSS	VSS
AE63	VSS	VSS	VSS
AE7	VSS	VSS	VSS
AE8	VSS	VSS	VSS
AG13	VSS	VSS	VSS
AG18	VSS	VSS	VSS
AG23	VSS	VSS	VSS
AG27	VSS	VSS	VSS
AG34	VSS	VSS	VSS
AG37	VSS	VSS	VSS
AG39	VSS	VSS	VSS
AG41	VSS	VSS	VSS
AG42	VSS	VSS	VSS
AG44	VSS	VSS	VSS
AG46	VSS	VSS	VSS
AH15	VSS	VSS	VSS
AH16	VSS	VSS	VSS
AH48	VSS	VSS	VSS
AH5	VSS	VSS	VSS
AH52	VSS	VSS	VSS
AH54	VSS	VSS	VSS
AH55	VSS	VSS	VSS
AH57	VSS	VSS	VSS
AH58	VSS	VSS	VSS
AH59	VSS	VSS	VSS
AH6	VSS	VSS	VSS
AH7	VSS	VSS	VSS
AJ1	VSS	VSS	VSS
AJ18	VSS	VSS	VSS
AJ2	VSS	VSS	VSS
AJ23	VSS	VSS	VSS
AJ27	VSS	VSS	VSS

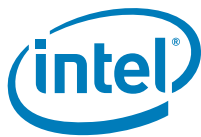


Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 22 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
AJ34	VSS	VSS	VSS
AJ36	VSS	VSS	VSS
AJ63	VSS	VSS	VSS
AK10	VSS	VSS	VSS
AK12	VSS	VSS	VSS
AK18	VSS	VSS	VSS
AK23	VSS	VSS	VSS
AK27	VSS	VSS	VSS
AK36	VSS	VSS	VSS
AK48	VSS	VSS	VSS
AK5	VSS	VSS	VSS
AK52	VSS	VSS	VSS
AK59	VSS	VSS	VSS
AK9	VSS	VSS	VSS
AM18	VSS	VSS	VSS
AM22	VSS	VSS	VSS
AM27	VSS	VSS	VSS
AM34	VSS	VSS	VSS
AM36	VSS	VSS	VSS
AM39	VSS	VSS	VSS
AM46	VSS	VSS	VSS
AN1	VSS	VSS	VSS
AN10	VSS	VSS	VSS
AN11	VSS	VSS	VSS
AN13	VSS	VSS	VSS
AN14	VSS	VSS	VSS
AN16	VSS	VSS	VSS
AN17	VSS	VSS	VSS
AN2	VSS	VSS	VSS
AN25	VSS	VSS	VSS
AN27	VSS	VSS	VSS
AN28	VSS	VSS	VSS
AN30	VSS	VSS	VSS
AN34	VSS	VSS	VSS
AN36	VSS	VSS	VSS
AN37	VSS	VSS	VSS
AN39	VSS	VSS	VSS

**Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 23 of 36)**

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
AN47	VSS	VSS	VSS
AN48	VSS	VSS	VSS
AN5	VSS	VSS	VSS
AN50	VSS	VSS	VSS
AN51	VSS	VSS	VSS
AN53	VSS	VSS	VSS
AN54	VSS	VSS	VSS
AN56	VSS	VSS	VSS
AN57	VSS	VSS	VSS
AN59	VSS	VSS	VSS
AN63	VSS	VSS	VSS
AN7	VSS	VSS	VSS
AN8	VSS	VSS	VSS
AP55	VSS	VSS	VSS
AP9	VSS	VSS	VSS
AR19	VSS	VSS	VSS
AR32	VSS	VSS	VSS
AR45	VSS	VSS	VSS
AT12	VSS	VSS	VSS
AT16	VSS	VSS	VSS
AT19	VSS	VSS	VSS
AT2	VSS	VSS	VSS
AT25	VSS	VSS	VSS
AT29	VSS	VSS	VSS
AT3	VSS	VSS	VSS
AT35	VSS	VSS	VSS
AT39	VSS	VSS	VSS
AT45	VSS	VSS	VSS
AT48	VSS	VSS	VSS
AT52	VSS	VSS	VSS
AT57	VSS	VSS	VSS
AT61	VSS	VSS	VSS
AT62	VSS	VSS	VSS
AT7	VSS	VSS	VSS
AU32	VSS	VSS	VSS
AV19	VSS	VSS	VSS
AV2	VSS	VSS	VSS

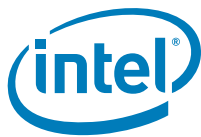


Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 24 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
AV21	VSS	VSS	VSS
AV23	VSS	VSS	VSS
AV29	VSS	VSS	VSS
AV3	VSS	VSS	VSS
AV32	VSS	VSS	VSS
AV35	VSS	VSS	VSS
AV41	VSS	VSS	VSS
AV43	VSS	VSS	VSS
AV45	VSS	VSS	VSS
AV55	VSS	VSS	VSS
AV61	VSS	VSS	VSS
AV62	VSS	VSS	VSS
AV9	VSS	VSS	VSS
AW14	VSS	VSS	VSS
AW30	VSS	VSS	VSS
AW34	VSS	VSS	VSS
AW50	VSS	VSS	VSS
AY10	VSS	VSS	VSS
AY32	VSS	VSS	VSS
AY54	VSS	VSS	VSS
AY58	VSS	VSS	VSS
AY6	VSS	VSS	VSS
B2	VSS	VSS	VSS
B3	VSS	VSS	VSS
B62	VSS	VSS	VSS
B63	VSS	VSS	VSS
B9	VSS	VSS	VSS
BA1	VSS	VSS	VSS
BA12	VSS	VSS	VSS
BA16	VSS	VSS	VSS
BA17	VSS	VSS	VSS
BA2	VSS	VSS	VSS
BA21	VSS	VSS	VSS
BA25	VSS	VSS	VSS
BA27	VSS	VSS	VSS
BA29	VSS	VSS	VSS
BA32	VSS	VSS	VSS

**Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 25 of 36)**

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
BA35	VSS	VSS	VSS
BA37	VSS	VSS	VSS
BA39	VSS	VSS	VSS
BA43	VSS	VSS	VSS
BA47	VSS	VSS	VSS
BA48	VSS	VSS	VSS
BA52	VSS	VSS	VSS
BA62	VSS	VSS	VSS
BA63	VSS	VSS	VSS
BB19	VSS	VSS	VSS
BB25	VSS	VSS	VSS
BB3	VSS	VSS	VSS
BB39	VSS	VSS	VSS
BB45	VSS	VSS	VSS
BB61	VSS	VSS	VSS
BC32	VSS	VSS	VSS
BD3	VSS	VSS	VSS
BD32	VSS	VSS	VSS
BD56	VSS	VSS	VSS
BD61	VSS	VSS	VSS
BD8	VSS	VSS	VSS
BE1	VSS	VSS	VSS
BE10	VSS	VSS	VSS
BE12	VSS	VSS	VSS
BE16	VSS	VSS	VSS
BE17	VSS	VSS	VSS
BE21	VSS	VSS	VSS
BE27	VSS	VSS	VSS
BE29	VSS	VSS	VSS
BE35	VSS	VSS	VSS
BE37	VSS	VSS	VSS
BE43	VSS	VSS	VSS
BE47	VSS	VSS	VSS
BE48	VSS	VSS	VSS
BE52	VSS	VSS	VSS
BE54	VSS	VSS	VSS
BE63	VSS	VSS	VSS

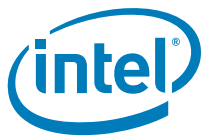


Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 26 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
BF3	VSS	VSS	VSS
BF32	VSS	VSS	VSS
BF61	VSS	VSS	VSS
BG19	VSS	VSS	VSS
BG23	VSS	VSS	VSS
BG29	VSS	VSS	VSS
BG32	VSS	VSS	VSS
BG35	VSS	VSS	VSS
BG41	VSS	VSS	VSS
BG45	VSS	VSS	VSS
BH1	VSS	VSS	VSS
BH2	VSS	VSS	VSS
BH21	VSS	VSS	VSS
BH25	VSS	VSS	VSS
BH39	VSS	VSS	VSS
BH43	VSS	VSS	VSS
BH62	VSS	VSS	VSS
BH63	VSS	VSS	VSS
BJ10	VSS	VSS	VSS
BJ14	VSS	VSS	VSS
BJ18	VSS	VSS	VSS
BJ28	VSS	VSS	VSS
BJ32	VSS	VSS	VSS
BJ36	VSS	VSS	VSS
BJ4	VSS	VSS	VSS
BJ46	VSS	VSS	VSS
BJ50	VSS	VSS	VSS
BJ54	VSS	VSS	VSS
BJ56	VSS	VSS	VSS
BJ60	VSS	VSS	VSS
BJ8	VSS	VSS	VSS
C12	VSS	VSS	VSS
C16	VSS	VSS	VSS
C28	VSS	VSS	VSS
C32	VSS	VSS	VSS
C40	VSS	VSS	VSS
C48	VSS	VSS	VSS

**Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 27 of 36)**

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
D32	VSS	VSS	VSS
D58	VSS	VSS	VSS
D6	VSS	VSS	VSS
E12	VSS	VSS	VSS
E14	VSS	VSS	VSS
E19	VSS	VSS	VSS
E27	VSS	VSS	VSS
E4	VSS	VSS	VSS
E54	VSS	VSS	VSS
F10	VSS	VSS	VSS
F21	VSS	VSS	VSS
F3	VSS	VSS	VSS
F32	VSS	VSS	VSS
F37	VSS	VSS	VSS
F43	VSS	VSS	VSS
F45	VSS	VSS	VSS
F50	VSS	VSS	VSS
F56	VSS	VSS	VSS
F59	VSS	VSS	VSS
F63	VSS	VSS	VSS
G1	VSS	VSS	VSS
G32	VSS	VSS	VSS
H17	VSS	VSS	VSS
H23	VSS	VSS	VSS
H29	VSS	VSS	VSS
H3	VSS	VSS	VSS
H37	VSS	VSS	VSS
H47	VSS	VSS	VSS
H61	VSS	VSS	VSS
H7	VSS	VSS	VSS
J12	VSS	VSS	VSS
J14	VSS	VSS	VSS
J19	VSS	VSS	VSS
J27	VSS	VSS	VSS
J30	VSS	VSS	VSS
J32	VSS	VSS	VSS
J35	VSS	VSS	VSS

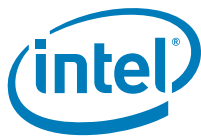


Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 28 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
J37	VSS	VSS	VSS
J48	VSS	VSS	VSS
J63	VSS	VSS	VSS
K32	VSS	VSS	VSS
K5	VSS	VSS	VSS
K54	VSS	VSS	VSS
K57	VSS	VSS	VSS
K6	VSS	VSS	VSS
L21	VSS	VSS	VSS
L27	VSS	VSS	VSS
L29	VSS	VSS	VSS
L35	VSS	VSS	VSS
L43	VSS	VSS	VSS
L45	VSS	VSS	VSS
L50	VSS	VSS	VSS
M14	VSS	VSS	VSS
M21	VSS	VSS	VSS
M27	VSS	VSS	VSS
M3	VSS	VSS	VSS
M32	VSS	VSS	VSS
M50	VSS	VSS	VSS
M59	VSS	VSS	VSS
M9	VSS	VSS	VSS
N1	VSS	VSS	VSS
N32	VSS	VSS	VSS
N63	VSS	VSS	VSS
P13	VSS	VSS	VSS
P19	VSS	VSS	VSS
P35	VSS	VSS	VSS
P37	VSS	VSS	VSS
P41	VSS	VSS	VSS
P43	VSS	VSS	VSS
P45	VSS	VSS	VSS
P5	VSS	VSS	VSS
P55	VSS	VSS	VSS
P59	VSS	VSS	VSS
P9	VSS	VSS	VSS

**Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 29 of 36)**

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
R23	VSS	VSS	VSS
R32	VSS	VSS	VSS
T49	VSS	VSS	VSS
U1	VSS	VSS	VSS
U10	VSS	VSS	VSS
U11	VSS	VSS	VSS
U13	VSS	VSS	VSS
U14	VSS	VSS	VSS
U16	VSS	VSS	VSS
U17	VSS	VSS	VSS
U18	VSS	VSS	VSS
U2	VSS	VSS	VSS
U27	VSS	VSS	VSS
U34	VSS	VSS	VSS
U5	VSS	VSS	VSS
U50	VSS	VSS	VSS
U51	VSS	VSS	VSS
U53	VSS	VSS	VSS
U54	VSS	VSS	VSS
U56	VSS	VSS	VSS
U57	VSS	VSS	VSS
U59	VSS	VSS	VSS
U62	VSS	VSS	VSS
U63	VSS	VSS	VSS
U7	VSS	VSS	VSS
U8	VSS	VSS	VSS
V20	VSS	VSS	VSS
V27	VSS	VSS	VSS
V34	VSS	VSS	VSS
V42	VSS	VSS	VSS
Y12	VSS	VSS	VSS
Y16	VSS	VSS	VSS
Y22	VSS	VSS	VSS
Y27	VSS	VSS	VSS
Y34	VSS	VSS	VSS
Y42	VSS	VSS	VSS
Y46	VSS	VSS	VSS

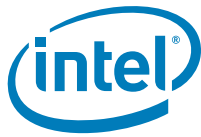


Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 30 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
Y48	VSS	VSS	VSS
Y5	VSS	VSS	VSS
Y52	VSS	VSS	VSS
Y54	VSS	VSS	VSS
Y55	VSS	VSS	VSS
Y57	VSS	VSS	VSS
Y59	VSS	VSS	VSS
Y6	VSS	VSS	VSS
Y7	VSS	VSS	VSS
AJ44	RSVD	RSVD	RSVD
AJ37	VNN_SVID	VNN_SVID	VNN_SVID
AJ39	VNN_SVID	VNN_SVID	VNN_SVID
AJ41	VNN_SVID	VNN_SVID	VNN_SVID
AJ42	VNN_SVID	VNN_SVID	VNN_SVID
AJ46	VNN_SVID	VNN_SVID	VNN_SVID
AK37	VNN_SVID	VNN_SVID	VNN_SVID
AK39	VNN_SVID	VNN_SVID	VNN_SVID
AK41	VNN_SVID	VNN_SVID	VNN_SVID
AK42	VNN_SVID	VNN_SVID	VNN_SVID
AK44	VNN_SVID	VNN_SVID	VNN_SVID
AK46	VNN_SVID	VNN_SVID	VNN_SVID
AM44	VNN_SVID	VNN_SVID	VNN_SVID
AG48	VNN_SENSE	VNN_SENSE	VNN_SENSE
BG63	RSVD	RSVD	RSVD
AC41	VCC_3P3V_A	VCC_3P3V_A	VCC_3P3V_A
AA42	VCC_3P3V_A	VCC_3P3V_A	VCC_3P3V_A
Y44	VCC_3P3V_A	VCC_3P3V_A	VCC_3P3V_A
V44	VCC_3P3V_A	VCC_3P3V_A	VCC_3P3V_A
V46	VCC_3P3V_A	VCC_3P3V_A	VCC_3P3V_A
AJ25	VCC_3P3V_A	VCC_3P3V_A	VCC_3P3V_A
AK25	VCC_3P3V_A	VCC_3P3V_A	VCC_3P3V_A
AC22	RSVD	RSVD	RSVD
AC20	RSVD	RSVD	RSVD
AG20	VDD2_1P24_USB2	VDD2_1P24_USB2	VDD2_1P24_USB2
AJ20	VDD2_1P24_AUD_ISH_PL PLL	VDD2_1P24_AUD_ISH_PL L	VDD2_1P24_AUD_ISH_PLL
AJ22	VDD2_1P24_AUD_ISH_PL PLL	VDD2_1P24_AUD_ISH_PL L	VDD2_1P24_AUD_ISH_PLL

**Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 31 of 36)**

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
AE18	VDD2_1P24	VDD2_1P24	VDD2_1P24
AE20	VDD2_1P24	VDD2_1P24	VDD2_1P24
AE22	VDD2_1P24	VDD2_1P24	VDD2_1P24
AG22	VDD2_1P24	VDD2_1P24	VDD2_1P24
AM20	VDD2_1P24_CPU	VDD2_1P24_CPU	VDD2_1P24_CPU
AM28	VDD2_1P24_CPU	VDD2_1P24_CPU	VDD2_1P24_CPU
AM37	VDD2_1P24_CPU	VDD2_1P24_CPU	VDD2_1P24_CPU
AK20	VDD2_1P24_CPU	VDD2_1P24_CPU	VDD2_1P24_CPU
AA18	VDD2_1P24_DSI_CSI	VDD2_1P24_DSI_CSI	VDD2_1P24_DSI_CSI
AA20	VDD2_1P24_DSI_CSI	VDD2_1P24_DSI_CSI	VDD2_1P24_DSI_CSI
AK22	VDD2_1P24_AUD_ISH_PL PLL	VDD2_1P24_AUD_ISH_PL L	VDD2_1P24_AUD_ISH_PL LL
V48	RSVD	RSVD	RSVD
AA46	VCC_1P8V_A	VCC_1P8V_A	VCC_1P8V_A
AC46	VCC_1P8V_A	VCC_1P8V_A	VCC_1P8V_A
AE44	VCC_1P8V_A	VCC_1P8V_A	VCC_1P8V_A
AE42	VCC_1P8V_A	VCC_1P8V_A	VCC_1P8V_A
AC42	VCC_1P8V_A	VCC_1P8V_A	VCC_1P8V_A
AC44	VCC_1P8V_A	VCC_1P8V_A	VCC_1P8V_A
AE46	VCC_1P8V_A	VCC_1P8V_A	VCC_1P8V_A
AG25	VCC_1P8V_A	VCC_1P8V_A	VCC_1P8V_A
AA36	VCC_VCGI	VCC_VCGI	VCC_VCGI
AA37	VCC_VCGI	VCC_VCGI	VCC_VCGI
AA39	VCC_VCGI	VCC_VCGI	VCC_VCGI
AC36	VCC_VCGI	VCC_VCGI	VCC_VCGI
AC37	VCC_VCGI	VCC_VCGI	VCC_VCGI
AE36	VCC_VCGI	VCC_VCGI	VCC_VCGI
AE37	VCC_VCGI	VCC_VCGI	VCC_VCGI
AG36	VCC_VCGI	VCC_VCGI	VCC_VCGI
E43	VCC_VCGI	VCC_VCGI	VCC_VCGI
E45	VCC_VCGI	VCC_VCGI	VCC_VCGI
E48	VCC_VCGI	VCC_VCGI	VCC_VCGI
E50	VCC_VCGI	VCC_VCGI	VCC_VCGI
R45	VCC_VCGI	VCC_VCGI	VCC_VCGI
R47	VCC_VCGI	VCC_VCGI	VCC_VCGI
U36	VCC_VCGI	VCC_VCGI	VCC_VCGI
U37	VCC_VCGI	VCC_VCGI	VCC_VCGI

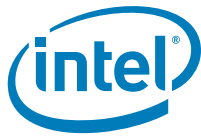


Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 32 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
U39	VCC_VCGI	VCC_VCGI	VCC_VCGI
U41	VCC_VCGI	VCC_VCGI	VCC_VCGI
U42	VCC_VCGI	VCC_VCGI	VCC_VCGI
U44	VCC_VCGI	VCC_VCGI	VCC_VCGI
U46	VCC_VCGI	VCC_VCGI	VCC_VCGI
U47	VCC_VCGI	VCC_VCGI	VCC_VCGI
U48	VCC_VCGI	VCC_VCGI	VCC_VCGI
V36	VCC_VCGI	VCC_VCGI	VCC_VCGI
V37	VCC_VCGI	VCC_VCGI	VCC_VCGI
V39	VCC_VCGI	VCC_VCGI	VCC_VCGI
V41	VCC_VCGI	VCC_VCGI	VCC_VCGI
Y36	VCC_VCGI	VCC_VCGI	VCC_VCGI
Y37	VCC_VCGI	VCC_VCGI	VCC_VCGI
Y39	VCC_VCGI	VCC_VCGI	VCC_VCGI
Y41	VCC_VCGI	VCC_VCGI	VCC_VCGI
AA28	VCC_VCGI	VCC_VCGI	VCC_VCGI
AA30	VCC_VCGI	VCC_VCGI	VCC_VCGI
AA32	VCC_VCGI	VCC_VCGI	VCC_VCGI
AC28	VCC_VCGI	VCC_VCGI	VCC_VCGI
AC30	VCC_VCGI	VCC_VCGI	VCC_VCGI
AC32	VCC_VCGI	VCC_VCGI	VCC_VCGI
AE28	VCC_VCGI	VCC_VCGI	VCC_VCGI
AE30	VCC_VCGI	VCC_VCGI	VCC_VCGI
AE32	VCC_VCGI	VCC_VCGI	VCC_VCGI
AG28	VCC_VCGI	VCC_VCGI	VCC_VCGI
AG30	VCC_VCGI	VCC_VCGI	VCC_VCGI
AG32	VCC_VCGI	VCC_VCGI	VCC_VCGI
AJ28	VCC_VCGI	VCC_VCGI	VCC_VCGI
AJ30	VCC_VCGI	VCC_VCGI	VCC_VCGI
AJ32	VCC_VCGI	VCC_VCGI	VCC_VCGI
AK28	VCC_VCGI	VCC_VCGI	VCC_VCGI
AK30	VCC_VCGI	VCC_VCGI	VCC_VCGI
AK32	VCC_VCGI	VCC_VCGI	VCC_VCGI
AK34	VCC_VCGI	VCC_VCGI	VCC_VCGI
AM30	VCC_VCGI	VCC_VCGI	VCC_VCGI
E29	VCC_VCGI	VCC_VCGI	VCC_VCGI
E35	VCC_VCGI	VCC_VCGI	VCC_VCGI

**Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 33 of 36)**

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
E37	VCC_VCGI	VCC_VCGI	VCC_VCGI
F29	VCC_VCGI	VCC_VCGI	VCC_VCGI
U28	VCC_VCGI	VCC_VCGI	VCC_VCGI
U30	VCC_VCGI	VCC_VCGI	VCC_VCGI
U32	VCC_VCGI	VCC_VCGI	VCC_VCGI
V28	VCC_VCGI	VCC_VCGI	VCC_VCGI
V30	VCC_VCGI	VCC_VCGI	VCC_VCGI
V32	VCC_VCGI	VCC_VCGI	VCC_VCGI
Y28	VCC_VCGI	VCC_VCGI	VCC_VCGI
Y30	VCC_VCGI	VCC_VCGI	VCC_VCGI
Y32	VCC_VCGI	VCC_VCGI	VCC_VCGI
BJ3	RSVD	RSVD	RSVD
BJ61	RSVD	RSVD	RSVD
AA44	VCCRTC_3P3V	VCCRTC_3P3V	VCCRTC_3P3V
D1	RSVD	RSVD	RSVD
AA25	VCCRAM_1P05	VCCRAM_1P05	VCCRAM_1P05
AC25	VCCRAM_1P05	VCCRAM_1P05	VCCRAM_1P05
AE25	VCCRAM_1P05	VCCRAM_1P05	VCCRAM_1P05
U22	VCCRAM_1P05	VCCRAM_1P05	VCCRAM_1P05
U23	VCCRAM_1P05	VCCRAM_1P05	VCCRAM_1P05
V22	VCCRAM_1P05	VCCRAM_1P05	VCCRAM_1P05
V23	VCCRAM_1P05	VCCRAM_1P05	VCCRAM_1P05
V25	VCCRAM_1P05	VCCRAM_1P05	VCCRAM_1P05
Y23	VCCRAM_1P05	VCCRAM_1P05	VCCRAM_1P05
Y25	VCCRAM_1P05	VCCRAM_1P05	VCCRAM_1P05
U25	VCCRAM_1P05	VCCRAM_1P05	VCCRAM_1P05
U20	VCCRAM_1P05	VCCRAM_1P05	VCCRAM_1P05
AA22	VCCRAM_1P05_IO	VCCRAM_1P05_IO	VCCRAM_1P05_IO
AC23	VCCRAM_1P05_IO	VCCRAM_1P05_IO	VCCRAM_1P05_IO
V18	VCCRAM_1P05_IO	VCCRAM_1P05_IO	VCCRAM_1P05_IO
Y18	VCCRAM_1P05_IO	VCCRAM_1P05_IO	VCCRAM_1P05_IO
Y20	VCCRAM_1P05_IO	VCCRAM_1P05_IO	VCCRAM_1P05_IO
P16	VCC_1P05_INT	VCC_1P05_INT	VCC_1P05_INT
T15	VCC_1P05_INT	VCC_1P05_INT	VCC_1P05_INT
T13	VCC_1P05_INT	VCC_1P05_INT	VCC_1P05_INT
AA23	VCCRAM_1P05_IO	VCCRAM_1P05_IO	VCCRAM_1P05_IO
AM23	VCCIOA	VCCIOA	VCCIOA

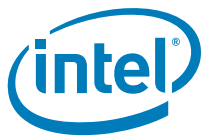


Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 34 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
AM25	VCCIOA	VCCIOA	VCCIOA
AM41	VCCIOA	VCCIOA	VCCIOA
AM42	VCCIOA	VCCIOA	VCCIOA
AN32	RSVD	RSVD	RSVD
AN18	VDDQ	VDDQ	VDDQ
AN20	VDDQ	VDDQ	VDDQ
AN22	VDDQ	VDDQ	VDDQ
AN23	VDDQ	VDDQ	VDDQ
AN41	VDDQ	VDDQ	VDDQ
AN42	VDDQ	VDDQ	VDDQ
AN44	VDDQ	VDDQ	VDDQ
AN46	VDDQ	VDDQ	VDDQ
AR17	VDDQ	VDDQ	VDDQ
AR47	VDDQ	VDDQ	VDDQ
AT13	VDDQ	VDDQ	VDDQ
AT17	VDDQ	VDDQ	VDDQ
AT47	VDDQ	VDDQ	VDDQ
AT51	VDDQ	VDDQ	VDDQ
AV14	VDDQ	VDDQ	VDDQ
AV50	VDDQ	VDDQ	VDDQ
AM32	RSVD	RSVD	RSVD
BJ62	RSVD	RSVD	RSVD
R43	VCC_VCGI_SENSE_N	VCC_VCGI_SENSE_N	VCC_VCGI_SENSE_N
R41	VCC_VCGI_SENSE_P	VCC_VCGI_SENSE_P	VCC_VCGI_SENSE_P
T51	NCTF	NCTF	NCTF
L14	NCTF	NCTF	NCTF
R19	NCTF	NCTF	NCTF
E6	NCTF	NCTF	NCTF
R17	NCTF	NCTF	NCTF
E3	NCTF	NCTF	NCTF
D4	NCTF	NCTF	NCTF
A60	NCTF	NCTF	NCTF
A61	NCTF	NCTF	NCTF
BJ2	NCTF	NCTF	NCTF
BG1	NCTF	NCTF	NCTF
P27	NCTF	NCTF	NCTF
A3	NCTF	NCTF	NCTF

**Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 35 of 36)**

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
M10	NCTF	NCTF	NCTF
B15	NCTF	NCTF	NCTF
M12	NCTF	NCTF	NCTF
C15	NCTF	NCTF	NCTF
F16	NCTF	NCTF	NCTF
J16	NCTF	NCTF	NCTF
D8	NCTF	NCTF	NCTF
E8	NCTF	NCTF	NCTF
H16	NCTF	NCTF	NCTF
C9	NCTF	NCTF	NCTF
F8	NCTF	NCTF	NCTF
E10	NCTF	NCTF	NCTF
E16	NCTF	NCTF	NCTF
F14	NCTF	NCTF	NCTF
F12	NCTF	NCTF	NCTF
H10	NCTF	NCTF	NCTF
H14	NCTF	NCTF	NCTF
H12	NCTF	NCTF	NCTF
A14	NCTF	NCTF	NCTF
C14	NCTF	NCTF	NCTF
M39	NCTF	NCTF	NCTF
P39	NCTF	NCTF	NCTF
R39	NCTF	NCTF	NCTF
R37	NCTF	NCTF	NCTF
C2	NCTF	NCTF	NCTF
J29	NCTF	NCTF	NCTF
P25	NCTF	NCTF	NCTF
R30	NCTF	NCTF	NCTF
C63	NCTF	NCTF	NCTF
E63	NCTF	NCTF	NCTF
D2	NCTF	NCTF	NCTF
AP57	NCTF	NCTF	NCTF
B13	NCTF	NCTF	NCTF
C13	NCTF	NCTF	NCTF
L16	NCTF	NCTF	NCTF
M16	NCTF	NCTF	NCTF
E23	NCTF	NCTF	NCTF



Table 6-1. SoC Pin Numbers - DDR3L, LPDDR3 and LPDDR4 (Sheet 36 of 36)

SoC Pin Numbers	DDR3L	LPDDR3	LPDDR4
F23	NCTF	NCTF	NCTF
R25	NCTF	NCTF	NCTF
AB49	NCTF	NCTF	NCTF
AC13	NCTF	NCTF	NCTF
AB13	NCTF	NCTF	NCTF
AM59	NCTF	NCTF	NCTF
AM58	NCTF	NCTF	NCTF



6.5 SoC X and Y Pin List

Table 6-2. SoC X and Y Pin List (Sheet 1 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
AA1	14814.17	-1854.2
AA2	14036.68	-1854.2
AA18	6299.2	-1447.8
AA20	5511.8	-1447.8
AA22	4724.4	-1447.8
AA23	3937	-1447.8
AA25	3149.6	-1447.8
AA27	2362.2	-1447.8
AA28	1574.8	-1447.8
AA30	787.4	-1447.8
AA32	0	-1447.8
AA34	-787.4	-1447.8
AA36	-1574.8	-1447.8
AA37	-2362.2	-1447.8
AA39	-3149.6	-1447.8
AA41	-3937	-1447.8
AA42	-4724.4	-1447.8
AA44	-5511.8	-1447.8
AA46	-6299.2	-1447.8
AA62	-14036.7	-1854.2
AA63	-14814.2	-1854.2
AB2	14413.87	-1390.65
AB3	13659.49	-1390.65
AB5	12999.09	-1397
AB6	12287.89	-1397
AB7	11576.69	-1397
AB9	10865.49	-1397
AB10	10154.29	-1397
AB12	9443.085	-1397
AB13	8731.885	-1397
AB15	8020.685	-1397
AB16	7309.485	-1397
AB48	-7309.49	-1397
AB49	-8020.69	-1397
AB51	-8731.89	-1397
AB52	-9443.09	-1397
AB54	-10154.3	-1397

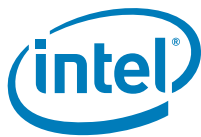


Table 6-2. SoC X and Y Pin List (Sheet 2 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
AB55	-10865.5	-1397
AB57	-11576.7	-1397
AB58	-12287.9	-1397
AB59	-12999.1	-1397
AB61	-13659.5	-1390.65
AB62	-14413.9	-1390.65
AC1	14814.17	-927.1
AC2	14036.68	-927.1
AC5	12999.09	-520.7
AC6	12287.89	-520.7
AC7	11576.69	-520.7
AC9	10865.49	-520.7
AC10	10154.29	-520.7
AC12	9443.085	-520.7
AC13	8731.885	-520.7
AC15	8020.685	-520.7
AC16	7309.485	-520.7
AC18	6299.2	-723.9
AC20	5511.8	-723.9
AC22	4724.4	-723.9
AC23	3937	-723.9
AC25	3149.6	-723.9
AC27	2362.2	-723.9
AC28	1574.8	-723.9
AC30	787.4	-723.9
AC32	0	-723.9
AC34	-787.4	-723.9
AC36	-1574.8	-723.9
AC37	-2362.2	-723.9
AC39	-3149.6	-723.9
AC41	-3937	-723.9
AC42	-4724.4	-723.9
AC44	-5511.8	-723.9
AC46	-6299.2	-723.9
AC48	-7309.49	-520.7
AC49	-8020.69	-520.7
AC51	-8731.89	-520.7
AC52	-9443.09	-520.7
AC54	-10154.3	-520.7



Table 6-2. SoC X and Y Pin List (Sheet 3 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
AC55	-10865.5	-520.7
AC57	-11576.7	-520.7
AC58	-12287.9	-520.7
AC59	-12999.1	-520.7
AC62	-14036.7	-927.1
AC63	-14814.2	-927.1
AD2	14413.87	-463.55
AD3	13659.49	-463.55
AD61	-13659.5	-463.55
AD62	-14413.9	-463.55
AE1	14814.17	0
AE2	14036.68	0
AE4	13284.84	0
AE5	12643.49	0
AE7	11932.29	0
AE8	11221.09	0
AE10	10509.89	0
AE11	9798.685	0
AE13	9087.485	0
AE14	8376.285	0
AE16	7665.085	0
AE17	6953.885	0
AE18	6299.2	0
AE20	5511.8	0
AE22	4724.4	0
AE23	3937	0
AE25	3149.6	0
AE27	2362.2	0
AE28	1574.8	0
AE30	787.4	0
AE32	0	0
AE34	-787.4	0
AE36	-1574.8	0
AE37	-2362.2	0
AE39	-3149.6	0
AE41	-3937	0
AE42	-4724.4	0
AE44	-5511.8	0
AE46	-6299.2	0

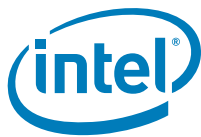


Table 6-2. SoC X and Y Pin List (Sheet 4 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
AE47	-6953.89	0
AE48	-7665.09	0
AE50	-8376.29	0
AE51	-9087.49	0
AE53	-9798.69	0
AE54	-10509.9	0
AE56	-11221.1	0
AE57	-11932.3	0
AE59	-12643.5	0
AE60	-13284.8	0
AE62	-14036.7	0
AE63	-14814.2	0
AF2	14413.87	463.55
AF3	13659.49	463.55
AF61	-13659.5	463.55
AF62	-14413.9	463.55
AG1	14814.17	927.1
AG2	14036.68	927.1
AG5	12999.09	520.7
AG6	12287.89	520.7
AG7	11576.69	520.7
AG9	10865.49	520.7
AG10	10154.29	520.7
AG12	9443.085	520.7
AG13	8731.885	520.7
AG15	8020.685	520.7
AG16	7309.485	520.7
AG18	6299.2	723.9
AG20	5511.8	723.9
AG22	4724.4	723.9
AG23	3937	723.9
AG25	3149.6	723.9
AG27	2362.2	723.9
AG28	1574.8	723.9
AG30	787.4	723.9
AG32	0	723.9
AG34	-787.4	723.9
AG36	-1574.8	723.9
AG37	-2362.2	723.9



Table 6-2. SoC X and Y Pin List (Sheet 5 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
AG39	-3149.6	723.9
AG41	-3937	723.9
AG42	-4724.4	723.9
AG44	-5511.8	723.9
AG46	-6299.2	723.9
AG48	-7309.49	520.7
AG49	-8020.69	520.7
AG51	-8731.89	520.7
AG52	-9443.09	520.7
AG54	-10154.3	520.7
AG55	-10865.5	520.7
AG57	-11576.7	520.7
AG58	-12287.9	520.7
AG59	-12999.1	520.7
AG62	-14036.7	927.1
AG63	-14814.2	927.1
AH2	14413.87	1390.65
AH3	13659.49	1390.65
AH5	12999.09	1397
AH6	12287.89	1397
AH7	11576.69	1397
AH9	10865.49	1397
AH10	10154.29	1397
AH12	9443.085	1397
AH13	8731.885	1397
AH15	8020.685	1397
AH16	7309.485	1397
AH48	-7309.49	1397
AH49	-8020.69	1397
AH51	-8731.89	1397
AH52	-9443.09	1397
AH54	-10154.3	1397
AH55	-10865.5	1397
AH57	-11576.7	1397
AH58	-12287.9	1397
AH59	-12999.1	1397
AH61	-13659.5	1390.65
AH62	-14413.9	1390.65
AJ1	14814.17	1854.2

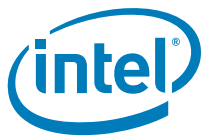


Table 6-2. SoC X and Y Pin List (Sheet 6 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
AJ2	14036.68	1854.2
AJ18	6299.2	1447.8
AJ20	5511.8	1447.8
AJ22	4724.4	1447.8
AJ23	3937	1447.8
AJ25	3149.6	1447.8
AJ27	2362.2	1447.8
AJ28	1574.8	1447.8
AJ30	787.4	1447.8
AJ32	0	1447.8
AJ34	-787.4	1447.8
AJ36	-1574.8	1447.8
AJ37	-2362.2	1447.8
AJ39	-3149.6	1447.8
AJ41	-3937	1447.8
AJ42	-4724.4	1447.8
AJ44	-5511.8	1447.8
AJ46	-6299.2	1447.8
AJ62	-14036.7	1854.2
AJ63	-14814.2	1854.2
AK2	14413.87	2317.75
AK3	13659.49	2317.75
AK5	12999.09	2349.5
AK6	12287.89	2349.5
AK7	11576.69	2349.5
AK9	10865.49	2349.5
AK10	10154.29	2349.5
AK12	9443.085	2349.5
AK13	8731.885	2349.5
AK15	8020.685	2349.5
AK16	7309.485	2349.5
AK18	6299.2	2171.7
AK20	5511.8	2171.7
AK22	4724.4	2171.7
AK23	3937	2171.7
AK25	3149.6	2171.7
AK27	2362.2	2171.7
AK28	1574.8	2171.7
AK30	787.4	2171.7



Table 6-2. SoC X and Y Pin List (Sheet 7 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
AK32	0	2171.7
AK34	-787.4	2171.7
AK36	-1574.8	2171.7
AK37	-2362.2	2171.7
AK39	-3149.6	2171.7
AK41	-3937	2171.7
AK42	-4724.4	2171.7
AK44	-5511.8	2171.7
AK46	-6299.2	2171.7
AK48	-7309.49	2349.5
AK49	-8020.69	2349.5
AK51	-8731.89	2349.5
AK52	-9443.09	2349.5
AK54	-10154.3	2349.5
AK55	-10865.5	2349.5
AK57	-11576.7	2349.5
AK58	-12287.9	2349.5
AK59	-12999.1	2349.5
AK61	-13659.5	2317.75
AK62	-14413.9	2317.75
AL1	14814.17	2781.3
AL2	14036.68	2781.3
AL62	-14036.7	2781.3
AL63	-14814.2	2781.3
AM2	14413.87	3244.85
AM3	13659.49	3244.85
AM5	12999.09	3225.8
AM6	12287.89	3225.8
AM7	11576.69	3225.8
AM9	10865.49	3225.8
AM10	10154.29	3225.8
AM12	9443.085	3225.8
AM13	8731.885	3225.8
AM15	8020.685	3225.8
AM16	7309.485	3225.8
AM18	6299.2	2895.6
AM20	5511.8	2895.6
AM22	4724.4	2895.6
AM23	3937	2895.6

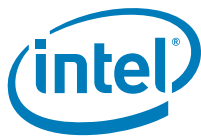


Table 6-2. SoC X and Y Pin List (Sheet 8 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
AM25	3149.6	2895.6
AM27	2362.2	2895.6
AM28	1574.8	2895.6
AM30	787.4	2895.6
AM32	0	2895.6
AM34	-787.4	2895.6
AM36	-1574.8	2895.6
AM37	-2362.2	2895.6
AM39	-3149.6	2895.6
AM41	-3937	2895.6
AM42	-4724.4	2895.6
AM44	-5511.8	2895.6
AM46	-6299.2	2895.6
AM48	-7309.49	3225.8
AM49	-8020.69	3225.8
AM51	-8731.89	3225.8
AM52	-9443.09	3225.8
AM54	-10154.3	3225.8
AM55	-10865.5	3225.8
AM57	-11576.7	3225.8
AM58	-12287.9	3225.8
AM59	-12999.1	3225.8
AM61	-13659.5	3244.85
AM62	-14413.9	3244.85
AN1	14814.17	3708.4
AN2	14036.68	3708.4
AN5	12643.49	3746.5
AN7	11932.29	3746.5
AN8	11221.09	3746.5
AN10	10509.89	3746.5
AN11	9798.685	3746.5
AN13	9087.485	3746.5
AN14	8376.285	3746.5
AN16	7665.085	3746.5
AN17	6953.885	3746.5
AN18	6299.2	3619.5
AN20	5511.8	3619.5
AN22	4724.4	3619.5
AN23	3937	3619.5



Table 6-2. SoC X and Y Pin List (Sheet 9 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
AN25	3149.6	3619.5
AN27	2362.2	3619.5
AN28	1574.8	3619.5
AN30	787.4	3619.5
AN32	0	3619.5
AN34	-787.4	3619.5
AN36	-1574.8	3619.5
AN37	-2362.2	3619.5
AN39	-3149.6	3619.5
AN41	-3937	3619.5
AN42	-4724.4	3619.5
AN44	-5511.8	3619.5
AN46	-6299.2	3619.5
AN47	-6953.89	3746.5
AN48	-7665.09	3746.5
AN50	-8376.29	3746.5
AN51	-9087.49	3746.5
AN53	-9798.69	3746.5
AN54	-10509.9	3746.5
AN56	-11221.1	3746.5
AN57	-11932.3	3746.5
AN59	-12643.5	3746.5
AN62	-14036.7	3708.4
AN63	-14814.2	3708.4
AP2	14413.87	4171.95
AP3	13659.49	4171.95
AP5	12999.09	4267.2
AP6	12287.89	4267.2
AP7	11576.69	4267.2
AP9	10865.49	4267.2
AP10	10154.29	4267.2
AP12	9443.085	4267.2
AP13	8731.885	4267.2
AP15	8020.685	4267.2
AP49	-8020.69	4267.2
AP51	-8731.89	4267.2
AP52	-9443.09	4267.2
AP54	-10154.3	4267.2
AP55	-10865.5	4267.2

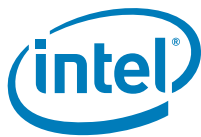


Table 6-2. SoC X and Y Pin List (Sheet 10 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
AP57	-11576.7	4267.2
AP58	-12287.9	4267.2
AP59	-12999.1	4267.2
AP61	-13659.5	4171.95
AP62	-14413.9	4171.95
AR1	14814.17	4635.5
AR2	14036.68	4635.5
AR17	7004.05	4431.792
AR19	6096	4431.792
AR21	5143.5	4431.792
AR23	4222.75	4431.792
AR25	3270.25	4431.792
AR27	2349.5	4431.792
AR29	1397	4431.792
AR30	476.25	4431.792
AR32	0	4787.392
AR34	-476.25	4431.792
AR35	-1397	4431.792
AR37	-2349.5	4431.792
AR39	-3270.25	4431.792
AR41	-4222.75	4431.792
AR43	-5143.5	4431.792
AR45	-6096	4431.792
AR47	-7004.05	4431.792
AR62	-14036.7	4635.5
AR63	-14814.2	4635.5
AT2	14413.87	5099.05
AT3	13659.49	5099.05
AT5	12999.09	5143.5
AT6	12287.89	5143.5
AT7	11576.69	5143.5
AT9	10865.49	5143.5
AT10	10154.29	5143.5
AT12	9443.085	5143.5
AT13	8731.885	5143.5
AT16	7626.35	5142.992
AT17	7004.05	5142.992
AT19	6096	5142.992
AT21	5143.5	5142.992



Table 6-2. SoC X and Y Pin List (Sheet 11 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
AT23	4222.75	5142.992
AT25	3270.25	5142.992
AT27	2349.5	5142.992
AT29	1397	5142.992
AT30	476.25	5142.992
AT34	-476.25	5142.992
AT35	-1397	5142.992
AT37	-2349.5	5142.992
AT39	-3270.25	5142.992
AT41	-4222.75	5142.992
AT43	-5143.5	5142.992
AT45	-6096	5142.992
AT47	-7004.05	5142.992
AT48	-7626.35	5142.992
AT51	-8731.89	5143.5
AT52	-9443.09	5143.5
AT54	-10154.3	5143.5
AT55	-10865.5	5143.5
AT57	-11576.7	5143.5
AT58	-12287.9	5143.5
AT59	-12999.1	5143.5
AT61	-13659.5	5099.05
AT62	-14413.9	5099.05
AU1	14814.17	5562.6
AU2	14036.68	5562.6
AU32	0	5498.592
AU62	-14036.7	5562.6
AU63	-14814.2	5562.6
AV2	14413.87	6026.15
AV3	13659.49	6026.15
AV5	12999.09	6096
AV6	12287.89	6096
AV7	11576.69	6096
AV9	10865.49	6096
AV10	10154.29	6096
AV12	9443.085	6096
AV14	8534.4	5854.192
AV16	7626.35	5854.192
AV17	7004.05	5854.192

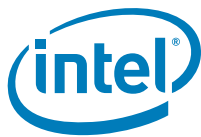


Table 6-2. SoC X and Y Pin List (Sheet 12 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
AV19	6096	5854.192
AV21	5143.5	5854.192
AV23	4222.75	5854.192
AV25	3270.25	5854.192
AV27	2349.5	5854.192
AV29	1397	5854.192
AV30	476.25	5854.192
AV32	0	6209.792
AV34	-476.25	5854.192
AV35	-1397	5854.192
AV37	-2349.5	5854.192
AV39	-3270.25	5854.192
AV41	-4222.75	5854.192
AV43	-5143.5	5854.192
AV45	-6096	5854.192
AV47	-7004.05	5854.192
AV48	-7626.35	5854.192
AV50	-8534.4	5854.192
AV52	-9443.09	6096
AV54	-10154.3	6096
AV55	-10865.5	6096
AV57	-11576.7	6096
AV58	-12287.9	6096
AV59	-12999.1	6096
AV61	-13659.5	6026.15
AV62	-14413.9	6026.15
AW1	14814.17	6489.7
AW2	14036.68	6489.7
AW14	8534.4	6565.392
AW16	7626.35	6565.392
AW17	7004.05	6565.392
AW19	6096	6565.392
AW21	5143.5	6565.392
AW23	4222.75	6565.392
AW25	3270.25	6565.392
AW27	2349.5	6565.392
AW29	1397	6565.392
AW30	476.25	6565.392
AW34	-476.25	6565.392



Table 6-2. SoC X and Y Pin List (Sheet 13 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
AW35	-1397	6565.392
AW37	-2349.5	6565.392
AW39	-3270.25	6565.392
AW41	-4222.75	6565.392
AW43	-5143.5	6565.392
AW45	-6096	6565.392
AW47	-7004.05	6565.392
AW48	-7626.35	6565.392
AW50	-8534.4	6565.392
AW62	-14036.7	6489.7
AW63	-14814.2	6489.7
AY2	14413.87	6953.25
AY3	13659.49	6953.25
AY5	12999.09	7048.5
AY6	12287.89	7048.5
AY7	11576.69	7048.5
AY9	10865.49	7048.5
AY10	10154.29	7048.5
AY32	0	6920.992
AY54	-10154.3	7048.5
AY55	-10865.5	7048.5
AY57	-11576.7	7048.5
AY58	-12287.9	7048.5
AY59	-12999.1	7048.5
AY61	-13659.5	6953.25
AY62	-14413.9	6953.25
A3	13954.13	-11314.18
A4	13221.34	-11314.18
A5	12548.24	-11314.18
A7	11697.34	-11314.18
A9	11024.24	-11314.18
A10	10198.1	-11314.18
A12	9271	-11314.18
A14	8343.9	-11314.18
A16	7416.8	-11314.18
A18	6489.7	-11314.18
A20	5562.6	-11314.18
A22	4635.5	-11314.18
A24	3708.4	-11314.18

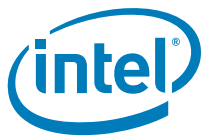


Table 6-2. SoC X and Y Pin List (Sheet 14 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
A26	2781.3	-11314.18
A28	1854.2	-11314.18
A30	927.1	-11314.18
A32	0	-11314.18
A34	-927.1	-11314.18
A36	-1854.2	-11314.18
A38	-2781.3	-11314.18
A40	-3708.4	-11314.18
A42	-4635.5	-11314.18
A44	-5562.6	-11314.18
A46	-6489.7	-11314.18
A48	-7416.8	-11314.18
A50	-8343.9	-11314.18
A52	-9271	-11314.18
A54	-10198.1	-11314.18
A56	-11410.7	-11314.18
A58	-12439.4	-11314.18
A60	-13112.5	-11314.18
A61	-13785.6	-11314.18
A62	-14382.5	-11314.18
BA1	14814.17	7416.8
BA2	14220.06	7543.8
BA12	9486.9	7276.592
BA14	8534.4	7276.592
BA16	7626.35	7276.592
BA17	7004.05	7276.592
BA19	6096	7276.592
BA21	5143.5	7276.592
BA23	4222.75	7276.592
BA25	3270.25	7276.592
BA27	2349.5	7276.592
BA29	1397	7276.592
BA30	476.25	7276.592
BA32	0	7632.192
BA34	-476.25	7276.592
BA35	-1397	7276.592
BA37	-2349.5	7276.592
BA39	-3270.25	7276.592
BA41	-4222.75	7276.592



Table 6-2. SoC X and Y Pin List (Sheet 15 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
BA43	-5143.5	7276.592
BA45	-6096	7276.592
BA47	-7004.05	7276.592
BA48	-7626.35	7276.592
BA50	-8534.4	7276.592
BA52	-9486.9	7276.592
BA62	-14220.1	7543.8
BA63	-14814.2	7416.8
BB1	14814.17	8088.63
BB3	13659.49	8001
BB5	12999.09	8001
BB6	12287.89	8001
BB7	11576.69	8001
BB10	10439.4	7987.792
BB12	9486.9	7987.792
BB14	8534.4	7987.792
BB16	7626.35	7987.792
BB17	7004.05	7987.792
BB19	6096	7987.792
BB21	5143.5	7987.792
BB23	4222.75	7987.792
BB25	3270.25	7987.792
BB27	2349.5	7987.792
BB29	1397	7987.792
BB30	476.25	7987.792
BB34	-476.25	7987.792
BB35	-1397	7987.792
BB37	-2349.5	7987.792
BB39	-3270.25	7987.792
BB41	-4222.75	7987.792
BB43	-5143.5	7987.792
BB45	-6096	7987.792
BB47	-7004.05	7987.792
BB48	-7626.35	7987.792
BB50	-8534.4	7987.792
BB52	-9486.9	7987.792
BB54	-10439.4	7987.792
BB57	-11576.7	8001
BB58	-12287.9	8001

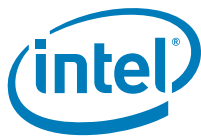


Table 6-2. SoC X and Y Pin List (Sheet 16 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
BB59	-12999.1	8001
BB61	-13659.5	8001
BB63	-14814.2	8088.63
BC2	14220.06	8353.552
BC32	0	8343.392
BC62	-14220.1	8353.552
BD1	14814.17	8939.53
BD2	14220.06	8950.452
BD3	13629.01	8890
BD5	12960.99	8890
BD6	12287.89	8890
BD8	11391.9	8698.992
BD10	10439.4	8698.992
BD12	9486.9	8698.992
BD14	8534.4	8698.992
BD16	7626.35	8698.992
BD17	7004.05	8698.992
BD19	6096	8698.992
BD21	5143.5	8698.992
BD23	4222.75	8698.992
BD25	3270.25	8698.992
BD27	2349.5	8698.992
BD29	1397	8698.992
BD30	476.25	8698.992
BD32	0	9054.592
BD34	-476.25	8698.992
BD35	-1397	8698.992
BD37	-2349.5	8698.992
BD39	-3270.25	8698.992
BD41	-4222.75	8698.992
BD43	-5143.5	8698.992
BD45	-6096	8698.992
BD47	-7004.05	8698.992
BD48	-7626.35	8698.992
BD50	-8534.4	8698.992
BD52	-9486.9	8698.992
BD54	-10439.4	8698.992
BD56	-11391.9	8698.992
BD58	-12287.9	8890



Table 6-2. SoC X and Y Pin List (Sheet 17 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
BD59	-12961	8890
BD61	-13629	8890
BD62	-14220.1	8950.452
BD63	-14814.2	8939.53
BE1	14814.17	9612.63
BE2	14220.06	9547.352
BE8	11391.9	9410.192
BE10	10439.4	9410.192
BE12	9486.9	9410.192
BE14	8534.4	9410.192
BE16	7626.35	9410.192
BE17	7004.05	9410.192
BE19	6096	9410.192
BE21	5143.5	9410.192
BE23	4222.75	9410.192
BE25	3270.25	9410.192
BE27	2349.5	9410.192
BE29	1397	9410.192
BE30	476.25	9410.192
BE34	-476.25	9410.192
BE35	-1397	9410.192
BE37	-2349.5	9410.192
BE39	-3270.25	9410.192
BE41	-4222.75	9410.192
BE43	-5143.5	9410.192
BE45	-6096	9410.192
BE47	-7004.05	9410.192
BE48	-7626.35	9410.192
BE50	-8534.4	9410.192
BE52	-9486.9	9410.192
BE54	-10439.4	9410.192
BE56	-11391.9	9410.192
BE62	-14220.1	9547.352
BE63	-14814.2	9612.63
BF3	13629.01	9682.48
BF5	12960.99	9682.48
BF6	12344.4	10121.392
BF32	0	9779.762
BF58	-12344.4	10121.392

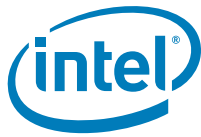


Table 6-2. SoC X and Y Pin List (Sheet 18 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
BF59	-12961	9682.48
BF61	-13629	9682.48
BG1	14814.17	10285.73
BG2	14220.06	10144.252
BG7	11588.75	10159.492
BG8	11125.2	10536.682
BG9	10661.65	10159.492
BG10	10198.1	10536.682
BG11	9734.55	10159.492
BG12	9271	10536.682
BG13	8807.45	10159.492
BG14	8343.9	10536.682
BG15	7880.35	10159.492
BG16	7416.8	10536.682
BG17	6953.25	10159.492
BG18	6489.7	10536.682
BG19	6026.15	10159.492
BG20	5562.6	10536.682
BG21	5099.05	10159.492
BG22	4635.5	10536.682
BG23	4171.95	10159.492
BG24	3708.4	10536.682
BG25	3244.85	10159.492
BG26	2781.3	10536.682
BG27	2317.75	10159.492
BG28	1854.2	10536.682
BG29	1390.65	10159.492
BG30	927.1	10536.682
BG31	463.55	10159.492
BG32	0	10536.682
BG33	-463.55	10159.492
BG34	-927.1	10536.682
BG35	-1390.65	10159.492
BG36	-1854.2	10536.682
BG37	-2317.75	10159.492
BG38	-2781.3	10536.682
BG39	-3244.85	10159.492
BG40	-3708.4	10536.682
BG41	-4171.95	10159.492



Table 6-2. SoC X and Y Pin List (Sheet 19 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
BG42	-4635.5	10536.682
BG43	-5099.05	10159.492
BG44	-5562.6	10536.682
BG45	-6026.15	10159.492
BG46	-6489.7	10536.682
BG47	-6953.25	10159.492
BG48	-7416.8	10536.682
BG49	-7880.35	10159.492
BG50	-8343.9	10536.682
BG51	-8807.45	10159.492
BG52	-9271	10536.682
BG53	-9734.55	10159.492
BG54	-10198.1	10536.682
BG55	-10661.7	10159.492
BG56	-11125.2	10536.682
BG57	-11588.8	10159.492
BG62	-14220.1	10144.252
BG63	-14814.2	10285.73
BH1	14814.17	10882.63
BH2	14237.84	10737.85
BH3	13631.67	10720.07
BH4	13034.77	10720.07
BH6	12437.87	10720.07
BH7	11840.97	10720.07
BH9	10661.65	10913.872
BH11	9734.55	10913.872
BH13	8807.45	10913.872
BH15	7880.35	10913.872
BH17	6953.25	10913.872
BH19	6026.15	10913.872
BH21	5099.05	10913.872
BH23	4171.95	10913.872
BH25	3244.85	10913.872
BH27	2317.75	10913.872
BH29	1390.65	10913.872
BH31	463.55	10913.872
BH33	-463.55	10913.872
BH35	-1390.65	10913.872
BH37	-2317.75	10913.872

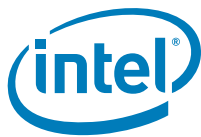


Table 6-2. SoC X and Y Pin List (Sheet 20 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
BH39	-3244.85	10913.872
BH41	-4171.95	10913.872
BH43	-5099.05	10913.872
BH45	-6026.15	10913.872
BH47	-6953.25	10913.872
BH49	-7880.35	10913.872
BH51	-8807.45	10913.872
BH53	-9734.55	10913.872
BH55	-10661.7	10913.872
BH57	-11841	10720.07
BH58	-12437.9	10720.07
BH60	-13034.8	10720.07
BH61	-13631.7	10720.07
BH62	-14237.8	10737.85
BH63	-14814.2	10882.63
BJ2	14382.5	11314.176
BJ3	13785.6	11314.176
BJ4	13112.5	11314.176
BJ6	12439.4	11314.176
BJ8	11410.7	11314.176
BJ10	10198.1	11314.176
BJ12	9271	11314.176
BJ14	8343.9	11314.176
BJ16	7416.8	11314.176
BJ18	6489.7	11314.176
BJ20	5562.6	11314.176
BJ22	4635.5	11314.176
BJ24	3708.4	11314.176
BJ26	2781.3	11314.176
BJ28	1854.2	11314.176
BJ30	927.1	11314.176
BJ32	0	11314.176
BJ34	-927.1	11314.176
BJ36	-1854.2	11314.176
BJ38	-2781.3	11314.176
BJ40	-3708.4	11314.176
BJ42	-4635.5	11314.176
BJ44	-5562.6	11314.176
BJ46	-6489.7	11314.176



Table 6-2. SoC X and Y Pin List (Sheet 21 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
BJ48	-7416.8	11314.176
BJ50	-8343.9	11314.176
BJ52	-9271	11314.176
BJ54	-10198.1	11314.176
BJ56	-11410.7	11314.176
BJ58	-12439.4	11314.176
BJ60	-13112.5	11314.176
BJ61	-13785.6	11314.176
BJ62	-14382.5	11314.176
B2	14382.88	-10882.88
B3	13758.8	-10720.07
B4	13161.9	-10720.07
B5	12565	-10720.07
B7	11968.1	-10720.07
B8	11371.2	-10720.07
B9	10774.3	-10745.47
B11	9734.55	-10913.87
B13	8807.45	-10913.87
B15	7880.35	-10913.87
B17	6953.25	-10913.87
B19	6026.15	-10913.87
B21	5099.05	-10913.87
B23	4171.95	-10913.87
B25	3244.85	-10913.87
B27	2317.75	-10913.87
B29	1390.65	-10913.87
B31	463.55	-10913.87
B33	-463.55	-10913.87
B35	-1390.65	-10913.87
B37	-2317.75	-10913.87
B39	-3244.85	-10913.87
B41	-4171.95	-10913.87
B43	-5099.05	-10913.87
B45	-6026.15	-10913.87
B47	-6953.25	-10913.87
B49	-7880.35	-10913.87
B51	-8807.45	-10913.87
B53	-9734.55	-10913.87
B55	-10661.7	-10913.87

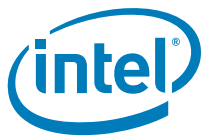


Table 6-2. SoC X and Y Pin List (Sheet 22 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
B57	-11841	-10720.07
B58	-12437.9	-10720.07
B60	-13034.8	-10720.07
B61	-13631.7	-10720.07
B62	-14237.8	-10737.85
B63	-14814.2	-10882.63
C1	14814.17	-10454.13
C2	14220.06	-10258.81
C9	10661.65	-10159.49
C10	10198.1	-10536.68
C11	9734.55	-10159.49
C12	9271	-10536.68
C13	8807.45	-10159.49
C14	8343.9	-10536.68
C15	7880.35	-10159.49
C16	7416.8	-10536.68
C17	6953.25	-10159.49
C18	6489.7	-10536.68
C19	6026.15	-10159.49
C20	5562.6	-10536.68
C21	5099.05	-10159.49
C22	4635.5	-10536.68
C23	4171.95	-10159.49
C24	3708.4	-10536.68
C25	3244.85	-10159.49
C26	2781.3	-10536.68
C27	2317.75	-10159.49
C28	1854.2	-10536.68
C29	1390.65	-10159.49
C30	927.1	-10536.68
C31	463.55	-10159.49
C32	0	-10536.68
C33	-463.55	-10159.49
C34	-927.1	-10536.68
C35	-1390.65	-10159.49
C36	-1854.2	-10536.68
C37	-2317.75	-10159.49
C38	-2781.3	-10536.68
C39	-3244.85	-10159.49



Table 6-2. SoC X and Y Pin List (Sheet 23 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
C40	-3708.4	-10536.68
C41	-4171.95	-10159.49
C42	-4635.5	-10536.68
C43	-5099.05	-10159.49
C44	-5562.6	-10536.68
C45	-6026.15	-10159.49
C46	-6489.7	-10536.68
C47	-6953.25	-10159.49
C48	-7416.8	-10536.68
C49	-7880.35	-10159.49
C50	-8343.9	-10536.68
C51	-8807.45	-10159.49
C52	-9271	-10536.68
C53	-9734.55	-10159.49
C54	-10198.1	-10536.68
C55	-10661.7	-10159.49
C56	-11125.2	-10536.68
C57	-11588.8	-10159.49
C62	-14220.1	-10144.25
C63	-14814.2	-10285.73
D1	14814.17	-9723.882
D2	14220.06	-9665.462
D4	13138.79	-10121.39
D6	12255.5	-10121.39
D8	11391.9	-10121.39
D32	0	-9779.762
D58	-12344.4	-10121.39
D59	-12961	-9682.48
D61	-13629	-9682.48
E3	13621.39	-9624.187
E4	13024.49	-9473.692
E6	12255.5	-9410.192
E8	11391.9	-9410.192
E10	10439.4	-9410.192
E12	9486.9	-9410.192
E14	8534.4	-9410.192
E16	7626.35	-9410.192
E17	7004.05	-9410.192
E19	6096	-9410.192

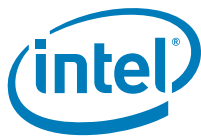


Table 6-2. SoC X and Y Pin List (Sheet 24 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
E21	5143.5	-9410.192
E23	4222.75	-9410.192
E25	3270.25	-9410.192
E27	2349.5	-9410.192
E29	1397	-9410.192
E30	476.25	-9410.192
E34	-476.25	-9410.192
E35	-1397	-9410.192
E37	-2349.5	-9410.192
E39	-3270.25	-9410.192
E41	-4222.75	-9410.192
E43	-5143.5	-9410.192
E45	-6096	-9410.192
E47	-7004.05	-9410.192
E48	-7626.35	-9410.192
E50	-8534.4	-9410.192
E52	-9486.9	-9410.192
E54	-10439.4	-9410.192
E56	-11391.9	-9410.192
E62	-14220.1	-9547.352
E63	-14814.2	-9612.63
F1	14814.17	-9050.782
F2	14220.06	-9072.118
F3	13697.59	-8699.5
F5	12999.09	-8699.5
F6	12287.89	-8699.5
F8	11391.9	-8698.992
F10	10439.4	-8698.992
F12	9486.9	-8698.992
F14	8534.4	-8698.992
F16	7626.35	-8698.992
F17	7004.05	-8698.992
F19	6096	-8698.992
F21	5143.5	-8698.992
F23	4222.75	-8698.992
F25	3270.25	-8698.992
F27	2349.5	-8698.992
F29	1397	-8698.992
F30	476.25	-8698.992



Table 6-2. SoC X and Y Pin List (Sheet 25 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
F32	0	-9054.592
F34	-476.25	-8698.992
F35	-1397	-8698.992
F37	-2349.5	-8698.992
F39	-3270.25	-8698.992
F41	-4222.75	-8698.992
F43	-5143.5	-8698.992
F45	-6096	-8698.992
F47	-7004.05	-8698.992
F48	-7626.35	-8698.992
F50	-8534.4	-8698.992
F52	-9486.9	-8698.992
F54	-10439.4	-8698.992
F56	-11391.9	-8698.992
F58	-12287.9	-8890
F59	-12961	-8890
F61	-13629	-8890
F62	-14220.1	-8950.452
F63	-14814.2	-8939.53
G1	14814.17	-8199.882
G2	14258.16	-8473.694
G32	0	-8343.392
G62	-14220.1	-8353.552
H3	13858.88	-8020.05
H5	12999.09	-7912.1
H6	12287.89	-7912.1
H7	11576.69	-7912.1
H10	10439.4	-7987.792
H12	9486.9	-7987.792
H14	8534.4	-7987.792
H16	7626.35	-7987.792
H17	7004.05	-7987.792
H19	6096	-7987.792
H21	5143.5	-7987.792
H23	4222.75	-7987.792
H25	3270.25	-7987.792
H27	2349.5	-7987.792
H29	1397	-7987.792
H30	476.25	-7987.792

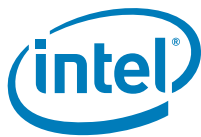


Table 6-2. SoC X and Y Pin List (Sheet 26 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
H34	-476.25	-7987.792
H35	-1397	-7987.792
H37	-2349.5	-7987.792
H39	-3270.25	-7987.792
H41	-4222.75	-7987.792
H43	-5143.5	-7987.792
H45	-6096	-7987.792
H47	-7004.05	-7987.792
H48	-7626.35	-7987.792
H50	-8534.4	-7987.792
H52	-9486.9	-7987.792
H54	-10439.4	-7987.792
H57	-11576.7	-8001
H58	-12287.9	-8001
H59	-12999.1	-8001
H61	-13659.5	-8001
H63	-14814.2	-8088.63
J1	14814.17	-7526.782
J2	14036.68	-7416.8
J12	9486.9	-7276.592
J14	8534.4	-7276.592
J16	7626.35	-7276.592
J17	7004.05	-7276.592
J19	6096	-7276.592
J21	5143.5	-7276.592
J23	4222.75	-7276.592
J25	3270.25	-7276.592
J27	2349.5	-7276.592
J29	1397	-7276.592
J30	476.25	-7276.592
J32	0	-7632.192
J34	-476.25	-7276.592
J35	-1397	-7276.592
J37	-2349.5	-7276.592
J39	-3270.25	-7276.592
J41	-4222.75	-7276.592
J43	-5143.5	-7276.592
J45	-6096	-7276.592
J47	-7004.05	-7276.592



Table 6-2. SoC X and Y Pin List (Sheet 27 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
J48	-7626.35	-7276.592
J50	-8534.4	-7276.592
J52	-9486.9	-7276.592
J62	-14220.1	-7543.8
J63	-14814.2	-7416.8
K2	14413.87	-6953.25
K3	13659.49	-6953.25
K5	12999.09	-7048.5
K6	12287.89	-7048.5
K7	11576.69	-7048.5
K9	10865.49	-7048.5
K10	10154.29	-7048.5
K32	0	-6920.992
K54	-10154.3	-7048.5
K55	-10865.5	-7048.5
K57	-11576.7	-7048.5
K58	-12287.9	-7048.5
K59	-12999.1	-7048.5
K61	-13659.5	-6953.25
K62	-14413.9	-6953.25
L1	14814.17	-6489.7
L2	14036.68	-6489.7
L14	8534.4	-6565.392
L16	7626.35	-6565.392
L17	7004.05	-6565.392
L19	6096	-6565.392
L21	5143.5	-6565.392
L23	4222.75	-6565.392
L25	3270.25	-6565.392
L27	2349.5	-6565.392
L29	1397	-6565.392
L30	476.25	-6565.392
L34	-476.25	-6565.392
L35	-1397	-6565.392
L37	-2349.5	-6565.392
L39	-3270.25	-6565.392
L41	-4222.75	-6565.392
L43	-5143.5	-6565.392
L45	-6096	-6565.392

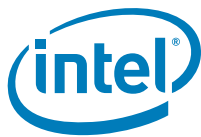


Table 6-2. SoC X and Y Pin List (Sheet 28 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
L47	-7004.05	-6565.392
L48	-7626.35	-6565.392
L50	-8534.4	-6565.392
L62	-14036.7	-6489.7
L63	-14814.2	-6489.7
M2	14413.87	-6026.15
M3	13659.49	-6026.15
M5	12999.09	-6096
M6	12287.89	-6096
M7	11576.69	-6096
M9	10865.49	-6096
M10	10154.29	-6096
M12	9443.085	-6096
M14	8534.4	-5854.192
M16	7626.35	-5854.192
M17	7004.05	-5854.192
M19	6096	-5854.192
M21	5143.5	-5854.192
M23	4222.75	-5854.192
M25	3270.25	-5854.192
M27	2349.5	-5854.192
M29	1397	-5854.192
M30	476.25	-5854.192
M32	0	-6209.792
M34	-476.25	-5854.192
M35	-1397	-5854.192
M37	-2349.5	-5854.192
M39	-3270.25	-5854.192
M41	-4222.75	-5854.192
M43	-5143.5	-5854.192
M45	-6096	-5854.192
M47	-7004.05	-5854.192
M48	-7626.35	-5854.192
M50	-8534.4	-5854.192
M52	-9443.09	-6096
M54	-10154.3	-6096
M55	-10865.5	-6096
M57	-11576.7	-6096
M58	-12287.9	-6096



Table 6-2. SoC X and Y Pin List (Sheet 29 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
M59	-12999.1	-6096
M61	-13659.5	-6026.15
M62	-14413.9	-6026.15
N1	14814.17	-5562.6
N2	14036.68	-5562.6
N32	0	-5498.592
N62	-14036.7	-5562.6
N63	-14814.2	-5562.6
P2	14413.87	-5099.05
P3	13659.49	-5099.05
P5	12999.09	-5143.5
P6	12287.89	-5143.5
P7	11576.69	-5143.5
P9	10865.49	-5143.5
P10	10154.29	-5143.5
P12	9443.085	-5143.5
P13	8731.885	-5143.5
P16	7626.35	-5142.992
P17	7004.05	-5142.992
P19	6096	-5142.992
P21	5143.5	-5142.992
P23	4222.75	-5142.992
P25	3270.25	-5142.992
P27	2349.5	-5142.992
P29	1397	-5142.992
P30	476.25	-5142.992
P34	-476.25	-5142.992
P35	-1397	-5142.992
P37	-2349.5	-5142.992
P39	-3270.25	-5142.992
P41	-4222.75	-5142.992
P43	-5143.5	-5142.992
P45	-6096	-5142.992
P47	-7004.05	-5142.992
P48	-7626.35	-5142.992
P51	-8731.89	-5143.5
P52	-9443.09	-5143.5
P54	-10154.3	-5143.5
P55	-10865.5	-5143.5

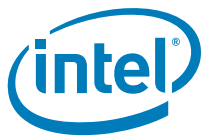


Table 6-2. SoC X and Y Pin List (Sheet 30 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
P57	-11576.7	-5143.5
P58	-12287.9	-5143.5
P59	-12999.1	-5143.5
P61	-13659.5	-5099.05
P62	-14413.9	-5099.05
R1	14814.17	-4635.5
R2	14036.68	-4635.5
R17	7004.05	-4431.792
R19	6096	-4431.792
R21	5143.5	-4431.792
R23	4222.75	-4431.792
R25	3270.25	-4431.792
R27	2349.5	-4431.792
R29	1397	-4431.792
R30	476.25	-4431.792
R32	0	-4787.392
R34	-476.25	-4431.792
R35	-1397	-4431.792
R37	-2349.5	-4431.792
R39	-3270.25	-4431.792
R41	-4222.75	-4431.792
R43	-5143.5	-4431.792
R45	-6096	-4431.792
R47	-7004.05	-4431.792
R62	-14036.7	-4635.5
R63	-14814.2	-4635.5
T2	14413.87	-4171.95
T3	13659.49	-4171.95
T5	12999.09	-4267.2
T6	12287.89	-4267.2
T7	11576.69	-4267.2
T9	10865.49	-4267.2
T10	10154.29	-4267.2
T12	9443.085	-4267.2
T13	8731.885	-4267.2
T15	8020.685	-4267.2
T49	-8020.69	-4267.2
T51	-8731.89	-4267.2
T52	-9443.09	-4267.2



Table 6-2. SoC X and Y Pin List (Sheet 31 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
T54	-10154.3	-4267.2
T55	-10865.5	-4267.2
T57	-11576.7	-4267.2
T58	-12287.9	-4267.2
T59	-12999.1	-4267.2
T61	-13659.5	-4171.95
T62	-14413.9	-4171.95
U1	14814.17	-3708.4
U2	14036.68	-3708.4
U5	12643.49	-3746.5
U7	11932.29	-3746.5
U8	11221.09	-3746.5
U10	10509.89	-3746.5
U11	9798.685	-3746.5
U13	9087.485	-3746.5
U14	8376.285	-3746.5
U16	7665.085	-3746.5
U17	6953.885	-3746.5
U18	6299.2	-3619.5
U20	5511.8	-3619.5
U22	4724.4	-3619.5
U23	3937	-3619.5
U25	3149.6	-3619.5
U27	2362.2	-3619.5
U28	1574.8	-3619.5
U30	787.4	-3619.5
U32	0	-3619.5
U34	-787.4	-3619.5
U36	-1574.8	-3619.5
U37	-2362.2	-3619.5
U39	-3149.6	-3619.5
U41	-3937	-3619.5
U42	-4724.4	-3619.5
U44	-5511.8	-3619.5
U46	-6299.2	-3619.5
U47	-6953.89	-3746.5
U48	-7665.09	-3746.5
U50	-8376.29	-3746.5
U51	-9087.49	-3746.5

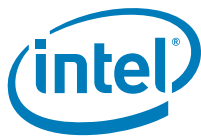


Table 6-2. SoC X and Y Pin List (Sheet 32 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
U53	-9798.69	-3746.5
U54	-10509.9	-3746.5
U56	-11221.1	-3746.5
U57	-11932.3	-3746.5
U59	-12643.5	-3746.5
U62	-14036.7	-3708.4
U63	-14814.2	-3708.4
V2	14413.87	-3244.85
V3	13659.49	-3244.85
V5	12999.09	-3225.8
V6	12287.89	-3225.8
V7	11576.69	-3225.8
V9	10865.49	-3225.8
V10	10154.29	-3225.8
V12	9443.085	-3225.8
V13	8731.885	-3225.8
V15	8020.685	-3225.8
V16	7309.485	-3225.8
V18	6299.2	-2895.6
V20	5511.8	-2895.6
V22	4724.4	-2895.6
V23	3937	-2895.6
V25	3149.6	-2895.6
V27	2362.2	-2895.6
V28	1574.8	-2895.6
V30	787.4	-2895.6
V32	0	-2895.6
V34	-787.4	-2895.6
V36	-1574.8	-2895.6
V37	-2362.2	-2895.6
V39	-3149.6	-2895.6
V41	-3937	-2895.6
V42	-4724.4	-2895.6
V44	-5511.8	-2895.6
V46	-6299.2	-2895.6
V48	-7309.49	-3225.8
V49	-8020.69	-3225.8
V51	-8731.89	-3225.8
V52	-9443.09	-3225.8



Table 6-2. SoC X and Y Pin List (Sheet 33 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
V54	-10154.3	-3225.8
V55	-10865.5	-3225.8
V57	-11576.7	-3225.8
V58	-12287.9	-3225.8
V59	-12999.1	-3225.8
V61	-13659.5	-3244.85
V62	-14413.9	-3244.85
W1	14814.17	-2781.3
W2	14036.68	-2781.3
W62	-14036.7	-2781.3
W63	-14814.2	-2781.3
Y2	14413.87	-2317.75
Y3	13659.49	-2317.75
Y5	12999.09	-2349.5
Y6	12287.89	-2349.5
Y7	11576.69	-2349.5
Y9	10865.49	-2349.5
Y10	10154.29	-2349.5
Y12	9443.085	-2349.5
Y13	8731.885	-2349.5
Y15	8020.685	-2349.5
Y16	7309.485	-2349.5
Y18	6299.2	-2171.7
Y20	5511.8	-2171.7
Y22	4724.4	-2171.7
Y23	3937	-2171.7
Y25	3149.6	-2171.7
Y27	2362.2	-2171.7
Y28	1574.8	-2171.7
Y30	787.4	-2171.7
Y32	0	-2171.7
Y34	-787.4	-2171.7
Y36	-1574.8	-2171.7
Y37	-2362.2	-2171.7
Y39	-3149.6	-2171.7
Y41	-3937	-2171.7
Y42	-4724.4	-2171.7
Y44	-5511.8	-2171.7
Y46	-6299.2	-2171.7



Table 6-2. SoC X and Y Pin List (Sheet 34 of 34)

Pin	Xcoord(mm)	Ycoord(mm)
Y48	-7309.49	-2349.5
Y49	-8020.69	-2349.5
Y51	-8731.89	-2349.5
Y52	-9443.09	-2349.5
Y54	-10154.3	-2349.5
Y55	-10865.5	-2349.5
Y57	-11576.7	-2349.5
Y58	-12287.9	-2349.5
Y59	-12999.1	-2349.5
Y61	-13659.5	-2317.75
Y62	-14413.9	-2317.75

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7 Package Information

The SoC comes in Flip-Chip Ball Grid Array (FCBGA) package.

7.1 Package Attributes

Table 7-1. Package Attributes

Category	SoC
Package	Flip-Chip Ball Grid Array (FCBGA)
Type	31x24 mm ²
I/O count	682
Ball count	1296
Ball pitch	0.593 mm
Z-height	1.318 mm +/- 0.092

Figure 7-1. Package Mechanical Drawing—Part 1 of 3

Figure 7-1. Package Mechanical Drawing—Part 1 of 3



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