

Intel® Pentium® Silver and Intel® Celeron® Processors Specification Update October 2020 Revision 007 and a underined underined under the dunder t

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The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Copies of documents which have an order number and are referenced in this document may be obtained by calling 1-800-548-4725 or visit www.intel.com/design/literature.htm.

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Revision Date	Revision Number	Description				
October 2020	007	Updated errata 006				
March 2020	006	Added Errata 038				
January 2020	005	Updated Section 7				
November 2019	004	Added Errata 037 Updated Table 3-3				
October 2019	003	Added Errata 026 to 036				
July 2018	002	Added Errata 023 to 025				
February 2018	001	Initial Release				
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1 Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this document and are no longer published in other documents. This document may also contain information that has not been previously published.

Note: Throughout this document Intel® Pentium® Silver and Intel® Celeron® Processor is referred as Processor or SoC.

Throughout this document Intel® Pentium® Silver and Intel® Celeron® Processors families refer to:

- Intel® Pentium® Silver N5000
- Intel[®] Pentium[®] Silver J5005
- Intel® Celeron® N4000 and N4100
- Intel® Celeron® J4105 and J4005

1.1 Affected Documents

od uno	Document Title	inger	Document Number
Intel® Pentium® Silver Volume 1 of 2	and Intel® Celeron® Proc	essors Datasheet	336560-003
Intel® Pentium® Silver Volume 2 of 2	and Intel® Celeron® Proc	essors Datasheet	336561-001

1.2 Related Documents

Document Title	Location
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference Manual A-M Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference Manual N-Z Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B: System Programming Guide Intel® 64 and IA-32 Intel Architecture Optimization Reference Manual	Vol:1 Vol.2A Vol.2B Vol.3A Vol.3B
Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes	Click here

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Nomenclature

Errata are design

Processor he'
esign Errata are design defects or errors in engineering samples. Errata may cause the processor behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping assumes that all errata documented for that stepping are present on all devices.

S-Spec Number is a five-digit code used to identify products. Products are differentiated by their unique characteristics, that is, core speed, L2 cache size, and package type as described in the processor identification information table. Read all notes associated with each S-Spec number.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, and so



Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes, which apply to the listed steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

2.2 **Stepping**

X: Erratum, Specification Change or Clarification that applies to this stepping.

(No mark) or (Blank Box): This erratum is fixed in listed stepping or specification change does not apply to list stepping.

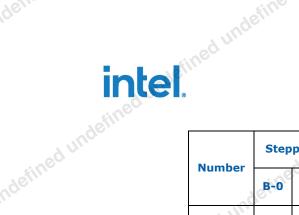
Status

Doc: Document change or update that will be implemented.

Row

	Plan Fix: This erratum may be fixed in a future stepping of the product.Fixed: This erratum has been previously fixed.							
	No Fix: Th	ere is	no pla	n to fix this e	ratum, ed the			
2.4 ed	Row			used u	no. Inden.			
ed under	Number	Step	ping	indefil.	Environ Title			
ndefine	Number	B-0	R-0	Status	Errata Title			
0.	001	Х	Х	No Fix	Certain MCA Events May Incorrectly Set Overflow Bit	efine		
م لا	002	Х	Х	No Fix	SATA Interface May Not Loopback Patterns in BIST-L Mode			
indefined undefined	003	Х	Х	No Fix	SATA Host Controller Does Not Pass Certain Compliance Tests			
defined s	004	X	X.	No Fix	HD Audio Recording May Experience a Glitch While Opening or Closing Audio Streams			
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ndefined undefine	Number	B-0	R-0	Status	Errata Title		
	005	х	х	No Fix	USB 2.0 Timing Responsiveness Degradation. Status rejected		
sined und	006	Х	Х	No Fix	Trace Data to Multiple Destinations is Not Supported		
indefined undefined unde	007	х	X	No Fix	Storage Controllers May Not Be Power Gated		
ndefin	008	dexin	Х	No Fix	Certain VT-d SVM Registers Are Writeable		
	69	х	х	No Fix	Changing VT-d Event Interrupt Configuration Control Registers May Not Behave as Expected		
sined une	010	х	х	No Fix	SoC May Not Meet The VOL(MAX) Specification for THERMTRIP_N.		
undefined undefined und	011	х	х	No Fix	Intermittent CATERR may occur when back to back Host controller reset is performed		
undefin.	012	X	Х	No Fix	USB xHCI Controller May Not Re-enter a D3 State After a USB Wake Event		
	60	х	х	No Fix	USB Device Controller Incorrectly Interprets U3 Wakeup For Warm Reset		
undefined undefined un	014	Х	х	No Fix	Start/Stop Bits in MOT packets are not set on an IMR Violation		
ined une	015	Х	X	No Fix	URES contents may be lost after entering S0ix		
undei	016	XS	Х	No Fix	Performance Monitoring Event TLB_FLUSHES.STLB_ANY Double Counts		
	017	Х	Х	No Fix	Non Canonical Instruction Fetch May Not Signal #GP Fault		
sined u	018	х	х	No Fix	Intel PT CR3 Filtering Compares Bits [11:5] of CR3 and IA32_RTIT_CR3_MATCH outside of PAE Paging Mode		
ed under.	019	х	х	No Fix	Performance Monitor Instructions Retired Event May Not Count Consistently		
d undefined undefined u	020	X	X	No Fix	RF May be Incorrectly Set In The EFLAGS That is Saved to The Stack or to The Enclave SSA		
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ndefined undefined un	Number	B-0	R-0	Status	Errata Title	ed und		
	021	Х	Х	No Fix	IA32_PERF_GLOBAL_INUSE[62] May be Non-Zero			
indefined undefined und	022	Х	Х	No Fix	Intel PT OVF Packet May Be Followed By TIP.PGD			
ed undefir.	023	Х	X	No Fix	Intel® PT OVF Packet May Not Be Followed By A FUP Or TIP.PGE Packet			
indefines	024	XII	X	No Fix	PWRBTN_STS And PWRBTNOR_STS Status Bits Not Set Following A Power Button Override Event	red uni		
	025	Х	Х	No Fix	PM1_STS_EN.WAK_STS is Not Set Waking From A Valid Sleep Type			
undefined undefined un	026	Х	Х	No Fix	Intel® Processor Trace Output May Over-write ToPA Output Region			
ed unden	027	Х	X	No Fix	IA32_PERF_GLOBAL_INUSE[PMI_InUse] Reports an Incorrect Value.			
undefine	028	X	X	No Fix	A single VM Entry or VM Exit That Both Disables And Re- enables Intel® PT May Cause Unpredictable System Behavior	fined u		
	029	Х	Х	No Fix	I2C TX_HOLD Hold Time Specification May be Violated			
adefined	030	Х	Х	No Fix	System May Experience Inability to Boot or May Cease Operation or Nonfunctioning of LPC, I2C and GPIO Circuitry			
d undefined undefined ur	031	X	X)	No Fix	eMMC controller may fail to detect a CRC error in HS400 mode			
Junge	032	X	Х	No Fix	Certain MIPI Display Panels May Remain Blank	efined		
ed1	033	х	х	No Fix	An Indirect JMP or Indirect CALL Whose Last Instruction Byte is on The Last Byte of a 4GB Region of Memory May Lead to Unpredictable System Behavior			
d undefil.	034	Х	Х	No Fix	Processor Energy Usage Calculation May Be Incorrect			
d undefined undefined u	035	X	X	No Fix	Unexpected #PF, #GP, #UD, or Other Unpredictable System Behavior May Occur	fined		
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red und	Number	Step	ping	Status	Errata Title
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>6	036	х	х	No Fix	PEBS DLA May Report Incorrect Value
fined uno.	037	х	Х	No Fix	System May Hang Under Complex Conditions
red under	038	Х	X	No Fix	Intel® PT TMA Packets Have Incorrect Payload
Table 2-1	: Specifica	ition C	Change	es	afined L
	Number	•			Specification Changes

Table 2-1: Specification Changes

	Number		Specification Changes	nde
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Table 2-2: Specification Clarifications

Number	define	Specification Clarifications
	None	inde.

Table 2-3: Documentation Changes

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	Number		Documentation (ind		
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Identification Information

The processor stepping can be identified by the following registers contents:

Table 3-1: Processor Signature by Using Programming Interface

Reserved	Extended Family ¹	Extended Model ²	Reserved	Processor Type ³	Family Code ⁴	Model Number ⁵	Stepping ID ⁶
31:28	27:20	19:16	15:13	12	11:8	7:4	3:0
0x0	0×00	0x7	0	0	0x6	0xA	1

NOTES:

- 1. The Extended Family, Bits [27:20] are used in conjunction with the Family Code, specified in Bits [11:8], to indicate whether the processor belongs to the Intel386™, Intel486™, Pentium®, Pentium® Pro, Pentium® 4, Intel® Core™2, or Intel® Atom™ processor series.
- The Extended Model, Bits [19:16] in conjunction with the Model Number, specified in Bits [7:4], are used to identify the model of the processor within the processor's family.
- 3. The Processor Type, specified in Bits [13:12] indicates whether the processor is an original OEM processor, an OverDrive processor, or a dual processor (capable of being used in a dual processor system).
- 4. The Family Code corresponds to Bits [11:8] of the EDX register after RESET, Bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register is accessible through Boundary Scan.
- 5. The Model Number corresponds to Bits [7:4] of the EDX register after RESET, Bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register is accessible through Boundary Scan.
- 6. The Stepping ID in Bits [3:0] indicates the revision number of that model.

When EAX is initialized to a value of 1, the CPUID instruction returns the Extended Family, Extended Model, Type, Family, Model and Stepping value in the EAX register.

Note: The EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

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Table 3-2: Processor Identification by Register Contents

Y a.		1	1	76.	1	
ndefiner	Processor Line	Stepping	Vendor ID ¹	Host Device ID ²	Processor Graphics Device ID ³	Revision ID ⁴
sined under	Intel® Pentium® Processor Series and Intel® Celeron® Processor Series	В0	8086	31F0	3184	0x3
under. N	OTE: Jefins					
sined li	The Vendor ID corresponds to 00h-01h in the PCI function 0			dor ID Regis	ter located	at offset
inde. 2.	The Host Device ID correspond Device 0 offset 02h- 03h in th					ated at
3	The Processor Graphics Device	י זט (טוט)) correction	nde to hite 1	5.0 of the I	Davica ID

NOTE:

- 1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00h-01h in the PCI function 0 configuration space.
- The Host Device ID corresponds to bits 15:0 of the Device ID Register located at Device 0 offset 02h- 03h in the PCI function 0 configuration space.
- The Processor Graphics Device ID (DID2) corresponds to bits 15:0 of the Device ID Register located at Device 2 offset 02h-03h in the PCI function 0 configuration space.
- The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

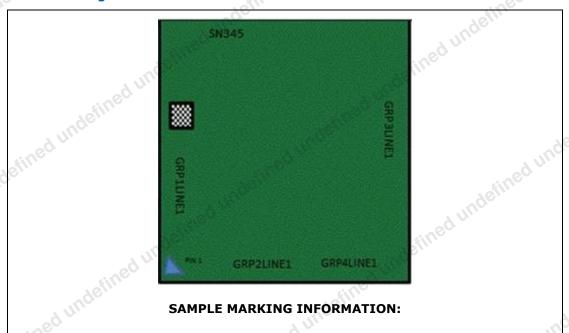
Table 3-3: S-Spec		690	Functional	Core s	Speed	Integrated Core S	Graphics peed	TDP
S-Spec	MM#	Stepping	Core	Burst Frequency Mode (BFM) 1C	High Frequency Mode (HFM)	Burst Frequency	LFM Frequency	(W)
R3RZ	961638	B-0	4	2.7GHz	1.1GHz	750 MHz	100MHz	6
R3S0	961639	B-0	4	2.4GHz	1.1GHz	700 MHz	100MHz	6
R3S1	961640	B-0	2	2.6GHz	1.1GHz	650 MHz	100MHz	6
R3S1 R3S3 R3S4 R3S5 RFDC	961642	B-0	4	2.8GHz	1.5GHz	800 MHz	100MHz	10
R3S4	961643	B-0	4	2.5GHz	1.5GHz	750 MHz	100MHz	10
R3S5	961644	B-0	2	2.7GHz	2.0GHz	700 MHz	100MHz	10
RFDC	999DAV	R-0	4	3.1GHz	1.1GHz	750 MHz	100MHz	6
RESZ	984729	R-0	4	2.6GHz	1.1GHz	700 MHz	100MHz	6
RET0	984730	R-0	2	2.8GHz	1.1GHz	650 MHz	100MHz	6
RFDB	999DAL	R-0	4	3.2GHz	2.0GHz	800 MHz	100MHz	10
RGZS	999PVK	R-0	4	2.7GHz	2.0GHz	750 MHz	100MHz	10
RET3	984796	R-0	2	2.9GHz	2.0GHz	700 MHz	100MHz	10
unde RET3	č	undefin	ed una	§ §	undefined un	Je.		defin
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Component Marking Information

Processor shipments can be identified by the following component markings and example

Figure 4-1: SoC Markings



	20,	
Legend	Mark Text	Orientation
GRP1LINE1	ed uno	North
GRP2LINE1	SR3S1	North
GRP3LINE1	J746B854	North
GRP4LINE1	{ e1}	North
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d undefined L	indefil	ned unit



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Jer.	dundefine	undefined "	defined un
intel	inec	d undefined by	rrata
Lefined undefine	Errata	d undefined by	- ind
,100	001 : Certain M	ICA Events May Incorrectly Set Overflow Bit	efined
ined und	Problem	A single machine check event may incorrectly set OVER (bit 62) of IA32_MC4_STATUS (MSR 411H). The affected MCA events are Unsupported IDI opcode (MCACOD 0x0408, MSCOD 0x0000), WBMTo* access to MMIO (MCACOD 0x0408, MCACOD 0x0003) and CLFLUSH to MMIO (MCACOD 0x0408, MCACOD 0x0004).	nde
fined under	Implication	Software analyzing system machine check error logs may incorrectly think that multiple errors have occurred. Intel has not observed this erratum impacting commercially available systems.	
	Workaround	None identified.	ined u
	Status	For the steppings affected, see the Summary Tables of Changes.	Indelli
, uni	le ₁ .	defined	
ined to	002 : SATA Inte	erface May Not Loopback Patterns in BIST-L Mode	

	7 01,	.,00	leill.
	Status	For the steppings affected, see the Summary Tables of Changes.	Mor
inde		define	•
of ined by	002 : SATA Inte	erface May Not Loopback Patterns in BIST-L Mode	
undefined unde	Problem	In certain BIST-L TX compliance test setups on SATA interface, the first 10b in the MFTP (Mid Frequency Test Pattern), i.e. 333h, inserted by J-BERT has disparity mismatch with the previous 10b, i.e. 363h, of previous HFTP (High Frequency Test Pattern) block. 333h has negative beginning disparity while 363h has positive ending disparity. When SoC detects disparity mismatch, it does not re-compute the running disparity based on the received 333h.	indefined un
sined und	Implication	Due to this erratum, SATA interface may not correctly loopback patterns in BIST-L mode. This erratum does not impact BIST-T compliance mode.	
undefined undefined und	Workaround	While using BIST-L loopback mode for SATA TX compliance testing, if a disparity error is encountered in subsequent MFTP block after receiving BIST-L FIS and HFTP block, insert a non-ALIGN primitive to correct back the disparity error at the beginning of MFTP pattern.	ed u
3	Status	For the steppings affected, see the Summary Tables of Changes.	ndefille
ed undefined und	efin.	ined undefined undefines	defined i
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9er.	ad undefine	Indefined	defined un
Errata _{Un} de ^{fil}		ed undefined E	
ndefined under	003 : SATA Hos	The SoC SATA host controller OOB (Out of Band) Host Responses, OOB Transmit Gap, and OOB Transmit Burst Length do not pass	offined und
ed undefi	Wed .	Serial ATA Interoperability Program Revision 1.4.3, Unified Test Document Version 1.01 tests OOB-03[a/b], OOB-05, and OOB-06[a/b].	nde
define	Implication	Intel has not observed any functional failures due to this erratum.	
raed un	Workaround	None identified.	
Indefil.	Status	For the steppings affected, see the Summary Tables of Changes.	defined un

Ye.	Status	For the steppings affected, see the Summary Tables of Changes.
	' nuge,	adefill
. 26	004 : HD Audio Streams	Recording May Experience A Glitch While Opening Or Closing Audio
isfined une	Problem	Setting CRSTB (bit 0 at Intel HD Audio Base Address + 8) to zero when opening and closing audio streams may result in audio glitches.
defined unos	Implication	Due to this erratum, audio glitches may occur while opening or closing audio streams
undefine	Workaround	Avoid setting CRSTB (bit 0 at Intel HD Audio Base Address + 8) to zero unless entering D3 for system suspend or unless asserting platform reset for reboot.
	Status	For the steppings affected, see the Summary Tables of Changes.
und	le _{II} .	defines

	Status	For the steppings affected, see the Summary Tables of Changes.
ind	em	define
ined b.	005 : USB 2.0 1	Fiming Responsiveness Degradation
defined under	Problem	USB specification requires 1ms resume reflection time from platform to the device indicating USB resume/wake. Due to this erratum, SoC implementation violates the USB2 timing specification.
	Implication	When this erratum occurs, USB devices that are sensitive to this timing specification may cease to function or re-enumerate upon waking from suspend.
dun	Workaround	None identified.
defines	Status	For the steppings affected, see the Summary Tables of Changes.
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ad undefines	006 : Trace Dat	a to Multiple Destinations Is Not Supported	
ndefine	Problem	Trace data from one trace source (i.e. ODLA, STH, SoCHAP, DTF) containing several STP Masters and sent in one Grant Duration will all be sent to a single destination, even if the SWDEST [0-31] registers (CSR_MTB_BAR Offsets 4h-8Bh) are configured to send data from those Masters to different destinations.	ndefined unde
ed under	Implication	Trace data from a given Master can be sent to the wrong destination.	_
ined undefine	Workaround	For Intel® Trace Hub to support multiple destinations, Grant Duration should be set to 11111111h in PGD0 (CSR_MTB_BAR Offset AC). This may impact aggregate trace throughput.	ه ه
unde ⁱ ll.	Status Action	For the steppings affected, see the Summary Tables of Changes.	ed un
	ed ulle	, unde	odefill.
adr	007 : Storage C	ontrollers May Not Be Power Gated	

11/10	Status	For the steppings affected, see the Summary rables of Changes.	ec.
	ed une	, unde	odefille
de	007 : Storage C	Controllers May Not Be Power Gated	
d undefined une	Problem	When disabled or placed in D3 state by BIOS, the SD Card and SDIO storage controllers may not be power gated unless this is done prior to the eMMC controller being disabled or placed in D3 state.	
.indefined	Implication	Due to this erratum, storage controllers may not be power gated. This erratum does not apply to SKUs without eMMC controllers.	ed un
. 6	Workaround	BIOS should ensure the SD Card and SDIO controllers are disabled before disabling the eMMC controller or putting it into D3.	undefine
ined une	Status	For the steppings affected, see the Summary Tables of Changes.	
indefil.		ined by	
7 (),		101	

	Workaround	BIOS should ensure the SD Card and SDIO controllers are disabled before disabling the eMMC controller or putting it into D3.	unde
inged uni	Status	For the steppings affected, see the Summary Tables of Changes.	
indefit.		defines "ined to	
sined u.	008 : Certain V	T-d SVM Registers Are Writeable	
A under.	Problem defi	VT-d engines that do not advertise SVM (Shared Virtual Memory) capability should treat the 32-bit registers at VTDBAR offsets 0xDC, 0xE0, 0xE4, 0xE8 and 0xEC as reserved and read-only. Due to this erratum, these registers are writeable.	, undefined u
ned une	Implication	Writing the listed registers does not affect the operation of the SoC.	S.
indefil.	Workaround	None identified.	
Hined L.	Status	For the steppings affected, see the Summary Tables of Changes.	
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ger.	od undefine	indefined a	defined un
Errata undefi	ine.	ined undefined to	
ed unde	009 : Changing Behave as Expe	VT-d Event Interrupt Configuration Control Registers May Not ected	
ndefine	Problem fine	Due to this erratum, the sequence used to change VT-d event interrupt service routine configuration for Fault Events and for Invalidation Events may not work as expected. Specifically, reading one of the associated configuration registers does not serialize VT-d event interrupts. As a result, VT-d event interrupts that were issued using the previous interrupt service configuration may be delivered after software has observed the interrupt service configuration to be updated.	ndefined uno
sined under.	Implication	VT-d event interrupts using stale configuration information may be lost or cause unexpected behavior. Intel has not observed this erratum to impact commercially available software.	
Inder.	Workaround	Reading a VT-d event control register twice achieves the intended interrupt serialization.	defined un
.ndr	Status	For the steppings affected, see the Summary Tables of Changes.	und
ined un.		ad unoc	7

	A Vi	interrupt Serialization.	76/1
40	Status	For the steppings affected, see the Summary Tables of Changes.	and
ad uno		under. define	
define	010 : SoC May	Not Meet The VOL(MAX) Specification for THERMTRIP_N	
adefined une	Problem	Under certain platform configurations and conditions, when the SoC asserts THERMTRIP_N, it may not meet the VOL(MAX) specification.	d un
un ^c	Implication	When this erratum occurs, the platform may not detect the assertion of THERMTRIP_N. This may, in turn, prevent the power-button override capability from resetting the platform placing the platform in a non-responsive state requiring the platform to go to G3 (completely drained battery needed) in order to reboot.	dundefined
sined undefinee	Workaround	Platforms designs should not have a pull-up resistor on the THERMTRIP_N signal and per Intel simulation analysis, platform design can limit exposure to this issue by ensuring IOL(MAX) does not exceed 4uA.	
huger.	Status	For the steppings affected, see the Summary Tables of Changes.	ined u
, un	defined un	odefined unde	ed undefin
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ige.	ed undefine	indefined	defined un
intel	ine	adefined &	Errata
defined		ined III.	¬
ined unit	011 : Intermitt Performed	ent CATERR May Occur When Back To Back Host Controller Reset Is	
	Problem	The xHCI host controller may fail to respond, due to an internal race condition, if consecutive xHCI Host Controller resets are performed.	defined ur
unde	Implication	A processor CATERR may occurs during long duration reboot testing or S4/S5 cycling tests.	
indefined	Workaround	Software should add a 120ms delay in between consecutive xHCI host controller resets.	
ined u	Status	For the steppings affected, see the Summary Tables of Changes.	
iden.	defin	sined s	ed u
	012 : USB xHCI	Controller May Not Re-enter A D3 State After A USB Wake Event	define

ined un	Status	For the steppings affected, see the Summary Tables of Changes.	. 6
Indeili.	defin	tined	ed un
	012 : USB xHC	Controller May Not Re-enter A D3 State After A USB Wake Event	ndefille
dund	Problem	After processing a USB 3.0 wake event, the USB xHCI controller may not re-enter D3 state.	200
definec	Implication	When the failure occurs, the system will not enter an Sx state.	
indefined unc	Workaround	Software should clear bit 8 PME Enable (PME_EN) of PM_CSPower management Control/Status Register (USB xHCI-D21:F0: Offset 74h) after the controller enters D0 state following an exit from D3.	ed un
	Status	For the steppings affected, see the Summary Tables of Changes.	indefine
.0	defill	ined ined	n,
ed un	013 : USB Devi	ce Controller Incorrectly Interprets U3 Wakeup for Warm Reset	

	Status	For the steppings affected, see the Summary Tables of Changes.	odefille
60.	Efile	ined ined	, Ull
ined un	013 : USB Device	ce Controller Incorrectly Interprets U3 Wakeup for Warm Reset	
undefined undefin	Problem	xHCI violates USB 3 specification for tU3WakeupRetryDelay, which dictates time to initiate the U3 wakeup LFPS Handshake signaling after an unsuccessful LFPS handshake. XHCI employs 12us for tU3WakeupRetryDelay instead of 100ms [as defined per spec].	edu
sined uni	Implication	Device may incorrectly interpret the LFPS asserted [due to the short tU3WakeupRetryDelay time] for duration greater than tResetDelay. If resume fails on the host side, this will be detected as a warm reset from xHCI and transition into Rx.Detect LTSSM state. Due to this erratum, the device may fail to respond to xHCIinitiated U3 wakeup request.	Jundefine
4 under	Workaround	None identified.	
1efined	Status	For the steppings affected, see the Summary Tables of Changes.	
ed unos	ed unde	, undefine	defined
Intel® Pentium® S Specification Upo 18	ilver and Intel® Cel date	eron® Processors October 2020 Document Number: 336562-00	
defined u.		ined under	



	ed undefil.	undefined	adefined or
Errata undefi	V.	integral defined a undefined a	
efined under	014 : Start/Sto	P Bits In Mot Packets Are Not Set On An IMR Violation Memory Order Tracing (MOT) does not set the start/stop bits in the header packet if the traced packet is aborted due to an IMR	ofined u
ined under	Implication	(Isolated Memory Regions) violation. The MOT trace may be missing start/stop indications. Intel has not observed this erratum to impact the operation of any commercially available software.	undle .
indefil.	Workaround	None identified.	
Sined W	Status	For the steppings affected, see the Summary Tables of Changes.	
	defin	afineo	- ined i
	015 : URES Con	itents May Be Lost After Entering S0ix	46 jii

ined u.	Status	For the steppings affected, see the Summary Tables of Changes.	. 8
Indeit.	adefin	afined by	ined une
	015 : URES Con	itents May Be Lost After Entering S0ix	indefill.
ndefined unde	Problem	The contents of URES (Unsupported Request Error Status) CSR (Bus:0, Device:13, Function:0, Offset: F0H) should be preserved across a S0ix transition. However, due to this erratum, the register gets cleared upon entry to S0ix and its error logging information is lost.	S-
Jefined III.	Implication	Software on a system that enters S0ix after an error is logged in URES will no longer be able to see the error details in URES.	, un
nur	Workaround	The system can be configured to generate an NMI on an error logged in URES, enabling software to manage the error prior to S0ix entry.	undefineo
d und	Status	For the steppings affected, see the Summary Tables of Changes.	
defined		sined di	

fined	logged in URES, enabling software to manage the error prior to S0ix entry.
Status	For the steppings affected, see the Summary Tables of Changes.
	ined a dunc
016 : Performan	nce Monitoring Event TLB_FLUSHES.STLB_ANY Double Counts
Problem	A performance monitoring counter programmed to count the event TLB_FLUSHES.STLB_ANY (EventID 0BDH, Mask 20H) will increment twice for each STLB flush operation instead of incrementing once.
Implication	Performance analysis software will read double the number of STLB flushes that have actually occurred.
Workaround	Software should treat every two counts of TLB_FLUSHES.STLB_ANY as an indication of a single STLB flush.
Status	For the steppings affected, see the Summary Tables of Changes.
ined under	Intel® Pentium® Silver and Intel® Celeron® Processors
	016 : Performan Problem Implication Workaround

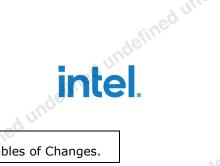
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96.	od undefine	Indefined	defined un
intel.	ue.	indefined &	rrata
d undefinee	017 : Non Cano	nical Instruction Fetch May Not Signal #GP Fault	
	Problem in C	An instruction fetch that includes linear address 8000_0000_0000H should signal a #GP fault due to a noncanonical violation. Due to this erratum, the instruction may be decoded using bytes starting from address ffff_8000_0000_0000H instead.	ndefined und
adefined unde	Implication	Software that relies on the signaling of a #GP fault to indicate the boundary between canonical and non-canonical spaces may not work as intended. Intel has not observed this erratum to affect any commercially available software.	
ined une	Workaround	None identified.	
indefin	Status Action	For the steppings affected, see the Summary Tables of Changes.	ed un
	ed un	, unde	define
290	018 : Intel PT C	R3 Filtering Compares Bits [11:5] Of CR3 And 3_MATCH Outside Of PAE Paging Mode	911.

1100	Status	For the steppings affected, see the Summary Tables of Changes.	eo,
	ed un	, unde.	ndefille
unde	018 : Intel PT (IA32_RTIT_CR	CR3 Filtering Compares Bits [11:5] Of CR3 And 3_MATCH Outside Of PAE Paging Mode	
ofined undefined &	Problem	R3[11:5] are used to locate the page-directory-pointer table only in PAE paging mode. When using Intel PT (Processor Trace), those bits of CR3 are compared to IA32_RTIT_CR3_MATCH (MSR 572H) when IA32_RTIT_CTL.CR3Filter (MSR 570H, bit 7) is set, independent of paging mode.	
unde	Implication	Any value written to the ignored CR3[11:5] bits, which can only be non-zero outside of PAE paging mode, must also be written to IA32_RTIT_CR3_MATCH[11:5] in order to result in a CR3 filtering match.	undefined U.
ed uno	Workaround	None identified.	
adefine	Status	For the steppings affected, see the Summary Tables of Changes.	
sed un.		4 linds	
alefin	019 : Performa	nce Monitor Instructions Retired Event May Not Count Consistently	401
A m.	Problem	Performance Monitor Instructions Retired (Event C0H; Umask 00H) and the instruction retired fixed counter (IA32_FIXED_CTR0	indefinect

	4 1/1,	
019 : Performa	ance Monitor Instructions Retired Event May Not Count Consistently	41
Problem	Performance Monitor Instructions Retired (Event COH; Umask 00H) and the instruction retired fixed counter (IA32_FIXED_CTR0 MSR (309H)) are used to track the number of instructions retired. Due to this erratum, certain situations may cause the counter(s) to increment when no instruction has retired or to not increment when specific instructions have retired.	Jundefinec
Implication	A performance counter counting instructions retired may over or under count. The count may not be consistent between multiple executions of the same code.	
Workaround	None identified.	ned
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Errata undefi	weer.	d undefined in	
od undeiti.	Status	For the steppings affected, see the Summary Tables of Changes.	
	tine	d S Cd ull	und
	020 : RF May B The Enclave SS	e Incorrectly Set In The EFLAGS That Is Saved To The Stack Or To A	defined
defined undef	Problem	After a page fault due to failed DS (debug store) save area address translation, the RF (resume flag) may be incorrectly set in the EFLAGS image that is saved to the stack or to the enclave SSA (State Save Area) in case of AEX (Asynchronous Enclave Exit)	
ndefined une	Implication	When this erratum occurs, a code breakpoint on the RIP of the instruction following a BTS (Branch Trace Store) trap will not be detected. In the case of AEX, it applies to the following enclave instruction.	sined un
AG	Workaround	None identified. The VMM and the OS should pin DS save area pages to avoid DS page faults	under.
ined und	Status	For the steppings affected, see the Summary Tables of Changes.	
indefit.		sined V.	-
A UII	021 · TA32 PFF	RF GLOBAL INUSE[62] May Be Non-Zero	

	7 01.	170
.80	Workaround	None identified. The VMM and the OS should pin DS save area pages to avoid DS page faults
ed une	Status	For the steppings affected, see the Summary Tables of Changes.
adefine		ined un
ined un.	021 : IA32_PE	RF_GLOBAL_INUSE[62] May Be Non-Zero
undefili	Problem	IA32_PERF_GLOBAL_INUSE[62] MSR (392H), which is a reserved bit, may contain a non-zero value when PEBS is enabled.
	Implication	Software reading IA32_PERF_GLOBAL_INUSE MSR and expects reserved bits to be zero, may see a non-zero value in bit 62.
isfined un	Workaround	Software must not rely on the value of reserved bits to always be zero.
dunde	Status	For the steppings affected, see the Summary Tables of Changes.
defined	c c	ned to a dunc
unde	022 : Intel PT (OVF Packet May Be Followed By TIP.PGD
	Broblem	Intol® Processor Trace internal buffer everflow that receives

Junes Jundefined undefined uni	022 : Intel PT 0	OVF Packet May Be Followed By TIP.PGD
	Problem	Intel® Processor Trace internal buffer overflow that resolves during a far transfer that changes bit 1 (ContextEn) in IA32_RTIT_STATUS (MSR 571H) from 1 to 0 may cause a TIP.PGD (Target IP Packet - Packet Generation Disabled) packet to be generated immediately following the OVF (Overflow) packet.
	Implication	The trace decoder may signal an error due to the OVF packet being followed by an unexpected TIP.PGD.
	Workaround	None identified.
d	ined und	Intol® Pontium® Silver and Intol® Coloron® Processors

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	ined undefined.	Errata
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od uli,	Status	For the steppings affected, see the Summary Tables of Changes.	
	eine	a sed un	d unde
	023 : Intel [®] PT	OVF Packet May Not Be Followed By A FUP Or TIP.PGE Packet	sined
ed unde	Problem	If Intel® PT (Processor Trace) encounters an internal buffer overflow and generates an OVF (Overflow) packet, in some rare cases that packet may not be immediately followed by the expected FUP (Flow Update Packet) or TIP.PGE (Target IP - Packet Generation Enabled) packet.	nder
ined undefine	Implication	An Intel® PT decoder may encounter a TNT (Taken Not Taken), TIP (Target IP), or other control flow packet immediately following an OVF packet.	٨
undefill	Workaround	An Intel® PT decoder should scan ahead to the next FUP, TIP, or TIP.PGE packet following the OVF to determine the current IP.	ofined une
	Status	For the steppings affected, see the Summary Tables of Changes.	auge.
unde	ý	ndefil's	_
iefineo	024 : PWRBTN_ Button Override	_STS And PWRBTNOR_STS Status Bits Not Set Following A Power e Event	

	Status	For the steppings affected, see the Summary Tables of Changes.	under.
undefined undefined unde		ndefil.	
	024 : PWRBTN Button Overrid	STS And PWRBTNOR_STS Status Bits Not Set Following A Power e Event	
	Problem	The PWRBTN_STS (bit 8) and PWRBTNOR _STS (bit 11) fields of PM1_STS_EN register (ABASE + 0x00) are incorrectly cleared on system wake following a Power Button Override Event.	71.
	Implication	System software is unable to detect the Power Button Override Event and may take the wrong boot path when Fastboot feature is enabled.	undefined L
	Workaround	A BIOS workaround has been identified.)
istineo	Status	For the steppings affected, see the Summary Tables of Changes.	

	eined	is enabled.	unde
und	Workaround	A BIOS workaround has been identified.	
iefine o	Status	For the steppings affected, see the Summary Tables of Changes.	
ed unoc		indein define	_
ie finec	025 : PM1_STS	_EN.WAK_STS Is Not Set Waking From A Valid Sleep Type	
3 unoc	Problem	PM1_STS_EN.WAK_STS (Bus 0; Device 0; Function 2; Offset 0h, Bit 15) is supposed to be set to '1' only upon exit from a valid sleep type (SLP_TYP). Due to this erratum, this bit is not set upon exit from a valid SLP_TYP.	undefined L
dung	Implication	SCI (System Control Interrupt) flows that read PM1_STS_EN.WAK_STS may not operate as expected.	
undefined	Workaround	The platform may use an alternate GPE (General Purpose Event) to signal Wake event from a given valid SLP_TYP. Software should clear WAK_STS prior to enabling a valid SLP_TYP.	
efined	Status	For the steppings affected, see the Summary Tables of Changes.	
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Errata	, ,	intel.	
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'ge,	026: Intel® Pro	cessor Trace Output May Over-write ToPA Output Region	red m.
	Problem	Due to a very rare microarchitectural condition, Intel® PT (Processor Trace) may over-write the most recently filled ToPA (Table of Physical Addresses) output region, rather than writing to the next ToPA output region.	
ndefined L	Implication	The trace will be corrupted and an Intel® PT decoder error is likely to result. Intel has only observed this erratum in a synthetic test environment.	
ined ur	Workaround	None identified.	
nden	Status	For the steppings affected, see the Summary Tables of Changes.	roed ur
	ed nu	Junde	
\ell_	027: IA32_PER	RF_GLOBAL_INUSE[PMI_InUse] Reports An Incorrect Value	

	Status	The state of the s	1260.
	ed un	4 unde	defill
ade	027: IA32_PER	RF_GLOBAL_INUSE[PMI_InUse] Reports An Incorrect Value	
undefined undefined und	Problem	IA32_PERF_GLOBAL_INUSE[PMI_InUse] (MSR 392H, bit 63) should be set when any performance monitoring counter is configured to cause a PMI (Performance Monitoring Interrupt) when it overflows or is configured to generate PEBS records. Due to this erratum, this bit may not be set if no counter is configured to generate a PMI on overflow and only fixed-function performance counters are configured to cause PEBS records to be generated.	, un
	Implication	Software relying on PMI_InUse may not operate correctly. Intel has not observed this erratum to affect any production software.	defined
	Workaround	None identified.	luc.
	Status	For the steppings affected, see the Summary Tables of Changes.	
		defined u.	1

		, ,
de	Workaround	None identified.
ed une	Status	For the steppings affected, see the Summary Tables of Changes.
adefine		ing ined un
		/M Entry Or VM Exit That Both Disables And Re-enables Intel® PT May ctable System Behavior
ined unde	Problem	If TraceEn[bit 0] and ToPA[bit 8] in IA32_RTIT_CTL (MSR 0570H) are set and if a single VM entry or VM exit uses the MSR load list to both clear TraceEn and then restore it, or if a VM exit caused by a VM entry failure clears TraceEn in the VM entry MSR load list and then restores it in the VM exit MSR load list, the Intel PT (Processor Trace) output may be written to an unexpected location within the ToPA (Table of Physical Addresses) tables or output regions or to an unpredictable memory location.
1	[mplication	Disabling and re-enabling Intel® PT during a single VM-exit, VM-entry, or failed VM-entry VM-exit, while using ToPA output can result in incorrect trace output or unpredictable system behavior.
· ·	Workaround	None identified. A hypervisor should take care to ensure that Intel® PT cannot be both disabled and re-enabled during VMX transitions when using ToPA output mode.
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vec	d undefined L	undefined Errata
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	029 : I2C TX_H	OLD Hold Time Specification May be Violated
bar	Problem	The processor may not meet the I2C specification minimum hold time for TX_HOLD on the PMIC I2C interface (PMIC I2C TX_HOLD parameter)
undefined undefined b	Implication	The I2C TX_HOLD time specification may not be met for the PMIC I2C interface. Intel has not observed this erratum to affect any commercially available system.
	Workaround	None identified.
	Status Jeffin	For the steppings affected, see the Summary Tables of Changes.
	ed une	1 unde
	020 - System M	lay Experience Inability To Poet Or May Coace Operation Or

	ed un	4 Unos
inde	030 : System M Nonfunctioning	lay Experience Inability To Boot Or May Cease Operation Or Of LPC, I2C and GPIO Circuitry
18 fined b	Problem	Under certain conditions LPC, I2C and GPIO circuitry may stop functioning in the outer years of use.
undefined unde.	Implication	LPC circuitry that stops functioning may cause operation to cease or inability to boot. I2C circuitry that stops functioning may cause operation to cease. Intel has only observed this behavior in simulation. Designs that implement the LPC interface at 1.8V signal voltage are not affected by the LPC portion of this sighting. Clockrun Protocol is not mandatory for GLK designs with LPC circuitry operating at 1.8V. When the platform drives the GPIO pin low, GPIO's programmed with weak pull-up circuitry may fail to maintain a value above VIH when not actively driven.
ined un.	Workaround	It is possible for BIOS to contain a workaround for this erratum.
undein.	Status	For the steppings affected, see the Summary Tables of Changes.
Jundefined &		ed unde.
	031 : eMMC Cor	ntroller May Fail To Detect A CRC Error In HS400 Mode
	Problem	The eMMC controller may fail to detect a CRC error if a bit error occurs on the DATA3 signal during read operations when in eMMC

	ed n. Inoc	
031 : eMMC Con	ntroller May Fail To Detect A CRC Error In HS400 Mode	"sed"
Problem	The eMMC controller may fail to detect a CRC error if a bit error occurs on the DATA3 signal during read operations when in eMMC HS400 mode. CRC detection on other DATA signals is not impacted.	dundefille
Implication	The controller will not flag the CRC error to the driver or application, which could result in data integrity issues. Bit errors on eMMC DATA signals are not expected on platforms that follow Intel recommended design guidelines and tuning processes.	
Workaround	None identified. To mitigate the issue, eMMC HS200 mode can be used instead of HS400.	
Status 👌	For the steppings affected, see the Summary Tables of Changes.	ined
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Errata		undefined ndeinte	•
red undefil.	032 : Certain M	IPI Display Panels May Remain Blank	7
efill	Problem	Certain sizes of the "Type 39 Long Write DCS" MIPI command, typically used to configure the MIPI panel during POST, do not work as intended.	lefined u
fined undef	Implication	Due to this erratum, the MIPI display will remain blank due to the MIPI enable sequence timing out when the LP FIFO empty status register (LP_DATA_FIFO, BDF XYZ, offset 74h, bit 10) fails to indicate it is not empty. It can also be observed, that the type 39 packets are not transmitted properly on the link.	n O
, under.	Workaround	None Identified	
iefineo	Status	For the steppings affected, see the Summary Tables of Changes.	
	indei	define	-fined

.0'	033 : An Indire Byte Of A 4GB I	ct JMP Or Indirect CALL Whose Last Instruction Byte Is On The Last Region Of Memory May Lead To Unpredictable System Behavior
, undefined und	Problem	Under complex microarchitectural conditions when a near indirect JMP or near indirect Call whose last instruction byte is on the last byte of a 4GB region of memory and whose target is in the same 4GB space, incorrect instructions may execute leading to unpredictable system behavior.
defined	Implication	When this erratum occurs, unpredictable system behavior may occur.
und	Workaround	It is possible for BIOS to contain a workaround for this erratum.
	Status	For the steppings affected, see the Summary Tables of Changes.
adun)	"Inder" define

	Status	For the steppings affected, see the Summary Tables of Changes.	Mude
duno	,9	inder. define	_
16tines	034 : Processor	r Energy Usage Calculation May Be Incorrect	
offined uno	Problem	After an S3 exit with initial high core activity, the processor may not calculate energy usage correctly until c-states are entered.	
I Thops.	Implication	Due to this erratum, energy reported (Imon) may be lower than what was actually used.	is fined u
	Workaround	It is possible for BIOS to contain a workaround for this erratum	unde
ad un	Status	For the steppings affected, see the Summary Tables of Changes.	
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ndefined		defined under sined under	
isfined U.	035 : Unexpecto	ed #PF, #GP, #UD, Or Other Unpredictable System Behavior May	in.
ide	Problem	Under complex microarchitectural conditions, incorrect instruction bytes may be used for code with linear addresses bits 5:4 = 10b.	efined u.
dunder	Implication	When this erratum occurs, unpredictable system behavior may occur. This unpredictable behavior often results in an unexpected #PF, #GP or #UD exception which causes an application to unexpectedly close.	,nde
finect	Workaround	It is possible for BIOS to contain a workaround for this erratum	7
inde	Status	For the steppings affected, see the Summary Tables of Changes.	
		ed under	_
	036 : PEBS DLA	May Report Incorrect Value	ed u
	Problem	Due to a rare microarchitectural condition, a PEBS (Processor	defille

	54445	To the steppings uncered, see the summary rusies of changes.	
fined		3d unde	-
inge,	036 : PEBS DLA	May Report Incorrect Value	sed un
	Problem	Due to a rare microarchitectural condition, a PEBS (Processor Event-Based Sampling) record taken on a load instruction may report an incorrect value in the DLA (Data Linear Address) field.	ndefills
od uno	Implication	A software profiler may be confused by a PEBS record suggesting that the associated load accessed an address that it did not.	
efine	Workaround	None identified	
unde	Status	For the steppings affected, see the Summary Tables of Changes.	
fined		ed unde	<u>-</u>
"luge,	037 : System M	ay Hang Under Complex Conditions	ned v
	Problem	Under complex conditions, insufficient access control in graphics	defill

ofine of		Jed und	<u>-</u>
unde	037 : System M	lay Hang Under Complex Conditions	red u.
	Problem	Under complex conditions, insufficient access control in graphics subsystem may lead to a system hang or crash upon a register read.	undefill.
م لا	Implication	When this erratum occurs a system hang or crash may occur.	
Hineo	Workaround	It is possible for BIOS to contain a workaround for this erratum.	
unde.	Status	For the steppings affected, see the Summary Tables of Changes.	
sined b		ed une	
inder	038 : Intel® P1	TMA Packets Have Incorrect Payloads	ed u
900	Problem	Intel® PT (Processor Trace) TMA (TSC/MTC Alignment) packets hae incorrect values in both the CTC (Core Timer Copy) and FC (Fast	indefine

*ineo		ed ui.	
inder.	038 : Intel® PT	TMA Packets Have Incorrect Payloads	ed u
3	Problem	Intel® PT (Processor Trace) TMA (TSC/MTC Alignment) packets hae incorrect values in both the CTC (Core Timer Copy) and FC (Fast Counter) fields. The FC value is always zero.	undefine
ed une	Implication	In Intel® PT decoder will be confused when using the TMA packet to align cycle time with wall-clock time.	
efines	Workaround	It is possible for BIOS to contain a workaround for this erratum.	
IInde	Status	For the steppings affected, see the Summary Tables of Changes.	
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Specification Clarifications

iden.	001: Power Lea	akage during system boot	efined	Astined un
Indefined undefined un	Implication	Intel® Pentium™ and Intel® C may exhibit power leakage on I milliseconds before platform po	eleron™ J and N Series processors \\^ P1V8A platform rail within few	36.
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Intel® Pention Specification	um® Silver and Intel® Ce n Update	eron® Processors	October 2020	O.
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Documentation Changes There are no documentation changes in this review underned under ned underned under under

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