Intel® 300 Series and Intel® C240 Series Chipset Families Platform Controller Hub

Specification Update

August 2022

Revision 012

Document Number: 337349-012

Contents

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Revision History

Revision	Description	Date
001	• Initial Release	May 2018
002	• The following errata are added: — DbC (Debug Capability) Device Fails To Enumerate When Connected To USB 3.1 Gen 2 Port — SDXC CRC Detection • The following errata are removed: — PCH PCIe* Controller Root Port Access Control Services Control Register (ACSCTLR) Appears As Read Only.	September 2018
003	• Added Z390 • Updated S-Spec for H310 • Added S-Spec for C242 and C246 • The following errata are added: — LPC Turn-Around Cycle Droop — Intel® Trace Hub Pipe Line Empty	December 2018
004	• Updated xHCI Minor Revision Value • The following errata are added: — SD_VDD1_PWR_EN# Is Always Asserted — SPI SFDP Program Suspend And Program Resume Instruction Fields Not Used — PCIe Root Port CLKREQ# Asserted Low To Clock Active Timing	January 2019
005	• The following erratum is added: — CLKOUT_LPC[1:0] t157 Violation With CLKRUN# Enabled	March 2019
006	• The following errata is added: — xHCI USB 2.0 ISOCH Device Missed Service Interval — xHCI Link Protocol Field Value	August 2019
007	• Removed erratum 1.	September 2019
008	• The following errata is added: — xHCI Short Packet Event Using Non-Event Data TRB — eSPI SBLCL Register Bit Not Cleared by PLTRST#	November 2019
009	• The following errata added:- — USB DbC or Device Mode Port When Resuming from S3, S4, S5, or G3 State — xHCI Power Management Link Timer — DbC (Debug Capability) Device Fails to Enumerate When Connected to USB 3.2 Gen 2x1 Port — xHCI Protocol Speed ID Count Field — System May Hang With USB-C* Power Adapter — SATA Enclosure Management LED Messaging	February 2020
010	• The following errata added:- — Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment — SLP_WLAN# and SLP_A# May Re-assert following G3 or Deep Sx Exits — Audio Global Time Synchronization Register Access — Phase Lock Loop (PLL) Feedback Circuit — DMI High Speed Clock Duty Cycle • The following specification clarification added:- — PCIe Precision Time Measurement (PTM) Byte Order — SX_EXIT_HOLDOFF# Not Functional with eSPI Enabled — xHCI D3 Exit Timing	July 2021
011	• The following specification clarification added:- — Leakage Current from VCCPRIM_1P8 Power Rail	February 2022

Revision	Description	Date
012	• The following errata added:- — USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst — G3 Current Specification on VCCRTC Rail — Timed GPIO Event May Have a Mismatched Time Stamp	August 2022

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Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation errata and specification changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents

Title	Document Number
Intel® 300 Series and Intel® C240 Series Chipset Families Platform Controller Hub Datasheet	337347 (Vol 1) 337348 (Vol 2)

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

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Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Stepping

X:	Erratum exists in the stepping indicated. Specification Change that applies to the stepping indicated.
(No mark) or (Blank box):	This erratum is fixed or not applicable in listed stepping or Specification Change does not apply to listed stepping.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Errata

Erratum Number	Stepping	Status	Errata
	B0		
1		N/A	N/A. Erratum has been removed.
2	X	No Plan to Fix	xHCI Host Controller Reset May Cause A System Hang
3	X	No Plan to Fix	Intermittent CATERR May Occur When Back To Back xHCI Host Controller Resets Are Performed
4	X	No Plan to Fix	USB DbC Or Device Mode Port When Resuming From S3, S4, S5, Or G3 State
5	X	No Plan to Fix	xHCI Minor Revision Value
6	X	No Plan to Fix	xHCI Link Error Count Field
7	X	No Plan to Fix	xHCI U1 Exit LFPS Duration
8	X	No Plan to Fix	xHCI Power Management Link Timer
9	X	No Plan to Fix	DbC (Debug Capability) Device Fails To Enumerate When Connected To USB 3.1 Gen 2 Port
10	X	No Plan to Fix	SDXC CRC Detection
11	X	No Plan to Fix	LPC Turn-Around Cycle Droop
12	X	No Plan to Fix	Intel® Trace Hub Pipe Line Empty
13	X	No Plan to Fix	SD_VDD1_PWR_EN# Is Always Asserted
14	X	No Plan to Fix	SPI SFDP Program Suspend And Program Resume Instruction Fields Not Used
15	X	No Plan to Fix	PCIe Root Port CLKREQ# Asserted Low To Clock Active Timing
16	X	No Plan to Fix	CLKOUT_LPC[1:0] t157 Violation With CLKRUN# Enabled
17	X	No Plan to Fix	xHCI USB 2.0 ISOCH Device Missed Service Interval
18	X	No Plan to Fix	xHCI Link Protocol Field Value
19	X	No Plan to Fix	USB DbC or Device Mode Port When Resuming from S3, S4, S5, or G3 State
20	X	No Plan to Fix	xHCI Power Management Link Timer
21	X	No Plan to Fix	DbC (Debug Capability) Device Fails to Enumerate When Connected to USB 3.2 Gen 2x1 Port
22	X	No Plan to Fix	xHCI Protocol Speed ID Count Field
23	X	No Plan to Fix	System May Hang With USB-C* Power Adapter
24	X	No Plan to Fix	SATA Enclosure Management LED Messaging
25	X	No Plan to Fix	Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment
26	X	No Plan to Fix	SLP_WLAN# and SLP_A# May Re-assert following G3 or Deep Sx Exits
27	X	No Plan to Fix	Audio Global Time Synchronization Register Access
28	X	No Plan to Fix	Phase Lock Loop (PLL) Feedback Circuit
29	X	No Plan to Fix	DMI High Speed Clock Duty Cycle
30	X	No Plan to Fix	Leakage Current from VCCPRIM_1P8 Power Rail
31	X	No Plan to Fix	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
32	X	No Plan to Fix	G3 Current Specification on VCCRTC Rail
33	X	No Plan to Fix	Timed GPIO Event May Have a Mismatched Time Stamp

Identification Information

Specification Changes

Number	Stepping	Specification Changes
	B0	
		No specification changes in this revision of the Specification Update

Specification Clarification

Number	Specification Clarifications
1	PCIe Precision Time Measurement (PTM) Byte Order
2	SX_EXIT_HOLDOFF# Not Functional with eSPI Enabled
3	xHCI D3 Exit Timing

Markings

PCH Stepping	Top Marking (S-Spec)	Notes
B0	SR404	Desktop Intel® Chipset Q370
B0	SR405	Desktop Intel® Chipset H370
B0	SR408	Desktop Intel® Chipset B360
B0	SRCXY	Desktop Intel® Chipset H310
B0	SR40E	Mobile Intel® Chipset CM246
B0	SR40D	Mobile Intel® Chipset QM370
B0	SR40B	Mobile Intel® Chipset HM370
B0	SR406	Desktop Intel® Chipset Z390
B0	R40C	Workstation / Server Intel® Chipset C242
B0	R40A	Workstation / Server Intel® Chipset C246

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Errata

1. N/A. Erratum has been removed.

2. xHCI Host Controller Reset May Cause A System Hang

Problem: xHCI Host Controller may not respond following system software setting (Bit 1 = '1') the Host Controller Reset (HCRST) of the USB Command Register (xHCIBAR + 80h).

Implication: CATERR may occur resulting in a system hang.

Workaround: A 1ms delay is necessary anytime following System Software setting (Bit 1 = '1') Host Controller Reset (HCRST) of the USB Command Register (xHCIBAR + 80h).

Status: No Plan To Fix.

3. Intermittent CATERR May Occur When Back To Back xHCI Host Controller Resets Are Performed

Problem: The xHCI host controller may fail to respond, due to an internal race condition, if consecutive Host Controller resets are performed.

Implication: A processor CATERR may occur during warm boot testing or S4/S5 cycling tests.

Workaround: Software should add a 120 ms delay in between consecutive host controller resets.

Status: No Plan to Fix.

4. USB DbC Or Device Mode Port When Resuming From S3, S4, S5, Or G3 State

Problem: If a PCH USB Type-C* port is configured in Device Mode (or in DbC mode) and connected to an external USB 3.1 host controller, it may cause the USB port to go into a non-functional state in the following scenarios:

1. The PCH resumes from S3, S4, or S5 state, the port may remain in U2.
2. The port is connected to a USB 3.1 Gen 1 host controller when resuming from S3, S4, S5, or G3, the port may enter into Compliance Mode or an inactive state if Compliance mode is disabled.
3. The port is connected to a USB 3.1 Gen 2 host controller when resuming from S3, S4, S5, or G3, the port may enter an inactive state.

Implication: PCH USB Type-C port configured in Device Mode (or in DbC mode) may fail to enumerate or become unavailable.

Workaround: None.

Status: No Plan to Fix.

5. xHCI Minor Revision Value

Problem: The PCH reports USB Minor Revision in the XECP_SUPP_USB3_0 register (offset 8020h) as 01h. The USB-IF released a ECN to update the minor revision to 0x10h.

Implication: USB-IF xHCI CV TD 1.5 may report a failure. Intel has obtained a waiver for TD 1.5.

Note: No functional impact is expected.

Workaround: None.

Status: No Plan to Fix.

6. xHCI Link Error Count Field

Problem: The xHCI Link Error Count Field in the USB 3.0 Port X Link Info – (PORTLI) register is implemented as Read/Write instead of Read Only as defined by the xHCI specification.

Implication: USB-IF xHCI CV TD 3.17 may report a failure. Intel has obtained a waiver for TD 3.17.

Note: No functional impact is expected.

Workaround: None.

Status: No Plan to Fix.

7. xHCI U1 Exit LFPS Duration

Problem: The xHCI U1 Exit LFPS (t13-t11) duration timing is implemented as 0.6 us to 0.9 us. The USB-IF released a ECN updating this timing value to 0.9 us to 1.2 us.

Implication: USB-IF xHCI CV TD 7.18 may report a failure. Intel has obtained a waiver for TD 7.18.

Note: No functional issues are expected.

Workaround: None.

Status: No Plan to Fix.

8. xHCI Power Management Link Timer

Problem: The xHCI implements the Power Management Link Timer (PM LC Timer) Timeout value as 10 us instead of 4 us as defined by the USB 3.1 specification.

Implication: USB-IF xHCI CV TD 7.21 may report a failure. Intel has obtained a waiver for TD 7.21.

Note: No functional issues are expected.

Workaround: None.

Status: No Plan to Fix.

9. DbC (Debug Capability) Device Fails To Enumerate When Connected To USB 3.1 Gen 2 Port

Problem: The PCH DbC (Debug Capability) Device may fail to enumerate if connected to a USB host controller's USB 3.1 Gen 2 port.

Implication: The PCH DbC may not function.

Workaround: None.

Status: No Plan to Fix.

10. SDXC CRC Detection

Problem: The PCH DbC (Debug Capability) Device may fail to enumerate if connected to a USB host controller’s USB3.1 Gen 2 port.

Implication: The PCH DbC may not function.

Workaround: None.

Status: No Plan to Fix.

11. LPC Turn-Around Cycle Droop

Problem: During the turn-around cycle where the PCH transfers ownership of the LPC LAD[3:0] signals to another device, a race condition may occur where the PCH LPC controller may improperly disable its output buffers.

Implication: During this condition, the voltage on LAD[3:0] may be observed to temporarily droop to below V_{IH} min from the 1st to 2nd clock of the turnaround cycle. There are no known functional failures due to this issue.

Workaround: None.

Status: No Plan to Fix.

12. Intel® Trace Hub Pipe Line Empty

Problem: The Intel® Trace Hub Pipe Line Empty bit (CSR_MTB_BAR, Offset D4h) for a given output port may be set while the Input Buffer Empty for the associated output port is not set. This will only happen when the captureDone signal is de-asserted by clearing the ForceCaptureDone bit (CSR_MTB_BAR, Offset D8h) is cleared or the StoreQual[0] signal is de-asserted by the Trigger Unit before the pipe line is empty, and the destination is either system memory or USB (DCI).

Implication: There may be valid trace data in the trace source input buffer which did not get sent to the destination (output port).

Workaround: None. CaptureDone should be cleared or de-asserted after the pipe line is empty.

Status: No Plan to Fix.

13. SD_VDD1_PWR_EN# Is Always Asserted

Problem: SD_VDD1_PWR_EN# does not de-assert during SDXC D3 or when SD card is not inserted.

Implication: For platforms using SD_VDD1_PWR_EN#, the SDXC card connector is always powered and may impact system power.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Plan to Fix.

14. SPI SFDP Program Suspend And Program Resume Instruction Fields Not Used

Problem: For flash device suspend / resume opcodes, the SPI controller does not use JEDEC SFDPs 13th DWORD bits [15:0], Program Suspend Instruction and Program Resume Instruction fields. The controller only uses bits [31:16], Suspend Instruction and Resume Instruction fields, to obtain the suspend / resume opcodes.

Implication: If the SPI flash requires bits [15:0] to be different than bits [31:16], then the suspend / resume feature is not functional. In this case, system behavior varies depending on what the suspend / resume instruction is and when it is generated.

Note: Major flash vendors have been using the same value for bits [31:16] and bits [15:0].

Workaround: None.If a device requires bits [15:0] to be different than bits [31:16], then disable the device suspend / resume via the SPI Suspend / Resume Enable soft strap.

Status: No Plan to Fix.

15. PCIe Root Port CLKREQ# Asserted Low To Clock Active Timing

Problem: During L1 exit, the PCH PCIe Root Ports may exceed the CLKREQ# asserted low to clock active maximum specification due to PCH PCIe clock un-gate path delays.

Implication: PCIe end point device L1 exit instabilities may be observed.

Note: PCIe end point devices that message LTR latency greater than or equal to 1 µs are not affected by this.

Workaround: None.

- Platforms not supporting S0ix with PCIe end point devices that do not support LTR may disable the associated PCH SRCCLKREQ# signal to keep the PCIe clock active during L1.
- Platforms supporting S0ix with PCIe end point devices that have LTR latencies less than 1 µs may disable the associated PCH SRCCLKREQ# signal to keep the PCIe clock active during L1.

Status: No Plan to Fix.

16. CLKOUT_LPC[1:0] t157 Violation With CLKRUN# Enabled

Problem: With CLKRUN# enabled, the PCH may exceed the t157 timing, LFRAME# Valid Delay from CLKOUT_LPC[1:0] Rising.

Implication: A LPC device may not observe the initial transaction from the PCH when CLKOUT_LPC is being re-started following the assertion of CLKRUN# by PCH.

Workaround: A Platform Firmware code change has been identified and may be implemented as a workaround for this erratum.

Status: No Plan to Fix.

17. xHCI USB 2.0 ISOCH Device Missed Service Interval

Problem: When the xHCI controller is stressed with concurrent traffic across multiple USB ports, the xHCI controller may fail to service USB 2.0 Isochronous IN endpoints within the required service interval.

Implication: USB 2.0 isochronous devices connected to the xHCI controller may experience dropped packets.

Note: This issue has only been observed in a synthetic environment.

Workaround: None.

Status: No Plan to Fix.

18. xHCI Link Protocol Field Value

Problem: The xHCI Host Controller reports the Link Protocol (LP) bits [15:14] as 0x0h in the XECP_SUPP_USB3_5 Super Speed Plus register (xHCI MMIO offset 8034h). The xHCI spec rev 1.1 (published in Nov. 2017) defines this bit should be set to 0x1h for SuperSpeed USB 10 Gbps port.

Implication: USB-IF xHCI CV TD 1.9 may report a failure. The failure was not observed during the USB certification for the xHCI USB host controller and thus a waiver was not required.

Note: No functional impact is expected.

Workaround: None.

Status: No Plan to Fix.

19. USB DbC or Device Mode Port When Resuming from S3, S4, S5, or G3 State

Problem: If a PCH USB Type-C* port is configured in Device Mode (or in DbC mode) and connected to an external USB 3.2 host controller, it may cause the USB port to go into a non-functional state in the following scenarios: 1)The PCH resumes from S3, S4, or S5 state, the port may remain in U2. 2)The port is connected to a USB 3.2 Gen 1x1 host controller when resuming from S3, S4, S5, or G3, the port may enter into Compliance Mode or an inactive state if Compliance Mode is disabled. 3)The port is connected to a USB 3.2 Gen 2x1 host controller when resuming from S3, S4, S5, or G3, the port may enter an inactive state.

Implication: PCH USB Type-C* port configured in Device Mode (or in DbC mode) may fail to enumerate or become unavailable.

Workaround: None identified.

Status: No Plan to Fix.

20. xHCI Power Management Link Timer

Problem: The xHCI implements the Power Management Link Timer (PM LC Timer) Timeout value as 10 us instead of 4 us as defined by the USB 3.2 specification.

Implication: USB-IF xHCI CV TD 7.21 may report a failure. Intel has obtained a waiver for TD 7.21. Note: No functional issues are expected.

Workaround: None identified.

Status: No Plan to Fix.

21. DbC (Debug Capability) Device Fails to Enumerate When Connected to USB 3.2 Gen 2x1 Port

Problem: The PCH DbC (Debug Capability) Device may fail to enumerate if connected to a USB host controller's USB 3.2 Gen 2x1 port.

Implication: The PCH DbC may not function.

Workaround: None identified.

Status: No Plan to Fix.

22. xHCI Protocol Speed ID Count Field

Problem: The xHCI Host Controller reports an incorrect Protocol Speed ID Count value for the USB 3.2 Supported Protocol Capability register - xHCI MMIO offset 8028 bits [31:28].

Implication: USB-IF xHCI CV TD 1.9 may report a failure. Note: No functional impact is expected.

Workaround: None identified.

Status: No plan to Fix.

23. System May Hang With USB-C* Power Adapter

Problem: Connecting a USB-C* power adapter to a PCH USB port may cause a race condition that can result in a xHCI controller hang. This issue only occurs on designs where the USB-C Power Delivery (PD) implements OOB messaging to communicate with the PCH for port mapping.

Implication: The system may hang. Note: This issue does not occur when the system is in Sx state and has only been observed when repeatedly connecting a USB-C power adapter.

Workaround: None identified.

Status: No plan to Fix.

24. SATA Enclosure Management LED Messaging

Problem: When sending a SATA enclosure LED message and all SATA ports are either idle or disabled, the PCH may not transmit the LED message due to an internal clock gating issue.

Implication: The LED status for SATA enclosure may be incorrect.

Workaround: None Identified. Enclosure Management SW can poll the Enclosure Management (EM_CTL) - Offset 20h bit 8 register for a 0 value immediately before writing LED messages.

Status: No plan to Fix.

25. Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment

Problem: If software assigns a 4 GB-aligned address to the Linked List Pointer (LLP_LOn = 0h) for Intel® Serial I/O Controller DMA engine, then the DMA engine interprets this as an empty link list and will not perform DMA transfers.

Implication: An Intel® Serial I/O Controller (i.e., I2C, GSPI, or UART) may stop operating which may cause the system to hang.

Workaround: Driver software should not assign LLP to a 4 GB-aligned address. Note: This issue has been addressed in the Intel® Serial I/O drivers in the following versions or later: For Microsoft Windows* 10, I2C device driver rev 30.100.1724.2, SPI device driver rev 30.100.1725.1, and UART device driver rev 30.100.1725.1

Status: No plan to Fix.

26. SLP_WLAN# and SLP_A# May Re-assert following G3 or Deep Sx Exits

Problem: Following G3 or Deep Sx exits, SLP_WLAN# and SLP_A# may re-assert for approximately 2 ms.

Implication: System implication is platform implementation-specific.Note: Intel observed that SLP_WLAN# reassertion may cause a WLAN power well voltage ripple resulting in WLAN device not enumerating.

Workaround: None identified. The platform Embedded Controller (EC) may implement a 10 ms timer to mask this behavior.

Status: No plan to Fix.

27. Audio Global Time Synchronization Register Access

Problem: Disabling the audio DSP through the Intel® High Definition Audio Function Configuration Register Offset 530h in the PCH Private Configuration Space by setting bit 2 to '1' will block accesses to the Audio Global Time Synchronization registers in the MMIO space (Offset 500h - 55Fh)

Implication: Audio Global Time Synchronization registers may not be accessible and any attempted accesses may result in a system hang.

Workaround: None identified.

Status: No plan to Fix.

28. Phase Lock Loop (PLL) Feedback Circuit

Problem: The Main PLL and USBPCIe PLL have independent feedback circuits. A feedback circuit timing marginality may result in a momentary jitter excursion in the corresponding PLL and downstream circuitry.

Implication: If the Main PLL loses lock, then the system may hang. If the USBPCIe PLL loses lock, USB 3.1 / SATA / PCIe / integrated GbE / DMI / CLKOUT_PCIE interfaces may experience errors, including correctable errors, interface down trains, or hangs.

Workaround: A fix for this erratum is available with a combination of updates in the Chipset_Init merged into BIOS and the Intel® Converged Security and Management Engine (Intel® CSME) FW. Please see code change for Chipset_Init version BxV13 in kit# 136494 based on BIOS version 216.1 or later. Additionally, please see the Intel CSME version 12.0.68.1606 FW package or later.

Status: No plan to Fix.

29. DMI High Speed Clock Duty Cycle

Problem: Internal PCH noise occurring during S3, S4, S5 transitions may cause an incorrect setting to be selected for the duty cycle of the DMI high speed clock.

Implication: DMI clock speed may downgrade to Gen 1 speed and the system may hang.

Workaround: A fix for this erratum is available with a combination of Chipset_Init and PMC. Please see the PMC FW Hot Fix 300.2.11.1024 for CNL PCH-H Platforms, Kit #134742 or later. Additionally, please use Chipset_Init version 10 or later.

Status: No plan to Fix.

30. Leakage Current from VCCPRIM_1P8 Power Rail

Problem: When the VCCPRIM_1P8 is off and the VCCPRIM_3P3 is powered on during G3 to S5, there may be a leakage current from the VCCPRIM_3P3 power rail to VCCPRIM_1P8 power rail.

Implication: The leakage voltage may be observed on VCCPRIM_1P8 power rail. There is no known functional or reliability impact.

Workaround: None identified.

Status: No plan to Fix.

31. USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst

Problem: On USB 3.2 Gen 1x1 capable ports, including ports configured as USB 3.2 Gen 1x1 by soft strap, the xHCI controller may send only 15 LFPS signals instead of a burst of 16 LFPS signals as specified by the USB 3.2 specification.

Implication: There are no known functional implications due to this erratum. LFPS handshake requires the receiver link partner to only detect 2 LFPS signals. This issue may impact the SuperSpeed compliance test case which checks for the 16 LFPS burst requirements: TD6.4, TD6.5, and TD7.31.

Workaround: None identified.

Status: No Plan to Fix.

32. G3 Current Specification on VCCRTC Rail

Problem: The PCH VCCRTC current draw during the G3 state may exceed the maximum current specification of 6 µA, as documented in the Intel® 300 Series and Intel® C240 Series Chipset Families Platform Controller Hub Datasheet – Volume 1 of 2 (Document number: 337347).

Implication: PCH units may experience VCCRTC rail current draw during the G3 state up to 8 uA. Platform implications are platform design specific.

Workaround: None identified.

Status: No Plan to Fix.

33. Timed GPIO Event May Have a Mismatched Time Stamp

Problem: When a Timed GPIO event is counted in the Event Counter Capture (TGPIOECCV) register (offset 1238h, bits 31 to 0 in PWRMBASE space), the Time Capture (TGPIOTCV) register (offset 1230h, bits 31 to 0 in PWRMBASE space) value is not immediately updated after that event is counted.

Implication: A Timed GPIO event may have a mismatched time stamp.

Workaround: None identified. A Timed GPIO driver can partially mitigate for this erratum by detecting that a TGPIOECCV register change has occurred without a TGPIOTCV register change and then repeatedly re-read the TGPIOTCV register until a change does occur.

Status: No Plan to Fix.

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Specification Changes

There are no Specification Changes in this revision of the Specification Update.

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Specification Clarifications

1. PCIe Precision Time Measurement (PTM) Byte Order

Add the following note to the Intel 300 Series and Intel C240 Series Chipset Family Platform Controller Hub Datasheet Volume 1 "Precision Time Measurement (PTM)" section:

•PCIe Root Ports transmit the lower byte [7:0] of the Propagation Delay Field first instead of the upper byte [31:24] within their PTM DelayResponseD (Response with Data) messages.

2. SX_EXIT_HOLDOFF# Not Functional with eSPI Enabled

Add the following note to the Intel® 300 Series and Intel® C240 Series Chipset Families Platform Controller Hub Datasheet Volume 1 (#337347) in the SX_EXIT_HOLDOFF# Signal Description in Section 27.4 table:

•“Note: When eSPI is enabled, SX_EXIT_HOLDOFF# functionality is not available, and assertion of the signal will not impact Sx exit flows.”

3. xHCI D3 Exit Timing

Add the following text to the Intel 300 Series Chipset Families Platform Controller Hub Datasheet Volume 2 of 2 (#337348) in the Power Management Control/Status (PM_CS) register summary, bits 1:0, 'PowerState (POWERSTATE)' field description section:

•"Software should wait for 100 ms before requesting the xHCI controller to re-enter D3 after a D3 exit."

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