Intel® 495 Series Chipset Family On-Package Platform Controller Hub (PCH)

Specification Update

Revision 015

August 2022

Document Number: 341082

Contents

Revision History

Revision Number	Description	Release Date
001	• Initial Release	August 2019
002	• The following errata are added: — xHCI CV TD 2.2 Interrupter Handling — xHCI Link Protocol Field Value	October 2019
003	• The following errata are added: — xHCI Short Packet Event Using Non-Event Data TRB — eSPI SBLCL Register Bit Not Cleared By PLTRST#	November 2019
004	• Updated: — USB DbC Or Device Mode Port When Resuming From S3, S4, S5, or G3 StatexHCI Power Management Link Timer • The following errata are added: — Leakage On VCC_VNNEXT_1P05 Power Rail With External Bypass VR — xHCI Protocol Speed ID Count Field	December 2019
005	• The following erratum is added: — System May Hang with USB-C* Power Adapter	January 2020
006	• The following erratum is added: — Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment	April 2020
007	• The following specification clarification is added: — PCIe Precision Time Measurement (PTM) Byte Order	May 2020
008	• The following erratum is added: — Audio Global Time Synchronization Register Access	July 2020
009	• The following erratum is added: — S0ix Entry When Connecting an USB-C* Power Adapter	August 2020
010	• The following errata are added: — FIVR Clock Frequency Variation — Phase Lock Loop (PLL) Feedback Circuit	September 2020
011	• The following erratum is added: — Time Synchronization with xHCI and GbE	October 2020
012	• The following errata are added: — SATA Controller Support for Automatic Partial to Slumber Transition (APST) Feature — Internal Clocking Phase Lock Loop (PLL) Locking — Increased PCIe* Gen1 RX L0s Exit Latencies • The following Specification Clarification is added: — SX_EXIT_HOLDOFF# Not Functional with eSPI Enabled	November 2020
013	• The following Specification Clarification is added: — xHCI D3 Exit Timing	September 2021

Revision Number	Description	Release Date
014	• The following errata is updated: — FIVR Clock Frequency Variation	November 2021
015	• The following errata are added: — Leakage Current from VCCPRIM_1P8 Power Rail — USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst — Timed GPIO Event May Have a Mismatched Time Stamp — G3 Current Specification on VCCRTC Rail	August 2022

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Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation errata, specification clarifications, and document changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents

Document Title	Document Number
Intel® 495 Series Chipset Family On-Package Platform Controller Hub (PCH) Datasheet	341080 (Vol1) 341081 (Vol2)

Nomenclature

Errata – These are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes – These are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications – This describes a specification in greater detail or further highlights a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes – These include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

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Summary Tables of Changes

The following tables indicate the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the product. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. These tables use the following notations:

Codes Used in Summary Table

Stepping	Description
(No mark) or (Blank Box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status	Description
Doc	Document change or update that is implemented.
Planned Fix	This erratum may be fixed in a future stepping of the product.
Fixed	This erratum has been previously fixed in Intel hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

Errata Summary Table

Erratum ID	Stepping	Errata
	A0	
1	No Fix	USB DbC Or Device Mode Port When Resuming from S3, S4, S5, or G3 State
2	No Fix	xHCI U1 Exit LFPS Duration
3	No Fix	xHCI Power Management Link Timer
4	No Fix	xHCI USB 2.0 ISOCH Device Missed Service Interval
5	No Fix	SPI SFDP Program Suspend and Program Resume Instruction Fields Not Used
6	No Fix	Intel® Trace Hub Pipe Line Empty
7	No Fix	PCIe* Root Port CLKREQ# Asserted Low to Clock Active Timing
8	No Fix	xHCI CV TD 2.2 Interrupter Handling

Erratum ID	Stepping	Errata
	A0	
9	No Fix	xHCI Link Protocol Field Value
10	No Fix	xHCI Short Packet Event Using Non-Event Data TRB
11	No Fix	eSPI SBLCL Register Bit Not Cleared By PLTRST#
12	No Fix	Leakage On VCC_VNNEXT_1P05 Power Rail With External Bypass VR
13	No Fix	xHCI Protocol Speed ID Count Field
14	No Fix	System May Hang with USB-C* Power Adapter
15	No Fix	Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment
16	No Fix	Audio Global Time Synchronization Register Access
17	No Fix	S0ix Entry When Connecting an USB-C* Power Adapter
18	No Fix	FIVR Clock Frequency Variation
19	No Fix	Phase Lock Loop (PLL) Feedback Circuit
20	No Fix	Time Synchronization with xHCI and GbE
21	No Fix	SATA Controller Support for Automatic Partial to Slumber Transition (APST) Feature
22	Fixed	Internal Clocking Phase Lock Loop (PLL) Locking
23	Fixed	Increased PCIe* Gen1 RX L0s Exit Latencies
24	No Fix	Leakage Current from VCCPRIM_1P8 Power Rail
25	No Fix	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
26	No Fix	Timed GPIO Event May Have a Mismatched Time Stamp
27	No Fix	G3 Current Specification on VCCRTC Rail

Specification Change

No.	Specification Changes
	None for this revision of this specification update.

Specification Clarifications

No.	Specification Clarifications
1	PCIe Precision Time Measurement (PTM) Byte Order
2	SX_EXIT_HOLDOFF# Not Functional with eSPI Enabled
3	xHCI D3 Exit Timing

Documentation Changes

No.	Documentation Changes
	None for this revision of this specification update.

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Errata Details

1. USB DbC Or Device Mode Port When Resuming from S3, S4, S5, or G3 State

Problem: If a PCH USB 3.2 Type-C port is configured in Device Mode (or in DbC mode) and connected to an external USB 3.2 host controller, it may cause the USB port to go into a non-functional state in the following scenarios:

1. The PCH resumes from S3, S4, or S5 state, the port may remain in U2.
2. The port is connected to a USB 3.2 Gen 1x1 host controller when resuming from S3, S4, S5, or G3, the port may enter into Compliance Mode or an inactive state if Compliance mode is disabled.
3. The port is connected to a USB 3.2 Gen 2x1 host controller when resuming from S3, S4, S5, or G3, the port may enter an inactive state.

Implication: PCH USB Type-C port configured in Device Mode (or in DbC mode) may fail to enumerate or become unavailable.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

2. xHCI U1 Exit LFPS Duration

Problem: The xHCI U1 Exit LFPS (t13-t11) duration timing is implemented as 0.6 us to 0.9 us. The USB-IF released an ECN updating this timing value to 0.9 us to 1.2 us.

Implication: USB-IF xHCI CV TD 7.18 may report a failure. Intel has obtained a waiver for TD 7.18.

NOTE: No functional issues are expected.

Workaround: None.

Status: For the steppings affected, refer to the Summary Tables of Changes.

3. xHCI Power Management Link Timer

Problem: The xHCI implements the Power Management Link Timer (PM LC Timer) Timeout value as 10 us instead of 4 us as defined by the USB 3.2 specification.

Implication: USB-IF xHCI CV TD 7.21 may report a failure. Intel has obtained a waiver for TD 7.21.

NOTE: No functional issues are expected.

Workaround: None.

Status: For the steppings affected, refer to the Summary Tables of Changes.

4. xHCI USB 2.0 ISOCH Device Missed Service Interval

Problem: When the xHCI controller is stressed with concurrent traffic across multiple USB ports, the xHCI controller may fail to service USB 2.0 Isochronous IN endpoints within the required service interval.

Implication: USB 2.0 isochronous devices connected to the xHCI controller may experience dropped packets.

NOTE: This issue has only been observed in a synthetic environment.

Workaround: None.

Status: For the steppings affected, refer to the Summary Tables of Changes.

5. SPI SFDP Program Suspend and Program Resume Instruction Fields Not Used

Problem: For flash device suspend/resume opcodes, the SPI controller does not use JEDEC SFDPs 13th DWORD bits [15:0], Program Suspend Instruction and Program Resume Instruction fields. The controller only uses bits [31:16], Suspend Instruction and Resume Instruction fields, to obtain the suspend/resume opcodes.

Implication: If the SPI flash requires bits [15:0] to be different than bits [31:16], then the suspend /resume feature is not functional. In this case, system behavior varies depending on what the suspend/resume instruction is and when it is generated.

NOTE: Major flash vendors have been using the same value for bits [31:16] and bits [15:0].

Workaround: None.

If a device requires bits [15:0] to be different than bits [31:16], then disable the device suspend / resume via the SPI Suspend / Resume Enable soft strap.

Status: For the steppings affected, refer to the Summary Tables of Changes.

6. Intel® Trace Hub Pipe Line Empty

Problem: The Intel® Trace Hub Pipe Line Empty bit (CSR_MTB_BAR, Offset D4h) for a given output port may be set while the Input Buffer Empty for the associated output port is not set. This will only happen when the captureDone signal is de-asserted by clearing the ForceCaptureDone bit (CSR_MTB_BAR, Offset D8h) is cleared or the StoreQual[0] signal is de-asserted by the Trigger Unit before the pipe line is empty, and the destination is either system memory or USB (DCI).

Implication: There may be valid trace data in the trace source input buffer which did not get sent to the destination (output port).

Workaround: None.

CaptureDone should be cleared or de-asserted after the pipe line is empty.

Status: For the steppings affected, refer to the Summary Tables of Changes.

7. PCIe* Root Port CLKREQ# Asserted Low to Clock Active Timing

Problem: During L1 exit, the PCH PCIe* Root Ports may exceed the CLKREQ# asserted low to clock active maximum specification due to PCH PCIe clock un-gate path delays.

Implication: PCIe end point device L1 exit instabilities may be observed.

NOTE: PCIe end point devices that message LTR latency greater than or equal to 1 µs are not affected by this.

Workaround: None.

- Platforms not supporting S0ix with PCIe end point devices that do not support LTR may disable the associated PCH SRCCLKREQ# signal to keep the PCIe clock active during L1.
- Platforms supporting S0ix with PCIe end point devices that have LTR latencies less than 1 µs may disable the associated PCH SRCCLKREQ# signal to keep the PCIe clock active during L1.

Status: For the steppings affected, refer to the Summary Tables of Changes.

8. xHCI CV TD 2.2 Interrupter Handling

Problem: The xHCI Host Controller will clear the Interrupt Pending (IP) bit when the Interrupt Enable (IE) bit is set, contrary to the expectation of the xHCI CV TD 2.2 Interrupt Handling test.

Implication: USB-IF xHCI CV TD 2.2 may report a failure. Intel has obtained a waiver for TD 2.2.

NOTE: No functional impact is expected.

Workaround: None.

Status: For the steppings affected, refer to the Summary Tables of Changes.

9. xHCI Link Protocol Field Value

Problem: The xHCI Host Controller reports the Link Protocol (LP) bits [15:14] as 0h in the XECP_SUPP_USB3_5 Super Speed Plus register (xHCI MMIO offset 8034h). The xHCI spec rev 1.1 (published in Nov. 2017) defines this bit should be set to 1h for SuperSpeed USB 10 Gbps port.

Implication: USB-IF xHCI CV TD 1.9 may report a failure. Intel has obtained a waiver for TD 1.9.

NOTE: No functional impact is expected.

Workaround: None.

Status: For the steppings affected, refer to the Summary Tables of Changes.

10. xHCI Short Packet Event Using Non-Event Data TRB

Problem: The xHCI may generate an unexpected short packet event for the last transfer's Transfer Request Block (TRB) when using Non-Event Data TRB with multiples TRBs.

Implication: Transfer may fail due to the packet size error.

NOTE: This issue has only been observed in a synthetic environment. No known implication has been identified with commercial software.

Workaround: None identified.

Intel recommends software to use Data Event TRBs for short packet completion.

Status: For the steppings affected, refer to the Summary Tables of Changes.

11. eSPI SBLCL Register Bit Not Cleared By PLTRST#

Problem: The IOSF-SB eSPI Link Configuration Lock (SBLCL) bit (offset 4000h, bit 27 in eSPI PCR space) is reset by RSMRST# assertion instead of PLTRST# assertion.

Implication: If the SBLCL bit is set to 1, software will not be able to access the eSPI device Capabilities and Configuration register in the reserved address range (0h - 7FFh) until RSMRST# asserts.

Workaround: None identified.

If software needs to access the eSPI device reserved range 0h - 7FFh while SBLCL bit is set to 1, a RSMRST# assertion should be performed.

Status: For the steppings affected, refer to the Summary Tables of Changes.

12. Leakage On VCC_VNNEXT_1P05 Power Rail With External Bypass VR

Problem: Leakage on VCC_VNNEXT_1P05 power rail may be observed when external bypass VR is operating with VID value of 0.76 V.

Implication: System may shut down due to the external VR over voltage protection (OVP) limits.

Workaround: Platform designs with an external VR must be designed to operate with Over Voltage Protection (OVP) range of: 1.155 V ≤ OVP ≤ 1.365 V for all VID settings (1.05 V and 0.76 V).

Status: For the steppings affected, refer to the Summary Tables of Changes.

13. xHCI Protocol Speed ID Count Field

Problem: The xHCI Host Controller reports an incorrect Protocol Speed ID Count value for the USB 3.2 Supported Protocol Capability register - xHCI MMIO offset 8028 bits [31:28].

Implication: USB-IF xHCI CV TD 1.9 may report a failure.

NOTE: No functional impact is expected.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

14. System May Hang with USB-C* Power Adapter

Problem: Connecting a USB-C* power adapter to a PCH USB port may cause a race condition that can result in a xHCI controller hang. This issue only occurs on designs where the USB-C Power Delivery (PD) implements OOB messaging to communicate with the PCH for port mapping.

Implication: The system may hang.

NOTE: This issue does not occur when the system is in Sx state and has only been observed when repeatedly connecting a USB-C power adapter.

Workaround: None identified for when xHCI DBC is enabled. A fix has been identified for this erratum and may be available in a software update when xHCI DBC is disabled.

Status: For the steppings affected, refer to the Summary Tables of Changes.

15. Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment

Problem: If software assigns a 4 GB-aligned address to the Linked List Pointer (LLP_LOn = 0h) for Intel® Serial I/O Controller DMA engine, then the DMA engine interprets this as an empty link list and will not perform DMA transfers.

Implication: An Intel® Serial IO controller (i.e., I^2C, GSPI, or UART) may stop operating which may cause the system to hang.

Workaround: Driver software should not assign LLP to a 4 GB aligned address.

NOTE: This issue has been addressed in the Intel Serial IO drivers in the following versions or later: For Microsoft* Windows* 10, I2C device driver rev 30.100.1724.2, SPI device driver rev 30.100.1725.1, and UART device driver rev 30.100.1725.1.

Status: For the steppings affected, refer to the Summary Tables of Changes.

16. Audio Global Time Synchronization Register Access

Problem: Disabling the audio DSP through the Intel® High Definition Audio Function Configuration Register Offset 530h in the PCH Private Configuration Space by setting bit 2 to '1' will block accesses to Audio Global Time Synchronization registers in MMIO space (Offset 500h - 55Fh).

Implication: Audio Global Time Synchronization registers may not be accessible and any attempted accesses may result in a system hang.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

17. S0ix Entry When Connecting an USB-C* Power Adapter

Problem: Connecting a USB-C* power adapter to a PCH USB port may cause a race condition that can prevent the system from entering S0ix. This issue only occurs on designs where the USB-C Power Delivery (PD) implements Out Of Band (OOB) messaging to communicate with the PCH for port mapping.

Implication: The system may fail to enter S0ix.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

18. FIVR Clock Frequency Variation

Problem: The PCH Fully Integrated Voltage Regulator (FIVR) subsystem clock may have frequency variation when resuming from S0ix or C10.

Implication: The clock frequency variation may result in unexpected functional issues including increased RFI with the Wi-Fi* radio and/or system shutdown due to increased current consumption.

Workaround: None identified. A mitigation has been identified for this erratum and may be available in a software update.

Status: For the steppings affected, refer to the Summary Tables of Changes.

19. Phase Lock Loop (PLL) Feedback Circuit

Problem: The Main PLL and USBPCIe PLL have independent feedback circuits. A feedback circuit timing marginality may result in a momentary jitter excursion in the corresponding PLL and downstream circuitry.

Implication: If the Main PLL loses lock, then the system may hang. If the USBPCIe PLL loses lock, USB 3.1 / SATA / PCIe / integrated GbE / DMI / CLKOUT_PCIE interfaces may experience errors, including correctable errors, interface downtrains, or hangs.

Workaround: A fix has been identified for this erratum and may be available in a software update.

Status: For the steppings affected, refer to the Summary Tables of Changes.

20. Time Synchronization with xHCI and GbE

Problem: The xHCI and GbE do not use the correct time base for time synchronization.

Implication: xHCI Precision Time Measurement and GbE IEEE 802.1AS are not supported.

NOTE: This issue has only been observed in a synthetic environment. No known implication has been identified with commercial software.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

21. SATA Controller Support for Automatic Partial to Slumber Transition (APST) Feature

Problem: When the Automatic Partial to Slumber Transition (APST) feature is enabled an internal logic issue may occur during the transition from Partial to Slumber causing the SATA controller not to respond properly to additional commands.

Implication: The system may hang.

Workaround: A BIOS code change has been identified and may be implemented as a mitigation for this erratum. Alternatively, a mitigation has been identified for this erratum and may be available in a software update.

Status: For the steppings affected, refer to the Summary Tables of Changes.

22. Internal Clocking Phase Lock Loop (PLL) Locking

Problem: The internal PCH PLL that generates CLKOUT_CPUBCLK_P/N and the On Package DMI (OPDMI) clocks implements incorrect configuration settings which may cause the PLL to unlock.

Implication: Increased clock jitter may occur and could result in system instabilities.

Workaround: A fix has been identified for this erratum and may be available in a software update.

Status: For the steppings affected, refer to the Summary Tables of Changes.

23. Increased PCIe* Gen1 RX L0s Exit Latencies

Problem: When PCIe Link is operating at Gen1 and L0s is enabled with end point devices that have minimum electrical idle timings < 200 ns, the Root Port receiver may fail to train on Fast Training Sequence (FTS) patterns.

Implication: The link may train back to L0 through Recovery instead of directly back to L0 resulting in increased L0s exit latencies.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: For the steppings affected, refer to the Summary Tables of Changes.

24. Leakage Current from VCCPRIM_1P8 Power Rail

Problem: When the VCCPRIM_1P8 is off and the VCCPRIM_3P3 is powered on during G3 to S5, there may be a leakage current from the VCCPRIM_3P3 power rail to VCCPRIM_1P8 power rail.

Implication: The leakage voltage may be observed on VCCPRIM_1P8 power rail. There is no known functional or reliability impact.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

25. USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst

Problem: On USB 3.2 Gen 1x1 only capable ports, including ports configured as USB 3.2 Gen 1x1 by soft strap, the xHCI controller may send only 15 LFPS signals instead of a burst of 16 LFPS signals as specified by the USB 3.2 specification.

Implication: There are no known functional implications due to this erratum. LFPS handshake requires the receiver link partner to only detect 2 LFPS signals. This issue may impact the SuperSpeed compliance test case which checks for the 16 LFPS burst requirements: TD6.4, TD6.5, and TD7.31.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

26. Timed GPIO Event May Have a Mismatched Time Stamp

Problem: When a Timed GPIO event is counted in the Event Counter Capture (TGPIOECCV) register (offset 1238h, bits 31 to 0 in PWRMBASE space),

the Time Capture (TGPIOTCV) register (offset 1230h, bits 31 to 0 in PWRMBASE space) value is not immediately updated after that event is counted.

Implication: A Timed GPIO event may have a mismatched time stamp

Workaround: None identified. A Timed GPIO driver can partially mitigate for this erratum by detecting that a TGPIOECCV register change has occurred without a TGPIOTCV register change and then repeatedly re-read the TGPIOTCV register until a change does occur.

Status: For the steppings affected, refer to the Summary Tables of Changes.

27. G3 Current Specification on VCCRTC Rail

Problem: The PCH VCCRTC current draw during the G3 state may exceed the maximum current specification of 6 µA, as documented in the Intel® 495 Series Chipset Family On-Package Platform Controller Hub (PCH) Datasheet – Volume 1 of 2 (Doc ID #341080).

Implication: PCH units may experience VCCRTC rail current draw during the G3 state up to 8 uA. Platform implications are platform design specific.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

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Specification Changes

None.

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Specification Clarification

1. PCIe Precision Time Measurement (PTM) Byte Order

Added the following note to the Intel® 495 Series Chipset Family On-Package Platform Controller Hub (PCH) Datasheet Volume 1 of 2 (#341080) in the section Precision Time Measurement (PTM):

> PCIe Root Ports transmit the lower byte [7:0] of the Propagation Delay Field first instead of the upper byte [31:24] within their PTM DelayResponseD (Response with Data) messages.

2. SX_EXIT_HOLDOFF# Not Functional with eSPI Enabled

Added the following note to the Intel® 495 Series Chipset Family On-Package Platform Controller Hub (PCH) Datasheet Volume 1 of 2 (#341080) in the Power Management chapter Signal Description section:

> When eSPI is enabled, SX_EXIT_HOLDOFF# functionality is not available, and assertion of the signal will not impact Sx exit flows.

3. xHCI D3 Exit Timing

Added the following text to the Intel® 495 Series Chipset On-Package Platform Controller Hub (PCH) Datasheet Volume 2 of 2 (#341081) in the Power Management Control/Status (PM_CS) register summary, bits 1:0, 'PowerState (POWERSTATE)' field description section:

> Software should wait for 100 ms before requesting the xHCI controller to re-enter D3 after a D3 exit.

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Documentation Changes

None.

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