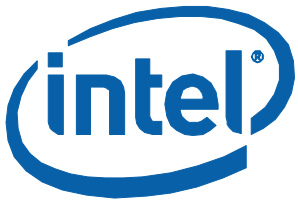

Intel® Ethernet Controller I350 Frequently Asked Questions (FAQs)

Networking Division (ND)

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Revision 2.2

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Revisions

Date	Revision	Notes
6/1/2011	2.0	First public release.
8/30/2011	2.1	Added entry #35
6/20/2014	2.2	Added entry #36

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Frequently Asked Questions

This document contains a list of Frequently Asked Questions (FAQ) for the I350. Entries are not listed in any particular order.

1. Does the I350 support EEPROMless designs?

Yes. This requires custom drivers for proper operation.

2. What power supplies does the I350 require?

3.3V, 1.8V and 1.0V.

3. Which power rails are sourced from main power?

I350 power should be derived from AUX power. Designers have the option of using on-die Voltage Regulation control to derive 1.8V and 1.0V power from a 3.3V aux power source.

4. Which ports are available on the dual port SKU?

Ports 0 and 1 are available on the dual port SKU.

5. Are the MAC addresses still automatically calculated like on the 82576?

No. Each MAC address must be programmed individually.

6. What Ethernet interfaces does the Intel device driver support for the I350?

As of this release, the following Ethernet interfaces are supported:
- Windows* NDIS - SerDes, Fiber, Copper and SGMII are supported.
- Linux* - SerDes, Fiber, Copper and SGMII are supported.

7. Does the I350 support Pre-boot?

Yes. It supports iSCSI*, PXE* and UEFI*.

8. Which Ethernet interfaces does the Pre-boot environment support?

As of this release, the following Ethernet interfaces are supported:
- iSCSI - SerDes, Fiber, Copper and SGMII are supported in Windows and Linux.
- PXE - SerDes, Fiber, Copper and SGMII are supported in Windows and Linux.
- UEFI - SerDes, Fiber, Copper and SGMII are supported in Windows and Linux.

9. What Device ID's are supported by the I350?

The following device ID's are supported:

LOMs	
151F	EEPROM-Less* (device default)
1523	SerDes (KX / BX)
1524	SGMII
1521	Copper
1522	Fiber
NICs	
1521	Quad-Port CU NIC (Retail and OEM)
1521	Dual-Port CU NIC (Retail and OEM)

* This ID is supported by the tools, but not by the driver.

10. Why do I see (4) devices, all with the same device ID?

Each port of the I350 is considered a unique device and has its own Device ID. A device with all 4 ports configured to the same interface type shows 4 Device IDs - all with the same value.

11. What's the Device ID of the I350 if each port is a different Ethernet type?

Device ID's are defined 'per port', not per silicon chip. This means there is no mixed-port type device ID, just one device ID per port.

Each port can be configured for one the 5 Ethernet interface types (Copper, Fiber, Kx, Bx or SGMII).

12. Are different device drivers needed for each Ethernet Interface type?

No. The I350 device driver supports each of the Ethernet Interface types.

13. Does the Intel device driver support the 1588 protocol standard?

Though the I350 supports the 1588 protocol standard, the device driver does not. Each application is unique and requires customers to develop their own custom driver to support this feature.

14. Can I/O addressing be disabled in the I350?

Yes. The I350 has a 'disable I/O mode' feature for disabling allocation of I/O port resources in systems and environments (such as Windows and UEFI) where the feature is either not desirable or not supported.

Legacy environment components (such as DOS, PXE and iSCSI Boot, which previously required I/O port access) can now either use I/O mode if available or an alternate mechanism if I/O mode is disabled.

15. Can I monitor the I350 temperature through the TSENSP/Z pins?

Yes and No. The TSENSP/Z pins can be used to measure temperature, but should only be used in the lab for characterization purposes. These pins should not be used in product systems to monitor and react to temperature changes. Refer to "Thermal Diode" section of the "Thermal Management" chapter of the Datasheet for details.

A thermal sensor is provided on-die and is available to software through Thermal Sensor registers as noted in various sections of the datasheet. This is the mechanism by which the device temperature can be monitored.

16. What are the I350 SMbus Slave addresses?

For the dev_starter EEPROM images that support SMBus manageability, SMbus addresses are defined as:

```
SMBus 0 Slave Address 0x92
SMBus 1 Slave Address 0x94
SMBus 2 Slave Address 0x96
SMBus 3 Slave Address 0x98
```

17. How long can Ethernet MDI trace lengths be?

In general, I350 Ethernet trace lengths can be up to 8 inches. This is be dependent upon the actual design and layout. Refer to the "Intel Long MDI Traces Design and Layout Guide" for details. An NDA agreement is required to access this document (Doc ID #435031).

18. Why do I see valid MAC addresses in the dev_starter EEPROM images?

Default MAC addresses do exist in the I350 dev_starter images so that users have working MAC addresses for design testing and validation. These MAC addresses should be overwritten with real MAC address values for production units.

The addresses are:

Location	EEPROM Value	MAC Address
0x00 -> 0x02	A000 00C9 0000	00A0C9000000
0x80 -> 0x82	A000 00C9 0100	00A0C9000001
0xC0 -> 0xC2	A000 00C9 0200	00A0C9000002
0x100 -> 0x102	A000 00C9 0300	00A0C9000003

19. How do I interpret the chip markings on my I350?

See "Marking Diagram" in the Specification Update.

20. Does the I350 have any ESD suppression on the MDI lines?

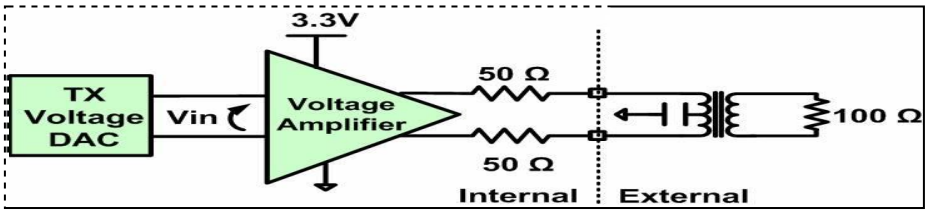
Yes, ESD suppression is built-in.

21. Is the 'MDI flip chip' option available on the I350?

Yes the I350 does support the MDI flip chip feature similar to the 82576 device. Meaning, port 0 can be swapped with port 3, and port 1 can be swapped with port 2.

22. The I350 Reference Schematic does not show a 1.8V on the system side magnetic center tap? Is this still required?

No. The 1.8V bias is not required for the I350. The I350's output buffers are internally biased with a voltage mode driver.



23. How do I get the latest drivers for the I350?

Windows* and Linux* drivers can be found at:
http://www.intel.com/cd/edesign/library/asmo-na/eng/475644.htm

Linux drivers can also be downloaded from Sourceforge at:
http://sourceforge.net/projects/e1000/files/

24. What do I do with unused pins?

Leave unused pins unconnected, except for manageability pins (SMBus and NC-SI Bus). These pins must be pulled-up. Reference the I350 Design Checklist for details.

25. Can other devices be connected to the I350 SMBus?

For best performance, each I350 should have its own dedicated SMBus link to the SMBus master device.

26. Can the quad port dev_starter EEPROM images be used on a dual port device or dual port configured quad port device?

Yes. Quad port images work with dual port devices as long as the configuration of ports 0 and 1 on the dual port device match ports 0 and 1 on the quad port image. See below:

Quad image	Port #	Dual port device
Copper	0	Copper
Copper	1	Copper
Copper	2	n/a
Copper	3	n/a
	OR	
SerDesBX	0	SerDesBX
SerDesBX	1	SerDesBX
SGMII	2	n/a
SGMII	3	n/a

27. Can the latest EEPROM images be used on A0 silicon?

No. A0 and A1 EEPROM images are **not** interchangeable on A0 and A1 Silicon. A0 silicon requires A0 images; A1 silicon requires A1 images.

A0 images are no longer available. A1 images can be found in CDI/IDL at:
http://www.intel.com/cd/edesign/library/asmo-na/eng/474233.htm

An NDA is required to access this information.

28. Does the I350 support MAC to MAC Communication?

No. Each MAC on the I350 is independent of the other MACs. There is no MAC to MAC communication path.

29. Is there an [Ethernet] line-side loopback option?

No. Loopback options are only available from the host side. Refer to "Loopback Support" in the Datasheet.

30. Does the Ethernet interface dynamically switch between media?

No. 0nce a port is configured for a specific media interface type, the configuration remains in place until it is reconfigured for another interface type (by software). The configuration is static.

Refer to "Switching between Medias" in the Datasheet.

31. The 82580 reference documents show a Ferrite Bead and Resistor Filter on the 1.0v, 1.8v and 3.3v power supplies. I350 documents do not show this. Are these required for the I350?

No, this is not required in a I350 design.

32. What EEPROM bit settings are required for Wake on LAN?

For wake in D3cold, these EEPROM settings are required: 0x0F:15 = 1, 0x20:2 = 1 and 0x24:10 = 1. Set the bits for each port that you enable for Wake on LAN. If Wake in D3hot is also desired, set 0x29:5 = 1 in addition.

See the "Non-Volatile Memory Map – EEPROM" chapter in the datasheet for details.

33. The peak differential output voltage is low when I test 10MB. What is the problem?

EEPROM images enable 10base-TE as a default. When you clear this bit and reset the system, the device should meet the standard test specification. 10base-TE is an energy saving, low power use feature and is part of the Energy Efficient Ethernet (802.3az) specification.

34. The I350 is design compatible with the Intel 82580 and X540 devices, where can I get information on this?

This information is available in the I350 datasheet and in the following documents; I350_AMx_GbE_LAN_Controller___82580_Pin_Compatibility_v1.0C.pdf and the X540_i350_Pin_Compatibility_book_rev_1_0.pdf.

35. Some of the EEPROM images can be applied to 2 or 4 port devices. Are there any settings that need to be made for the 2 port devices?

There are no changes that need to be made for the 2 port devices. However, you may optionally disable the last 2 ports in the eeprom image and then resize the Transmit and Receive buffers resulting in a larger packet buffer for the remaining 2 ports. This can result in slightly better performance for a 2 port device. Please consult section 6 in the datasheet for disabling the ports using the SDP register LAN_DIS (LAN Base + 0x20:11 = 1) bit and resizing the buffers to Tx = 40KB and Rx = 72KB using Initialization Control Word 4 (LAN Base + 0x13).

36. I want to retain the Ethernet Frame Check Sequence (FCS) field (containing the Ethernet CRC) in the received packets that are copied into system memory. How can I do this?

Under normal operating conditions the FCS is added to an Ethernet packet to support data integrity of the packet as it is transferred across the network connection. Once the target device receives the packet and verifies the validity of the packet data, the FCS is stripped from the packet before it is moved into memory. In some rare cases an application or test process may want to retain the FCS for additional verification or inspection. To disable stripping of the CRCs on all packets; the RCTL.SECRC bit and the per-VM, DVMOLR[n].Strip_CRC bits for the queues that are in use must all be cleared.

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