Intel® 400 Series Chipset On-Package Platform Controller Hub Register Database

Online Register Database

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Contents

Introduction

Use the sidebar to browse through the register files or search for something in particular. Contact PCDC.ADMIN@INTEL.COM for assistance.

Note: The registers posted on this web page are also published in the PCH EDS Vol 2 (in PDF format). However, the registers posted here may contain updated register info compared to the PDF version as the posted registers are being updated when needed until the next PDF version is released.

The version used in this web page indicates the EDS version the registers are based off of, together with the web posting update release info.For example, Version 0.71 indicates the registers are based on the EDS Version 0.7 but have first update after the PDF EDS release.Similarly, 0.72, 0.73, etc.indicate second, third, etc update after rev 0.7 release.

The following notations and definitions are used in the register description:

RO	Read Only. Writes to this register bit have no effect. When writing to RO bits, software must preserve the value. When software updates a register that has RO fields, it must read the register value first so that the appropriate merge between the reserved and updated fields will occur.
WO	Write Only. Reads to this register bit have no effect.
RW	Read/Write. A register bit with this attribute can be read and written.
RW / O	Read / Write Once. A register bit with this attribute can be written only once after power up.After the first write, the bit becomes read only.
RW / 1C	Read / Write Clear. The register bit is set to 1 by hardware and cleared by software writing a 1 to it.
RW / 1S	Read / Write Set. The register bit is set to 1 by software and cleared by hardware.
RW / L	Read / Write Locked. A register bit with this attribute can be read and write, but cannot be written after the lock bit is set.
/ V	Volatile or variable. This attribute indicates that the register bit can be updated by hardware(aside from resetting it). For example, RO/ V means hardware controls the value; RW / V means that generally the bit is written by SW / FW but can be also updated by hardware.
/ P	This attribute indicates that the register is reset only on loss of power.
/ S	This attribute indicates that the initial value of the register bit is taken from software.

Danger:
The PCH contains registers and bits that are reserved. These are designated by being defined as Reserved or RSVD. In addition, registers or register bits not defined in this document are also reserved. Software must not attempt to access a reserved register, use the value read from a reserved register or bit, or modify the value in a reserved register or bit. Doing so is unsupported and may cause unexpected behavior on the platform. When writing to reserved bits, software must preserve the value. When software updates a register that has reserved fields, it must read the register value first so that the appropriate merge between the reserved and updated fields will occur.

8254 Timer Registers

Summary of Bus:, Device:, Function: (IO)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40h	1	Counter 0 - Interval Timer Status Byte Format Register (C0_ITSBFR)	C4h
42h	1	Counter 2 - Interval Timer Status Byte Format Register (C2_ITSBFR)	0h
43h	1	Timer Control Word Register (TCW)	0h
40h	1	Counter 0 - Counter Access Ports Register (C0_CAPR)	0h
42h	1	Counter 2 - Counter Access Ports Register (C2_CAPR)	0h
43h	1	Read Back Command (RBC)	C0h
43h	1	Counter Latch Command (CLC)	0h

Counter 0 - Interval Timer Status Byte Format Register (C0_ITSBFR) – Offset 40

Each counter's status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for a given counter, the next read from the counter's Counter Access Ports Register (40h for counter 0 and 42h for counter 2) returns the status byte. The status byte returns the following:

Bit Range	Default	Access	Field Name and Description
7	1b	RO	**Counter OUT Pin State (COPS)** When this bit is a 1, the OUT pin of the counter is also a 1. When this bit is a 0, the OUT pin of the counter is also a 0.

Bit Range	Default	Access	Field Name and Description
6	1b	RO	**Count Register Status (CRSTS)** This bit indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the counter mode, but until the count is loaded into the counting element (CE), the count value will be incorrect. 0 Count has been transferred from CR to CE and is available for reading. 1 Null Count. Count has not been transferred from CR to CE and is not yet available for reading.
5:4	00b	RO	**Read/Write Selection Status (RW_SLT_STS)** These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	010b	RO	

Bit Range	Default	Access	Mode Selection Status (MD_SLT_STS) Field Name and Description
			These bits return the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe

Bit Range	Default	Access	Field Name and Description
0	0b	RO	**Countdown Type Status (CDT_STS)** This bit reflects the current countdown type, ether 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

Counter 2 - Interval Timer Status Byte Format Register (C2_ITSBFR) – Offset 42

Same definition as counter 0

Timer Control Word Register (TCW) – Offset 43

This register is programmed prior to any counter being accessed to specify counter modes. Following reset, the control words for each register are undefined and each counter output is 0. Each timer must be programmed to bring it into a known state.

There are two special commands that can be issued to the counters through this register, the Read Back Command and the Counter Latch Command. When these commands are chosen, several bits within this register are redefined.

Bit Range	Default	Access	Field Name and Description
7:6	00b	WO	**Counter Select (CNT_SLT)** The Counter Selection bits select the counter the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1 00 Counter 0 select 01 Reserved 10 Counter 2 select 11 Read Back Command

Bit Range	Default	Access	Field Name and Description
5:4	00b	WO	**Read/Write Select: (RW_SLT)** These bits are the read/write control bits. The actual counter programming is done through the counter port (40h for counter 0 and 42h for counter 2) 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	000b	WO	**Counter Mode Selection (CNT_MD_SLTN)** These bits select one of six possible modes of operation for the selected counter. 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe

Bit Range	Default	Access	Field Name and Description
0	0b	WO	**Binary/BCD Countdown Select (B_BCD_CNTDWN_SLT)** 0 Binary countdown is used. The largest possible binary count is 2^16 1 Binary coded decimal (BCD) count is used.The largest possible BCD count is 10^4

Counter 0 - Counter Access Ports Register (C0_CAPR) – Offset 40

*Address should be 40h

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW/V	**Counter Port (CP)** Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

Counter 2 - Counter Access Ports Register (C2_CAPR) – Offset 42

Same definition as Counter 0 - Counter Access Ports Register

Read Back Command (RBC) – Offset 43

The Read Back Command is used to determine the count value, programmed mode, and current states of the OUT pin and Null count flag of the selected counter or counters. Status and/or count may be latched in any or all of the counters by selecting the counter during the register write. The count and status remain latched until read, and further latch commands are ignored until the count is read.

Both count and status of the selected counters may be latched simultaneously by setting both bit 5 and bit 4 to 0. If both are latched, the first read operation from that counter returns the latched status. The next one or two reads, depending on whether the counter is programmed for one or two byte counts, returns the latched count. Subsequent reads return an unlatched count.

Bit Range	Default	Access	Field Name and Description
7:6	11b	WO	**Read Back Command (RBC)** Must be 11 to select the Read Back Command

Bit Range	Default	Access	Field Name and Description
5	0b	WO	**Latch Count of Selected Counters (LCSC)** 0 Current count value of the selected counters will be latched 1 Current count will not be latched
4	0b	WO	**Latch Status of Selected Counters (LSSC)** 0 Status of the selected counters will be latched 1 Status will not be latched
3	0b	WO	**Counter 2 Select (CNT_2_SLT)** When set to 1, Counter 2 count and/or status will be latched
2	-	-	**Reserved**
1	0b	WO	**Counter 0 Select (CNT_0_SLT)** When set to 1, Counter 0 count and/or status will be latched.
0	-	-	**Reserved**

Counter Latch Command (CLC) – Offset 43

The Counter Latch Command latches the current count value. This command is used to insure that the count read from the counter is accurate. The count value is then read from each counter's count register through the Counter Ports Access Ports Register (40h for counter 0 and 42h for counter 2). The count must be read according to the programmed format, i.e. if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other (read, write, or programming operations for other counters may be inserted between the reads). If a counter is latched once and then latched again before the count is read, the second Counter Latch Command is ignored.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
7:6	00b	WO	**Counter Selection (CNT_SLT)** These bits select the counter for latching. If 11 is written, then the write is interpreted as a read back command. 00 = Counter 0 01 = Reserved 10 = Counter 2
5:4	00b	WO	**Counter Latch Command (CLC)** Write 00 to select the Counter Latch Command.
3:0	-	-	**Reserved**

Advanced Programmable Interrupt Controller (APIC) Registers

The APIC is accessed using an indirect addressing scheme. Two registers are visible by software for manipulation of most of the APIC registers. These registers are mapped into memory space. The address bits 19:12 of the address range are programmable through bits 7:0 of OIC register (Chipset Configuration Register: Offset 31FEh). The registers are shown below.

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
fec00000h	4	Index Register (IDX)	0h
fec00010h	4	Data Register (DAT)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
fec00040h	4	EOI Register (EOIR)	0h

Index Register (IDX) – Offset fec00000

The Index Register will select which APIC indirect register to be manipulated by software. Software will program this register to select the desired APIC internal register.

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	00h	RW	**APIC Index ()** This is an 8 bit pointer into the I/O APIC register table.

Data Register (DAT) – Offset fec00010

This 32-bit register specifies the data to be read or written to the register pointed to by the Index register. This register can be accessed only in DW quantities.

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW/V	**APIC Data ()** This is a 32-bit register for the data to be read or written to the APIC indirect register pointed to by the Index register (Memory Address FEC0_0000h).

EOI Register (EOIR) – Offset fec00040

When a write is issued to this register, the IOxAPIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, RTE.RIRR for that entry will be cleared. If multiple entries have the same vector, each of those entries will have RTE.RIRR cleared. Only bits 7:0 are used. Bits 31:8 are ignored.

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	00h	WO	**Redirection Entry Clear ()** When a write is issued to this register, the I/O APIC will check this field and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit for that I/O Redirection Entry will be cleared.

APIC Indirect Registers

APIC Indirect Registers lists the registers that can be accessed within the APIC using the Index Register. When accessing these registers, accesses must be done one DWord at a time. For example, software should never access byte 2 from the Data register before accessing bytes 0 and 1. The hardware will not attempt to recover from a bad programming model in this case.

Index Mnemonic Register Name

10-11h RTE0 Redirection Table Entry 0

12-13h RTE1 Redirection Table Entry 1

14-15h RTE2 Redirection Table Entry 2

... ...

3E-3Fh RTE23 Redirection Table Entry 23

40-41h RTE24 Redirection Table Entry 24

... ...

FE-FFh RTE119 Redirection Table Entry 119

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Identification Register (ID)	0h
1h	4	Version Register (VER)	770020h
10h	8	Redirection Table Entry 0 (RTE0)	10000h
12h	8	Redirection Table Entry 1 (RTE1)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
14h	8	Redirection Table Entry 2 (RTE2)	0h
16h	8	Redirection Table Entry 3 (RTE3)	0h
18h	8	Redirection Table Entry 4 (RTE4)	0h
1ah	8	Redirection Table Entry 5 (RTE5)	0h
1ch	8	Redirection Table Entry 6 (RTE6)	0h
1eh	8	Redirection Table Entry 7 (RTE7)	0h
20h	8	Redirection Table Entry 8 (RTE8)	0h
22h	8	Redirection Table Entry 9 (RTE9)	0h
24h	8	Redirection Table Entry 10 (RTE10)	0h
26h	8	Redirection Table Entry 11 (RTE11)	0h
28h	8	Redirection Table Entry 12 (RTE12)	0h
2ah	8	Redirection Table Entry 13 (RTE13)	0h
2ch	8	Redirection Table Entry 14 (RTE14)	0h
2eh	8	Redirection Table Entry 15 (RTE15)	0h
30h	8	Redirection Table Entry 16 (RTE16)	0h
32h	8	Redirection Table Entry 17 (RTE17)	0h
34h	8	Redirection Table Entry 18 (RTE18)	0h
36h	8	Redirection Table Entry 19 (RTE19)	0h
38h	8	Redirection Table Entry 20 (RTE20)	0h
3ah	8	Redirection Table Entry 21 (RTE21)	0h
3ch	8	Redirection Table Entry 22 (RTE22)	0h
3eh	8	Redirection Table Entry 23 (RTE23)	0h
40h	8	Redirection Table Entry 24 (RTE24)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
42h	8	Redirection Table Entry 25 (RTE25)	0h
44h	8	Redirection Table Entry 26 (RTE26)	0h
46h	8	Redirection Table Entry 27 (RTE27)	0h
48h	8	Redirection Table Entry 28 (RTE28)	0h
4ah	8	Redirection Table Entry 29 (RTE29)	0h
4ch	8	Redirection Table Entry 30 (RTE30)	0h
4eh	8	Redirection Table Entry 31 (RTE31)	0h
50h	8	Redirection Table Entry 32 (RTE32)	0h
52h	8	Redirection Table Entry 33 (RTE33)	0h
54h	8	Redirection Table Entry 34 (RTE34)	0h
56h	8	Redirection Table Entry 35 (RTE35)	0h
58h	8	Redirection Table Entry 36 (RTE36)	0h
5ah	8	Redirection Table Entry 37 (RTE37)	0h
5ch	8	Redirection Table Entry 38 (RTE38)	0h
5eh	8	Redirection Table Entry 39 (RTE39)	0h
60h	8	Redirection Table Entry 40 (RTE40)	0h
62h	8	Redirection Table Entry 41 (RTE41)	0h
64h	8	Redirection Table Entry 42 (RTE42)	0h
66h	8	Redirection Table Entry 43 (RTE43)	0h
68h	8	Redirection Table Entry 44 (RTE44)	0h
6ah	8	Redirection Table Entry 45 (RTE45)	0h
6ch	8	Redirection Table Entry 46 (RTE46)	0h
6eh	8	Redirection Table Entry 47 (RTE47)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
70h	8	Redirection Table Entry 48 (RTE48)	0h
72h	8	Redirection Table Entry 49 (RTE49)	0h
74h	8	Redirection Table Entry 50 (RTE50)	0h
76h	8	Redirection Table Entry 51 (RTE51)	0h
78h	8	Redirection Table Entry 52 (RTE52)	0h
7ah	8	Redirection Table Entry 53 (RTE53)	0h
7ch	8	Redirection Table Entry 54 (RTE54)	0h
7eh	8	Redirection Table Entry 55 (RTE55)	0h
80h	8	Redirection Table Entry 56 (RTE56)	0h
82h	8	Redirection Table Entry 57 (RTE57)	0h
84h	8	Redirection Table Entry 58 (RTE58)	0h
86h	8	Redirection Table Entry 59 (RTE59)	0h
88h	8	Redirection Table Entry 60 (RTE60)	0h
8ah	8	Redirection Table Entry 61 (RTE61)	0h
8ch	8	Redirection Table Entry 62 (RTE62)	0h
8eh	8	Redirection Table Entry 63 (RTE63)	0h
90h	8	Redirection Table Entry 64 (RTE64)	0h
92h	8	Redirection Table Entry 65 (RTE65)	0h
94h	8	Redirection Table Entry 66 (RTE66)	0h
96h	8	Redirection Table Entry 67 (RTE67)	0h
98h	8	Redirection Table Entry 68 (RTE68)	0h
9ah	8	Redirection Table Entry 69 (RTE69)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
9ch	8	Redirection Table Entry 70 (RTE70)	0h
9eh	8	Redirection Table Entry 71 (RTE71)	0h
a0h	8	Redirection Table Entry 72 (RTE72)	0h
a2h	8	Redirection Table Entry 73 (RTE73)	0h
a4h	8	Redirection Table Entry 74 (RTE74)	0h
a6h	8	Redirection Table Entry 75 (RTE75)	0h
a8h	8	Redirection Table Entry 76 (RTE76)	0h
aah	8	Redirection Table Entry 77 (RTE77)	0h
ach	8	Redirection Table Entry 78 (RTE78)	0h
aeh	8	Redirection Table Entry 79 (RTE79)	0h
b0h	8	Redirection Table Entry 80 (RTE80)	0h
b2h	8	Redirection Table Entry 81 (RTE81)	0h
b4h	8	Redirection Table Entry 82 (RTE82)	0h
b6h	8	Redirection Table Entry 83 (RTE83)	0h
b8h	8	Redirection Table Entry 84 (RTE84)	0h
bah	8	Redirection Table Entry 85 (RTE85)	0h
bch	8	Redirection Table Entry 86 (RTE86)	0h
beh	8	Redirection Table Entry 87 (RTE87)	0h
c0h	8	Redirection Table Entry 88 (RTE88)	0h
c2h	8	Redirection Table Entry 89 (RTE89)	0h
c4h	8	Redirection Table Entry 90 (RTE90)	0h
c6h	8	Redirection Table Entry 91 (RTE91)	0h
c8h	8	Redirection Table Entry 92 (RTE92)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
cah	8	Redirection Table Entry 93 (RTE93)	0h
cch	8	Redirection Table Entry 94 (RTE94)	0h
ceh	8	Redirection Table Entry 95 (RTE95)	0h
d0h	8	Redirection Table Entry 96 (RTE96)	0h
d2h	8	Redirection Table Entry 97 (RTE97)	0h
d4h	8	Redirection Table Entry 98 (RTE98)	0h
d6h	8	Redirection Table Entry 99 (RTE99)	0h
d8h	8	Redirection Table Entry 100 (RTE100)	0h
dah	8	Redirection Table Entry 101 (RTE101)	0h
dch	8	Redirection Table Entry 102 (RTE102)	0h
deh	8	Redirection Table Entry 103 (RTE103)	0h
e0h	8	Redirection Table Entry 104 (RTE104)	0h
e2h	8	Redirection Table Entry 105 (RTE105)	0h
e4h	8	Redirection Table Entry 106 (RTE106)	0h
e6h	8	Redirection Table Entry 107 (RTE107)	0h
e8h	8	Redirection Table Entry 108 (RTE108)	0h
eah	8	Redirection Table Entry 109 (RTE109)	0h
ech	8	Redirection Table Entry 110 (RTE110)	0h
eeh	8	Redirection Table Entry 111 (RTE111)	0h
f0h	8	Redirection Table Entry 112 (RTE112)	0h
f2h	8	Redirection Table Entry 113 (RTE113)	0h
f4h	8	Redirection Table Entry 114 (RTE114)	0h
f6h	8	Redirection Table Entry 115 (RTE115)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
f8h	8	Redirection Table Entry 116 (RTE116)	0h
fah	8	Redirection Table Entry 117 (RTE117)	0h
fch	8	Redirection Table Entry 118 (RTE118)	0h
feh	8	Redirection Table Entry 119 (RTE119)	0h

Identification Register (ID) – Offset 0

This APIC ID serves as a physical name of the APIC. The APIC bus arbitration ID for the APIC is derived from its I/O APIC ID. This register is reset to 0 on power-up reset.

Bit Range	Default	Access	Field Name and Description
30:28	-	-	**Reserved**
27:24	0h	RW	**APIC Identification (AID)** Software must program this value before using the APIC.
23:16	-	-	**Reserved**
15	0b	RW	**Scratchpad (SPD)** Scratchpad Field
14:0	-	-	**Reserved**

Version Register (VER) – Offset 1

Each I/O APIC contains a hardwired Version Register that identifies different implementation of APIC and their versions. The maximum redirection entry information is also in this register to let software know how many interrupt are supported by this APIC.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:16	77h	RW/O	**Maximum Redirection Entries (MRE)** This is the entry number (0 being the lowest entry) of the highest entry in the redirection table. It is equal to the number of interrupt input pins minus one and is in the range of 0 through 239. In PCH this field is defaulted to 17h to indicate 24 interrupts. This field is Read-Write-Once. BIOS must write to this field after PLTRST# to lockdown the value. This allows BIOS to utilize some of the entries for its own purpose and thus advertising fewer IOxAPIC Redirection Entries to OS. BIOS may to program this field up to 78h (maximum 120 entries).
15	0b	RO	**Pin Assertion Register Supported (PRQ)** Indicate that the IOxAPIC does not implement the Pin Assertion Register.
14:8	-	-	**Reserved**
7:0	20h	RO	**Version (VS)** Identifies the implementation version as IOxAPIC.

Redirection Table Entry 0 (RTE0) – Offset 10

The Redirection Table has a dedicated entry for each interrupt input pin. The information in the Redirection Table is used to translate the interrupt manifestation on the corresponding interrupt pin into an APIC message.

The APIC will respond to an edge triggered interrupt as long as the interrupt is held until after the acknowledge cycle has begun. Once the interrupt is detected, a delivery status bit internally to the I/O APIC is set. The state machine will step ahead and wait for an ackledgement from the APIC unit that the interrupt message was sent. Only then will the I/O APIC be able to recognize a new edge on that interrupt pin. That new edge will only result in a new invocation of the handler if its acceptance by the destination APIC causes the Interrupt Request register bit to go from 0 to 1. (In other words, if the interrupt was not already pending a the destination.)

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
63:56	00h	RW	**Destination ID (DID)** If bit 11 of this entry is 0 (Physical), then bits 59:56 specifies an APIC ID. In this case, bits 63:59 should be programmed by software to 0. If bit 11 of this entry is 1 (Logical), then bits 63:56 specify the logical destination address of a set of processors.
55:48	00h	RW	**Extended Destination ID (EDID)** These bits are sent to a local APIC only when in Processor System Bus mode. They become bits 11:4 of the address.
47:17	-	-	**Reserved**
16	1b	RW	**Mask (MSK)** 0 = Not masked. An edge or level on this interrupt pin results in the delivery of the interrupt to the destination. 1 = Masked. Interrupts are not delivered nor held pending. Setting this bit after the interrupt is accepted by a local APIC has no effect on that interrupt. This behavior is identical to the device withdrawing the interrupt before it is posted to the processor. It is software's responsibility to deal with the case where the mask bit is set after the interrupt message has been accepted by a local APIC unit but before the interrupt is dispensed to the processor.
15	0b	RW	**Trigger Mode (TM)** This field indicates the type of signal on the interrupt pin that triggers an interrupt. 0 = The interrupt is edge sensitive. 1 = The interrupt is level sensitive.
14	0b	RO/V	**Remote IRR (RIRR)** This is used for level triggered interrupts; its meaning is undefined for edge triggered interrupts. 0 = Reset when an EOI message is received that matches the VCT field. 1 = Set when IOxAPIC sends the level interrupt message to the CPU. Note, this bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.

Bit Range	Default	Access	Field Name and Description
13	0b	RW	**Polarity (POL)** This bit specifies the polarity of each interrupt signal connected to the interrupt pins. 0 = Signal is active high. 1 = Signal is active low.
12	0b	RO/V	**Delivery Status (DS)** This field contains the current status of the delivery of this interrupt. 0 = Idle. There is no activity for this interrupt. 1 = Pending. An interrupt has been injected, but delivery is not complete. Note, writes to this bit have no effect.
11	0b	RW	**Destination Mode (DSM)** This field is used by the local Apic to determine whether it is the destination of the message. 0 = Physical. Destination APIC ID is identified by bits 59:56. 1 = Logical. Destinations are identified by matching bit 63:56 with Logical Destination in the Destination Format register and Logical Destination register in each Local APIC.

Bit Range	Default	Access	Field Name and Description
10:8	000b	RW	**Delivery Mode (DLM)** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported 011 Reserved 100 NMI Not supported 101 INIT Not supported 110 Reserved 111 ExtINT
7:0	00h	RW	**Vector (VCT)** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

Redirection Table Entry 1 (RTE1) – Offset 12

This register has the same bit definition as RTE0.

Redirection Table Entry 2 (RTE2) – Offset 14

This register has the same bit definition as RTE0.

Redirection Table Entry 3 (RTE3) – Offset 16

This register has the same bit definition as RTE0.

Redirection Table Entry 4 (RTE4) – Offset 18

This register has the same bit definition as RTE0.

Redirection Table Entry 5 (RTE5) – Offset 1a

This register has the same bit definition as RTE0.

Redirection Table Entry 6 (RTE6) – Offset 1c

This register has the same bit definition as RTE0.

Redirection Table Entry 7 (RTE7) – Offset 1e

This register has the same bit definition as RTE0.

Redirection Table Entry 8 (RTE8) – Offset 20

This register has the same bit definition as RTE0.

Redirection Table Entry 9 (RTE9) – Offset 22

This register has the same bit definition as RTE0.

Redirection Table Entry 10 (RTE10) – Offset 24

This register has the same bit definition as RTE0.

Redirection Table Entry 11 (RTE11) – Offset 26

This register has the same bit definition as RTE0.

Redirection Table Entry 12 (RTE12) – Offset 28

This register has the same bit definition as RTE0.

Redirection Table Entry 13 (RTE13) – Offset 2a

This register has the same bit definition as RTE0.

Redirection Table Entry 14 (RTE14) – Offset 2c

This register has the same bit definition as RTE0.

Redirection Table Entry 15 (RTE15) – Offset 2e

This register has the same bit definition as RTE0.

Redirection Table Entry 16 (RTE16) – Offset 30

This register has the same bit definition as RTE0.

Redirection Table Entry 17 (RTE17) – Offset 32

This register has the same bit definition as RTE0.

Redirection Table Entry 18 (RTE18) – Offset 34

This register has the same bit definition as RTE0.

Redirection Table Entry 19 (RTE19) – Offset 36

This register has the same bit definition as RTE0.

Redirection Table Entry 20 (RTE20) – Offset 38

This register has the same bit definition as RTE0.

Redirection Table Entry 21 (RTE21) – Offset 3a

This register has the same bit definition as RTE0.

Redirection Table Entry 22 (RTE22) – Offset 3c

This register has the same bit definition as RTE0.

Redirection Table Entry 23 (RTE23) – Offset 3e

This register has the same bit definition as RTE0.

Redirection Table Entry 24 (RTE24) – Offset 40

This register has the same bit definition as RTE0.

Redirection Table Entry 25 (RTE25) – Offset 42

This register has the same bit definition as RTE0.

Redirection Table Entry 26 (RTE26) – Offset 44

This register has the same bit definition as RTE0.

Redirection Table Entry 27 (RTE27) – Offset 46

This register has the same bit definition as RTE0.

Redirection Table Entry 28 (RTE28) – Offset 48

This register has the same bit definition as RTE0.

Redirection Table Entry 29 (RTE29) – Offset 4a

This register has the same bit definition as RTE0.

Redirection Table Entry 30 (RTE30) – Offset 4c

This register has the same bit definition as RTE0.

Redirection Table Entry 31 (RTE31) – Offset 4e

This register has the same bit definition as RTE0.

Redirection Table Entry 32 (RTE32) – Offset 50

This register has the same bit definition as RTE0.

Redirection Table Entry 33 (RTE33) – Offset 52

This register has the same bit definition as RTE0.

Redirection Table Entry 34 (RTE34) – Offset 54

This register has the same bit definition as RTE0.

Redirection Table Entry 35 (RTE35) – Offset 56

This register has the same bit definition as RTE0.

Redirection Table Entry 36 (RTE36) – Offset 58

This register has the same bit definition as RTE0.

Redirection Table Entry 37 (RTE37) – Offset 5a

This register has the same bit definition as RTE0.

Redirection Table Entry 38 (RTE38) – Offset 5c

This register has the same bit definition as RTE0.

Redirection Table Entry 39 (RTE39) – Offset 5e

This register has the same bit definition as RTE0.

Redirection Table Entry 40 (RTE40) – Offset 60

This register has the same bit definition as RTE0.

Redirection Table Entry 41 (RTE41) – Offset 62

This register has the same bit definition as RTE0.

Redirection Table Entry 42 (RTE42) – Offset 64

This register has the same bit definition as RTE0.

Redirection Table Entry 43 (RTE43) – Offset 66

This register has the same bit definition as RTE0.

Redirection Table Entry 44 (RTE44) – Offset 68

This register has the same bit definition as RTE0.

Redirection Table Entry 45 (RTE45) – Offset 6a

This register has the same bit definition as RTE0.

Redirection Table Entry 46 (RTE46) – Offset 6c

This register has the same bit definition as RTE0.

Redirection Table Entry 47 (RTE47) – Offset 6e

This register has the same bit definition as RTE0.

Redirection Table Entry 48 (RTE48) – Offset 70

This register has the same bit definition as RTE0.

Redirection Table Entry 49 (RTE49) – Offset 72

This register has the same bit definition as RTE0.

Redirection Table Entry 50 (RTE50) – Offset 74

This register has the same bit definition as RTE0.

Redirection Table Entry 51 (RTE51) – Offset 76

This register has the same bit definition as RTE0.

Redirection Table Entry 52 (RTE52) – Offset 78

This register has the same bit definition as RTE0.

Redirection Table Entry 53 (RTE53) – Offset 7a

This register has the same bit definition as RTE0.

Redirection Table Entry 54 (RTE54) – Offset 7c

This register has the same bit definition as RTE0.

Redirection Table Entry 55 (RTE55) – Offset 7e

This register has the same bit definition as RTE0.

Redirection Table Entry 56 (RTE56) – Offset 80

This register has the same bit definition as RTE0.

Redirection Table Entry 57 (RTE57) – Offset 82

This register has the same bit definition as RTE0.

Redirection Table Entry 58 (RTE58) – Offset 84

This register has the same bit definition as RTE0.

Redirection Table Entry 59 (RTE59) – Offset 86

This register has the same bit definition as RTE0.

Redirection Table Entry 60 (RTE60) – Offset 88

This register has the same bit definition as RTE0.

Redirection Table Entry 61 (RTE61) – Offset 8a

This register has the same bit definition as RTE0.

Redirection Table Entry 62 (RTE62) – Offset 8c

This register has the same bit definition as RTE0.

Redirection Table Entry 63 (RTE63) – Offset 8e

This register has the same bit definition as RTE0.

Redirection Table Entry 64 (RTE64) – Offset 90

This register has the same bit definition as RTE0.

Redirection Table Entry 65 (RTE65) – Offset 92

This register has the same bit definition as RTE0.

Redirection Table Entry 66 (RTE66) – Offset 94

This register has the same bit definition as RTE0.

Redirection Table Entry 67 (RTE67) – Offset 96

This register has the same bit definition as RTE0.

Redirection Table Entry 68 (RTE68) – Offset 98

This register has the same bit definition as RTE0.

Redirection Table Entry 69 (RTE69) – Offset 9a

This register has the same bit definition as RTE0.

Redirection Table Entry 70 (RTE70) – Offset 9c

This register has the same bit definition as RTE0.

Redirection Table Entry 71 (RTE71) – Offset 9e

This register has the same bit definition as RTE0.

Redirection Table Entry 72 (RTE72) – Offset a0

This register has the same bit definition as RTE0.

Redirection Table Entry 73 (RTE73) – Offset a2

This register has the same bit definition as RTE0.

Redirection Table Entry 74 (RTE74) – Offset a4

This register has the same bit definition as RTE0.

Redirection Table Entry 75 (RTE75) – Offset a6

This register has the same bit definition as RTE0.

Redirection Table Entry 76 (RTE76) – Offset a8

This register has the same bit definition as RTE0.

Redirection Table Entry 77 (RTE77) – Offset aa

This register has the same bit definition as RTE0.

Redirection Table Entry 78 (RTE78) – Offset ac

This register has the same bit definition as RTE0.

Redirection Table Entry 79 (RTE79) – Offset ae

This register has the same bit definition as RTE0.

Redirection Table Entry 80 (RTE80) – Offset b0

This register has the same bit definition as RTE0.

Redirection Table Entry 81 (RTE81) – Offset b2

This register has the same bit definition as RTE0.

Redirection Table Entry 82 (RTE82) – Offset b4

This register has the same bit definition as RTE0.

Redirection Table Entry 83 (RTE83) – Offset b6

This register has the same bit definition as RTE0.

Redirection Table Entry 84 (RTE84) – Offset b8

This register has the same bit definition as RTE0.

Redirection Table Entry 85 (RTE85) – Offset ba

This register has the same bit definition as RTE0.

Redirection Table Entry 86 (RTE86) – Offset bc

This register has the same bit definition as RTE0.

Redirection Table Entry 87 (RTE87) – Offset be

This register has the same bit definition as RTE0.

Redirection Table Entry 88 (RTE88) – Offset c0

This register has the same bit definition as RTE0.

Redirection Table Entry 89 (RTE89) – Offset c2

This register has the same bit definition as RTE0.

Redirection Table Entry 90 (RTE90) – Offset c4

This register has the same bit definition as RTE0.

Redirection Table Entry 91 (RTE91) – Offset c6

This register has the same bit definition as RTE0.

Redirection Table Entry 92 (RTE92) – Offset c8

This register has the same bit definition as RTE0.

Redirection Table Entry 93 (RTE93) – Offset ca

This register has the same bit definition as RTE0.

Redirection Table Entry 94 (RTE94) – Offset cc

This register has the same bit definition as RTE0.

Redirection Table Entry 95 (RTE95) – Offset ce

This register has the same bit definition as RTE0.

Redirection Table Entry 96 (RTE96) – Offset d0

This register has the same bit definition as RTE0.

Redirection Table Entry 97 (RTE97) – Offset d2

This register has the same bit definition as RTE0.

Redirection Table Entry 98 (RTE98) – Offset d4

This register has the same bit definition as RTE0.

Redirection Table Entry 99 (RTE99) – Offset d6

This register has the same bit definition as RTE0.

Redirection Table Entry 100 (RTE100) – Offset d8

This register has the same bit definition as RTE0.

Redirection Table Entry 101 (RTE101) – Offset da

This register has the same bit definition as RTE0.

Redirection Table Entry 102 (RTE102) – Offset dc

This register has the same bit definition as RTE0.

Redirection Table Entry 103 (RTE103) – Offset de

This register has the same bit definition as RTE0.

Redirection Table Entry 104 (RTE104) – Offset e0

This register has the same bit definition as RTE0.

Redirection Table Entry 105 (RTE105) – Offset e2

This register has the same bit definition as RTE0.

Redirection Table Entry 106 (RTE106) – Offset e4

This register has the same bit definition as RTE0.

Redirection Table Entry 107 (RTE107) – Offset e6

This register has the same bit definition as RTE0.

Redirection Table Entry 108 (RTE108) – Offset e8

This register has the same bit definition as RTE0.

Redirection Table Entry 109 (RTE109) – Offset ea

This register has the same bit definition as RTE0.

Redirection Table Entry 110 (RTE110) – Offset ec

This register has the same bit definition as RTE0.

Redirection Table Entry 111 (RTE111) – Offset ee

This register has the same bit definition as RTE0.

Redirection Table Entry 112 (RTE112) – Offset f0

This register has the same bit definition as RTE0.

Redirection Table Entry 113 (RTE113) – Offset f2

This register has the same bit definition as RTE0.

Redirection Table Entry 114 (RTE114) – Offset f4

This register has the same bit definition as RTE0.

Redirection Table Entry 115 (RTE115) – Offset f6

This register has the same bit definition as RTE0.

Redirection Table Entry 116 (RTE116) – Offset f8

This register has the same bit definition as RTE0.

Redirection Table Entry 117 (RTE117) – Offset fa

This register has the same bit definition as RTE0.

Redirection Table Entry 118 (RTE118) – Offset fc

This register has the same bit definition as RTE0.

Redirection Table Entry 119 (RTE119) – Offset fe

This register has the same bit definition as RTE0.

CNVi PCI Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Vendor and Device ID (CNVI_WIFI_VEN_DEV_ID)	XXXX8086h
4h	4	Device Command and Status (CNVI_WIFI_PCI_COM_STAT)	100000h
8h	4	Class Code and Revision ID (CNVI_WIFI_PCI_CLASS_CODE)	28000XXh
10h	4	Base Address Register BAR0 Low (CNVI_WIFI_BAR0)	4h
14h	4	Base Address Register BAR0 High (CNVI_WIFI_BAR1)	0h
2ch	4	Subsystem ID (CNVI_WIFI_SUBSYS_ID)	8086h
34h	4	Capabilities Pointer (CNVI_WIFI_CAP_PTR)	C8h
3ch	4	Interrupt (CNVI_WIFI_INTERRUPT)	100h
40h	4	PCI Express Capabilities (CNVI_WIFI_GIO_CAP)	928010h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
44h	4	Device Capabilities (CNVI_WIFI_GIO_DEV_CAP)	10000EC0h
48h	4	Device Control Register (CNVI_WIFI_GIO_DEV)	100C10h
64h	4	Device Control 2 (CNVI_WIFI_GIO_DEV_CAP_2)	80812h
68h	4	Device Control (CNVI_WIFI_GIO_DEV_2)	5h
80h	4	MSIX Capability (CNVI_WIFI_MSIX_CAP_HEAD)	F0011h
84h	4	MSIX Capability Structure (CNVI_WIFI_MSIX_TABLE_OFFSET)	2000h
88h	4	MSIX Capability Structure (CNVI_WIFI_MSIX_PBA_OFFSET)	3000h
c8h	4	Power Management Capabilities (CNVI_WIFI_PMC)	C823D001h
cch	4	Power Management Status and Control (CNVI_WIFI_PMCSR)	D000008h
d0h	4	Capability ID and Message Control (CNVI_WIFI_MSI_MSG_CTRL)	804005h
d4h	4	MSI Low Address (CNVI_WIFI_MSI_LOW_ADD)	0h
d8h	4	MSI High Address (CNVI_WIFI_MSI_HIGH_ADD)	0h
dch	4	MSI Data (CNVI_WIFI_MSI_DATA)	0h
104h	4	Uncorrectable Error Status Register (CNVI_WIFI_UNCORRECT_ERR_STAT)	0h
108h	4	Uncorrectable Error mask Register (CNVI_WIFI_UNCORRECT_ERR_MASK)	0h
10ch	4	Uncorrectable Error Severity (CNVI_WIFI_UNCORRECT_ERR_SEV)	62031h
110h	4	Error Status (CNVI_WIFI_CORRECT_ERR_STAT)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
114h	4	Error Mask (CNVI_WIFI_CORRECT_ERR_MASK)	0h
118h	4	Advanced Error Capabilities and Control (CNVI_WIFI_ADVANCED_ERR_CAP)	0h
11ch	4	Header Log 1 (CNVI_WIFI_HEADER_LOG1)	0h
120h	4	Header Log 2 (CNVI_WIFI_HEADER_LOG2)	0h
124h	4	Header Log 3 (CNVI_WIFI_HEADER_LOG3)	0h
128h	4	Header Log 4 (CNVI_WIFI_HEADER_LOG4)	0h
140h	4	Device Serial Number Capability (CNVI_WIFI_GIO_SERIAL_CAP)	14C00000h
144h	4	Serial Number Low (CNVI_WIFI_GIO_SERIAL_LOW)	FF000000h
148h	4	Serial Number Upper (CNVI_WIFI_GIO_SERIAL_UP)	FFh
14ch	4	Header of LTR Extended Capability (CNVI_WIFI_LTR_EXTND_CAP_HEAD)	16410018h
150h	4	No Snoop Request (CNVI_WIFI_LTR_MAX_SNOOP_NOSNOOP_LAT)	0h
154h	4	L1 substates Extended Capability Header (CNVI_WIFI_L1PM_SUB_EXTND_CAP_HEAD)	1001Eh
158h	4	L1 Substates Capability (CNVI_WIFI_L1PM_SUB_CAP)	481E1Fh
15ch	4	L1 Substates Control (CNVI_WIFI_L1PM_SUB_CNTRL)	0h
160h	4	L1 Substates Control 2 (CNVI_WIFI_L1PM_SUB_CNTRL2)	28h
164h	4	Vendor Specific Capability Header (CNVI_WIFI_VEN_SPEC_CAP)	1000Bh

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
168h	4	Vendor Specific Extended Capability (CNVI_WIFI_VEN_SPEC_EXTND_CAP)	1400010h
16ch	4	SW LTR Pointer (CNVI_WIFI_LTP_PTR)	0h
170h	4	DevIdle Pointer (CNVI_WIFI_DEV_IDLE_PTR)	31800001h
174h	4	DevIdle Power on Latency (CNVI_WIFI_DEV_IDLE_PWR)	800h

Vendor and Device ID (CNVI_WIFI_VEN_DEV_ID) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:16	See Description	RO	**Device ID (DEV_ID)** Indicates the Device ID of the controller. Refer to the Device and Revision ID Table in Volume 1 for the default value.
15:0	0x8086	RO	**Vendor ID (VEN_ID)** Indicates Intel.

Device Command and Status (CNVI_WIFI_PCI_COM_STAT) – Offset 4

Bit Range	Default	Access	Field Name and Description
31	0x0	RW/1C	**Detected Parity Error (DET_PAR_ERR)**
30	0x0	RW/1C	**Signaled System Error (SIG_SYS_ERR)**
29	0x0	RW/1C	**Received Master Abort (REC_MAS_ABRT)**

Bit Range	Default	Access	Field Name and Description
28	0x0	RW/1C	**Received Target Abort (REC_TAR_ABRT)**
27	0x0	RW/1C	**Signaled Target Abort (SIG_TAR_ABRT)**
26:25	0x0	RO	**DEVSEL Timing (DEVSEL_TIMING)** Does not apply. Hardwired to 0.
24	0x0	RW/1C	**Master Data Parity Error (MAS_DATA_PAR_ER)** Master Data Parity Error
23	0x0	RO	**Fast Back to Back Transaction Capable (FAST_BTB_TCAP)** Does not apply. Hardwired to 0.
22	-	-	**Reserved**
21	0x0	RO	**66 MHz Capable (OLF_FREQ_CAP)** Does not apply. Hardwired to 0.
20	0x1	RO	**Capability List (CAP_LST)** Hardwired to 1.
19	0x0	RO	**Interrupt Status (INTRPT_STS)** Reflects the state of the interrupt in the device.
18:11	-	-	**Reserved**
10	0x0	RW	**Interrupt Disable (INTRPT_DIS)** Controls the ability of the device to generate legacy interrupt messages. 0 = Enable. 1 = Disable.
9	0x0	RO	**Fast Back to Back Enable (FAST_BTB_TNSCEN)** Does not apply. Hardwired to 0.
8	0x0	RW	**SERR Enable (SERR_EN)** Enable SERR# to be generated if this bit is set.

Bit Range	Default	Access	Field Name and Description
7	0x0	RO	**Wait Cycle Control (IDSEL_STEP_W_CY)** Does not apply. Hardwired to 0.
6	0x0	RW	**Parity Error Enable (PAR_ERR)** This bit is set to 1 to enable response to parity errorswhen detected.
5	0x0	RO	**VGA Palette Snoop (VGA_PALT_SNOOP)** Does not apply. Hardwired to 0.
4	0x0	RO	**Memory Write and Invalidate (MEM_WR_INVALD)** Does not apply. Hardwired to 0.
3	0x0	RO	**Special Cycle Enable (SPEC_CYC_ENB)** Does not apply. Hardwired to 0.
2	0x0	RW	**Bus Master Enable (BUS_MAS)** 0 = Bus master is disabled. 1 = Bus master is enabled.
1	0x0	RW	**Memory Space Access Enable (MEM_SP_ACC)** 0 = Memory space access is disabled. 1 = Memory space access is enabled.
0	0x0	RO	**IO Space Access Enable (IO_SPC_AC_EN_0)** 0 = IO space access is disabled. 1 = IO space access is enabled.

Class Code and Revision ID (CNVI_WIFI_PCI_CLASS_CODE) – Offset 8

Bit Range	Default	Access	Field Name and Description
31:24	0x2	RO	**Base Class Code (SE_CLASS)** Classifies the type of function the device perform.
23:16	0x80	RO	**Sub-Class Code (SUB_CLASS)** Identifies more specifically the function of the device.

Bit Range	Default	Access	Field Name and Description
15:8	0x0	RO	**Interface (INTERFACE)** Identifies a specific register-level programming interface. Does not apply. Hardwired to 0.
7:0	See Description	RO	**Revision ID (REV_ID)** Identifies the revision of the device. Refer to Device and Revision ID Table in Vol1 for specific value.

Base Address Register BAR0 Low (CNVI_WIFI_BAR0) – Offset 10

Bit Range	Default	Access	Field Name and Description
31:14	0x0	RW	**Base Address Field (BS_ADD_FLD_RW)** Provides system memory base address for thecontroller.
13:4	0x0	RO	**Base Address Field (BS_ADD_FLD_RO)** Hardwired to 0.
3	0x0	RO	**Prefetchable (PREFETCHBL)** Defines the block of memory as Prefetchable or not. 0 indicates that this BAR is not prefetchable.
2:1	0x2	RO	**Decoder Width Field (DECOD_WDTH_FLD)** Decoder Width Field (10b-64bit reg).
0	0x0	RO	**Memory Space Indicator (MEM_SPAC_INDIC)** Hardwired to 0.Indicates this BAR is present in the memory space.

Base Address Register BAR0 High (CNVI_WIFI_BAR1) – Offset 14

Bit Range	Default	Access	Field Name and Description
31:0	0x0	RW	**Base Address High (BS_ADD_FLD)**

Subsystem ID (CNVI_WIFI_SUBSYS_ID) – Offset 2c

Bit Range	Default	Access	Field Name and Description
31:16	0x0	RO	**Subsystem Device ID (SB_DEV_ID)**
15:0	0x8086	RO	**Subsystem Vendor ID (SB_VEN_ID)** Indicates Intel.

Capabilities Pointer (CNVI_WIFI_CAP_PTR) – Offset 34

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	0xc8	RO	**Capabilities Pointer (CARDB_PTR)** Indicates what the next capability is.

Interrupt (CNVI_WIFI_INTERRUPT) – Offset 3c

Bit Range	Default	Access	Field Name and Description
31:24	0x0	RO	**Max Latency (MAX_LATNC)** Does not apply. Hardwired to 0.
23:16	0x0	RO	**Min Latency (MIN_GNT)** Does not apply. Hardwired to 0.
15:8	0x1	RO	**Interrupt Pin (INT_PIN)** Identifies which interrupt pin the device uses.
7:0	0x0	RW	**Interrupt Line (INT_LINE)** Identifies which input interrupt request pin is routed to.

PCI Express Capabilities (CNVI_WIFI_GIO_CAP) – Offset 40

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29:25	0x0	RO	**Interrupt Message Number (INTRPT_MSG_NUM)**
24	0x0	RO	**Slot Implemented (SLT_IMPLNT)**
23:20	0x9	RO	**Device Port Type (DEV_POR_TYP)**
19:16	0x2	RO	**Capability Version (CAP_VER)** 2h = Gen 2.0.
15:8	0x80	RO	**Next Capability Pointer (GIO_CAP_NXT_OFS)** The offset to the next PCI capability structure.
7:0	0x10	RO	**Capability Structure (INCD_PCIE_CST)** Indicates PCI Express Capability Structure.

Device Capabilities (CNVI_WIFI_GIO_DEV_CAP) – Offset 44

The Device Capabilities register identifies PCI Express device specific capabilities.(Offset 044 h)

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**
28	0x1	RO	**Function Level Reset Capability (FUNC_LVL_RES)**
27:26	0x0	RO	**Slot Power Limit Scale (SLT_PW_LSCL)** Captured Slot Power Limit Scale

Bit Range	Default	Access	Field Name and Description
25:18	0x0	RO	**Slot Power Limit Value (SLT_PW_LVAL)** Captured Slot Power Limit Value
17:16	-	-	**Reserved**
15	0x0	RO	**Error Reporting Support (ROLE_BASED_ERR)** This field indicates that the device supports Error reporting.
14:12	-	-	**Reserved**
11:9	0x7	RO	**Endpoint L1 Acceptable Latency (L1_ACC_LAT)**
8:6	0x3	RO	**Endpoint L0s Acceptable Latency (L0S_ACC_LAT)**
5	0x0	RO	**Extended Tag Field Supported (EX_TAG_FIELD)**
4:3	-	-	**Reserved**
2:0	0x0	RO	**Max Payload Size Supported (MAX_PL_SIZE)**

Device Control Register (CNVI_WIFI_GIO_DEV) – Offset 48

Bit Range	Default	Access	Field Name and Description
30:22	-	-	**Reserved**
21	0x0	RO	**TRANS_PEND (TRANS_PEND)** indicates that a device has Non-Posted Requests which have not been completed
20	0x1	RO	**Aux Power (AUX_P_DET)** device that requires AUX power reports this bit (asynch signal)

Bit Range	Default	Access	Field Name and Description
19	0x0	RW/1C	**Unsupported Request Detected (UNSOP_REQ_DET)** indicates that the device received Unsupported Request
18	0x0	RW/1C	**Fatal Error Detected (FAT_ERR_DET)** indicates status of fatal errors detected
17	0x0	RW/1C	**Non-Fatal Error Detected (NFAT_ER_DET)** indicates status of non-fatal errors detected
16	0x0	RW/1C	**Correctable Errors Detected (COR_ERR_DET)** indicates status of correctable errors detected
15	0x0	RO	**Initiate Function Level Reset (INIT_FNC_LV_RS)** A write of 1b initiates Function (init FLR)
14:12	0x0	RW	**Max Read Request Size (MAX_RDRQ_SIZE)** sets the maximum Read Request size
11	0x1	RW	**Enable No Snoop (EN_NO_SNOOP)** if set device is permitted to set No Snoop bit.
10	0x1	RW	**Auxiliary Power PM Enable (AUX_PM_EN)** Sticky value.
9	-	-	**Reserved**
8	0x0	RO	**IO Space access Enable (IO_SPC_AC_EN_8)**
7:5	0x0	RW	**Max Payload Size (MAX_PAY_SIZE)** sets maximum TLP payload size for the device functions
4	0x1	RW	**Relax Order Enable (EN_REL_ORD)** when set device permitted to set the Relaxed Ordering bit
3	0x0	RW	**Unsupported Request Reporting (UNSOP_REQ_REP)** enables reporting of Unsupported Request when set
2	0x0	RW	**Fatal Error Reporting (FAT_ERR_REP)** controls reporting of fatal errors

Bit Range	Default	Access	Field Name and Description
1	0x0	RW	**Non-Fatal Error Reporting (NFAT_ER_REP)** controls reporting of non-fatal errors
0	0x0	RW	**Correctable Error Reporting (COR_ERR_REP)** controls reporting of correctable errors

Device Control 2 (CNVI_WIFI_GIO_DEV_CAP_2) – Offset 64

Bit Range	Default	Access	Field Name and Description
30:20	-	-	**Reserved**
19:18	0x2	RO	**OBFF Support (OBFF_MEC_SUP)** 0x00 = unsupported 0x01 = supported using message signaling A 0x10 = suported using signaling B 0x11 = supported using WAKE signaling
17:12	-	-	**Reserved**
11	0x1	RO	**LTR Mechanism Support (LTR_MEC_SUP)** A value of 1b indicates support for LTR.
10:5	-	-	**Reserved**
4	0x1	RO	**Complete Timeout Disable (CMP_TO_DIS_SUP)** 1 = support for the Completion Timeout Disable, 0 = not supported. Hardwired to 0x1.
3:0	0x2	RO	**Completion Timeout Ranges Supported (CMP_TO_RNG_SUP)** Hardwired to 0x2.

Device Control (CNVI_WIFI_GIO_DEV_2) – Offset 68

Bit Range	Default	Access	Field Name and Description
30:15	-	-	**Reserved**
14:13	0x0	RW	**OBFF enable (OBFF_MEC_ENA)** OBFF enable: 0x00 -disable , 0x01 - enabled using message signaling A, 0x10 - message signaling B ,0x11-enabled using WAKE signaling
12:11	-	-	**Reserved**
10	0x0	RW	**LTR Mechanism Enable (LTR_MEC_EN)** When Set enables the LTR.
9:5	-	-	**Reserved**
4	0x0	RW	**CMP_TO_DIS (CMP_TO_DIS)** When Set, this bit disables the Completion Timeout mechanism
3:0	0x5	RW	**CMP_TO_VAL (CMP_TO_VAL)** this field allows system SW to modify the Completion Timeout value

MSIX Capability (CNVI_WIFI_MSIX_CAP_HEAD) – Offset 80

Bit Range	Default	Access	Field Name and Description
31	0x0	RW	**MSIX_ENABLE (MSIX_ENABLE)** If set to 1, the function is permitted to use MSI-X to request service. System configuration software sets this bit to enable MSI-X. A device driver is prohibited from writing this bit to mask a function's service request. If 0, the function is prohibited from using MSI-X to request service.

Bit Range	Default	Access	Field Name and Description
30	0x0	RW	**FUN_MASK (FUN_MASK)** If set to 1, all of the vectors associated with the function are masked, regardless of their per-vector Mask bit states. If 0, each vector's Mask bit determines whether the vector is masked or not. Setting or clearing the MSI-X Function Mask bit has no effect on the state of the per-vector Mask bits
29:27	-	-	**Reserved**
26:16	0xf	RO	**TABLE_SIZE (TABLE_SIZE)** System software reads this field to determine the MSI-X Table Size N, which is encoded as (N-1). Wifi Host supports Table Size of 16 and encodes a number of 15.
15:8	0x0	RO	**NEXT_PTR (NEXT_PTR)** Pointer to the next item in the capabilities list. NULL if last
7:0	0x11	RO	**MSIX_CAP_ID (MSIX_CAP_ID)** The value of 11h in this field identifies the function as being MSI-X capable.

MSIX Capability Structure (CNVI_WIFI_MSIX_TABLE_OFFSET) – Offset 84

Bit Range	Default	Access	Field Name and Description
31:3	0x400	RO	**TABLE_OFFSET (TABLE_OFFSET)** Used as an offset from the address contained by the Base Address register to point to the base of the MSI-X Table. The lower 3 bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. In Wifi Host the table is at 0x2000, so the value of this field in 0x400.

Bit Range	Default	Access	Field Name and Description
2:0	0x0	RO	**TABLE_BIR (TABLE_BIR)** Indicates which one of a function's Base Address registers, located beginning at 10h in configuration Space, and is used to map the function's MSI-X Table into Memory Space. Wifi Host cluster uses a single BAR to point to the MSI-X structures.

MSIX Capability Structure (CNVI_WIFI_MSIX_PBA_OFFSET) – Offset 88

Bit Range	Default	Access	Field Name and Description
31:3	0x600	RO	**TABLE_OFFSET (TABLE_OFFSET)** Used as an offset from the address contained by the Base Address register to point to the base of the MSI-X PBA Table. The lower 3 bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. In Wifi Host the table is at 0x3000, so the value of this field in 0x600.
2:0	0x0	RO	**TABLE_BIR (TABLE_BIR)** Indicates which one of a function's Base Address registers, located beginning at 10h in configuration Space, and is used to map the function's MSI-X Table into Memory Space. Wifi Host cluster uses a single BAR to point to the MSI-X structures.

Power Management Capabilities (CNVI_WIFI_PMC) – Offset c8

Bit Range	Default	Access	Field Name and Description
31:27	0x19	RO	**PME_SUPRT (PME_SUPRT)** PME Support,indicates the power states in which the device may assert PME

Bit Range	Default	Access	Field Name and Description
26	0x0	RO	**D2_PWR_MANG (D2_PWR_MANG)** D2 Power Management State support
25	0x0	RO	**D1_PWR_MANG (D1_PWR_MANG)** D1 Power Management State support
24:22	0x0	RO	**AUX_CUR (AUX_CUR)** AUX Current (Used data register instead)
21	0x1	RO	**DEV_SPC_INT (DEV_SPC_INT)** Device Specific Initialization
20	-	-	**Reserved**
19	0x0	RO	**PME_CLK (PME_CLK)** Does not apply. Hardwired to 0.
18:16	0x3	RO	**VERSION (VERSION)** value indicates that this function complies with the Revision 1.2
15:8	0xd0	RO	**PMC_NXT_PTR (PMC_NXT_PTR)** Next PTR, pointing to the location of next item in the functions capability list HARDWIRED
7:0	0x1	RO	**PMC_CAP_ID (PMC_CAP_ID)** Capability ID, Indicates the linked list item is the PCI Power Management Registers HARDWIRED

Power Management Status and Control (CNVI_WIFI_PMCSR) – Offset cc

Bit Range	Default	Access	Field Name and Description
31:24	0xd	RO	**PWR_DIS_CON (PWR_DIS_CON)** used to report power consumption and heat dissipation (default for D3-0x1)

Bit Range	Default	Access	Field Name and Description
23	0x0	RO	**BUS_PWR_CLK_CEN (BUS_PWR_CLK_CEN)** Bus Power/Clock Control Enable. Does not apply. Hardwired to 0.
22	0x0	RO	**B2_B3_SUPRT (B2_B3_SUPRT)** B2/B3 Support. Does not apply. Hardwired to 0.
21:16	-	-	**Reserved**
15	0x0	RW/1C	**PME_STAT (PME_STAT)** This bit reflects whether the function has experienced a PME. sticky value.
14:13	0x0	RO	**DAT_SCALE (DAT_SCALE)** Data Scale
12:9	0x0	RW	**DAT_SEL (DAT_SEL)** Data Select, selects the data value to be viewed through the Data register
8	0x0	RW	**PME_ENA (PME_ENA)** PME Enable. sticky value.
7:4	-	-	**Reserved**
3	0x1	RO	**NO_SOFT_RESET (NO_SOFT_RESET)** No_Soft_Reset
2	-	-	**Reserved**
1:0	0x0	RW	**PWR_STATE (PWR_STATE)** Power State

Capability ID and Message Control (CNVI_WIFI_MSI_MSG_CTRL) – Offset d0

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0x1	RO	**64 Bit Address Capable (BITA_CAP_64)** Hardwired to 1.
22:20	0x0	RO	**Multiple Message Enable (MUL_MSG_ENB)** Hardwired to 0.
19:17	0x0	RO	**Multiple Message Capable (MUL_MSG_CAP)** Hardwired to 0.
16	0x0	RW	**MSI Enable (MSI_ENA)** function is enabled to use MSI to request service and is forbidden to use its interrupt pin
15:8	0x40	RO	**Next Capability Pointer (MSI_MC_NXT_PTR)**
7:0	0x5	RO	**Capability ID (MSI_MC_CAP_ID)** Hardwired to 0x5.

MSI Low Address (CNVI_WIFI_MSI_LOW_ADD) – Offset d4

Specifies the lower DWORD of the address for the MSI memory write transaction (Offset 0D4 h)

Bit Range	Default	Access	Field Name and Description
31:2	0x0	RW	**MSG_ADD_LOW (MSG_ADD_LOW)** Lower DWORD of the address
1:0	0x0	RO	**MSI_LOW_AD_1_0 (MSI_LOW_AD_1_0)** HARDWIRED

MSI High Address (CNVI_WIFI_MSI_HIGH_ADD) – Offset d8

Specifies the upper DWORD of the address for the MSI memory write transaction

Bit Range	Default	Access	Field Name and Description
31:0	0x0	RW	**MSG_ADD_UP (MSG_ADD_UP)** upper DWORD of the address

MSI Data (CNVI_WIFI_MSI_DATA) – Offset dc

Written by the system to indicate the lower 16 bits of the data written in the MSI memory write DWORD transaction (Offset 0DC h)

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0x0	RW	**MSG_DATA (MSG_DATA)** data written in the MSI memory write DWORD transaction

Uncorrectable Error Status Register (CNVI_WIFI_UNCORRECT_ERR_STAT) – Offset 104

Bits in this register are of type RW1CS. Software may clear an error status by writing a 1

Bit Range	Default	Access	Field Name and Description
30:21	-	-	**Reserved**
20	0x0	RW/1C	**Unsupported Request Error Status (UNSPR_REQ_ERR_ST)** Sticky value
19	0x0	RO	**ECRC Error Status (ECRC_ERR_STS_19)** Not implemented
18	0x0	RW/1C	**Malformed TLP Status (MAL_TLP_ST)** if set indicates that the error occurred. Sticky value
17	0x0	RW/1C	**Receiver Overflow Status (REC_OVRF_ERR)** if set indicates that the error occurred. Sticky value

Bit Range	Default	Access	Field Name and Description
16	0x0	RW/1C	**Unexpected Completion Status (UNXPC_COM_ER)** if set indicates that the error occurred. Sticky value
15	0x0	RW/1C	**Completer Abort Status (COM_AB_ERR)** if set indicates that the error occurred. Sticky value
14	0x0	RW/1C	**Completion Timeout Status (COM_TO_ERR)** if set indicates that the error occurred. Sticky value
13	0x0	RW/1C	**Flow Control Protocol Error Status (FLWCNT_PR_ER)** if set indicates that the error occurred. Sticky value
12	0x0	RW/1C	**Poisoned TLP Status (POIS_TLP_ERR)** if set indicates that the error occurred. Sticky value
11:5	-	-	**Reserved**
4	0x0	RW/1C	**Data Link Protocol Error Status (DLNK_PRERR_ST)** if set indicates that the error occurred. sticky value
3:1	-	-	**Reserved**
0	0x0	RO	**Training Error Status (TRNG_ERR_STS_0)** Not implemented.

Uncorrectable Error mask Register (CNVI_WIFI_UNCORRECT_ERR_MASK) – Offset 108

Bits in this register are of type RWS - if set to 1 the error is not logged in the Header Log register, or does not update the First Error Pointer and is not reported to PCI Express Root Complex.

Bit Range	Default	Access	Field Name and Description
30:21	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
20	0x0	RW	**Unsupported Request Error Mask (UNSPR_REQ_ERR_MSK)** Sticky value.
19	0x0	RO	**ECRC Error mask (ECRC_ERR_MSK_19)** Not implemented.
18	0x0	RW	**Malformed TLP Mask (MAL_TLP_MSK)** Sticky value.
17	0x0	RW	**Receiver Overflow Mask (REC_OVRF_MSK)** Sticky value.
16	0x0	RW	**Unexpected Completion Mask (UNXPL_COM_MSK)** Sticky value.
15	0x0	RW	**Completer Abort Mask (COM_AB_MSK)** Sticky value.
14	0x0	RW	**Completion Timeout Mask (COM_TO_MSK)** Sticky value.
13	0x0	RW	**Flow Control Protocol Error Mask (FLWCNT_PR_MSK)** Sticky value.
12	0x0	RW	**Poisoned TLP Mask (POIS_TLP_MSK)** Sticky value.
11:5	-	-	**Reserved**
4	0x0	RW	**Header Log (DLNK_PRERR_MSK)** Does not update the First Error Pointer and is not Data Link Protocol Error Mask, if set to 1 the error is not logged in the Header. Sticky value
3:1	-	-	**Reserved**
0	0x0	RO	**Training Error Mask (TRNG_ERR_MSK_0)** Not implemented.

Uncorrectable Error Severity (CNVI_WIFI_UNCORRECT_ERR_SEV) – Offset 10c

Bit value in this register are sticky - the error is reported as fatal when the field is set to 1; if it is cleared to 0, the error is considered non-fatal.

Bit Range	Default	Access	Field Name and Description
30:21	-	-	**Reserved**
20	0x0	RW	**Unsupported Request Error Severity (UNSPR_REQ_ERR_SVR)**
19	-	-	**Reserved**
18	0x1	RW	**Malformed TLP Severity (MAL_TLP_SVR)**
17	0x1	RW	**Receiver Overflow Severity (REC_OVRF_SVR)**
16	0x0	RW	**Unexpected Completion Severity (UNXPL_COM_SVR)**
15	0x0	RW	**Completer Abort Severity (COM_AB_SVR)**
14	0x0	RW	**Completion Timeout Severity (COM_TO_SVR)**
13	0x1	RW	**Flow Control Protocol Error Severity (FLWCNT_PR_SVR)**
12	0x0	RW	**Poisoned TLP Severity (POIS_TLP_SVR)**
11:6	-	-	**Reserved**
5	0x1	RW	**Surprise Down Error Severity (SURPRISE_DWN_SVR)**

Bit Range	Default	Access	Field Name and Description
4	0x1	RW	**Data Link Protocol Error Severity (DLNK_PRERR_SVR)**
3:1	-	-	**Reserved**
0	0x1	RO	**Training Error severity (TRNG_ERR_SVR_0)**

Error Status (CNVI_WIFI_CORRECT_ERR_STAT) – Offset 110

Reg bits in this register are of type RW1CS - if set to 1 indicates that the error occurred. Software may clear the bit by writing a 1.

Bit Range	Default	Access	Field Name and Description
30:13	-	-	**Reserved**
12	0x0	RW/1C	**Replay Timer Timeout Error Status (REPL_TO_ST)**
11:9	-	-	**Reserved**
8	0x0	RW/1C	**REPLAY_NUM Rollover Status (REPL_ROLVR_ST)**
7	0x0	RW/1C	**Bad DLLP Status (BD_DLLP_ST)**
6	0x0	RW/1C	**Bad TLP Status (BD_TLP_ST)**
5:1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	0x0	RW/1C	**REV_ERR_ST (REV_ERR_ST)**

Error Mask (CNVI_WIFI_CORRECT_ERR_MASK) – Offset 114

Bits in this register are of type RWS (Sticky) - if set to 1 the error is masked and not reported.

Bit Range	Default	Access	Field Name and Description
30:13	-	-	**Reserved**
12	0x0	RW	**Replay Timer Timeout Error Mask (REPL_TO_MSK)**
11:9	-	-	**Reserved**
8	0x0	RW	**REPLAY_NUM Rollover Mask (REPL_ROLVR_MSK)**
7	0x0	RW	**Bad DLLP Mask (BD_DLLP_MSK)**
6	0x0	RW	**Bad TLP Mask (BD_TLP_MSK)**
5:1	-	-	**Reserved**
0	0x0	RW	**Receiver Error Mask (REV_ERR_MSK)**

Advanced Error Capabilities and Control (CNVI_WIFI_ADVANCED_ERR_CAP) – Offset 118

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RO	**ECRC Check Enable (ECRC_CHK_EN)** if set enables ECRC checking.
7	0x0	RO	**ECRC Check Capable (ECRC_CHK_CP)** indicates the device is capable of checking ECRC.
6	0x0	RO	**ECRC Generation Enable (ECRC_GEN_EN)** if set enables ECRC generation.
5	0x0	RO	**ECRC Generation Capable (ECRC_GEN_CP)** indicates that the device is capable of generation ECRC.
4:0	0x0	RO	**First Error Pointer (FRST_ERR_PNT)** error reported in the Uncorrectable Error Status register First Error Pointer, identifies bit position of the first

Header Log 1 (CNVI_WIFI_HEADER_LOG1) – Offset 11c

Captures the header of TLP associated with error.

Bit Range	Default	Access	Field Name and Description
31:0	0x0	RO	**HEADER_LOG_1 (HEADER_LOG_1)** captures the header of TLP associated with error

Header Log 2 (CNVI_WIFI_HEADER_LOG2) – Offset 120

Captures the header of TLP associated with error.

Bit Range	Default	Access	Field Name and Description
31:0	0x0	RO	**HEADER_LOG_2 (HEADER_LOG_2)** captures the header of TLP associated with error

Header Log 3 (CNVI_WIFI_HEADER_LOG3) – Offset 124

Captures the header of TLP associated with error.

Bit Range	Default	Access	Field Name and Description
31:0	0x0	RO	**HEADER_LOG_3 (HEADER_LOG_3)** captures the header of TLP associated with error

Header Log 4 (CNVI_WIFI_HEADER_LOG4) – Offset 128

Captures the header of TLP associated with error.

Bit Range	Default	Access	Field Name and Description
31:0	0x0	RO	**HEADER_LOG_4 (HEADER_LOG_4)** captures the header of TLP associated with error

Device Serial Number Capability (CNVI_WIFI_GIO_SERIAL_CAP) – Offset 140

Bit Range	Default	Access	Field Name and Description
31:20	0x14c	RO	**NXT_CAP_OFF (NXT_CAP_OFF)** Next Capability Offset, next is the LTR header
19:16	0x0	RO	**CAP_VER (CAP_VER)** Capability Version: Zero to skip Serial Number
15:0	0x0	RO	**EXT_CAP_ID (EXT_CAP_ID)** PCI Express Extended Capability ID: Zero to skip Serial Number

Serial Number Low (CNVI_WIFI_GIO_SERIAL_LOW) – Offset 144

Bit Range	Default	Access	Field Name and Description
31:24	0xff	RO	**HARDWIRED_SR_LW (HARDWIRED_SR_LW)** hardwired to 0xFF
23:16	0x0	RO	**Byte 6 (BYTE_6)**
15:8	0x0	RO	**Byte 5 (BYTE_5)**
7:0	0x0	RO	**Byte 4 (BYTE_4)**

Serial Number Upper (CNVI_WIFI_GIO_SERIAL_UP) – Offset 148

Bit Range	Default	Access	Field Name and Description
31:24	0x0	RO	**Byte 1 (BYTE_1)**
23:16	0x0	RO	**Byte 2 (BYTE_2)**
15:8	0x0	RO	**Byte 3 (BYTE_3)**
7:0	0xff	RO	**HARDWIRED_SR_UP (HARDWIRED_SR_UP)** hardwired to 0xFF

Header of LTR Extended Capability (CNVI_WIFI_LTR_EXTND_CAP_HEAD) – Offset 14c

Bit Range	Default	Access	Field Name and Description
31:20	0x164	RO	**Next Capability Offset (LTR_HD_NXT_PTR)** Next is the Vendor Specific Capability Header.

Bit Range	Default	Access	Field Name and Description
19:16	0x1	RO	**Capability Version (LTR_HD_CAP_VER)** Hardwired to 1.
15:0	0x18	RO	**Capability ID (LTR_HD_CAP_ID)** PCI Express Extended Capability ID for the LTR Extended Capability is 0018h

No Snoop Request (CNVI_WIFI_LTR_MAX_SNOOP_NOSNOOP_LAT) – Offset 150

This register specifies the maximum no-snoop latency that a device is permitted to request.

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**
28:26	0x0	RW	**NSNP_MX_LAT_SCL (NSNP_MX_LAT_SCL)** no-snoop max latency scale. set by SW
25:16	0x0	RW	**NSNP_MX_LAT_VAL (NSNP_MX_LAT_VAL)** no-snoop max latency value. set by SW
15:13	-	-	**Reserved**
12:10	0x0	RW	**SNP_MAX_LAT_SCL (SNP_MAX_LAT_SCL)** snoop max latency scale. set by SW
9:0	0x0	RW	**SNP_MAX_LAT_VAL (SNP_MAX_LAT_VAL)** snoop max latency value. set by SW

L1 substates Extended Capability Header (CNVI_WIFI_L1PM_SUB_EXTND_CAP_HEAD) – Offset 154

Bit Range	Default	Access	Field Name and Description
31:20	0x0	RO	**Next Capability Offset (NXT_PTR)** 0x0 for last extended capability.
19:16	0x1	RO	**Capability Version (CAP_VER)** Hardwired to 1.
15:0	0x1e	RO	**Capability ID (EXT_CAP_ID)** PCI Express Extended Capability ID for L1 PM

L1 Substates Capability (CNVI_WIFI_L1PM_SUB_CAP) – Offset 158

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:19	0x9	RO	**L1SUB_PWRON_REQ (L1SUB_PWRON_REQ)** Port requirement for T_POWER_ON value
18	-	-	**Reserved**
17:16	0x0	RO	**T_PWRON_SCALE (T_PWRON_SCALE)** Portrequirement for T_POWER_ON scale
15:8	0x1e	RO	**CMN_RESTORE_TM (CMN_RESTORE_TM)** Port common mode restore time
7:5	-	-	**Reserved**
4	0x1	RO	**L1SUB_PM_SUP (L1SUB_PM_SUP)** 1 = L1 PM substate supported.
3	0x1	RO	**L11_ASPM_SUP (L11_ASPM_SUP)** 1 = ASPM L1.1 is supported.

Bit Range	Default	Access	Field Name and Description
2	0x1	RO	**L12_ASPM_SUP (L12_ASPM_SUP)** 1 = ASPM L1.2 is supported.
1	0x1	RO	**L11_PM_SUP (L11_PM_SUP)** 1 = PM L1.1 is supported.
0	0x1	RO	**L12_PM_SUP (L12_PM_SUP)** 1 = PM L1.2 is supported.

L1 Substates Control (CNVI_WIFI_L1PM_SUB_CNTRL) – Offset 15c

Bit Range	Default	Access	Field Name and Description
31:29	0x0	RW	**LTR_L1_THRS_SCL (LTR_L1_THRS_SCL)** LTR L1.2 threshold scale
28:26	-	-	**Reserved**
25:16	0x0	RW	**LTR_L1_THRS_VAL (LTR_L1_THRS_VAL)** LTR L1.1 threshold value, detemines if entry to L1 results in L1.1 or L1.2 (if they are enabled). scale of value set by: LTR L1.2 threshold scale
15:4	-	-	**Reserved**
3	0x0	RW	**L11_ASPM_EN (L11_ASPM_EN)** L1.1 ASPM is enabled
2	0x0	RW	**L12_ASPM_EN (L12_ASPM_EN)** L1.2 ASPM is enabled
1	0x0	RW	**L11_PM_EN (L11_PM_EN)** L1.1 PM is enabled
0	0x0	RW	**L12_PM_EN (L12_PM_EN)** L1.2 PM is enabled

L1 Substates Control 2 (CNVI_WIFI_L1PM_SUB_CNTRL2) – Offset 160

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:3	0x5	RW	**T_POWER_ON_VAL (T_POWER_ON_VAL)** T power on value. Along with power on scale - sets min time in L1.2.exit
2	-	-	**Reserved**
1:0	0x0	RW	**L12_PWRON_SCALE (L12_PWRON_SCALE)** T power on scale. 0 =2us, 1=10us, 2=100us, 11 = reserved

Vendor Specific Capability Header (CNVI_WIFI_VEN_SPEC_CAP) – Offset 164

Bit Range	Default	Access	Field Name and Description
31:20	0x0	RO	**Next Capability Offset (VSNEXT)** This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.
19:16	0x1	RO	**Vendor Specific Extended Capability Revision (VSECREV)** The version of the PCIe capability structure present. Hardwired to 1h.
15:0	0xb	RO	**Vendor Specific PCI Express Extended Capability ID (VSPCIECID)** The Extended Capability ID for the Vendor-Specific Capability is 000Bh.

Vendor Specific Extended Capability (CNVI_WIFI_VEN_SPEC_EXTND_CAP) – Offset 168

Bit Range	Default	Access	Field Name and Description
31:20	0x14	RO	**VSECLEN (VSECLEN)** Vendor Specific Extended Capability Length (VSECLEN): This field indicates the # of bytes of this Vendor Specific capability inclusive of the 1st DW which includes the capability ID and Next pointer. For DevIdle, this is 14h
19:16	0x0	RO	**VSECREV (VSECREV)** Vendor Specific Extended Capability Revision (VSECREV): For this revision of DevIdle, this field is 0h
15:0	0x10	RO	**VSECID (VSECID)** Vendor Specific Extended Capability ID (VSECID): DevIdle has been assigned the Intel VSEC ID of 10h

SW LTR Pointer (CNVI_WIFI_LTP_PTR) – Offset 16c

Bit Range	Default	Access	Field Name and Description
31:20	0x0	RO	**SWLTRLOC (SWLTRLOC)** SW LTR Update MMIO Offset Location This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR. The value of this register is a don't care, if the Valid bit is not set
19:4	-	-	**Reserved**
3:1	0x0	RO	**BARNUM (BARNUM)** Base Address Register Number. Contains the 0's based AR Number of the BAR which contains the location of the SW LTR MMIO register.
0	0x0	RO	**VALID (VALID)** Hardwired to '0' to indicate that the function has not implemented a SW LTR register that is compliant to the DevIdle definition. This could be because the function has not implemented SW LTR at all, or has a device specific version of SW LTR.

DevIdle Pointer (CNVI_WIFI_DEV_IDLE_PTR) – Offset 170

Bit Range	Default	Access	Field Name and Description
31:20	0x318	RO	**DEVIDLELOC (DEVIDLELOC)** DevIdle MMIO Offset Location.Contains the location pointer to the DevIdle register in MMIO space, as an offset from the specified BAR. The value of this register is a don't care, if the Valid bit is not set
19:4	-	-	**Reserved**
3:1	0x0	RO	**BARNUM (BARNUM)** Base Address Register Number. Contains the 0's based BAR Number of the BAR which contains the location of the DevIdle MMIO register. When counting BAR Numbers, all BARs, regardless of size and type, consume one BAR BAR Number. Bar 0 is the 1st BAR. The value of this register is a don't care, if the Valid bit is not set. Fixed to 3'b0
0	0x1	RO	**VALID (VALID)** Hardwired to '1' to indicate that the function has implemented a DevIdle register as specified in the DevIdle that can be located using the DEVIDLELOC register and BARNUM.

DevIdle Power on Latency (CNVI_WIFI_DEV_IDLE_PWR) – Offset 174

Bit Range	Default	Access	Field Name and Description
30:13	-	-	**Reserved**
12:10	0x2	RO	**POLS (POLS)** Power On Latency Scale. Latency Scale multiplier: 010: 1us 011: 32us All other settings are reserved. The value of this register is multiplied with the Power On Latency Value (POLV) to provide the DevIdle power on exit latency multiplier scale from 1us to 32ms.

Bit Range	Default	Access	Field Name and Description
9:0	0x0	RO	**POLV (POLV)** Power On Latency Value. 10-bit value that is multiplied by the Power On Latency Scale. A value of 0 indicates a power on latency of less than 1us.

DCI PCR Registers

These registers are within the PCH Private Configuration Space which is accessiblethrough the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID+ Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4h	4	DCI Control (ECTRL)	60h

DCI Control (ECTRL) – Offset 4

ExI Control Register

Bit Range	Default	Access	Field Name and Description
30:7	-	-	**Reserved**
6	1h	RW	**USB3 DBC Enable Indication (USB3DBCEN)** This bit is used in conjunction with bit 5. Below are the encodings of bits [6:5]: 00 = DCI OOB / XDP enabled 01 = USB2 / DCI OOB + DbC enabled 10 = USB3 DbC enabled 11 = Reserved (Default)Note: BIOS needs to change the values of bits [6:5] from default value so that they are not simultaneously set to 1.

Bit Range	Default	Access	Field Name and Description
5	1h	RW	**USB2 DBC enable indication (USB2DBCEN)** This bit is used in conjunction with bit 6. See bit 6 for details.
4	0h	RW/L	**Host DCI Enable (HEEN)** 0 = Disable DCI 1 = Enable DCI This bit resides in the RTC well and is only reset by RTCRST#. Read or write to this bit is qualified by DCI Lock bit. When DCI Lock bit is 0, this bit is RW. When DCI Lock bit is 1, this bit can only be cleared by writing a 0 to it; write 1 has no effect.
3:1	-	-	**Reserved**
0	0h	RW/1L	**DCI Lock (HOST_EXI_EN_LOCK)** When set, the Host DCI Enable bit is locked.

EMMC Additional Registers

These registers are memory mapped based on BAR0 defined in PCI configuration space.

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
804h	2	Software LTR Value (SW_LTR_val)	800h
808h	2	Auto LTR Value (Auto_LTR_val)	800h
810h	4	Capabilities Bypass (Cap_byps)	0h
814h	4	Capabilities Bypass 1 (Cap_byps_reg1)	3040EF3Ch
818h	4	Capabilities Bypass Register II (Cap_byps_reg2)	40040C8h
81ch	4	Device Idle D0i3 (reg_D0i3)	8h
820h	4	Tx CMD Delay Control (Tx_CMD_dly)	400h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
824h	4	Tx Delay Control 1 (Tx_DATA_dly_1)	A18h
828h	4	Tx Delay Control 2 (Tx_DATA_dly_2)	1C1C1C00h
82ch	4	Rx CMD Data Delay Control 1 (Rx_CMD_Data_dly_1)	1C1C1C00h
830h	4	Rx Strobe Delay Control (Rx_Strobe_Ctrl_Path)	500h
834h	4	Rx CMD Data Path Delay Control 2 (Rx_CMD_Data_dly_2)	181Ch
838h	4	Master DLL Software Control (Master_Dll)	1h
840h	4	Auto Tuning Value (Auto_tuning)	0h

Software LTR Value (SW_LTR_val) – Offset 804

Bit Range	Default	Access	Field Name and Description
15	0h	RW	**(Snoop_Requirment)** Snoop_Requirment
14:13	-	-	**Reserved**
12:10	2h	RW	**Snoop Latency Scale (Snoop_latency_scale)** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -) 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	000h	RW	**Snoop Value (Snoop_value)** 10-bit latency value

Auto LTR Value (Auto_LTR_val) – Offset 808

Bit Range	Default	Access	Field Name and Description
15	0h	RW	**Snoop Requirment (Snoop_Requirment)** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	-	-	**Reserved**
12:10	2h	RW	**Snoop Latency Scale (Snoop_latency_scale)** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -) 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	000h	RW	**Snoop Value (Snoop_value)** 10-bit latency value

Capabilities Bypass (Cap_byps) – Offset 810

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	00h	RW	**Enable Capabilities Bypass (Enable_Cap_Bypass)** 5Ah: Enable Capabilities Bypass Others: Capabilities Bypass disabled (using default values)

Capabilities Bypass 1 (Cap_byps_reg1) – Offset 814

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
29	1h	RW	**(hs400_support)** 1 – HS400 Mode Supported 0 – HS400 Mode NOT Supported
28	1h	RW	**Timeout Clock Unit (timeout_clock_unit)** 1 - to Select MHz Clock 0 - to Select KHz Clock
27:22	01h	RW	**Timeout Clock Frequency (timeout_clock_freq)**
21	0h	RW	**SPI Mode Support (SPI_mode_support)** 1: SPI Mode Supported 0: SPI Mode Not Supported
20:17	0h	RW	**Timer Count for Re-Tuning (timer_count)** This is the Timer Count for Re-Tuning Timer for Re-Tuning Mode 1 to 3. Setting to 0h disables Re-Tuning Timer.
16	0h	RW	**Use Tuning for SDR50 (tuning_for_SDR50)** 1 = Use Tuning0 = Don't use Tuning
15	1h	RW	**DDR50 Support (ddr50_support)** 1'b1 – DDR50 Mode Supported 1'b0 – DDR50 Mode NOT Supported
14	1h	RW	**SDR104 Support (sdr104_support)** 1'b1 – SDR104 Mode Supported 1'b0 – SDR104 Mode NOT Supported
13	1h	RW	**SDR50 Support (sdr50_support)** 1'b1 – SDR50 Mode Supported 1'b0 – SDR50 Mode NOT Supported

Bit Range	Default	Access	Field Name and Description
12:11	1h	RW	**Slot Type (Slot_Type)** 00 - Removable Card Slot 01 - Embedded Slot for One Device 10 - Shared Bus Slot 11 - Reserved
10	1h	RW	**Asynchronous Interrupt Support (Asynchronus_Interrupt_Support)** 1'b1 – Asynchronous Interrupt Supported 1'b0 – Asynchronous Interrupt NOT Supported
9	1h	RW	**64 Bit System Address Support (Sys_Addr_64bit_Support)** 1 - Core supports 64-bit System Address Bus 0 - Core supports only 32-bit System Address Bus
8	1h	RW	**Voltage Support 1.8V (Voltage_Support_1_8V)** 1'b1 – 1.8V Supported 1'b0 – 1.8V NOT Supported
7	0h	RW	**Voltage Support 3.0V (Voltage_Support_3V)** 1'b1 – 3.0V Supported 1'b0 – 3.0V NOT Supported
6	0h	RW	**Voltage Support 3.3V (Voltage_Support_3_3V)** 1'b1 – 3.3V Supported 1'b0 – 3.3V NOT Supported
5	1h	RW	**Suspend / Resume Support (Suspend_Resume_Support)** 1'b1 – Suspend/Resume Supported 1'b0 – Suspend/Resume NOT Supported

Bit Range	Default	Access	Field Name and Description
4	1h	RW	**SDMA Support (SDMA_Support)** 1'b1 – SDMA Mode Supported 1'b0 – SDMA Mode NOT Supported
3	1h	RW	**High Speed Support (High_Speed_Support)** 1'b1 – High Speed Mode Supported 1'b0 – High Speed Mode NOT Supported
2	1h	RW	**ADMA2 Support (ADMA2_Support)** 1'b1 – ADMA2 Mode Supported 1'b0 – ADAM2 Mode NOT Supported
1:0	0h	RW	**Max Burst Length (Max_Burst_Length)** Maximum Block Length supported by the Core/Device 00: 512 (Bytes) 01: 1024 10: 2048 11: Reserved

Capabilities Bypass Register II (Cap_byps_reg2) – Offset 818

Bit Range	Default	Access	Field Name and Description
30:27	-	-	**Reserved**
26:21	20h	RW	**Tuning Count Value (tuning_count_val)** Configures the Number of Taps (Phases) of the rxclk_in that is supported. The Tuning State machine uses this information toselect one of the Taps (Phases) of the rxclk_in during the Tuning Procedure

Bit Range	Default	Access	Field Name and Description
20	0h	RW	**Tuning Disable (tuning_dis)** Disable the 1.5x Tuning count when calculatingtotal tuning count.
19	0h	RW	**Driver Type 4 Support (driver_type_4)** 1: Supported 0: NOT Supported
18	0h	RW	**Driver Type D Support (driver_type_D)** 1: Supported 0: NOT Supported
17	0h	RW	**Driver Type C Support (driver_type_C)** 1: Supported 0: NOT Supported
16	0h	RW	**Driver Type A Support (driver_type_A)** 1: Supported 0: NOT Supported
15	-	-	**Reserved**
14	1h	RW	**8-bit Support for Embedded Device (support_8_bit_embedded)** 1: Supported 0: NOT Supported
13:8	-	-	**Reserved**
7:0	C8h	RW	**Base Clock Frequency (base_sd_clock)**

Device Idle D0i3 (reg_D0i3) – Offset 81c

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4	0h	RO	**Interrupt Request Capable (Interrupt_Request_Capable)** 0 – HW not capable to issue in interrupt on command completion 1 – HW capable to issue an interrupt on command completion
3	1h	RW/1C	**Restore Required (RestoreRequired)** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h	RW	**D0i3 (D0i3)** SW sets this bit to 1 to move the IP into the D0i3 state. Writing this bit to 0 will return the IP to the fully active D0 state (D0i0).
1	-	-	**Reserved**
0	0h	RO	**Command In Progress (Cmd_In_Progress)** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit. If Interrupt Request bit [1] was set for the current command, HW may clear this bit before the interrupt has been made visible to SW.

Tx CMD Delay Control (Tx_CMD_dly) – Offset 820

Bit Range	Default	Access	Field Name and Description
30:15	-	-	**Reserved**
14:8	04h	RW	**Tx CMD Delay (DDR Mode) (ddr_mode)** Tx CMD Delay (DDR Mode). 0 - 39: Select number of active delay elements. Each = 125pSec. 40 - 127: Reserved

Bit Range	Default	Access	Field Name and Description
7	-	-	**Reserved**
6:0	00h	RW	**Tx CMD Delay (SDR Mode) (sdr_mode)** Tx CMD Delay (SDR Mode). 0 - 39: Select number of active delay elements. Each = 125pSec. 40 - 127 - Reserved

Tx Delay Control 1 (Tx_DATA_dly_1) – Offset 824

Bit Range	Default	Access	Field Name and Description
30:15	-	-	**Reserved**
14:8	0Ah	RW	**Tx Data Delay (HS400 Mode) (hs400_mode)** Tx Data Delay (HS400 Mode). 0 - 78: Select number of active delay elements. Each = 125pSec. 79 - 127: Reserved
7	-	-	**Reserved**
6:0	18h	RW	**Tx Data Delay (SDR104/HS200 Mode) (sdr104_hs200_mode)** 0-79 - Select the required delay, as a multiple of 125pSec. 80 – 127 – Reserved

Tx Delay Control 2 (Tx_DATA_dly_2) – Offset 828

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30:24	1Ch	RW	**Tx Data Delay (SDR50 Mode) (sdr50_mode)** 0 - 79: Select the required delay, as a multiple of 125pSec. 80 - 127: Reserved
23	-	-	**Reserved**
22:16	1Ch	RW	**Tx Data Delay (DDR50 Mode) (ddr50_mode)** 0 - 78: Select number of active delay elements. Each = 125pSec. 79 - 127: Reserved
15	-	-	**Reserved**
14:8	1Ch	RW	**Tx Data Delay (SDR25/HS50 Mode) (sdr25_hs50_mode)** 0 - 79: Select the required delay, as a multiple of 125pSec. 80 - 127: Reserved
7	-	-	**Reserved**
6:0	00h	RW	**Tx Data Delay (SDR12/Compatibility Mode) (sdr12_comp_mode)** 0 - 79: Select the required delay, as a multiple of 125pSec. 80 - 127: Reserved

Rx CMD Data Delay Control 1 (Rx_CMD_Data_dly_1) – Offset 82c

Bit Range	Default	Access	Field Name and Description
30:24	1Ch	RW	**Rx CMD + Data Delay (SDR50 Mode) (sdr50_mode)** 0-119 - Select the required delay, as a multiple of 125pSec. 120 – 127 – Reserved

Bit Range	Default	Access	Field Name and Description
23	-	-	**Reserved**
22:16	1Ch	RW	**Rx CMD + Data Delay (DDR50 Mode) (ddr50_mode)** 0-78: Select number of active delay elements. Each = 125 pSec. 79-127: Reserved
15	-	-	**Reserved**
14:8	1Ch	RW	**Rx CMD + Data Delay (SDR25/HS50 Mode) (sdr25_hs50_mode)** 0-119 - Select the required delay, as a multiple of 125pSec. 120 – 127 – Reserved
7	-	-	**Reserved**
6:0	00h	RW	**Rx CMD + Data Delay (SDR12/Compatibility Mode) (sdr12_comp_mode)** 0-119 - Select the required delay, as a multiple of 125pSec. 120 – 127 – Reserved

Rx Strobe Delay Control (Rx_Strobe_Ctrl_Path) – Offset 830

Bit Range	Default	Access	Field Name and Description
30:17	-	-	**Reserved**
16	0h	RW	**Auto Tuning (auto_tuning)** Enable Auto Tuning for HS400 Strobe Path. 0: Auto Tuning Disabled 1: Auto Tuning Enabled
15	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
14:8	05h	RW	**Rx Strobe Delay DLL 1(HS400 Mode) (hs400_mode1)** 0-39: Select number of active delay elements. Each = 125 pSec. 0-63: Reserved
7	-	-	**Reserved**
6:0	00h	RW	**Rx Strobe Delay DLL 2(HS400 Mode) (hs400_mode2)** 0-39: Select number of active delay elements. Each = 125 pSec. 40-63: Reserved

Rx CMD Data Path Delay Control 2 (Rx_CMD_Data_dly_2) – Offset 834

Bit Range	Default	Access	Field Name and Description
30:18	-	-	**Reserved**
17:16	0h	RW	**Clock Source (clk_source)** Clock Source for Rx Path. 00: Rx Clock after Output Buffer 01: Rx Clock before Output Buffer 10: Automatic Selection based on Working mode (HS 200 before buffer, all others after buffer) 11 - Reserved
15:14	-	-	**Reserved**
13:8	18h	RW	**Rx Path PLL (path_pll)** Rx Path PLL #3 Delay value For Auto Tuning Mode. 0-39: Select the required delay, as a multiple of 125 pSec. 40-63: Reserved

Bit Range	Default	Access	Field Name and Description
7	-	-	**Reserved**
6:0	1Ch	RW	**Rx CMD + Data Delay (SDR104/HS200 Mode) (cmd_data_sdr104_hs200)** 0-79: Select the required delay, as a multiple of 125 pSec. 80-127: Reserved

Master DLL Software Control (Master_Dll) – Offset 838

Bit Range	Default	Access	Field Name and Description
30:25	-	-	**Reserved**
24	0h	RW	**SW reset for Master DLL (SW_reset_dll)** 0: No SW Reset for Master DLL 1: Force Reset for Master DLL
23	0h	RO/V	**Master DLL Lock Indication (DLL_lock)**
22:2	-	-	**Reserved**
1	0h	RW	**Master DLL Software Control (Master_DLL_Software_Ctrl)** 0: Master DLL Automatic Control (SW Control Disabled). 1: Master DLL Software Control Enabled
0	1h	RW	**Control of Master DLL Ref Clock (Ctrl_of_Mst_DLL_Ref_Clk)** 0: Clock is Disabled. 1: Clock is Enabled

Auto Tuning Value (Auto_tuning) – Offset 840

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4:0	00h	RO/V	**Auto Tuning Value (auto_tuning_val)** Auto Tuning Value found by host controller.

EMMC Memory Mapped Registers

These registers are memory mapped based on BAR0 defined in PCI configuration space.

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	SDMA System Address (sdmasysaddr)	0h
4h	2	Block Size (blocksize)	0h
6h	2	Block Count Register (blockcount)	0h
8h	4	Argument 1 (argument1)	0h
ch	2	Transfer Mode Register (transfermode)	0h
eh	2	Command (command)	0h
10h	4	Response (Response 0 And 1)	0h
14h	2	Response 2 (response2)	0h
16h	2	Response 3 (response3)	0h
18h	2	Response 4 (response4)	0h
1ah	2	Response 5 (response5)	0h
1ch	2	Response 6 (response6)	0h
1eh	2	Response 6 (response7)	0h
20h	4	Buffer Data Port Register (dataport)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
24h	4	Present State (PRESENTSTATE)	1FF00000h
28h	1	Host Control 1 (hostcontrol1)	0h
29h	1	Power Control Register (powercontrol)	0h
2ah	1	Block Gap Control Register (blockgapcontrol)	80h
2bh	1	Wakeup Control (wakeupcontrol)	0h
2ch	2	Clock Control (clockcontrol)	0h
2eh	1	Timeout Control (timeoutcontrol)	0h
2fh	1	Software Reset (softwarereset)	0h
30h	2	Normal Interrupt Status (normalintrsts)	0h
32h	2	Error Interrupt Status (errorintrsts)	0h
34h	2	Normal Interrupt Status Enable (normalintrstsena)	0h
36h	2	Error Interrupt Status Enable (errorintrstsena)	0h
38h	2	Normal Interrupt Signal Enable (normalintrsigena)	0h
3ah	2	Error Interrupt Signal Enable (errorintrsigena)	0h
3ch	2	Auto CMD12 Error Status (autocmderrsts)	0h
3eh	2	Host Control 2 (hostcontrol2)	0h
40h	8	Capabilities (capabilities)	74462C881h
48h	8	Maximum Current Capabilities (maxcurrentcap)	0h
50h	2	Force Event for AUTO CMD Error Status (ForceEventforAUTOCMDErrorStatus)	0h
52h	2	Force Event Register for Error Interrupt Status (forceeventforerrintsts)	0h
54h	1	ADMA Error Status (admaerrsts)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
58h	4	ADMA System Address Register 1 (admasysaddr01)	0h
5ch	2	ADMA System Address Register2 (admasysaddr2)	0h
60h	2	Preset Value for Initialization (presetvalue0)	4h
62h	2	Preset Value for Default Speed (presetvalue1)	0h
64h	2	Preset Value for High Speed (presetvalue2)	0h
66h	2	Preset Value for SDR12 (presetvalue3)	0h
68h	2	Preset Value for SDR25 (presetvalue4)	0h
6ah	2	Preset Value for SDR50 (presetvalue5)	0h
6ch	2	Preset Value for SDR104 (presetvalue6)	0h
6eh	2	Preset Value for DDR50 (presetvalue7)	0h
70h	4	Boot Timeout Control (boottimeoutcnt)	0h
fch	2	Slot Interrupt Status (slotintrsts)	0h

SDMA System Address (sdmasysaddr) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**SDMA System Address Register/Argument2 Register (sdma_sysaddress)** This register contains the physical system memory address used for DMA transfers or the second argument for the Auto CMD23. 1) SDMA System Address: This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. 2) Argument 2: This register is used with the Auto CMD23 to set a 32-bit block count value to the argument of the CMD23 while executing Auto CMD23.

Block Size (blocksize) – Offset 4

Bit Range	Default	Access	Field Name and Description
14:12	0h	RW	**Host DMA Buffer Size (host_sdma_buf_size)** To perform long DMA transfer, System Address register shall be updated at every system boundary during DMA transfer. These bits specify the size of contiguous buffer in the system memory. The DMA transfer shall wait at the every boundary specified by these fields and the HC generates the DMA Interrupt to request the HD to update the System Address register.These bits shall support when the DMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. 000b - 4KB(Detects A11 Carry out) 001b - 8KB(Detects A12 Carry out) 010b - 16KB(Detects A13 Carry out) 011b - 32KB(Detects A14 Carry out) 100b - 64KB(Detects A15 Carry out) 101b -128KB(Detects A16 Carry out) 110b - 256KB(Detects A17 Carry out) 111b - 512KB(Detects A18 Carry out)

Bit Range	Default	Access	Field Name and Description
11:0	000h	RW	**Transfer Block Size (xfer_blocksize)** This register specifies the block size for block datatransfers for CMD17, CMD18, CMD24, CMD25, andCMD53. It can be accessed only if no transaction isexecuting. Readoperations during transfer return an invalid value andwrite operations shall be ignored. 0000h - No Data Transfer 0001h - 1 Byte 0002h - 2 Bytes 0003h - 3 Bytes 0004h - 4 Bytes 01FFh - 511 Bytes 0200h - 512 Bytes 0800h - 2048 Bytes

Block Count Register (blockcount) – Offset 6

This register is enabled when Block Count Enable in theTransfer Mode register is set to 1 and is valid only formultiple block transfers. The HC decrements the blockcount after each block transfer and stops when the countreaches zero.

0000h - Stop Count

0001h - 1 block

0002h - 2 blocks

FFFFh - 65535 blocks.

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW	**Block Count (block_cnt_16bit)**

Argument 1 (argument1) – Offset 8

The SD/eMMC Command Argument is specified as bit39-8 of Command-Format.

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Command Argument 1 (command_argument1)** The Command Argument is specified as bit [39:8] of Command-Format

Transfer Mode Register (transfermode) – Offset c

Bit Range	Default	Access	Field Name and Description
14:6	-	-	**Reserved**
5	0h	RW	**Multi / Single Block Select (xfermode_multiblksel)** This bit enables multiple block data transfers. 0 - Single Block 1 - Multiple Block.
4	0h	RW	**Data Transfer Direction Select (xfermode_dataxferdir)** This bit defines the direction of data transfers. 0 - Write (Host to Card) 1 - Read (Card to Host)
3:2	0h	RW	**Auto CMD Enable (xfermode_autocmdena)** This field determines use of auto command functions 00b - Auto Command Disabled 01b - Auto CMD12 Enable 10b - Auto CMD23 Enable.
1	0h	RW	**Block Count Enable (xfermode_blkcntena)** This bit is used to enable the Block count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is usefulin executing an infinite transfer. 0 - Disable 1 - Enable.

Bit Range	Default	Access	Field Name and Description
0	0h	RW	**DMA Enable (xfermode_dmaenable)** If this bit is set to 1, a DMA operation shall begin when the HD writes to the upper byte of Command register (00Fh). 0 - Disable 1 - Enable.

Command (command) – Offset e

Bit Range	Default	Access	Field Name and Description
14	-	-	**Reserved**
13:8	00h	RW	**Command Index (command_cmdindex)** This bit shall be set to the command number (CMD0-63,ACMD0-63).
7:6	0h	RW	**Command Type (command_cmdtype)** There are three types of special commands. Suspend, Resume and Abort. These bits shall be set to 00b for all other commands. 00b - Normal 01b - Suspend 10b - Resume 11b - Abort

Bit Range	Default	Access	Field Name and Description
5	0h	RW	**Data Present Select (command_datapresent)** This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. If is set to 0 for the following: 1. Commands using only CMD line(ex. CMD52) 2. Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b ex. CMD38) 3. Resume Command 0 - No Data Present 1 - Data Present
4	0h	RW	**Command Index Check Enable (command_indexchkena)** If this bit is set to 1, the HC shall check the index field in the response to see if it has the same value as the command index.
3	0h	RW	**Command CRC Check Enable (command_crcchkena)** If this bit is set to 1, the HC shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. 0 - Disable 1 – Enable
2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1:0	0h	RW	**Response Type Select (command_responsetype)** 00 - No Response 01 - Response length 136 10 - Response length 48 11 - Response length 48 checkBusy after response

Response (Response 0 And 1) – Offset 10

The response registers contains the 128 bit response received from the External Device.

There are 8 response registers:

Response 0: offset 10h

Response 1: offset 12h

Response 2: offset 14h

Response 3: offset 16h

Response 4: offset 18h

Response 5: offset 1Ah

Response 6: offset 1Ch

Response 7: offset 1Eh

Register details:

Response Register 0 and 1 = Response [31:0]

Response Register 2 and 3 = Response [63:32]

Response Register 4 and 5 = Response [95:64]

Response Register 6 and 7 = Response [127:96]

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO	**Command Response 31_0 (command_response_31_0)** Response bits [31:0]

Response 2 (response2) – Offset 14

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RO	**Command Response 47_32 (command_response_47_32)** Response bits [47:32]

Response 3 (response3) – Offset 16

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RO	**command Response 63_48 (command_response_63_48)** Response bits [63:48]

Response 4 (response4) – Offset 18

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RO	**Command Response 79_64 (command_response_79_64)** Response bits [79:64]

Response 5 (response5) – Offset 1a

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RO	**Command Response 95_80 (command_response_95_80)** Response bits [95:80]

Response 6 (response6) – Offset 1c

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RO	**Command Response 111_96 (command_response_111_96)** Response bits [111:96]

Response 6 (response7) – Offset 1e

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RO	**Command Response 127_112 (command_response_127_112)** Response bits [127:112]

Buffer Data Port Register (dataport) – Offset 20

The Host Controller Buffer can be accessed through this32-bit Data Port Register.

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Data Port (sdhcdmactrl_piobufrddata)** The Host Controller Buffer can be accessed through this 32-bit Data Port Register.

Present State (PRESENTSTATE) – Offset 24

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**
28:25	fh	RO	**DAT4 Line Signal Level (sdif_dat4in_dsync)** sdif_dat4in_dsync
24	1h	RO	**CMD Line Signal Level (sdif_cmdin_dsync)** This status is used to check CMD line level to recoverfrom errors, and for debugging

Bit Range	Default	Access	Field Name and Description
23:20	fh	RO	**DAT0 Line Signal Level (sdif_dat0in_dsync)** This status is used to check DAT line level to recover from errors, and for debugging.
19	0h	RO	**Write Protect Switch Pin Level (sdif_wp_dsync)** The Write Protect Switch is supported for memory andcombo cards. This bit reflects the SDWP# pin.0 - Write protected (SDWP# = 0) 1 - Write enabled (SDWP# = 1).
18	0h	RO	**Card Level Detect (sdif_cd_n_dsync)** This bit reflects the inverse value of the SDCD# pin. 0 - No Card present (SDCD# = 1) 1 - Card present (SDCD# = 0).
17	0h	RO	**Card State Stable (sdhccarddet_statestable_dsync)** This bit is used for testing. If it is 0, the Card Detect PinLevel is not stable. If this bit is set to 1, it means theCard Detect Pin Level is stable. The Software Reset ForAll in the Software Reset Register shall not affect this bit. 0 - Reset of Debouncing 1 - No Card or Inserted.
16	0h	RO	**Card Inserted (sdhccarddet_inserted_dsync)** This bit indicates whether a card has been inserted.Changing from 0 to 1 generates a Card InsertionInterrupt in the Normal Interrupt Status register andchanging from 1 to 0 generates a Card RemovalInterrupt in the Normal Interrupt Status register.
15:12	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
11	0h	RO	**Buffer Read Enable (sdhcdmactrl_piobufrdena)** This status is used for non-DMA read transfers. This read only flag indicates that valid data exists in the host side buffer status. If this bit is 1, readable dataexists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when all the block data is ready in the buffer and generates the Buffer Read Ready Interrupt. 0 - Read Disable 1 - Read Enable
10	0h	RO	**Buffer Write Enable (sdhcdmactrl_piobufwrena)** This status is used for non-DMA write transfers. This read only flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer. A change of this bit from 1 to 0 occurs when all the block data is written to the buffer.
9	0h	RO	**Read Transfer Active (sdhcdmactrl_rdxferactive)** This status is used for detecting completion of a read transfer.This bit is set to 1 for either of the following conditions: • After the end bit of the read command • When writing a 1 to continue Request in the Block Gap Control register to restart a read transfer. This bit is cleared to 0 for either of the following conditions: • When the last data block as specified by block length is transferred to the system. • When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the Stop At Block Gap Request set to 1. A transfer complete interrupt is generated when this bit changes to 0. 1 - Transferring data 0 - No valid data

Bit Range	Default	Access	Field Name and Description
8	0h	RO	**Write Transfer Active (sdhcdmactrl_wrxferactive)** This status indicates a write transfer is active. If this bit is 0, it means no valid write data exists in the HC. This bit is set in either of the following cases: • After the end bit of the write command. • When writing a 1 to Continue Request in the Block Gap Control register to restart a write transfer. This bit is cleared in either of the following cases: • After getting the CRC status of the last datablock as specified by the transfer count (Single or Multiple) • After getting a CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0, as a result of the Stop At Block Gap Request being set. This status is useful for the HD in determining when to issue commands during write busy. 1 - transferring data 0 - No valid data
7:4	-	-	**Reserved**
3	0h	RO	**Re-Tuning Request (Re-Tune)** Host Controller may request Host Driver to execute re-tuning sequence by setting this bit when the datawindow is shifted by temperature drift and any issue receiving the correct data. This bit is cleared when a command is issued withsetting Execute Tuning in the Host Control 2 register.Changing of this bit from 0 to 1 generates Re-TuningEvent. This bit is cleared when a command is issued with setting Execute Tuning in the Host Control 2 register.Changing of this bit from 0 to 1 generates Re-Tuning Event. Refer to Normal Interrupt registers for more detail. This bit isn't set to 1 if Sampling Clock Select in the Host Control 2 register is set to 0 (using fixed sampling clock). 1: Sampling clock needs re-tuning 0: Fixed or well tuned sampling clock

Bit Range	Default	Access	Field Name and Description
2	0h	RO	**DATA line Active (Data Activity)** This bit indicates whether one of the DAT line on SD busis in use.1 - DAT line active0 - DAT line inactive
1	0h	RO	**Command Inhibit (DAT) (presentstate_inhibitdat)** This status bit is generated if either the DAT Line Activeor the Read transfer Active is set to 1. If this bit is 0, it indicates the HC can issue the next SD command.Commands with busy signal belong to Command Inhibit(DAT). Changing from 1 to 0 generates a Transfer Completeinterrupt in the Normal interrupt status register.
0	0h	RO	**Command Inhibit (CMD) (presentstate_inhibitcmd)** If this bit is 0, it indicates the CMD line is not in use andthe HC can issue a SD command using the CMD line.This bit is set immediately after the Command register(00Fh) is written. This bit is cleared when the commandresponse is received. Even if the Command Inhibit (DAT) is set to 1, Commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 generates a Command complete interrupt in the Normal Interrupt Status register. If the HC cannot issue the command because of a command conflict error or because of Command Not Issued By Auto CMD12 Error, this bit shall remain 1 and the Command Complete is not set. Status issuing AutoCMD12 is not read from this bit. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 operation, Host Controller shall manage to issue two commands: CMD12 and a command set by Command register.

Host Control 1 (hostcontrol1) – Offset 28

Bit Range	Default	Access	Field Name and Description
7	0h	RW	**Card Detect Signal Detection (hostctrl1_cdsigselect)** This bit selects source for card detection. 1- The card detect test level is selected 0- SDCD# is selected (for normal use).

Bit Range	Default	Access	Field Name and Description
6	0h	RW	**Card Detect Test Level (hostctrl1_cdtestlevel)** This bit is enabled while the Card Detect SignalSelection is set to 1 and it indicates card inserted or not. Generates (card ins or card removal) interrupt when the normal int sts enable bit is set. 1 - Card Inserted 0 - No Card.
5	0h	RW	**Extended Data Transfer Width (hostctrl1_extdatawidth)** This bit controls 8-bit bus width mode for embeddeddevice. Support of this function is indicated in 8-bit Support for Embedded Device in the Capabilitiesregister. If a device supports 8-bit bus mode, this bit may be set to 1. If this bit is 0, bus width is controlled by Data Transfer Width in the Host Control 1 register.
4:3	0h	RW	**DMA Select (hostctrl1_dmaselect)** One of supported DMA modes can be selected. The hostdriver shall check support of DMA modes by referringthe Capabilities register. 00 - SDMA is selected 01 - 32-bit Address ADMA1 is selected 10 - 32-bit Address ADMA2 is selected 11 - 64-bit Address ADMA2 is selected.
2	0h	RW	**High Speed Enable (hostctrl1_highspeedena)** This bit is optional. Before setting this bit, the HD shall check the High Speed Support in the capabilitiesregister. If this bit is set to 0 (default), the HC outputs CMD line and DAT lines at the falling edge of the SD clock (up to 25 MHz/ 20MHz for MMC). If this bit is set to 1, the HC outputs CMD line and DAT lines at the rising edge of the SD clock (up to 50 MHz for SD/52MHz for MMC)/ 208Mhz.

Bit Range	Default	Access	Field Name and Description
1	0h	RW	**Data Transfer Width (hostctrl1_datawidth)** This bit selects the data width of the HC. The HD shallselect it to match the data width of the SD card. 1 - 4 bit mode 0 - 1 bit mode.
0	0h	RW	**LED Control (hostctrl1_ledcontrol)** This bit is used to caution the user not to remove thecard while the SD card is being accessed. If the software is going to issue multiple SD commands, this bit can be set during all transactions. It is not necessary to changefor each transaction. 1 - LED on 0 - LED off.

Power Control Register (powercontrol) – Offset 29

This register is used to program the Bus power and voltage level

Bit Range	Default	Access	Field Name and Description
6:5	-	-	**Reserved**
4	0h	RW	**eMMC HW Reset (emmc_hwreset)** Hardware reset signal is generated for eMMC card whenthis bit is set 1 - Drives the hardware reset pin as ZERO(Active LOW to eMMC card) 0 - Deassert the hardware reset pin.
3:1	0h	RW	**SD Bus Voltage Select (pwrctrl_sdbusvoltage)** By setting these bits, the HC selects the voltage level for the SD card. Before setting this register, the HC shall check the voltage support bits in the capabilities register. If unsupported voltage is selected, the Host System shall not supply SD bus voltage 111b - 3.3 V 110b - 3.0 V 101b - 1.8 V.

Bit Range	Default	Access	Field Name and Description
0	0h	RW	**Bus Power (pwrctrl_sdbuspower)** Before setting this bit, the SD host driver shall set SDBus Voltage Select. If the HC detects the No Card State,this bit shall be cleared. 1 - Power on 0 - Power off.

Block Gap Control Register (blockgapcontrol) – Offset 2a

This register is used to program the block gap request, read wait control and interrupt at blockgap.

Bit Range	Default	Access	Field Name and Description
7	1h	RW	**Boot Acknowledge Check (boot_ack_chk)** To check for the boot acknowledge in boot operation. 1 - wait for boot ack from eMMC card 0 - Will not wait for boot ack from eMMC card.
6	0h	RW	**Alternate Boot Enable (alt_boot_en)** To start boot code access in alternative mode. 1- To start alternate boot mode access 0 - To stop alternate boot mode access.
5	0h	RW	**Boot Code Access (BOOT_EN)** To start boot code access 1- To start boot code access 0 - To stop boot code access
4	0h	RW	**SPI mode enable (spi_mode)** SPI mode enable bit. 1- SPI mode 0 - SD mode

Bit Range	Default	Access	Field Name and Description
3	-	-	**Reserved**
2	0h	RW	**Read Wait Control (rd_wait_ctrl)** The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using DAT[2] line. Otherwise the HC has to stop the SD clock to hold read data, which restricts commands generation. When the HD detects a card insertion, it shall set this bit according to the CCCR of the card. If the card does not support read wait, this bit shall never be set to 1 otherwise DAT line conflict may occur. If this bit is set to 0, Suspend / Resume cannot be supported 1 - Enable Read Wait Control 0 - Disable Read Wait Control
1	0h	RW	**Continue Request (continue_req)** This bit is used to restart a transaction which wasstopped using the Stop At Block Gap Request. To cancelstop at the block gap, set Stop At block Gap Request to0 and set this bit to restart the transfer. The HC automatically clears this bit in either of thefollowing cases: 1) In the case of a read transaction, the DAT Line Active changes from 0 to 1 as a read transaction restarts. 2) In the case of a write transaction, the Write transfer active changes from 0 to 1 as the write transaction restarts.
0	0h	RW	**Stop At Block Gap Request (stopatblkgap_req)** This bit is used to stop executing a transaction at thenext block gap for non-DMA,SDMA and ADMA transfers.Until the transfer complete is set to 1, indicating atransfer completion the HD shall leave this bit set to 1. Clearing both the Stop At Block Gap Request andContinue Request shall not cause the transaction torestart.

Wakeup Control (wakeupcontrol) – Offset 2b

This register is used to program the wakeup functionality.

Bit Range	Default	Access	Field Name and Description
6:3	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
2	0h	RW	**Wakeup Event On SD Card Removal (wkupctrl_cardremoval)** This bit enables wakeup event via Card Removalassertion in the Normal Interrupt Status register.FN_WUS (Wake up Support) in CIS does not affect thisbit. 1 - Enable 0 – Disable.
1	0h	RW	**Wakeup On Card Insertion (wkupctrl_cardinsertion)** This bit enables wakeup event via Card Insertionassertion in the Normal Interrupt Status register.FN_WUS (Wake up Support) in CIS does not affect thisbit. 1 - Enable 0 – Disable
0	0h	RW	**Wakeup Event Enable On Card Interrupt (wkupctrl_cardinterrupt)** This bit enables wakeup event via Card Interruptassertion in the Normal Interrupt Status register.This bit can be set to 1 if FN_WUS (Wake Up Support) inCIS is set to 1. 1 - Enable 0 - Disable.

Clock Control (clockcontrol) – Offset 2c

This register is used to program the Clock frequency select, generator select, Clock enable,Internal Clock state fields.

Bit Range	Default	Access	Field Name and Description
15:8	00h	RW	**SDCLK Frequency Select (clkctrl_sdclkfreqsel)** This register is used to select the frequency of the clock pin. The frequency is not programmed directly; rather this register holds the divisor of the Base Clock Frequency in the capabilities register. Only the following settings are allowed. 1) 8-bit Divided Clock Mode 80h - base clock divided by 256 40h - base clock divided by 128 20h - base clock divided by 64 10h - base clock divided by 32

Bit Range	Default	Access	Field Name and Description
			08h - base clock divided by 16 04h - base clock divided by 8 02h - base clock divided by 4 01h - base clock divided by 2 00h - base clock(10MHz-63MHz) Setting 00h specifies the highest frequency of the SD Clock. When setting multiple bits, the most significant bit is used as the divisor. But multiple bits should not be set. The two default divider values can be calculated by the frequency that is defined by the Base Clock Frequency in the Capabilities register. a) 25 MHz divider value b) 400 KHz divider value The frequency of the clock is set by the following formula: Clock Frequency = (Baseclock) / divisor. Thus choose the smallest possible divisor which results in a clock frequency that is less than or equal to the target frequency. 2) 10-bit Divided Clock Mode Host Controller Version 3.00 supports this mandatory mode instead of the 8-bit Divided Clock Mode. The length of divider is extended to 10 bits and all divider values shall be supported. 3FFh --1/2046 Divided Clock N -------1/2N Divided Clock (Duty 50%) 002h -- 1/4 Divided Clock 001h ---1/2 Divided Clock 000h --- Base Clock (10MHz-254MHz)
7:6	0h	RW	**Upper Bits of SDCLK Frequency Select (clkctrl_sdclkfreqsel_upperbits)** Bit 07-06 is assigned to bit 09-08 of clock divider inSDCLK Frequency Select.

Bit Range	Default	Access	Field Name and Description
5	0h	RW	**Clock Generator Select (clkctrl_clkgensel)** This bit is used to select the clock generator mode inSDCLK Frequency Select.If the Programmable Clock Mode is supported (non-zerovalue is set to Clock Multiplier in the Capabilitiesregister), this bit attribute is RW, and if not supported,this bit attribute is RO and zero is read.This bit depends on the setting of Preset Value Enable in the Host Control 2 register. If the Preset Value Enable = 0, this bit is set by HostDriver. If the Preset Value Enable = 1, this bit is automatically set to a value specified in one of Preset Value registers. 1: Programmable Clock Mode 0: Divided Clock Mode.
4:3	-	-	**Reserved**
2	0h	RW	**SD Clock Enable (clkctrl_sdclkena)** The HC shall stop SDCLK when writing this bit to 0.SDCLK frequency Select can be changed when this bit is0.
1	0h	RO	**Internal Clock Stable (sdhcclkgen_intclkstable_dsync)** This bit is set to 1 when SD clock is stable after writingto Internal Clock Enable in this register to 1. The SDHost Driver shall wait to set SD Clock Enable until this bit is set to 1.
0	0h	RW	**Internal Clock Enable (clkctrl_intclkena)** This bit is set to 0 when the HD is not using the HC orthe HC awaits a wakeup event. The HC should stop itsinternal clock to go very low power state.1 - Oscillate 0 - Stop.

Timeout Control (timeoutcontrol) – Offset 2e

This value determines the interval by which DAT linetime-outs are detected.Refer to the Data Time-out Error in the Error InterruptStatus register for information on factors that dictatetime-out generation. Time-out clock frequency will

begenerated by dividing the sd clock TMCLK by this value.When setting this register, prevent inadvertenttime-out events by clearing the Data Time-out ErrorStatus Enable (in the Error Interrupt Status Enableregister)

1110 - TMCLK * 2^27

0001 - TMCLK * 2^14

0000 - TMCLK * 2^13.

Bit Range	Default	Access	Field Name and Description
6:4	-	-	**Reserved**
3:0	0h	RW	**Data Timeout Counter Value (timeout_ctrvalue)** This value determines the interval by which DAT line time-outs are detected. Refer to the Data Time-out Error in the Error Interrupt Status register for information on factors that dictate time-out generation. Time-out clock frequency will be generated by dividing the sd clock TMCLK by this value. When setting this register, prevent inadvertent time-out events by clearing the Data Time-out Error Status Enable (in the Error Interrupt Status Enable register) 1111 - Reserved 1110 - TMCLK * 2^27---------- ---------- 0001 - TMCLK * 2^14 0000 - TMCLK * 2^13

Software Reset (softwarereset) – Offset 2f

This register is used to program the software reset for data, command and for all.

Bit Range	Default	Access	Field Name and Description
6:3	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
2	0h	RW	**Software Reset for DAT Line (swreset_for_dat)** Only part of data circuit is reset. The followingregisters and bits are cleared by this bit: Buffer Data Port Register - Buffer is cleared and initialized. Present State register - Buffer read Enable - Buffer write Enable - Read Transfer Active - Write Transfer Active - DAT Line Active - Command Inhibit (DAT)Block Gap Control register - Continue Request - Stop At Block Gap Request Normal Interrupt Status register - Buffer Read Ready - Buffer Write Ready - Block Gap Event - Transfer Complete 1 - Reset 0 - Work.

Bit Range	Default	Access	Field Name and Description
1	0h	RW	**Software Reset for CMD Line (swreset_for_cmd)** Only part of command circuit is reset. The following registers and bits arecleared by this bit: Present State register - Command Inhibit (CMD) Normal Interrupt Status register - Command Complete 1 - Reset 0 - Work.
0	0h	RW	**Software Reset for All (swreset_for_all)** This reset affects the entire HC except for the carddetection circuit. Register bits of type ROC, RW, RW1C,RWAC are cleared to 0. During its initialization, the HD shall set this bit to 1 to reset the HC. The HC shall reset this bit to 0 when capabilities registers are valid and the HD can read them. Additional use of Software Reset ForAll may not affect the value of the Capabilities registers. If this bit is set to 1, the SD card shall reset itself and must be re initialized by the HD. 1 - Reset 0 - Work

Normal Interrupt Status (normalintrsts) – Offset 30

This register gives the status of all the interrupts

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
15	0h	RO	**Error Interrupt (reg_errorintrsts)** If any of the bits in the Error Interrupt Status Register are set, then this bit is set. Therefore the HD can test for an error by checking this bit first. 0 - No Error 1 – Error.
14	0h	RW1C	**Boot terminate Interrupt (normalintrsts_bootcomplete)** This status is set if the boot operation get terminated 0 - Boot operation is not terminated 1 - Boot operation is terminated.
13	0h	RW1C	**Boot Acknowledge Rcv (normalintrsts_rcvbootack)** This status is set if the boot acknowledge is receivedfrom device. 0 - Boot ack is not received 1 - Boot ack is received.
12	0h	RO	**Re-Tuning Event (normalintrsts_retuningevent)** This status is set if Re-Tuning Request in the PresentState register changes from 0 to 1. Host Controller requests Host Driver to perform re-tuning for next data transfer. Current data transfer(not large block count) can be completed without retuning. 1 Re-Tuning should be performed 0 Re-Tuning is not required.
11	0h	RO	**INT_C_ Status (normalintrsts_intc)** This status is set if INT_C is enabled and INT_C# pin isin low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_C interrupt factor.
10	0h	RO	**INT_B_Status (normalintrsts_intb)** This status is set if INT_B is enabled and INT_B# pin isin low level. Writing this bit to 1 does not clear this bit.It is cleared by resetting the INT_B interrupt factor.
9	0h	RO	**INT_A Status (normalintrsts_inta)** This status is set if INT_A is enabled and INT_A# pin isin low level. Writing this bit to 1 does not clear this bit.It is cleared by resetting the INT_A interrupt factor.

Bit Range	Default	Access	Field Name and Description
8	0h	RO	**Card Interrupt (normalintrsts_cardintsts)** In 1-bit mode, the HC shall detect the Card Interruptwithout SD Clock to support wakeup.In 4-bit mode, the card interrupt signal is sampledduring the interrupt cycle, so there are some sampledelays between the interrupt signal from the card andthe interrupt to the Host system. 0 - No Card Interrupt 1 - Generate Card Interrupt.
7	0h	RW1C	**Card Removal (normalintrsts_cardremsts)** This status is set if the Card Inserted in the PresentState register changes from 1 to 0.When the HD writes this bit to 1 to clear this status thestatus of the Card Inserted in the Present State registershould be confirmed. 0 - Card State Stable or Debouncing 1 - Card Removed.
6	0h	RW1C	**Card Insertion (normalintrsts_cardinssts)** This status is set if the Card Inserted in the PresentState register changes from 0 to 1.
5	0h	RW/1C	**Buffer Read Ready (normalintrsts_bufrdready)** This status is set if the Buffer Read Enable changes from 0 to 1.
4	0h	RW1C	**Buffer Write Ready (normalintrsts_bufwrready)** This status is set if the Buffer Write Enable changesfrom 0 to 1.
3	0h	RW1C	**DMA Interrupt (normalintrsts_dmainterrupt)** This status is set if the HC detects the Host DMA BufferBoundary in the Block Size Register.
2	0h	RW1C	**Block Gap Event (normalintrsts_blkgapevent)** If the Stop At Block Gap Request in the Block GapControl Register is set, this bit is set.
1	0h	RW1C	**Transfer Complete (normalintrsts_xfercomplete)** This bit is set when a read / write transaction iscompleted.

Bit Range	Default	Access	Field Name and Description
0	0h	RW1C	**Command Complete (normalintrsts_cmdcomplete)** This bit is set when we get the end bit of the commandresponse (Except Auto CMD12 and Auto CMD23). 0 - No Command Complete 1 - Command Complete

Error Interrupt Status (errorintrsts) – Offset 32

Bit Range	Default	Access	Field Name and Description
14:13	-	-	**Reserved**
12	0h	RW/1C	**Target Response Error (errorintrsts_hosterror)** Occurs when detecting ERROR in DMA transaction 0 - no error 1 – error.
11:10	-	-	**Reserved**
9	0h	RW	**ADMA Error (errorintrsts_admaerror)** This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status Register. 1- Error 0- No error.
8	0h	RW	**Auto CMD Error (errorintrsts_autocmderror)** This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register has changed from0 to 1.
7	0h	RW	**Current Limit Error (errorintrsts_currlimiterror)** By setting the SD Bus Power bit in the Power ControlRegister, the HC is requested to supply power for the SD Bus.

Bit Range	Default	Access	Field Name and Description
6	0h	RW	**Data End Bit Error (errorintrsts_dataendbiterror)** Occurs when detecting 0 at the end bit position of readdata which uses the DAT line or the end bit position ofthe CRC status. 0 - No Error 1 – Error.
5	0h	RW	**Data CRC Error (errorintrsts_datacrcerror)** Occurs when detecting CRC error when transferring readdata which uses the DAT line or when detecting theWrite CRC Status having a value of other than “010”. 0 - No Error 1 – Error.
4	0h	RW	**Data Timeout Error (errorintrsts_datatimeouterror)** Occurs when detecting one of following timeoutconditions. 1. Busy Timeout for R1b, R5b type. 2. Busy Timeout after Write CRC status 3. Write CRC status Timeout 4. Read Data Timeout 0 - No Error 1 – Timeout.
3	0h	RW	**Command Index Error (errorintrsts_cmdindexerror)** Occurs if a Command Index error occurs in the Command Response. 0 - No Error 1 – Error.
2	0h	RW	**Command End Bit Error (errorintrsts_cmdendbiterror)** Occurs when detecting that the end bit of a commandresponse is 0. 0 - No Error 1 - End Bit Error Generated.

Bit Range	Default	Access	Field Name and Description
1	0h	RW	**Command CRC Error (errorintrsts_cmdcrcerror)** 0 - No Error 1 - CRC Error Generated.
0	0h	RW	**Command Timeout Error (errorintrsts_cmdtimeouterror)** Occurs only if the no response is returned within 64 SDCLK cycles from the end bit of the command. 0 - No Error 1 – Timeout.

Normal Interrupt Status Enable (normalintrstsena) – Offset 34

Bit Range	Default	Access	Field Name and Description
14:10	-	-	**Reserved**
9	0h	RW	**INT_A Status Enable (int_a_stsena)** If this bit is set to 0, the Host Controller shall clear theinterrupt request to the System. The Host Driver mayclear this bit before servicing the INT_A and may set this bit again after all interrupt requests to INT_A pin are cleared to prevent inadvertent interrupts.
8	0h	RW	**Card Interrupt Status Enable (sdhcregset_cardintstsena)** If this bit is set to 0, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is setto 1.
7	0h	RW	**Card Removal Status Enable (sdhcregset_cardremstsena)** This status is set if the Card Inserted in the PresentState register changes from 1 to 0.
6	0h	RW	**Card Insertion Status Enable (sdhcregset_cardinsstsena)** This status is set if the Card Inserted in the PresentState register changes from 0 to 1.

Bit Range	Default	Access	Field Name and Description
5	0h	RW	**Buffer Read Ready Status Enable (buffrd_readtstsena)** This status is set if the Buffer Read Enable changes from 0 to 1.
4	0h	RW	**Buffer Write Ready Status Enable (buffwr_readtstsena)** This status is set if the Buffer Write Enable changesfrom 0 to 1.
3	0h	RW	**DMA Interrupt Status Enable (dmaintrstsena)** This status is set if the HC detects the Host DMA BufferBoundary in the Block Size register.
2	0h	RW	**Block Gap Event Status Enable (blockgap_eventstsena)** If the Stop At Block Gap Request in the BlockGap Control Register is set, this bit is set.
1	0h	RW	**Transfer Complete Status Enable (xfrcmpltstsena)** This bit is set when a read / write transaction iscompleted.
0	0h	RW	**Command Complete Status Enable (cmdcmpltstsena)** This bit is set when we get the end bit of the commandresponse.

Error Interrupt Status Enable (errorintrstsena) – Offset 36

This register is used to enable the Error Interrupt Status register fields.

Bit Range	Default	Access	Field Name and Description
14:13	-	-	**Reserved**
12	0h	RO	**Transfer Response Error (xfrresponce_err)** 0 - Masked 1 - Enabled
11	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
10	0h	RW	**Tuning error status enable (tune_errstsena)** 0 - Masked 1 - Enabled
9	0h	RW	**ADMA Error Status Enable (adma_errstsena)** 0 - Masked 1 - Enabled
8	0h	RW	**Auto CMD12 Error Status Enable (autocmd12_errstsena)** 0 - Masked 1 - Enabled
7	0h	RW	**Current Limit Error Status Enable (currentlim_errstsena)** 0 - Masked 1 - Enabled
6	0h	RW	**Data End Bit Error Status Enable (dataendbit_errstsena)** 0 - Masked 1 - Enabled
5	0h	RW	**Data CRC Error Status Enable (datacrc_errstsena)** 0 - Masked 1 - Enabled
4	0h	RW	**Data Timeout Error Status Enable (datatimeout_errstsena)** 0 - Masked 1 - Enabled
3	0h	RW	**Command Index Error Status Enable (cmdindex_errstsena)** 0 - Masked 1 - Enabled
2	0h	RW	**Command End Bit Error Status Enable (cmdendbit_errstsena)** 0 - Masked 1 - Enabled

Bit Range	Default	Access	Field Name and Description
1	0h	RW	**Command CRC Error Status Enable (cmdcrc_errstsena)** 0 - Masked 1 - Enabled
0	0h	RW	**Command Timeout Error Status Enable (cmdtimeout_errstsena)** 0 - Masked 1 - Enabled

Normal Interrupt Signal Enable (normalintrsigena) – Offset 38

This register is used to enable the Normal Interrupt Signal register. All the bits are RW, except for Reserved bits, and defined as follows:

0 - Masked

1 - Enabled.

Bit Range	Default	Access	Field Name and Description
14	0h	RW	**Boot Terminate Interrupt Signal Enable (bootintr_sigena)**
13	0h	RW	**Boot ack rcv Signal Enable (bootack_rcvsigena)**
12	0h	RW	**Re-Tuning Event Signal Enable (retune_eventsigena)**
11	0h	RW	**INT_C Signal Enable (int_c_sigena)**
10	0h	RW	**INT_B Signal Enable (int_b_sigena)**
9	0h	RW	**INT_A Signal Enable (int_a_sigena)**
8	0h	RW	**Card Interrupt Signal Enable (sdhcregset_cardintstsena)**

Bit Range	Default	Access	Field Name and Description
7	0h	RW	**Card Removal Signal Enable (sdhcregset_cardremstsena)**
6	0h	RW	**Card Insertion Signal Enable (sdhcregset_cardinsstsena)**
5	0h	RW	**Buffer Read Ready Signal Enable (buffrd_readtsigena)**
4	0h	RW	**Buffer Write Ready Signal Enable (buffwr_readtsigena)**
3	0h	RW	**DMA Interrupt Signal Enable (dmaintrsigena)**
2	0h	RW	**Block Gap Event Signal Enable (blockgap_eventsigena)**
1	0h	RW	**Transfer Complete Signal Enable (xfrcmpltsigena)**
0	0h	RW	**Command Complete Signal Enable (cmdcmpltsigena)**

Error Interrupt Signal Enable (errorintrsigena) – Offset 3a

This register is used to enable the Normal Interrupt Signal register. All the bits are RW, except for Reserved bits, and defined as follows:

0 - Masked

1 - Enabled.

Bit Range	Default	Access	Field Name and Description
14:11	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
10	0h	RW	**Tuning Error Signal Enable (tune_errsigena)**
9	0h	RW	**ADMA Error Signal Enable (adma_errsigena)**
8	0h	RW	**Auto CMD Error Signal Enable (autocmd12_errsigena)**
7	0h	RW	**Current Limit Error Signal Enable (currentlim_errsigena)**
6	0h	RW	**Data End Bit Error Signal Enable (dataendbit_errsigena)**
5	0h	RW	**Data CRC Error Signal Enable (datacrc_errsigena)**
4	0h	RW	**Data Timeout Error Signal Enable (datatimeout_errsigena)**
3	0h	RW	**Command Index Error Signal Enable (cmdindex_errsigena)**
2	0h	RW	**Command End Bit Error Signal Enable (cmdendbit_errsigena)**
1	0h	RW	**Command CRC Error Signal Enable (cmdcrc_errsigena)**
0	0h	RW	**Command Timeout Error Signal Enable (cmdtimeout_errsigena)**

Auto CMD12 Error Status (autocmderrsts) – Offset 3c

Bit Range	Default	Access	Field Name and Description
14:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7	0h	RO	**Command Not Issued By Auto CMD12 Error (autocmderrsts_nexterror)** Setting this bit to 1 means CMD_wo_DAT is notexecuted due to an Auto CMD12 error(D04- D01) in thisregister. This bit is set to 0 when Auto CMD Error isgenerated by Auto CMD23 0 – No Error 1 – Not Issued.
6:5	-	-	**Reserved**
4	0h	RO	**Auto CMD Index Error (autocmderrsts_indexerror)** Occurs if the Command Index error occurs in responseto a command. 0 – No Error 1 – Error
3	0h	RO	**Auto CMD End Bit Error (autocmderrsts_endbiterror)** Occurs when detecting that the end bit of commandresponse is 0. 0 – No Error 1 – End Bit Error Generated.
2	0h	RO	**Auto CMD CRC Error (autocmderrsts_crcerror)** Occurs when detecting a CRC error in the commandresponse. 0 – No Error 1 – CRC Error Generated.
1	0h	RO	**Auto CMD Timeout Error (autocmderrsts_timeouterror)** Occurs if the no response is returned within 64 SDCLKcycles from the end bit of the command.If this bit is set to 1, the other error status bits (D04 -D02) are meaningless. 0 - No Error 1 - Timeout.

Bit Range	Default	Access	Field Name and Description
0	0h	RO	**Auto CMD12 not Executed (autocmderrsts_notexecerror)** If memory multiple block data transfer is not starteddue to command error, this bit is not set because it isnot necessary to issue Auto CMD12.Setting this bit to 1 means the HC cannot issue AutoCMD12 to stop memory multiple block transfer due to some error. 0 - Executed 1 - Not Executed.

Host Control 2 (hostcontrol2) – Offset 3e

Bit Range	Default	Access	Field Name and Description
15	0h	RW	**Preset Value Enable (hostctrl2_presetvalueenable)** Host Controller Version 3.00 supports this bit. As theoperating SDCLK frequency and I/O driver strengthdepend on the Host System implementation, it isdifficult to determine these parameters in the StandardHost Driver.When Preset Value Enable is set to automatic. This bitenables the functions defined in the Preset Valueregisters.1 Automatic Selection by Preset Value are Enabled0 SDCLK and Driver Strength are controlled by HostDriver.
14	0h	RW	**Asynchronous Interrupt Enable (hostctrl2_asynchintrenable)** This bit can be set to 1 if a card support asynchronousinterrupt and Asynchronous Interrupt Support is set to 1in the Capabilities register. 0 – Disabled 1 – Enabled.
13:10	-	-	**Reserved**
9	0h	RW	**Driver Strength Select (hostctrl2_driverstrength)** Host Controller output driver in 1.8V signaling isselected by this bit. In 3.3V signaling, this field is noteffective.
8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7	0h	RW	**Sampling Clock Select (hostctrl2_samplingclkselect)** This bit is set by tuning procedure when Execute Tuningis cleared. Writing 1 to this bit is meaningless andignored. Setting 1 means that tuning is completedsuccessfully and setting 0 means that tuning is failed. Controller is receiving response or a read data block. 0 - Fixed clock is used to sample data 1 - Tuned clock is used to sample data
6	0h	RW	**Execute Tuning (hostctrl2_executetuning)** This bit is set to 1 to start tuning procedure andautomatically cleared when tuning procedure iscompleted. The result of tuning is indicated to SamplingClock Select. Tuning procedure is aborted by writing 0for more detail about tuning procedure. 0 - Not Tuned or Tuning Completed 1 - Execute Tuning.
5:4	-	-	**Reserved**
3	0h	RW	**1.8V Signaling Enable (hostctrl2_1p8vsignallingena)** This bit controls voltage regulator for I/O cell. 3.3V issupplied to the card regardless of signaling voltage.Setting this bit from 0 to 1 starts changing signal voltagefrom 3.3V to 1.8V.

Bit Range	Default	Access	Field Name and Description
2:0	0h	RW	**UHS Mode Select (hostctrl2_uhsmodeselect)** This field is used to select one of UHS-I modes andeffective when 1.8V Signaling Enable is set to 1. Select in the Clock Control register and Driver StrengthSelect according to Preset Value registers. In this case,one of preset value registers is selected by this field.Host Driver needs to reset SD Clock Enable beforechanging this field to avoid generating clock glitch. Aftersetting this field, Host Driver sets SD Clock Enableagain. 000b - SDR12 001b - SDR25 010b - SDR50 011b - SDR104 100b - DDR50 101b - HS400

Capabilities (capabilities) – Offset 40

This register provides the host driver with information specific to the host controllerimplementation. Please note, that the default values shown here assume no bypass of thecapabilities register. In case software decides to bypass the default capabilities register valuesthe reset values will present the bypassed value.

Bit Range	Default	Access	Field Name and Description
62:35	-	-	**Reserved**
34	1h	RO	**DDR50 Support (corecfg_ddr50support)** This bit indicates whether DDR50 is supported. 0 –Not Supported 1 –Supported.
33	1h	RO	**SDR104 Support (corecfg_sdr104support)** This bit indicates whether SDR104 is supported.SDR104requires tuning. 0 –Not Supported 1 –Supported.

Bit Range	Default	Access	Field Name and Description
32	1h	RO	**SDR50 Support (corecfg_sdr50support)** This bit indicates whether SDR50 is supported. 0 –Not Supported 1 –Supported.
31:30	1h	RO	**Slot Type (corecfg_slottype)** This field indicates usage of a slot by a specific HostSystem. (A host controller register set is defined perslot.) Embedded slot for one device (01b) means thatonly one on-removable device is connected to a SD busslot. Shared Bus Slot (10b) can be set if Host Controllersupports Shared Bus Control register.The Standard Host Driver controls only a removablecard or one embedded device is connected to a SD busslot.
29	0h	RO	**Asynchronous Interrupt Support (corecfg_asynchintrsupport)** This bit indicates whether the HC supportsAsynchronous Interrupt 0 –Not Supported 1 –Supported.
28:27	-	-	**Reserved**
26	1h	RO	**Voltage Support 1.8V (corecfg_1p8voltsupport)** This bit indicates whether the HC supports 1.8V. 0 –Not Supported 1 –Supported.
25	0h	RO	**Voltage Support 3.0V (corecfg_3p0voltsupport)** This bit indicates whether the HC supports 3.0V. 0 –Not Supported 1 –Supported.
24	0h	RO	**Voltage Support 3.3V (corecfg_3p3voltsupport)** This bit indicates whether the HC supports 3.3V. 0 –Not Supported 1 –Supported.

Bit Range	Default	Access	Field Name and Description
23	-	-	**Reserved**
22	1h	RO	**SDMA Support (corecfg_sdmasupport)** This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly. (SDMA Mode) 0 –Not Supported 1 –Supported
21	1h	RO	**High Speed Support (corecfg_highspeedsupport)** This bit indicates whether the HC and the Host System support High Speed mode. 0 –Not Supported 1 –Supported
20:18	-	-	**Reserved**
17:16	2h	RO	**Max Block Length (corecfg_maxblklength)** This value indicates the maximum block size that the HDcan read and write to the buffer in the HC.The buffer shall transfer this block size without waitcycles. Sizes can be defined as indicated below. 00 - 512 byte 01 - 1024 byte 10 - 2048 byte 11 - 4096 byte.

Bit Range	Default	Access	Field Name and Description
15:8	C8h	RO	**Base Clock Frequency for SD Clock (corecfg_baseclkfreq)** (1) 6-bit Base Clock Frequency This mode is supportedby the Host Controller Version 1.00 and 2.00. Upper 2-bit is not effective and always 0.Unit values are1MHz. The supported clock rangeis 10MHz to 63MHz. 0011 1111b 63MHz 0000 0010b 2MHz 0000 0001b 1MHz (2) 8-bit Base Clock Frequency This mode is supportedby the Host Controller Version 3.00. Unit values are1MHz. The supported clock range is 10MHz to 255MHz. FFh 255MHz 02h 2MHz 01h 1MHz.
7	1h	RO	**Timeout Clock Unit (corecfg_timeoutclkunit)** This bit shows the unit of base clock frequency used todetect Data Timeout Error. 0 - KHz 1 - MHz.
6	-	-	**Reserved**
5:0	01h	RO	**Timeout Clock Frequency (corecfg_timeoutclkfreq)** This bit shows the base clock frequency used to detectData Timeout Error. Not 0 - 1Khz to 63Khz or 1Mhz to 63Mhz.

Maximum Current Capabilities (maxcurrentcap) – Offset 48

Maximum Current Capabilities

Bit Range	Default	Access	Field Name and Description
62:24	-	-	**Reserved**
23:16	00h	WO	**Maximum Current for 1.8V (corecfg_maxcurrent1p8v)** 0 – Get value via another method 1 – 4mA 2 – 8mA 3 – 12mA … 255 – 1020mA
15:8	00h	WO	**Maximum Current for 3.0V (corecfg_maxcurrent3p0v)** 0 – Get value via another method 1 – 4mA 2 – 8mA 3 – 12mA … 255 – 1020mA
7:0	00h	WO	**(corecfg_maxcurrent3p3v)** 0 – Get value via another method 1 – 4mA 2 – 8mA 3 – 12mA … 255 – 1020mA

Force Event for AUTO CMD Error Status (ForceEventforAUTOCMDErrorStatus) – Offset 50

Force Event REGISTER for AUTO CMD Error Status

Bit Range	Default	Access	Field Name and Description
14:8	-	-	**Reserved**
7	0h	RO	**Force Event for Command Not Issued by AUTO CMD12 Error (forcecmdnotissuedbyautocmd12err)** Force Event for Command Not Issued by AUTO CMD12 Error 1 – Interrupt is generated 0 – No Interrupt
6:5	-	-	**Reserved**
4	0h	RO	**Force Event for AUTO CMD Index Error (forceautocmdindexerr)** Force Event for AUTO CMD Index Error 1 – Interrupt is generated 0 – No Interrupt
3	0h	RO	**Force Event for AUTO CMD End Bit Error (forceautocmdendbiterr)** Force Event for AUTO CMD End Bit Error 1 – Interrupt is generated 0 – No Interrupt
2	0h	RO	**Force Event for AUTO CMD CRC Error (forceautocmdcrcerr)** Force Event for AUTO CMD CRC Error 1 – Interrupt is generated0 – No Interrupt
1	0h	RO	**Force Event for AUTO CMD Timeout Error (forceautocmdtimeouterr)** Force Event for AUTO CMD Timeout Error 1 – Interrupt is generated 0 – No Interrupt

Bit Range	Default	Access	Field Name and Description
0	0h	WO	**Force Event for AUTO CMD12 Not Executed (forceautocmdnotexec)** Force Event for AUTO CMD12 Not Executed 1 – Interrupt is generated 0 – No Interrupt

Force Event Register for Error Interrupt Status (forceeventforerrintsts) – Offset 52

Bit Range	Default	Access	Field Name and Description
14:11	-	-	**Reserved**
10	0h	RO	**Force Event for Tuning Error (forcetuningerr)** 1 – Interrupt is generated 0 – No Interrupt
9	0h	RO	**Force Event for ADMA (forceadmaerr)** 1 - Interrupt is generated 0 - No interrupt
8	0h	RO	**Force Event for Auto CMD Error (forceautocmderr)** 1 – Interrupt is generated 0 – No Interrupt
7	0h	RO	**Force Event for Current Limit (forcecurrlimerr)** 1 – Interrupt is generated 0 – No Interrupt
6	0h	WO	**Force Event for Data End Bit Error (forcedatendbiterr)** 1 – Interrupt is generated 0 – No Interrupt

Bit Range	Default	Access	Field Name and Description
5	0h	RO	**Force Event for Data CRC Error (forcedatcrcerr)** 1 – Interrupt is generated 0 – No Interrupt
4	0h	RO	**Force Event for Data Timeout Error (forcedattimeouterr)** 1 – Interrupt is generated 0 – No Interrupt
3	0h	RO	**Force Event for Command Index Error (forcecmdindexerr)** 1 – Interrupt is generated 0 – No Interrupt
2	0h	RO	**Force Event for Command CRC Error (forcecmdendbiterr)** 1 – Interrupt is generated 0 – No Interrupt
1	0h	RO	**Force Event for Command CRC Error (forcecmdcrcerr)** 1 – Interrupt is generated 0 – No Interrupt
0	0h	RO	**Force Event for CMD Timeout Error (forcecmdtimeouterr)** 1 – Interrupt is generated 0 – No Interrupt

ADMA Error Status (admaerrsts) – Offset 54

When the ADMA Error interrupt occur, this register holds the ADMA State in ADMA Error States field and ADMA System Address holds address around the error descriptor

Bit Range	Default	Access	Field Name and Description
6:3	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
2	0h	RO	**ADMA Length Mismatch Error (admaerrsts_admalenmismatcherr)** ADMA Length Mismatch ErrorThis error occurs in the following 2 cases.While Block Count Enable being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. Total data length can not be divided by the block length. 1 - Error 0 - No error
1:0	0h	RO	**ADMA Error State (admaerrsts_admaerrorstate)** This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "10" because ADMA never stops in this state. D01 – D00 : ADMA Error State when error occurred Contents of SYS_SDR register. 00 - ST_STOP (Stop DMA) Points to next of the error descriptor. 01 - ST_FDS (Fetch Descriptor) Points to the error descriptor10 - Never set this state (Not used). 11 - ST_TFR (Transfer Data) Points to the next of the error descriptor

ADMA System Address Register 1 (admasysaddr01) – Offset 58

This register contains the physical address used for ADMA data transfer.

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**ADMA 32 bit System Address (adma_32bit_sysaddress)** This register holds byte address of executing command of the Descriptor table.

ADMA System Address Register2 (admasysaddr2) – Offset 5c

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW	**ADMA System Address (adma_64bit_sysaddress2)** This register holds byte address of executing command of the Descriptor table. 64-bit Address Descriptor uses Upper 32-bit of this register.

Preset Value for Initialization (presetvalue0) – Offset 60

Bit Range	Default	Access	Field Name and Description
15:14	0h	RO	**Driver Strength Select Value (DriverStrengthSelectValue)** Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 11b Driver Type D is Selected 10b Driver Type C is Selected 01b Driver Type A is Selected 00b Driver Type B is Selected
13:11	-	-	**Reserved**
10	0h	RO	**Clock Generator Select Value (ClockGeneratorSelectValue)** This bit is effective when Host Controller supports programmable clock generator. 1: Programmable Clock Generator 0: Host Controller Ver2.00 Compatible Clock Generator
9:0	004h	RO	**SDCLK Frequency Select Value (SDCLKFrequencySelectValue)** 10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.

Preset Value for Default Speed (presetvalue1) – Offset 62

Same description as Preset Value 0 register.

Preset Value for High Speed (presetvalue2) – Offset 64

Same description as Preset Value 0 register.

Preset Value for SDR12 (presetvalue3) – Offset 66

Same description as Preset Value 0 register.

Preset Value for SDR25 (presetvalue4) – Offset 68

Same description as Preset Value 0 register.

Preset Value for SDR50 (presetvalue5) – Offset 6a

Same description as Preset Value 0 register.

Preset Value for SDR104 (presetvalue6) – Offset 6c

Same description as Preset Value 0 register.

Preset Value for DDR50 (presetvalue7) – Offset 6e

Same description as Preset Value 0 register.

Boot Timeout Control (boottimeoutcnt) – Offset 70

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Boot Timeout Control (boot_timeoutcnt)** This value determines the interval by which DAT line time-outs are detected during boot operation for eMMC card.

Slot Interrupt Status (slotintrsts) – Offset fc

Bit Range	Default	Access	Field Name and Description
14:1	-	-	**Reserved**
0	0h	RO	**Slot 0 Interrupt Status (sdhchostif_slotintrstsslot0)**

EMMC PCI Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device & Vendor ID (DEVVENDID)	XXXX8086h
4h	4	PCI Status & Command (STATUSCOMMAND)	100000h
8h	4	Rev ID & Class Code (REVCLASSCODE)	80501XXh
ch	4	Carche Line & Latency & Header Type & BIST (CLLATHEADERBIST)	0h
10h	4	Base Address Low (BAR0)	4h
14h	4	Base Address Register high (BAR0_HIGH)	0h
18h	4	Base Address Register1 (BAR1)	4h
1ch	4	(BAR1_HIGH)	0h
2ch	4	Subsystem Vendor ID (SUBSYSTEMID)	0h
30h	4	(EXPANSION_ROM_BASEADDR)	0h
34h	4	Capabilities Pointer (CAPABILITYPTR)	80h
3ch	4	Interrupt (INTERRUPTREG)	0h
80h	4	Power Management Capability ID Register (POWERCAPID)	39001h
84h	4	Power Management Control and Status Register (PMECTRLSTATUS)	8h
90h	4	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)	F0140009h
94h	4	Device Vendor Specific (DEVID_VEND_SPECIFIC_REG)	1400010h
98h	4	SW LTR update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)	8041h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
9ch	4	Device IDLE Pointer Register (DEVICE_IDLE_POINTER_REG)	81C1h
a0h	4	DOI3 Max Power & PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)	290800h
b0h	4	General Purpose PCI RW Register1 (GEN_REGRW1)	0h
b4h	4	General Purpose PCI RW Register2 (GEN_REGRW2)	0h
b8h	4	General Purpose PCI RW Register3 (GEN_REGRW3)	0h
bch	4	General Purpose PCI RW Register4 (GEN_REGRW4)	0h
c0h	4	General Input Register (GEN_INPUT_REG)	0h

Device & Vendor ID (DEVVENDID) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:16	See Description	RO	**Device ID (DID)** Identifies the device. Refer to the Device and Revision ID Table in Volume 1 for default value.
15:0	8086h	RO	**Vendor ID (VID)** Intel default value is 8086h

PCI Status & Command (STATUSCOMMAND) – Offset 4

STATUSCOMMAND- Status and Command

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29	0h	RW/1C	**Received Master Abort (RMA)** The software writes a 1 to this bit to clear it.
28	0h	RW/1C	**Received Target Abort (RTA)** The software writes a 1 to this bit to clear it.
27:21	-	-	**Reserved**
20	1h	RO	**Capabilities List (CAPLIST)** Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at the configuration offset 34h.
19	0h	RO	**Interrupt Status (INTR_STATUS)** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and thisInterrupt Status bit is a 1, is the device/function interrupt message sent.
18:11	-	-	**Reserved**
10	0h	RW	**Interrupt Disable (INTR_DISABLE)** Setting this bit disables INTx assertion.
9	-	-	**Reserved**
8	0h	RW	**(Reserved)**
7:3	-	-	**Reserved**
2	0h	RW	**Bus Master Enable (BME)** 0 = the Bridge does not generate any new upstream transaction onIOSF as a master. Reset value of this bit is 0.

Bit Range	Default	Access	Field Name and Description
1	0h	RW	**Memory Space Enable (MSE)** MSE is part of the Type PCI configuration space eachdevice has. When disabled no downstream traffic from the bridge is available.
0	-	-	**Reserved**

Rev ID & Class Code (REVCLASSCODE) – Offset 8

REVCLASSCODE - Revision ID and Class Code

Bit Range	Default	Access	Field Name and Description
31:8	80501h	RO	**Class Code (CLASS_CODES)** The Class Code register is read-only and is used to identify the genericfunction of the device, and in some cases, a specific register-levelprogramming interface. The register is broken into 3 Byte-size fields. - The upper Byte (at offset 0Bh) is a base class code that broadlyclassifies the type of function the device performs. - The middle Byte (at offset 0Ah) is a sub-class code that identifiesmore specifically the function of the device. - The lower Byte (at offset 09h) identifies a specific register-levelprogramming interface (if any) so that device independentsoftware can interact with the device. This register is tied to a strap at the top level.
7:0	See Description	RO	**Rev ID (RID)** Revision ID identifies the revision of particular PCI device. Refer to Device and Revision ID table in Vol1 for specific value.

Carche Line & Latency & Header Type & BIST (CLLATHEADERBIST) – Offset c

CLLATHEADERBIST - Cache Line Latency Header and BIST

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0h	RO	**Multi-Function Device (MULFNDEV)** This bit is 0 or 1 depending upon the value assigned o thetop level strap
22:16	00h	RO	**Header Type (HEADERTYPE)** Implements Type 0 Configuration header.
15:8	00h	RO	**Latency Timer (LATTIMER)** This register is implemented as R/W with default as 0.
7:0	00h	RW	**Cacheline Size (CACHELINE_SIZE)** This register is implemented as R/W with default as 0.

Base Address Low (BAR0) – Offset 10

BAR -Base Address Register

Bit Range	Default	Access	Field Name and Description
31:12	00000h	RW	**BARL (BASEADDR)** Base address of the memory space.
11:4	00h	RO	**Size Indicator (SIZEINDICATOR)** Size Indicator Read Only. The size of this register depends on the size of the memory space.
3	0h	RO	**Prefetchable (PREFETCHABLE)** Indicates that this BAR is not prefetchable.
2:1	2h	RO	**(TYPE)** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range. If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range.
0	0h	RO	**Memory Space Indicator (MSI)** 0 indicates this BAR is present in the memory space.

Base Address Register high (BAR0_HIGH) – Offset 14

This register is present on if BAR_64_EN is set as 1.

This register enables 64-bit BARs.

IfBAR_64_EN is 0, then this register is RO.

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**BARH (BASEADDR_HIGH)** Base address of the OCP fabric memory space.

Base Address Register1 (BAR1) – Offset 18

Memory accesses to BAR1 region are aliased to the PCI configuration space. The BAR1 regionis always 4K.

Bit Range	Default	Access	Field Name and Description
31:12	00000h	RW	**Base Address Register1 (BASEADDR1)** This field is present if BAR1 is enabled through private configuration space.
11:4	00h	RO	**SIZEBAR1 (SIZEINDICATOR1)** Always is 0 as minimum size is 4K
3	0h	RO	**Prefetchable (PREFETCHABLE1)** Indicates that this BAR is not prefetchable.
2:1	2h	RO	**TYPE (TYPE1)** Always 0 as minimum size is 4K
0	0h	RO	**Base Address Register1 (BAR1)** This field is present if BAR1 is enabled through private configuration space.

(BAR1_HIGH) – Offset 1c

This register is present on if BAR_64_EN is set as 1.

This register enables 64bit BARs.

IfBAR_64_EN is 0 then this register is RO.

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**(BASEADDR1_HIGH)** Base address of the OCP fabric memory space.

Subsystem Vendor ID (SUBSYSTEMID) – Offset 2c

This register must be implemented for any function that can be instantiated morethan once in a given system.The SVID register, in combination with the Subsystem ID register, enables theoperating environment to distinguish one subsystem from the other.

This register is a Read Write Once register

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/O	**(SUBSYSTEMID)**
15:0	0000h	RW/O	**(SUBSYSTEMVENDORID)**

(EXPANSION_ROM_BASEADDR) – Offset 30

EXPANSION ROM base address

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RO	**(EXPANSION_ROM_BASE)** Value of all zeros indicates no support for Expansion ROM.

Capabilities Pointer (CAPABILITYPTR) – Offset 34

This capability points to the PM Capability (0x80) structure.

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	80h	RO	**(CAPPTR_POWER)**

Interrupt (INTERRUPTREG) – Offset 3c

INTERRUPTREG - Interrupt Register

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO	**Maximum Latency (MAX_LAT)** Value of 0 indicates device has no major requirements for the settings of latencytimers
23:16	00h	RO	**Minimum Latency (MIN_GNT)** Value of 0 indicates device has nomajor requirements for the settings of latency timers.
15:12	-	-	**Reserved**
11:8	0h	RO	**Interrupt Pin (INTPIN)** Interrupt Pin Value in this register is reflected from the IPIN value inthe private configuration space. For a single function device, this ideally is INTA.
7:0	00h	RW	**Interrupt Line (INTLINE)** It is used to communicate to software, the interrupt line to which the interrupt pinis connected.

Power Management Capability ID Register (POWERCAPID) – Offset 80

POWERCAPID - PowerManagement Capability ID

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:27	00h	RO	**PME_Support (PMESUPPORT)** This 5-bit field indicates the power states in which the function can assert the PME#. A value of 0b for any bit indicates that the function is not capable of asserting thePME# signal in that power state. bit 27 = 1: PME# can be asserted from D0 bit28 = 1: PME# can be asserted from D1. bit 29 = 1: PME# can be asserted from D2. bit30 = 1:PME# can be asserted from D3hot bit 31 = 1:PME# can be asserted from D3cold.
26:19	-	-	**Reserved**
18:16	3h	RO	**Version (VERSION)** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	90h	RO	**Next Capability (NXTCAP)** Points to the next capability structure. This points to NULL if eitherENABLE_PCI_IDLE_CAP is 0 or if Disable PCI Device Idle capability bit is set as 1in the private space. Else this points to PCI Device Idle capability structure atoffset 90h
7:0	01h	RO	**Power Management Capability (POWER_CAP)** Indicates this is power management capability.

Power Management Control and Status Register (PMECTRLSTATUS) – Offset 84

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
15	0h	RW/1C	**PME Status (PMESTATUS)** 0: Software clears the bit by writing a 1 to it. 1: This bit is set when the PME# signal is asserted independent of the state ofthe PME Enable bit (bit 8 in this register)
14:9	-	-	**Reserved**
8	0h	RW	**PME Enable (PMEENABLE)** 1: Enables the function to assert PME#. 0: PME# message on Sideband is disabled.
7:4	-	-	**Reserved**
3	1h	RO	**(NO_SOFT_RESET)** This bit indicates that devices transitioning from D3hot to D0 because ofPowerstate commands do not perform an internal reset.Configuration Context is preserved.
2	-	-	**Reserved**
1:0	0h	RW	**Power State (POWERSTATE)** This field is used both to determine the current power state and to set a newpower state.The values are: 00 D0 state 11 D3HOT state

PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD) – Offset 90

Bit Range	Default	Access	Field Name and Description
31:28	0Fh	RO	**Vendor ID (VEND_CAP)** Indicates this is Vendor Specific capability.

Bit Range	Default	Access	Field Name and Description
27:24	0h	RO	**(REVID)** Revision ID of capability structure.
23:16	14h	RO	**Length (CAP_LENGTH)** Indicates the number of bytes in the capability structure.
15:8	00h	RO	**Next Capability (NEXT_CAP)** Points to the next capability structure. This points to NULL.
7:0	09h	RO	**Capability ID (CAPID)**

Device Vendor Specific (DEVID_VEND_SPECIFIC_REG) – Offset 94

Bit Range	Default	Access	Field Name and Description
31:20	014h	RO	**VSEC Length (VSEC_LENGTH)** Vendor Specific Capability Length.
19:16	0h	RO	**Vendor Revision (VSEC_REV)** Vendor specific revision.
15:0	0010h	RO	**Vendor ID (VSECID)** Vendor specific ID.

SW LTR update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) – Offset 98

SW LTR Update MMIO Location Register

Bit Range	Default	Access	Field Name and Description
31:4	804h	RO	**SWLTRLOC (SW_LAT_DWORD_OFFSET)** This register contains the location pointer to the SW LTR register in MMIO space,as an offset from the specified BAR.

Bit Range	Default	Access	Field Name and Description
3:1	0h	RO	**BAR NUM (SW_LAT_BAR_NUM)** Indicates that the SW LTR update MMIO location is always at BAR0.
0	1h	RO	**(SW_LAT_VALID)** This value is reflected from the SW LTR valid strap at the top level.

Device IDLE Pointer Register (DEVICE_IDLE_POINTER_REG) – Offset 9c

Device IDLE pointer register

Bit Range	Default	Access	Field Name and Description
31:4	000081Ch	RO	**(DWORD_OFFSET)** This register contains the location pointer to the SW LTR register in MMIO space,as an offset from the specified BAR.
3:1	0h	RO	**(BAR_NUM)** Indicates that the D0i3 MMIO location is always at BAR0.
0	1h	RO	**(VALID)** 0= not valid1= valid

D0I3 Max Power & PG Config (D0I3_MAX_POW_LAT_PG_CONFIG) – Offset a0

D0idle_Max_Power_On_Latency is set by BIOS at boot and read by device driver SW tocalculate approximate cost of a D0idle entry + exit cycle. This allows driver to avoid idle entryin cases where device duty cycle is larger than D0idle entry + exit cycle.

Bit Range	Default	Access	Field Name and Description
30:22	-	-	**Reserved**
21	1h	RW	**Hardware Autonomous Enable (HAE)** If set, then the PGCB may request a PGwhenever it is idle.

Bit Range	Default	Access	Field Name and Description
20	-	-	**Reserved**
19	1h	RW	**(SLEEP_EN)** if clear, then IP will never asset Sleep to the retention flops. Ifset, then IP may assert Sleep during PG'ing.
18	0h	RW	**PG Enable (PGE)** If clear, then IP will never request a PG. If set, then IP may requestPG when proper conditions are met.
17	0h	RW	**(I3_ENABLE)** if set, then IP will PG when idle and the D0i3 register (in PGCB) isset. If this bit is set, the IP will not PG unless the IPs D0i3 control bit ='1'. Bit [5] isnot required to be set when this bit is set.
16	1h	RW	**PMC Request Enable (PMCRE)** When bits [1:0] = '11', power gating is enabled whenever either the D3register or the D0i3 register is set.
15:13	-	-	**Reserved**
12:10	2h	RW/O	**Power On Latency Scale (POW_LAT_SCALE)** Support for codes 010 (1us) or 011 (32us) for Exit Latency Scale (1us -) 32mstotal span) only.
9:0	000h	RW/O	**Power On Latency value (POW_LAT_VALUE)** This value is written by BIOS to communicate to the Driver.

General Purpose PCI RW Register1 (GEN_REGRW1) – Offset b0

General Purpose PCI Register

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**(GEN_REG_RW1)**

General Purpose PCI RW Register2 (GEN_REGRW2) – Offset b4

General Purpose PCI Register

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**(GEN_REG_RW2)**

General Purpose PCI RW Register3 (GEN_REGRW3) – Offset b8

General Purpose PCI Register.

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**(GEN_REG_RW3)**

General Purpose PCI RW Register4 (GEN_REGRW4) – Offset bc

General Purpose PCI Register

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**(GEN_REG_RW4)**

General Input Register (GEN_INPUT_REG) – Offset c0

General Purpose Input Register.

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO	**(GEN_REG_INPUT_RW)**

eMMC PCR Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
600h	4	Dynamic Clock Gating Control (GPPRVRW1)	0h

Dynamic Clock Gating Control (GPPRVRW1) – Offset 600

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Bit Range	Default	Access	Field Name and Description
30:7	-	-	**Reserved**
6	0h	RW	**eMMC Functional Clock Gating Enable (emmc_func)** 1 = Enabled 0 = Disabled
5	0h	RW	**eMMC Synchronous Clock Gating Enable (emmc_ocp)** 1 = Enabled 0 = Disabled
4:0	-	-	**Reserved**

Enhanced SPI (eSPI) PCI Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Identifiers (ESPI_DID_VID)	XXXX8086h
4h	4	Device Status and Command (ESPI_STS_CMD)	403h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8h	4	Class Code and Revision ID (ESPI_CC_RID)	60100XXh
2ch	4	Sub System Identifiers (ESPI_SS)	0h
34h	4	Capability List Pointer (ESPI_CAPP)	0h
80h	4	I/O Decode Ranges and I/O Enables (ESPI_IOD_IOE)	0h
84h	4	eSPI Generic I/O Range 1 (ESPI_LGIR1)	0h
88h	4	eSPI Generic I/O Range 2 (ESPI_LGIR2)	0h
8ch	4	eSPI Generic I/O Range 3 (ESPI_LGIR3)	0h
90h	4	eSPI Generic I/O Range 4 (ESPI_LGIR4)	0h
94h	4	USB Legacy Keyboard/Mouse Control (ESPI_ULKMC)	0h
98h	4	eSPI Generic Memory Range (ESPI_LGMR)	0h
d8h	4	BIOS Decode Enable (ESPI_BDE)	FFCFh
dch	4	BIOS Control (ESPI_BC)	20h

Identifiers (ESPI_DID_VID) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:16	See Description	RO/V	**Device Identification (DID)** Indicates the Device ID of the controller. Refer to the Device and Revision ID Table in Volume 1 for the default value.
15:0	8086h	RO	**Vendor Identification (VID)** Indicates Intel

Device Status and Command (ESPI_STS_CMD) – Offset 4

Bit Range	Default	Access	Field Name and Description
31	0b	RW/1C/V	**Detected Parity Error (DPE)** Set when a parity error is detected on the internal bus. This bit gets set even if CMD.PERE is not set.
30	0b	RW/1C/V	**Signaled System Error (SSE)** Set when the eSPI controller signals a system error to the internal SERR# logic.
29	0b	RW/1C/V	**Received Master Abort (RMA)** Set when the bridge receives a completion with unsupported request status.
28	0b	RW/1C/V	**Received Target Abort (RTA)** Set when the bridge receives a completion with completer abort status.
27	0b	RW/1C/V	**Signaled Target Abort (STA)** Set when the bridge generates a completion packet with target abort status.
26:25	00b	RO	**DEVSEL# Timing Status (DTS)** Indicates medium timing, although this has no meaning on the HW.
24	0b	RW/1C/V	**Data Parity Error Detected (DPD)** Set when the bridge receives a completion packet from the backbone from a previous request, and detects a parity error, and CMD.PERE is set.
23	0b	RO	**Fast Back to Back Capable (FBC)** Reserved - bit has no meaning on the HW.
22	-	-	**Reserved**
21	0b	RO	**66 MHz Capable (C66)** Reserved - bit has no meaning on the HW.
20	0b	RO	**Capabilities List (CLIST)** Reserved.
19	0b	RO	**Interrupt Status (INTS)**
18:11	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
10	1b	RO	**Interrupt Disable (INTD)**
9	0b	RO	**Fast Back to Back Enable (FBE)** Reserved as 0 per PCI-Express spec.
8	0b	RW	**SERR# Enable (SEE)** Enable SERR# to be generated if this bit is set.
7	0b	RO	**Wait Cycle Control (WCC)** Reserved as 0 per PCI-Express spec.
6	0b	RW	**Parity Error Response Enable (PERE)** This bit is set to 1 to enable response to parity errors when detected.
5	0b	RO	**VGA Palette Snoop (VGA_PSE)** Reserved as 0 per PCI-Express spec.
4	0b	RO	**Memory Write and Invalidate Enable (MWIE)** Reserved as 0 per PCI-Express spec.
3	0b	RO	**Special Cycle Enable (SCE)** Reserved as 0 per PCI-Express spec.
2	0b	RW	**Bus Master Enable (BME)** When this bit is set to 1, it enables the devices connected to eSPI to master upstream transactions to Host memory. Note: Any eSPI device connected to eSPI also has a BME bit in its Peripheral Channel Configuration register. This eSPI Slave BME bit also needs to be set in order for the Slave to send upstream memory requests. BIOS is responsible for setting both the eSPI-MC's BME (this bit) and the eSPI Slaves' BME bits using theTunneled Access to Slave Configuration mechanism. Furthermore, for proper operation, SW should ensure that the BME field in both the host and device are programmed with the same value (i.e. either 0 or 1)
1	1b	RO	**Memory Space Enable (MSE)** Memory space cannot be disabled.
0	1b	RO	**I/O Space Enable (IOSE)** I/O space cannot be disabled.

Class Code and Revision ID (ESPI_CC_RID) – Offset 8

Bit Range	Default	Access	Field Name and Description
31:24	06h	RO	**Base Class Code (BCC)** Indicates the device is a bridge device.
23:16	01h	RO	**Sub-Class Code (SCC)** Indicates the device a PCI to ISA bridge.
15:8	00h	RO	**Programming Interface (PI)** The eSPI bridge has no programming interface.
7:0	See Description	RO/V	**Revision ID (RID)** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 of the EDS for specific value.

Sub System Identifiers (ESPI_SS) – Offset 2c

This register is initialized to logic 0 by the assertion of PLTRST#. This register can be

written only once after PLTRST# de-assertion.

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/O	**Subsystem ID (SSID)** This is written by BIOS. No hardware action taken on this value.
15:0	0000h	RW/O	**Subsystem Vendor ID (SSVID)** This is written by BIOS. No hardware action taken on this value.

Capability List Pointer (ESPI_CAPP) – Offset 34

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	00h	RO	**Capability Pointer (CP)** Indicates the offset of the first Capability Item.

I/O Decode Ranges and I/O Enables (ESPI_IOD_IOE) – Offset 80

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29	0b	RW	**Microcontroller Enable #2 (ME2)** Enables decoding of I/O locations 4Eh and 4Fh.
28	0b	RW	**SuperI/O Enable (SE)** Enables decoding of I/O locations 2Eh and 2Fh.
27	0b	RW	**Microcontroller Enable #1 (ME1)** Enables decoding of I/O locations 62h and 66h.
26	0b	RW	**Keyboard Enable (KE)** Enables decoding of the keyboard I/O locations 60h and 64h.
25	0b	RW	**High Gameport Enable (HGE)** Enables decoding of the I/O locations 208h to 20Fh.
24	0b	RW	**Low Gameport Enable (LGE)** Enables decoding of the I/O locations 200h to 207h.
23:20	-	-	**Reserved**
19	0b	RW	**Floppy Drive Enable (FDE)** Enables decoding of the FDD range. Range is selected by LIOD.FDE
18	0b	RW	**Parallel Port Enable (PPE)** Enables decoding of the LPT range. Range is selected by LIOD.LPT.

Bit Range	Default	Access	Field Name and Description
17	0b	RW	**Com Port B Enable (CBE)** Enables decoding of the COMB range. Range is selected by LIOD.CB.
16	0b	RW	**Com Port A Enable (CAE)** Enables decoding of the COMA range. Range is selected by LIOD.CA.
15:13	-	-	**Reserved**
12	0b	RW	**FDD Range (FDD)** The following table describes which range to decode for the FDD Port Bits Decode Range 0 3F0h - 3F5h, 3F7h (Primary) 1 370h - 375h, 377h (Secondary)
11:10	-	-	**Reserved**
9:8	00b	RW	**LPT Range (LPT)** The following table describes which range to decode for the LPT Port: Bits Decode Range 00 378h - 37Fh and 778h - 77Fh 01 278h - 27Fh (port 279h is read only) and 678h - 67Fh 10 3BCh - 3BEh and 7BCh - 7BEh 11 Reserved
7	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
6:4	000b	RW	**ComB Range (CB)** The following table describes which range to decode for the COMB Port Bits Decode Range 000 3F8h - 3FFh (COM 1) 001 2F8h - 2FFh (COM 2) 010 220h - 227h 011 228h - 22Fh 100 238h - 23Fh 101 2E8h - 2EFh (COM 4) 110 338h - 33Fh 111 3E8h - 3EFh (COM 3)
3	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
2:0	000b	RW	**ComA Range (CA)** The following table describes which range to decode for the COMA Port Bits Decode Range 000 3F8h - 3FFh (COM 1) 001 2F8h - 2FFh (COM 2) 010 220h - 227h 011 228h - 22Fh 100 238h - 23Fh 101 2E8h - 2EFh (COM 4) 110 338h - 33Fh 111 3E8h - 3EFh (COM 3)

eSPI Generic I/O Range 1 (ESPI_LGIR1) – Offset 84

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:18	00h	RW	**Address[7:2] Mask (ADDR_MASK)** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	-	-	**Reserved**
15:2	0000h	RW	**Address[15:2] (ADDR)** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**eSPI Decode Enable (LDE)** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

eSPI Generic I/O Range 2 (ESPI_LGIR2) – Offset 88

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:18	00h	RW	**Address[7:2] Mask (ADDR_MASK)** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	-	-	**Reserved**
15:2	0000h	RW	**Address[15:2] (ADDR)** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	-	-	**Reserved**
0	0b	RW	**Decode Enable (LDE)** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

eSPI Generic I/O Range 3 (ESPI_LGIR3) – Offset 8c

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:18	00h	RW	**Address[7:2] Mask (ADDR_MASK)** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	-	-	**Reserved**
15:2	0000h	RW	**Address[15:2] (ADDR)** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	-	-	**Reserved**
0	0b	RW	**Decode Enable (LDE)** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

eSPI Generic I/O Range 4 (ESPI_LGIR4) – Offset 90

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:18	00h	RW	**Address[7:2] Mask (ADDR_MASK)** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
15:2	0000h	RW	**Address[15:2] (ADDR)** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	-	-	**Reserved**
0	0b	RW	**Decode Enable (LDE)** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

USB Legacy Keyboard/Mouse Control (ESPI_ULKMC) – Offset 94

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15	0b	RW/1C/V	**SMI Caused by End of Pass-through (SMIBYENDPS)** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 7, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
14:12	-	-	**Reserved**
11	0b	RW/1C/V	**SMI Caused by Port 64 Write (TRAPBY64W)** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 3, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch. Note that the A20Gate Pass-Through Logic allows specific port 64h Writes to complete without setting this bit.
10	0b	RW/1C/V	**SMI Caused by Port 64 Read (TRAPBY64R)** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 2, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.

Bit Range	Default	Access	Field Name and Description
9	0b	RW/1C/V	**SMI Caused by Port 60 Write (TRAPBY60W)** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 1, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch. Note that the A20Gate Pass-Through Logic allows specific port 60h Writes to complete without setting this bit.
8	0b	RW/1C/V	**SMI Caused by Port 60 Read (TRAPBY60R)** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 0, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
7	0b	RW	**SMI at End of Pass-through Enable (SMIATENDPS)** May need to cause SMI at the end of a pass-through. Can occur if an SMI is generated in the middle of a pass through, and needs to be serviced later.
6	0b	RO/V	**Pass Through State (PSTATE)** This read-only bit indicates that the state machine is in the middle of an A20GATE pass-through sequence. If software needs to reset this bit, it should set Bit 5 0.
5	0b	RW	**A20Gate Pass-Through Enable (A20PASSEN)** When enabled, allows A20GATE sequence Pass-Through function. When enabled, a specific cycle sequence involving writes to port 60h and port 64h does not result in the setting of the SMI status bits.SMI# will not be generated, even if the various enable bits are set.
4	-	-	**Reserved**
3	0b	RW	**SMI on Port 64 Writes Enable (s64WEN)** When set, a 1 in bit 11 will cause an SMI event.
2	0b	RW	**SMI on Port 64 Reads Enable (s64REN)** When set, a 1 in bit 10 will cause an SMI event.
1	0b	RW	**SMI on Port 60 Writes Enable (s60WEN)** When set, a 1 in bit 9 will cause an SMI event.
0	0b	RW	**SMI on Port 60 Reads Enable (s60REN)** When set, a 1 in bit 8 will cause an SMI event.

eSPI Generic Memory Range (ESPI_LGMR) – Offset 98

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW	**Memory Address[31:16] (MADDR)** This field specifies a 64KB memory block anywhere in the 4GB memory space that will be decoded to eSPI as standard Memory Cycle if enabled.
15:1	-	-	**Reserved**
0	0b	RW	**Memory Range Decode Enable (LGMRD_EN)** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

BIOS Decode Enable (ESPI_BDE) – Offset d8

Note that this register effects the BIOS decode regardless of whether the BIOS is

resident on LPC or SPI. The concept of Feature Space does not apply to SPI-based

flash. PCH simply decodes these ranges as memory accesses when enabled for the SPI

flash interface.

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15	1b	RO	**F8-FF Enable (EF8)** Enables decoding of 512K of the following BIOS range: Data space: FFF80000h - FFFFFFFFh Feature space: FFB80000h - FFBFFFFFh

Bit Range	Default	Access	Field Name and Description
14	1b	RW	**F0-F8 Enable (EF0)** Enables decoding of 512K of the following BIOS range: Data space: FFF00000h - FFF7FFFFh Feature space: FFB00000h - FFB7FFFFh
13	1b	RW	**E8-EF Enable (EE8)** Enables decoding of 512K of the following BIOS range: Data space: FFE80000h - FFEFFFFFh Feature space: FFA80000h - FFAFFFFFh
12	1b	RW	**E0-E8 Enable (EE0)** Enables decoding of 512K of the following BIOS range: Data space: FFE00000h - FFE7FFFFh Feature Space: FFA00000h - FFA7FFFFh
11	1b	RW	**D8-DF Enable (ED8)** Enables decoding of 512K of the following BIOS range: Data space: FFD80000h - FFDFFFFFh Feature space: FF980000h - FF9FFFFFh
10	1b	RW	**D0-D7 Enable (ED0)** Enables decoding of 512K of the following BIOS range: Data space: FFD00000h - FFD7FFFFh Feature space: FF900000h - FF97FFFFh
9	1b	RW	**C8-CF Enable (EC8)** Enables decoding of 512K of the following BIOS range: Data space: FFC80000h - FFCFFFFFh Feature space: FF880000h - FF8FFFFFh
8	1b	RW	**C0-C7 Enable (EC0)** Enables decoding of 512K of the following BIOS range: Data space: FFC00000h - FFC7FFFFh Feature space: FF800000h - FF87FFFFh

Bit Range	Default	Access	Field Name and Description
7	1b	RW	**Legacy F Segment Enable (LFE)** This enables the decoding of the legacy 64KB range at F0000h - FFFFFh Note that decode for the BIOS legacy F segment is enabled by the LFE bit only.
6	1b	RW	**Legacy E Segment Enable (LEE)** This enables the decoding of the legacy 64KB range at E0000h - EFFFFh Note that decode for the BIOS legacy E segment is enabled by the LEE bit only.
5:4	-	-	**Reserved**
3	1b	RW	**70-7F Enable (E70)** Enables decoding of 1MB of the following BIOS range: Data space: FF700000h - FF7FFFFFh Feature space: FF300000h - FF3FFFFFh
2	1b	RW	**60-6F Enable (E60)** Enables decoding of 1MB of the following BIOS range: Data space: FF600000h - FF6FFFFFh Feature Space: FF200000h - FF2FFFFFh
1	1b	RW	**50-5F Enable (E50)** Enables decoding of 1MB of the following BIOS range: Data space: FF500000h - FF5FFFFFh Feature space: FF100000h - FF1FFFFFh
0	1b	RW	**40-4F Enable (E40)** Enables decoding of 1MB of the following BIOS range: Data space: FF400000h - FF4FFFFFh Feature space: FF000000h - FF0FFFFFh

BIOS Control (ESPI_BC) – Offset dc

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**
11	0b	RW/L	**BIOS Write Reporting (Async-SMI) Enable (BWRE)** 0: Disable reporting of BIOS Write event. 1: Enable reporting of BIOS Write event (PCBC.BWRS = 1) using Async-SMI.
10	0b	RW/1C/V	**BIOS Write Status (BWRS)** HW sets this bit if a memory write access is detected to a protected BIOS range. 0: Memory write to BIOS region not attempted or attempted with PCBC.WPD = 1. 1: A memory write transaction to BIOS region has been received with PCBC.WPD = 0. Note: SW must write a 1 to this bit to clear.
9	-	-	**Reserved**
8	0b	RW/1C/V	**BIOS Write Protect Disable Status (BWPDS)** HW sets this bit if configuration write access is detected to protected PCBC.WPD bit. 0: No attempt has been made to set PCBC.WPD with PCBC.LE = 1. 1: A configuration write request has been received to set PCBC.WPD (from 0 to 1) with PCBC.LE = 1. Note: SW must write a 1 to this bit to clear it.
7	0b	RW/L	**BIOS Interface Lock-Down (BILD)** When set, prevents BC.TS and BC.BBS from being changed. This bit can only be written from 0 to 1 once. BIOS Note: This bit is not backed up in the RTC well. This bit should also be set in the BUC register in the RTC device to record the last state of this value following a cold reset.

Bit Range	Default	Access	Field Name and Description
6	0b	RW/V/L	**Boot BIOS Strap (BBS)** This field determines the destination of accesses to the BIOS memory range. For the default, see the Strap section for details. 0: SPI 1: LPC/eSPI When SPI or LPC/eSPI is selected, the range that is decoded is further qualified by other configuration bits described in the respective sections. The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down is not set.
5	1b	RW/L	**Enable InSMM.STS (EISS)** When this bit is set, the BIOS region is not writable until SMM sets the InSMM.STS bit. If this bit is set, then WPD must be a 1 and InSMM.STS (0xFED3_0880(0)) must be 1 also. If this bit is clear, then BIOS is writable based only on WPD = 1 and the InSMM.STS is a dont care.
4	0b	RO/V	**Top Swap (TS)** When set, PCH will invert either A16, A17, A18, A19, or A20 for cycles going to the BIOS space (but not the Feature space). When cleared, PCH will not invert the lines. If booting from LPC (FWH) or eSPI, then the Boot Block Size is fixed at 64KB and A16 is inverted if Top Swap is enabled. If booting from SPI, then the BOOT_BLOCK_SIZE soft strap determines if A16, A17, A18, A19, or A20 should be inverted if Top Swap is enabled. Note: If the Top-Swap strap is asserted, then this bit cannot be cleared by software. The strap jumper should be removed and the system rebooted. BIOS Note: This bit provides a read-only path to view the state of the Top Swap strap. It is backed up and driven from the RTC well. BIOS will need to program the corresponding register in the RTC well, which will be reflected in this register.
3	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
2	0b	RO/V	**eSPI Enable Pin Strap (ESPI)** This field determines the destination of accesses to the D31:F0 and related Fixed and Variable IO and Memory decode ranges, including BIOS memory range. 0 = LPC is the D31:F0 target. 1 = eSPI is the D31:F0 target. Note: This field cannot be overwritten by software (unlike the PCBC.BBS field).
1	0b	RW/L	**Lock Enable (LE)** When set, setting the WP bit will cause SMI. When cleared, setting the WP bit will not cause SMI. Once set, this bit can only be cleared by a PLTRST#. When this bit is set, EISS - bit (5) of this register is locked down.
0	0b	RW	**Write Protect Disable (WPD)** When set, access to the BIOS space is enabled for both read and write cycles to BIOS. When cleared, only read cycles are permitted to the FWH or SPI flash. When this bit is written from a 0 to a 1 and the LE bit is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

eSPI PCR Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4000h	4	eSPI Slave Configuration Register And Link Control (SLV_CFG_REG_CTL)	0h
4004h	4	eSPI Slave Configuration Register Data (SLV_CFG_REG_DATA)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4020h	4	Peripheral Channel Error for Slave 0 (PCERR_SLV0)	0h
4030h	4	Virtual Wire Channel Error for Slave 0 (VWERR_SLV0)	0h
4040h	4	Flash Access Channel Error for Slave 0 (FCERR_SLV0)	0h
4050h	4	Link Error for Slave 0 (LNKERR_SLV0)	FF00h

eSPI Slave Configuration Register And Link Control (SLV_CFG_REG_CTL) – Offset 4000

Along with SLV_CFG_REG_DATA, this register controls Rd/Wr access to Slave Configuration registers using eSPI Get/Set_Configuration, Get_Status and In-Band Reset cycles. It allows Tunneled Access to Slave Configuration (TASC) registers from Host/ME software/firmware.

Bit Range	Default	Access	Field Name and Description
31	0b	RW/1S/V	**Slave Configuration Register Access Enable (SCRE)** Writing a 1 to this field triggers an access (SCRT) to a Slave Config Register ('Go'). Note: Hardware clears this bit to 0 (& sets the SCRS field) when the transaction hascompleted on the eSPI bus. In the case of a configuration/status register read, the datais valid only after this bit has been cleared by HW. Note: The SCRE is effective only if SCRS is clear.

Bit Range	Default	Access	Field Name and Description
30:28	0b	RW/1C/V	**Slave Configuration Register Access Status (SCRS)** This field is set by upon thecompletion of a configuration register access (SCRE). Software must clear this field bywriting all 1s before initiating another Slave configuration register access (SCRE). 0h: Status not valid 1h: Slave No_Response 2h: Slave Response CRC Error 3h: Slave Response Fatal Error 4h: Slave Response Non-Fatal Error 5h – 6h: Reserved 7h: No errors (transaction completed successfully)
27	0b	RW/1S	**IOSF-SB eSPI Link Configuration Lock (SBLCL)** When set, eSPI controller prevents writes (i.e.,SET_CONFIGURATION)to any eSPI Specificationdefined Slave Capabilities and Configuration registers in the reserved register addressrange (0h – 7FFh). Access to Slave implementation specific configuration registersoutside this range are not impacted by this lock bit and are always available – accessprotections to such registers are Slave implementation dependent. Note: This bit cannot be written to 0 once it has been set to 1. It can only be cleared byPLTRST# assertion. The lock is automatically disabled if and while theLNKERR_ SLV0.SLCRR register bit is asserted (upon an eSPI link Fatal Error condition) toallow BIOS (or another SW agent) to attempt to recover the link. Note: This bit has no effect when PLTRST# isasserted. BIOS Note: BIOS must ensure that this bit is set to 1 after initial eSPI link configurationis over to prevent any further (unintentional or malicious) changes to the eSPI link configuration
26:21	-	-	**Reserved**
20:19	0b	RW	**Slave ID (SID)** eSPI Slave ID (CS#) to which the Slave Configuration Register Access (SCRT) is directed. 00: eSPI Slave 0 (EC/BMC) Others: Reserved

Bit Range	Default	Access	Field Name and Description
18	-	-	**Reserved**
17:16	0b	RW	**Slave Configuration Register Access Type (SCRT)** 00: Slave Configuration register read from address SCRA[11:0] (GET_CONFIG 01: Slave Configuration register write to address SCRA[11:0] (SET_CONFIG) 10: Slave Status register read (GET_STATUS) 11: In-Band Reset Note: Writes to Slave Configuration registers in the reserved address range (0h – 7FFh)are gated by the SBLCL bit. Note: Setting this field to 10 triggers a Get_Status command to the Slave. In thiscase, the SCRA field is ignored and only the lower 16-bits of the returned data(SLV_CFG_REG_DATA[15:0]) are valid. Note: Setting this field to 11 triggers an In-Band Reset command to the Slave. In thiscase, the SCRA field is ignored and no data is returned. This command resets the link forthe targeted Slave to a default configuration. Software is responsible for reinitializingthe link to optimized (higher performance) settings using these registers.
15:12	-	-	**Reserved**
11:0	0h	RW	**Slave Configuration Register Address (SCRA)** Per eSPI Spec / eSPI Compatibility Spec.

eSPI Slave Configuration Register Data (SLV_CFG_REG_DATA) – Offset 4004

Along with SLV_CFG_REG_CTL, this register controls Rd/Wr access to Slave Configuration registers using eSPI Get/Set_ Configuration cycles. It allows access to Slave configuration registers from Host/CSME software/firmware.

For writes (SCRT = 2'b01) to Slave Configuration registers, this register should be written to first with the required data before writing to the CTL register. The eSPI-MC processes the write to the Slave using an eSPI Set_Configuration command.

If a write is to a supported register in the reserved register address range (0h 7FFh), the eSPI-MC updates its local copy of the Slave configuration registers after the write has been successfully sent to the Slave.

Note: eSPI-MC does no checking of the register values (even for supported Slave Capabilities / Configuration Registers) the SW assumes full responsibility for programming legal values supported by both the eSPI-MC and the Slave.

For reads (SCRT = 2'b00 or 2b10) to Slave Configuration registers, the hardware writes the data read back from the Slave into this register. The read data is valid after hardware has cleared the SCRE bit in the CTL register and the SCRS field indicates a successful transaction.

Bit Range	Default	Access	Field Name and Description
31:0	0b	RW/V	**Slave Configuration Register for Read and Write data (SCRD)** Configuration register Write data from software or read data from the Slave. For writes, this register must be programmed before the CTL register. For reads, data in this register is valid after the CTL.SCRE bit has been cleared by HWand the CTL.SCRS field indicates a successful transaction.

Peripheral Channel Error for Slave 0 (PCERR_SLV0) – Offset 4020

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
28	0b	RW	**Slave Host Reset Ack Override (SLV_HOST_RST_ACK_OVRD)** A 1 in this bit will cause the eSPI-MC to not wait for theSlave HOST_RESET_ACK Virtual Wire before (immediately) asserting the ResetPrepAck(Host space, GenPrep). The Host_Reset_Warn VW will be transmitted to the Slaveindependent of the setting for this bit.
27:26	0b	RW	**Peripheral Channel Received Master or Target Abort Reporting Enable (PCRMTARE)** 00: Disable RMA or RTA Reporting 01: Reserved 10: Enable RMA or RTA Reporting as SERR 11: Enable RMA or RTA Reporting as SMI Note: SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# isdeasserted. Note: SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted.
25	0b	RW	**Peripheral Channel Unsupported Request Reporting Enable (PCURRE)** If set to 1 bysoftware, it allows reporting of an Unsupported Request (UR) as a System Error (SERR). If eSPI controller decodes a Posted transaction that is not supported, it sets the PCURD bit. If PCCMD.SEE (SERR enable) is also set to 1, then eSPIMCsets the PCSTS.SSE (Signaled System Error) bit and sends a Do_SErr message. Note: If the transaction was a Non-Posted request, then the agent handles thetransaction as an Advisory Non-Fatal error, and no error logging or signaling is done. The Completion with UR Completion Status serves the purpose of error reporting.
24	0b	RW/1C/V	**Peripheral Channel Unsupported Request Detected (PCURD)** Set to 1 by hardwareupon detecting an Unspported Request (UR) that is not considered an Advisory Non-Fatal error and PCERR.PCURRE is set. Cleared to 0 when software writes a 1 to thisregister.
23:15	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
14:13	0b	RW	**Peripheral Channel Non-Fatal Error Reporting Enable (PCNFEE)** 00: Disable Non-Fatal Error Reporting 01: Reserved 10: Enable Non-Fatal Error Reporting as SERR 11: Enable Non-Fatal Error Reporting as SMI Note: SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# isdeasserted. Note: SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. Note: SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
12	0b	RW/1C/V	**Peripheral Channel Non-Fatal Status (PCNFES)** This field is set by hardware if a Non-Fatal Error condition is detected on the Peripheral Channel. Software must clearthis bit. 0: No Non-Fatal Error detected 1: Non-Fatal Error detected (PCNFEC has a non-zero value) Note: Clearing this unlocks the PCNFEC field and triggers a SB Deassert_ SMImessage if PCNFEE is set to SMI. Note: Setting of this bit is independent of the enable to generate a SMI/SERR (PCNFEE)

Bit Range	Default	Access	Field Name and Description
11:8	0b	RO/V	**Peripheral Channel Non-Fatal Cause (PCNFEC)** 0h: No error 1h: Slave Response Code: NONFATAL_ERROR 2h: Slave Response Code: Unsuccessful Completion 3h: Unexpected completion received from Slave (i.e. completion without non-postedrequest or completion with invalid tag or completion with invalid length) 4h: Unsupported Cycle Type (w.r.t. Command) 5h: Unsupported Message Code 6h: Unsupported Address/Length alignment (upstream only): Memory: Address +Length > 64 B (aligned) [for both Posted and Non-Posted transactions] 7h: Unsupported Address/Length alignment (upstream only): Memory: 64-bit Addresswith Addr[63:32] = 0h [for both Posted and Non-Posted transactions] 8h – Fh: Reserved Note: This field is updated after a Peripheral channel transaction is completed if the PCNFES bit is not set.
7	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
6:5	0b	RW	**Peripheral Channel Fatal Error Reporting (PCFEE)** 00: Disable Fatal Error Reporting 01: Reserved 10: Enable Fatal Error Reporting as SERR (IOSF-SB Do_SErr message) 11: Enable Fatal Error Reporting as SMI (IOSF-SB Assert_SMI message) Note: SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# isdeasserted. Note: SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. Note: SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
4	0b	RW/1C/V	**Peripheral Channel Fatal Error Reporting (PCFES)** This field is set by hardware if a FatalError condition is detected on the Peripheral Channel. Software must clear this bit by writing a 1 to it. 0: No Fatal Error detected 1: Fatal Error Type 2 detected (PCFEC has a non-zero value) Note: Clearing this unlocks the PCFEC field and triggers an SB Deassert_ SMImessage if PCFEE is set to SMI. Note: Setting of this bit is independent of the enable to generate a SMI/SERR (PCFEE).

Bit Range	Default	Access	Field Name and Description
3:0	0b	RO/V	**Peripheral Channel Fatal Error Cause (PCFEC)** 0h: No error 1h – 7h: Reserved 8h: Malformed Slave Response Payload: Payload length > Max Payload Size (aligned)[Type 2] 9h: Malformed Slave Response Payload: Read request size > Max Read Request Size(aligned) [Type 2] Ah: Malformed Slave Response Payload: Address + Length > 4KB (aligned) [Type 2] Bh – Fh: Reserved Note: This field is updated after a Peripheral channel transaction is completed if the PCFES bit is not set.

Virtual Wire Channel Error for Slave 0 (VWERR_SLV0) – Offset 4030

This register is used to control error reporting for the eSPI Virtual Wire Channel

Bit Range	Default	Access	Field Name and Description
30:15	-	-	**Reserved**
14:13	0b	RW	**Virtual Wire Channel Non-Fatal Error Reporting Enable (VWNFEE)** 00: Disable Non-Fatal Error Reporting 01: Reserved 10: Enable Non-Fatal Error Reporting as SERR (SB Do_SErr message) 11: Enable Non-Fatal Error Reporting as SMI (SB Assert_SMI message) Note: SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# isdeasserted. Note: SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. Note: SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).

Bit Range	Default	Access	Field Name and Description
12	0b	RW/1C/V	**Virtual Wire Channel Non-Fatal Error Status (VWNFES)** This field is set by hardware ifa Non-Fatal Error condition is detected on the Virtual Wire Channel. Software mustclear this bit. 0: No Non-Fatal Error detected 1: Non-Fatal Error detected (VWNFEC has a non-zero value) Note: Clearing this unlocks the VWNFEC field and triggers an SB Deassert_ SMImessage if VWNFEE is set to SMI. Note: Setting of this bit is independent of the enable to generate a SMI/SERR(VWNFEE).
11:8	0b	RO/V	**Virtual Wire Channel Non-Fatal Error Cause (VWNFEC)** 0h: No error 1h: Slave Response Code: NONFATAL_ERROR 2h – Dh: Reserved Eh: Slave Virtual Wire: NON_FATAL_ERROR: 0 to 1 transition (1 to 0 transition on thisVW is ignored) Fh: Reserved Note: This field is updated after a Virtual Wire Channel transaction is completed if theVWNFES bit is not set.
7	-	-	**Reserved**
6:5	0b	RW	**Virtual Wire Channel Fatal Error Reporting Enable (VWFEE)** 00: Disable Fatal Error Reporting 01: Reserved 10: Enable Fatal Error Reporting as SERR (IOSF-SB Do_SErr message) 11: Enable Fatal Error Reporting as SMI (SB Assert_SMI message) Note: SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# isdeasserted. Note: SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted.Note: SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).

Bit Range	Default	Access	Field Name and Description
4	0b	RW/1C/V	**Virtual Wire Channel Fatal Error Status (VWFES)** This field is set by hardware if a FatalError condition is detected on the Virtual Wire Channel. Software must clear this bit bywriting all 1s to it. 0: No Fatal Error detected 1: Fatal Error Type 2 detected (VWFEC has a non-zero value) Note: Clearing this unlocks the VWFEC field and triggers an SB Deassert_ SMImessage if VWFEE is set to SMI. Note: Setting of this bit is independent of the enable to generate a SMI/SERR (VWFEE).
3:0	0b	RO/V	**Virtual Wire Channel Fatal Error Cause (VWFEC)** 0h: No error 1h – 7h: Reserved 8h: Malformed Slave Response Payload: VW Count > Max. VW Count [Type 2] 9h – 4'hD: Reserved Eh: Slave Virtual Wire: FATAL_ERROR 0 to 1 transition (1 to 0 transition on this VW isignored) [Type 2] Fh: Reserved Note: This field is updated after a Virtual Wire Channel transaction is completed if the VWFES bit is not set.

Flash Access Channel Error for Slave 0 (FCERR_SLV0) – Offset 4040

This register is used to determine how to log and report errors on the Flash Access channel, for both Master and Slave Attached Flash configurations.

Bit Range	Default	Access	Field Name and Description
30:15	-	-	**Reserved**
14:13	0b	RW	**Flash Access Channel Non-Fatal Error Reporting Enable (FCNFEE)** 00: Disable Non-Fatal Error Reporting 01: Reserved 10: Enable Non-Fatal Error Reporting as SERR (SB Do_SErr message) 11: Enable Non-Fatal Error Reporting as SMI (SB Assert_SMI message) Note: SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# isdeasserted. Note: SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. Note: SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
12	0b	RW/1C/V	**Flash Access Channel Non-Fatal Error Status (FCNFES)** This field is set by hardware if aNon-Fatal Error condition is detected on the Flash Access Channel. Software must clearthis bit. 0: No Non-Fatal Error detected 1: Non-Fatal Error detected (FCNFEC has a non-zero value)Note: Clearing this unlocks the FCNFEC field and triggers an SB Deassert_SMImessage if FCNFEE is set to SMI. Note: Setting of this bit is independent of the enable to generate a SMI/SERR (FCNFEE).

Bit Range	Default	Access	Field Name and Description
11:8	0b	RO/V	**Flash Access Channel Non-Fatal Error Cause (FCNFEC)** 0h: No error 1h: Slave Response Code: NONFATAL_ERROR 2h: Slave Response Code: Unsuccessful Completion [for Slave-Attached Flashaccesses only] 3h: Unexpected completion received from Slave (i.e. completion without non-postedrequest or completion with invalid tag or completion with invalid length) [for Slave-Attached Flash accesses only] 2h – 3h: Reserved 4h: Unsupported Cycle Type (w.r.t. Command) 5h: Reserved 6h: Unsupported Address (i.e., address > Flash linear address range) 7h: Reserved 8h – Fh: Reserved Note: This field is updated after a Flash Access Channel transaction is completed if theFCNFES bit is not set
7	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
6:5	0b	RW	**Flash Access Channel Fatal Error Reporting Enable (FCFEE)** 00: Disable Fatal Error Reporting 01: Reserved 10: Enable Fatal Error Reporting as SERR (SB Do_SErr message) 11: Enable Fatal Error Reporting as SMI (SB Assert_SMI message) Note: SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# isdeasserted. Note: SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. Note: SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
4	0b	RW/1C/V	**Flash Access Channel Fatal Error Status (FCFES)** This field is set by hardware if a FatalError condition is detected on the Flash Access Channel. Software must clear this bit by writing a 1 to it. 0: No Fatal Error detected 1: Fatal Error Type 2 detected (FCFEC has a non-zero value) Note: Clearing this unlocks the FCFEC field and triggers an IOSF-SB Deassert_ SMImessage if FCFEE is set to SMI. Note: Setting of this bit is independent of the enable to generate a SMI/SERR (FCFEE).

Bit Range	Default	Access	Field Name and Description
3:0	0b	RO/V	**Flash Access Channel Fatal Error Cause (FCFEC)** 0h: No error 1h – 7h: Reserved 8h: Malformed Slave Response Payload: Payload length > Max Payload Size [Type 2] 9h: Malformed Slave Response Payload: Read request size > Max Read Request Size[for Master-Attached Flash accesses only] [Type 2] Ah – Fh: Reserved Note: This field is updated after a Flash Access Channel transaction is completed if theFCFES bit is not set.

Link Error for Slave 0 (LNKERR_SLV0) – Offset 4050

This register is used to control link error reporting for the eSPI Slave 0.

Bit Range	Default	Access	Field Name and Description
31	0b	RW/1C/V	**eSPI Link and Slave Channel Recovery Required (SLCRR)** HW sets this bit when it has detected a Type 1 Fatal Error condition, for any channel (LFET1C is non-zero). Setting of this bit will trigger an error handling sequence by the eSPI-MC, followed by the suspension of all HW initiated transactions on the eSPI link with the Slave. SW must clear this bit (by writing a 1 to it) after it has taken all necessary actions to recover the link. This indicates the eSPI-MC to resume HW initiated transactions with the Slave.
30:23	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
22:21	0b	RW	**Fatal Error Type 1 Reporting Enable (LFET1E)** 00: Disable Fatal Error Type 1 Reporting 01: Reserved 10: Enable Fatal Error Type 1 Reporting as SERR (IOSF-SB Do_SErr message) 11: Enable Fatal Error Type 1 Reporting as SMI (IOSF-SB Assert_SMI message) Notes: 1. SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. 2. SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. 3. SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted). 4. When this error is reported, SW must also inspect and handle the SLCRR field.
20	0b	RW/1C/V	**Fatal Error Type 1 Reporting Status (LFET1S)** This field is set by hardware if a Link Fatal Error Type 1 condition is detected on the eSPI link (any transaction). Software must clear this bit by writing a 1 to it. 0: No Link Fatal Error Type 1 detected 1: Fatal Error Type 1 detected (LFET1C has a non-zero value) Note: 1. Clearing this unlocks the LFET1C field and triggers an IOSF-SB Deassert_SMI message if LFET1E is set to SMI. 2. Setting of this bit is independent of the enable to generate a SMI/SERR (LFET1E).

Bit Range	Default	Access	Field Name and Description
19:16	0h	RO/V	**Link Fatal Type 1 cause (LFET1C)** 4'h0: No error 4'h1: Slave Response Code: NO_RESPONSE [Type 1] 4'h2: Slave Response Code: FATAL_ERROR [Type 1] 4'h3: Slave Response Code: CRC_ERROR [Type 1] 4'h4: Invalid Slave Response Code (w.r.t. to Command) [Type 1] 4'h5: Invalid Slave Cycle Type (w.r.t. to Command) [Type 1] 4'h6 - 4'hF: Reserved Note: 1. This field is updated after a transaction (any channel) is completed if the LFET1S bit is clear. 2. A non-zero value in this field also causes the SLCRR bit to be set.
15:8	FFh	RO/V	**Link Fatal Error Type 1 Cycle Type (LFET1CTYP)** When LFET1C is set, this field reflects the Cycle Type for the transaction that encountered the Fatal Error Type 1. If no valid Cycle Type exists w.r.t. the Command (LFET1CMD), this field is set to 8hFF to indicate that it should be ignored. Note: This field is updated after a transaction (any channel) is completed if the LFET1S bit is clear.
7:0	0h	RO/V	**Link Fatal Error Type 1 Command (LFET1CMD)** When LFET1C is set, this field reflects the Command for the transaction that encountered the Fatal Error Type 1. Note: This field is updated after a transaction (any channel) is completed if the LFET1S bit is clear.

FIA Configuration PCR Registers

These registers are within the PCH Private Configuration Space which is accessiblethrough the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID+ Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Common Control (CC)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
100h	4	PCIe* Device Reference Clock Request Mapping 1 (DRCRM1)	A418820h
104h	4	PCIe* Device Reference Clock Request Mapping 2 (DRCRM2)	16A4A0E6h
108h	4	Device Reference Clock Request Mapping 3 (DRCRM3)	7B9ACh
200h	4	Strap Configuration 1 (STRPFUSECFG1)	0h
250h	4	HSIO Lane Owner Status 1 (LOS1)	0h
254h	4	HSIO Lane Owner Status 2 (LOS2)	0h

Common Control (CC) – Offset 0

Bit Range	Default	Access	Field Name and Description
31	0b	RW/O	**Secured Register Lock (SRL)** When this bit is set, all the secured registers will be locked and will be Read-Only.
30:18	-	-	**Reserved**
17	0b	RW	**Partition/Trunk Oscillator Clock Gating Enable (PTOCGE)** When set, the oscillator and side clock will be dynamically clock gated when the conditions to clock gate are met. When clear, the oscillator and side clock will never be dynamically clock gated.
16	0b	RW	**Oscillator/Side Clock Dynamic Clock Gating Enable (OSCDCGE)** When set, the oscillator and side clock will be dynamically clock gated when the conditions to clock gate are met. When clear, the oscillator and side clock will never be dynamically clock gated.
15	0b	RW	**Side Clock Partition/Trunk Clock Gating Enable (SCPTCGE)** When set, the Side Clock will be clock gated at the partition/trunk level when the conditions to clock gate are met. When clear, the Side Clock will never be clock gated at the partition/trunk level.

Bit Range	Default	Access	Field Name and Description
14:0	-	-	**Reserved**

PCIe* Device Reference Clock Request Mapping 1 (DRCRM1) – Offset 100

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29:25	00101b	RW/L	**PCIe Express Port 6 CLKREQ Mapping ()** Same description as bit [4:0], except that this field applies to PCIe Port 6.
24:20	00100b	RW/L	**PCI Express Port 5 CLKREQ Mapping ()** Same description as bit [4:0], except that this field applies to PCIe Port 5.
19:15	00011b	RW/L	**PCI Express Port 4 CLKREQ Mapping ()** Same description as bit [4:0], except that this field applies to PCIe Port 4.
14:10	00010b	RW/L	**PCI Express Port 3 CLKREQ Mapping ()** Same description as bit [4:0], except that this field applies to PCIe Port 3.
9:5	00001b	RW/L	**PCI Express Port 2 CLKREQ Mapping ()** Same description as bit [4:0], except that this field applies to PCIe Port 2.

Bit Range	Default	Access	Field Name and Description
4:0	00000b	RW/L	**PCI Express Port 1 CLKREQ Mapping ()** The mapping of PCIe Port 1 to the corresponding CLKREQ# pin is configured by this field. 00h: Port 1 maps to CLKREQ0# pin. 01h: Port 1 maps to CLKREQ1# pin. ... 05h: Port 1 maps to CLKREQ5# pin. Others: Reserved Software must never map multiple PCIe Ports to the same CLKREQ# pin. The hardware behavior is undefined if this ever happens. Note:This field must be configured prior to enabling any power management features. Note: Configuring this field to map to any unsupported CLKREQ# pins may result in undefined hardware behavior. This register bit is Read-Only when the CC.SRL bit is set. Register Attribute: Static.

PCIe* Device Reference Clock Request Mapping 2 (DRCRM2) – Offset 104

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29:25	01011b	RW/L	**PCI Express Port 12 CLKREQ Mapping ()** Same description as bit [4:0], except that this field applies to PCIe Port 12.
24:20	01010b	RW/L	**PCI Express Port 11 CLKREQ Mapping ()** Same description as bit [4:0], except that this field applies to PCIe Port 11.
19:15	01001b	RW/L	**PCI Express Port 10 CLKREQ Mapping ()** Same description as bit [4:0], except that this field applies to PCIe Port 10.
14:10	01000b	RW/L	**PCI Express Port 9 CLKREQ Mapping ()** Same description as bit [4:0], except that this field applies to PCIe Port 9.
9:5	00111b	RW/L	**PCI Express Port 8 CLKREQ Mapping ()** Same description as bit [4:0], except that this field applies to PCIe Port 8.
4:0	00110b	RW/L	

Bit Range	Default	Access	Field Name and Description
			PCI Express Port 7 CLKREQ Mapping () The mapping of PCIe Port 7 to the corresponding CLKREQ# pin is configured by this field. 00h: Port 7 maps to CLKREQ0# pin. 01h: Port 7 maps to CLKREQ1# pin. ... 05h: Port 7 maps to CLKREQ5# pin. Others: Reserved Software must never map multiple PCIe Ports to the same CLKREQ# pin. The hardware behavior is undefined if this ever happens. Note:This field must be configured prior to enabling any power management features. Note: Configuring this field to map to any unsupported CLKREQ# pins may result in undefined hardware behavior. This register bit is Read-Only when the CC.SRL bit is set. Register Attribute: Static.

Device Reference Clock Request Mapping 3 (DRCRM3) – Offset 108

Bit Range	Default	Access	Field Name and Description
30:20	-	-	**Reserved**
19:15	01111b	RW/L	**PCI Express Port 16 CLKREQ Mapping ()** Same description as bit [4:0], except that this field applies to PCIe Port 16.
14:10	01110b	RW/L	**PCI Express Port 15 CLKREQ Mapping ()** Same description as bit [4:0], except that this field applies to PCIe Port 15.

Bit Range	Default	Access	Field Name and Description
9:5	01101b	RW/L	**PCI Express Port 14 CLKREQ Mapping ()** Same description as bit [4:0], except that this field applies to PCIe Port 14.
4:0	01100b	RW/L	**PCI Express Port 13 CLKREQ Mapping ()** The mapping of PCIe Port 13 to the corresponding CLKREQ# pin is configured by this field. 00h: Port 13 maps to CLKREQ0# pin. 01h: Port 13 maps to CLKREQ1# pin. ... 05h: Port 13 maps to CLKREQ5# pin. Others: Reserved Software must never map multiple PCIe Ports to the same CLKREQ# pin. The hardware behavior is undefined if this ever happens. Note:This field must be configured prior to enabling any power management features. Note: Configuring this field to map to any unsupported CLKREQ# pins may result in undefined hardware behavior. This register bit is Read-Only when the CC.SRL bit is set. Register Attribute: Static.

Strap Configuration 1 (STRPFUSECFG1) – Offset 200

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31	0b	RO/V	**GbE Over PCI Express Port Enable Strap (GBE_PCIE_PEN)** 0 : GbE MAC/PHY port communication is not enabled over PCI Express. 1 : The PCI Express port will be used for GbE MAC/PHY over PCI Express communication. Note: This field is only applicable if GbE is supported, otherwise this will be RO Reserved bit.
30:28	000b	RO/V	**GBE PCIe Port Select Strap (GBE_PCIEPORTSEL)** Used to determine which PCIe port to be used for GbE MAC/PHY over PCI Express communication. 000: Port 3. 001: Port 4. 010: Port 5. 011: Port 9. 100: Port 10. Others: Reserved.
27:24	-	-	**Reserved**
23:8	0000h	RO/V	**PCIe/SATA Combo Port Select Polarity (PSCPSP)** 0: When the Combo Port Select pin is '0, PCIe mode is selected. When the Combo Port Select pin is '1, SATA mode is selected. 1: When the Combo Port Select pin is '0, SATA mode is selected. When the Combo Port Select pin is '1, PCIe mode is selected. This field is expected to be set to '1 when the combo port is mapped to M.2 or SATAe connector and set to '0 when the combo port is mapped to mSATA connector.

Bit Range	Default	Access	Field Name and Description
7:2	-	-	**Reserved**
1	0b	RO/V	**Core Dynamic Clock Gating Disable (CDCGDIS)** 0: Core dynamic clock gating enabled. 1: Core dynamic clock gating disabled. This affects clock gating in SATA, DMI, PCIe, PMC, Audio, LAN, and SMBUS.
0	0b	RO/V	**HSIO Power Gating Disabled (MPGD)** 0b: HSIO power gating capability is enabled. 1b: HSIO power gating capability is disabled.

HSIO Lane Owner Status 1 (LOS1) – Offset 250

Bit Range	Default	Access	Field Name and Description
31:28	0h	RO/V	**Lane 7 Owner (L7O)** This register indicates the lane owner for Lane 7 Same description as bits [3:0].
27:24	0h	RO/V	**Lane 6 Owner (L6O)** This register indicates the lane owner for Lane 6 Same description as bits [3:0].
23:20	0h	RO/V	**Lane 5 Owner (L5O)** This register indicates the lane owner for Lane 5 Same description as bits [3:0].
19:16	0h	RO/V	**Lane 4 Owner (L4O)** This register indicates the lane owner for Lane 4 Same description as bits [3:0].

Bit Range	Default	Access	Field Name and Description
15:12	0h	RO/V	**Lane 3 Owner (L3O)** This register indicates the lane owner for Lane 3 Same description as bits [3:0].
11:8	0h	RO/V	**Lane 2 Owner (L2O)** This register indicates the lane owner for Lane 2 Same description as bits [3:0].
7:4	0h	RO/V	**Lane 1 Owner (L1O)** This register indicates the lane owner for Lane 1 Same description as bits [3:0].
3:0	0h	RO/V	**Lane 0 Owner (L0O)** This register indicates the lane owner for Lane 0. 0000: PCIe/DMI. 0001: USB3.1. 0010: SATA. 0011: GbE. Others: Reserved.

HSIO Lane Owner Status 2 (LOS2) – Offset 254

Bit Range	Default	Access	Field Name and Description
31:28	0h	RO/V	**Lane 15 Owner (L15O)** This register indicates the lane owner for Lane 15 Same description as bits [3:0].
27:24	0h	RO/V	**Lane 14 Owner (L14O)** This register indicates the lane owner for Lane 14 Same description as bits [3:0].

Bit Range	Default	Access	Field Name and Description
23:20	0h	RO/V	**Lane 13 Owner (L13O)** This register indicates the lane owner for Lane 13 Same description as bits [3:0].
19:16	0h	RO/V	**Lane 12 Owner (L12O)** This register indicates the lane owner for Lane 12 Same description as bits [3:0].
15:12	0h	RO/V	**Lane 11 Owner (L11O)** This register indicates the lane owner for Lane 11 Same description as bits [3:0].
11:8	0h	RO/V	**Lane 10 Owner (L10O)** This register indicates the lane owner for Lane 10 Same description as bits [3:0].
7:4	0h	RO/V	**Lane 9 Owner (L9O)** This register indicates the lane owner for Lane 9 Same description as bits [3:0].
3:0	0h	RO/V	**Lane 8 Owner (L8O)** This register indicates the lane owner for Lane 8. 0000: PCIe/DMI. 0001: USB3.1. 0010: SATA. 0011: GbE. Others: Reserved.

GbE Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	GbE Vendor and Device Identification Register (GBE_VID_DID)	15B78086h
4h	4	PCI Command & Status Register (PCICMD_STS)	100000h
8h	4	Revision Identification & Class Code Register (RID_CC)	20000XXh
ch	4	Cache Line Size Primary Latency Timer & Header Type Register (CLS_PLT_HEADTYP)	0h
10h	4	Memory Base Address Register A (MBARA)	0h
2ch	4	Subsystem Vendor & Subsytem ID (DMI_CONFIG11)	8086h
30h	4	Expansion ROM Base Address Register (ERBA)	0h
34h	4	Capabilities List Pointer Register (CAPP)	C8h
3ch	4	Interrupt Information & Maximum Latency/Minimum GrantRegister (INTR_MLMG)	100h
a0h	4	LAN Disable Control (LANDISCTRL)	0h
a4h	4	Lock LAN Disable (LOCKLANDIS)	0h
a8h	4	System Time Control High Register (LTRCAP)	0h
c8h	4	Capabilities List and Power Managment Capabilities Register (CLIST1_PMC)	23D001h
cch	4	PCI Power Management Control Status & Data Register (PMCS_DR)	0h
d0h	4	Capabilities List 2 & Message Control Register (CLIST2_MCTL)	80E005h
d4h	4	Message Address Low Register (MADDL)	0h
d8h	4	Message Address High Register (MADDH)	0h
dch	4	Message Data Register (MDAT)	0h

GbE Vendor and Device Identification Register (GBE_VID_DID) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:16	0x15b7	RW/V	**Device ID (DID)** This is a 16-bit value assigned to the PCH Gigabit LAN controller. The field may beauto-loaded from the NVM word 0Dh during initialization time depending on the “Load Vendor/Device ID” bit field in NVM word 0Ah.
15:0	0x8086	RW/V	**Vendor ID (VID)** This is a 16-bit value assigned to Intel. The field may be auto-loaded from theNVM at address 0Dh during INIT time depending on the “Load Vendor/Device ID” bit field in NVMword 0Ah with a default value of 8086h.

PCI Command & Status Register (PCICMD_STS) – Offset 4

Bit Range	Default	Access	Field Name and Description
31	0x0	RW/V	**Detected Parity Error (DPE)** 0 = No parity error detected. 1 = Set when the Gb LAN controller receives a command or data from the backbone with a parityerror. This is set even if PCIMD.PER (D25:F0, bit 6) is not set.
30	0x0	RW/V	**Signaled System Error (SSE)** 0 = No system error signaled. 1 = Set when the Gb LAN controller signals a system error to the internal SERR# logic.
29	0x0	RW/V	**Received Master Abort (RMA)** 0 = Root port has not received a completion with unsupported request status from the backbone. 1 = Set when the GbE LAN controller receives a completion with unsupported request status fromthe backbone.
28	0x0	RW/V	**Received Target Abort (RTA)** 0 = Root port has not received a completion with completer abort from the backbone. 1 = Set when the Gb LAN controller receives a completion with completer abort from the backbone.

Bit Range	Default	Access	Field Name and Description
27	0x0	RW/V	**Signaled Target Abort (STA)** 0 = No target abort received. 1 = Set whenever the Gb LAN controller forwards a target abort received from the downstreamdevice onto the backbone.
26:25	0x0	RW/V	**DEVSEL# Timing Status (DEV_STS)** Hardwired to 0.
24	0x0	RW/V	**Master Data Parity Error Detected (DPED)** 0 = No data parity error received. 1 = Set when the Gb LAN Controller receives a completion with a data parity error on the backboneand PCIMD.PER (D25:F0, bit 6) is set.
23	0x0	RW/V	**Fast Back to Back Capable (FB2BC)** Hardwired to 0.
22	-	-	**Reserved**
21	0x0	RW/V	**66 MHz Capable ()** Hardwired to 0.
20	0x1	RW/V	**Capabilities List ()** Hardwired to 1. Indicates the presence of a capabilities list.
19	0x0	RW/V	**Interrupt Status ()** Indicates status of hot-plug and power management interrupts on the rootport that result in INTx# message generation. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state ofPCICMD.Interrupt Disable bit (D25:F0:04h:bit 10).

Bit Range	Default	Access	Field Name and Description
18:11	-	-	**Reserved**
10	0x0	RW	**Interrupt Disable (INT_DIS)** This disables pin-based INTx# interrupts on enabled hot-plug and powermanagement events. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt for hot-plug or power management and MSI is not enabled. 1 = Internal INTx# messages will not be generated. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTxand de-assert_INTx messages will still be forwarded to the internal interrupt controllers if this bit isset.
9	0x0	RW/V	**Fast Back to Back Enable (FBE)** Hardwired to 0.
8	0x0	RW	**SERR# Enable (SEE)** 0 = Disable 1 = Enables the Gb LAN controller to generate an SERR# message when PSTS.SSE is set.
7	0x0	RW/V	**Wait Cycle Control (WCC)** Hardwired to 0.
6	0x0	RW	**Parity Error Response (PER)** 0 = Disable. 1 = Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0x0	RW/V	**Palette Snoop Enable (PSE)** Hardwired to 0.

Bit Range	Default	Access	Field Name and Description
4	0x0	RW/V	**Postable Memory Write Enable (PMWE)** Hardwired to 0.
3	0x0	RW/V	**Special Cycle Enable (SCE)** Hardwired to 0.
2	0x0	RW	**Bus Master Enable (BME)** 0 = Disable. All cycles from the device are master aborted 1 = Enable. Allows the root port to forward cycles onto the backbone from a Gigabit LAN device.
1	0x0	RW	**Memory Space Enable (MSE)** 0 = Disable. Memory cycles within the range specified by the memory base and limit registers aremaster aborted on the backbone. 1 = Enable. Allows memory cycles within the range specified by the memory base and limitregisters can be forwarded to the Gigabit LAN device.
0	0x0	RW/V	**I/O Space Enable (IOSE)** This bit controls access to the I/O space registers. 0 = Disable. I/O cycles within the range specified by the I/O base and limit registers are masteraborted on the backbone. 1 = Enable. Allows I/O cycles within the range specified by the I/O base and limit registers can beforwarded to the Gigabit LAN device.

Revision Identification & Class Code Register (RID_CC) – Offset 8

Bit Range	Default	Access	Field Name and Description
31:8	0x20000	RW/V	**Class Code ()** Identifies the device as an Ethernet Adapter. 020000h = Ethernet Adapter.

Bit Range	Default	Access	Field Name and Description
7:0	See Description	RW/V	**Revision ID ()** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

Cache Line Size Primary Latency Timer & Header Type Register (CLS_PLT_HEADTYP) – Offset c

Bit Range	Default	Access	Field Name and Description
31:24	0x0	RW/V	**Reserved ()**
23:16	0x0	RW/V	**Header Type (HT)** 00h = Indicates this is a single function device.
15:8	0x0	RW/V	**Latency Timer (LT)** Hardwired to 0.
7:0	0x0	RW/V	**Cache Line Size (CLS)** This field is implemented by PCI devices as a read/write field for legacycompatibility purposes but has no impact on any device functionality.

Memory Base Address Register A (MBARA) – Offset 10

Bit Range	Default	Access	Field Name and Description
31:17	0x0	RW	**Base Address (BA)** Software programs this field with the base address of this region.
16:4	0x0	RW/V	**Memory Size (MSIZE)** Memory size is 128KB.
3	0x0	RW/V	**Prefetchable Memory (PM)** The GbE LAN controller does not implement prefetchablememory.

Bit Range	Default	Access	Field Name and Description
2:1	0x0	RW/V	**Memory Type (MT)** Set to 00b indicating a 32-bit BAR.
0	0x0	RW/V	**Memory/I/O Space (MIOS)** Set to 0 indicating a Memory Space BAR.

Subsystem Vendor & Subsytem ID (DMI_CONFIG11) – Offset 2c

Bit Range	Default	Access	Field Name and Description
31:16	0x0	RW/V	**Subsystem ID (SID)** This value may be loaded automatically from the NVM Word 0Bh uponpower up or reset depending on the “Load Subsystem ID” bit field in NVM word 0Ah with a defaultvalue of 0000h. This value is loadable from NVM word location 0Ah.
15:0	0x8086	RW/V	**Subsystem Vendor ID (SVID)** This value may be loaded automatically from the NVM Word0Ch upon power up or reset depending on the “Load Subsystem ID” bit field in NVM word 0Ah. Avalue of 8086h is default for this field upon power up if the NVM does not respond or is notprogrammed. All functions are initialized to the same value.

Expansion ROM Base Address Register (ERBA) – Offset 30

Bit Range	Default	Access	Field Name and Description
31:0	0x0	RW/V	**Expansion ROM Base Address (ERBA)** This register is used to define the address and sizeinformation for boot-time access to the optional FLASH memory. If no Flash memory exists, thisregister reports 00000000h.

Capabilities List Pointer Register (CAPP) – Offset 34

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	0xc8	RW/V	**Capabilities Pointer (PTR)** Indicates that the pointer for the first entry in the capabilities listis at C8h in configuration space.

Interrupt Information & Maximum Latency/Minimum GrantRegister (INTR_MLMG) – Offset 3c

Bit Range	Default	Access	Field Name and Description
31:24	0x0	RW/V	**Maximum Latency (ML)** Not used. Hardwired to 00h.
23:16	0x0	RW/V	**Minimum Grant (MG)** Not used. Hardwired to 00h.
15:8	0x1	RW/V	**Interrupt Pin (IPIN)** Indicates the interrupt pin driven by the GbE LAN controller.01h = The GbE LAN controller implements legacy interrupts on INTA.
7:0	0x0	RW	**Interrupt Line (ILINE)** Default = 00h. Software written value indicates which interrupt line(vector) the interrupt is connected. No hardware action is taken on this register.

LAN Disable Control (LANDISCTRL) – Offset a0

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0x0	RW	**LAN Disable (LD)** Setting this bit to 1 will disable the LAN Controllerfunctionality.

Lock LAN Disable (LOCKLANDIS) – Offset a4

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0x0	RW	**Lock LAN Disable (LLD)** When set this bit blocks writes to the LANDISCTRL register.Note: Once set this bit will only be cleared on host reset.

System Time Control High Register (LTRCAP) – Offset a8

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**
28:26	0x0	RW	**Maximum Non-Snoop Latency Scale (MNSLS)** Provides a scale for the value containedwithin the Maximum Non-Snoop Latency Value field. 000b = Value times 1 ns 001b = Value times 32 ns 010b = Value times 1,024 ns 011b = Value times 32,768 ns 100b = Value times 1,048,576 ns 101b = Value times 33,554,432 ns 110b–111b = Reserved
25:16	0x0	RW	**Maximum Non-Snoop Latency (MNSL)** Specifies the maximum non-snoop latency that adevice is permitted to request. Software should set this to the platform's maximum supportedlatency or less. This field is also an indicator of the platforms maximum latency, should an endpoint send up LTRLatency Values with the Requirement bit not set.

Bit Range	Default	Access	Field Name and Description
15:13	-	-	**Reserved**
12:10	0x0	RW	**Maximum Snoop Latency Scale (MSLS)** Provides a scale for the value contained withinthe Maximum Snoop Latency Value field. 000b = Value times 1 ns 001b = Value times 32 ns 010b = Value times 1,024 ns 011b = Value times 32,768 ns 100b = Value times 1,048,576 ns 101b = Value times 33,554,432 ns 110b–111b = Reserved
9:0	0x0	RW	**Maximum Snoop Latency (MSL)** Specifies the maximum snoop latency that a device ispermitted to request. Software should set this to the platform's maximum supported latency or less.This field is also an indicator of the platforms maximum latency, should an endpoint send up LTRLatency Values with the Requirement bit not set.

Capabilities List and Power Managment Capabilities Register (CLIST1_PMC) – Offset c8

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:27	0x0	RW/V	**PME_SUPPORT (PMES)** This five-bit field indicates the power states in which the function mayassert PME#. It depend on PM Ena and AUX-PWR bits in word 0Ah in the NVM: Condition Functionality Value PM Ena=0 No PME at all states 0000b PM Ena and AUX-PWR=0 PME at D0 and D3HOT 01001b PM Ena and AUX-PWR=1 PME at D0, D3HOT and D3COLD 11001b These bits are not reset by Function Level Reset.
26	0x0	RW/V	**D2_SUPPORT (D2S)** The D2 state is not supported.
25	0x0	RW/V	**D1_SUPPORT (D1S)** The D1 state is not supported.
24:22	0x0	RW/V	**AUX_CURRENT (AC)** Required current defined in the Data register.
21	0x1	RW/V	**Device Specific Initialization (DSI)** Set to 1. The GbE LAN Controller requires its devicedriver to be executed following transition to the D0 un-initialized state.
20	-	-	**Reserved**
19	0x0	RW/V	**PME Clock (PMEC)** Hardwired to 0.
18:16	011b	RW/V	**Version (VER)** Hardwired to 010b to indicate support for Revision 1.1 of the PCI PowerManagement Specification.
15:8	0xd0	RW/V	**Next Capability (NEXT)** Value of D0h indicates the location of the next pointer.
7:0	0x1	RW/V	**Capability ID (CID)** Indicates the linked list item is a PCI Power Management Register.

PCI Power Management Control Status & Data Register (PMCS_DR) – Offset cc

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15	0x0	RW/V	**PME STATUS (PMES)** This bit is set to 1 when the function detects a wake-up eventindependent of the state of the PMEE bit. Writing a 1 will clear this bit.
14:13	0x0	RW/V	**DATA SCALE (DSC)** This field indicates the scaling factor to be used when interpreting thevalue of the Data register. For the GbE LAN and common functions this field equals 01b (indicating 0.1 watt units) if the PM isenabled in the NVM, and the Data_Select field is set to 0, 3, 4, 7, (or 8 for Function 0). Otherwise, itequals 00b. For the manageability functions, this field equals 10b (indicating 0.01 watt units) if the PM isenabled in the NVM, and the Data_Select field is set to 0, 3, 4, 7. Otherwise, it equals 00b.
12:9	0x0	RW	**Data Select (DSL)** This four-bit field is used to select which data is to be reported throughthe Data register (offset CFh) and Data_Scale field. These bits are writeable only when PowerManagement is enabled using NVM. 0h = D0 Power Consumption 3h = D3 Power Consumption 4h = D0 Power Dissipation 7h = D3 Power Dissipation 8h = Common Power All other values are reserved.
8	0x0	RW	**PME Enable (PMEE)** If Power Management is enabled in the NVM, writing a 1 to this bit willenable Wakeup. If Power Management is disabled in the NVM, writing a 1 to this bit has no affect,and will not set the bit to 1. This bit is not reset by Function Level Reset.
7:2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1:0	0x0	RW/V	**Power State (PS)** This field is used both to determine the current power state of the GbE LAN Controller and to set a new power state. The values are: 00 = D0 state (default) 01 = Ignored 10 = Ignored 11 = D3 state (Power Management must be enabled in the NVM or this cycle will be ignored).

Capabilities List 2 & Message Control Register (CLIST2_MCTL) – Offset d0

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0x1	RW/V	**64-bit Capable (64BC)** Set to 1 to indicate that the GbE LAN Controller is capable ofgenerating 64-bit message addresses.
22:20	0x0	RW/V	**Multiple Message Enable (MME)** Returns 000b to indicate that the GbE LAN controller only supports a single message.
19:17	0x0	RW/V	**Multiple Message Capable (MMC)** The GbE LAN controller does not support multiplemessages.
16	0x0	RW	**Message Signal Interrupt Enable (MSIE)** 0 = MSI generation is disabled. 1 = The Gb LAN controller will generate MSI for interrupt assertion instead of INTx signaling.

Bit Range	Default	Access	Field Name and Description
15:8	0xe0	RW/V	**Next Capability (NEXT)** Value of E0h points to the Function Level Reset capability structure. These bits are not reset by Function Level Reset.
7:0	0x5	RW/V	**Capability ID (CID)** Indicates the linked list item is a Message Signaled Interrupt Register.

Message Address Low Register (MADDL) – Offset d4

Bit Range	Default	Access	Field Name and Description
31:2	0x0	RW/V	**Message Address Low (MADDL)** These bits combine with MADDL2 to create one 32 bit field which is written by the system to indicate the lower 32 bits of theaddress to use for the MSI memory write transaction.
1:0	0x0	RW/V	**Message Address Low 2 (MADDL2)** These bits combine with MADDL to create one 32 bit field which is written by the system to indicate the lower 32 bits of theaddress to use for the MSI memory write transaction. These lower two bits will always return 0.

Message Address High Register (MADDH) – Offset d8

Bit Range	Default	Access	Field Name and Description
31:0	0x0	RW	**Message Address High (MADDH)** Written by the system to indicate the upper 32 bits ofthe address to use for the MSI memory write transaction.

Message Data Register (MDAT) – Offset dc

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0x0	RW	**Message Data (MDAT)** Written by the system to indicate the lower 16 bits of the datawritten in the MSI memory write DWord transaction. The upper 16 bits of the transaction are writtenas 0000h.

GbE Memory Mapped I/O Registers

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Gigabit Ethernet Capabilities and Status (GBECSR_00)	0h
18h	4	Gigabit Ethernet Capabilities and Status (GBECSR_18)	0h
20h	4	Gigabit Ethernet Capabilities and Status (GBECSR_20)	10000000h
f00h	4	Gigabit Ethernet Capabilities and Status (GBECSR_F00)	0h
f10h	4	Gigabit Ethernet Capabilities and Status F10 (GBECSR_F10)	Ch
5400h	4	Gigabit Ethernet Capabilities and Status (GBECSR_5400)	0h
5404h	4	Gigabit Ethernet Capabilities and Status (GBECSR_5404)	0h
5800h	4	Gigabit Ethernet Capabilities and Status (GBECSR_5800)	0h
5b54h	4	Gigabit Ethernet Capabilities and Status (GBECSR_5B54)	0h

Gigabit Ethernet Capabilities and Status (GBECSR_00) – Offset 0

Bit Range	Default	Access	Field Name and Description
30:25	-	-	**Reserved**
24	0x0	RW	**PHY Power Down (PHYPDN)** When cleared (0b), the PHY power down setting is controlled by the internal logic of PCH.
23:0	-	-	**Reserved**

Gigabit Ethernet Capabilities and Status (GBECSR_18) – Offset 18

Bit Range	Default	Access	Field Name and Description
30:21	-	-	**Reserved**
20	0x0	RW	**PHY Power Down Enable (PHYPDEN)** When set, this bit enables the PHY to enter a low-power state when the LAN controller is at the DMOff/D3 or with no WOL.
19:0	-	-	**Reserved**

Gigabit Ethernet Capabilities and Status (GBECSR_20) – Offset 20

Bit Range	Default	Access	Field Name and Description
31	0x0	RW/V	**Wait ()** Set to 1 by the Gigabit Ethernet Controller to indicate that a PCI Express* to SMBus transition is taking place. The ME/Host should not issue new MDIC transactions while this bit is set to 1. This bit is auto cleared by hardware after the transition has occurred.

Bit Range	Default	Access	Field Name and Description
30	0x0	RW/V	**Error ()** Set to 1 by the Gigabit Ethernet Controller when it fails to complete an MDI read.Software should make sure this bit is clear before making an MDI read or write command.
29	0x0	RW/V	**Interrupt Enable (IE)** When set to 1 by software, it will causean Interrupt to be asserted to indicate the end of an MDI cycle.
28	0x1	RW/V	**Ready Bit (RB)** Set to 1 by the Gigabit Ethernet Controller at the end of the MDItransaction. This bit should be reset to 0 by software at the same time the command is written.
27:26	0x0	RW/V	**MDI Type ()** [br[01 = MDI Write 10 = MDI Read All other values are reserved.
25:21	0x0	RW/V	**LAN Connected Device Address (PHYADD)**
20:16	0x0	RW/V	**LAN Connected Device Register Address (REGADD)**
15:0	0x0	RW/V	**DATA ()** In a Write command, software places the data bits and the MAC shifts them out to the LAN Connected Device. In a Read command, the MAC reads these bits serially from theLAN Connected Device and software can read them from this location.

Gigabit Ethernet Capabilities and Status (GBECSR_F00) – Offset f00

Bit Range	Default	Access	Field Name and Description
30:6	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
5	0x0	RW/V	**Software Semaphore FLAG (SWFLAG)** This bit is set by the device driver to gain accesspermission to shared CSR registers with the firmware and hardware.
4:0	-	-	**Reserved**

Gigabit Ethernet Capabilities and Status F10 (GBECSR_F10) – Offset f10

Bit Range	Default	Access	Field Name and Description
30:7	-	-	**Reserved**
6	0x0	RW	**Global GbE Disable (GGD)** Prevents the PHY from auto-negotiating 1000Mb/s link in all power states.
5:4	-	-	**Reserved**
3	0x1	RW	**GbE Disable at non D0a— ()** Prevents the PHY from auto-negotiating 1000Mb/s link in all power states except D0a. This bit must be set since GbE is not supported in Sx states.
2	0x1	RW	**LPLU in non D0a (LPLUND)** Enables the PHY to negotiate for the slowest possible linkin all power states except D0a.
1	0x0	RW	**LPLU in D0a (LPLUD)** Enables the PHY to negotiate for the slowest possible link in allpower states. This bit overrides bit 2.
0	-	-	**Reserved**

Gigabit Ethernet Capabilities and Status (GBECSR_5400) – Offset 5400

Bit Range	Default	Access	Field Name and Description
31:0	0x0	RW	**Receive Address Low (RAL)** The lower 32 bits of the 48-bit Ethernet Address.

Gigabit Ethernet Capabilities and Status (GBECSR_5404) – Offset 5404

Bit Range	Default	Access	Field Name and Description
31	0x0	RW	**Address Valid (AV)**
30:16	-	-	**Reserved**
15:0	0x0	RW	**Receive Address High (RAH)** The lower 16 bits of the 48-bit Ethernet Address.

Gigabit Ethernet Capabilities and Status (GBECSR_5800) – Offset 5800

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0x0	RW	**Advanced Power Management Enable (APME)** [br[1 = APM Wakeup is enabled 0 = APM Wakeup is disabled

Gigabit Ethernet Capabilities and Status (GBECSR_5B54) – Offset 5b54

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15	0x0	RW	**Firmware Valid Bit (FWVAL)** [br[1 = Firmware is ready 0 = Firmware is not ready
14:0	-	-	**Reserved**

Generic SPI (GSPI) Additional Registers

The registers in this section are memory mapped based on the BAR defined in PCI configuration space.

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
200h	4	CLOCKS (CLOCKS)	0h
204h	4	RESETS (RESETS)	0h
210h	4	ACTIVE LTR (ACTIVELTR_VALUE)	800h
214h	4	Idle LTR Value (IDLELTR_VALUE)	800h
218h	4	TX Bit Count (TX_BIT_COUNT)	0h
21ch	4	Rx Bit Count (RX_BIT_COUNT)	0h
220h	4	DMA Finish Disable (SSP_REG)	0h
224h	4	SPI CS CONTROL (SPI_CS_CONTROL)	3000h
228h	4	reg_SW_Scratch_0 (SW_SCRATCH)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
238h	4	Clock Gate (CLOCK_GATE)	0h
240h	4	Remap Address Low (REMAP_ADDR_LO)	0h
244h	4	Remap Address High (REMAP_ADDR_HI)	0h
24ch	4	Device Idle Control (DEVIDLE_CONTROL)	8h
250h	4	Delay Rx Clock (DEL_RX_CLK)	0h
2fch	4	Capabilities (CAPABLITIES)	20h

CLOCKS (CLOCKS) – Offset 200

Bit Range	Default	Access	Field Name and Description
31	0h	RW	**Clock Update (CLK_UPDATE)** Update the clock divider after seeing new m and n values 0 = No clock Update. 1 – Clock gets updated.
30:16	0h	RW	**N-Value (N_VAL)** n value for the m over n divider
15:1	0h	RW	**M_VAL (M_VAL)** m value for the m over n divider
0	0h	RW	**Clock Enable (CLK_EN)** Clock Enable of the m over n divider 0 = Clock disabled 1 = Clock Enabled.

RESETS (RESETS) – Offset 204

software reset

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**
2	0h	RW	**DMA Reset (RESET_DMA)** DMA Software Reset Control 0 = DMA is in reset (Reset Asserted) 1 = DMA is NOT at reset (Reset Released)
1:0	-	-	**Reserved**

ACTIVE LTR (ACTIVELTR_VALUE) – Offset 210

Bit Range	Default	Access	Field Name and Description
31	0h	RO	**Non Snoop Requirment (non_snoop_requirment)** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
30:29	-	-	**Reserved**
28:26	0h	RO	**Non-Snoop Latency Scale (non_snoop_latency_scale)** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale (1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
25:16	0h	RO	**Non-Snoop Value (non_snoop_value)** 10-bit latency value
15	0h	RW	**Snoop Requirement (snoop_requirment)** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.

Bit Range	Default	Access	Field Name and Description
14:13	-	-	**Reserved**
12:10	2h	RW	**Snoop Latency Scale (snoop_latency_scale)** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h	RW	**Snoop Value (SNOOP_VALUE)** 10-bit latency value

Idle LTR Value (IDLELTR_VALUE) – Offset 214

Bit Range	Default	Access	Field Name and Description
31	0h	RO	**Non Snoop Requirment (non_snoop_requirment)** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
30:29	-	-	**Reserved**
28:26	0h	RO	**Non Snoop Latency Scale (non_snoop_latency_scale)** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale (1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
25:16	0h	RO	**Non Snoop Value (non_snoop_value)** 10-bit latency value
15	0h	RW	**Snoop Requirment (snoop_requirment)** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.

Bit Range	Default	Access	Field Name and Description
14:13	-	-	**Reserved**
12:10	2h	RW	**Snoop Latency Scale (snoop_latency_scale)** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h	RW	**Snoop Value (snoop_value)** 10-bit latency value

TX Bit Count (TX_BIT_COUNT) – Offset 218

Bit Range	Default	Access	Field Name and Description
31	0h	RO	**Tx Count Overflow (tx_count_overflow)** 0 = Count valid 1 = count overflow/invalid
30:24	-	-	**Reserved**
23:0	0h	RO	**Tx Bit Count (tx_bit_count)** 24-bit up-counter which counts the number of TX bits on the Serial bus. The counter is forced to be cleared by software Read

Rx Bit Count (RX_BIT_COUNT) – Offset 21c

Bit Range	Default	Access	Field Name and Description
31	0h	RO	**Rx Count Overflow (rx_count_overflow)** 0 = count valid 1 = count overflow/invalid

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:0	0h	RO	**Rx Bit Count (rx_bit_count)** 24-bit up-counter which counts the number of RX Bits on the Serial bus. The counter is forced to be cleared by software Read

DMA Finish Disable (SSP_REG) – Offset 220

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RW	**Disable DMA Finish (disable_ssp_dma_finish)** This bit needs to be set to 1 if SPI is using DMA multi-Block Chaining and the SW driver does not plan to re-enable the DMA manually after every Link List completion 1 = DMA finish DisabledNote: Required for multi-block transfer 0 – DMA finish not disabled.

SPI CS CONTROL (SPI_CS_CONTROL) – Offset 224

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13	1h	RW	**Chip Select 1 Polarity (cs1_polarity)** 0 = low, 1 = high
12	1h	RW	**Chip Select 0 Polarity (cs0_polarity)** 0 = low, 1 = high

Bit Range	Default	Access	Field Name and Description
11:10	-	-	**Reserved**
9:8	0h	RW	**Chip Select Output (cs1_output_sel)** These Bits select which SPI CS Signal is to be driven by the controller. 00 = SPI CS0 01 = SPI CS1 10 = Reserved 11= Reserved
7:2	-	-	**Reserved**
1	0h	RW	**Chip Select State (cs_state)** Manual SW control of SPI Chip Select (CS) 0 = CS is set to low 1 = CS is set to high
0	0h	RW	**Chip Select Mode (cs_mode)** SPI Chip Select Mode. 0 = HW Mode- CS is under HW control 1 = SW Mode – CS is under SW Control using cs_state bit

reg_SW_Scratch_0 (SW_SCRATCH) – Offset 228

NOTE: The same registers are available at the following offsets:

SW SCRATCH 1: offset 22Ch

SW SCRATCH 2: offset 230h

SW SCRATCH 3: offset 234h

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**SW Scratch Pad (reg_SW_Scratch_0)** Scratch Pad Register for SW to generate Local DATA for DMA

Clock Gate (CLOCK_GATE) – Offset 238

Bit Range	Default	Access	Field Name and Description
30:4	-	-	**Reserved**
3:2	0h	RW	**DMA Clock Control (sw_dma_clk_ctl)** DMA Clock Control 00 = Dyanamic Clock Gate Enable 01 = Reserved 10 = Force DMA Clock off 11 = Force DMA Clock on
1:0	0h	RW	**Clock Control (sw_ip_clk_ctl)** Clock Control 00 = Dyanamic Clock Gate Enable 01 = Reserved 10 = Force Clocks off 11 = Force Clocks on

Remap Address Low (REMAP_ADDR_LO) – Offset 240

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Remap Address Low (spi_remap_addr_low)** Low 32 bits of BAR address read by SW

Remap Address High (REMAP_ADDR_HI) – Offset 244

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Remap Address High (spi_remap_addr_high)** High 32 bits of BAR address read by SW

Device Idle Control (DEVIDLE_CONTROL) – Offset 24c

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4	0h	RO	**Interrupt Request Capable (intr_req_capable)** Set to '1' by HW if it is capable of generating an interrupt on command completion, else '0'.
3	1h	RW/1C	**Restore Required (restore_required)** When set (by HW), SW must restore state to the controller. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a '1'. This bit will be set on initial power up.
2	0h	RW	**Device Idle (devidle)** SW sets this bit to '1' to move the function into the DevIdle state. Writing this bit to '0' will return the function to the fully active D0 state (D0i0).
1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	0h	RO	**CMD In Progress (cmd_in_progress)** HW sets this bit on a 1->0 or 0->1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register.HW clears this bit upon completing the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

Delay Rx Clock (DEL_RX_CLK) – Offset 250

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RW	**Delayed Rx Clock Select (RX_CLK_SEL)** 00 = The output of the internal (M/N and/or baud rate) clock divider is used as-is to clock in the receive data to the RxFIFO. 01 = An internally delayed version of the internal clock divider output is used to clock in the receive data to the RxFIFO. This allows some additional setup time on the PCH side. 10 = The receive data is clocked on the subsequent negedge of the Tx clock, allowing a full cycle propagation delay on the platform. 11: The receive data is clocked on the subsequent negedge of the delayed Rx clock, maximizing the amount of delay allowed for capturing the receive data. Note: This capability is only supported for default SSP configuration with active high clocks (SSCR1.SPO = 0 and SSCR1.SPH = 0). Other combinations of SPO and SPH setting are not supported for non-zero settings of this field.

Capabilities (CAPABLITIES) – Offset 2fc

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0h	RO	**DMA Present (iDMA_present)** 0= DMA present 1= DMA not present
7:4	2h	RO	**Instant Type (instance_type)** 0000 = IC2 0001 = UART 0010 = SPI 0011 – 1111 = Reserved
3:0	0h	RO	**Instance Number (instance_number)** 0h: SPI0 1h: SPI1

Generic SPI (GSPI) DMA Controller Registers

The registers in this section are memory mapped based on the BAR defined in PCI configuration space.

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
868h	4	CH 1 Linked List Pointer Low (LLP_LO1)	0h
86ch	4	CH 1 Linked List Pointer High (LLP_HI1)	0h
ac0h	4	Raw Interrupt Status (RawTfr)	0h
800h	4	DMA Transfer Source Address Low (SAR_LO0)	0h
804h	4	DMA Transfer Source Address High (SAR_HI0)	0h
808h	4	DMA Transfer Destination Address Low (DAR_LO0)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
80ch	4	DMA Transfer Destination Address High (DAR_HI0)	0h
810h	4	CH 0 Linked List Pointer Low (LLP_LO0)	0h
814h	4	CH 0 Linked List Pointer High (LLP_HI0)	0h
ac8h	4	Raw Status for Block Interrupts (RawBlock)	0h
ad0h	4	Raw Status for Source Transaction Interrupts (RawSrcTran)	0h
ad8h	4	Raw Status for Destination Transaction Interrupts (RawDstTran)	0h
818h	4	Control Register Low (CTL_LO0)	0h
81ch	4	Control Register High (CTL_HI0)	0h
820h	4	Source Status (SSTAT0)	0h
828h	4	Destination Status (DSTAT0)	0h
830h	4	Source Status Address Low (SSTATAR_LO0)	0h
834h	4	Source Status Address High (SSTATAR_HI0)	0h
838h	4	Destination Status Address Low (DSTATAR_LO0)	0h
83ch	4	Destination Status Address High (DSTATAR_HI0)	0h
840h	4	DMA Transfer Configuration Low (CFG_LO0)	203h
844h	4	DMA Transfer Configuration High (CFG_HI0)	0h
848h	4	Source Gather (SGR0)	0h
850h	4	Destination Scatter (DSR0)	0h
ae0h	4	Raw Status for Error Interrupts (RawErr)	0h
ae8h	4	Interrupt Status (StatusTfr)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
af0h	4	Status for Block Interrupts (StatusBlock)	0h
af8h	4	Status for Source Transaction Interrupts (StatusSrcTran)	0h
b00h	4	Status for Destination Transaction Interrupts (StatusDstTran)	0h
b08h	4	Status for Error Interrupts (StatusErr)	0h
b10h	4	Mask for Transfer Interrupts (MaskTfr)	0h
b18h	4	Mask for Block Interrupts (MaskBlock)	0h
b20h	4	Mask for Source Transaction Interrupts (MaskSrcTran)	0h
b28h	4	Mask for Destination Transaction Interrupts (MaskDstTran)	0h
b30h	4	Mask for Error Interrupts (MaskErr)	0h
b38h	4	Clear for Transfer Interrupts (ClearTfr)	0h
b40h	4	Clear for Block Interrupts (ClearBlock)	0h
b48h	4	Clear for Source Transaction Interrupts (ClearSrcTran)	0h
b50h	4	Clear for Destination Transaction Interrupts (ClearDstTran)	0h
b58h	4	Clear for Error Interrupts (ClearErr)	0h
b60h	4	Combined Status register (StatusInt)	0h
b98h	4	DMA Configuration (DmaCfgReg)	0h
ba0h	4	DMA Channel Enable (ChEnReg)	0h

CH 1 Linked List Pointer Low (LLP_LO1) – Offset 868

LLP_LO1 is for DMA Channel 1.

The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Bit Range	Default	Access	Field Name and Description
31:2	0000000 0h	RW	**LLP Address Low (LOC)** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit. Note: SW should avoid a LLP lower 32 bits equal to 0s assigned to 4GB boundary address.
1:0	-	-	**Reserved**

CH 1 Linked List Pointer High (LLP_HI1) – Offset 86c

LLP_HI1 is for DMA Channel 1.

The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Bit Range	Default	Access	Field Name and Description
31:2	0000000 0h	RW	**LLP Address High (LOC)** LLP upper address.
1:0	-	-	**Reserved**

Raw Interrupt Status (RawTfr) – Offset ac0

Interrupt events are stored in these Raw Interrupt Status registers before masking:

RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status

register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2

raw transfer complete interrupt.

Each bit in these registers is cleared by writing a 1 to the corresponding

location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers

The following RAW registers are available in the DMA

RawTfr - Raw Status for Transfer Interrupts

RawBlock - Raw Status for Block Interrupts Register

RawSrcTran - Raw Status for Source Transaction Interrupts Register

RawDstTran - Raw Status for Destination Transaction Interrupts Register

RawErr - Raw Status for Error Interrupts Register

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Raw Interrupt Status (RAW)** Bit0 for channel 0 and bit 1 for channel 1.

DMA Transfer Source Address Low (SAR_LO0) – Offset 800

NOTE: SAR_LO0 is for DMA Channel 0. The same register definition,SAR_LO1, is available for Channel 1 at address 858h.

SAR_LO0 (CH0): offset 800h

SAR_LO1 (CH1): offset 858h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**(SAR_LO)** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

DMA Transfer Source Address High (SAR_HI0) – Offset 804

NOTE: SAR_HI0 is for DMA Channel 0. The same register definition, SAR_HI1, is available for Channel 1 at address 85Ch.

SAR_HI0 (CH0): offset 804h

SAR_HI1 (CH1): offset 85Ch

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**(SAR_HI)** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value.

Bit Range	Default	Access	Field Name and Description
			5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

DMA Transfer Destination Address Low (DAR_LO0) – Offset 808

NOTE: DAR_LO0 is for DMA Channel 0. The same register definition, DAR_LO1, is available for Channel 1 at address 860h.

DAR_LO0 (CH0): offset 808h

DAR_LO1 (CH1): offset 860h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**(DAR_LO)** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register.

Bit Range	Default	Access	Field Name and Description
			It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

DMA Transfer Destination Address High (DAR_HI0) – Offset 80c

NOTE: DAR_HI0 is for DMA Channel 0. The same register definition, DAR_HI1, is available for Channel 1 at address 864h.

DAR_HI0 (CH0): offset 80Ch

DAR_HI1 (CH1): offset 864h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**(DAR_HI)** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value.

Bit Range	Default	Access	Field Name and Description
			5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

CH 0 Linked List Pointer Low (LLP_LO0) – Offset 810

LLP_LO0 is for DMA Channel 0.

The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Bit Range	Default	Access	Field Name and Description
31:2	0000000 0h	RW	**LLP Address Low (LOC)** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit. Note: SW should avoid a LLP lower 32 bits equal to 0s assigned to 4GB boundary address.
1:0	-	-	**Reserved**

CH 0 Linked List Pointer High (LLP_HI0) – Offset 814

LLP_HI0 is for DMA Channel 0.

The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Bit Range	Default	Access	Field Name and Description
31:2	0000000 0h	RW	**LLP Address High (LOC)** LLP upper address.
1:0	-	-	**Reserved**

Raw Status for Block Interrupts (RawBlock) – Offset ac8

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Raw Interrupt Status (RAW)** Bit 0 for channel 0 and bit 1 for channel 1.

Raw Status for Source Transaction Interrupts (RawSrcTran) – Offset ad0

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Raw Interrupt Status (RAW)** Bit 0 for channel 0 and bit 1 for channel 1.

Raw Status for Destination Transaction Interrupts (RawDstTran) – Offset ad8

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Raw Interrupt Status (RAW)** Bit 0 for channel 0 and bit 1 for channel 1.

Control Register Low (CTL_LO0) – Offset 818

NOTE: CTL_LO0 is for DMA Channel 0. The same register definition, CTL_LO1, is available for Channel 1 at address 870h.

LLP_HI0 (CH0): offset 818h

LLP_LO1 (CH1): offset 870h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**
28	0h	RW	**LLP Source Enable (LLP_SRC_EN)** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h	RW	**LLP Destination Enable (LLP_DST_EN)** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
21:20	0h	RW	**(TT_FC)** The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	-	-	**Reserved**
18	0h	RW	**Destination Scatter Enable (DST_SCATTER_EN)** 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h	RW	**Source Gather Enable (SRC_GATHER_EN)** 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h	RW	**Source Burst Transaction Length (SRC_MSIZE)** Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source.

Bit Range	Default	Access	Field Name and Description
13:11	0h	RW	**Destination Burst Transaction Length (DEST_MSIZE)** Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h	RW	**Source Address Increment (SINC)** Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	-	-	**Reserved**
8	0h	RW	**Destination Address Increment (DINC)** Indicates whether to increment or decrement the destination address on every destination transfer. If the device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	-	-	**Reserved**
6:4	0h	RW	**Source Transfer Width (SRC_TR_WIDTH)** BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
3:1	0h	RW	**Destination Transfer Width (DST_TR_WIDTH)** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)

Bit Range	Default	Access	Field Name and Description
0	0h	RW	**Interrupt Enable (INT_EN)** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

Control Register High (CTL_HI0) – Offset 81c

NOTE: CTL_HI0 is for DMA Channel 0. The same register definition, CTL_HI1, is available for Channel 1 at address 874h.

CTL_HI0 (CH0): offset 81Ch

CTL_HI1 (CH1): offset 874h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Bit Range	Default	Access	Field Name and Description
31:29	0h	RW	**(CH_CLASS)** A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.
28:18	0h	RW	

Bit Range	Default	Access	Field Name and Description
			(CH_WEIGHT) Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.
17	0h	RW	**Done (DONE)** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.

Bit Range	Default	Access	Field Name and Description
16:0	0h	RW	**Block Transfer Size (BLOCK_TS)** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

Source Status (SSTAT0) – Offset 820

NOTE: SSTAT0 is for DMA Channel 0. The same register definition, SSTAT1, is available for Channel 1 at address 878h.

SSTAT0 (CH0): offset 820h

SSTAT1 (CH1): offset 878h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.

Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Source Status (SSTAT)** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

Destination Status (DSTAT0) – Offset 828

NOTE: DSTAT0 is for DMA Channel 0. The same register definition, DSTAT1, is available for Channel 1 at address 880h.

DSTAT0 (CH0): offset 828h

DSTAT1 (CH1): offset 880h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.

Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Destination Status (DSTAT)** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

Source Status Address Low (SSTATAR_LO0) – Offset 830

NOTE: SSTATAR_LO0 is for DMA Channel 0. The same register definition, SSTATAR_LO1, is available for Channel 1 at address 888h.

SSTATAR_LO0(CH0): offset 830h

SSTATAR_LO1(CH1): offset 888h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Source Status Address Low (SSTATAR_LO)** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

Source Status Address High (SSTATAR_HI0) – Offset 834

NOTE: SSTATAR_HI0 is for DMA Channel 0. The same register definition, SSTATAR_HI1, is available for Channel 1 at address 88Ch.

SSTATAR_HI0(CH0): offset 834h

SSTATAR_HI1(CH1): offset 88Ch

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Source Status Address High (SSTATAR_HI)** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

Destination Status Address Low (DSTATAR_LO0) – Offset 838

NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_LO1, is available for Channel 1 at address 890h.

DSTATAR_LO0(CH0): offset 838h

DSTATAR_LO1(CH1): offset 890h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Destination Status Address Low (DSTATAR_LO)** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

Destination Status Address High (DSTATAR_HI0) – Offset 83c

NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_HI1, is available for Channel 1 at address 894h.

DSTATAR_HI0(CH0): offset 83Ch

DSTATAR_HI1(CH1): offset 894h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Destination Status Address High (DSTATAR_HI)** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

DMA Transfer Configuration Low (CFG_LO0) – Offset 840

NOTE: CFG_LO0 is for DMA Channel 0. The same register definition, CFG_LO1, is available for Channel 1 at address 898h.

CFG_LO0(CH0): offset 840h

CFG_LO1(CH1): offset 898h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Bit Range	Default	Access	Field Name and Description
31	0h	RW	**Automatic Destination Reload (RELOAD_DST)** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h	RW	**Automatic Source Reload (RELOAD_SRC)** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	-	-	**Reserved**
21	0h	RW	**Source Burst Length (SRC_OPT_BL)** Optimize Source Burst Length: 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ SRC_MSIZE)) This bit should be set to (0) if Source HW-Handshake is enabled

Bit Range	Default	Access	Field Name and Description
20	0h	RW	**Destination Burst Length (DST_OPT_BL)** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ DST_MSIZE)) This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h	RW	**Source Handshaking Interface Polarity (SRC_HS_POL)** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h	RW	**Destination Handshaking Interface Polarity (DST_HS_POL)** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17:11	-	-	**Reserved**
10	0b	RW	**Channel FIFO Drain (CH_DRAIN)** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1b	RO	**FIFO Empty (FIFO_EMPTY)** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default	Access	Field Name and Description
8	0h	RW	**Channel Suspend (CH_SUSP)** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h	RW	**Source Status Update Enable (SS_UPD_EN)** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h	RW	**Destination Status Update Enable (DS_UPD_EN)** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h	RW	**CTL_HI Update Enable (CTL_HI_UPD_EN)** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	-	-	**Reserved**
3	0h	RW	**Handshake Non-Posted Write (HSHAKE_NP_WR)** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h	RW	**Non Posted Write (ALL_NP_WR)** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.

Bit Range	Default	Access	Field Name and Description
1	1h	RW	**Source Burst Align (SRC_BURST_ALIGN)** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h	RW	**Destination Burst Align (DST_BURST_ALIGN)** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary.

DMA Transfer Configuration High (CFG_HI0) – Offset 844

NOTE: CFG_HI0 is for DMA Channel 0. The same register definition, CFG_HI1, is available for Channel 1 at address 89Ch.

CFG_HI0(CH0): offset 844h

CFG_HI1(CH1): offset 89Ch

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Bit Range	Default	Access	Field Name and Description
30:28	-	-	**Reserved**
27:18	0h	RW	**Write Issue Threshold (WR_ISSUE_THD)** Write Issue Threshold. Used to relax the issue criterion for Writes. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h	RW	**Read Issue Threshold (RD_ISSUE_THD)** Read Issue Threshold. Used to relax the issue criterion for Reads. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_ MSIZE)*TW.

Bit Range	Default	Access	Field Name and Description
7:4	0h	RW	**Destination Peripheral ID (DST_PER)** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.
3:0	0h	RW	**Source Peripheral ID (SRC_PER)** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

Source Gather (SGR0) – Offset 848

NOTE: SGR0 is for DMA Channel 0. The same register definition, SGR1, is available for Channel 1 at address 8A0h.

SGR0(CH0): offset 848h

SGR1(CH1): offset 8A0h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Bit Range	Default	Access	Field Name and Description
31:20	0h	RW	**Source Gather Count (SGC)** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h	RW	**Source Gather Interval (SGI)**

Destination Scatter (DSR0) – Offset 850

NOTE: DSR0 is for DMA Channel 0. The same register definition, DSR1, is available for Channel 1 at address 8A8h.

DSR0(CH0): offset 850h

DSR1(CH1): offset 8A8h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Bit Range	Default	Access	Field Name and Description
31:20	0h	RW	**Destination Scatter Count (DSC)**
19:0	0h	RW	**Destination Scatter Interval (DSI)**

Raw Status for Error Interrupts (RawErr) – Offset ae0

Interrupt events are stored in these Raw Interrupt Status registers before masking:

RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status

register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2

raw transfer complete interrupt.

Each bit in these registers is cleared by writing a 1 to the corresponding

location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers

The following RAW registers are available in the DMA

RawTfr - Raw Status for Transfer Interrupts

RawBlock - Raw Status for Block Interrupts Register

RawSrcTran - Raw Status for Source Transaction Interrupts Register

RawDstTran - Raw Status for Destination Transaction Interrupts Register

RawErr - Raw Status for Error Interrupts Register

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Raw Interrupt Status (RAW)** Bit 0 for channel 0 and bit 1 for channel 1.

Interrupt Status (StatusTfr) – Offset ae8

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Interrupt Status (STATUS)** Bit 0 for channel 0 and bit 1 for channel 1.

Status for Block Interrupts (StatusBlock) – Offset af0

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Interrupt Status (STATUS)** Bit 0 for channel 0 and bit 1 for channel 1.

Status for Source Transaction Interrupts (StatusSrcTran) – Offset af8

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Interrupt Status (STATUS)** Bit 0 is for channel 0 and bit 1 is for channel 1.

Status for Destination Transaction Interrupts (StatusDstTran) – Offset b00

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Interrupt Status (STATUS)** Bit 0 is for channel 0 and bit 1 is for channel 1.

Status for Error Interrupts (StatusErr) – Offset b08

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Interrupt Status (STATUS)** Bit 0 is for channel 0 and bit 1 is for channel 1.

Mask for Transfer Interrupts (MaskTfr) – Offset b10

The contents of the Raw Status registers are masked with the contents of the Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr. Each Interrupt Mask register has a bit allocated per channel, for example, MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt.

When the source peripheral of DMA channel i is memory, then the source transaction complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal.

A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged.

Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port

signals.

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:8	0h	WO	**Interrupt Mask Write Enable (INT_MASK_WE)** 0 = write disabled 1 = write enabled
7:2	-	-	**Reserved**
1:0	0h	RW	**Interrupt Mask (INT_MASK)** 0-mask 1-unmask

Mask for Block Interrupts (MaskBlock) – Offset b18

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:8	0h	WO	**Interrupt Mask Write Enable (INT_MASK_WE)** 0 = write disabled 1 = write enabled
7:2	-	-	**Reserved**
1:0	0h	RW	**Interrupt Mask (INT_MASK)** 0-mask 1-unmask

Mask for Source Transaction Interrupts (MaskSrcTran) – Offset b20

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:8	0h	WO	**Interrupt Mask Write Enable (INT_MASK_WE)** 0 = write disabled 1 = write enabled
7:2	-	-	**Reserved**
1:0	0h	RW	**Interrupt Mask (INT_MASK)** 0-mask 1-unmask

Mask for Destination Transaction Interrupts (MaskDstTran) – Offset b28

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:8	0h	WO	**Interrupt Mask Write Enable (INT_MASK_WE)** 0 = write disabled 1 = write enabled
7:2	-	-	**Reserved**
1:0	0h	RW	**Interrupt Mask (INT_MASK)** 0-mask 1-unmask

Mask for Error Interrupts (MaskErr) – Offset b30

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:8	0h	WO	**Interrupt Mask Write Enable (INT_MASK_WE)** 0 = write disabled 1 = write enabled
7:2	-	-	**Reserved**
1:0	0h	RW	**Interrupt Mask (INT_MASK)** 0-mask 1-unmask

Clear for Transfer Interrupts (ClearTfr) – Offset b38

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	WO	**Interrupt Clear (CLEAR)** 0 = no effect 1 = clear interrupt

Clear for Block Interrupts (ClearBlock) – Offset b40

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	WO	**Interrupt Clear (CLEAR)** 0 = no effect 1 = clear interrupt

Clear for Source Transaction Interrupts (ClearSrcTran) – Offset b48

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	WO	**Interrupt Clear (CLEAR)** 0 = no effect 1 = clear interrupt

Clear for Destination Transaction Interrupts (ClearDstTran) – Offset b50

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	WO	**Interrupt Clear (CLEAR)** 0 = no effect 1 = clear interrupt

Clear for Error Interrupts (ClearErr) – Offset b58

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	WO	**Interrupt Clear (CLEAR)** 0 = no effect 1 = clear interrupt

Combined Status register (StatusInt) – Offset b60

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is ORed to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4	0h	RO	**(ERR)** OR of the contents of StatusErr register.
3	0h	RO	**(DSTT)** OR of the contents of StatusDst register.
2	0h	RO	**(SRCT)** OR of the contents of StatusSrcTran register
1	0h	RO	**(BLOCK)** OR of the contents of StatusBlock register.
0	0h	RO	**(TFR)** OR of the contents of StatusTfr register.

DMA Configuration (DmaCfgReg) – Offset b98

This register is used to enable the DMA, which must be done before any channel

activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RW	**(DMA_EN)** 0 = DMA Disabled 1 = DMA Enabled

DMA Channel Enable (ChEnReg) – Offset ba0

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority.
All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0.

The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer. For example, writing hex 01x1 writes a 1 into ChEnReg(0), while ChEnReg(7:1) remains unchanged. Writing hex 00xx leaves ChEnReg(7:0) unchanged.
Note that a read-modified write is not required.

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
9:8	0h	WO	**(CH_EN_WE)** Channel enable write enable.
7:2	-	-	**Reserved**
1:0	0h	RW	**(CH_EN)** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

Generic SPI (GSPI) Memory Mapped Registers

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	SSP (GSPI) Control Register 0 (SSCR0)	0h
4h	4	SSP (GSPI) Control Register 1 (SSCR1)	0h
8h	4	SSP (GSPI) Status Register (SSSR)	4h
10h	4	SSP (GSPI) Data (SSDR)	0h
28h	4	SSP (GSPI) Time Out (SSTO)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
44h	4	SPI Transmit FIFO (SITF)	0h
48h	4	SPI Receive FIFO (SIRF)	0h

SSP (GSPI) Control Register 0 (SSCR0) – Offset 0

All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

Bit Range	Default	Access	Field Name and Description
31	0b	RW	**MOD (MOD)** ModeSet to 0 - Normal SSP Mode : Full Duplex Serial peripheral interface. 1 = reserved
30	0b	RW	**ACS (ACS)** Audio Clock Select 0 - Clock selection is determined by the NCS and ECS bits 1 - reserved
29:24	-	-	**Reserved**
23	0b	RW	**TIM (TIM)** Transmit FIFO Under Run Interrupt Mask When set, this bit will mask the Transmit FIFO Under Run (TUR) event from generating an SSP interrupt. The SSSR status register will still indicate that an TUR event has occurred. This bit can be written to at any time (before or after SSP is enabled). 0 = Transmit FIFO Under Run(TUR) events will generate an SSP interrupt 1 = TUR events will be masked

Bit Range	Default	Access	Field Name and Description
22	0b	RW	**RIM (RIM)** Receive FIFO Over Run Interrupt Mask When set, this bit will mask the Receive FIFO Over Run (ROR) event from generating an SSP interrupt. The SSSR status register will still indicate that an ROR event has occurred. This bit can be written to at any time (before or after SSP is enabled) 0 = receive FIFO Over Run(ROR) events will generate an SSP interrupt 1 = ROR events will be masked
21	0b	RW	**NCS (NCS)** Network Clock SelectThe SSCR0.NCS bit in conjunction with SSCR0.ECS determines which clock is used. 0 - Clock selection is determined by ECS bit 1 – Reserved
20	0b	RW	**EDSS (EDSS)** Extended Data Size SelectThe 1-bit extended field is used in conjunction with the data size select SSCR0.DSS bits to select the size of the data transmitted and received by the Enhanced SSP. 0 = A zero is prepended to the DSS value which sets the DSS range from 4-16 bits 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits
19:8	0h	RW	**SCR (SCR)** Serial Clock Rate Value (0 to 4095) used to generate transmission rate of SSP. Serial bit rate = SSP clock/(SCR+1), where SCR is decimal integer.
7	0b	RW	**SSE (SSE)** Synchronous Serial Port Enable 0 - SSP operation disabled 1 - SSP operation enabled

Bit Range	Default	Access	Field Name and Description
6	0b	RW	**ECS (ECS)** External Clock Select:0 = use On-chip clock (output of M/N Divider) to produce the SSP's serial clock (SSPSCLK). Selects the use of the the output of the M/N Divider (MBAR0 + 0x800, CLOCKS) to create the SSP's serial clock (SSPCLK) Note: Setting M=N=1 will provide a pass through of the M/N Divider of the serial clock. See SCR for Serial Clock Rate generation. 1 = Reserved
5:4	00b	RW	**FRF (FRF)** Frame FormatSet to 00 - Motorola Serial Peripheral Interface (SPI) 01 - 10 = reserved
3:0	0000b	RW	**DSS (DSS)** Data Size Select With EDSS as MSB, value+1 gives data size. Values 4 to 32 allowed.

SSP (GSPI) Control Register 1 (SSCR1) – Offset 4

The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW	**RWOT (RWOT)** Receive With Out Transmit 0 = Transmit/Receive mode 1 = Receive without transmit mode

Bit Range	Default	Access	Field Name and Description
22	0b	RW	**TRAIL (TRAIL)** Trailing Byte 0 = Processor based, trailing bytes are handled by processor 1 - DMA based, trailing bytes are handled by DMA
21	0b	RW	**TSRE (TSRE)** Transmit Service Request Enable 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
20	0b	RW	**RSRE (RSRE)** Receive Service Request Enable 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	0b	RW	**TINTE (TINTE)** Receiver Time-out Interrupt Enable 0 - Receiver Time-out interrupts are disabled 1 - Receiver Time-out interrupts are enabled
18:17	-	-	**Reserved**
16	0b	RW	**IFS (IFS)** Invert Frame Signal0 = Frame signal (Chip Select) is active low 1 = Frame signal (Chip Select) is active high
15:5	-	-	**Reserved**
4	0b	RW	**SPH (SPH)** Motorola SPI SSPSCLK phase setting 0 = SSPSCLK is inactive one sycle at the start of a frame and cycle at the end of a frame 1 = SSPSCLK is inactive for one half cycle at the start of a frame and one cycle at the end of a frame

Bit Range	Default	Access	Field Name and Description
3	0b	RW	**SPO (SPO)** Motorola SPI SSPSCLK polarity setting 0 = The inactive or idle state of SSPSCLK is low 1 = The inactive or idle state of SSPSCLK is high
2	-	-	**Reserved**
1	0b	RW	**TIE (TIE)** Transmit FIFO Interrupt Enable 0 = Transmit FIFO level interrupt is disabled 1 = Transmit FIFO level interrupt is enabled
0	0b	RW	**RIE (RIE)** Receive FIFO Interrupt Enable 0 = Receive FIFO level interrupt is disabled 1 = Receive FIFO level interrupt is enabled

SSP (GSPI) Status Register (SSSR) – Offset 8

The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request.

Bit Range	Default	Access	Field Name and Description
30:22	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
21	0b	RW/1C	**TUR (TUR)** Transmit FIFO Under Run 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	-	-	**Reserved**
19	0b	RW/1C	**TINT (TINT)** Receiver Time-out Interrupt 0 = No receiver time-out pending 1 = Receiver time-out pending
18	0b	RW/1C	**PINT (PINT)** Peripheral Trailing Byte Interrupt 0 - No peripheral trailing byte interrupt pending 1 - Peripheral trailing byte interrupt pending
17:8	-	-	**Reserved**
7	0b	RW/1C	**ROR (ROR)** Receive FIFO Overrun 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	0b	RO	**RFS (RFS)** Receive FIFO Service Request 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt

Bit Range	Default	Access	Field Name and Description
5	0b	RO	**TFS (TFS)** Transmit FIFO Service Request 0 = Transmit FIFO level exceeds the Low Water Mark Transmit FIFO (SITF.LWMTF), or SSP disabled 1 = Transmit FIFO level is at or below the Low Water Mark Transmit FIFO (SITF.LWMTF), request interrupt
4	0b	RO	**BSY (BSY)** SSP Busy 0 = SSP is idle or disabled 1 = SSP currently transmitting or receiving a frame
3	0b	RO	**RNE (RNE)** Receive FIOF Not Empty 0 = Receive FIFO is empty 1 = Receive FIFO is not empty
2	1b	RO	**TNF (TNF)** Transmit FIFO Not Full 0 = Transmit FIFO is full 1 = Transmit FIFO is not full
1:0	-	-	**Reserved**

SSP (GSPI) Data (SSDR) – Offset 10

The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access.

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO	**DATA (DATA)** Data word to be written to/read from transmit/receive FIFO

SSP (GSPI) Time Out (SSTO) – Offset 28

The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:0	000000h	RW	**TIMEOUT (TIMEOUT)** Timeout Value Is the value that defines the timeout interval for the rcv FIFO.The Interval is given by TIMEOUT/Parallel (Bus) Clock Frequency. When the number of samples in the Receive FIFO is less than rcv FIFO trigger threshold level, and no additional data is received, the Timeout timer will decrement. The time-out timer is reset after a new sample is received. In DMA Mode of operation this value needs to be set when the Rcv FIFO Trigger Threshold is greater than 1 Rcv FIFO Entry (the required MSize (Single Burst) for SSP DMA peripheral transfers)When in PIO mode of operation this value needs to be set when the total transfer size is not a even divison of the Rcv FIFO trigger threshold level.Is such a case the TIMEOUT value is calculated to be greater than the time to transfer the FIFO Entry size at the desired Bit Rate.

SPI Transmit FIFO (SITF) – Offset 44

The SPI Transmit FIFO register is for writing the water mark for the SPI transmit FIFO and also for reading the number of entries in the SPI transmit FIFO

Bit Range	Default	Access	Field Name and Description
30:22	-	-	**Reserved**
21:16	0b	RO	**SITFL (SITFL)** SPI Transmit FIFO Level Number of entries in SPI Transmit FIFO.
15:14	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
13:8	0b	RW	**LWMTF (LWMTF)** Low Water Mark Transmit FIFO. Set the low water mark of the SPI transmit FIFO. 6'b000000 = 1 entry through 6'b111111 = 64 entries
7:6	-	-	**Reserved**
5:0	0b	RW	**HWMTF (HWMTF)** High Water Mark Transmit FIFO. Set the high water mark of the SPI transmit FIFO. 6'b000000 = 1 entry through 6'b111111 = 64 entries

SPI Receive FIFO (SIRF) – Offset 48

The SPI Receive FIFO register is for writing the water mark for the SPI receive FIFO and also for reading the number of entries in the SPI receive FIFO

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13:8	0b	RO	**SIRFL (SIRFL)** SPI Receive FIFO Level Number of entries in SPI Receive FIFO.
7:6	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
5:0	0b	RW	**WMRF (WMRF)** Water Mark Receive FIFO. Set the water mark of the SPI receive FIFO. 6'b000000 = 1 entry through 6'b111111 = 64 entries

GPIO Community 0 Registers

GPIO pins are grouped into different Community (Example: Community 0, Community1, etc.). Each Community consists of one or more GPIO groups.

This section covers registers for Community 0, which consists of GPP_A, GPP_B, and GPP_G,groups.

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
600h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_0)	44000X00h. Refer to register for X value
604h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_0)	18h
610h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_1)	44000X00h. Refer to register for X value
614h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_1)	See Register
620h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_2)	44000X00h. Refer to register for X value

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
624h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_2)	See Register
8h	4	Family Base Address (FAMBAR)	300h
ch	4	Pad Base Address (PADBAR)	600h
10h	4	Miscellaneous Configuration (MISCCFG)	32043200h
20h	4	Pad Ownership (PAD_OWN_GPP_A_0)	0h
24h	4	Pad Ownership (PAD_OWN_GPP_A_1)	0h
28h	4	Pad Ownership (PAD_OWN_GPP_A_2)	0h
30h	4	Pad Ownership (PAD_OWN_GPP_B_0)	0h
630h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_3)	44000X00h. Refer to register for X value
634h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_3)	See Register
640h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_4)	44000X00h. Refer to register for X value
644h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_4)	See Register
650h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_5)	44000X00h. Refer to register for X value
654h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_5)	See Register
34h	4	Pad Ownership (PAD_OWN_GPP_B_1)	0h
38h	4	Pad Ownership (PAD_OWN_GPP_B_2)	0h
40h	4	Pad Ownership (PAD_OWN_GPP_G_0)	0h
80h	4	Pad Configuration Lock (PADCFGLOCK_GPP_A_0)	0h
84h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_A_0)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
88h	4	Pad Configuration Lock (PADCFGLOCK_GPP_B_0)	0h
8ch	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_B_0)	0h
660h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_6)	44000X00h. Refer to register for X value
664h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_6)	See Register
670h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_7)	44000X00h. Refer to register for X value
674h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_7)	See Register
680h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_8)	44000X00h. Refer to register for X value
684h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_8)	See Register
90h	4	Pad Configuration Lock (PADCFGLOCK_GPP_G_0)	0h
94h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_G_0)	0h
b0h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_A_0)	0h
b4h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_B_0)	0h
b8h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_G_0)	0h
100h	4	GPI Interrupt Status (GPI_IS_GPP_A_0)	0h
104h	4	GPI Interrupt Status (GPI_IS_GPP_B_0)	0h
108h	4	GPI Interrupt Status (GPI_IS_GPP_G_0)	0h
120h	4	GPI Interrupt Enable (GPI_IE_GPP_A_0)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
124h	4	GPI Interrupt Enable (GPI_IE_GPP_B_0)	0h
128h	4	GPI Interrupt Enable (GPI_IE_GPP_G_0)	0h
140h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_0)	0h
144h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_B_0)	0h
148h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_G_0)	0h
160h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_0)	0h
164h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_B_0)	0h
168h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_G_0)	0h
184h	4	SMI Status (GPI_SMI_STS_GPP_B_0)	0h
1a4h	4	SMI Enable (GPI_SMI_EN_GPP_B_0)	0h
1c4h	4	NMI Status (GPI_NMI_STS_GPP_B_0)	0h
690h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_9)	44000X00h. Refer to register for X value
694h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_9)	See Register
6a0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_10)	44000X00h. Refer to register for X value
6a4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_10)	See Register
6b0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_11)	44000X00h. Refer to register for X value
6b4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_11)	See Register

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
6c0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_12)	44000X00h. Refer to register for X value
6c4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_12)	See Register
6d0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_13)	44000X00h. Refer to register for X value
6d4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_13)	See Register
6e0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_14)	44000X00h. Refer to register for X value
6e4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_14)	See Register
6f0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_15)	44000X00h. Refer to register for X value
6f4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_15)	See Register
700h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_16)	44000X00h. Refer to register for X value
704h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_16)	See Register
710h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_17)	44000X00h. Refer to register for X value
714h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_17)	See Register
720h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_18)	44000X00h. Refer to register for X value
724h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_18)	See Register
730h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_19)	44000X00h. Refer to register for X value
734h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_19)	See Register

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
740h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_20)	44000X00h. Refer to register for X value
744h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_20)	See Register
750h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_21)	44000X00h. Refer to register for X value
754h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_21)	See Register
760h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_22)	44000X00h. Refer to register for X value
764h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_22)	See Register
770h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_23)	44000X00h. Refer to register for X value
774h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_23)	See Register
790h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_0)	44000X00h. Refer to register for X value
794h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_0)	See Register
7a0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_1)	44000X00h. Refer to register for X value
7a4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_1)	See Register
7b0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_2)	44000X00h. Refer to register for X value
7b4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_2)	See Register
7c0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_3)	44000X00h. Refer to register for X value
7c4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_3)	See Register

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7d0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_4)	44000X00h. Refer to register for X value
7d4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_4)	See Register
7e0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_5)	44000X00h. Refer to register for X value
7e4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_5)	See Register
7f0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_6)	44000X00h. Refer to register for X value
7f4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_6)	See Register
800h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_7)	44000X00h. Refer to register for X value
804h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_7)	See Register
810h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_8)	44000X00h. Refer to register for X value
814h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_8)	See Register
820h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_9)	44000X00h. Refer to register for X value
824h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_9)	See Register
830h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_10)	44000X00h. Refer to register for X value
834h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_10)	See Register
840h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_11)	44000X00h. Refer to register for X value

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
844h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_11)	See Register
850h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_12)	44000X00h. Refer to register for X value
854h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_12)	See Register
860h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_13)	44000X00h. Refer to register for X value
864h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_13)	See Register
870h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_14)	44000X00h. Refer to register for X value
874h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_14)	See Register
880h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_15)	44000X00h. Refer to register for X value
884h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_15)	See Register
890h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_16)	44000X00h. Refer to register for X value
894h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_16)	See Register
8a0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_17)	44000X00h. Refer to register for X value
8a4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_17)	See Register
8b0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_18)	44000X00h. Refer to register for X value
8b4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_18)	See Register
8c0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_19)	44000X00h. Refer to register for X value

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8c4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_19)	See Register
8d0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_20)	44000X00h. Refer to register for X value
8d4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_20)	See Register
8e0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_21)	44000X00h. Refer to register for X value
8e4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_21)	See Register
8f0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_22)	44000X00h. Refer to register for X value
8f4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_22)	See Register
900h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_23)	44000X00h. Refer to register for X value
904h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_23)	See Register
930h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_0)	44000X00h. Refer to register for X value
934h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_0)	See Register
940h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_1)	44000X00h. Refer to register for X value
944h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_1)	See Register
950h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_2)	44000X00h. Refer to register for X value
954h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_2)	See Register
960h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_3)	44000X00h. Refer to register for X value

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
964h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_3)	See Register
970h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_4)	44000X00h. Refer to register for X value
974h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_4)	See Register
980h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_5)	44000X00h. Refer to register for X value
984h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_5)	See Register
990h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_6)	44000X00h. Refer to register for X value
994h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_6)	See Register
9a0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_7)	44000X00h. Refer to register for X value
9a4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_7)	See Register
1e4h	4	NMI Enable (GPI_NMI_EN_GPP_B_0)	0h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_0) – Offset 600

This register applies to GPP_A0.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:30	01b	RW	**Pad Reset Config (PADRSTCFG)** This register controls which reset is used to reset GPIO pad register fields in PAD_CFG_DW0 and PAD_CFG_DW1 registers. This register can be used for Sx isolation of the associated signal if needed. 00 = RSMRST# 01 = Host deep reset. This reset occurs when any of the following occur: Host reset (with or without power cycle) is initiated, Global reset is initiated, or Deep Sx entry. This reset does NOT occur as part of S3/S4/S5 entry. 10 = PLTRST# 11 = Reserved
29	0b	RW	**RX Pad State Select (RXPADSTSEL)** Determines from which node the RX pad state for native function should be taken from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from RX buffer 1 = Internal RX pad state (subject to RXINV and PreGfRXSel settings)
28	0b	RW	**RX Raw Override to '1' (RXRAW1)** This bit determines if the selected pad state is being overridden to '1'. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
26:25	10b	RW	**RX Level/Edge Configuration (RXEVCFG)** Determines if the internal RX pad state (synchronized, filtered vs non-filtered version as determined by PreGfRXSel, and is further subject to RXInv) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller . 0h = Level 1h = Edge (RxInv=0 for rising edge; 1 for falling edge) 2h = Disable 3h = Either rising edge or falling edge
24	0b	RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL)** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV

Bit Range	Default	Access	Field Name and Description
23	0b	RW	**RX Invert (RXINV)** This bit determines if the selected pad state should go through the polarity inversion stage. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	00b	RW	**RX/TX Enable Config (RXTXENCFG)** This controls the RX and TX buffer enablement for the function selected by Pad Mode. This field is not applicable in GPIO mode (PMode = 0. 0h = Function defined in Pad Mode controls TX and RX enablement 1h = Function controls TX enablement and RX is disabled with 0 being driven internally 2h = Function controls TX enablement and RX is disabled with 1 being driven internally 3h = Function controls TX enablement and RX is always enabled
20	0b	RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC)** Determines if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default	Access	Field Name and Description
19	0b	RW	**GPIO Input Route SCI (GPIROUTSCI)** Determines if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI. 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s).
18	0b	RO	**GPIO Input Route SMI (GPIROUTSMI)** Determines if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s). This bit only applies to a GPIO that has SMI capability. Otherwise, the bit is RO.
17	0b	RO	**GPIO Input Route NMI (GPIROUTNMI)** Determines if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit. This bit only applies to a GPIO that has NMI capability. Otherwise, the bit is RO.
16:12	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
11:10	See Description	RW	**Pad Mode (PMODE)** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad. 1h = native function 1, if applicable, controls the Pad 2h = native function 2, if applicable, controls the Pad. 3h = native function 3, if applicable, controls the Pad Dedicated (unmuxed) GPIO shall report RO of all 0's in this register field If GPIO vs. native mode is configured via soft strap, this bit has no effect. Default value is determined by the default functionality of the pad.
9	1b	RW	**GPIO RX Disable (GPIORXDIS)** 0 = Enable the input buffer (active low enable) of the pad. 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0'.
8	1b	RW	**GPIO TX Disable (GPIOTXDIS)** 0 = Enable the output buffer (active low enable) of the pad. 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	-	-	**Reserved**
1		RO/V	**GPIO RX State (GPIORXSTATE)** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV settings.
0	0b	RW	**GPIO TX State (GPIOTXSTATE)** 0 = Drive a level '0' to the TX output pad. 1 = Drive a level '1' to the TX output pad.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_0) – Offset 604

This register applies to GPP_A0

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13:10	See Description	RW	**Termination (TERM)** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. Others: Reserved NOTES: 1.The 20K ull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. All other bit encodings are reserved. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily.
9:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	18h	RO	**Interrupt Select (INTSEL)** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 .... Up to the max IOxAPIC IRQ supported

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_1) – Offset 610

This register applies to GPP_A1 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_1) – Offset 614

This register applies to GPP_A1 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 19h

TERM bit field default:

1111b in LPC mode. Note that TERM bit field must be set to 1111b when the signal is used as native function.1100b in eSPI mode

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_2) – Offset 620

This register applies to GPP_A2 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_2) – Offset 624

This register applies to GPP_A2 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 1Ah

TERM bit field default:

1111b in LPC mode. Note that TERM bit field must be set to 1111b when the signal is used as native function.

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Family Base Address (FAMBAR) – Offset 8

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	300h	RO	**Family Base Address (FAMBAR)** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

Pad Base Address (PADBAR) – Offset c

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	600h	RO	**Pad Base Address (PADBAR)** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

Miscellaneous Configuration (MISCCFG) – Offset 10

Bit Range	Default	Access	Field Name and Description
31:24	32h	RW	**GPIO Driver Mode Interrupt Select (GPDMINTSEL)** IRQ globally for all pads (GPI_IS with corresponding GPI_IE enable). 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255
23:20	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
19:16	0100b	RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2)** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 1h = GPP_B[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 2h = GPP_G[7:0] mapped to GPE[71:64]; GPE[95:72] not used. 3h = Reserved. 4h = GPP_C[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 5h = GPP_D[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 6h = GPP_F[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 7h = GPP_H[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 8h = vGPIO39 (vSD_CD#) mapped to GPE bit 70. 9h = Reserved Ah = GPD[11:0] mapped to GPE[75:64]; GPE[95:76] not used Bh - Ch = Reserved Dh = GPP_E[23:0] mapped to GPE[87:64]; GPE[95:88] not used. Eh - Fh = Reserved
15:12	0011b	RW	

Bit Range	Default	Access	GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1) Field Name and Description
			This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 1h = GPP_B[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 2h = GPP_G[7:0] mapped to GPE[39:32]; GPE[63:40] not used. 3h = Reserved. 4h = GPP_C[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 5h = GPP_D[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 6h = GPP_F[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 7h = GPP_H[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 8h = vGPIO39 (vSD_CD#) mapped to GPE bit 38. 9h = Reserved Ah = GPD[11:0] mapped to GPE[43:32]; GPE[63:44] not used Bh - Ch = Reserved Dh = GPP_E[23:0] mapped to GPE[55:32]; GPE[63:56] not used. Dh = GPP_E[23:0] mapped to GPE[55:32]; GPE[63:56] not used. Eh - Fh = Reserved

Bit Range	Default	Access	Field Name and Description
11:8	0010b	RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0)** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 1h = GPP_B[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 2h = GPP_G[7:0] mapped to GPE[7:0]; GPE[31:8] not used. 3h = Reserved. 4h = GPP_C[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 5h = GPP_D[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 6h = GPP_F[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 7h = GPP_H[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 8h = vGPIO_39 (vSD_CD#) mapped to GPE bit 7. 9h = Reserved Ah = GPD[11:0] mapped to GPE[11:0]; GPE[31:12] not used Bh - Ch = Reserved Dh = GPP_E[23:0] mapped to GPE[23:0]; GPE[31:24] not used Eh - Fh = Reserved
7:2	-	-	**Reserved**
1	0b	RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN)** Specifies whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN)** Specifies whether the GPIO Community should perform local clock gating. 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating

Pad Ownership (PAD_OWN_GPP_A_0) – Offset 20

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29:28	00b	RW	**Pad Ownership (PAD_OWN_GPPC_A_7)** Same description as bits [1:0], except that the bit field applies to GPP_A7.
27:26	-	-	**Reserved**
25:24	00b	RW	**Pad Ownership (PAD_OWN_GPPC_A_6)** Same description as bits [1:0], except that the bit field applies to GPP_A6.
23:22	-	-	**Reserved**
21:20	00b	RW	**Pad Ownership (PAD_OWN_GPPC_A_5)** Same description as bits [1:0], except that the bit field applies to GPP_A5.
19:18	-	-	**Reserved**
17:16	00b	RW	**Pad Ownership (PAD_OWN_GPPC_A_4)** Same description as bits [1:0], except that the bit field applies to GPP_A4.

Bit Range	Default	Access	Field Name and Description
15:14	-	-	**Reserved**
13:12	00b	RW	**Pad Ownership (PAD_OWN_GPPC_A_3)** Same description as bits [1:0], except that the bit field applies to GPP_A3.
11:10	-	-	**Reserved**
9:8	00b	RW	**Pad Ownership (PAD_OWN_GPPC_A_2)** Same description as bits [1:0], except that the bit field applies to GPP_A2.
7:6	-	-	**Reserved**
5:4	00b	RW	**Pad Ownership (PAD_OWN_GPPC_A_1)** Same description as bits [1:0], except that the bit field applies to GPP_A1.
3:2	-	-	**Reserved**
1:0	00b	RW	**Pad Ownership (PAD_OWN_GPPC_A_0)** 00 = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIODriver) has ownership of the pad. In Host GPIO Driver Mode (refer toHOSTSW_OWN), GPIO input event update is limited to GPI_STS update only.Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STSand/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership 01 = ME GPIO Mode. ME has ownership of the pad. 10 = ISH GPIO Mode. ME has ownership of the pad 11 = Reserved

Pad Ownership (PAD_OWN_GPP_A_1) – Offset 24

Same description as PAD_OWN_GPP_A_0, except that this register is for GPP_A[15:8].

Pad Ownership (PAD_OWN_GPP_A_2) – Offset 28

Same description as PAD_OWN_GPP_A_0, except that this register is for GPP_A[23:16].

Pad Ownership (PAD_OWN_GPP_B_0) – Offset 30

Same description as PAD_OWN_GPP_A_0, except that this register is for GPP_B[7:0].

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_3) – Offset 630

This register applies to GPP_A3 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_3) – Offset 634

This register applies to GPP_A3 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 1Bh

TERM bit field default:

1111b in LPC mode. Note that TERM bit field must be set to 1111b when the signal is used as native function.

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Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_4) – Offset 640

This register applies to GPP_A4 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_4) – Offset 644

This register applies to GPP_A4 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 1Ch

TERM bit field default:

1111b in LPC mode. Note that TERM bit field must be set to 1111b when the signal is used as native function.

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Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_5) – Offset 650

This register applies to GPP_A5 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_5) – Offset 654

This register applies to GPP_A5 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 1Dh

TERM bit field default: 0000b.

Pad Ownership (PAD_OWN_GPP_B_1) – Offset 34

Same description as PAD_OWN_GPP_A_0, except that this register is for GPP_B[15:8]

Pad Ownership (PAD_OWN_GPP_B_2) – Offset 38

Same description as PAD_OWN_GPP_A_0, except that this register is for GPP_B[23:16]

Pad Ownership (PAD_OWN_GPP_G_0) – Offset 40

Same description as PAD_OWN_GPP_A_0, except that this register is for GPP_G[7:0].

Pad Configuration Lock (PADCFGLOCK_GPP_A_0) – Offset 80

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_23)** Applied to GPP_A23. Same description as PADCFGLOCK_GPP_A_0.
22	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_22)** Applied to GPP_A22. Same description as PADCFGLOCK_GPP_A_0.
21	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_21)** Applied to GPP_A21. Same description as PADCFGLOCK_GPP_A_0.
20	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_20)** Applied to GPP_A20. Same description as PADCFGLOCK_GPP_A_0.
19	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_19)** Applied to GPP_A19. Same description as PADCFGLOCK_GPP_A_0.
18	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_18)** Applied to GPP_A18. Same description as PADCFGLOCK_GPP_A_0.

Bit Range	Default	Access	Field Name and Description
17	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_17)** Applied to GPP_A17. Same description as PADCFGLOCK_GPP_A_0.
16	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_16)** Applied to GPP_A16. Same description as PADCFGLOCK_GPP_A_0.
15	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_15)** Applied to GPP_A15. Same description as PADCFGLOCK_GPP_A_0.
14	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_14)** Applied to GPP_A14. Same description as PADCFGLOCK_GPP_A_0.
13	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_13)** Applied to GPP_A13. Same description as PADCFGLOCK_GPP_A_0.
12	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_12)** Applied to GPP_A12. Same description as PADCFGLOCK_GPP_A_0.
11	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_11)** Applied to GPP_A11. Same description as PADCFGLOCK_GPP_A_0.
10	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_10)** Applied to GPP_A10. Same description as PADCFGLOCK_GPP_A_0.
9	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_9)** Applied to GPP_A9. Same description as PADCFGLOCK_GPP_A_0.
8	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_8)** Applied to GPP_A8. Same description as PADCFGLOCK_GPP_A_0.
7	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_7)** Applied to GPP_A7. Same description as PADCFGLOCK_GPP_A_0.
6	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_6)** Applied to GPP_A6. Same description as PADCFGLOCK_GPP_A_0.
5	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_5)** Applied to GPP_A5. Same description as PADCFGLOCK_GPP_A_0.
4	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_4)** Applied to GPP_A4. Same description as PADCFGLOCK_GPP_A_0.

Bit Range	Default	Access	Field Name and Description
3	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_3)** Applied to GPP_A3. Same description as PADCFGLOCK_GPP_A_0.
2	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_2)** Applied to GPP_A2. Same description as PADCFGLOCK_GPP_A_0.
1	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_1)** Applied to GPP_A1. Same description as PADCFGLOCK_GPP_A_0.
0	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_A_0)** Pad Configuration Lock locks specific register fields in the GPP specific registers from being configured. The registers affected become Read-Only and software writes to these registers have no effect. 0 = Unlock 1 = Lock the following register fields as read-only (RO): - Pad Configuration registers (exclude GPIOTXState) - GPI_NMI_EN Register (if implemented) - GPI_SMI_EN Register (if implemented) - GPI_GPE_EN Register (if implemented) When PadCfgLock is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_A_0) – Offset 84

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_23)** Applied to GPP_A23. Same description as PADCFGLOCKTX_GPP_A_0

Bit Range	Default	Access	Field Name and Description
22	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_22)** Applied to GPP_A22. Same description as PADCFGLOCKTX_GPP_A_0
21	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_21)** Applied to GPP_A21. Same description as PADCFGLOCKTX_GPP_A_0
20	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_20)** Applied to GPP_A20. Same description as PADCFGLOCKTX_GPP_A_0
19	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_19)** Applied to GPP_A19. Same description as PADCFGLOCKTX_GPP_A_0
18	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_18)** Applied to GPP_A18. Same description as PADCFGLOCKTX_GPP_A_0
17	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_17)** Applied to GPP_A17. Same description as PADCFGLOCKTX_GPP_A_0
16	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_16)** Applied to GPP_A16. Same description as PADCFGLOCKTX_GPP_A_0
15	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_15)** Applied to GPP_A15. Same description as PADCFGLOCKTX_GPP_A_0
14	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_14)** Applied to GPP_A14. Same description as PADCFGLOCKTX_GPP_A_0
13	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_13)** Applied to GPP_A13. Same description as PADCFGLOCKTX_GPP_A_0
12	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_12)** Applied to GPP_A12. Same description as PADCFGLOCKTX_GPP_A_0
11	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_11)** Applied to GPP_A11. Same description as PADCFGLOCKTX_GPP_A_0
10	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_10)** Applied to GPP_A10. Same description as PADCFGLOCKTX_GPP_A_0
9	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_9)** Applied to GPP_A9. Same description as PADCFGLOCKTX_GPP_A_0

Bit Range	Default	Access	Field Name and Description
8	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_8)** Applied to GPP_A8. Same description as PADCFGLOCKTX_GPP_A_0
7	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_7)** Applied to GPP_A7. Same description as PADCFGLOCKTX_GPP_A_0
6	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_6)** Applied to GPP_A6. Same description as PADCFGLOCKTX_GPP_A_0
5	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_5)** Applied to GPP_A5. Same description as PADCFGLOCKTX_GPP_A_0
4	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_4)** Applied to GPP_A4. Same description as PADCFGLOCKTX_GPP_A_0.
3	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_3)** Applied to GPP_A3. Same description as PADCFGLOCKTX_GPP_A_0.
2	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_2)** Applied to GPP_A2. Same description as PADCFGLOCKTX_GPP_A_0.
1	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_1)** Applied to GPP_A1. Same description as PADCFGLOCKTX_GPP_A_0
0	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_A_0)** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) When PadCfgLockTx is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

Pad Configuration Lock (PADCFGLOCK_GPP_B_0) – Offset 88

Same description as PADCFGLOCK_GPP_A_0 register, except this register applies to GPP_B[23:0].

Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_B_0) – Offset 8c

Same description as PADCFGLOCKTX_GPP_A_0 register, except that this register applies to GPP_B[23:0].

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_6) – Offset 660

This register applies to GPP_A6 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_6) – Offset 664

This register applies to GPP_A6 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 1Eh

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_7) – Offset 670

This register applies to GPP_A7 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_7) – Offset 674

This register applies to GPP_A7 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 1Fh

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_8) – Offset 680

This register applies to GPP_A8 and has the same description as PAD_CFG_DW0_GPP_A_0.

Exception: the PMODE bit is RO/V bit.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_8) – Offset 684

This register applies to GPP_A8 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 20h

TERM bit field default: 0000b.

Pad Configuration Lock (PADCFGLOCK_GPP_G_0) – Offset 90

Same description as PADCFGLOCK_GPP_A_0 register, except this register applies to GPP_G[7:0].

Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_G_0) – Offset 94

Same description as PADCFGLOCKTX_GPP_A_0 register, except this register applies to GPP_G[7:0].

Host Software Pad Ownership (HOSTSW_OWN_GPP_A_0) – Offset b0

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_23)** Applied to GPP_A23. Same description as bit 0.
22	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_22)** Applied to GPP_A22. Same description as bit 0.
21	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_21)** Applied to GPP_A21. Same description as bit 0.
20	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_20)** Applied to GPP_A20. Same description as bit 0.
19	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_19)** Applied to GPP_A19. Same description as bit 0.
18	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_18)** Applied to GPP_A18. Same description as bit 0.
17	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_17)** Applied to GPP_A17. Same description as bit 0.
16	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_16)** Applied to GPP_A16. Same description as bit 0.
15	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_15)** Applied to GPP_A15. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
14	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_14)** Applied to GPP_A14. Same description as bit 0.
13	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_13)** Applied to GPP_A13. Same description as bit 0.
12	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_12)** Applied to GPP_A12. Same description as bit 0.
11	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_11)** Applied to GPP_A11. Same description as bit 0.
10	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_10)** Applied to GPP_A10. Same description as bit 0.
9	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_9)** Applied to GPP_A9. Same description as bit 0.
8	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_8)** Applied to GPP_A8. Same description as bit 0.
7	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_7)** Applied to GPP_A7. Same description as bit 0.
6	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_6)** Applied to GPP_A6. Same description as bit 0.
5	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_5)** Applied to GPP_A5. Same description as bit 0.
4	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_4)** Applied to GPP_A4. Same description as bit 0.
3	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_3)** Applied to GPP_A3. Same description as bit 0.
2	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_2)** Applied to GPP_A2. Same description as bit 0.
1	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_1)** Applied to GPP_A1. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_A_0)** This register determines the appropriate host status bit update when a pad is under host ownership. 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS,GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited toGPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updatesare masked.

Host Software Pad Ownership (HOSTSW_OWN_GPP_B_0) – Offset b4

Same description as HOSTSW_OWN_GPP_A_0 register, except that this register applies to GPP_B[23:0].

Host Software Pad Ownership (HOSTSW_OWN_GPP_G_0) – Offset b8

Same description as HOSTSW_OWN_GPP_A_0 register, except this register applies to GPP_G[7:0].

GPI Interrupt Status (GPI_IS_GPP_A_0) – Offset 100

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_23)** Applied to GPP_A23. Same description as bit 0.
22	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_22)** Applied to GPP_A22. Same description as bit 0.
21	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_21)** Applied to GPP_A21. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
20	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_20)** Applied to GPP_A20. Same description as bit 0.
19	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_19)** Applied to GPP_A19. Same description as bit 0.
18	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_18)** Applied to GPP_A18. Same description as bit 0.
17	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_17)** Applied to GPP_A17. Same description as bit 0.
16	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_16)** Applied to GPP_A16. Same description as bit 0.
15	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_15)** Applied to GPP_A15. Same description as bit 0.
14	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_14)** Applied to GPP_A14. Same description as bit 0.
13	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_13)** Applied to GPP_A13. Same description as bit 0.
12	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_12)** Applied to GPP_A12. Same description as bit 0.
11	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_11)** Applied to GPP_A11. Same description as bit 0.
10	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_10)** Applied to GPP_A10. Same description as bit 0.
9	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_9)** Applied to GPP_A9. Same description as bit 0.
8	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_8)** Applied to GPP_A8. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
7	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_7)** Applied to GPP_A7. Same description as bit 0.
6	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_6)** Applied to GPP_A6. Same description as bit 0.
5	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_5)** Applied to GPP_A5. Same description as bit 0.
4	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_4)** Applied to GPP_A4. Same description as bit 0.
3	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_3)** Applied to GPP_A3. Same description as bit 0.
2	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_2)** Applied to GPP_A2. Same description as bit 0.
1	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_1)** Applied to GPP_A1. Same description as bit 0.
0	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_A_0)** GPI Interrupt Status (GPI_INT_STS) This bit is set to '1' by hardware when either an edge or a level event isdetected (See RxEdCfg RxInv) on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode - HOSTSW_OWN = 1 (i.e. Host GPIO Driver Mode). Writing a value of 1 will clear the bit while writing a value of 0 has noeffect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x].

GPI Interrupt Status (GPI_IS_GPP_B_0) – Offset 104

Same description as GPI_IS_GPP_A_0 register, except that this register applies to GPP_B[23:0].

GPI Interrupt Status (GPI_IS_GPP_G_0) – Offset 108

Same description as GPI_IS_GPP_A_0 register, except that this register applies to GPP_G[7:0].

GPI Interrupt Enable (GPI_IE_GPP_A_0) – Offset 120

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_23)** Applied to GPP_A23. Same description as bit 0.
22	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_22)** Applied to GPP_A22. Same description as bit 0.
21	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_21)** Applied to GPP_A21. Same description as bit 0.
20	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_20)** Applied to GPP_A20. Same description as bit 0.
19	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_19)** Applied to GPP_A19. Same description as bit 0.
18	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_18)** Applied to GPP_A18. Same description as bit 0.
17	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_17)** Applied to GPP_A17. Same description as bit 0.
16	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_16)** Applied to GPP_A16. Same description as bit 0.
15	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_15)** Applied to GPP_A15. Same description as bit 0.
14	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_14)** Applied to GPP_A14. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
13	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_13)** Applied to GPP_A13. Same description as bit 0.
12	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_12)** Applied to GPP_A12. Same description as bit 0.
11	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_11)** Applied to GPP_A11. Same description as bit 0.
10	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_10)** Applied to GPP_A10. Same description as bit 0.
9	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_9)** Applied to GPP_A9. Same description as bit 0.
8	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_8)** Applied to GPP_A8. Same description as bit 0.
7	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_7)** Applied to GPP_A7. Same description as bit 0.
6	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_6)** Applied to GPP_A6. Same description as bit 0.
5	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_5)** Applied to GPP_A5. Same description as bit 0.
4	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_4)** Applied to GPP_A4. Same description as bit 0.
3	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_3)** Applied to GPP_A3. Same description as bit 0.
2	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_2)** Applied to GPP_A2. Same description as bit 0.
1	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_1)** Applied to GPP_A1. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_A_0)** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation

GPI Interrupt Enable (GPI_IE_GPP_B_0) – Offset 124

Same description as GPI_IE_GPP_A_0 register, except that this register is for GPP_B[23:0].

GPI Interrupt Enable (GPI_IE_GPP_G_0) – Offset 128

Same description as GPI_IE_GPP_A_0 register, except that this register applies to GPP_G[7:0].

GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_0) – Offset 140

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_23)** Applied to GPP_A23. Same description as bit 0.
22	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_22)** Applied to GPP_A22. Same description as bit 0.
21	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_21)** Applied to GPP_A21. Same description as bit 0.
20	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_20)** Applied to GPP_A20. Same description as bit 0.
19	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_19)** Applied to GPP_A19. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
18	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_18)** Applied to GPP_A18. Same description as bit 0.
17	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_17)** Applied to GPP_A17. Same description as bit 0.
16	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_16)** Applied to GPP_A16. Same description as bit 0.
15	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_15)** Applied to GPP_A15. Same description as bit 0.
14	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_14)** Applied to GPP_A14. Same description as bit 0.
13	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_13)** Applied to GPP_A13. Same description as bit 0.
12	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_12)** Applied to GPP_A12. Same description as bit 0.
11	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_11)** Applied to GPP_A11. Same description as bit 0.
10	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_10)** Applied to GPP_A10. Same description as bit 0.
9	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_9)** Applied to GPP_A9. Same description as bit 0.
8	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_8)** Applied to GPP_A8. Same description as bit 0.
7	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_7)** Applied to GPP_A7. Same description as bit 0.
6	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_6)** Applied to GPP_A6. Same description as bit 0.
5	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_5)** Applied to GPP_A5. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
4	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_4)** Applied to GPP_A4. Same description as bit 0.
3	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_3)** Applied to GPP_A3. Same description as bit 0.
2	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_2)** Applied to GPP_A2. Same description as bit 0.
1	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_1)** Applied to GPP_A1. Same description as bit 0.
0	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_A_0)** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high(or low if the corresponding RXINV bit is set). If the correspondingenable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: - If the system is in an S3-S5 state, the event will also wake the system. - If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for thecorresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS.

GPI General Purpose Events Status (GPI_GPE_STS_GPP_B_0) – Offset 144

Same description as PI_GPE_STS_GPP_A_0 register, except that this is for GPP_B[23:0].

GPI General Purpose Events Status (GPI_GPE_STS_GPP_G_0) – Offset 148

Same description as GPI_GPE_STS_GPP_A_0 register, except that this register applies to GPP_G[7:0].

GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_0) – Offset 160

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_23)** Applied to GPP_A23. Same description as bit 0.
22	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_22)** Applied to GPP_A22. Same description as bit 0.
21	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_21)** Applied to GPP_A21. Same description as bit 0.
20	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_20)** Applied to GPP_A20. Same description as bit 0.
19	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_19)** Applied to GPP_A19. Same description as bit 0.
18	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_18)** Applied to GPP_A18. Same description as bit 0.
17	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_17)** Applied to GPP_A17. Same description as bit 0.
16	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_16)** Applied to GPP_A16. Same description as bit 0.
15	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_15)** Applied to GPP_A15. Same description as bit 0.
14	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_14)** Applied to GPP_A14. Same description as bit 0.
13	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_13)** Applied to GPP_A13. Same description as bit 0.
12	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_12)** Applied to GPP_A12. Same description as bit 0.
11	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_11)** Applied to GPP_A11. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
10	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_10)** Applied to GPP_A10. Same description as bit 0.
9	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_9)** Applied to GPP_A9. Same description as bit 0.
8	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_8)** Applied to GPP_A8. Same description as bit 0.
7	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_7)** Applied to GPP_A7. Same description as bit 0.
6	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_6)** Applied to GPP_A6. Same description as bit 0.
5	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_5)** Applied to GPP_A5. Same description as bit 0.
4	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_4)** Applied to GPP_A4. Same description as bit 0.
3	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_3)** Applied to GPP_A3. Same description as bit 0.
2	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_2)** Applied to GPP_A2. Same description as bit 0.
1	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_1)** Applied to GPP_A1. Same description as bit 0.
0	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_A_0)** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note:The pad must also be routed for GPE functionality in order for GPE tobe generated, i.e. the corresponding GPIRoutSCI must be set to '1'.

GPI General Purpose Events Enable (GPI_GPE_EN_GPP_B_0) – Offset 164

Same description as GPI_GPE_EN_GPP_A_0 register, except that this is for GPP_B[23:0].

GPI General Purpose Events Enable (GPI_GPE_EN_GPP_G_0) – Offset 168

Same description as GPI_GPE_EN_GPP_A_0 register, except that this register applies to GPP_G[7:0].

SMI Status (GPI_SMI_STS_GPP_B_0) – Offset 184

Register bits in this register are implemented for GPP_B signals that have SMI capability only. Other bits are reserved and RO.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_B_23)** Same description as bit 14.
22:21	-	-	**Reserved**
20	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_B_20)** Same description as bit 14.
19:15	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
14	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_B_14)** This bit is set to 1 by hardware when a level event (See RxEdCfg,RxInv) is detected, and all the following conditions are true: - The corresponding pad is used in GPIO input mode - The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if theGPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of 1 will clear the bit while writing a value of 0 has noeffect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN does not prevent the setting of GPI_SMI_STS. Defaults for these bits are dependent on the state of the GPI pads.
13:0	-	-	**Reserved**

SMI Enable (GPI_SMI_EN_GPP_B_0) – Offset 1a4

Register bits in this register are implemented for GPP_B signals that have SMI capability only. Other bits are reserved and

RO.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_23)** Same description as bit 14.
22:21	-	-	**Reserved**
20	0b	RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_20)** Same description as bit 14.
19:15	-	-	**Reserved**
14	0b	RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_14)** This bit is used to enable/disable the generation of SMI when thecorresponding GPI_SMI_STS bit is set. The pad must also be routed forSMI functionality in order for SMI to be generated, i.e. the correspondingGPIROUTSMI must be set to 1. 0 = disable SMI generation 1 = enable SMI generation Note:Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is 1, bit0 of this bit is locked down to read-only.
13:0	-	-	**Reserved**

NMI Status (GPI_NMI_STS_GPP_B_0) – Offset 1c4

Register bits in this register are implemented for GPP_B signals that have NMI capability only. Other bits are reserved and RO.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
23	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_B_23)** Same description as bit 14.
22:21	-	-	**Reserved**
20	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_B_20)** Same description as bit 14.
19:15	-	-	**Reserved**
14	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_B_14)** This bit is set to 1 by hardware when an edge event is detected (SeeRxEdCfg, RxInv) on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode (PMode) - The corresponding GPIONMIRout is set to 1, i.e. programmed toroute as NMI - The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). - The corresponding GPI_NMI_EN is set Writing a value of 1 will clear the bit while writing a value of 0 has noeffect. 0 = There is no NMI event 1 = There is an NMI event
13:0	-	-	**Reserved**

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_9) – Offset 690

This register applies to GPP_A9 and has the same description as PAD_CFG_DW0_GPP_A_0.

Exception: the PMODE bit is RO/V bit.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_9) – Offset 694

This register applies to GPP_A9 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 21h

TERM bit field default: 0100b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_10) – Offset 6a0

This register applies to GPP_A10 and has the same description as PAD_CFG_DW0_GPP_A_0.

Exception: the PMODE bit is RO/V bit.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_10) – Offset 6a4

This register applies to GPP_A10 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 22h

TERM bit field default: 0100b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_11) – Offset 6b0

This register applies to GPP_A11 and has the same description as PAD_CFG_DW2_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_11) – Offset 6b4

This register applies to GPP_A11 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 23h

TERM bit field default: 1100b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_12) – Offset 6c0

This register applies to GPP_A12 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_12) – Offset 6c4

This register applies to GPP_A12 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 24h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_13) – Offset 6d0

This register applies to GPP_A13 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_13) – Offset 6d4

This register applies to GPP_A13 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 25h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_14) – Offset 6e0

This register applies to GPP_A14 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_14) – Offset 6e4

This register applies to GPP_A14 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 26h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_15) – Offset 6f0

This register applies to GPP_A15 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_15) – Offset 6f4

This register applies to GPP_A15 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 27h

TERM bit field default: 1100b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_16) – Offset 700

This register applies to GPP_A16 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_16) – Offset 704

This register applies to GPP_A16 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 28h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_17) – Offset 710

This register applies to GPP_A17 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_17) – Offset 714

This register applies to GPP_A17 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 29h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_18) – Offset 720

This register applies to GPP_A18 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_18) – Offset 724

This register applies to GPP_A18 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 2Ah

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_19) – Offset 730

This register applies to GPP_A19 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_19) – Offset 734

This register applies to GPP_A19 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 2Bh

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_20) – Offset 740

This register applies to GPP_A20 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_20) – Offset 744

This register applies to GPP_A20 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 2Ch

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_21) – Offset 750

This register applies to GPP_A21 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_21) – Offset 754

This register applies to GPP_A21 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 2Dh

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_22) – Offset 760

This register applies to GPP_A22 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_22) – Offset 764

This register applies to GPP_A22 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 2Eh

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_23) – Offset 770

This register applies to GPP_A23 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_23) – Offset 774

This register applies to GPP_A23 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 2Fh

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_0) – Offset 790

This register applies to GPP_B0 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_0) – Offset 794

This register applies to GPP_B0 and has the same description as PAD_CFG_DW1_GPP_A_0.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_1) – Offset 7a0

This register applies to GPP_B1 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_1) – Offset 7a4

This register applies to GPP_B1 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 31h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_2) – Offset 7b0

This register applies to GPP_B2 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_2) – Offset 7b4

This register applies to GPP_B2 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 32h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_3) – Offset 7c0

This register applies to GPP_B3 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_3) – Offset 7c4

This register applies to GPP_B3 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 33h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_4) – Offset 7d0

This register applies to GPP_B4 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_4) – Offset 7d4

This register applies to GPP_B4 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 34h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_5) – Offset 7e0

This register applies to GPP_B5 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_5) – Offset 7e4

This register applies to GPP_B5 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 35h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_6) – Offset 7f0

This register applies to GPP_B6 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_6) – Offset 7f4

This register applies to GPP_B6 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 36h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_7) – Offset 800

This register applies to GPP_B7 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_7) – Offset 804

This register applies to GPP_B7 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 37h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_8) – Offset 810

This register applies to GPP_B8 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_8) – Offset 814

This register applies to GPP_B8 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 38h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_9) – Offset 820

This register applies to GPP_B9 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_9) – Offset 824

This register applies to GPP_B9 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 39h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_10) – Offset 830

This register applies to GPP_B10 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_10) – Offset 834

This register applies to GPP_B10 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 3Ah

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_11) – Offset 840

This register applies to GPP_B11 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_11) – Offset 844

This register applies to GPP_B11 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 3Bh

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_12) – Offset 850

This register applies to GPP_B12 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_12) – Offset 854

This register applies to GPP_B12 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 3Ch

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_13) – Offset 860

This register applies to GPP_B13 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_13) – Offset 864

This register applies to GPP_B13 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 3Dh

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_14) – Offset 870

This register applies to GPP_B14 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_14) – Offset 874

This register applies to GPP_B14 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 3Eh

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_15) – Offset 880

This register applies to GPP_B15 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_15) – Offset 884

This register applies to GPP_B15 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 3Fh

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_16) – Offset 890

This register applies to GPP_B16 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_16) – Offset 894

This register applies to GPP_B16 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 40h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_17) – Offset 8a0

This register applies to GPP_B17 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_17) – Offset 8a4

This register applies to GPP_B17 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 41h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_18) – Offset 8b0

This register applies to GPP_B18 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_18) – Offset 8b4

This register applies to GPP_B18 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 42h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_19) – Offset 8c0

This register applies to GPP_B19 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_19) – Offset 8c4

This register applies to GPP_B19 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 43h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_20) – Offset 8d0

This register applies to GPP_B20 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_20) – Offset 8d4

This register applies to GPP_B20 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 44h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_21) – Offset 8e0

This register applies to GPP_B21 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_21) – Offset 8e4

This register applies to GPP_B21 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 45h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_22) – Offset 8f0

This register applies to GPP_B22 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_22) – Offset 8f4

This register applies to GPP_B22 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 46h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_23) – Offset 900

This register applies to GPP_B23 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_23) – Offset 904

This register applies to GPP_B23 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 47h

TERM bit field default: 0000b.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_0) – Offset 930

This register applies to GPP_G0 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_0) – Offset 934

This register applies to GPP_G0 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 6Ch

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_1) – Offset 940

This register applies to GPP_G1 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_1) – Offset 944

This register applies to GPP_G1 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 6Dh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_2) – Offset 950

This register applies to GPP_G2 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_2) – Offset 954

This register applies to GPP_G2 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 6Eh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_3) – Offset 960

This register applies to GPP_G3 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_3) – Offset 964

This register applies to GPP_G3 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 6Fh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_4) – Offset 970

This register applies to GPP_G4 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_4) – Offset 974

This register applies to GPP_G4 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 70h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_5) – Offset 980

This register applies to GPP_G5 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_5) – Offset 984

This register applies to GPP_G5 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 71h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_6) – Offset 990

This register applies to GPP_G6 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_6) – Offset 994

This register applies to GPP_G6 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 72h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_G_7) – Offset 9a0

This register applies to GPP_G7 and has the same description as PAD_CFG_DW0_GPP_A_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_G_7) – Offset 9a4

This register applies to GPP_G7 and has the same description as PAD_CFG_DW1_GPP_A_0.

Exception:

INTSEL bit field default: 73h

NMI Enable (GPI_NMI_EN_GPP_B_0) – Offset 1e4

Register bits in this register are implemented for GPP_B signals that have NMI capability only. Other bits are reserved and RO.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_23)** Same description as bit 14.
22:21	-	-	**Reserved**
20	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_20)** Same description as bit 14.
19:15	-	-	**Reserved**
14	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_14)** This bit is used to enable/disable the generation of NMI when thecorresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configurationregister PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 ofthis bit is locked down to read-only.
13:0	-	-	**Reserved**

GPIO Community 1 Registers

GPIO pins are grouped into different Community (Example: Community 0, Community1, etc.). Each Community consists of one or more GPIO groups.

This section covers registers for Community 1, which consists of GPP_D, GPP_F, GPP_H,groups, and vGPIO39.

These registers are within the PCH Private Configuration Space which is accessiblethrough the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
180h	4	SMI Status (GPI_SMI_STS_GPP_D_0)	0h
1a0h	4	SMI Enable (GPI_SMI_EN_GPP_D_0)	0h
1c0h	4	NMI Status (GPI_NMI_STS_GPP_D_0)	0h
1e0h	4	NMI Enable (GPI_NMI_EN_GPP_D_0)	0h
204h	4	PWM Control (PWMC)	0h
20ch	4	GPIO Serial Blink Enable (GP_SER_BLINK)	0h
8h	4	Family Base Address (FAMBAR)	300h
ch	4	Pad Base Address (PADBAR)	600h
10h	4	Miscellaneous Configuration (MISCCFG)	43200h
20h	4	Pad Ownership (PAD_OWN_GPP_D_0)	0h
24h	4	Pad Ownership (PAD_OWN_GPP_D_1)	0h
28h	4	Pad Ownership (PAD_OWN_GPP_D_2)	0h
30h	4	Pad Ownership (PAD_OWN_GPP_F_0)	0h
34h	4	Pad Ownership (PAD_OWN_GPP_F_1)	0h
38h	4	Pad Ownership (PAD_OWN_GPP_F_2)	0h
3ch	4	Pad Ownership (PAD_OWN_GPP_H_0)	0h
40h	4	Pad Ownership (PAD_OWN_GPP_H_1)	0h
44h	4	Pad Ownership (PAD_OWN_GPP_H_2)	0h
80h	4	Pad Configuration Lock (PADCFGLOCK_GPP_D_0)	0h
84h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_D_0)	0h
210h	4	GPIO Serial Blink Command/Status (GP_SER_CMDSTS)	80000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
214h	4	GPIO Serial Blink Data (GP_SER_DATA)	0h
600h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_0)	44000X00h. Refer to register for X value
604h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_0)	See Register
610h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_1)	44000X00h. Refer to register for X value
614h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_1)	See Register
620h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_2)	44000X00h. Refer to register for X value
88h	4	Pad Configuration Lock (PADCFGLOCK_GPP_F_0)	0h
8ch	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_F_0)	0h
90h	4	Pad Configuration Lock (PADCFGLOCK_GPP_H_0)	0h
94h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_H_0)	0h
b0h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_D_0)	0h
b4h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_F_0)	0h
b8h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_H_0)	0h
624h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_2)	See Register
630h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_3)	44000X00h. Refer to register for X value

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
634h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_3)	See Register
640h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_4)	44000X00h. Refer to register for X value
644h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_4)	See Register
650h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_5)	44000X00h. Refer to register for X value
654h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_5)	See Register
660h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_6)	44000X00h. Refer to register for X value
664h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_6)	See Register
670h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_7)	44000X00h. Refer to register for X value
674h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_7)	See Register
680h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_8)	44000X00h. Refer to register for X value
684h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_8)	See Register
690h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_9)	44000X00h. Refer to register for X value
694h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_9)	See Register
6a0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_10)	44000X00h. Refer to register for X value
6a4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_10)	See Register
6b0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_11)	44000X00h. Refer to register for X value

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
6b4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_11)	See Register
6c0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_12)	44000X00h. Refer to register for X value
6c4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_12)	See Register
6d0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_13)	44000X00h. Refer to register for X value
6d4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_13)	See Register
6e0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_14)	44000X00h. Refer to register for X value
6e4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_14)	See Register
6f0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_15)	44000X00h. Refer to register for X value
6f4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_15)	See Register
700h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_16)	44000X00h. Refer to register for X value
704h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_16)	See Register
710h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_17)	44000X00h. Refer to register for X value
714h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_17)	See Register
720h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_18)	44000X00h. Refer to register for X value
724h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_18)	See Register
730h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_19)	44000X00h. Refer to register for X value

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
734h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_19)	See Register
740h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_20)	44000X00h. Refer to register for X value
744h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_20)	See Register
750h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_21)	44000X00h. Refer to register for X value
754h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_21)	See Register
760h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_22)	44000X00h. Refer to register for X value
764h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_22)	See Register
770h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_23)	44000X00h. Refer to register for X value
774h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_23)	See Register
790h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_0)	44000X00h. Refer to register for X value
794h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_0)	See Register
7a0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_1)	44000X00h. Refer to register for X value
7a4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_1)	See Register
7b0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_2)	44000X00h. Refer to register for X value
7b4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_2)	See Register

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
c0h	4	Host Software Pad Ownership (HOSTSW_OWN_vGPIO_1)	0h
100h	4	GPI Interrupt Status (GPI_IS_GPP_D_0)	0h
104h	4	GPI Interrupt Status (GPI_IS_GPP_F_0)	0h
108h	4	GPI Interrupt Status (GPI_IS_GPP_H_0)	0h
110h	4	GPI Interrupt Status (GPI_IS_vGPIO_1)	0h
120h	4	GPI Interrupt Enable (GPI_IE_GPP_D_0)	0h
124h	4	GPI Interrupt Enable (GPI_IE_GPP_F_0)	0h
128h	4	GPI Interrupt Enable (GPI_IE_GPP_H_0)	0h
130h	4	GPI Interrupt Enable (GPI_IE_vGPIO_1)	0h
140h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_D_0)	0h
144h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_0)	0h
148h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_H_0)	0h
150h	4	GPI General Purpose Events Status (GPI_GPE_STS_vGPIO_1)	0h
160h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_D_0)	0h
7c0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_3)	44000X00h. Refer to register for X value
7c4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_3)	See Register
7d0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_4)	44000X00h. Refer to register for X value
7d4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_4)	See Register

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7e0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_5)	44000X00h. Refer to register for X value
7e4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_5)	See Register
7f0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_6)	44000X00h. Refer to register for X value
7f4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_6)	See Register
800h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_7)	44000X00h. Refer to register for X value
804h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_7)	See Register
810h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_8)	44000X00h. Refer to register for X value
814h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_8)	See Register
820h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_9)	44000X00h. Refer to register for X value
824h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_9)	See Register
830h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_10)	44000X00h. Refer to register for X value
834h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_10)	See Register
840h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_11)	44000X00h. Refer to register for X value
844h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_11)	See Register
850h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_12)	44000X00h. Refer to register for X value
854h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_12)	See Register

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
860h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_13)	44000X00h. Refer to register for X value
864h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_13)	See Register
870h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_14)	44000X00h. Refer to register for X value
874h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_14)	See Register
880h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_15)	44000X00h. Refer to register for X value
884h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_15)	See Register
890h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_16)	44000X00h. Refer to register for X value
894h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_16)	See Register
8a0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_17)	44000X00h. Refer to register for X value
8a4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_17)	See Register
8b0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_18)	44000X00h. Refer to register for X value
8b4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_18)	See Register
8c0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_19)	44000X00h. Refer to register for X value
8c4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_19)	See Register
8d0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_20)	44000X00h. Refer to register for X value

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8d4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_20)	See Register
8e0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_21)	44000X00h. Refer to register for X value
8e4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_21)	See Register
8f0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_22)	44000X00h. Refer to register for X value
8f4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_22)	See Register
900h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_23)	44000X00h. Refer to register for X value
904h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_23)	See Register
164h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_0)	0h
168h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_H_0)	0h
170h	4	GPI General Purpose Events Enable (GPI_GPE_EN_vGPIO_1)	0h
940h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_3)	44000X00h. Refer to register for X value
944h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_3)	See Register
950h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_4)	44000X00h. Refer to register for X value
954h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_4)	See Register
960h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_5)	44000X00h. Refer to register for X value

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
964h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_5)	See Register
970h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_6)	44000X00h. Refer to register for X value
974h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_6)	See Register
980h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_7)	44000X00h. Refer to register for X value
984h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_7)	See Register
990h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_8)	44000X00h. Refer to register for X value
994h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_8)	See Register
9a0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_9)	44000X00h. Refer to register for X value
9a4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_9)	See Register
9b0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_10)	44000X00h. Refer to register for X value
9b4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_10)	See Register
9c0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_11)	44000X00h. Refer to register for X value
9c4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_11)	See Register
9d0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_12)	44000X00h. Refer to register for X value
9d4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_12)	See Register

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
9e0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_13)	44000X00h. Refer to register for X value
9e4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_13)	See Register
9f0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_14)	44000X00h. Refer to register for X value
9f4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_14)	See Register
a00h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_15)	44000X00h. Refer to register for X value
a04h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_15)	See Register
a10h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_16)	44000X00h. Refer to register for X value
a14h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_16)	See Register
a20h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_17)	44000X00h. Refer to register for X value
a24h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_17)	See Register
a30h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_18)	44000X00h. Refer to register for X value
a34h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_18)	See Register
a40h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_19)	44000X00h. Refer to register for X value
a44h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_19)	See Register
a50h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_20)	44000X00h. Refer to register for X value

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
a54h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_20)	See Register
a60h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_21)	44000X00h. Refer to register for X value
a64h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_21)	See Register
a70h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_22)	44000X00h. Refer to register for X value
a74h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_22)	See Register
a80h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_23)	44000X00h. Refer to register for X value
a84h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_23)	See Register
a90h	4	Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_0)	40000001h
ac0h	4	Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_3)	See Register
c70h	4	Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_30)	See Register
c80h	4	Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_31)	See Register
c90h	4	Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_32)	See Register
ca0h	4	Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_33)	See Register
cb0h	4	Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_34)	See Register
cc0h	4	Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_35)	See Register
cd0h	4	Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_36)	See Register

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
ce0h	4	Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_37)	See Register
d00h	4	Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_39)	40000400h
910h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_0)	44000X00h. Refer to register for X value
914h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_0)	See Register
920h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_1)	44000X00h. Refer to register for X value
924h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_1)	See Register
930h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_2)	44000X00h. Refer to register for X value
934h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_2)	See Register

SMI Status (GPI_SMI_STS_GPP_D_0) – Offset 180

Register bits in this register are implemented for GPP_D signals that have SMI capability only. Other bits are reserved and RO.

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_4)** Same description as bit 0.
3	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_3)** Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
2	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_2)** Same description as bit 0.
1	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_1)** Same description as bit 0.
0	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_0)** This bit is set to 1 by hardware when a level event (See RxEdCfg,RxInv) is detected, and all the following conditions are true: - The corresponding pad is used in GPIO input mode - The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if theGPI_SMI_ STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of 1 will clear the bit while writing a value of 0 has noeffect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN does not prevent the setting of GPI_SMI_STS. Defaults for these bits are dependent on the state of the GPI pads.

SMI Enable (GPI_SMI_EN_GPP_D_0) – Offset 1a0

Register bits in this register are implemented for GPP_D signals that have SMI capability only. Other bits are reserved and RO.

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4	0b	RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_4)** Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
3	0b	RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_3)** Same description as bit 0.
2	0b	RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_2)** Same description as bit 0.
1	0b	RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_1)** Same description as bit 0.
0	0b	RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_0)** This bit is used to enable/disable the generation of SMI when thecorresponding GPI_SMI_STS bit is set. The pad must also be routed forSMI functionality in order for SMI to be generated, i.e. the correspondingGPIROUTSMI must be set to 1. 0 = disable SMI generation 1 = enable SMI generation Note:Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is 1, bit0 of this bit is locked down to read-only.

NMI Status (GPI_NMI_STS_GPP_D_0) – Offset 1c0

Register bits in this register are implemented for GPP_D signals that have NMI capability only. Other bits are reserved and RO.

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_4)** Same description as bit 0.
3	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_3)** Same description as bit 0.
2	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_2)** Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
1	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_1)** Same description as bit 0.
0	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_0)** This bit is set to 1 by hardware when an edge event is detected (SeeRxEdCfg, RxInv) on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode (PMode) - The corresponding GPIONMIRout is set to 1, i.e. programmed toroute as NMI - The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). - The corresponding GPI_NMI_EN is set Writing a value of 1 will clear the bit while writing a value of 0 has noeffect. 0 = There is no NMI event 1 = There is an NMI event

NMI Enable (GPI_NMI_EN_GPP_D_0) – Offset 1e0

Register bits in this register are implemented for GPP_D signals that have NMI capability only. Other bits are reserved and RO.

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_4)** Same description as bit 0.
3	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_3)** Same description as bit 0.
2	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_2)** Same description as bit 0.
1	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_1)** Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_0)** This bit is used to enable/disable the generation of NMI when thecorresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configurationregister PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 ofthis bit is locked down to read-only.

PWM Control (PWMC) – Offset 204

Bit Range	Default	Access	Field Name and Description
31	0b	RW	**Enable (EN)** 0 = Disable PWM Output 1 = Enable PWM Output
30	0b	RW/1S/V	**Software Update (SWUP)** Indication that there is an update to PWM settings pending. SW sets this bit to 1 when updating the PWM_base_unit or PWM_on_time_divisor fields. The PWM module will apply the new settings at the end of the current cycle and reset this bit. 0 = No updates pending 1 = Update pending
29:8	000000h	RW	**Base Unit (BASEUNIT)** Base unit register. Unsigned 8 integer bits, 14 fraction bits. Used to determine PWM output frequency. The PWM base frequency for SPT is 32.768 KHz.
7:0	00h	RW	**On Time Divisor (ONTIMEDIV)** PWM duty cycle = PWM_on-time_divisor/256.

GPIO Serial Blink Enable (GP_SER_BLINK) – Offset 20c

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4:0	00h	RW	**GP SER BLINK (GP_SER_BLINK)** The setting of this bit has no effect if the corresponding GPIO is programmed as an input, if the corresponding GPIO has the PWM enabled, or if Serial Blink capability does not exist . This bit should be set to a 1 before output buffer is enabled. When set to a '0', the corresponding GPIO will function normally. This bit should be set to a 1 while the corresponding PMode bit is set to 0h (GPIO Mode). Setting the PMode bit to other value (non-GPIO Mode) after the GP_SER_ BLINK bit ensures PCH will not drive a 1 on the pin as an output. When this corresponding bit is set to a 1 and the pin is configured to output mode, the serial blink capability is enabled and the programmed message is serialized out through an open-drain buffer configuration. The value of the corresponding GPIOTxState bit remains unchanged and does not impact the serial blink capability in any way. Writes to this register have no effect when the corresponding pin is configured in native mode and the read value returned is undefined. Bit0 = GPP_D0 Bit1 = GPP_D1 Bit2 = GPP_D2 Bit3 = GPP_D3. Bit4 = GPP_D4

Family Base Address (FAMBAR) – Offset 8

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
15:0	300h	RO	**Family Base Address (FAMBAR)** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

Pad Base Address (PADBAR) – Offset c

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	600h	RO	**Pad Base Address (PADBAR)** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

Miscellaneous Configuration (MISCCFG) – Offset 10

Bit Range	Default	Access	Field Name and Description
30:20	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
19:16	0100b	RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2)** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 1h = GPP_B[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 2h = GPP_G[7:0] mapped to GPE[71:64]; GPE[95:72] not used. 3h = Reserved. 4h = GPP_C[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 5h = GPP_D[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 6h = GPP_F[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 7h = GPP_H[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 8h = vGPIO39 (vSD_CD#) mapped to GPE bit 70. 9h = Reserved Ah = GPD[11:0] mapped to GPE[75:64]; GPE[95:76] not used Bh - Ch = Reserved Dh = GPP_E[23:0] mapped to GPE[87:64]; GPE[95:88] not used. Eh - Fh = Reserved

Bit Range	Default	Access	Field Name and Description
15:12	0011b	RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1)** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 1h = GPP_B[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 2h = GPP_G[7:0] mapped to GPE[39:32]; GPE[63:40] not used. 3h = Reserved. 4h = GPP_C[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 5h = GPP_D[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 6h = GPP_F[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 7h = GPP_H[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 8h = vGPIO39 (vSD_CD#) mapped to GPE bit 38. 9h = Reserved Ah = GPD[11:0] mapped to GPE[43:32]; GPE[63:44] not used Bh - Ch = Reserved Dh = GPP_E[23:0] mapped to GPE[55:32]; GPE[63:56] not used. Dh = GPP_E[23:0] mapped to GPE[55:32]; GPE[63:56] not used. Eh - Fh = Reserved

Bit Range	Default	Access	Field Name and Description
11:8	0010b	RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0)** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 1h = GPP_B[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 2h = GPP_G[7:0] mapped to GPE[7:0]; GPE[31:8] not used. 3h = Reserved. 4h = GPP_C[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 5h = GPP_D[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 6h = GPP_F[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 7h = GPP_H[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 8h = vGPIO_39 (vSD_CD#) mapped to GPE bit 7.9h = Reserved Ah = GPD[11:0] mapped to GPE[11:0]; GPE[31:12] not used Bh - Ch = Reserved Dh = GPP_E[23:0] mapped to GPE[23:0]; GPE[31:24] not used Eh - Fh = Reserved
7:2	-	-	**Reserved**
1	0b	RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN)** Specifies whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating.

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN)** Specifies whether the GPIO Community should perform local clock gating. 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating

Pad Ownership (PAD_OWN_GPP_D_0) – Offset 20

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29:28	00b	RW	**Pad Ownership (PAD_OWN_GPPC_D_7)** Same description as bits [1:0], except that the bit field applies to GPP_D7.
27:26	-	-	**Reserved**
25:24	00b	RW	**Pad Ownership (PAD_OWN_GPPC_D_6)** Same description as bits [1:0], except that the bit field applies to GPP_D6.
23:22	-	-	**Reserved**
21:20	00b	RW	**Pad Ownership (PAD_OWN_GPPC_D_5)** Same description as bits [1:0], except that the bit field applies to GPP_D5.
19:18	-	-	**Reserved**
17:16	00b	RW	**Pad Ownership (PAD_OWN_GPPC_D_4)** Same description as bits [1:0], except that the bit field applies to GPP_D4.
15:14	-	-	**Reserved**
13:12	00b	RW	**Pad Ownership (PAD_OWN_GPPC_D_3)** Same description as bits [1:0], except that the bit field applies to GPP_D3.

Bit Range	Default	Access	Field Name and Description
11:10	-	-	**Reserved**
9:8	00b	RW	**Pad Ownership (PAD_OWN_GPPC_D_2)** Same description as bits [1:0], except that the bit field applies to GPP_D2.
7:6	-	-	**Reserved**
5:4	00b	RW	**Pad Ownership (PAD_OWN_GPPC_D_1)** Same description as bits [1:0], except that the bit field applies to GPP_D1.
3:2	-	-	**Reserved**
1:0	00b	RW	**Pad Ownership (PAD_OWN_GPPC_D_0)** 00 = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIODriver) has ownership of the pad. In Host GPIO Driver Mode (refer toHOSTSW_OWN), GPIO input event update is limited to GPI_STS update only.Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STSand/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership 01 = ME GPIO Mode. ME has ownership of the pad. 10 = ISH GPIO Mode. ME has ownership of the pad 11 = Reserved

Pad Ownership (PAD_OWN_GPP_D_1) – Offset 24

Same description as PAD_OWN_GPP_D_0, except that this register is for GPP_D[15:8].

Pad Ownership (PAD_OWN_GPP_D_2) – Offset 28

Same description as PAD_OWN_GPP_D_0, except that this register is for GPP_D[23:16].

Pad Ownership (PAD_OWN_GPP_F_0) – Offset 30

Same description as PAD_OWN_GPP_D_0, except that this register is for GPP_F[7:0].

Pad Ownership (PAD_OWN_GPP_F_1) – Offset 34

Same description as PAD_OWN_GPP_D_0, except that this register is for GPP_F[15:8].

Pad Ownership (PAD_OWN_GPP_F_2) – Offset 38

Same description as PAD_OWN_GPP_D_0, except that this register is for GPP_F[23:16].

Pad Ownership (PAD_OWN_GPP_H_0) – Offset 3c

Same description as PAD_OWN_GPP_D_0, except that this register is for GPP_H[7:0].

Pad Ownership (PAD_OWN_GPP_H_1) – Offset 40

Same description as PAD_OWN_GPP_D_0, except that this register is for GPP_H[15:8].

Pad Ownership (PAD_OWN_GPP_H_2) – Offset 44

Same description as PAD_OWN_GPP_D_0, except that this register is for GPP_H[23:16].

Pad Configuration Lock (PADCFGLOCK_GPP_D_0) – Offset 80

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_23)** Applied to GPP_D23. Same description as PADCFGLOCK_GPP_D_0.
22	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_22)** Applied to GPP_D22. Same description as PADCFGLOCK_GPP_D_0.
21	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_21)** Applied to GPP_D21. Same description as PADCFGLOCK_GPP_D_0.
20	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_20)** Applied to GPP_D20. Same description as PADCFGLOCK_GPP_D_0.
19	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_19)** Applied to GPP_D19. Same description as PADCFGLOCK_GPP_D_0.

Bit Range	Default	Access	Field Name and Description
18	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_18)** Applied to GPP_D18. Same description as PADCFGLOCK_GPP_D_0.
17	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_17)** Applied to GPP_D17. Same description as PADCFGLOCK_GPP_D_0.
16	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_16)** Applied to GPP_D16. Same description as PADCFGLOCK_GPP_D_0.
15	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_15)** Applied to GPP_D15. Same description as PADCFGLOCK_GPP_D_0.
14	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_14)** Applied to GPP_D14. Same description as PADCFGLOCK_GPP_D_0.
13	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_13)** Applied to GPP_D13. Same description as PADCFGLOCK_GPP_D_0.
12	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_12)** Applied to GPP_D12. Same description as PADCFGLOCK_GPP_D_0.
11	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_11)** Applied to GPP_D11. Same description as PADCFGLOCK_GPP_D_0.
10	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_10)** Applied to GPP_D10. Same description as PADCFGLOCK_GPP_D_0.
9	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_9)** Applied to GPP_D9. Same description as PADCFGLOCK_GPP_D_0.
8	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_8)** Applied to GPP_D8. Same description as PADCFGLOCK_GPP_D_0.
7	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_7)** Applied to GPP_D7. Same description as PADCFGLOCK_GPP_D_0.
6	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_6)** Applied to GPP_D6. Same description as PADCFGLOCK_GPP_D_0.
5	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_5)** Applied to GPP_D5. Same description as PADCFGLOCK_GPP_D_0.

Bit Range	Default	Access	Field Name and Description
4	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_4)** Applied to GPP_D4. Same description as PADCFGLOCK_GPP_D_0.
3	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_3)** Applied to GPP_D3. Same description as PADCFGLOCK_GPP_D_0.
2	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_2)** Applied to GPP_D2. Same description as PADCFGLOCK_GPP_D_0.
1	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_1)** Applied to GPP_D1. Same description as PADCFGLOCK_GPP_D_0.
0	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_D_0)** Pad Configuration Lock locks specific register fields in the GPP specific registers from being configured. The registers affected become Read-Only and software writes to these registers have no effect. 0 = Unlock 1 = Lock the following register fields as read-only (RO): - Pad Configuration registers (exclude GPIOTXState) - GPI_NMI_EN Register (if implemented) - GPI_SMI_EN Register (if implemented) - GPI_GPE_EN Register (if implemented) When PadCfgLock is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_D_0) – Offset 84

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_23)** Applied to GPP_D23. Same description as PADCFGLOCKTX_GPP_D_0.

Bit Range	Default	Access	Field Name and Description
22	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_22)** Applied to GPP_D22. Same description as PADCFGLOCKTX_GPP_D_0.
21	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_21)** Applied to GPP_D21. Same description as PADCFGLOCKTX_GPP_D_0.
20	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_20)** Applied to GPP_D20. Same description as PADCFGLOCKTX_GPP_D_0.
19	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_19)** Applied to GPP_D19. Same description as PADCFGLOCKTX_GPP_D_0.
18	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_18)** Applied to GPP_D18. Same description as PADCFGLOCKTX_GPP_D_0.
17	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_17)** Applied to GPP_D17. Same description as PADCFGLOCKTX_GPP_D_0.
16	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_16)** Applied to GPP_D16. Same description as PADCFGLOCKTX_GPP_D_0.
15	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_15)** Applied to GPP_D15. Same description as PADCFGLOCKTX_GPP_D_0.
14	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_14)** Applied to GPP_D14. Same description as PADCFGLOCKTX_GPP_D_0.
13	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_13)** Applied to GPP_D13. Same description as PADCFGLOCKTX_GPP_D_0.
12	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_12)** Applied to GPP_D12. Same description as PADCFGLOCKTX_GPP_D_0.
11	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_11)** Applied to GPP_D11. Same description as PADCFGLOCKTX_GPP_D_0.
10	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_10)** Applied to GPP_D10. Same description as PADCFGLOCKTX_GPP_D_0.
9	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_9)** Applied to GPP_D9. Same description as PADCFGLOCKTX_GPP_D_0.

Bit Range	Default	Access	Field Name and Description
8	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_8)** Applied to GPP_D8. Same description as PADCFGLOCKTX_GPP_D_0.
7	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_7)** Applied to GPP_D7. Same description as PADCFGLOCKTX_GPP_D_0.
6	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_6)** Applied to GPP_D6. Same description as PADCFGLOCKTX_GPP_D_0.
5	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_5)** Applied to GPP_D5. Same description as PADCFGLOCKTX_GPP_D_0.
4	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_4)** Applied to GPP_D4. Same description as PADCFGLOCKTX_GPP_D_0.
3	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_3)** Applied to GPP_D3. Same description as PADCFGLOCKTX_GPP_D_0.
2	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_2)** Applied to GPP_D2. Same description as PADCFGLOCKTX_GPP_D_0.
1	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_1)** Applied to GPP_D1. Same description as PADCFGLOCKTX_GPP_D_0.
0	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_D_0)** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) When PadCfgLockTx is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

GPIO Serial Blink Command/Status (GP_SER_CMDSTS) – Offset 210

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:22	00b	RW	**Data Length Select (DLS)** This read/write field determines the number of bytes to serialize on GPIO 00: Serialize bits 7:0 of GP_GB_DATA (1 byte) 01: Serialize bits 15:0 of GP_GB_DATA (2 bytes) 10: Undefined - Software must not write this value 11: Serialize bits 31:0 of GP_GB_DATA (4 bytes) Software should not modify the value in this register unless the Busy bit is clear
21:16	08h	RW	**Data Rate Select (DRS)** This read/write field selects the number of 166.64ns (4 clock periods GPIO clock - if GPIO clock is 24MHz) time intervals to count between Manchester data transitions. The default of 8h results in a 1333.33 ns minimum time between transitions. A value of 0h in this register produces undefined behavior. Software should not modify the value in this register unless the Busy bit is clear.
15:9	-	-	**Reserved**
8	0b	RO/V	**Busy (BUSY)** This read-only status bit is the hardware indication that a serialization is in progress. Hardware sets this bit to 1 based on the Go bit being set. Hardware clears this bit when the Go bit is cleared by the hardware.
7:1	-	-	**Reserved**
0	0b	RW	**Go (GO)** This bit is set to 1 by software to start the serialization process. Hardware clears the bit after the serialized data is sent. Writes of 0 to this register have no effect. Software should not write this bit to 1 unless the Busy status bit is cleared.

GPIO Serial Blink Data (GP_SER_DATA) – Offset 214

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**GP Serial Blink Data (GP_GB_DATA)** This read-write register contains the data serialized out. The number of bits shifted out is selected through the DLS field in the GP_GB_CMDSTS register. This register should not be modified by software when the Busy bit is set.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_0) – Offset 600

This register applies to GPP_D0.

Bit Range	Default	Access	Field Name and Description
31:30	01b	RW	**Pad Reset Config (PADRSTCFG)** This register controls which reset is used to reset GPIO pad register fields in PAD_CFG_DW0 and PAD_CFG_DW1 registers. This register can be used for Sx isolation of the associated signal if needed. 00 = RSMRST# 01 = Host deep reset. This reset occurs when any of the following occur: Host reset (with or without power cycle) is initiated, Global reset is initiated, or Deep Sx entry. This reset does NOT occur as part of S3/S4/S5 entry. 10 = PLTRST# 11 = Reserved
29	0b	RW	**RX Pad State Select (RXPADSTSEL)** Determines from which node the RX pad state for native function should be taken from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from RX buffer 1 = Internal RX pad state (subject to RXINV and PreGfRXSel settings)

Bit Range	Default	Access	Field Name and Description
28	0b	RW	**RX Raw Override to '1' (RXRAW1)** This bit determines if the selected pad state is being overridden to '1'. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	-	-	**Reserved**
26:25	10b	RW	**RX Level/Edge Configuration (RXEVCFG)** Determines if the internal RX pad state (synchronized, filtered vs non-filtered version as determined by PreGfRXSel, and is further subject to RXInv) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller . 0h = Level 1h = Edge (RxInv=0 for rising edge; 1 for falling edge) 2h = Disable 3h = Either rising edge or falling edge
24	0b	RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL)** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV

Bit Range	Default	Access	Field Name and Description
23	0b	RW	**RX Invert (RXINV)** This bit determines if the selected pad state should go through the polarity inversion stage. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	00b	RW	**RX/TX Enable Config (RXTXENCFG)** This controls the RX and TX buffer enablement for the function selected by Pad Mode. This field is not applicable in GPIO mode (PMode = 0. 0h = Function defined in Pad Mode controls TX and RX enablement 1h = Function controls TX enablement and RX is disabled with 0 being driven internally 2h = Function controls TX enablement and RX is disabled with 1 being driven internally 3h = Function controls TX enablement and RX is always enabled
20	0b	RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC)** Determines if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).

Bit Range	Default	Access	Field Name and Description
19	0b	RW	**GPIO Input Route SCI (GPIROUTSCI)** Determines if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI. 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s).
18	0b	RW	**GPIO Input Route SMI (GPIROUTSMI)** Determines if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s). This bit only applies to a GPIO that has SMI capability. Otherwise, the bit is RO.
17	0b	RW	**GPIO Input Route NMI (GPIROUTNMI)** Determines if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit. This bit only applies to a GPIO that has NMI capability. Otherwise, the bit is RO.

Bit Range	Default	Access	Field Name and Description
16:12	-	-	**Reserved**
11:10	See Description	RW	**Pad Mode (PMODE)** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad. 1h = native function 1, if applicable, controls the Pad 2h = native function 2, if applicable, controls the Pad. 3h = native function 3, if applicable, controls the Pad Dedicated (unmuxed) GPIO shall report RO of all 0's in this register field If GPIO vs. native mode is configured via soft strap, this bit has no effect. Default value is determined by the default functionality of the pad.
9	1b	RW	**GPIO RX Disable (GPIORXDIS)** 0 = Enable the input buffer (active low enable) of the pad. 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0'.
8	1b	RW	**GPIO TX Disable (GPIOTXDIS)** 0 = Enable the output buffer (active low enable) of the pad. 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	-	-	**Reserved**
1		RO/V	**GPIO RX State (GPIORXSTATE)** This is the current internal RX pad state after Glitch Filter logic stage and hardware debouncer (if any) and is not affected by PMode and RXINV settings.
0	0b	RW	**GPIO TX State (GPIOTXSTATE)** 0 = Drive a level '0' to the TX output pad. 1 = Drive a level '1' to the TX output pad.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_0) – Offset 604

This register applies to GPP_D0.

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13:10	See Description	RW	**Termination (TERM)** The Pad Termination state defines the different weak internal pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. Others: Reserved NOTES: 1. The 20K internal pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily.
9:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	60h	RO	**Interrupt Select (INTSEL)** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 .... Up to the max IOxAPIC IRQ supported.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_1) – Offset 610

This register applies to GPP_D1 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_1) – Offset 614

This register applies to GPP_D1 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 61h

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_2) – Offset 620

This register applies to GPP_D2 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration Lock (PADCFGLOCK_GPP_F_0) – Offset 88

Same description as PADCFGLOCK_GPP_D_0 register, except this register applies to GPP_F[23:0].

Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_F_0) – Offset 8c

Same description as PADCFGLOCKTX_GPP_D_0 register, except this register applies to GPP_F[23:0].

Pad Configuration Lock (PADCFGLOCK_GPP_H_0) – Offset 90

Same description as PADCFGLOCK_GPP_D_0 register, except this register applies to GPP_H[23:0].

Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_H_0) – Offset 94

Same description as PADCFGLOCKTX_GPP_D_0 register, except this register applies to GPP_H[23:0].

Host Software Pad Ownership (HOSTSW_OWN_GPP_D_0) – Offset b0

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_23)** Applied to GPP_D23. Same description as bit 0.
22	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_22)** Applied to GPP_D22. Same description as bit 0.
21	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_21)** Applied to GPP_D21. Same description as bit 0.
20	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_20)** Applied to GPP_D20. Same description as bit 0.
19	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_19)** Applied to GPP_D19. Same description as bit 0.
18	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_18)** Applied to GPP_D18. Same description as bit 0.
17	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_17)** Applied to GPP_D17. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
16	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_16)** Applied to GPP_D16. Same description as bit 0.
15	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_15)** Applied to GPP_D15. Same description as bit 0.
14	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_14)** Applied to GPP_D14. Same description as bit 0.
13	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_13)** Applied to GPP_D13. Same description as bit 0.
12	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_12)** Applied to GPP_D12. Same description as bit 0.
11	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_11)** Applied to GPP_D11. Same description as bit 0.
10	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_10)** Applied to GPP_D10. Same description as bit 0.
9	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_9)** Applied to GPP_D9. Same description as bit 0.
8	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_8)** Applied to GPP_D8. Same description as bit 0.
7	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_7)** Applied to GPP_D7. Same description as bit 0.
6	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_6)** Applied to GPP_D6. Same description as bit 0.
5	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_5)** Applied to GPP_D5. Same description as bit 0.
4	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_4)** Applied to GPP_D4. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
3	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_3)** Applied to GPP_D3. Same description as bit 0.
2	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_2)** Applied to GPP_D2. Same description as bit 0.
1	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_1)** Applied to GPP_D1. Same description as bit 0.
0	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_D_0)** This register determines the appropriate host status bit update when a pad is under host ownership. 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS,GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited toGPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updatesare masked.

Host Software Pad Ownership (HOSTSW_OWN_GPP_F_0) – Offset b4

Same description as HOSTSW_OWN_GPP_D_0 register, except that this register applies to GPP_F[23:0].

Host Software Pad Ownership (HOSTSW_OWN_GPP_H_0) – Offset b8

Same description as HOSTSW_OWN_GPP_D_0 register, except that this register applies to GPP_H[23:0].

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_2) – Offset 624

This register applies to GPP_D2 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 62h

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_3) – Offset 630

This register applies to GPP_D3 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_3) – Offset 634

This register applies to GPP_D3 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 63h

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_4) – Offset 640

This register applies to GPP_D4 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_4) – Offset 644

This register applies to GPP_D4 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 64h

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_5) – Offset 650

This register applies to GPP_D5 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_5) – Offset 654

This register applies to GPP_D5 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 65h

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_6) – Offset 660

This register applies to GPP_D6 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_6) – Offset 664

This register applies to GPP_D6 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 66h

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_7) – Offset 670

This register applies to GPP_D7 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_7) – Offset 674

This register applies to GPP_D7 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 67h

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_8) – Offset 680

This register applies to GPP_D8 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_8) – Offset 684

This register applies to GPP_D8 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 68h

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_9) – Offset 690

This register applies to GPP_D9 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_9) – Offset 694

This register applies to GPP_D9 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 69h

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_10) – Offset 6a0

This register applies to GPP_D10 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_10) – Offset 6a4

This register applies to GPP_D10 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 6Ah

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_11) – Offset 6b0

This register applies to GPP_D11 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_11) – Offset 6b4

This register applies to GPP_D11 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 6Bh

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_12) – Offset 6c0

This register applies to GPP_D12 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_12) – Offset 6c4

This register applies to GPP_D12 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 6Ch

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_13) – Offset 6d0

This register applies to GPP_D13 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_13) – Offset 6d4

This register applies to GPP_D13 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 6Dh

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_14) – Offset 6e0

This register applies to GPP_D14 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_14) – Offset 6e4

This register applies to GPP_D14 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 6Eh

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_15) – Offset 6f0

This register applies to GPP_D15 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_15) – Offset 6f4

This register applies to GPP_D15 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 6Fh

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_16) – Offset 700

This register applies to GPP_D16 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_16) – Offset 704

This register applies to GPP_D16 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 70h

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_17) – Offset 710

This register applies to GPP_D17 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_17) – Offset 714

This register applies to GPP_D17 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 71h

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_18) – Offset 720

This register applies to GPP_D18 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_18) – Offset 724

This register applies to GPP_D18 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 72h

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_19) – Offset 730

This register applies to GPP_D19 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_19) – Offset 734

This register applies to GPP_D19 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 73h

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_20) – Offset 740

This register applies to GPP_D20 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_20) – Offset 744

This register applies to GPP_D20 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 74h

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_21) – Offset 750

This register applies to GPP_D21 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_21) – Offset 754

This register applies to GPP_D21 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 75h

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_22) – Offset 760

This register applies to GPP_D22 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_22) – Offset 764

This register applies to GPP_D22 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 76h

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_23) – Offset 770

This register applies to GPP_D23 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_23) – Offset 774

This register applies to GPP_D23 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 77h

TERM bit field default: 0000b

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_0) – Offset 790

This register applies to GPP_F0 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_0) – Offset 794

This register applies to GPP_F0 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 30h

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_1) – Offset 7a0

This register applies to GPP_F1 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_1) – Offset 7a4

This register applies to GPP_F1 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 31h

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_2) – Offset 7b0

This register applies to GPP_F2 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_2) – Offset 7b4

This register applies to GPP_F2 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 32h

Host Software Pad Ownership (HOSTSW_OWN_vGPIO_1) – Offset c0

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7	0b	RO	**HostSW_Own (HOSTSW_OWN_vGPIO_39)** This register determines the appropriate host status bit update when a pad is under host ownership (refer to PAD_OWN). 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked.
6:0	-	-	**Reserved**

GPI Interrupt Status (GPI_IS_GPP_D_0) – Offset 100

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_23)** Applied to GPP_D23. Same description as bit 0.
22	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_22)** Applied to GPP_D22. Same description as bit 0.
21	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_21)** Applied to GPP_D21. Same description as bit 0.
20	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_20)** Applied to GPP_D20. Same description as bit 0.
19	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_19)** Applied to GPP_D19. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
18	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_18)** Applied to GPP_D18. Same description as bit 0.
17	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_17)** Applied to GPP_D17. Same description as bit 0.
16	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_16)** Applied to GPP_D16. Same description as bit 0.
15	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_15)** Applied to GPP_D15. Same description as bit 0.
14	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_14)** Applied to GPP_D14. Same description as bit 0.
13	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_13)** Applied to GPP_D13. Same description as bit 0.
12	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_12)** Applied to GPP_D12. Same description as bit 0.
11	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_11)** Applied to GPP_D11. Same description as bit 0.
10	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_10)** Applied to GPP_D10. Same description as bit 0.
9	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_9)** Applied to GPP_D9. Same description as bit 0.
8	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_8)** Applied to GPP_D8. Same description as bit 0.
7	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_7)** Applied to GPP_D7. Same description as bit 0.
6	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_6)** Applied to GPP_D6. Same description as bit 0.
5	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_5)** Applied to GPP_D5. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
4	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_4)** Applied to GPP_D4. Same description as bit 0.
3	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_3)** Applied to GPP_D3. Same description as bit 0.
2	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_2)** Applied to GPP_D2. Same description as bit 0.
1	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_1)** Applied to GPP_D1. Same description as bit 0.
0	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_D_0)** GPI Interrupt Status (GPI_INT_STS) This bit is set to '1' by hardware when either an edge or a level event isdetected (See RxEdCfg RxInv) on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode - HOSTSW_OWN = 1 (i.e. Host GPIO Driver Mode). Writing a value of 1 will clear the bit while writing a value of 0 has noeffect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x].

GPI Interrupt Status (GPI_IS_GPP_F_0) – Offset 104

Same description as GPI_IE_GPP_D_0 register, except that this register is for GPP_F[23:0].

GPI Interrupt Status (GPI_IS_GPP_H_0) – Offset 108

Same description as GPI_IE_GPP_D_0 register, except that this register is for GPP_H[23:0].

GPI Interrupt Status (GPI_IS_vGPIO_1) – Offset 110

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7	0b	RO	**GPI Interrupt Status (GPI_INT_STS_vGPIO_39)** This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: The corresponding pad is used in GPIO input mode The corresponding PAD_OWN[1:0] is '00' and HOSTSW_OWN ='1' (i.e. Host GPIO Driver Mode). Writing a value of '1' will clear the bit while writing a value of '0' has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN does not prevent the setting of GPI_INT_STS.
6:0	-	-	**Reserved**

GPI Interrupt Enable (GPI_IE_GPP_D_0) – Offset 120

Bit Range	Default	Access	Field Name and Description
30:23	-	-	**Reserved**
22	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_22)** Applied to GPP_D22. Same description as bit 0.
21	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_21)** Applied to GPP_D21. Same description as bit 0.
20	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_20)** Applied to GPP_D20. Same description as bit 0.
19	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_19)** Applied to GPP_D19. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
18	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_18)** Applied to GPP_D18. Same description as bit 0.
17	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_17)** Applied to GPP_D17. Same description as bit 0.
16	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_16)** Applied to GPP_D16. Same description as bit 0.
15	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_15)** Applied to GPP_D15. Same description as bit 0.
14	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_14)** Applied to GPP_D14. Same description as bit 0.
13	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_13)** Applied to GPP_D13. Same description as bit 0.
12	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_12)** Applied to GPP_D12. Same description as bit 0.
11	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_11)** Applied to GPP_D11. Same description as bit 0.
10	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_10)** Applied to GPP_D10. Same description as bit 0.
9	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_9)** Applied to GPP_D9. Same description as bit 0.
8	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_8)** Applied to GPP_D8. Same description as bit 0.
7	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_7)** Applied to GPP_D7. Same description as bit 0.
6	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_6)** Applied to GPP_D6. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
5	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_5)** Applied to GPP_D5. Same description as bit 0.
4	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_4)** Applied to GPP_D4. Same description as bit 0.
3	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_3)** Applied to GPP_D3. Same description as bit 0.
2	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_2)** Applied to GPP_D2. Same description as bit 0.
1	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_1)** Applied to GPP_D1. Same description as bit 0.
0	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_D_0)** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation

GPI Interrupt Enable (GPI_IE_GPP_F_0) – Offset 124

Same description as GPI_IE_GPP_D_0 register, except that this register is for GPP_F[23:0].

GPI Interrupt Enable (GPI_IE_GPP_H_0) – Offset 128

Same description as GPI_IE_GPP_D_0 register, except that this register is for GPP_H[23:0].

GPI Interrupt Enable (GPI_IE_vGPIO_1) – Offset 130

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7	0b	RO	**GPI Interrupt Enable (GPI_INT_EN_vGPIO_39)** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation Refer to GPI_IRQ_ROUTE for host GPIO Driver Mode interrupt routing.
6:0	-	-	**Reserved**

GPI General Purpose Events Status (GPI_GPE_STS_GPP_D_0) – Offset 140

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_23)** Applied to GPP_D23. Same description as bit 0.
22	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_22)** Applied to GPP_D22. Same description as bit 0.
21	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_21)** Applied to GPP_D21. Same description as bit 0.
20	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_20)** Applied to GPP_D20. Same description as bit 0.
19	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_19)** Applied to GPP_D19. Same description as bit 0.
18	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_18)** Applied to GPP_D18. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
17	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_17)** Applied to GPP_D17. Same description as bit 0.
16	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_16)** Applied to GPP_D16. Same description as bit 0.
15	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_15)** Applied to GPP_D15. Same description as bit 0.
14	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_14)** Applied to GPP_D14. Same description as bit 0.
13	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_13)** Applied to GPP_D13. Same description as bit 0.
12	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_12)** Applied to GPP_D12. Same description as bit 0.
11	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_11)** Applied to GPP_D11. Same description as bit 0.
10	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_10)** Applied to GPP_D10. Same description as bit 0.
9	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_9)** Applied to GPP_D9. Same description as bit 0.
8	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_8)** Applied to GPP_D8. Same description as bit 0.
7	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_7)** Applied to GPP_D7. Same description as bit 0.
6	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_6)** Applied to GPP_D6. Same description as bit 0.
5	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_5)** Applied to GPP_D5. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
4	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_4)** Applied to GPP_D4. Same description as bit 0.
3	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_3)** Applied to GPP_D3. Same description as bit 0.
2	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_2)** Applied to GPP_D2. Same description as bit 0.
1	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_1)** Applied to GPP_D1. Same description as bit 0.
0	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_D_0)** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high(or low if the corresponding RXINV bit is set). If the correspondingenable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: - If the system is in an S3-S5 state, the event will also wake the system. - If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for thecorresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS.

GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_0) – Offset 144

Same description as PI_GPE_STS_GPP_D_0 register, except that this is for GPP_F[23:0].

GPI General Purpose Events Status (GPI_GPE_STS_GPP_H_0) – Offset 148

Same description as PI_GPE_STS_GPP_D_0 register, except that this is for GPP_H[23:0].

GPI General Purpose Events Status (GPI_GPE_STS_vGPIO_1) – Offset 150

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7	0b	RO	**GPI General Purpose Events Status (GPI_GPE_STS_vGPIO_39)** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: If the system is in an S3-S5 state, the event will also wake the system. If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS.
6:0	-	-	**Reserved**

GPI General Purpose Events Enable (GPI_GPE_EN_GPP_D_0) – Offset 160

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_23)** Applied to GPP_D23. Same description as bit 0.
22	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_22)** Applied to GPP_D22. Same description as bit 0.
21	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_21)** Applied to GPP_D21. Same description as bit 0.
20	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_20)** Applied to GPP_D20. Same description as bit 0.
19	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_19)** Applied to GPP_D19. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
18	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_18)** Applied to GPP_D18. Same description as bit 0.
17	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_17)** Applied to GPP_D17. Same description as bit 0.
16	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_16)** Applied to GPP_D16. Same description as bit 0.
15	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_15)** Applied to GPP_D15. Same description as bit 0.
14	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_14)** Applied to GPP_D14. Same description as bit 0.
13	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_13)** Applied to GPP_D13. Same description as bit 0.
12	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_12)** Applied to GPP_D12. Same description as bit 0.
11	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_11)** Applied to GPP_D11. Same description as bit 0.
10	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_10)** Applied to GPP_D10. Same description as bit 0.
9	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_9)** Applied to GPP_D9. Same description as bit 0.
8	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_8)** Applied to GPP_D8. Same description as bit 0.
7	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_7)** Applied to GPP_D7. Same description as bit 0.
6	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_6)** Applied to GPP_D6. Same description as bit 0.
5	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_5)** Applied to GPP_D5. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
4	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_4)** Applied to GPP_D4. Same description as bit 0.
3	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_3)** Applied to GPP_D3. Same description as bit 0.
2	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_2)** Applied to GPP_D2. Same description as bit 0.
1	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_1)** Applied to GPP_D1. Same description as bit 0.
0	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_D_0)** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note:The pad must also be routed for GPE functionality in order for GPE tobe generated, i.e. the corresponding GPIRoutSCI must be set to '1'.

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_3) – Offset 7c0

This register applies to GPP_F3 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_3) – Offset 7c4

This register applies to GPP_F3 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 33h

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_4) – Offset 7d0

This register applies to GPP_F4 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_4) – Offset 7d4

This register applies to GPP_F4 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 34h

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_5) – Offset 7e0

This register applies to GPP_F5 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_5) – Offset 7e4

This register applies to GPP_F5 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 35h

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_6) – Offset 7f0

This register applies to GPP_F6 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_6) – Offset 7f4

This register applies to GPP_F6 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 36h

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_7) – Offset 800

This register applies to GPP_F7 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_7) – Offset 804

This register applies to GPP_F7 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 37h

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_8) – Offset 810

This register applies to GPP_F8 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_8) – Offset 814

This register applies to GPP_F8 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 38h

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_9) – Offset 820

This register applies to GPP_F9 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_9) – Offset 824

This register applies to GPP_F9 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 39h

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_10) – Offset 830

This register applies to GPP_F10 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_10) – Offset 834

This register applies to GPP_F10 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 3Ah

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_11) – Offset 840

This register applies to GPP_F11 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_11) – Offset 844

This register applies to GPP_F11 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 3Bh

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_12) – Offset 850

This register applies to GPP_F12 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_12) – Offset 854

This register applies to GPP_F12 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 3Ch

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_13) – Offset 860

This register applies to GPP_F13 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_13) – Offset 864

This register applies to GPP_F13 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 3Dh

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_14) – Offset 870

This register applies to GPP_F14 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_14) – Offset 874

This register applies to GPP_F14 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 3Eh

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_15) – Offset 880

This register applies to GPP_F15 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_15) – Offset 884

This register applies to GPP_F15 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 3Fh

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_16) – Offset 890

This register applies to GPP_F16 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_16) – Offset 894

This register applies to GPP_F16 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 40h

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_17) – Offset 8a0

This register applies to GPP_F17 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_17) – Offset 8a4

This register applies to GPP_F17 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 41h

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_18) – Offset 8b0

This register applies to GPP_F18 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_18) – Offset 8b4

This register applies to GPP_F18 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 42h

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_19) – Offset 8c0

This register applies to GPP_F19 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_19) – Offset 8c4

This register applies to GPP_F19 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 43h

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_20) – Offset 8d0

This register applies to GPP_F20 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_20) – Offset 8d4

This register applies to GPP_F20 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 44h

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_21) – Offset 8e0

This register applies to GPP_F21 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_21) – Offset 8e4

This register applies to GPP_F21 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 45h

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_22) – Offset 8f0

This register applies to GPP_F22 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_22) – Offset 8f4

This register applies to GPP_F22 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 46h

Pad Configuration DW0 (PAD_CFG_DW0_GPP_F_23) – Offset 900

This register applies to GPP_F23 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPP_F_23) – Offset 904

This register applies to GPP_F23 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 47h

GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_0) – Offset 164

Same description as GPI_GPE_EN_GPP_D_0 register, except that this is for GPP_F[23:0].

GPI General Purpose Events Enable (GPI_GPE_EN_GPP_H_0) – Offset 168

Same description as GPI_GPE_EN_GPP_D_0 register, except that this is for GPP_H[23:0].

GPI General Purpose Events Enable (GPI_GPE_EN_vGPIO_1) – Offset 170

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_vGPIO_39)** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'.
6:0	-	-	**Reserved**

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_3) – Offset 940

This register applies to GPP_H3 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_3) – Offset 944

This register applies to GPP_H3 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 4Bh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_4) – Offset 950

This register applies to GPP_H4 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_4) – Offset 954

This register applies to GPP_H4 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 4Ch

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_5) – Offset 960

This register applies to GPP_H5 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_5) – Offset 964

This register applies to GPP_H5 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 4Dh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_6) – Offset 970

This register applies to GPP_H6 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_6) – Offset 974

This register applies to GPP_H6 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 4Eh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_7) – Offset 980

This register applies to GPP_H7 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_7) – Offset 984

This register applies to GPP_H7 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 4Fh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_8) – Offset 990

This register applies to GPP_H8 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_8) – Offset 994

This register applies to GPP_H8 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 50h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_9) – Offset 9a0

This register applies to GPP_H9 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_9) – Offset 9a4

This register applies to GPP_H8 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 51h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_10) – Offset 9b0

This register applies to GPP_H10 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_10) – Offset 9b4

This register applies to GPP_H10 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 52h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_11) – Offset 9c0

This register applies to GPP_H11 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_11) – Offset 9c4

This register applies to GPP_H11 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 53h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_12) – Offset 9d0

This register applies to GPP_H12 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_12) – Offset 9d4

This register applies to GPP_H12 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 54h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_13) – Offset 9e0

This register applies to GPP_H13 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_13) – Offset 9e4

This register applies to GPP_H13 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 55h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_14) – Offset 9f0

This register applies to GPP_H14 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_14) – Offset 9f4

This register applies to GPP_H14 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 56h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_15) – Offset a00

This register applies to GPP_H15 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_15) – Offset a04

This register applies to GPP_H15 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 57h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_16) – Offset a10

This register applies to GPP_H16 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_16) – Offset a14

This register applies to GPP_H16 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 58h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_17) – Offset a20

This register applies to GPP_H17 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_17) – Offset a24

This register applies to GPP_H17 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 59h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_18) – Offset a30

This register applies to GPP_H18 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_18) – Offset a34

This register applies to GPP_H18 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 5Ah

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_19) – Offset a40

This register applies to GPP_H19 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_19) – Offset a44

This register applies to GPP_H19 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 5Bh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_20) – Offset a50

This register applies to GPP_H20 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_20) – Offset a54

This register applies to GPP_H20 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 5Ch

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_21) – Offset a60

This register applies to GPP_H21 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_21) – Offset a64

This register applies to GPP_H21 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 5Dh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_22) – Offset a70

This register applies to GPP_H22 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_22) – Offset a74

This register applies to GPP_H22 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 5Eh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_23) – Offset a80

This register applies to GPP_H23 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_23) – Offset a84

This register applies to GPP_H23 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 5Fh

Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_0) – Offset a90

Bit Range	Default	Access	Field Name and Description
31:30	01b	RO	**Pad Reset Config (PADRSTCFG)** This register controls which reset is used to reset GPIO pad register fields in PAD_CFG_DW0 and PAD_CFG_DW1 registers. This bit is hardwired to 01 01 = Host deep reset. This reset occurs when any of the following occur: Host reset(with or without power cycle) is initiated, Global reset is initiated, or Deep Sx entry.This reset does NOT occur as part of S3/S4/S5 entry.
29:24	-	-	**Reserved**
23	0b	RW	**RX Invert (RXINV)** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode.This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:11	-	-	**Reserved**
10	0b	RO	**Pad Mode (PMODE)** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad.0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad
9	0b	RW	**GPIO RX Disable (GPIORXDIS)** 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0'.
8	0b	RW	**GPIO TX Disable (GPIOTXDIS)** 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z

Bit Range	Default	Access	Field Name and Description
7:2	-	-	**Reserved**
1		RO/V	**GPIO RX State (GPIORXSTATE)** This is the current internal RX pad state after Glitch Filter logic stage and hardware debouncer (if any) and is not affected by PMode and RXINV settings.
0	1b	RW	**GPIO TX State (GPIOTXSTATE)** 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_3) – Offset ac0

Same definition as PAD_CFG_DW0_vGPIO_0.

Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_30) – Offset c70

Same definition as PAD_CFG_DW0_vGPIO_0.

Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_31) – Offset c80

Same definition as PAD_CFG_DW0_vGPIO_0.

Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_32) – Offset c90

Same definition as PAD_CFG_DW0_vGPIO_0.

Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_33) – Offset ca0

Same definition as PAD_CFG_DW0_vGPIO_0.

Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_34) – Offset cb0

Same definition as PAD_CFG_DW0_vGPIO_0.

Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_35) – Offset cc0

Same definition as PAD_CFG_DW0_vGPIO_0.

Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_36) – Offset cd0

Same definition as PAD_CFG_DW0_vGPIO_0.

Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_37) – Offset ce0

Same definition as PAD_CFG_DW0_vGPIO_0.

Pad Configuration DW0 (PAD_CFG_DW0_vGPIO_39) – Offset d00

Bit Range	Default	Access	Field Name and Description
31:30	01b	RO	**Pad Reset Config (PADRSTCFG)** This register controls which reset is used to resetGPIO pad register fields in PAD_CFG_DW0 and PAD_CFG_DW1 registers. This bit ishardwired to 01. 00 = RSMRST# 01 = Host deep reset. This reset occurs when any of the following occur: Host reset(with or without power cycle) is initiated, Global reset is initiated, or Deep Sx entry.This reset does NOT occur as part of S3/S4/S5 entry. 10 = PLTRST# 11 = Reserved
29:24	-	-	**Reserved**
23	0b	RW	**RX Invert (RXINV)** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion

Bit Range	Default	Access	Field Name and Description
22:21	-	-	**Reserved**
20	0b	RO	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC)** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0b	RO	**GPIO Input Route SCI (GPIROUTSCI)** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0b	RO	**GPIO Input Route SMI (GPIROUTSMI)** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default	Access	Field Name and Description
17	0b	RO	**GPIO Input Route NMI (GPIROUTNMI)** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	-	-	**Reserved**
10	1b	RW	**Pad Mode (PMODE)** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad 1h = Function 1, if applicable, control the Pad.
9	0b	RW	**GPIO RX Disable (GPIORXDIS)** 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0'.
8	0b	RW	**GPIO TX Disable (GPIOTXDIS)** 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	-	-	**Reserved**
1		RO/V	**GPIO RX State (GPIORXSTATE)** This is the current internal RX pad state after Glitch Filter logic stage and hardware debouncer (if any) and is not affected by PMode and RXINV settings.

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**GPIO TX State (GPIOTXSTATE)** 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_0) – Offset 910

This register applies to GPP_H0 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_0) – Offset 914

This register applies to GPP_H0 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 48h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_1) – Offset 920

This register applies to GPP_H1 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_1) – Offset 924

This register applies to GPP_H1 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 49h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_2) – Offset 930

This register applies to GPP_H2 and has the same description as PAD_CFG_DW0_GPP_D_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_2) – Offset 934

This register applies to GPP_H2 and has the same description as PAD_CFG_DW1_GPP_D_0.

Exception:

INTSEL bit field default: 4Ah

GPIO Community 2 Registers

GPIO pins are grouped into different Community (e.g. Community 0, Community 1,etc.). Each Community consists of one or more GPIO groups.

This section covers registers for Community 2, which consists of GPD group.

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8h	4	Family Base Address (FAMBAR)	300h
ch	4	Pad Base Address (PADBAR)	600h
10h	4	Miscellaneous Configuration (MISCCFG)	43200h
20h	4	Pad Ownership (PAD_OWN_DSW_0)	0h
24h	4	Pad Ownership (PAD_OWN_DSW_1)	0h
80h	4	Pad Configuration Lock (PADCFGLOCK_DSW_0)	0h
84h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_DSW_0)	0h
600h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_0)	44000X00h. Refer to register for X value
604h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_0)	60h
610h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_1)	44000X00h. Refer to register for X value
614h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_1)	3C61h
620h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_2)	44000X00h. Refer to register for X value
624h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_2)	3C62h
630h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_3)	44000X00h. Refer to register for X value

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
634h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_3)	3063h
638h	4	Pad Configuration DW2 (PAD_CFG_DW2_GPD_3)	10h
640h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_4)	44000X00h. Refer to register for X value
644h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_4)	64h
650h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_5)	44000X00h. Refer to register for X value
654h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_5)	65h
660h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_6)	44000X00h. Refer to register for X value
664h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_6)	66h
670h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_7)	44000X00h. Refer to register for X value
674h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_7)	67h
680h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_8)	44000X00h. Refer to register for X value
684h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_8)	68h
690h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_9)	44000X00h. Refer to register for X value
694h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_9)	69h
b0h	4	Host Software Pad Ownership (HOSTSW_OWN_DSW_0)	0h
120h	4	GPI Interrupt Enable (GPI_IE_DSW_0)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
140h	4	GPI General Purpose Events Status (GPI_GPE_STS_DSW_0)	0h
160h	4	GPI General Purpose Events Enable (GPI_GPE_EN_DSW_0)	0h
6a0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_10)	44000X00h. Refer to register for X value
6a4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_10)	6Ah
6b0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPD_11)	44000X00h. Refer to register for X value
6b4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPD_11)	6Bh

Family Base Address (FAMBAR) – Offset 8

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	300h	RO	**Family Base Address (FAMBAR)** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

Pad Base Address (PADBAR) – Offset c

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
15:0	600h	RO	**Pad Base Address (PADBAR)** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

Miscellaneous Configuration (MISCCFG) – Offset 10

Bit Range	Default	Access	Field Name and Description
30:20	-	-	**Reserved**
19:16	0100b	RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2)** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 1h = GPP_B[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 2h = GPP_G[7:0] mapped to GPE[71:64]; GPE[95:72] not used. 3h = Reserved. 4h = GPP_C[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 5h = GPP_D[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 6h = GPP_F[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 7h = GPP_H[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 8h = vGPIO39 (vSD_CD#) mapped to GPE bit 70. 9h = Reserved Ah = GPD[11:0] mapped to GPE[75:64]; GPE[95:76] not used Bh - Ch = Reserved Dh = GPP_E[23:0] mapped to GPE[87:64]; GPE[95:88] not used. Eh - Fh = Reserved

Bit Range	Default	Access	Field Name and Description
15:12	0011b	RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1)** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 1h = GPP_B[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 2h = GPP_G[7:0] mapped to GPE[39:32]; GPE[63:40] not used. 3h = Reserved. 4h = GPP_C[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 5h = GPP_D[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 6h = GPP_F[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 7h = GPP_H[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 8h = vGPIO39 (vSD_CD#) mapped to GPE bit 38. 9h = Reserved Ah = GPD[11:0] mapped to GPE[43:32]; GPE[63:44] not used Bh - Ch = Reserved Dh = GPP_E[23:0] mapped to GPE[55:32]; GPE[63:56] not used. Dh = GPP_E[23:0] mapped to GPE[55:32]; GPE[63:56] not used. Eh - Fh = Reserved

Bit Range	Default	Access	Field Name and Description
11:8	0010b	RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0)** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 1h = GPP_B[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 2h = GPP_G[7:0] mapped to GPE[7:0]; GPE[31:8] not used. 3h = Reserved. 4h = GPP_C[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 5h = GPP_D[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 6h = GPP_F[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 7h = GPP_H[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 8h = vGPIO_39 (vSD_CD#) mapped to GPE bit 7.9h = Reserved Ah = GPD[11:0] mapped to GPE[11:0]; GPE[31:12] not used Bh - Ch = Reserved Dh = GPP_E[23:0] mapped to GPE[23:0]; GPE[31:24] not used Eh - Fh = Reserved

Bit Range	Default	Access	Field Name and Description
7:2	-	-	**Reserved**
1	0b	RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN)** Specifies whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating.
0	0b	RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN)** Specifies whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating.

Pad Ownership (PAD_OWN_DSW_0) – Offset 20

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29:28	00b	RW	**Pad Ownership (PAD_OWN_GPD_7)** Same description as bits [1:0], except that the bit field applies to GPD7.
27:26	-	-	**Reserved**
25:24	00b	RW	**Pad Ownership (PAD_OWN_GPD_6)** Same description as bits [1:0], except that the bit field applies to GPD6.
23:22	-	-	**Reserved**
21:20	00b	RW	**Pad Ownership (PAD_OWN_GPD_5)** Same description as bits [1:0], except that the bit field applies to GPD5.
19:18	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
17:16	00b	RW	**Pad Ownership (PAD_OWN_GPD_4)** Same description as bits [1:0], except that the bit field applies to GPD4.
15:14	-	-	**Reserved**
13:12	00b	RW	**Pad Ownership (PAD_OWN_GPD_3)** Same description as bits [1:0], except that the bit field applies to GPD3.
11:10	-	-	**Reserved**
9:8	00b	RW	**Pad Ownership (PAD_OWN_GPD_2)** Same description as bits [1:0], except that the bit field applies to GPD2.
7:6	-	-	**Reserved**
5:4	00b	RW	**Pad Ownership (PAD_OWN_GPD_1)** Same description as bits [1:0], except that the bit field applies to GPD1.
3:2	-	-	**Reserved**
1:0	00b	RW	**Pad Ownership (PAD_OWN_GPD_0)** 00 = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIODriver) has ownership of the pad. In Host GPIO Driver Mode (refer toHOSTSW_OWN), GPIO input event update is limited to GPI_STS update only.Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STSand/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership 01 = ME GPIO Mode. ME has ownership of the pad. 10 = ISH GPIO Mode. ME has ownership of the pad 11 = Reserved

Pad Ownership (PAD_OWN_DSW_1) – Offset 24

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13:12	00b	RW	**Pad Ownership (PAD_OWN_GPD_11)** Same description as bit [1:0] in PAD_OWN_DSW_0, except that this register is for GPD11.
11:10	-	-	**Reserved**
9:8	00b	RW	**Pad Ownership (PAD_OWN_GPD_10)** Same description as bit [1:0] in PAD_OWN_DSW_0, except that this register is for GPD10.
7:6	-	-	**Reserved**
5:4	00b	RW	**Pad Ownership (PAD_OWN_GPD_9)** Same description as bit [1:0] in PAD_OWN_DSW_0, except that this register is for GPD9.
3:2	-	-	**Reserved**
1:0	00b	RW	**Pad Ownership (PAD_OWN_GPD_8)** Same description as bit [1:0] in PAD_OWN_DSW_0, except that this register is for GPD8.

Pad Configuration Lock (PADCFGLOCK_DSW_0) – Offset 80

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**
11	0b	RW	**Pad Config Lock (PADCFGLOCK_GPD_11)** Applied to GPD11. Same description as PADCFGLOCK_GPD_0.

Bit Range	Default	Access	Field Name and Description
10	0b	RW	**Pad Config Lock (PADCFGLOCK_GPD_10)** Applied to GPD10. Same description as bit 0.
9	0b	RW	**Pad Config Lock (PADCFGLOCK_GPD_9)** Applied to GPD9. Same description as bit 0.
8	0b	RW	**Pad Config Lock (PADCFGLOCK_GPD_8)** Applied to GPD8. Same description as bit 0.
7	0b	RW	**Pad Config Lock (PADCFGLOCK_GPD_7)** Applied to GPD7. Same description as bit 0.
6	0b	RW	**Pad Config Lock (PADCFGLOCK_GPD_6)** Applied to GPD6. Same description as bit 0.
5	0b	RW	**Pad Config Lock (PADCFGLOCK_GPD_5)** Applied to GPD5. Same description as bit 0.
4	0b	RW	**Pad Config Lock (PADCFGLOCK_GPD_4)** Applied to GPD4. Same description as bit 0.
3	0b	RW	**Pad Config Lock (PADCFGLOCK_GPD_3)** Applied to GPD3. Same description as bit 0.
2	0b	RW	**Pad Config Lock (PADCFGLOCK_GPD_2)** Applied to GPD2. Same description as bit 0.
1	0b	RW	**Pad Config Lock (PADCFGLOCK_GPD_1)** Applied to GPD1. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**Pad Config Lock (PADCFGLOCK_GPD_0)** Pad Configuration Lock locks specific register fields in the GPP specific registers from being configured. The registers affected become Read-Only and software writes to these registers have no effect. 0 = Unlock 1 = Lock the following register fields as read-only (RO): - Pad Configuration registers (exclude GPIOTXState) - GPI_NMI_EN Register (if implemented) - GPI_SMI_EN Register (if implemented) - GPI_GPE_EN Register (if implemented) When PadCfgLock is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_DSW_0) – Offset 84

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**
11	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_11)** Applied to GPD4. Same description as bit 0.
10	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_10)** Applied to GPD10. Same description as bit 0.
9	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_9)** Applied to GPD9. Same description as bit 0.
8	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_8)** Applied to GPD8. Same description as bit 0.
7	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_7)** Applied to GPD7. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
6	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_6)** Applied to GPD6. Same description as bit 0.
5	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_5)** Applied to GPD5. Same description as bit 0.
4	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_4)** Applied to GPD4. Same description as bit 0.
3	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_3)** Applied to GPD3. Same description as bit 0.
2	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_2)** Applied to GPD2. Same description as bit 0.
1	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_1)** Applied to GPD1. Same description as bit 0.
0	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_0)** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) When PadCfgLockTx is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

Pad Configuration DW0 (PAD_CFG_DW0_GPD_0) – Offset 600

This register applies to GPD0.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:30	00b	RW	**Pad Reset Config (PADRSTCFG)** This register controls which reset is used to reset GPIO pad register fields in PAD_CFG_DW0 and PAD_CFG_DW1 registers. This register can be used for Sx isolation of the associated signal if needed. 00 = DSW_PWROK# 01 = Host deep reset. This reset occurs when any of the following occur: Host reset (with or without power cycle) is initiated, Global reset is initiated, or Deep Sx entry. This reset does NOT occur as part of S3/S4/S5 entry. 10 = PLTRST# 11 = RSMRST#
29	0b	RW	**RX Pad State Select (RXPADSTSEL)** Determines from which node the RX pad state for native function should be taken from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from RX buffer 1 = Internal RX pad state (subject to RXINV and PreGfRXSel settings)
28	0b	RW	**RX Raw Override to '1' (RXRAW1)** This bit determines if the selected pad state is being overridden to '1'. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
26:25	10b	RW	**RX Level/Edge Configuration (RXEVCFG)** Determines if the internal RX pad state (synchronized, filtered vs non-filtered version as determined by PreGfRXSel, and is further subject to RXInv) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller . 0h = Level 1h = Edge (RxInv=0 for rising edge; 1 for falling edge) 2h = Disable 3h = Either rising edge or falling edge
24	0b	RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL)** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0b	RW	**RX Invert (RXINV)** This bit determines if the selected pad state should go through the polarity inversion stage. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion

Bit Range	Default	Access	Field Name and Description
22:21	00b	RO	**RX/TX Enable Config (RXTXENCFG)** This controls the RX and TX buffer enablement for the function selected by Pad Mode. This field is not applicable in GPIO mode (PMode = 0. 0h = Function defined in Pad Mode controls TX and RX enablement 1h = Function controls TX enablement and RX is disabled with 0 being driven internally 2h = Function controls TX enablement and RX is disabled with 1 being driven internally 3h = Function controls TX enablement and RX is always enabled
20	0b	RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC)** Determines if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0b	RW	**GPIO Input Route SCI (GPIROUTSCI)** Determines if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI. 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s).

Bit Range	Default	Access	Field Name and Description
18	0b	RO	**GPIO Input Route SMI (GPIROUTSMI)** Determines if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s). This bit only applies to a GPIO that has SMI capability. Otherwise, the bit is RO.
17	0b	RO	**GPIO Input Route NMI (GPIROUTNMI)** Determines if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit. This bit only applies to a GPIO that has NMI capability. Otherwise, the bit is RO.
16:11	-	-	**Reserved**
10	See Description	RW	**Pad Mode (PMODE)** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad. 1h = native function 1, if applicable, controls the Pad Dedicated (unmuxed) GPIO shall report RO of all 0's in this register field If GPIO vs. native mode is configured via soft strap, this bit has no effect. Default value is determined by the default functionality of the pad.

Bit Range	Default	Access	Field Name and Description
9	1b	RW	**GPIO RX Disable (GPIORXDIS)** 0 = Enable the input buffer (active low enable) of the pad. 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0'.
8	1b	RW	**GPIO TX Disable (GPIOTXDIS)** 0 = Enable the output buffer (active low enable) of the pad. 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	-	-	**Reserved**
1		RO/V	**GPIO RX State (GPIORXSTATE)** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV settings.
0	0b	RW	**GPIO TX State (GPIOTXSTATE)** 0 = Drive a level '0' to the TX output pad. 1 = Drive a level '1' to the TX output pad.

Pad Configuration DW1 (PAD_CFG_DW1_GPD_0) – Offset 604

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
13:10	0000b	RW	**Termination (TERM)** The Pad Termination state defines the different weak internal pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. Others: Reserved NOTES: 1. The internal 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily.
9:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	60h	RO	**Interrupt Select (INTSEL)** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 .... Up to the max IOxAPIC IRQ supported.

Pad Configuration DW0 (PAD_CFG_DW0_GPD_1) – Offset 610

This register applies to GPD1 and has the same description as PAD_CFG_DW0_GPD_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPD_1) – Offset 614

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13:10	1111b	RW	**Termination (TERM)** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	-	-	**Reserved**
7:0	61h	RO	**Interrupt Select (INTSEL)** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

Pad Configuration DW0 (PAD_CFG_DW0_GPD_2) – Offset 620

This register applies to GPD2 and has the same description as PAD_CFG_DW0_GPD_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPD_2) – Offset 624

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13:10	1111b	RW	**Termination (TERM)** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	-	-	**Reserved**
7:0	62h	RO	**Interrupt Select (INTSEL)** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

Pad Configuration DW0 (PAD_CFG_DW0_GPD_3) – Offset 630

This register applies to GPD3 and has the same description as PAD_CFG_DW0_GPD_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPD_3) – Offset 634

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13:10	1100b	RW	**Termination (TERM)** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	-	-	**Reserved**
7:0	63h	RO	**Interrupt Select (INTSEL)** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

Pad Configuration DW2 (PAD_CFG_DW2_GPD_3) – Offset 638

This register applies to GPD3 pad only.

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4:1	1000b	RW	**Debounce duration (DEBOUNCE)** The debounce duration of value should be not less than 3. In other words, the value should not be any of 0, 1 and 2. The debounce time should be calculated as (2^debounce) * (glitch filter clock period). For example, when RTC clock (32 KHz) is used for glitch filter and debounce duration is set to 4b1011, the debounce time is (2 ^ 11) * (31.25 us) = 64ms
0	0b	RW	**Debounce Enable (DEBEN)** This bit enables or disables the debouncer with the pad. 1 = Enable the debouncer of the pad 0 = Disable the debouncer of the pad

Pad Configuration DW0 (PAD_CFG_DW0_GPD_4) – Offset 640

This register applies to GPD4 and has the same description as PAD_CFG_DW0_GPD_0.

Exception: the PMODE bit is RO/V bit.

Pad Configuration DW1 (PAD_CFG_DW1_GPD_4) – Offset 644

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13:10	0000b	RW	**Termination (TERM)** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	-	-	**Reserved**
7:0	64h	RO	**Interrupt Select (INTSEL)** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

Pad Configuration DW0 (PAD_CFG_DW0_GPD_5) – Offset 650

This register applies to GPD5 and has the same description as PAD_CFG_DW0_GPD_0.

Exception: the PMODE bit is RO/V bit.

Pad Configuration DW1 (PAD_CFG_DW1_GPD_5) – Offset 654

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13:10	0000b	RW	**Termination (TERM)** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	-	-	**Reserved**
7:0	65h	RO	**Interrupt Select (INTSEL)** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

Pad Configuration DW0 (PAD_CFG_DW0_GPD_6) – Offset 660

This register applies to GPD6 and has the same description as PAD_CFG_DW0_GPD_0.

Exception: the PMODE bit is RO/V bit.

Pad Configuration DW1 (PAD_CFG_DW1_GPD_6) – Offset 664

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13:10	0000b	RW	**Termination (TERM)** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	66h	RO	**Interrupt Select (INTSEL)** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

Pad Configuration DW0 (PAD_CFG_DW0_GPD_7) – Offset 670

This register applies to GPD7 and has the same description as PAD_CFG_DW0_GPD_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPD_7) – Offset 674

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13:10	0000b	RW	**Termination (TERM)** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	-	-	**Reserved**
7:0	67h	RO	**Interrupt Select (INTSEL)** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

Pad Configuration DW0 (PAD_CFG_DW0_GPD_8) – Offset 680

This register applies to GPD8 and has the same description as PAD_CFG_DW0_GPD_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPD_8) – Offset 684

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13:10	0000b	RW	**Termination (TERM)** Same description as TERM bits in PAD_CFG_DW1_GPD_0.

Bit Range	Default	Access	Field Name and Description
9:8	-	-	**Reserved**
7:0	68h	RO	**Interrupt Select (INTSEL)** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

Pad Configuration DW0 (PAD_CFG_DW0_GPD_9) – Offset 690

This register applies to GPD9 and has the same description as PAD_CFG_DW0_GPD_0.

Exception: the PMODE bit is RO/V bit.

Pad Configuration DW1 (PAD_CFG_DW1_GPD_9) – Offset 694

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13:10	0000b	RW	**Termination (TERM)** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	-	-	**Reserved**
7:0	69h	RO	**Interrupt Select (INTSEL)** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

Host Software Pad Ownership (HOSTSW_OWN_DSW_0) – Offset b0

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
11	0b	RW	**HostSW_Own (HOSTSW_OWN_GPD_11)** Applied to GPD11. Same description as bit 0.
10	0b	RW	**HostSW_Own (HOSTSW_OWN_GPD_10)** Applied to GPD10. Same description as bit 0.
9	0b	RW	**HostSW_Own (HOSTSW_OWN_GPD_9)** Applied to GPD9. Same description as bit 0.
8	0b	RW	**HostSW_Own (HOSTSW_OWN_GPD_8)** Applied to GPD8. Same description as bit 0.
7	0b	RW	**HostSW_Own (HOSTSW_OWN_GPD_7)** Applied to GPD7. Same description as bit 0.
6	0b	RW	**HostSW_Own (HOSTSW_OWN_GPD_6)** Applied to GPD6. Same description as bit 0.
5	0b	RW	**HostSW_Own (HOSTSW_OWN_GPD_5)** Applied to GPD5. Same description as bit 0.
4	0b	RW	**HostSW_Own (HOSTSW_OWN_GPD_4)** Applied to GPD4. Same description as bit 0.
3	0b	RW	**HostSW_Own (HOSTSW_OWN_GPD_3)** Applied to GPD3. Same description as bit 0.
2	0b	RW	**HostSW_Own (HOSTSW_OWN_GPD_2)** Applied to GPD2. Same description as bit 0.
1	0b	RW	**HostSW_Own (HOSTSW_OWN_GPD_1)** Applied to GPD1. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**HostSW_Own (HOSTSW_OWN_GPD_0)** This register determines the appropriate host status bit update when a pad is under host ownership. 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS,GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited toGPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updatesare masked.

GPI Interrupt Enable (GPI_IE_DSW_0) – Offset 120

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**
11	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_11)** Applied to GPD11. Same description as bit 0.
10	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_10)** Applied to GPD10. Same description as bit 0.
9	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_9)** Applied to GPD9. Same description as bit 0.
8	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_8)** Applied to GPD8. Same description as bit 0.
7	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_7)** Applied to GPD7. Same description as bit 0.
6	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_6)** Applied to GPD6. Same description as bit 0.
5	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_5)** Applied to GPD5. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
4	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_4)** Applied to GPD4. Same description as bit 0.
3	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_3)** Applied to GPD3. Same description as bit 0.
2	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_2)** Applied to GPD2. Same description as bit 0.
1	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_1)** Applied to GPD1. Same description as bit 0.
0	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_0)** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation

GPI General Purpose Events Status (GPI_GPE_STS_DSW_0) – Offset 140

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**
11	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_11)** Applied to GPD11. Same description as bit 0.
10	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_10)** Applied to GPD10. Same description as bit 0.
9	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_9)** Applied to GPD9. Same description as bit 0.
8	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_8)** Applied to GPD8. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
7	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_7)** Applied to GPD7. Same description as bit 0.
6	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_6)** Applied to GPD6. Same description as bit 0.
5	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_5)** Applied to GPD5. Same description as bit 0.
4	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_4)** Applied to GPD4. Same description as bit 0.
3	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_3)** Applied to GPD3. Same description as bit 0.
2	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_2)** Applied to GPD2. Same description as bit 0.
1	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_1)** Applied to GPD1. Same description as bit 0.
0	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_0)** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high(or low if the corresponding RXINV bit is set). If the correspondingenable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: - If the system is in an S3-S5 state, the event will also wake the system. - If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for thecorresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS.

GPI General Purpose Events Enable (GPI_GPE_EN_DSW_0) – Offset 160

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**
11	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_11)** Applied to GPD11. Same description as bit 0.
10	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_10)** Applied to GPD10. Same description as bit 0.
9	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_9)** Applied to GPD9. Same description as bit 0.
8	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_8)** Applied to GPD8. Same description as bit 0.
7	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_7)** Applied to GPD7. Same description as bit 0.
6	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_6)** Applied to GPD6. Same description as bit 0.
5	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_5)** Applied to GPD5. Same description as bit 0.
4	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_4)** Applied to GPD4. Same description as bit 0.
3	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_3)** Applied to GPD3. Same description as bit 0.
2	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_2)** Applied to GPD2. Same description as bit 0.
1	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_1)** Applied to GPD1. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_0)** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note:The pad must also be routed for GPE functionality in order for GPE tobe generated, i.e. the corresponding GPIRoutSCI must be set to '1'.

Pad Configuration DW0 (PAD_CFG_DW0_GPD_10) – Offset 6a0

This register applies to GPD10 and has the same description as PAD_CFG_DW0_GPD_0.

Exception: the PMODE bit is RO/V bit.

Pad Configuration DW1 (PAD_CFG_DW1_GPD_10) – Offset 6a4

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13:10	0000b	RW	**Termination (TERM)** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	-	-	**Reserved**
7:0	6Ah	RO	**Interrupt Select (INTSEL)** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

Pad Configuration DW0 (PAD_CFG_DW0_GPD_11) – Offset 6b0

This register applies to GPD11 and has the same description as PAD_CFG_DW0_GPD_0.

Exception: the PMODE bit is RO/V bit.

Pad Configuration DW1 (PAD_CFG_DW1_GPD_11) – Offset 6b4

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13:10	0000b	RW	**Termination (TERM)** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	-	-	**Reserved**
7:0	6Bh	RO	**Interrupt Select (INTSEL)** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

GPIO Community 3 Registers

Community 3 contains registers for selecting muxed functions on audio signals.

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
600h	4	Pad Configuration DW0 (PAD_CFG_DW0_HDA_BCLK)	400h
610h	4	Pad Configuration DW0 (PAD_CFG_DW0_HDA_RSTB)	400h
620h	4	Pad Configuration DW0 (PAD_CFG_DW0_HDA_SYNC)	400h
630h	4	Pad Configuration DW0 (PAD_CFG_DW0_HDA_SDO)	400h
640h	4	Pad Configuration DW0 (PAD_CFG_DW0_HDA_SDI_0)	400h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
650h	4	Pad Configuration DW0 (PAD_CFG_DW0_HDA_SDI_1)	400h
660h	4	Pad Configuration DW0 (PAD_CFG_DW0_SSP1_SFRM)	400h
670h	4	Pad Configuration DW0 (PAD_CFG_DW0_SSP1_TXD)	400h

Pad Configuration DW0 (PAD_CFG_DW0_HDA_BCLK) – Offset 600

Bit Range	Default	Access	Field Name and Description
30:13	-	-	**Reserved**
12:10	001b	RW	**Pad Mode (PMODE)** This field determines whether the Pad is controlled by one of the native functions muxed onto the Pad. 1h = HDA_BCLK controls the Pad (default) 2h = I2S0_SCLK controls the Pad Others = Reserved
9:0	-	-	**Reserved**

Pad Configuration DW0 (PAD_CFG_DW0_HDA_RSTB) – Offset 610

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
11:10	01b	RW	**Pad Mode (PMODE)** This field determines whether the Pad is controlled by one of the native functions muxed onto the Pad.1h = HDA_RST# controls the Pad (default) 2h = I2S1_SCLK controls the Pad 3h = SNDW1_CLK Others = Reserved
9:0	-	-	**Reserved**

Pad Configuration DW0 (PAD_CFG_DW0_HDA_SYNC) – Offset 620

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**
11:10	01b	RW	**Pad Mode (PMODE)** This field determines whether the Pad is controlled by one of the native functions muxed onto the Pad.1h = HDA_SYNC controls the Pad (default) 2h = I2S0_SFRM controls the Pad 0thers = Reserved
9:0	-	-	**Reserved**

Pad Configuration DW0 (PAD_CFG_DW0_HDA_SDO) – Offset 630

Bit Range	Default	Access	Field Name and Description
30:13	-	-	**Reserved**
12:10	001b	RW	**Pad Mode (PMODE)** This field determines whether the Pad is controlled by one of the native functions muxed onto the Pad.1h = HDA_SDO controls the Pad (default) 2h = I2S0_TXD controls the Pad Others = Reserved
9:0	-	-	**Reserved**

Pad Configuration DW0 (PAD_CFG_DW0_HDA_SDI_0) – Offset 640

Bit Range	Default	Access	Field Name and Description
30:13	-	-	**Reserved**
12:10	001b	RW	**Pad Mode (PMODE)** This field determines whether the Pad is controlled by one of the native functions muxed onto the Pad.1h = HDA_SDI0 controls the Pad (default) 2h = I2S0_RXD controls the Pad Others = Reserved
9:0	-	-	**Reserved**

Pad Configuration DW0 (PAD_CFG_DW0_HDA_SDI_1) – Offset 650

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
11:10	01b	RW	**Pad Mode (PMODE)** This field determines whether the Pad is controlled by one of the native functions muxed onto the Pad.1h = HDA_SDI1 controls the Pad (default) 2h = I2S1_RXD controls the Pad 3h = SNDW1_DATA controls the Pad Others = Reserved
9:0	-	-	**Reserved**

Pad Configuration DW0 (PAD_CFG_DW0_SSP1_SFRM) – Offset 660

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**
11:10	01b	RW	**Pad Mode (PMODE)** This field determines whether the Pad is controlled by one of the native functions muxed onto the Pad.1h = I2S1_SFRM controls the Pad (default) 2h = SNDW2_CLK controls the Pad Others = Reserved
9:0	-	-	**Reserved**

Pad Configuration DW0 (PAD_CFG_DW0_SSP1_TXD) – Offset 670

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
11:10	01b	RW	**Pad Mode (PMODE)** This field determines whether the Pad is controlled by one of the native functions muxed onto the Pad.1h = I2S1_TXD controls the Pad (default) 2h = SNDW2_DATA controls the Pad Others = Reserved
9:0	-	-	**Reserved**

GPIO Community 4 Registers

GPIO pins are grouped into different Community (e.g. Community 0, Community 1,etc.). Each Community consists of one or more GPIO groups.

This section covers registers for Community 4, which consists of GPP_C and GPP_E groups.

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
720h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_18)	44000X00h. Refer to register for X value
724h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_18)	See Register
730h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_19)	44000X00h. Refer to register for X value
734h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_19)	See Register
740h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_20)	44000X00h. Refer to register for X value
744h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_20)	See Register

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
750h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_21)	44000X00h. Refer to register for X value
8h	4	Family Base Address (FAMBAR)	300h
ch	4	Pad Base Address (PADBAR)	600h
10h	4	Miscellaneous Configuration (MISCCFG)	43200h
20h	4	Pad Ownership (PAD_OWN_GPP_C_0)	0h
24h	4	Pad Ownership (PAD_OWN_GPP_C_1)	0h
28h	4	Pad Ownership (PAD_OWN_GPP_C_2)	0h
2ch	4	Pad Ownership (PAD_OWN_GPP_E_0)	0h
754h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_21)	See Register
760h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_22)	44000X00h. Refer to register for X value
764h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_22)	See Register
770h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_23)	44000X00h. Refer to register for X value
774h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_23)	See Register
780h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_0)	44000X00h. Refer to register for X value
784h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_0)	See Register
30h	4	Pad Ownership (PAD_OWN_GPP_E_1)	0h
34h	4	Pad Ownership (PAD_OWN_GPP_E_2)	0h
80h	4	Pad Configuration Lock (PADCFGLOCK_GPP_C_0)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
84h	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_C_0)	0h
88h	4	Pad Configuration Lock (PADCFGLOCK_GPP_E_0)	0h
8ch	4	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_E_0)	0h
b0h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_C_0)	0h
790h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_1)	44000X00h. Refer to register for X value
794h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_1)	See Register
7a0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_2)	44000X00h. Refer to register for X value
7a4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_2)	See Register
7b0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_3)	44000X00h. Refer to register for X value
7b4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_3)	See Register
7c0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_4)	44000X00h. Refer to register for X value
7c4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_4)	See Register
7d0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_5)	44000X00h. Refer to register for X value
7d4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_5)	See Register
7e0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_6)	44000X00h. Refer to register for X value
7e4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_6)	See Register

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
7f0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_7)	44000X00h. Refer to register for X value
7f4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_7)	See Register
800h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_8)	44000X00h. Refer to register for X value
804h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_8)	See Register
810h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_9)	44000X00h. Refer to register for X value
814h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_9)	See Register
820h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_10)	44000X00h. Refer to register for X value
824h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_10)	See Register
830h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_11)	44000X00h. Refer to register for X value
834h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_11)	See Register
840h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_12)	44000X00h. Refer to register for X value
844h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_12)	See Register
850h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_13)	44000X00h. Refer to register for X value
854h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_13)	See Register
860h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_14)	44000X00h. Refer to register for X value
864h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_14)	See Register

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
870h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_15)	44000X00h. Refer to register for X value
874h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_15)	See Register
880h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_16)	44000X00h. Refer to register for X value
884h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_16)	See Register
890h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_17)	44000X00h. Refer to register for X value
894h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_17)	See Register
8a0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_18)	44000X00h. Refer to register for X value
8a4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_18)	See Register
8b0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_19)	44000X00h. Refer to register for X value
8b4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_19)	See Register
8c0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_20)	44000X00h. Refer to register for X value
8c4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_20)	See Register
8d0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_21)	44000X00h. Refer to register for X value
8d4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_21)	See Register
b4h	4	Host Software Pad Ownership (HOSTSW_OWN_GPP_E_0)	0h
100h	4	GPI Interrupt Status (GPI_IS_GPP_C_0)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
104h	4	GPI Interrupt Status (GPI_IS_GPP_E_0)	0h
120h	4	GPI Interrupt Enable (GPI_IE_GPP_C_0)	0h
124h	4	GPI Interrupt Enable (GPI_IE_GPP_E_0)	0h
140h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_0)	0h
144h	4	GPI General Purpose Events Status (GPI_GPE_STS_GPP_E_0)	0h
160h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_0)	0h
164h	4	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_E_0)	0h
180h	4	SMI Status (GPI_SMI_STS_GPP_C_0)	0h
184h	4	SMI Status (GPI_SMI_STS_GPP_E_0)	0h
1c0h	4	NMI Status (GPI_NMI_STS_GPP_C_0)	0h
1c4h	4	NMI Status (GPI_NMI_STS_GPP_E_0)	0h
1e0h	4	NMI Enable (GPI_NMI_EN_GPP_C_0)	0h
1e4h	4	NMI Enable (GPI_NMI_EN_GPP_E_0)	0h
600h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_0)	44000X00h. Refer to register for X value
604h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_0)	See Register
610h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_1)	44000X00h. Refer to register for X value
614h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_1)	See Register
620h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_2)	44000X00h. Refer to register for X value
624h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_2)	See Register

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
630h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_3)	44000X00h. Refer to register for X value
634h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_3)	See Register
640h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_4)	44000X00h. Refer to register for X value
644h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_4)	See Register
650h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_5)	44000X00h. Refer to register for X value
654h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_5)	See Register
660h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_6)	44000X00h. Refer to register for X value
664h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_6)	See Register
670h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_7)	44000X00h. Refer to register for X value
674h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_7)	See Register
680h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_8)	44000X00h. Refer to register for X value
684h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_8)	See Register
690h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_9)	44000X00h. Refer to register for X value
694h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_9)	See Register
6a0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_10)	44000X00h. Refer to register for X value
6a4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_10)	See Register

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
6b0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_11)	44000X00h. Refer to register for X value
6b4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_11)	See Register
6c0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_12)	44000X00h. Refer to register for X value
6c4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_12)	See Register
6d0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_13)	44000X00h. Refer to register for X value
6d4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_13)	See Register
6e0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_14)	44000X00h. Refer to register for X value
6e4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_14)	See Register
6f0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_15)	44000X00h. Refer to register for X value
6f4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_15)	See Register
700h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_16)	44000X00h. Refer to register for X value
704h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_16)	See Register
8e0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_22)	44000X00h. Refer to register for X value
8e4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_22)	See Register
8f0h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_23)	44000X00h. Refer to register for X value
8f4h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_23)	See Register

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
710h	4	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_17)	44000X00h. Refer to register for X value
714h	4	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_17)	See Register

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_18) – Offset 720

This register applies to GPP_C18 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_18) – Offset 724

This register applies to GPP_C18 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 5Ah

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_19) – Offset 730

This register applies to GPP_C19 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_19) – Offset 734

This register applies to GPP_C19 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 5Bh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_20) – Offset 740

This register applies to GPP_C20 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_20) – Offset 744

This register applies to GPP_C20 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 5Ch

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_21) – Offset 750

This register applies to GPP_C21 and has the same description as PAD_CFG_DW0_GPP_C_0.

Family Base Address (FAMBAR) – Offset 8

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	300h	RO	**Family Base Address (FAMBAR)** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

Pad Base Address (PADBAR) – Offset c

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	600h	RO	**Pad Base Address (PADBAR)** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

Miscellaneous Configuration (MISCCFG) – Offset 10

Bit Range	Default	Access	Field Name and Description
30:20	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
19:16	0100b	RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2)** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 1h = GPP_B[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 2h = GPP_G[7:0] mapped to GPE[71:64]; GPE[95:72] not used. 3h = Reserved. 4h = GPP_C[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 5h = GPP_D[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 6h = GPP_F[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 7h = GPP_H[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 8h = vGPIO39 (vSD_CD#) mapped to GPE bit 70. 9h = Reserved Ah = GPD[11:0] mapped to GPE[75:64]; GPE[95:76] not used Bh - Ch = Reserved Dh = GPP_E[23:0] mapped to GPE[87:64]; GPE[95:88] not used. Eh - Fh = Reserved
15:12	0011b	RW	

Bit Range	Default	Access	GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1) Field Name and Description
			This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 1h = GPP_B[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 2h = GPP_G[7:0] mapped to GPE[39:32]; GPE[63:40] not used. 3h = Reserved. 4h = GPP_C[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 5h = GPP_D[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 6h = GPP_F[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 7h = GPP_H[23:0] mapped to GPE[55:32]; GPE[63:56] not used. 8h = vGPIO39 (vSD_CD#) mapped to GPE bit 38. 9h = Reserved Ah = GPD[11:0] mapped to GPE[43:32]; GPE[63:44] not used Bh - Ch = Reserved Dh = GPP_E[23:0] mapped to GPE[55:32]; GPE[63:56] not used. Dh = GPP_E[23:0] mapped to GPE[55:32]; GPE[63:56] not used. Eh - Fh = Reserved

Bit Range	Default	Access	Field Name and Description
11:8	0010b	RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0)** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 1h = GPP_B[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 2h = GPP_G[7:0] mapped to GPE[7:0]; GPE[31:8] not used. 3h = Reserved. 4h = GPP_C[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 5h = GPP_D[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 6h = GPP_F[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 7h = GPP_H[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 8h = vGPIO_39 (vSD_CD#) mapped to GPE bit 7.9h = Reserved Ah = GPD[11:0] mapped to GPE[11:0]; GPE[31:12] not used Bh - Ch = Reserved Dh = GPP_E[23:0] mapped to GPE[23:0]; GPE[31:24] not used Eh - Fh = Reserved
7:2	-	-	**Reserved**
1	0b	RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN)** Specifies whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating
0	0b	RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN)** Specifies whether the GPIO Community should perform local clock gating. 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating

Pad Ownership (PAD_OWN_GPP_C_0) – Offset 20

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29:28	00b	RW	**Pad Ownership (PAD_OWN_GPPC_C_7)** Same description as bits [1:0], except that the bit field applies to GPP_C7.
27:26	-	-	**Reserved**
25:24	00b	RW	**Pad Ownership (PAD_OWN_GPPC_C_6)** Same description as bits [1:0], except that the bit field applies to GPP_C6.
23:22	-	-	**Reserved**
21:20	00b	RW	**Pad Ownership (PAD_OWN_GPPC_C_5)** Same description as bits [1:0], except that the bit field applies to GPP_C5.
19:18	-	-	**Reserved**
17:16	00b	RW	**Pad Ownership (PAD_OWN_GPPC_C_4)** Same description as bits [1:0], except that the bit field applies to GPP_C4.
15:14	-	-	**Reserved**
13:12	00b	RW	**Pad Ownership (PAD_OWN_GPPC_C_3)** Same description as bits [1:0], except that the bit field applies to GPP_C3.
11:10	-	-	**Reserved**
9:8	00b	RW	**Pad Ownership (PAD_OWN_GPPC_C_2)** Same description as bits [1:0], except that the bit field applies to GPP_C2.
7:6	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
5:4	00b	RW	**Pad Ownership (PAD_OWN_GPPC_C_1)** Same description as bits [1:0], except that the bit field applies to GPP_C1.
3:2	-	-	**Reserved**
1:0	00b	RW	**Pad Ownership (PAD_OWN_GPPC_C_0)** 00 = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIODriver) has ownership of the pad. In Host GPIO Driver Mode (refer toHOSTSW_OWN), GPIO input event update is limited to GPI_STS update only.Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STSand/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership 01 = ME GPIO Mode. ME has ownership of the pad. 10 = ISH GPIO Mode. ME has ownership of the pad 11 = Reserved

Pad Ownership (PAD_OWN_GPP_C_1) – Offset 24

Same description as PAD_OWN_GPP_C_0, except that this register is for GPP_C[15:8].

Pad Ownership (PAD_OWN_GPP_C_2) – Offset 28

Same description as PAD_OWN_GPP_C_0, except that this register is for GPP_C[23:16].

Pad Ownership (PAD_OWN_GPP_E_0) – Offset 2c

Same description as PAD_OWN_GPP_C_0, except that this register is for GPP_E[7:0].

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_21) – Offset 754

This register applies to GPP_C21 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 5Dh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_22) – Offset 760

This register applies to GPP_C22 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_22) – Offset 764

This register applies to GPP_C22 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 5Eh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_23) – Offset 770

This register applies to GPP_C23 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_23) – Offset 774

This register applies to GPP_C23 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 5Fh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_0) – Offset 780

This register applies to GPP_E0 and has the same description as PAD_CFG_DW0_GPP_C_0.

Exception: PMODE bit is RW/V bit.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_0) – Offset 784

This register applies to GPP_E0 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 18h

Pad Ownership (PAD_OWN_GPP_E_1) – Offset 30

Same description as PAD_OWN_GPP_C_0, except that this register is for GPP_E[15:8].

Pad Ownership (PAD_OWN_GPP_E_2) – Offset 34

Same description as PAD_OWN_GPP_C_0, except that this register is for GPP_E[23:16].

Pad Configuration Lock (PADCFGLOCK_GPP_C_0) – Offset 80

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_23)** Applied to GPP_C23. Same description as bit 0.
22	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_22)** Applied to GPP_C22. Same description as bit 0.
21	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_21)** Applied to GPP_C21. Same description as bit 0.
20	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_20)** Applied to GPP_C20. Same description as bit 0.
19	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_19)** Applied to GPP_C19. Same description as bit 0.
18	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_18)** Applied to GPP_C18. Same description as bit 0.
17	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_17)** Applied to GPP_C17. Same description as bit 0.
16	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_16)** Applied to GPP_C16. Same description as bit 0.
15	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_15)** Applied to GPP_C15. Same description as bit 0.
14	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_14)** Applied to GPP_C14. Same description as bit 0.
13	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_13)** Applied to GPP_C13. Same description as bit 0.
12	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_12)** Applied to GPP_C12. Same description as bit 0.
11	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_11)** Applied to GPP_C11. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
10	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_10)** Applied to GPP_C10. Same description as bit 0.
9	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_9)** Applied to GPP_C9. Same description as bit 0.
8	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_8)** Applied to GPP_C8. Same description as bit 0.
7	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_7)** Applied to GPP_C7. Same description as bit 0.
6	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_6)** Applied to GPP_C6. Same description as bit 0.
5	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_5)** Applied to GPP_C5. Same description as bit 0.
4	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_4)** Applied to GPP_C4. Same description as bit 0.
3	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_3)** Applied to GPP_C3. Same description as bit 0.
2	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_2)** Applied to GPP_C2. Same description as bit 0.
1	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_1)** Applied to GPP_C1. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**Pad Config Lock (PADCFGLOCK_GPPC_C_0)** Pad Configuration Lock locks specific register fields in the GPP specific registers from being configured. The registers affected become Read-Only and software writes to these registers have no effect. 0 = Unlock 1 = Lock the following register fields as read-only (RO): - Pad Configuration registers (exclude GPIOTXState) - GPI_NMI_EN Register (if implemented) - GPI_SMI_EN Register (if implemented) - GPI_GPE_EN Register (if implemented) When PadCfgLock is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_C_0) – Offset 84

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_23)** Applied to GPP_C23. Same description as PADCFGLOCKTX_GPP_C_0.
22	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_22)** Applied to GPP_C22. Same description as PADCFGLOCKTX_GPP_C_0.
21	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_21)** Applied to GPP_C21. Same description as PADCFGLOCKTX_GPP_C_0.
20	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_20)** Applied to GPP_C20. Same description as PADCFGLOCKTX_GPP_C_0.
19	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_19)** Applied to GPP_C19. Same description as PADCFGLOCKTX_GPP_C_0.

Bit Range	Default	Access	Field Name and Description
18	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_18)** Applied to GPP_C18. Same description as PADCFGLOCKTX_GPP_C_0.
17	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_17)** Applied to GPP_C17. Same description as PADCFGLOCKTX_GPP_C_0.
16	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_16)** Applied to GPP_C16. Same description as PADCFGLOCKTX_GPP_C_0.
15	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_15)** Applied to GPP_C15. Same description as PADCFGLOCKTX_GPP_C_0.
14	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_14)** Applied to GPP_C14. Same description as PADCFGLOCKTX_GPP_C_0.
13	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_13)** Applied to GPP_C13. Same description as PADCFGLOCKTX_GPP_C_0.
12	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_12)** Applied to GPP_C12. Same description as PADCFGLOCKTX_GPP_C_0.
11	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_11)** Applied to GPP_C11. Same description as PADCFGLOCKTX_GPP_C_0.
10	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_10)** Applied to GPP_C10. Same description as PADCFGLOCKTX_GPP_C_0.
9	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_9)** Applied to GPP_C9. Same description as PADCFGLOCKTX_GPP_C_0.
8	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_8)** Applied to GPP_C8. Same description as PADCFGLOCKTX_GPP_C_0.
7	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_7)** Applied to GPP_C7. Same description as PADCFGLOCKTX_GPP_C_0.
6	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_6)** Applied to GPP_C6. Same description as PADCFGLOCKTX_GPP_C_0.
5	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_5)** Applied to GPP_C5. Same description as PADCFGLOCKTX_GPP_C_0.

Bit Range	Default	Access	Field Name and Description
4	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_4)** Applied to GPP_C4. Same description as PADCFGLOCKTX_GPP_C_0.
3	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_3)** Applied to GPP_C3. Same description as PADCFGLOCKTX_GPP_C_0.
2	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_2)** Applied to GPP_C2. Same description as PADCFGLOCKTX_GPP_C_0.
1	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_1)** Applied to GPP_C1. Same description as PADCFGLOCKTX_GPP_C_0.
0	0b	RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_C_0)** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) When PadCfgLockTx is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

Pad Configuration Lock (PADCFGLOCK_GPP_E_0) – Offset 88

Same description as PADCFGLOCK_GPP_C_0 register, except this register applies to GPP_E[23:0].

Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_E_0) – Offset 8c

Same description as PADCFGLOCKTX_GPP_C_0 register, except this register applies to GPP_E[23:0].

Host Software Pad Ownership (HOSTSW_OWN_GPP_C_0) – Offset b0

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
23	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_23)** Applied to GPP_C23. Same description as bit 0.
22	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_22)** Applied to GPP_C22. Same description as bit 0.
21	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_21)** Applied to GPP_C21. Same description as bit 0.
20	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_20)** Applied to GPP_C20. Same description as bit 0.
19	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_19)** Applied to GPP_C19. Same description as bit 0.
18	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_18)** Applied to GPP_C18. Same description as bit 0.
17	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_17)** Applied to GPP_C17. Same description as bit 0.
16	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_16)** Applied to GPP_C16. Same description as bit 0.
15	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_15)** Applied to GPP_C15. Same description as bit 0.
14	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_14)** Applied to GPP_C14. Same description as bit 0.
13	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_13)** Applied to GPP_C13. Same description as bit 0.
12	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_12)** Applied to GPP_C12. Same description as bit 0.
11	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_11)** Applied to GPP_C11. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
10	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_10)** Applied to GPP_C10. Same description as bit 0.
9	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_9)** Applied to GPP_C9. Same description as bit 0.
8	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_8)** Applied to GPP_C8. Same description as bit 0.
7	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_7)** Applied to GPP_C7. Same description as bit 0.
6	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_6)** Applied to GPP_C6. Same description as bit 0.
5	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_5)** Applied to GPP_C5. Same description as bit 0.
4	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_4)** Applied to GPP_C4. Same description as bit 0.
3	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_3)** Applied to GPP_C3. Same description as bit 0.
2	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_2)** Applied to GPP_C2. Same description as bit 0.
1	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_1)** Applied to GPP_C1. Same description as bit 0.
0	0b	RW	**HostSW_Own (HOSTSW_OWN_GPPC_C_0)** This register determines the appropriate host status bit update when a pad is under host ownership. 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS,GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited toGPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updatesare masked.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_1) – Offset 790

This register applies to GPP_E1 and has the same description as PAD_CFG_DW0_GPP_C_0.

Exception: PMODE bit is RW/V bit.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_1) – Offset 794

This register applies to GPP_E1 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 19h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_2) – Offset 7a0

This register applies to GPP_E2 and has the same description as PAD_CFG_DW0_GPP_C_0.

Exception: PMODE bit is RW/V bit.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_2) – Offset 7a4

This register applies to GPP_E2 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 1Ah

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_3) – Offset 7b0

This register applies to GPP_E3 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_3) – Offset 7b4

This register applies to GPP_E3 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 1Bh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_4) – Offset 7c0

This register applies to GPP_E4 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_4) – Offset 7c4

This register applies to GPP_E4 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 1Ch

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_5) – Offset 7d0

This register applies to GPP_E5 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_5) – Offset 7d4

This register applies to GPP_E5 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 1Dh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_6) – Offset 7e0

This register applies to GPP_E6 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_6) – Offset 7e4

This register applies to GPP_E6 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 1Eh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_7) – Offset 7f0

This register applies to GPP_E7 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_7) – Offset 7f4

This register applies to GPP_E7 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 1Fh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_8) – Offset 800

This register applies to GPP_E8 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_8) – Offset 804

This register applies to GPP_E8 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 20h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_9) – Offset 810

This register applies to GPP_E9 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_9) – Offset 814

This register applies to GPP_E9 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 21h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_10) – Offset 820

This register applies to GPP_E10 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_10) – Offset 824

This register applies to GPP_E10 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 22h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_11) – Offset 830

This register applies to GPP_E11 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_11) – Offset 834

This register applies to GPP_E11 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 23h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_12) – Offset 840

This register applies to GPP_E12 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_12) – Offset 844

This register applies to GPP_E12 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 24h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_13) – Offset 850

This register applies to GPP_E13 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_13) – Offset 854

This register applies to GPP_E13 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 25h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_14) – Offset 860

This register applies to GPP_E14 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_14) – Offset 864

This register applies to GPP_E14 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 26h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_15) – Offset 870

This register applies to GPP_E15 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_15) – Offset 874

This register applies to GPP_E15 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 27h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_16) – Offset 880

This register applies to GPP_E16 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_16) – Offset 884

This register applies to GPP_E16 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 28h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_17) – Offset 890

This register applies to GPP_E17 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_17) – Offset 894

This register applies to GPP_E17 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 29h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_18) – Offset 8a0

This register applies to GPP_E18 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_18) – Offset 8a4

This register applies to GPP_E18 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 2Ah

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_19) – Offset 8b0

This register applies to GPP_E19 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_19) – Offset 8b4

This register applies to GPP_E19 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 2Bh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_20) – Offset 8c0

This register applies to GPP_E20 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_20) – Offset 8c4

This register applies to GPP_E20 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 2C

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_21) – Offset 8d0

This register applies to GPP_E21 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_21) – Offset 8d4

This register applies to GPP_E21 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 2Dh

Host Software Pad Ownership (HOSTSW_OWN_GPP_E_0) – Offset b4

Same description as HOSTSW_OWN_GPP_C_0 register, except that this register applies to GPP_E[23:0].

GPI Interrupt Status (GPI_IS_GPP_C_0) – Offset 100

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_23)** Applied to GPP_C23. Same description as bit 0.
22	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_22)** Applied to GPP_C22. Same description as bit 0.
21	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_21)** Applied to GPP_C21. Same description as bit 0.
20	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_20)** Applied to GPP_C20. Same description as bit 0.
19	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_19)** Applied to GPP_C19. Same description as bit 0.
18	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_18)** Applied to GPP_C18. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
17	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_17)** Applied to GPP_C17. Same description as bit 0.
16	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_16)** Applied to GPP_C16. Same description as bit 0.
15	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_15)** Applied to GPP_C15. Same description as bit 0.
14	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_14)** Applied to GPP_C14. Same description as bit 0.
13	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_13)** Applied to GPP_C13. Same description as bit 0.
12	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_12)** Applied to GPP_C12. Same description as bit 0.
11	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_11)** Applied to GPP_C11. Same description as bit 0.
10	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_10)** Applied to GPP_C10. Same description as bit 0.
9	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_9)** Applied to GPP_C9. Same description as bit 0.
8	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_8)** Applied to GPP_C8. Same description as bit 0.
7	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_7)** Applied to GPP_C7. Same description as bit 0.
6	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_6)** Applied to GPP_C6. Same description as bit 0.
5	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_5)** Applied to GPP_C5. Same description as bit 0.
4	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_4)** Applied to GPP_C4. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
3	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_3)** Applied to GPP_C3. Same description as bit 0.
2	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_2)** Applied to GPP_C2. Same description as bit 0.
1	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_1)** Applied to GPP_C1. Same description as bit 0.
0	0b	RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_C_0)** GPI Interrupt Status (GPI_INT_STS) This bit is set to '1' by hardware when either an edge or a level event isdetected (See RxEdCfg RxInv) on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode - HOSTSW_OWN = 1 (i.e. Host GPIO Driver Mode). Writing a value of 1 will clear the bit while writing a value of 0 has noeffect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x].

GPI Interrupt Status (GPI_IS_GPP_E_0) – Offset 104

Same description as GPI_IE_GPP_C_0 register, except that this register is for GPP_E[23:0].

GPI Interrupt Enable (GPI_IE_GPP_C_0) – Offset 120

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_23)** Applied to GPP_C23. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
22	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_22)** Applied to GPP_C22. Same description as bit 0.
21	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_21)** Applied to GPP_C21. Same description as bit 0.
20	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_20)** Applied to GPP_C20. Same description as bit 0.
19	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_19)** Applied to GPP_C19. Same description as bit 0.
18	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_18)** Applied to GPP_C18. Same description as bit 0.
17	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_17)** Applied to GPP_C17. Same description as bit 0.
16	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_16)** Applied to GPP_C16. Same description as bit 0.
15	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_15)** Applied to GPP_C15. Same description as bit 0.
14	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_14)** Applied to GPP_C14. Same description as bit 0.
13	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_13)** Applied to GPP_C13. Same description as bit 0.
12	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_12)** Applied to GPP_C12. Same description as bit 0.
11	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_11)** Applied to GPP_C11. Same description as bit 0.
10	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_10)** Applied to GPP_C10. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
9	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_9)** Applied to GPP_C9. Same description as bit 0.
8	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_8)** Applied to GPP_C8. Same description as bit 0.
7	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_7)** Applied to GPP_C7. Same description as bit 0.
6	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_6)** Applied to GPP_C6. Same description as bit 0.
5	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_5)** Applied to GPP_C5. Same description as bit 0.
4	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_4)** Applied to GPP_C4. Same description as bit 0.
3	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_3)** Applied to GPP_C3. Same description as bit 0.
2	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_2)** Applied to GPP_C2. Same description as bit 0.
1	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_1)** Applied to GPP_C1. Same description as bit 0.
0	0b	RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_C_0)** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation

GPI Interrupt Enable (GPI_IE_GPP_E_0) – Offset 124

Same description as GPI_IE_GPP_C_0 register, except that this register is for GPP_E[23:0].

GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_0) – Offset 140

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_23)** Applied to GPP_C23. Same description as bit 0.
22	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_22)** Applied to GPP_C22. Same description as bit 0.
21	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_21)** Applied to GPP_C21. Same description as bit 0.
20	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_20)** Applied to GPP_C20. Same description as bit 0.
19	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_19)** Applied to GPP_C19. Same description as bit 0.
18	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_18)** Applied to GPP_C18. Same description as bit 0.
17	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_17)** Applied to GPP_C17. Same description as bit 0.
16	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_16)** Applied to GPP_C16. Same description as bit 0.
15	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_15)** Applied to GPP_C15. Same description as bit 0.
14	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_14)** Applied to GPP_C14. Same description as bit 0.
13	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_13)** Applied to GPP_C13. Same description as bit 0.
12	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_12)** Applied to GPP_C12. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
11	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_11)** Applied to GPP_C11. Same description as bit 0.
10	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_10)** Applied to GPP_C10. Same description as bit 0.
9	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_9)** Applied to GPP_C9. Same description as bit 0.
8	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_8)** Applied to GPP_C8. Same description as bit 0.
7	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_7)** Applied to GPP_C7. Same description as bit 0.
6	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_6)** Applied to GPP_C6. Same description as bit 0.
5	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_5)** Applied to GPP_C5. Same description as bit 0.
4	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_4)** Applied to GPP_C4. Same description as bit 0.
3	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_3)** Applied to GPP_C3. Same description as bit 0.
2	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_2)** Applied to GPP_C2. Same description as bit 0.
1	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_1)** Applied to GPP_C1. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
0	0b	RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_C_0)** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high(or low if the corresponding RXINV bit is set). If the correspondingenable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: - If the system is in an S3-S5 state, the event will also wake the system. - If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIRoutSCI bit for thecorresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS.

GPI General Purpose Events Status (GPI_GPE_STS_GPP_E_0) – Offset 144

Same description as PI_GPE_STS_GPP_C_0 register, except that this is for GPP_E[23:0].

GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_0) – Offset 160

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_23)** Applied to GPP_C23. Same description as bit 0.
22	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_22)** Applied to GPP_C22. Same description as bit 0.
21	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_21)** Applied to GPP_C21. Same description as bit 0.
20	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_20)** Applied to GPP_C20. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
19	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_19)** Applied to GPP_C19. Same description as bit 0.
18	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_18)** Applied to GPP_C18. Same description as bit 0.
17	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_17)** Applied to GPP_C17. Same description as bit 0.
16	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_16)** Applied to GPP_C16. Same description as bit 0.
15	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_15)** Applied to GPP_C15. Same description as bit 0.
14	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_14)** Applied to GPP_C14. Same description as bit 0.
13	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_13)** Applied to GPP_C13. Same description as bit 0.
12	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_12)** Applied to GPP_C12. Same description as bit 0.
11	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_11)** Applied to GPP_C11. Same description as bit 0.
10	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_10)** Applied to GPP_C10. Same description as bit 0.
9	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_9)** Applied to GPP_C9. Same description as bit 0.
8	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_8)** Applied to GPP_C8. Same description as bit 0.
7	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_7)** Applied to GPP_C7. Same description as bit 0.
6	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_6)** Applied to GPP_C6. Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
5	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_5)** Applied to GPP_C5. Same description as bit 0.
4	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_4)** Applied to GPP_C4. Same description as bit 0.
3	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_3)** Applied to GPP_C3. Same description as bit 0.
2	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_2)** Applied to GPP_C2. Same description as bit 0.
1	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_1)** Applied to GPP_C1. Same description as bit 0.
0	0b	RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_C_0)** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note:The pad must also be routed for GPE functionality in order for GPE tobe generated, i.e. the corresponding GPIRoutSCI must be set to '1'.

GPI General Purpose Events Enable (GPI_GPE_EN_GPP_E_0) – Offset 164

Same description as GPI_GPE_EN_GPP_C_0 register, except that this is for GPP_E[23:0].

SMI Status (GPI_SMI_STS_GPP_C_0) – Offset 180

Register bits in this register are implemented for GPP_C signals that have SMI capability only. Other bits are reserved and RO.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
23	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_C_23)** Same description as bit 22.
22	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_C_22)** This bit is set to 1 by hardware when a level event (See RxEdCfg,RxInv) is detected, and all the following conditions are true: - The corresponding pad is used in GPIO input mode - The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if theGPI_SMI_ STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of 1 will clear the bit while writing a value of 0 has noeffect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN does not prevent the setting of GPI_SMI_STS. Defaults for these bits are dependent on the state of the GPI pads.
21:0	-	-	**Reserved**

SMI Status (GPI_SMI_STS_GPP_E_0) – Offset 184

Register bits in this register are implemented for GPP_E signals that have SMI capability only. Other bits are reserved and RO.

Bit Range	Default	Access	Field Name and Description
30:17	-	-	**Reserved**
16	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_16)** Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
15	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_15)** Same description as bit 0.
14	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_14)** Same description as bit 0.
13	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_13)** Same description as bit 0.
12:9	-	-	**Reserved**
8	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_8)** Same description as bit 0.
7	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_7)** Same description as bit 0.
6	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_6)** Same description as bit 0.
5	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_5)** Same description as bit 0.
4	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_4)** Same description as bit 0.
3	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_3)** Same description as bit 0.
2	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_2)** Same description as bit 0.
1	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_1)** Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
0	0b	RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_0)** This bit is set to 1 by hardware when a level event (See RxEdCfg,RxInv) is detected, and all the following conditions are true: - The corresponding pad is used in GPIO input mode - The corresponding PAD_OWN[2:0] is '000' (i.e. ACPI GPIO Mode). If the following conditions are true, then an SMI will be generated if theGPI_SMI_STS bit is set: 1. The corresponding bit in the GPI_SMI_EN register is set 2. The corresponding pad's GPIROUTSMI is set Writing a value of 1 will clear the bit while writing a value of 0 has noeffect. 0 = There is no SMI event 1 = There is an SMI event The state of GPI_SMI_EN does not prevent the setting of GPI_SMI_STS. Defaults for these bits are dependent on the state of the GPI pads.

NMI Status (GPI_NMI_STS_GPP_C_0) – Offset 1c0

Register bits in this register are implemented for GPP_C signals that have NMI capability only. Other bits are reserved and RO.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
23	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_C_23)** Same description as bit 22.
22	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_C_22)** This bit is set to 1 by hardware when an edge event is detected (SeeRxEdCfg, RxInv) on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode (PMode) - The corresponding GPIONMIRout is set to 1, i.e. programmed toroute as NMI - The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). - The corresponding GPI_NMI_EN is set Writing a value of 1 will clear the bit while writing a value of 0 has noeffect. 0 = There is no NMI event 1 = There is an NMI event
21:0	-	-	**Reserved**

NMI Status (GPI_NMI_STS_GPP_E_0) – Offset 1c4

Register bits in this register are implemented for GPP_E signals that have NMI capability only. Other bits are reserved and RO.

Bit Range	Default	Access	Field Name and Description
30:17	-	-	**Reserved**
16	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_16)** Same description as bit 0.
15	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_15)** Same description as bit 0.
14	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_14)** Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
13	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_13)** Same description as bit 0.
12:9	-	-	**Reserved**
8	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_8)** Same description as bit 0.
7	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_7)** Same description as bit 0.
6	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_6)** Same description as bit 0.
5	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_5)** Same description as bit 0.
4	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_4)** Same description as bit 0.
3	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_3)** Same description as bit 0.
2	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_2)** Same description as bit 0.
1	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_1)** Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
0	0b	RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_0)** This bit is set to 1 by hardware when an edge event is detected (SeeRxEdCfg, RxInv) on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode (PMode) - The corresponding GPIONMIRout is set to 1, i.e. programmed toroute as NMI - The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). - The corresponding GPI_NMI_EN is set Writing a value of 1 will clear the bit while writing a value of 0 has noeffect. 0 = There is no NMI event 1 = There is an NMI event

NMI Enable (GPI_NMI_EN_GPP_C_0) – Offset 1e0

Register bits in this register are implemented for GPP_C signals that have NMI capability only. Other bits are reserved and RO.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_23)** Same description as bit 22.
22	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_22)** This bit is used to enable/disable the generation of NMI when thecorresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configurationregister PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 ofthis bit is locked down to read-only.
21:0	-	-	**Reserved**

NMI Enable (GPI_NMI_EN_GPP_E_0) – Offset 1e4

Register bits in this register are implemented for GPP_E signals that have NMI capability only. Other bits are reserved and RO.

Bit Range	Default	Access	Field Name and Description
30:17	-	-	**Reserved**
16	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_16)** Same description as bit 0.
15	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_15)** Same description as bit 0.
14	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_14)** Same description as bit 0.
13	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_13)** Same description as bit 0.
12:9	-	-	**Reserved**
8	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_8)** Same description as bit 0.
7	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_7)** Same description as bit 0.
6	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_6)** Same description as bit 0.
5	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_5)** Same description as bit 0.
4	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_4)** Same description as bit 0.
3	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_3)** Same description as bit 0.

Bit Range	Default	Access	Field Name and Description
2	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_2)** Same description as bit 0.
1	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_1)** Same description as bit 0.
0	0b	RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_0)** This bit is used to enable/disable the generation of NMI when thecorresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configurationregister PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 ofthis bit is locked down to read-only.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_0) – Offset 600

This register applies to GPP_C0.

Bit Range	Default	Access	Field Name and Description
31:30	01b	RW	**Pad Reset Config (PADRSTCFG)** This register controls which reset is used to reset GPIO pad register fields in PAD_CFG_DW0 and PAD_CFG_DW1 registers. This register can be used for Sx isolation of the associated signal if needed. 00 = RSMRST# 01 = Host deep reset. This reset occurs when any of the following occur: Host reset (with or without power cycle) is initiated, Global reset is initiated, or Deep Sx entry. This reset does NOT occur as part of S3/S4/S5 entry. 10 = PLTRST# 11 = Reserved

Bit Range	Default	Access	Field Name and Description
29	0b	RW	**RX Pad State Select (RXPADSTSEL)** Determines from which node the RX pad state for native function should be taken from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from RX buffer 1 = Internal RX pad state (subject to RXINV and PreGfRXSel settings)
28	0b	RW	**RX Raw Override to '1' (RXRAW1)** This bit determines if the selected pad state is being overridden to '1'. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	-	-	**Reserved**
26:25	10b	RW	**RX Level/Edge Configuration (RXEVCFG)** Determines if the internal RX pad state (synchronized, filtered vs non-filtered version as determined by PreGfRXSel, and is further subject to RXInv) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller . 0h = Level 1h = Edge (RxInv=0 for rising edge; 1 for falling edge) 2h = Disable 3h = Either rising edge or falling edge
24	0b	RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL)** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV

Bit Range	Default	Access	Field Name and Description
23	0b	RW	**RX Invert (RXINV)** This bit determines if the selected pad state should go through the polarity inversion stage. This field is only applicable when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	00b	RW	**RX/TX Enable Config (RXTXENCFG)** This controls the RX and TX buffer enablement for the function selected by Pad Mode. This field is not applicable in GPIO mode (PMode = 0. 0h = Function defined in Pad Mode controls TX and RX enablement 1h = Function controls TX enablement and RX is disabled with 0 being driven internally 2h = Function controls TX enablement and RX is disabled with 1 being driven internally 3h = Function controls TX enablement and RX is always enabled

Bit Range	Default	Access	Field Name and Description
20	0b	RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC)** Determines if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0b	RW	**GPIO Input Route SCI (GPIROUTSCI)** Determines if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI. 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s).
18	0b	RO	**GPIO Input Route SMI (GPIROUTSMI)** Determines if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s). This bit only applies to a GPIO that has SMI capability. Otherwise, the bit is RO.
17	0b	RO	**GPIO Input Route NMI (GPIROUTNMI)** Determines if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit. This bit only applies to a GPIO that has NMI capability. Otherwise, the bit is RO.

Bit Range	Default	Access	Field Name and Description
16:11	-	-	**Reserved**
10	See Description	RW	**Pad Mode (PMODE)** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO control the Pad. 1h = native function 1, if applicable, controls the Pad Dedicated (unmuxed) GPIO shall report RO of all 0's in this register field If GPIO vs. native mode is configured via soft strap, this bit has no effect. Default value is determined by the default functionality of the pad.
9	1b	RW	**GPIO RX Disable (GPIORXDIS)** 0 = Enable the input buffer (active low enable) of the pad. 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0'.
8	1b	RW	**GPIO TX Disable (GPIOTXDIS)** 0 = Enable the output buffer (active low enable) of the pad. 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	-	-	**Reserved**
1		RO/V	**GPIO RX State (GPIORXSTATE)** This is the current internal RX pad state after Glitch Filter logic stage and hardware debouncer (if any) and is not affected by PMode and RXINV settings.
0	0b	RW	**GPIO TX State (GPIOTXSTATE)** 0 = Drive a level '0' to the TX output pad. 1 = Drive a level '1' to the TX output pad.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_0) – Offset 604

This register applies to GPP_C0.

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13:10	See Description	RW	**Termination (TERM)** The Pad Termination state defines the different weak internal pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. Others: Reserved NOTES: 1. The internal 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily.
9:8	-	-	**Reserved**
7:0	48h	RO	**Interrupt Select (INTSEL)** The Interrupt Select defines which interrupt line driven from the GPIO Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 .... Up to the max IOxAPIC IRQ supported.

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_1) – Offset 610

This register applies to GPP_C1 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_1) – Offset 614

This register applies to GPP_C1 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 49h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_2) – Offset 620

This register applies to GPP_C2 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_2) – Offset 624

This register applies to GPP_C2 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 4Ah

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_3) – Offset 630

This register applies to GPP_C3 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_3) – Offset 634

This register applies to GPP_C3 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default:4Bh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_4) – Offset 640

This register applies to GPP_C4 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_4) – Offset 644

This register applies to GPP_C4 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 4Ch

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_5) – Offset 650

This register applies to GPP_C5 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_5) – Offset 654

This register applies to GPP_C5 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 4Dh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_6) – Offset 660

This register applies to GPP_C6 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_6) – Offset 664

This register applies to GPP_C6 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 4Eh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_7) – Offset 670

This register applies to GPP_C7 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_7) – Offset 674

This register applies to GPP_C7 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 4Fh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_8) – Offset 680

This register applies to GPP_C8 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_8) – Offset 684

This register applies to GPP_C8 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 50h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_9) – Offset 690

This register applies to GPP_C9 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_9) – Offset 694

This register applies to GPP_C9 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 51h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_10) – Offset 6a0

This register applies to GPP_C10 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_10) – Offset 6a4

This register applies to GPP_C10 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 52h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_11) – Offset 6b0

This register applies to GPP_C11 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_11) – Offset 6b4

This register applies to GPP_C11 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 53h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_12) – Offset 6c0

This register applies to GPP_C12 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_12) – Offset 6c4

This register applies to GPP_C12 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 54h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_13) – Offset 6d0

This register applies to GPP_C13 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_13) – Offset 6d4

This register applies to GPP_C13 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 55h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_14) – Offset 6e0

This register applies to GPP_C14 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_14) – Offset 6e4

This register applies to GPP_C14 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 56h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_15) – Offset 6f0

This register applies to GPP_C15 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_15) – Offset 6f4

This register applies to GPP_C15 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 57h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_16) – Offset 700

This register applies to GPP_C16 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_16) – Offset 704

This register applies to GPP_C16 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 58h

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_22) – Offset 8e0

This register applies to GPP_E22 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_22) – Offset 8e4

This register applies to GPP_E22 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 2Eh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_23) – Offset 8f0

This register applies to GPP_E23 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_23) – Offset 8f4

This register applies to GPP_E23 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 2Fh

Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_17) – Offset 710

This register applies to GPP_C17 and has the same description as PAD_CFG_DW0_GPP_C_0.

Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_17) – Offset 714

This register applies to GPP_C17 and has the same description as PAD_CFG_DW1_GPP_C_0.

Exception:

INTSEL bit field default: 59h

GSPI PCI Configuration Registers

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID and Vendor ID (DEVVENDID)	XXXX8086h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4h	4	Status and Command (STATUSCOMMAND)	100000h
8h	4	Revision ID and Class Code (REVCLASSCODE)	C8000XXh
ch	4	Cache Line Latency Header and BIST (CLLATHEADERBIST)	800000h
10h	4	Base Address (BAR)	4h
14h	4	Base Address High (BAR_HIGH)	0h
18h	4	Base Address 1 (BAR1)	4h
1ch	4	Base Address 1 High (BAR1_HIGH)	0h
2ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)	0h
34h	4	Capabilities Pointer (CAPABILITYPTR)	80h
3ch	4	Interrupt (INTERRUPTREG)	100h
80h	4	Power Management Capability ID (POWERCAPID)	39001h
84h	4	Power Management Control and Status (PMECTRLSTATUS)	8h
90h	4	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)	F0140009h
98h	4	SW LTR Update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)	2101h
9ch	4	Device IDLE Pointer (DEVICE_IDLE_POINTER_REG)	24C1h
a0h	4	Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)	70800h
b0h	4	General Purpose Read Write 1 (GEN_REGRW1)	0h
b4h	4	General Purpose Read Write 2 (GEN_REGRW2)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
b8h	4	General Purpose Read Write 3 (GEN_REGRW3)	0h
bch	4	General Purpose Read Write 4 (GEN_REGRW4)	0h
c0h	4	General Purpose Input (GEN_INPUT_REG)	0h

Device ID and Vendor ID (DEVVENDID) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:16	See Description	RO	**Device Identification (DEVICEID)** This is a 16-bit value assigned to the controller. See the Device and Revision ID Table in Volume 1 for the default value.
15:0	8086h	RO	**Vendor ID (VENDORID)** Identifies the manufacturer of the device. 8086h = Intel.

Status and Command (STATUSCOMMAND) – Offset 4

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29	0h	RW/1C	**Received Master Abort (RMA)** S/W writes a '1' to this bit to clear it.
28	0h	RW/1C	**Received Target Abort (RTA)** S/W writes a '1' to this bit to clear it.
27:21	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
20	1h	RO	**Capabilities List (CAPLIST)** Indicates that the controller contains a capabilities pointer list.
19	0h	RO	**Interrupt Status (INTR_STATUS)** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit is a 0 and this Interrupt Status bit is a 1, will the device's/function's interrupt message be sent. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:11	-	-	**Reserved**
10	0h	RW	**Interrupt Disable (INTR_DISABLE)** Setting this bit disables INTx assertion. The interrupt disabled is legacy INTx# interrupt. This bit has no connection with interrupt status bit.
9	-	-	**Reserved**
8	0h	RW	**SERR Enable (SERR_ENABLE)** Not implemented.
7:3	-	-	**Reserved**
2	0h	RW	**Bus Master Enable (BME)** If this bit is 0, the controller does not generate any new upstream transaction as a master.
1	0h	RW	**Memory Space Enable (MSE)** 0 = Disables memory mapped Configuration space. 1 = Enables memory mapped Configuration space.
0	-	-	**Reserved**

Revision ID and Class Code (REVCLASSCODE) – Offset 8

Bit Range	Default	Access	Field Name and Description
31:8	0C8000h	RO	**Class Codes (CLASS_CODES)** Class Code register is read-only and is used to identify the generic function of the device, and in some cases, a specific register-level programming interface
7:0	See Description	RO	**Revision ID (RID)** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

Cache Line Latency Header and BIST (CLLATHEADERBIST) – Offset c

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	1b	RO	**Multi Function Device (MULFNDEV)** 0 = Single Function Device 1 = Multi Function device.
22:16	00h	RO	**Header Type (HEADERTYPE)** Implements Type 0 Configuration header.
15:8	00h	RO	**Latency Timer (LATTIMER)** Hardwired to 0.
7:0	00h	RW	**Cache Line Size (CACHELINE_SIZE)**

Base Address (BAR) – Offset 10

Bit Range	Default	Access	Field Name and Description
31:12	00000h	RW	**Base Address (BASEADDR)** Provides system memory base address for the controller.

Bit Range	Default	Access	Field Name and Description
11:4	00h	RO	**Size Indicator (SIZEINDICATOR)** Always returns 0. The size of this register depends on the size of the memory space.
3	0h	RO	**Prefetchable (PREFETCHABLE)** 0 indicates that this BAR is not prefetchable.
2:1	10b	RO	**Type (TYPE)** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range, If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h	RO	**Memory Space Indicator (MESSAGE_SPACE)** 0 indicates this BAR is present in the memory space.

Base Address High (BAR_HIGH) – Offset 14

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Base Address High (BASEADDR_HIGH)**

Base Address 1 (BAR1) – Offset 18

Bit Range	Default	Access	Field Name and Description
31:12	00000h	RW	**Base Address (BASEADDR1)** This field is present if BAR1 is enabled.
11:4	00h	RO	**Size Indicator (SIZEINDICATOR1)** Always is 0 as minimum size is 4K
3	0h	RO	**Prefetchable (PREFETCHABLE1)** 0 indicates that this BAR is not prefetchable.
2:1	2h	RO	**Type (TYPE1)** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range

Bit Range	Default	Access	Field Name and Description
0	0h	RO	**Memory Space Indicator (MESSAGE_SPACE1)** 0 Indicates this BAR is present in the memory space.

Base Address 1 High (BAR1_HIGH) – Offset 1c

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Base Address High (BASEADDR1_HIGH)**

Subsystem Vendor and Subsystem ID (SUBSYSTEMID) – Offset 2c

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/O	**Subsystem ID (SUBSYSTEMID)** The register, in combinationwith the Subsystem Vendor ID register make it possible for theoperating environment to distinguish one subsystem from theother. This register is a Read Write Once type register.
15:0	0000h	RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID)** The register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from theother. This register is a Read Write Once register.

Capabilities Pointer (CAPABILITYPTR) – Offset 34

Capabilities Pointer register indicates what the next capability is

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	80h	RO	**Capabilities Pointer (CAPPTR_POWER)** Indicates what the next capability is.

Interrupt (INTERRUPTREG) – Offset 3c

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO	**Max Latency (MAX_LAT)** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h	RO	**Min Latency (MIN_GNT)** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	-	-	**Reserved**
11:8	1h	RO	**Interrupt Pin (INTPIN)**
7:0	00h	RW	**Interrupt Line (INTLINE)** It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

Power Management Capability ID (POWERCAPID) – Offset 80

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:27	00h	RO	**PME Support (PMESUPPORT)** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for for a bit indicates that the function is not capable of asserting the PME# signal while in that power state. Bit 27 = 1: PME# can be asserted from D0. Bit 30 = 1: PME# can be asserted from D3 hot. Other bits are not used.
26:19	-	-	**Reserved**
18:16	3h	RO	**Version (VERSION)** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h	RO	**Next Capability (NXTCAP)** Points to the next capability structure.
7:0	01h	RO	**Power Management Capability (POWER_CAP)** Indicates power management capability.

Power Management Control and Status (PMECTRLSTATUS) – Offset 84

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
15	0h	RW/1C	**PME Status (PMESTATUS)**
14:9	-	-	**Reserved**
8	0h	RW	**PME Enable (PMEENABLE)** 0 = PME message is disabled 1 = PME message is enabled.
7:4	-	-	**Reserved**
3	1h	RO	**No Soft Reset (NO_SOFT_RESET)** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	-	-	**Reserved**
1:0	0h	RW	**Power State (POWERSTATE)** This field is used both todetermine the current power state and to set a new power state.The values are:00 = D0 state11 = D3HOT stateOthers = ReservedNotes: If software attempts to write a value of 01b or 10b in to this field,the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked.

PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD) – Offset 90

Bit Range	Default	Access	Field Name and Description
31:28	0Fh	RO	**Vendor Capability (VEND_CAP)** Vendor Specific Capability ID
27:24	0h	RO	**Revision ID (REVID)** Revision ID of capability structure
23:16	14h	RO	**Capability Length (CAP_LENGTH)** Vendor Specific Capability Length

Bit Range	Default	Access	Field Name and Description
15:8	00h	RO	**Next Capability (NEXT_CAP)** Points to the next capabilitystructure. This points to NULL.
7:0	09h	RO	**Capability ID (CAPID)**

SW LTR Update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG) – Offset 98

Software location pointer in MMIO space as an offset specified by BAR

Bit Range	Default	Access	Field Name and Description
31:4	0000210h	RO	**Location Pointer Offset (SW_LAT_DWORD_OFFSET)** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h	RO	**Bar Number (SW_LAT_BAR_NUM)** Indicates that the SW LTR update MMIO location is always at BAR0
0	1h	RO	**Valid (SW_LAT_VALID)**

Device IDLE Pointer (DEVICE_IDLE_POINTER_REG) – Offset 9c

Device IDLE pointer register giving details on Device MMIO offset location , BAR NUM and D0i3 Valid Strap

Bit Range	Default	Access	Field Name and Description
31:4	000024Ch	RO	**Device Idle Pointer (DWORD_OFFSET)** contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR
3:1	0h	RO	**BAR Number (BAR_NUM)** Indicates that the D0i3 MMIO location is always at BAR0.

Bit Range	Default	Access	Field Name and Description
0	1h	RO	**Valid (VALID)** 0 = Not valid 1 = Valid

Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG) – Offset a0

Bit Range	Default	Access	Field Name and Description
30:19	-	-	**Reserved**
18	1b	RW	**Power Gate Enable (PGE)** If clear, the controller will never request a PG. If 1, then the function will power gate when idle and the DevIdle bit is set.
17	1b	RW	**D3-Hot Enable (I3_ENABLE)** If 1, then function will power gate when idle and the POWERSTATE bits in the function = 11 (D3).
16	1b	RW	**PMC Request Enable (PMCRE)** If this bit is set to '1', thefunction will power gate when idle.
15:13	-	-	**Reserved**
12:10	2h	RW/O	**Power On Latency Scale (POW_LAT_SCALE)** This value is written by BIOS to communicate to the Driver.
9:0	000h	RW/O	**Power On Latency Value (POW_LAT_VALUE)** This value is written by BIOS to communicate to the Driver.

General Purpose Read Write 1 (GEN_REGRW1) – Offset b0

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**General Purpose Read Write (GEN_REG_RW1)** General purpose read write PCI register.

General Purpose Read Write 2 (GEN_REGRW2) – Offset b4

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**General Purpose Read Write (GEN_REG_RW2)** General purpose read write PCI register.

General Purpose Read Write 3 (GEN_REGRW3) – Offset b8

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**General Purpose Read Write (GEN_REG_RW3)** General purpose read write PCI register.

General Purpose Read Write 4 (GEN_REGRW4) – Offset bc

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**(GEN_REG_RW4)** General purpose read write PCI register.

General Purpose Input (GEN_INPUT_REG) – Offset c0

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO	**General Purpose Input (GEN_REG_INPUT_RW)** General purpose input register.

High Definition Audio (D31:F3) Memory Mapped I/O Registers

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	Global Capabilities (GCAP)	9701h
2h	1	Minor Version (VMIN)	0h
3h	1	Major Version (VMAJ)	1h
4h	2	Output Payload Capability (OUTPAY)	0h
6h	2	Input Payload Capability (INPAY)	0h
8h	4	Global Control (GCTL)	0h
ch	2	Wake Enable (WAKEEN)	0h
800h	4	Processing Pipe Capability Header (PPCH)	30500h
804h	4	Processing Pipe Control (PPCTL)	0h
808h	4	Processing Pipe Status (PPSTS)	0h
810h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC0LLPL)	0h
814h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC0LLPU)	0h
818h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC0LDPL)	0h
eh	2	Wake Status (WAKESTS)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
10h	2	Global Status (GSTS)	0h
12h	2	Global Capabilities 2 (GCAP2)	1h
14h	2	Linked List Capabilities Header (LLCH)	C00h
18h	2	Output Stream Payload Capability (OUTSTRMPAY)	30h
1ah	2	Input Stream Payload Capability (INSTRMPAY)	18h
20h	4	Interrupt Control (INTCTL)	0h
24h	4	Interrupt Status (INTSTS)	0h
30h	4	Wall Clock Counter (WALCLK)	0h
38h	4	Stream Synchronization (SSYNC)	0h
81ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC0LDPU)	0h
820h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC1LLPL)	0h
824h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC1LLPU)	0h
828h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC1LDPL)	0h
82ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC1LDPU)	0h
830h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC2LLPL)	0h
834h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC2LLPU)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40h	4	CORB Lower Base Address (CORBLBASE)	0h
44h	4	CORB Upper Base Address (CORBUBASE)	0h
48h	2	CORB Write Pointer (CORBWP)	0h
4ah	2	CORB Read Pointer (CORBRP)	0h
4ch	1	CORB Control (CORBCTL)	0h
4dh	1	CORB Status (CORBSTS)	0h
4eh	1	CORB Size (CORBSIZE)	42h
50h	4	RIRB Lower Base Address (RIRBLBASE)	0h
54h	4	RIRB Upper Base Address (RIRBUBASE)	0h
58h	2	RIRB Write Pointer (RIRBWP)	0h
5ah	2	Response Interrupt Count (RINTCNT)	0h
5ch	1	RIRB Control (RIRBCTL)	0h
5dh	1	RIRB Status (RIRBSTS)	0h
5eh	1	RIRB Size (RIRBSIZE)	42h
60h	4	Immediate Command (IC)	0h
64h	4	Immediate Response (IR)	0h
68h	2	Immediate Command Status (ICS)	0h
70h	4	DMA Position Lower Base Address (DPLBASE)	0h
74h	4	DMA Position Upper Base Address (DPUBASE)	0h
80h	4	Input/Output Stream Descriptor x Control (ISD0CTL)	40000h
83h	1	Input/Output Stream Descriptor x Status (ISD0STS)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
84h	4	Input/Output Stream Descriptor x Link Position in Buffer (ISD0LPIB)	0h
88h	4	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD0CBL)	0h
8ch	2	Input/Output Stream Descriptor x Last Valid Index (ISD0LVI)	0h
8eh	2	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD0FIFOW)	4h
90h	2	Input/Output Stream Descriptor x FIFO Size (ISD0FIFOS)	0h
92h	2	Input/Output Stream Descriptor x Format (ISD0FMT)	0h
94h	2	Input/Output Stream Descriptor x FIFO Limit (ISD0FIFOL)	0h
98h	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD0BDLPLBA)	0h
9ch	4	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD0BDLPUBA)	0h
904h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC8LLPU)	0h
908h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC8LDPL)	0h
90ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC8LDPU)	0h
910h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC0CTL)	0h
914h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC0FMT)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
918h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC0LLPL)	0h
91ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC0LLPU)	0h
920h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC1CTL)	0h
924h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC1FMT)	0h
928h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC1LLPL)	0h
92ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC1LLPU)	0h
930h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC2CTL)	0h
934h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC2FMT)	0h
938h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC2LLPL)	0h
93ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC2LLPU)	0h
940h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC3CTL)	0h
944h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC3FMT)	0h
948h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC3LLPL)	0h
94ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC3LLPU)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
950h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC4CTL)	0h
954h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC4FMT)	0h
838h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC2LDPL)	0h
83ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC2LDPU)	0h
840h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC3LLPL)	0h
844h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC3LLPU)	0h
848h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC3LDPL)	0h
84ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC3LDPU)	0h
850h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC4LLPL)	0h
958h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC4LLPL)	0h
95ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC4LLPU)	0h
960h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC5CTL)	0h
964h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC5FMT)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
968h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC5LLPL)	0h
96ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC5LLPU)	0h
970h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC6CTL)	0h
854h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC4LLPU)	0h
858h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC4LDPL)	0h
85ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC4LDPU)	0h
860h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC5LLPL)	0h
864h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC5LLPU)	0h
868h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC5LDPL)	0h
86ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC5LDPU)	0h
974h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC6FMT)	0h
978h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC6LLPL)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
97ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC6LLPU)	0h
980h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC0CTL)	0h
984h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC0FMT)	0h
988h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC0LLPL)	0h
98ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC0LLPU)	0h
990h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC1CTL)	0h
994h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC1FMT)	0h
998h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC1LLPL)	0h
99ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC1LLPU)	0h
9a0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC2CTL)	0h
9a4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC2FMT)	0h
9a8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC2LLPL)	0h
9ach	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC2LLPU)	0h
9b0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC3CTL)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
9b4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC3FMT)	0h
9b8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC3LLPL)	0h
9bch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC3LLPU)	0h
9c0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC4CTL)	0h
9c4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC4FMT)	0h
9c8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC4LLPL)	0h
9cch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC4LLPU)	0h
9d0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC5CTL)	0h
9d4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC5FMT)	0h
9d8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC5LLPL)	0h
9dch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC5LLPU)	0h
9e0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC6CTL)	0h
9e4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC6FMT)	0h
9e8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC6LLPL)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
9ech	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC6LLPU)	0h
9f0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC7CTL)	0h
9f4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC7FMT)	0h
9f8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC7LLPL)	0h
9fch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC7LLPU)	0h
a00h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC8CTL)	0h
a04h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC8FMT)	0h
a08h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC8LLPL)	0h
a0ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC8LLPU)	0h
4a10h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC7LLPL)	0h
4a14h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC7LLPU)	0h
4a18h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC7LDPL)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
870h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC6LLPL)	0h
874h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC6LLPU)	0h
878h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC6LDPL)	0h
87ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC6LDPU)	0h
880h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC0LLPL)	0h
884h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC0LLPU)	0h
888h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC0LDPL)	0h
4a1ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC7LDPU)	0h
4a20h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC8LLPL)	0h
4a24h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC8LLPU)	0h
4a28h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC8LDPL)	0h
4a2ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC8LDPU)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4a30h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC9LLPL)	0h
4a34h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC9LLPU)	0h
88ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC0LDPU)	0h
890h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC1LLPL)	0h
894h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC1LLPU)	0h
898h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC1LDPL)	0h
89ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC1LDPU)	0h
8a0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC2LLPL)	0h
8a4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC2LLPU)	0h
4a38h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC9LDPL)	0h
4a3ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC9LDPU)	0h
4a40h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC10LLPL)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4a44h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC10LLPU)	0h
4a48h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC10LDPL)	0h
4a4ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC10LDPU)	0h
4a50h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC11LLPL)	0h
4a54h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC11LLPU)	0h
4a58h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC11LDPL)	0h
4a5ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC11LDPU)	0h
4a60h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC12LLPL)	0h
4a64h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC12LLPU)	0h
4a68h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC12LDPL)	0h
4a6ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC12LDPU)	0h
4a70h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC13LLPL)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4a74h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC13LLPU)	0h
4a78h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC13LDPL)	0h
4a7ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC13LDPU)	0h
4a80h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC14LLPL)	0h
4a84h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC14LLPU)	0h
4a88h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC14LDPL)	0h
4a8ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC14LDPU)	0h
4a90h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC9LLPL)	0h
4a94h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC9LLPU)	0h
4a98h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC9LDPL)	0h
4a9ch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC9LDPU)	0h
4aa0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC10LLPL)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4aa4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC10LLPU)	0h
4aa8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC10LDPL)	0h
4aach	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC10LDPU)	0h
4ab0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC11LLPL)	0h
4ab4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC11LLPU)	0h
4ab8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC11LDPL)	0h
4abch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC11LDPU)	0h
4ac0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC12LLPL)	0h
4ac4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC12LLPU)	0h
4ac8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC12LDPL)	0h
4acch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC12LDPU)	0h
4ad0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC13LLPL)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4ad4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC13LLPU)	0h
4ad8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC13LDPL)	0h
4adch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC13LDPU)	0h
4ae0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC14LLPL)	0h
4ae4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC14LLPU)	0h
4ae8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC14LDPL)	0h
4aech	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC14LDPU)	0h
4af0h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC7CTL)	0h
4af4h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC7FMT)	0h
4af8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC7LLPL)	0h
4afch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC7LLPU)	0h
4b00h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC8CTL)	0h
4b04h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC8FMT)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4b08h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC8LLPL)	0h
4b0ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC8LLPU)	0h
4b10h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC9CTL)	0h
4b14h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC9FMT)	0h
4b18h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC9LLPL)	0h
4b1ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC9LLPU)	0h
4b20h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC10CTL)	0h
4b24h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC10FMT)	0h
4b28h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC10LLPL)	0h
4b2ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC10LLPU)	0h
4b30h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC11CTL)	0h
4b34h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC11FMT)	0h
4b38h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC11LLPL)	0h
4b3ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC11LLPU)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4b40h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC12CTL)	0h
4b44h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC12FMT)	0h
4b48h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC12LLPL)	0h
4b4ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC12LLPU)	0h
4b50h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC13CTL)	0h
4b54h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC13FMT)	0h
4b58h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC13LLPL)	0h
4b5ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC13LLPU)	0h
4b60h	4	Input/Output Processing Pipe's Link Connection x Control (IPPLC14CTL)	0h
4b64h	2	Input/Output Processing Pipe's Link Connection x Format (IPPLC14FMT)	0h
4b68h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC14LLPL)	0h
4b6ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC14LLPU)	0h
4b70h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC9CTL)	0h
4b74h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC9FMT)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4b78h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC9LLPL)	0h
4b7ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC9LLPU)	0h
4b80h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC10CTL)	0h
4b84h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC10FMT)	0h
4b88h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC10LLPL)	0h
4b8ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC10LLPU)	0h
4b90h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC11CTL)	0h
4b94h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC11FMT)	0h
4b98h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC11LLPL)	0h
4b9ch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC11LLPU)	0h
4ba0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC12CTL)	0h
4ba4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC12FMT)	0h
4ba8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC12LLPL)	0h
4bach	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC12LLPU)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4bb0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC13CTL)	0h
4bb4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC13FMT)	0h
4bb8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC13LLPL)	0h
4bbch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC13LLPU)	0h
4bc0h	4	Input/Output Processing Pipe's Link Connection x Control (OPPLC14CTL)	0h
4bc4h	2	Input/Output Processing Pipe's Link Connection x Format (OPPLC14FMT)	0h
4bc8h	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC14LLPL)	0h
4bcch	4	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC14LLPU)	0h
c00h	4	Multiple Links Capability Header (MLCH)	20800h
c04h	4	Multiple Links Capability Declaration (MLCD)	1h
c40h	4	Link x Capabilities (LCAP0)	7h
8a8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC2LDPL)	0h
8ach	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC2LDPU)	0h
8b0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC3LLPL)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8b4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC3LLPU)	0h
8b8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC3LDPL)	0h
8bch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC3LDPU)	0h
8c0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC4LLPL)	0h
8c4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC4LLPU)	0h
8c8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC4LDPL)	0h
8cch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC4LDPU)	0h
8d0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC5LLPL)	0h
8d4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC5LLPU)	0h
8d8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC5LDPL)	0h
8dch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC5LDPU)	0h
8e0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC6LLPL)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8e4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC6LLPU)	0h
8e8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC6LDPL)	0h
8ech	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC6LDPU)	0h
8f0h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC7LLPL)	0h
8f4h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC7LLPU)	0h
8f8h	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC7LDPL)	0h
c44h	4	Link 0 Control (LCTL0)	10000h
c84h	4	Link 1 Control (LCTL1)	10000h
8fch	4	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC7LDPU)	0h
900h	4	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC8LLPL)	0h

Global Capabilities (GCAP) – Offset 0

This register resides in Primary well, and reset by platform reset.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
15:12	9h	RW/L	**Number of Output Streams Supported (OSS)** 0100b indicates that the Intel HD Audio controller supports four output streams. Locked when FNCFG.BCLD = 1.
11:8	7h	RW/L	**Number of Input Streams Supported (ISS)** 0100b indicates that the Intel HD Audio controller supports four input streams. Locked when FNCFG.BCLD = 1.
7:3	0h	RO	**Number of Bidirectional Streams Supported (BSS)** 00000b indicates that the Intel HD Audio controller supports 0 bidirectional streams.
2:1	0h	RW/L	**Number of Serial Data Out Signals (NSDO)** 00b indicates that the Intel HD Audio controller supports one Serial Data Output signal. For the case of multiple link segments is supported, this field indicates the number of SDO for link 0. Locked when FNCFG.BCLD = 1.
0	1b	RW/L	**64 Bit Address Supported (ADD64OK)** A 1 indicates that the Intel HD Audio controller supports 64 bit addressing for BDL addresses, data buffer addresses, and command buffer addresses. Locked when FNCFG.BCLD = 1.

Minor Version (VMIN) – Offset 2

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW/L	**Minor Version (VMIN)** Indicates the Intel HD Audio controller supports minor revision number 00h of the Intel HD Audio specification.

Major Version (VMAJ) – Offset 3

Bit Range	Default	Access	Field Name and Description
7:0	01h	RW/L	**Major Version (VMAJ)** Indicates the Intel HD Audio controller supports major revision number 1 of the Intel HD Audio specification.

Output Payload Capability (OUTPAY) – Offset 4

This register resides in Primary well and reset by platform reset.

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW/L	

Bit Range	Default	Access	Output Payload Capability (OUTPAY) Field Name and Description
			Indicates the total output payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. The default link clock speed of 24.000 MHz (the data is double pumped) provides 1000 bits per frame, or 62.5 words in total. 40 bits are used for command and control, leaving 60 words available for data payload. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Note: In the event that multiple links is supported (GCAP2.LCOUNT) 0), the payload advertised will be the lowest common denominator offered by the default clock frequency on each link. Locked when FNCFG.BCLD = 1.

Input Payload Capability (INPAY) – Offset 6

This register resides in Primary well and reset by platform reset.

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW/L	**Input Payload Capability (INPAY)** Indicates the total input payload available on the link. This does not include bandwidth used for response. This measurement is in 16-bit word quantities per 48 kHz frame. The default link clock speed of 24.000 MHz provides 500 bits per frame, or 31.25 words in total. 36 bits are used for response, leaving 29 words for data payload. Note that this value does not reflect any bandwidth increase due to support for multiple SDI lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Note: In the event that multiple links is supported (GCAP2.LCOUNT) 0), the payload advertised will be the lowest common denominator offered by the default clock frequency on each link. Locked when FNCFG.BCLD = 1.

Global Control (GCTL) – Offset 8

CRSTB bit is not affected by controller reset.

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0b	RW	**Accept Unsolicited Response Enable (UNSOL)** If UNSOL is a 1, Unsolicited Responses from the codecs are accepted by the controller and placed into the Response Input Ring Buffer. If UNSOL is a 0, unsolicited responses are not accepted, and dropped on the floor.
7:2	-	-	**Reserved**
1	0b	RW/1S/V	**Flush Control (FCNTRL)** Writing a 1 to this bit initiates a flush. When the flush completion is received by the controller, hardware sets the Flush Status bit and clears this Flush Control bit. Before a flush cycle is initiated, the DMA Position Buffer must be programmed with a valid memory address by software, but the DMA Position Buffer bit 0 need not be set to enable the position reporting mechanism. Also, all streams must be stopped (the associated RUN bit must be 0). When the flush is initiated, the controller will flush pipelines to memory to guarantee that the hardware is ready to transition to a D3 state. Setting this bit is not a critical step in the power state transition if the content of the FIFOs is not critical.

Bit Range	Default	Access	Field Name and Description
0	0b	RW/V	**Controller Reset# (CRSTB)** After the hardware has completed sequencing into the reset state, it will report a 0 in this bit. Software must read a 0 from this bit to verify that the controller is in reset. Writing a 1 to this bit causes the controller to exit its reset state and deassert the Intel HD Audio link RESET# signal. Software is responsible for setting/clearing this bit such that the minimum Intel HD Audio link RESET# signal assertion pulse width specification is met. When the controller hardware is ready to begin operation, it will report a 1 in this bit. Software must read a 1 from this bit before accessing any controller registers. The CRST bit defaults to a 0 after hardware reset, therefore software needs to write a 1 to this bit to begin operation. Note that the CORB/RIRB RUN bits and all Stream RUN bits must be verified cleared to zero before CRST bit is written to 0 (asserted) in order to assure a clean re-start. When setting or clearing CRST, software must ensure that minimum link timing requirements (minimum RESET# assertion time, etc.) are met. When CRST is 0 indicating that the controller is in reset, writes to all Intel HD Audio memory mapped registers are ignored as if the device is not present. The only exception is the Global Control register containing the CRST bit itself. The Global Control register is write-able as a DWord, Word, or Byte even when CRST is 0 if the byte enable for the byte containing the CRST bit (Byte Enable 0) is active. If Byte Enable 0 is not active, writes to the Global Control register will be ignored when CRST is 0. When CRST is 0, reads to Intel HD Audio memory mapped registers will return their default value except for registers that are not reset with PLTRST# or on a D3hot to D0 transition.

Wake Enable (WAKEEN) – Offset c

This register indicates which bits in the WAKESTS register may cause either a wake event or an interrupt.

Bit Range	Default	Access	Field Name and Description
14:3	-	-	**Reserved**
2:0	0h	RW	**SDIN Wake Enable Flags (WAKEEN)** Bits which control which SDI signal(s) may generate a wake event. A 1 bit in the bit mask indicates that the associated SDIN signal is enabled to generate a wake. These bits are cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

Processing Pipe Capability Header (PPCH) – Offset 800

This register resides in Primary well (always on), or resides in Primary well (gated) with

state retention, and reset by platform reset.

Bit Range	Default	Access	Field Name and Description
31:28	0h	RW/L	**Capability Version (VER)** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1.
27:16	003h	RW/L	**Capability Identifier (ID)** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1.
15:0	0500h	RW/L	**Next Capability Pointer (PTR)** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. Point to Global Time Synchronization capability. Locked when FNCFG.BCLD = 1.

Processing Pipe Control (PPCTL) – Offset 804

This register is not affected by stream reset.

Note that the PROCEN bit should only be modified when the corresponding host DMA and link DMA are idle, i.e. RUN bits are cleared, and the DMA contexts have been destroyed through SRST bits if it was previously activated.

Note that GPROCEN bit does not really enable or disable the Audio DSP operation, but mainly to workaround some legacy

Intel HD Audio driver software such that if GPROCEN = 0, ADSPxBA (BAR2) is mapped to the Intel HD Audio memory mapped configuration registers, for compliancy with some legacy SW implementation. If GPROCEN = 1, only then ADSPxBA (BAR2) is mapped to the actual Audio DSP memory mapped configuration registers.

The number of PROCEN bits in this register is depending on the total number of stream DMA implemented.

Bit Range	Default	Access	Field Name and Description
31	0b	RW	**Processing Interrupt Enable (PIE)** Enables the general interrupt for the Audio DSP function. When set to 1 (and GIE is enabled), the Audio DSP generates an interrupt when the PIS bit gets set.
30:16	-	-	**Reserved**
15:0	0h	RW	**Processing Enable (PROCEN)** When set to 1 the DMA engine associated with this stream will be enabled to route the audio stream to DSP audio pipes in the Audio DSP for processing. When cleared to 0 the DMA engine associated with this stream will be bypassing the Audio DSP and route the audio stream directly to the audio link.

Processing Pipe Status (PPSTS) – Offset 808

Bit Range	Default	Access	Field Name and Description
31	0b	RO/V	**Processing Interrupt Status (PIS)** Status of general interrupt for the Audio DSP function. A 1 indicates that an interrupt condition occurred in the Audio DSP function. The exact cause can be determined by interrogating the ADSPIS register. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of the interrupt status bits in ADSPIS register.

Bit Range	Default	Access	Field Name and Description
30:0	-	-	**Reserved**

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC0LLPL) – Offset 810

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Linear Link Position Lower (LLPL)** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC0LLPU) – Offset 814

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Linear Link Position Upper (LLPU)** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC0LDPL) – Offset 818

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Linear DMA Position Lower (LDPL)** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

Wake Status (WAKESTS) – Offset e

This register indicates that a Status Change event has occurred on the link, which usually indicates that either the codec has just come out of reset and is requesting an address, or that a codec is signaling a wake event.

Bit Range	Default	Access	Field Name and Description
14:3	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
2:0	0h	RW/1C/V	**SDIN State Change Status Flags (WAKESTS)** Flag bits that indicate which SDI signal(s) received a State Change event. The bits are cleared by writing 1's to them. These bits are cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

Global Status (GSTS) – Offset 10

Bit Range	Default	Access	Field Name and Description
14:2	-	-	**Reserved**
1	0b	RW/1C/V	**Flush Status (FSTS)** This bit is set to a 1 by the hardware to indicate that the flush cycle initiated when the FCNTRL bit was set has completed. Software must write a 1to clear this bit before the next time FCNTRL is set.
0	-	-	**Reserved**

Global Capabilities 2 (GCAP2) – Offset 12

This register resides in Primary well and reset by platform reset.

Bit Range	Default	Access	Field Name and Description
14:1	-	-	**Reserved**
0	1b	RW/V/L	**Energy Efficient Audio Capability (EEAC)** Indicates whether the energy efficient audio with deeper buffering is supported or not. 0 = Not supported. 1 = Supported. Locked when FNCFG.BCLD = 1.

Linked List Capabilities Header (LLCH) – Offset 14

This register resides in Primary well and reset by platform reset.

Bit Range	Default	Access	Field Name and Description
15:0	0C00h	RW/L	**First Capability Pointer (PTR)** This field contains the offset to the first capability structure of the linked list capabilities, or 0000h if no linked list capabilities exist. Point to Multiple Links Capability. Locked when FNCFG.BCLD = 1.

Output Stream Payload Capability (OUTSTRMPAY) – Offset 18

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
15:0	0030h	RO	**Output Stream Payload Capability (OUTSTRMPAY)** Indicates maximum number of words per frame for any single output stream. This measurement is in 16 bit word quantities per 48 kHz frame. 48 Words (96B) is the maximum supported, therefore a value of 30h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Output Stream Descriptor register. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload

Input Stream Payload Capability (INSTRMPAY) – Offset 1a

This register indicates the maximum number of Words per frame for any single input stream.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
15:0	0018h	RO	**Input Stream Payload Capability (INSTRMPAY)** Indicates maximum number of words per frame for any single input stream. This measurement is in 16 bit word quantities per 48 kHz frame. 24 Words (48B) is the maximum supported, therefore a value of 18h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Input Stream Descriptor register. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload

Interrupt Control (INTCTL) – Offset 20

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31	0b	RW	**Global Interrupt Enable (GIE)** Global bit to enable device interrupt generation. When set to 1 the Intel HD Audio function is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space, such as the Interrupt Enable bit in the PCI Configuration Space.
30	0b	RW	**Controller Interrupt Enable (CIE)** Enables the general interrupt for controller functions. When set to 1 (and GIE is enabled), the controller generates an interrupt when the CIS bit gets set.
29:16	-	-	**Reserved**
15:0	0h	RW	**Stream Interrupt Enable (SIE)** When set to 1 the individual Streams are enabled to generate an interrupt when the corresponding stream status bits get set. A stream interrupt will be caused as a result of a buffer with IOC=1 in the BDL entry being completed, or as a result of a FIFO error (underrun or overrun) occurring. Control over the generation of each of these sources is in the associated Stream Descriptor. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set.

Interrupt Status (INTSTS) – Offset 24

GIS and CIS bits are not affected by controller reset.

The number of SIS bits in this register is depending on the total number of stream DMA implemented.

Bit Range	Default	Access	Field Name and Description
31	0b	RO/V	**Global Interrupt Status (GIS)** This bit is an OR of all of the interrupt status bits in this register and PPSTS register
30	0b	RW/V	**Controller Interrupt Status (CIS)** Status of general controller interrupt. A 1 indicates that an interrupt condition occurred due to a Response Interrupt, a Response Buffer Overrun Interrupt, CORB Memory Error Interrupt, or a SDIN State Change event. The exact cause can be determined by interrogating other registers. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of the stated interrupt status bits for this register.
29:16	-	-	**Reserved**
15:0	0h	RW/V	**Stream Interrupt Status (SIS)** A 1 indicates that an interrupt condition occurred on the corresponding Stream. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of an individual stream s interrupt status bits. The streams are numbered and the SIS bits assigned sequentially, based on their order in the register set.

Wall Clock Counter (WALCLK) – Offset 30

The 32 bit monotonic counter provides a 'wall clock' that can be used by system software to synchronize independent audio controllers.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO/V	**Wall Clock Counter (WALCLK)** 32 bit counter that is incremented on each link BCLK period and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds. This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset. With the introduction of multiple link segments for the Intel HD Audio controller, and the capability of running each link segment at different clock speed, the BCLK definition for this counter is fixed at 24 MHz equivalent rate always, independent of the physical link clock speed, and reports the link 0 wall clock value.

Stream Synchronization (SSYNC) – Offset 38

To synchronize two or more streams the corresponding SSYNC bits for the streams to be synchronized should be set to 1 before the 'RUN' bit for each stream is set.

The RUN bit for the corresponding stream must be set to 1 (and FIFORDY=1) prior to that stream's SSYNC bit being written to 0. To start multiple streams synchronously, the stream sync bits for those streams should be written to 0 at the same time. For all SSYNC bits on output engines that transition from 1 to 0 on the same write, the formatter will deliver a sample over the link in the same 48kHz frame. For all SSYNC bits on input engines that transition from 1 to 0 on the same write, the formatter will take stream data off the link and place it in the FIFO.

If synchronization is not desired, the stream synchronization bits may be left 0, and the stream will simply begin running normally when the stream's 'RUN' bit is set.

In addition to platform reset, FLR, and controller reset, the register is also reset by stream reset.

The number of SSYNC bits in this register is depending on the total number of stream DMA implemented.

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0h	RW	**Stream Synchronization Bits (SSYNC)** The Stream Synchronization bits, when set to 1, block data from being sent on or received from the link. Each bit controls the associated Stream Descriptor, bit 0 corresponds to the first Stream Descriptor, etc. To synchronously start a set of DMA engines, the bits in the SSYNC register are first set to a 1. The RUN bits for the associated Stream Descriptors are then set to a 1 to start the DMA engines. When all streams are ready (FIFORDY=1), the associated SSYNC bits can all be set to 0 at the same time, and transmission or reception of bits to or from the link will begin together at the start of the next full link frame. To synchronously stop streams, first the bits are set in the SSYNC register, and then the individual RUN bits in the Stream Descriptors are cleared by software. The streams are numbered and the SSYNC bits assigned sequentially, based on their order in the register set.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC0LDPU) – Offset 81c

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Linear DMA Position Offset Upper (LDPU)** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC1LLPL) – Offset 820

Same definition as IPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC1LLPU) – Offset 824

Same definition as IPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC1LDPL) – Offset 828

Same definition as IPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC1LDPU) – Offset 82c

Same definition as IPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC2LLPL) – Offset 830

Same definition as IPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC2LLPU) – Offset 834

Same definition as IPPHC0LLPU.

CORB Lower Base Address (CORBLBASE) – Offset 40

Bit Range	Default	Access	Field Name and Description
31:7	0000000h	RW	**CORB Lower Base Address (CORBLBASE)** Lower address of the Command Output Ring Buffer, allowing the CORB Base Address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	-	-	**Reserved**

CORB Upper Base Address (CORBUBASE) – Offset 44

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW/L	**CORB Upper Base Address (CORBUBASE)** Upper 32 bits of address of the Command Output Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.ADD64OK = 0.

CORB Write Pointer (CORBWP) – Offset 48

Bit Range	Default	Access	Field Name and Description
14:8	-	-	**Reserved**
7:0	00h	RW	**CORB Write Pointer (CORBWP)** Software writes the last valid CORB entry offset into this field in Dword granularity. The DMA engine fetches commands from the CORB until the Read Pointer matches the Write Pointer. Supports 256 CORB entries (256 x 4B=1KB). This field may be written while the DMA engine is running.

CORB Read Pointer (CORBRP) – Offset 4a

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
15	0b	RW/V	**CORB Read Pointer Reset (CORBRPRST)** Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual pre-fetched commands in the CORB hardware buffer within the Intel Audio controller. The hardware will physically update this bit to 1 when the CORB Pointer reset is complete. Software must read a 1 to verify that the reset completed correctly. Software must clear this bit back to 0 and read back the 0 to verify that the clear completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted.
14:8	-	-	**Reserved**
7:0	00h	RO/V	**CORB Read Pointer (CORBRP)** Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB Read Pointer offset in Dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports 256 CORB entries (256 x 4B=1KB). This field may be read while the DMA engine is running.

CORB Control (CORBCTL) – Offset 4c

Length: 1 bytes

Bit Range	Default	Access	Field Name and Description
6:2	-	-	**Reserved**
1	0b	RW/V	**Enable CORB DMA Engine (CORBRUN)** 0 = DMA Stop 1 = DMA Run After SW writes a 0 to this bit, the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.
0	0b	RW	**CORB Memory Error Interrupt Enable (CMEIE)** If this bit is set (and GIE and CIE are enabled), the controller will generate an interrupt if the MEI status bit is set.

CORB Status (CORBSTS) – Offset 4d

Bit Range	Default	Access	Field Name and Description
6:1	-	-	**Reserved**
0	0b	RW/1C/V	**CORB Memory Error Indication (CMEI)** If this status bit is set, the controller has detected an error in the pathway between the controller and memory. This may be an ECC bit error or any other type of detectable data error which renders the command data fetched invalid. Software can clear this bit by writing a 1 to it. However, this type of error leaves the audio subsystem in an unviable state and typically requires CRST#.

CORB Size (CORBSIZE) – Offset 4e

Bit Range	Default	Access	Field Name and Description
7:4	4h	RO	**CORB Size Capability (CORBSZCAP)** 0100b indicates that the PCH only supports a CORB size of 256 CORB entries (1024B).
3:2	-	-	**Reserved**
1:0	10b	RO	**CORB Size (CORBSIZE)** Hardwired to 10b which sets the CORB size to 256 entries (1024B).

RIRB Lower Base Address (RIRBLBASE) – Offset 50

Bit Range	Default	Access	Field Name and Description
31:7	0000000 h	RW	**RIRB Lower Base Address (RIRBLBASE)** Lower address of the Response Input Ring Buffer, allowing the RIRB Base Address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	-	-	**Reserved**

RIRB Upper Base Address (RIRBUBASE) – Offset 54

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW/L	**RIRB Upper Base Address (RIRBUBASE)** Upper 32 bits of address of the Command Output Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

RIRB Write Pointer (RIRBWP) – Offset 58

Bit Range	Default	Access	Field Name and Description
15	0b	WO	**RIRB Write Pointer Reset (RIRBWPRST)** Software writes a 1 to this bit to reset the RIRB Write Pointer to 0's. The RIRB DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit will always be read as 0.
14:8	-	-	**Reserved**
7:0	00h	RO/V	**RIRB Write Pointer (RIRBWP)** Indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in 2 Dword RIRB entry units (since each RIRB entry is 2 Dwords long). Supports up to 256 RIRB entries (256 x 8B=2KB). This field may be read while the DMA engine is running.

Response Interrupt Count (RINTCNT) – Offset 5a

Bit Range	Default	Access	Field Name and Description
14:8	-	-	**Reserved**
7:0	00h	RW	**N Response Interrupt Count (RINTCNT)** 0000_0001b = 1 Response sent to RIRB ... 1111_1111b = 255 Responses sent to RIRB 0000_0000b = 256 Responses sent to RIRB The DMA engine should be stopped when changing this field or else an interrupt may be lost. Note that each Response occupies 2 Dwords in the RIRB. This is compared to the total number of responses that have been returned, as opposed to the number of frames in which there were responses. If more than one codec responds in one frame, then the count is increased by the number of responses received in the frame.

RIRB Control (RIRBCTL) – Offset 5c

Bit Range	Default	Access	Field Name and Description
6:3	-	-	**Reserved**
2	0b	RW	**Response Overrun Interrupt Control (RIRBOIC)** If this bit is set (and GIE and CIE are enabled), the hardware will generate an interrupt when the Response Overrun Interrupt Status bit is set.

Bit Range	Default	Access	Field Name and Description
1	0b	RW/V	**RIRB DMA Enable (RIRBRUN)** 0 = DMA Stop 1 = DMA Run After SW writes a 0 to this bit, the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.
0	0b	RW	**Response Interrupt Control (RINTCTL)** 0 = Disable Interrupt 1 = Generate an interrupt (if GIE and CIE are enabled) after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI_x inputs (whichever occurs first). The N counter is reset when the interrupt is generated.

RIRB Status (RIRBSTS) – Offset 5d

Bit Range	Default	Access	Field Name and Description
6:3	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
2	0b	RW/1C/V	**Response Overrun Interrupt Status (RIRBOIS)** Hardware sets this bit to a 1 when the RIRB DMA engine is not able to write the incoming responses to memory before additional incoming responses overrun the internal FIFO. When the overrun occurs, the hardware will drop the responses which overrun the buffer. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.
1	-	-	**Reserved**
0	0b	RW/1C/V	**Response Interrupt (RINTFL)** Hardware sets this bit to a 1 when an interrupt has been generated after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI(x) inputs (whichever occurs first). Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.

RIRB Size (RIRBSIZE) – Offset 5e

Bit Range	Default	Access	Field Name and Description
7:4	4h	RO	**RIRB Size Capability (RIRBSZCAP)** 0100b indicates that the PCH only supports a RIRB size of 256 RIRB entries (2048B).

Bit Range	Default	Access	Field Name and Description
3:2	-	-	**Reserved**
1:0	10b	RO	**RIRB Size (RIRBSIZE)** Hardwired to 10b which sets the RIRB size to 256 entries (2048B).

Immediate Command (IC) – Offset 60

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Immediate Command (IC)** The command to be sent to the codec via the Immediate Command mechanism is written to this register. The command stored in this register is sent out over the link during the next available frame after a 1 is written to the ICB bit.

Immediate Response (IR) – Offset 64

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO/V	**Immediate Response (IR)** This register contains the response received from a codec resulting from a command sent via the Immediate Command mechanism. If multiple codecs responded in the same frame, there is no guarantee as to which response will be latched. Therefore broadcast-type commands must not be issued via the Immediate Command mechanism.

Immediate Command Status (ICS) – Offset 68

Bit Range	Default	Access	Field Name and Description
14:2	-	-	**Reserved**
1	0b	RW/1C/V	**Immediate Result Valid (IRV)** This bit is set to a 1 by hardware when a new response is latched into the IR register. This is a status flag indicating that software may read the response from the Immediate Response register. Software must clear this bit (by writing a one to it) before issuing a new command so that the software may determine when a new response has arrived.
0	0b	RW/V	**Immediate Command Busy (ICB)** When this bit as read as a 0 it indicates that a new command may be issued using the Immediate Command mechanism. When this bit transitions from a 0 to a 1 (via software writing a 1), the controller issues the command currently stored in the Immediate Command register to the codec over the link. When the corresponding response is latched into the Immediate Response register, the controller hardware sets the IRV flag and clears the ICB bit back to 0. SW may write this bit to a 0 if the bit fails to return to 0 after a reasonable timeout period. Note that an Immediate Command must not be issued while the CORB/RIRB mechanism is operating, otherwise the responses conflict. This must be enforced by software.

DMA Position Lower Base Address (DPLBASE) – Offset 70

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:7	0000000h	RW	**DMA Position Lower Base Address (DPLBASE)** Lower 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control, and must be programmed with a valid value before the FLCNRTL bit is set.
6:1	-	-	**Reserved**
0	0b	RW	**DMA Position Buffer Enable (DPBE)** When this bit is set to a '1', the controller will write the DMA positions of each of the DMA engines to the buffer in main memory periodically (typically once/frame). Software can use this value to know what data in memory is valid data. The controller must guarantee that the values in the DMA Position Buffer that the software can read represent positions in the stream for which valid data exists in the Stream's DMA buffer. This has particular relevance in systems which support isochronous transfer, the stream positions in the software-visible memory buffer must represent stream data which has reached the Global Observation point.

DMA Position Upper Base Address (DPUBASE) – Offset 74

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW/L	**DMA Position Upper Base Address (DPUBASE)** Upper 32 bits of address of the DMA Position Buffer Base Address. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.ADD64OK = 0.

Input/Output Stream Descriptor x Control (ISD0CTL) – Offset 80

NOTE: This register definition applies to all of the following input and output streams at the corresponding offsets:

Input stream 0: offset 80h

Input stream 1: offset A0h

Input stream 2: offset C0h

Input stream 3: offset E0h

Input stream 4: offset 100h

Input stream 5: offset 120h

Input stream 6: offset 140h

Input stream 7: offset 280h

Input stream 8: offset 2A0h

Input stream 9: offset 2C0h

Input stream 10: offset 2E0h

Input stream 11: offset 300h

Input stream 12: offset 320h

Input stream 13: offset 340h

Input stream 14: offset 360h

Output stream 0: offset 160h

Output stream 1: offset 180h

Output stream 2: offset 1A0h

Output stream 3: offset 1C0h

Output stream 4: offset 1E0h

Output stream 5: offset 200h

Output stream 6: offset 220h

output stream 7: offset 240h

Output stream 8: offset 260h

Output stream 9: offset 380h

Output stream 10: offset 3A0h

Output stream 11: offset 3C0h

Output stream 12: offset 3E0h

Output stream 13: offset 400h

Output stream 14: offset 420h

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:20	0h	RW	

Bit Range	Default	Access	Stream Number (STRM) Field Name and Description
			This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.

Bit Range	Default	Access	Field Name and Description
19	0b	RO	**Bidirectional Direction Control (DIR)** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	1b	RO	**Traffic Priority (TP)** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	00b	RW/L	**Stripe Control (STRIPE)** Input Stream: This field is meaningless for input streams. Output Stream: For output streams it controls the number of SDO signals to stripe data across. Locked when GCAP.NSDO = 00b.
15:6	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
5	0b	RW/V/L	**FIFO Limit Change (FIFOLC)** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set).
4	0b	RW	**Descriptor Error Interrupt Enable (DEIE)** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0b	RW	**FIFO Error Interrupt Enable (FEIE)** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0b	RW	**Interrupt On Completion Enable (IOCE)** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur

Bit Range	Default	Access	Field Name and Description
1	0b	RW/V	**Stream Run (RUN)** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0b	RW/V	**Stream Reset (SRST)** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

Input/Output Stream Descriptor x Status (ISD0STS) – Offset 83

NOTE: This register applies to the following input and output streams at the corresponding offsets:

Input stream 0: offset 83h

Input stream 1: offset A3h

Input stream 2: offset C3h

Input stream 3: offset E3h

Input stream 4: offset 103h

Input stream 5: offset 123h

Input stream 6: offset 143h

Input stream 7: offset 283h

Input stream 8: offset 2A3h

Input stream 9: offset 2C3h

Input stream 10: offset 2E3h

Input stream 11: offset 303h

Input stream 12: offset 323h

Input stream 13: offset 343h

Input stream 14: offset 363h

Output stream 0: offset 163h

Output stream 1: offset 183h

Output stream 2: offset 1A3h

Output stream 3: offset 1C3h

Output stream 4: offset 1E3h

Output stream 5: offset 203h

Output stream 6: offset 223h

output stream 7: offset 243h

Output stream 8: offset 263h

Output stream 9: offset 383h

Output stream 10: offset 3A3h

Output stream 11: offset 3C3h

Output stream 12: offset 3E3h

Output stream 13: offset 403h

Output stream 14: offset 423h

Bit Range	Default	Access	Field Name and Description
6	-	-	**Reserved**
5	0b	RO/V	**FIFO Ready (FIFORDY)** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0b	RW/1C/V	**Descriptor Error (DESE)** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.

Bit Range	Default	Access	Field Name and Description
3	0b	RW/1C/V	**FIFO Error (FIFOE)** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0b	RW/1C/V	**Buffer Completion Interrupt Status (BCIS)** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	-	-	**Reserved**

Input/Output Stream Descriptor x Link Position in Buffer (ISD0LPIB) – Offset 84

NOTE: This register applies to the following input and output streams at the corresponding offsets:

Input stream 0: offset 84h

Input stream 1: offset A4h

Input stream 2: offset C4h

Input stream 3: offset E4h

Input stream 4: offset 104h

Input stream 5: offset 124h

Input stream 6: offset 144h

Input stream 7: offset 284h

Input stream 8: offset 2A4h

Input stream 9: offset 2C4h

Input stream 10: offset 2E4h

Input stream 11: offset 304h

Input stream 12: offset 324h

Input stream 13: offset 344h

Input stream 14: offset 364h

Output stream 0: offset 164h

Output stream 1: offset 184h

Output stream 2: offset 1A4h

Output stream 3: offset 1C4h

Output stream 4: offset 1E4h

Output stream 5: offset 204h

Output stream 6: offset 224h

output stream 7: offset 244h

Output stream 8: offset 264h

Output stream 9: offset 384h

Output stream 10: offset 3A4h

Output stream 11: offset 3C4h

Output stream 12: offset 3E4h

Output stream 13: offset 404h

Output stream 14: offset 324h

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW/V	**Link Position in Buffer (LPIB)** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

Input/Output Stream Descriptor x Cyclic Buffer Length (ISD0CBL) – Offset 88

NOTE: This register applies to the following input and output streams at the corresponding offsets:

Input stream 0: offset 88h

Input stream 1: offset A8h

Input stream 2: offset C8h

Input stream 3: offset E8h

Input stream 4: offset 108h

Input stream 5: offset 128h

Input stream 6: offset 148h

Input stream 7: offset 288h

Input stream 8: offset 2A8h

Input stream 9: offset 2C8h

Input stream 10: offset 2E8h

Input stream 11: offset 308h

Input stream 12: offset 328h

Input stream 13: offset 348h

Input stream 14: offset 368h

Output stream 0: offset 168h

Output stream 1: offset 188h

Output stream 2: offset 1A8h

Output stream 3: offset 1C8h

Output stream 4: offset 1E8h

Output stream 5: offset 208h

Output stream 6: offset 228h

output stream 7: offset 248h

Output stream 8: offset 268h

Output stream 9: offset 388h

Output stream 10: offset 3A8h

Output stream 11: offset 3C8h

Output stream 12: offset 3E8h

Output stream 13: offset 408h

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Cyclic Buffer Length (CBL)** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

Input/Output Stream Descriptor x Last Valid Index (ISD0LVI) – Offset 8c

NOTE: This register applies to the following input and output streams at the corresponding offsets:

Input stream 0: offset 8Ch

Input stream 1: offset ACh

Input stream 2: offset CCh

Input stream 3: offset ECh

Input stream 4: offset 10Ch

Input stream 5: offset 12Ch

Input stream 6: offset 14Ch

Input stream 7: offset 28Ch

Input stream 8: offset 2ACh

Input stream 9: offset 2CCh

Input stream 10: offset 2ECh

Input stream 11: offset 30Ch

Input stream 12: offset 32Ch

Input stream 13: offset 34Ch

Input stream 14: offset 36Ch

Output stream 0: offset 16Ch

Output stream 1: offset 18Ch

Output stream 2: offset 1ACh

Output stream 3: offset 1CCh

Output stream 4: offset 1ECh

Output stream 5: offset 20Ch

Output stream 6: offset 22Ch

output stream 7: offset 24Ch

Output stream 8: offset 26Ch

Output stream 9: offset 38Ch

Output stream 10: offset 3ACh

Output stream 11: offset 3CCh

Output stream 12: offset 3ECh

Output stream 13: offset 40Ch

Output stream 14: offset 42Ch

Bit Range	Default	Access	Field Name and Description
14:8	-	-	**Reserved**
7:0	00h	RW	**Last Valid Index (LVI)** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD0FIFOW) – Offset 8e

NOTE: This register applies to the following input and output streams at the corresponding offsets:

Input stream 0: offset 8Eh

Input stream 1: offset AEh

Input stream 2: offset CEh

Input stream 3: offset EEh

Input stream 4: offset 10Eh

Input stream 5: offset 12Eh

Input stream 6: offset 14Eh

Input stream 7: offset 28Eh

Input stream 8: offset 2AEh

Input stream 9: offset 2CEh

Input stream 10: offset 2EEh

Input stream 11: offset 30Eh

Input stream 12: offset 32Eh

Input stream 13: offset 34Eh

Input stream 14: offset 36Eh

Output stream 0: offset 16Eh

Output stream 1: offset 18Eh

Output stream 2: offset 1AEh

Output stream 3: offset 1CEh

Output stream 4: offset 1EEh

Output stream 5: offset 20Eh

Output stream 6: offset 22Eh

output stream 7: offset 24Eh

Output stream 8: offset 26Eh

Output stream 9: offset 38Eh

Output stream 10: offset 3AEh

Output stream 11: offset 3CEh

Output stream 12: offset 3EEh

Output stream 13: offset 40Eh

Output stream 14: offset 42Eh

Bit Range	Default	Access	Field Name and Description
14:3	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
2:0	100b	RO/V	**FIFOW (FIFOW)** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. 000-011: Reserved 100: 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101: 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111: Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

Input/Output Stream Descriptor x FIFO Size (ISD0FIFOS) – Offset 90

NOTE: This register applies to the following input and output streams at the corresponding offsets:

Input stream 0: offset 90h

Input stream 1: offset B0h

Input stream 2: offset D0h

Input stream 3: offset F0h

Input stream 4: offset 110h

Input stream 5: offset 130h

Input stream 6: offset 150h

Input stream 7: offset 290h

Input stream 8: offset 2B0h

Input stream 9: offset 2D0h

Input stream 10: offset 2F0h

Input stream 11: offset 310h

Input stream 12: offset 330h

Input stream 13: offset 350h

Input stream 14: offset 370h

Output stream 0: offset 170h

Output stream 1: offset 190h

Output stream 2: offset 1B0h

Output stream 3: offset 1D0h

Output stream 4: offset 1F0h

Output stream 5: offset 210h

Output stream 6: offset 230h

output stream 7: offset 250h

Output stream 8: offset 270h

Output stream 9: offset 390h

Output stream 10: offset 3B0h

Output stream 11: offset 3D0h

Output stream 12: offset 3F0h

Output stream 13: offset 410h

Output stream 14: offset 430h

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW/V	

Bit Range	Default	Access	FIFO Size (FIFOS) Field Name and Description
			When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

Input/Output Stream Descriptor x Format (ISD0FMT) – Offset 92

NOTE: This register applies to the following input and output streams at the corresponding offsets:

Input stream 0: offset 92h

Input stream 1: offset B2h

Input stream 2: offset D2h

Input stream 3: offset F2h

Input stream 4: offset 112h

Input stream 5: offset 132h

Input stream 6: offset 152h

Input stream 7: offset 292h

Input stream 8: offset 2B2h

Input stream 9: offset 2D2h

Input stream 10: offset 2F2h

Input stream 11: offset 312h

Input stream 12: offset 332h

Input stream 13: offset 352h

Input stream 14: offset 372h

Output stream 0: offset 172h

Output stream 1: offset 192h

Output stream 2: offset 1B2h

Output stream 3: offset 1D2h

Output stream 4: offset 1F2h

Output stream 5: offset 212h

Output stream 6: offset 232h

output stream 7: offset 252h

Output stream 8: offset 272h

Output stream 9: offset 392h

Output stream 10: offset 3B2h

Output stream 11: offset 3D2h

Output stream 12: offset 3F2h

Output stream 13: offset 412h

Output stream 14: offset 432h

Bit Range	Default	Access	Field Name and Description
14	0b	RW	**Sample Base Rate (BASE)** 0=48 kHz 1=44.1 kHz
13:11	000b	RW	**Sample Base Rate Multiple (MULT)** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved

Bit Range	Default	Access	Field Name and Description
10:8	000b	RW	**Sample Base Rate Divisor (DIV)** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)

Bit Range	Default	Access	Field Name and Description
7	-	-	**Reserved**
6:4	000b	RW	**Bits per Sample (BITS)** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved

Bit Range	Default	Access	Field Name and Description
3:0	0000b	RW	**Number of Channels (CHAN)** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

Input/Output Stream Descriptor x FIFO Limit (ISD0FIFOL) – Offset 94

NOTE: This register applies to the following input and output streams at the corresponding offsets:

Input stream 0: offset 94h

Input stream 1: offset B4h

Input stream 2: offset D4h

Input stream 3: offset F4h

Input stream 4: offset 114h

Input stream 5: offset 134h

Input stream 6: offset 154h

Input stream 7: offset 294h

Input stream 8: offset 2B4h

Input stream 9: offset 2D4h

Input stream 10: offset 2F4h

Input stream 11: offset 314h

Input stream 12: offset 334h

Input stream 13: offset 354h

Input stream 14: offset 374h

Output stream 0: offset 174h

Output stream 1: offset 194h

Output stream 2: offset 1B4h

Output stream 3: offset 1D4h

Output stream 4: offset 1F4h

Output stream 5: offset 214h

Output stream 6: offset 234h

output stream 7: offset 254h

Output stream 8: offset 274h

Output stream 9: offset 394h

Output stream 10: offset 3B4h

Output stream 11: offset 3D4h

Output stream 12: offset 3F4h

Output stream 13: offset 414h

Output stream 14: offset 434h

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
14	0b	RW/L	**Granularity (GNL)** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

Bit Range	Default	Access	Field Name and Description
13:0	0000h	RW/L	**FIFO Limit (FIFOL)** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. 0 = Disabled (FIFOS is the limit) 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD0BDLPLBA) – Offset 98

NOTE: This register applies to the following input and output streams at the corresponding offsets:

Input stream 0: offset 98h

Input stream 1: offset B8h

Input stream 2: offset D8h

Input stream 3: offset F8h

Input stream 4: offset 118h

Input stream 5: offset 138h

Input stream 6: offset 158h

Input stream 7: offset 298h

Input stream 8: offset 2B8h

Input stream 9: offset 2D8h

Input stream 10: offset 2F8h

Input stream 11: offset 318h

Input stream 12: offset 338h

Input stream 13: offset 358h

Input stream 14: offset 378h

Output stream 0: offset 178h

Output stream 1: offset 198h

Output stream 2: offset 1B8h

Output stream 3: offset 1D8h

Output stream 4: offset 1F8h

Output stream 5: offset 218h

Output stream 6: offset 238h

output stream 7: offset 258h

Output stream 8: offset 278h

Output stream 9: offset 398h

Output stream 10: offset 3B8h

Output stream 11: offset 3D8h

Output stream 12: offset 3F8h

Output stream 13: offset 418h

Output stream 14: offset 438h

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:7	0000000h	RW	**Buffer Descriptor List Lower Base Address (BDLPLBA)** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	-	-	**Reserved**

Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD0BDLPUBA) – Offset 9c

NOTE: This register applies to the following input and output streams at the corresponding offsets:

Input stream 0: offset 9Ch

Input stream 1: offset BCh

Input stream 2: offset DCh

Input stream 3: offset FCh

Input stream 4: offset 11Ch

Input stream 5: offset 13Ch

Input stream 6: offset 15Ch

Input stream 7: offset 29Ch

Input stream 8: offset 2BCh

Input stream 9: offset 2DCh

Input stream 10: offset 2FCh

Input stream 11: offset 31Ch

Input stream 12: offset 33Ch

Input stream 13: offset 35Ch

Input stream 14: offset 37Ch

Output stream 0: offset 17Ch

Output stream 1: offset 19Ch

Output stream 2: offset 1BCh

Output stream 3: offset 1DCh

Output stream 4: offset 1FCh

Output stream 5: offset 21Ch

Output stream 6: offset 23Ch

output stream 7: offset 25Ch

Output stream 8: offset 27Ch

Output stream 9: offset 39Ch

Output stream 10: offset 3BCh

Output stream 11: offset 3DCh

Output stream 12: offset 4FCh

Output stream 13: offset 41Ch

Output stream 14: offset 43Ch

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA)** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC8LLPU) – Offset 904

Same definition as OPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC8LDPL) – Offset 908

Same definition as OPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC8LDPU) – Offset 90c

Same definition as OPPHC0LDPU.

Input/Output Processing Pipe's Link Connection x Control (IPPLC0CTL) – Offset 910

SRST bit is not affected by stream reset.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:20	0h	RW	

Bit Range	Default	Access	Field Name and Description
			Stream Number (STRM) This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19:2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1	0b	RW/V	**Stream Run (RUN)** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0b	RW/V	**Stream Reset (SRST)** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

Input/Output Processing Pipe's Link Connection x Format (IPPLC0FMT) – Offset 914

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
14	0b	RW	**Sample Base Rate (BASE)** 0=48 kHz 1=44.1 kHz
13:11	0h	RW	**Sample Base Rate Multiple (MULT)** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved

Bit Range	Default	Access	Field Name and Description
10:8	0h	RW	**Sample Base Rate Divisor (DIV)** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
6:4	0h	RW	**Bits per Sample (BITS)** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h	RW	**Number of Channels (CHAN)** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

Input/Output Processing Pipe's Link Connection x Linear Link

Position Lower (IPPLC0LLPL) – Offset 918

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Linear Link Position Lower (LLPL)** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC0LLPU) – Offset 91c

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Linear Link Position Upper (LLPU)** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

Input/Output Processing Pipe's Link Connection x Control (IPPLC1CTL) – Offset 920

Same definition as IPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (IPPLC1FMT) – Offset 924

Same definition as IPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC1LLPL) – Offset 928

Same definition as IPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC1LLPU) – Offset 92c

Same definition as IPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (IPPLC2CTL) – Offset 930

Same definition as IPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (IPPLC2FMT) – Offset 934

Same definition as IPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC2LLPL) – Offset 938

Same definition as IPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC2LLPU) – Offset 93c

Same definition as IPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (IPPLC3CTL) – Offset 940

Same definition as IPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (IPPLC3FMT) – Offset 944

Same definition as IPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link

Position Lower (IPPLC3LLPL) – Offset 948

Same definition as IPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC3LLPU) – Offset 94c

Same definition as IPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (IPPLC4CTL) – Offset 950

Same definition as IPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (IPPLC4FMT) – Offset 954

Same definition as IPPLC0FMT

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC2LDPL) – Offset 838

Same definition as IPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC2LDPU) – Offset 83c

Same definition as IPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC3LLPL) – Offset 840

Same definition as IPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC3LLPU) – Offset 844

Same definition as IPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC3LDPL) – Offset 848

Same definition as IPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC3LDPU) – Offset 84c

Same definition as IPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC4LLPL) – Offset 850

Same definition as IPPHC0LLPL.

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC4LLPL) – Offset 958

Same definition as IPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC4LLPU) – Offset 95c

Same definition as IPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (IPPLC5CTL) – Offset 960

Same definition as IPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (IPPLC5FMT) – Offset 964

Same definition as IPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC5LLPL) – Offset 968

Same definition as IPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC5LLPU) – Offset 96c

Same definition as IPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (IPPLC6CTL) – Offset 970

Same definition as IPPLC0CTL

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC4LLPU) – Offset 854

Same definition as IPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC4LDPL) – Offset 858

Same definition as IPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC4LDPU) – Offset 85c

Same definition as IPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC5LLPL) – Offset 860

Same definition as IPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC5LLPU) – Offset 864

Same definition as IPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC5LDPL) – Offset 868

Same definition as IPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC5LDPU) – Offset 86c

Same definition as IPPHC0LDPU.

Input/Output Processing Pipe's Link Connection x Format (IPPLC6FMT) – Offset 974

Same definition as IPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC6LLPL) – Offset 978

Same definition as IPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC6LLPU) – Offset 97c

Same definition as IPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (OPPLC0CTL) – Offset 980

SRST bit is not affected by stream reset.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:20	0h	RW	

Bit Range	Default	Access	Field Name and Description
			Stream Number (STRM) This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19:2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1	0b	RW/V	**Stream Run (RUN)** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.

Bit Range	Default	Access	Field Name and Description
0	0b	RW/V	**Stream Reset (SRST)** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

Input/Output Processing Pipe's Link Connection x Format (OPPLC0FMT) – Offset 984

Bit Range	Default	Access	Field Name and Description
14	0b	RW	**Sample Base Rate (BASE)** 0=48 kHz 1=44.1 kHz

Bit Range	Default	Access	Field Name and Description
13:11	0h	RW	**Sample Base Rate Multiple (MULT)** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h	RW	**Sample Base Rate Divisor (DIV)** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
6:4	0h	RW	**Bits per Sample (BITS)** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h	RW	**Number of Channels (CHAN)** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC0LLPL) – Offset 988

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Linear Link Position Lower (LLPL)** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC0LLPU) – Offset 98c

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Linear Link Position Upper (LLPU)** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

Input/Output Processing Pipe's Link Connection x Control (OPPLC1CTL) – Offset 990

Same definition as OPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (OPPLC1FMT) – Offset 994

Same definition as OPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC1LLPL) – Offset 998

Same definition as OPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC1LLPU) – Offset 99c

Same definition as OPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (OPPLC2CTL) – Offset 9a0

Same definition as OPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (OPPLC2FMT) – Offset 9a4

Same definition as OPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC2LLPL) – Offset 9a8

Same definition as OPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC2LLPU) – Offset 9ac

Same definition as OPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (OPPLC3CTL) – Offset 9b0

Same definition as OPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (OPPLC3FMT) – Offset 9b4

Same definition as OPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC3LLPL) – Offset 9b8

Same definition as OPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC3LLPU) – Offset 9bc

Same definition as OPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (OPPLC4CTL) – Offset 9c0

Same definition as OPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (OPPLC4FMT) – Offset 9c4

Same definition as OPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC4LLPL) – Offset 9c8

Same definition as OPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC4LLPU) – Offset 9cc

Same definition as OPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (OPPLC5CTL) – Offset 9d0

Same definition as OPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (OPPLC5FMT) – Offset 9d4

Same definition as OPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC5LLPL) – Offset 9d8

Same definition as OPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC5LLPU) – Offset 9dc

Same definition as OPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (OPPLC6CTL) – Offset 9e0

Same definition as OPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (OPPLC6FMT) – Offset 9e4

Same definition as OPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC6LLPL) – Offset 9e8

Same definition as OPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC6LLPU) – Offset 9ec

Same definition as OPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (OPPLC7CTL) – Offset 9f0

Same definition as OPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (OPPLC7FMT) – Offset 9f4

Same definition as OPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC7LLPL) – Offset 9f8

Same definition as OPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link

Position Upper (OPPLC7LLPU) – Offset 9fc

Same definition as OPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (OPPLC8CTL) – Offset a00

Same definition as OPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (OPPLC8FMT) – Offset a04

Same definition as OPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC8LLPL) – Offset a08

Same definition as OPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC8LLPU) – Offset a0c

Same definition as OPPLC0LLPU

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC7LLPL) – Offset 4a10

Same definition as IPPHC0LLPL

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC7LLPU) – Offset 4a14

Same description as IPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC7LDPL) – Offset 4a18

Same description as IPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC6LLPL) – Offset 870

Same definition as IPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC6LLPU) – Offset 874

Same definition as IPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC6LDPL) – Offset 878

Same definition as IPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC6LDPU) – Offset 87c

Same definition as IPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC0LLPL) – Offset 880

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Linear Link Position Lower (LLPL)** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC0LLPU) – Offset 884

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Linear Link Position Upper (LLPU)** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC0LDPL) – Offset 888

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Linear DMA Position Lower (LDPL)** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC7LDPU) – Offset 4a1c

Same description as IPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC8LLPL) – Offset 4a20

Same description as IPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC8LLPU) – Offset 4a24

Same description as IPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC8LDPL) – Offset 4a28

Same description as IPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC8LDPU) – Offset 4a2c

Same description as IPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC9LLPL) – Offset 4a30

Same description as IPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC9LLPU) – Offset 4a34

Same description as IPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC0LDPU) – Offset 88c

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Linear DMA Position Offset Upper (LDPU)** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC1LLPL) – Offset 890

Same definition as OPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC1LLPU) – Offset 894

Same definition as OPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC1LDPL) – Offset 898

Same definition as OPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC1LDPU) – Offset 89c

Same definition as OPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC2LLPL) – Offset 8a0

Same definition as OPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC2LLPU) – Offset 8a4

Same definition as OPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC9LDPL) – Offset 4a38

Same description as IPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC9LDPU) – Offset 4a3c

Same description as IPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC10LLPL) – Offset 4a40

Same description as IPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC10LLPU) – Offset 4a44

Same description as IPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC10LDPL) – Offset 4a48

Same description as IPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC10LDPU) – Offset 4a4c

Same description as IPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC11LLPL) – Offset 4a50

Same description as IPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC11LLPU) – Offset 4a54

Same description as IPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC11LDPL) – Offset 4a58

Same description as IPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC11LDPU) – Offset 4a5c

Same description as IPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC12LLPL) – Offset 4a60

Same description as IPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC12LLPU) – Offset 4a64

Same description as IPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC12LDPL) – Offset 4a68

Same description as IPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA

Position Upper (IPPHC12LDPU) – Offset 4a6c

Same description as IPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC13LLPL) – Offset 4a70

Same description as IPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC13LLPU) – Offset 4a74

Same description as IPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC13LDPL) – Offset 4a78

Same description as IPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC13LDPU) – Offset 4a7c

Same description as IPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC14LLPL) – Offset 4a80

Same description as IPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC14LLPU) – Offset 4a84

Same description as IPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC14LDPL) – Offset 4a88

Same description as IPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC14LDPU) – Offset 4a8c

Same description as IPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC9LLPL) – Offset 4a90

Same description as OPHC0LLPL

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC9LLPU) – Offset 4a94

Same description as OPHC0LLPU

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC9LDPL) – Offset 4a98

Same description as OPHC0LDPL

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC9LDPU) – Offset 4a9c

Same description as OPHC0LDPU

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC10LLPL) – Offset 4aa0

Same description as OPHC0LLPL

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC10LLPU) – Offset 4aa4

Same description as OPHC0LLPU

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC10LDPL) – Offset 4aa8

Same description as OPHC0LDPL

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC10LDPU) – Offset 4aac

Same description as OPHC0LDPU

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC11LLPL) – Offset 4ab0

Same description as OPHC0LLPL

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC11LLPU) – Offset 4ab4

Same description as OPHC0LLPU

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC11LDPL) – Offset 4ab8

Same description as OPHC0LDPL

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC11LDPU) – Offset 4abc

Same description as OPHC0LDPU

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC12LLPL) – Offset 4ac0

Same description as OPHC0LLPL

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC12LLPU) – Offset 4ac4

Same description as OPHC0LLPU

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC12LDPL) – Offset 4ac8

Same description as OPHC0LDPL

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC12LDPU) – Offset 4acc

Same description as OPHC0LDPU

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC13LLPL) – Offset 4ad0

Same description as OPHC0LLPL

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC13LLPU) – Offset 4ad4

Same description as OPHC0LLPU

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC13LDPL) – Offset 4ad8

Same description as OPHC0LDPL

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC13LDPU) – Offset 4adc

Same description as OPHC0LDPU

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC14LLPL) – Offset 4ae0

Same description as OPHC0LLPL

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC14LLPU) – Offset 4ae4

Same description as OPHC0LLPU

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC14LDPL) – Offset 4ae8

Same description as OPHC0LDPL

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC14LDPU) – Offset 4aec

Same description as OPHC0LDPU

Input/Output Processing Pipe's Link Connection x Control (IPPLC7CTL) – Offset 4af0

Same definition as IPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format

(IPPLC7FMT) – Offset 4af4

Same definition as IPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC7LLPL) – Offset 4af8

Same definition as IPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC7LLPU) – Offset 4afc

Same definition as IPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (IPPLC8CTL) – Offset 4b00

Same definition as IPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (IPPLC8FMT) – Offset 4b04

Same definition as IPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC8LLPL) – Offset 4b08

Same definition as IPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC8LLPU) – Offset 4b0c

Same definition as IPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (IPPLC9CTL) – Offset 4b10

Same definition as IPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (IPPLC9FMT) – Offset 4b14

Same definition as IPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC9LLPL) – Offset 4b18

Same definition as IPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC9LLPU) – Offset 4b1c

Same definition as IPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (IPPLC10CTL) – Offset 4b20

Same definition as IPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (IPPLC10FMT) – Offset 4b24

Same definition as IPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC10LLPL) – Offset 4b28

Same definition as IPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC10LLPU) – Offset 4b2c

Same definition as IPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (IPPLC11CTL) – Offset 4b30

Same definition as IPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (IPPLC11FMT) – Offset 4b34

Same definition as IPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC11LLPL) – Offset 4b38

Same definition as IPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC11LLPU) – Offset 4b3c

Same definition as IPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (IPPLC12CTL) – Offset 4b40

Same definition as IPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (IPPLC12FMT) – Offset 4b44

Same definition as IPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC12LLPL) – Offset 4b48

Same definition as IPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC12LLPU) – Offset 4b4c

Same definition as IPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (IPPLC13CTL) – Offset 4b50

Same definition as IPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (IPPLC13FMT) – Offset 4b54

Same definition as IPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC13LLPL) – Offset 4b58

Same definition as IPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC13LLPU) – Offset 4b5c

Same definition as IPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (IPPLC14CTL) – Offset 4b60

Same definition as IPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (IPPLC14FMT) – Offset 4b64

Same definition as IPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC14LLPL) – Offset 4b68

Same definition as IPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC14LLPU) – Offset 4b6c

Same definition as IPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (OPPLC9CTL) – Offset 4b70

Same definition as OPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (OPPLC9FMT) – Offset 4b74

Same definition as OPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC9LLPL) – Offset 4b78

Same definition as OPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link

Position Upper (OPPLC9LLPU) – Offset 4b7c

Same definition as OPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (OPPLC10CTL) – Offset 4b80

Same definition as OPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (OPPLC10FMT) – Offset 4b84

Same definition as OPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC10LLPL) – Offset 4b88

Same definition as OPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC10LLPU) – Offset 4b8c

Same definition as OPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (OPPLC11CTL) – Offset 4b90

Same definition as OPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (OPPLC11FMT) – Offset 4b94

Same definition as OPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC11LLPL) – Offset 4b98

Same definition as OPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC11LLPU) – Offset 4b9c

Same definition as OPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (OPPLC12CTL) – Offset 4ba0

Same definition as OPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (OPPLC12FMT) – Offset 4ba4

Same definition as OPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC12LLPL) – Offset 4ba8

Same definition as OPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC12LLPU) – Offset 4bac

Same definition as OPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (OPPLC13CTL) – Offset 4bb0

Same definition as OPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (OPPLC13FMT) – Offset 4bb4

Same definition as OPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC13LLPL) – Offset 4bb8

Same definition as OPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC13LLPU) – Offset 4bbc

Same definition as OPPLC0LLPU

Input/Output Processing Pipe's Link Connection x Control (OPPLC14CTL) – Offset 4bc0

Same definition as OPPLC0CTL

Input/Output Processing Pipe's Link Connection x Format (OPPLC14FMT) – Offset 4bc4

Same definition as OPPLC0FMT

Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC14LLPL) – Offset 4bc8

Same definition as OPPLC0LLPL

Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC14LLPU) – Offset 4bcc

Same definition as OPPLC0LLPU

Multiple Links Capability Header (MLCH) – Offset c00

This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Bit Range	Default	Access	Field Name and Description
31:28	0h	RW/L	**Capability Version (VER)** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1.
27:16	002h	RW/L	**Capability Identifier (ID)** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1.

Bit Range	Default	Access	Field Name and Description
15:0	0800h	RW/L	**Next Capability Pointer (PTR)** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. Point to Processing Pipe capability. Locked when FNCFG.BCLD = 1.

Multiple Links Capability Declaration (MLCD) – Offset c04

Bit Range	Default	Access	Field Name and Description
30:4	-	-	**Reserved**
3:0	1h	RO	**Link Count (LCOUNT)** Indicates the number of links. Up to 15 links can be supported. A '0' indicates 1 link, and '1110' indicates 15 links. Note: '1111' is reserved. Note that this Link Count is the cumulative total number of links where the links can be heterogeneous. This field is hardcoded to parameter LNKC-1.

Link x Capabilities (LCAP0) – Offset c40

This register resides in Primary well (always on), or resides in Primary well (gated) with state retention, and reset by platform reset.

Bit Range	Default	Access	Field Name and Description
31:28	0h	RW/L	**Audio Link Type (ALT)** Indicates which Link Type this link belongs to. 0001-1111 = Reserved 0000 = Intel HD Audio Link Locked when FNCFG.BCLD = 1.
27:26	-	-	**Reserved**
25:24	0h	RW/L	**Number of Serial Data Out Signals (NSDO)** 00b indicates that the Intel HD Audio controller supports one Serial Data Output signal. Locked when FNCFG.BCLD = 1.
23:6	-	-	**Reserved**
5	0h	RW/L	**192 MHz Supported (S192)** Indicates 192 MHz clock is supported. Locked when FNCFG.BCLD = 1.
4	0h	RW/L	**96 MHz Supported (S96)** Indicates 96 MHz clock is supported. Locked when FNCFG.BCLD = 1.
3	0h	RW/L	**48 MHz Supported (S48)** Indicates 48 MHz clock is supported. Locked when FNCFG.BCLD = 1.
2	1h	RW/L	**24 MHz Supported (S24)** Indicates 24 MHz clock is supported. Locked when FNCFG.BCLD = 1.

Bit Range	Default	Access	Field Name and Description
1	1h	RW/L	**12 MHz Supported (S12)** Indicates 12 MHz clock is supported. Locked when FNCFG.BCLD = 1.
0	1h	RW/L	**6 MHz Supported (S6)** Indicates 6 MHz clock is supported. Locked when FNCFG.BCLD = 1.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC2LDPL) – Offset 8a8

Same definition as OPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC2LDPU) – Offset 8ac

Same definition as OPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC3LLPL) – Offset 8b0

Same definition as OPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC3LLPU) – Offset 8b4

Same definition as OPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC3LDPL) – Offset 8b8

Same definition as OPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC3LDPU) – Offset 8bc

Same definition as OPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC4LLPL) – Offset 8c0

Same definition as OPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC4LLPU) – Offset 8c4

Same definition as OPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC4LDPL) – Offset 8c8

Same definition as OPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC4LDPU) – Offset 8cc

Same definition as OPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC5LLPL) – Offset 8d0

Same definition as OPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC5LLPU) – Offset 8d4

Same definition as OPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC5LDPL) – Offset 8d8

Same definition as OPPHC0LDPL.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC5LDPU) – Offset 8dc

Same definition as OPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC6LLPL) – Offset 8e0

Same definition as OPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC6LLPU) – Offset 8e4

Same definition as OPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC6LDPL) – Offset 8e8

Same description as OPHC0LDPL

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC6LDPU) – Offset 8ec

Same definition as OPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC7LLPL) – Offset 8f0

Same definition as OPPHC0LLPL.

Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC7LLPU) – Offset 8f4

Same definition as OPPHC0LLPU.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC7LDPL) – Offset 8f8

Same definition as OPPHC0LDPL.

Link 0 Control (LCTL0) – Offset c44

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
23	0b	RO/V	**Current Power Active (CPA)** This value changes to the value set by SPA when the power of the link has reached that state. Software sets SPA, then monitors CPA to know when the link has changed state.
22:17	-	-	**Reserved**
16	1b	RW	**Set Power Active (SPA)** Software sets this bit to '1' to turn the link on (provided CRSTB = 1), and clears it to '0' when it wishes to turn the link off. When CPA matches the value of this bit, the achieved power state has been reached. Software is expected to wait for CPA to match SPA before it can program SPA again. Any deviation may result in undefined behaviour
15:4	-	-	**Reserved**
3:0	0h	RW	**Set Clock Frequency (SCF)** Indicates the frequency that software wishes the link to run at. Changing this value to a value not supported by Link Capabilities shall result in indeterminate results. The possible encodings are: 0000: 6 MHz 0001: 12 MHz 0010: 24 MHz 0011: 48 MHz 0100: 96 MHz 0110-1111: Reserved When the frequency changes, CCF shall change to SCF, indicating to software that the frequency change occurred. Software is expepcted to wait for CCF to match SCF, indicating that the frequency change occurred.

Link 1 Control (LCTL1) – Offset c84

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RO/V	**Current Power Active (CPA)** This value changes to the value set by SPA when the power of the link has reached that state. Software sets SPA, then monitors CPA to know when the link has changed state.
22:17	-	-	**Reserved**
16	1b	RW	**Set Power Active (SPA)** Software sets this bit to '1' to turn the link on (provided CRSTB = 1), and clears it to '0' when it wishes to turn the link off. When CPA matches the value of this bit, the achieved power state has been reached. Software is expected to wait for CPA to match SPA before it can program SPA again. Any deviation may result in undefined behaviour
15:4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3:0	0h	RW	**Set Clock Frequency (SCF)** Indicates the frequency that software wishes the link to run at. Changing this value to a value not supported by Link Capabilities shall result in indeterminate results. The possible encodings are: Encoding Frequency 0000 6 MHz 0001 12 MHz 0010 24 MHz 0011 48 MHz 0100 96 MHz 0101 Reserved for 192 MHz 0110-1111 Reserved When the frequency changes, CCF shall change to SCF, indicating to software that the frequency change occurred. Software is expepcted to wait for CCF to match SCF, indicating that the frequency change occured.

Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC7LDPU) – Offset 8fc

Same definition as OPPHC0LDPU.

Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC8LLPL) – Offset 900

Same definition as OPPHC0LLPL.

High Definition Audio (D31:F3) PCI Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	Vendor Identification (VID)	8086h
2h	2	Device ID (DID)	XXXXh
4h	2	Command (CMD)	0h
6h	2	Status (STS)	10h
8h	1	Revision Identification (RID)	0h
9h	1	Programming Interface (PI)	0h
ah	1	Sub Class Code (SCC)	3h
bh	1	Base Class Code (BCC)	4h
ch	1	Cache Line Size (CLS)	0h
dh	1	Latency Timer (LT)	0h
eh	1	Header Type (HTYPE)	0h
10h	4	Intel HD Audio Base Lower Address (HDALBA)	4h
14h	4	Intel HD Audio Base Upper Address (HDAUBA)	0h
18h	4	Shadowed PCI Configuration Lower Base Address (SPCLBA)	4h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1ch	4	Shadowed PCI Configuration Upper Base Address (SPCUBA)	0h
20h	4	Audio DSP Lower Base Address (ADSPLBA)	4h
24h	4	Audio DSP Upper Base Address (ADSPUBA)	0h
2ch	2	Subsystem Vendor ID (SVID)	0h
2eh	2	Subsystem ID (SID)	0h
34h	1	Capability Pointer (CAPPTR)	50h
3ch	1	Interrupt Line (INTLN)	0h
3dh	1	Interrupt Pin (INTPN)	1h
44h	4	Power Gating Control (PGCTL)	0h
48h	4	Clock Gating Control (CGCTL)	1B01F9h
50h	2	PCI Power Management Capability ID (PID)	6001h
52h	2	Power Management Capabilities (PC)	C043h
54h	4	Power Management Control And Status (PCS)	8h
62h	2	Message Signal Interrupt Message Control (MMC)	80h
64h	4	MSI Message Lower Address (MMLA)	0h
68h	4	MSI Message Upper Address (MMUA)	0h
6ch	2	MSI Message Data (MMD)	0h
70h	2	PCI Express Capability ID (PXID)	10h
72h	2	PCI Express Capabilities (PXC)	91h
74h	4	Device Capabilities (DEVCAP)	10000000h
78h	2	Device Control (DEVC)	2800h
7ah	2	Device Status (DEVS)	10h

Vendor Identification (VID) – Offset 0

Bit Range	Default	Access	Field Name and Description
15:0	8086h	RO	**Vendor ID (VID)** Indicates that Intel is the vendor.

Device ID (DID) – Offset 2

This register is not affected by D3HOT to D0 reset or FLR.

Bit Range	Default	Access	Field Name and Description
15:0	See Description	RO/V	**Device ID (DID)** Indicates the device ID. Refer to the Device and Revision ID Table in Volume 1 for default value.

Command (CMD) – Offset 4

Bit Range	Default	Access	Field Name and Description
14:11	-	-	**Reserved**
10	0b	RW	**Interrupt Disable (ID)** Enables the device to assert an INTx#. When set, the Intel(r) HD Audio controller's INTx# signal will be de-asserted. When cleared, the INTx# signal may be asserted. Note that this bit does not affect the generation of MSI's.
9	0b	RO	**Fast Back to Back Enable (FBE)** Not implemented. Hardwired to 0.
8	0b	RW	**SERR Enable (SEN)** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
7	0b	RO	**Wait Cycle Control (WCC)** Not implemented. Hardwired to 0.

Bit Range	Default	Access	Field Name and Description
6	0b	RW	**Parity Error Response (PER)** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
5	0b	RO	**VGA Palette Snoop (VPS)** Not implemented. Hardwired to 0.
4	0b	RO	**Memory Write and Invalidate Enable (MWI)** Not implemented. Hardwired to 0.
3	0b	RO	**Special Cycle Enable (SCE)** Not implemented. Hardwired to 0.
2	0b	RW	**Bus Master Enable (BME)** 1 = Enable, 0 = Disable. Controls standard PCI Express bus mastering capabilities for Memory and IO, reads and writes. Note that this also controls MSI generation since MSI are essentially Memory writes.
1	0b	RW	**Memory Space Enable (MSE)** When set, enables memory space accesses to the Intel HD Audio controller.
0	0b	RO	**I/O Space (IOS)** The Intel HD Audio controller does not implement IO Space, therefore this bit is hardwired to 0.

Status (STS) – Offset 6

Bit Range	Default	Access	Field Name and Description
15	0b	RO	**Detected Parity Error (DPE)** Not implemented. Hardwired to 0.
14	0b	RO	**SERR# Status (SERRS)** Not implemented. Hardwired to 0.
13	0b	RW/1C/V	**Received Master Abort (RMA)** If the completion status received from IOSF is UR, this bit is set. SW writes a 1 to this bit to clear it.

Bit Range	Default	Access	Field Name and Description
12	0b	RW/1C/V	**Received Target Abort (RTA)** If the completion status received from IOSF is CA, this bit is set. SW writes a 1 to this bit to clear it.
11	0b	RO	**Signaled Target-Abort (STA)** Not implemented. Hardwired to 0.
10:9	00b	RO	**DEVSEL# Timing Status (DEVT)** Does not apply. Hardwired to 0.
8	0b	RO	**Master Data Parity Error (MDPE)** Not implemented. Hardwired to 0.
7	0b	RO	**Fast Back to Back Capable (FBC)** Does not apply. Hardwired to 0.
6	-	-	**Reserved**
5	0b	RO	**66 MHz Capable (C66)** Does not apply. Hardwired to 0.
4	1b	RO	**Capabilities List Exists (CLIST)** Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	0b	RO/V	**Interrupt Status (IS)** Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted. This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register). Note that this bit is not set by an MSI.
2:0	-	-	**Reserved**

Revision Identification (RID) – Offset 8

This register is not affected by D3HOT to D0 reset or FLR

Bit Range	Default	Access	Field Name and Description
7:0	See Description	RO/V	**Revision ID (RID)** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

Programming Interface (PI) – Offset 9

This register is not affected by D3HOT to D0 reset or FLR

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW/L	**Programming Interface (PI)** Intel HD Audio subsystem. Locked when FNCFG.BCLD = 1.

Sub Class Code (SCC) – Offset a

This register is not affected by D3HOT to D0 reset or FLR

Bit Range	Default	Access	Field Name and Description
7:0	03h	RW/L	**Sub Class Code (SCC)** This indicates the device is an Intel HD Audio device, in the context of a multimedia device. Locked when FNCFG.BCLD = 1.

Base Class Code (BCC) – Offset b

This register is not affected by D3HOT to D0 reset or FLR

Bit Range	Default	Access	Field Name and Description
7:0	04h	RW/L	**Base Class Code (BCC)** This register indicates that the function implements a multimedia device. Locked when FNCFG.BCLD = 1.

Cache Line Size (CLS) – Offset c

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**Cache Line Size (CLS)** Doesn't apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the PCH.

Latency Timer (LT) – Offset d

RO. Hardwired to 00

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW/L	**Latency Timer (LT)** Doesn t apply to PCI Express. RO as 00h if PCI Express. If configured to appear as PCI device, maintain RW for Legacy PCI SW compliancy. Locked when FNCFG.HDASPCID = 0

Header Type (HTYPE) – Offset e

Bit Range	Default	Access	Field Name and Description
7	0h	RW/L	**Multi Function Device (MFD)** Value of 0 indicates a single function device. Value of 1 indicates a multi function device. Locked when FNCFG.BCLD = 1.
6:0	00h	RO	**Header Type (HTYPE)** Implements Type 0 Configuration header.

Intel HD Audio Base Lower Address (HDALBA) – Offset 10

This BAR creates a selected size of memory space to signify the base address of the Intel HD Audio memory mapped configuration registers depending on implementation.

Bit Range	Default	Access	Field Name and Description
31:14	0h	RW	**Lower Base Address (LBA)** Base address for the Intel HD Audio subsystem s memory mapped configuration registers. 16 Kbytes are requested by hardwiring bits 13:4 to 0 s.
13:4	-	-	**Reserved**
3	0b	RO	**Prefetchable (PREF)** Indicates that this BAR is NOT pre-fetchable.
2:1	10b	RO	**Address Range (ADDRNG)** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0b	RO	**Space Type (SPTYP)** Indicates that this BAR is located in memory space.

Intel HD Audio Base Upper Address (HDAUBA) – Offset 14

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Intel HD Audio Upper Base Address (UBA)** Upper 32 bits of the Base address for the Intel(r) HD Audio controller's memory mapped configuration registers.

Shadowed PCI Configuration Lower Base Address (SPCLBA) – Offset 18

Bit Range	Default	Access	Field Name and Description
31:12	0h	RW/L	**Lower Base Address (LBA)** Base address for the PCI Configuration register shadowed to memory mapped. 4 KB is requested by hardwiring bits 11:4 to 0 s. Locked when PCICFGCTL0.SPCBAD = 1.
11:4	-	-	**Reserved**
3	0b	RO	**Prefetchable (PREF)** Indicates that this BAR is NOT pre-fetchable.
2:1	10b	RO/V	**Address Range (ADDRNG)** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0b	RO	**Space Type (SPTYP)** Indicates that this BAR is located in memory space.

Shadowed PCI Configuration Upper Base Address (SPCUBA) – Offset 1c

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW/L	**Upper Base Address (UBA)** Upper 32 bits of the Base address for the PCI Configuration register shadowed to memory mapped. Locked when PCICFGCTL0.SPCBAD = 1.

Audio DSP Lower Base Address (ADSPLBA) – Offset 20

This BAR creates a selected size of memory space to signify the base address of the Audio DSP memory mapped configuration registers depending on implementation.

The number of LBA bits in this register is depending on the size of the memory window implemented.

Bit Range	Default	Access	Field Name and Description
31:20	0h	RW	**Lower Base Address (LBA)** Base address for the Audio DSP memory mapped configuration registers.
19:4	0h	RO	**Hardwired to 0's (RSVD)**
3	0b	RO	**Prefetchable (PREF)** Indicates that this BAR is NOT pre-fetchable.
2:1	10b	RO	**Address Range (ADDRNG)** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0b	RO	**Space Type (SPTYP)** Indicates that this BAR is located in memory space.

Audio DSP Upper Base Address (ADSPUBA) – Offset 24

Upper Base address for the Audio DSP memory mapped configuration registers.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Upper Base Address (UBA)** Upper 32 bits of the Base address for the Audio DSP memory mapped configuration registers.

Subsystem Vendor ID (SVID) – Offset 2c

This register should be implemented for any function that could be instantiated more than once in a given system, for example, a system with 2 audio subsystems, one down on the motherboard and the other plugged into a PCI expansion slot, should have the SVID register implemented. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one

audio subsystem from the other(s).

Software (BIOS) will write the value to this register. After that,

the value can be read, but writes to the register will have no effect.

The write to this register should be combined with the write to the

SID to create one 32-bit write.

This register is not affected by D3HOT to D0 reset or FLR

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW/L	**SVID (SVID)** These RW bits have no functionality. Locked when FNCFG.BCLD = 1.

Subsystem ID (SID) – Offset 2e

This register should be implemented for any function that could be

instantiated more than once in a given system, for example, a system

with 2 audio subsystems, one down on the motherboard and the other

plugged into a PCI expansion slot. The SID register, in combination

with the Subsystem Vendor ID register make it possible for the

operating environment to distinguish one audio subsystem from the

other(s).

Software (BIOS) will write the value to this register. After that,

the value can be read, but writes to the register will have no effect.

The write to this register should be combined with the write to the

SVID to create one 32-bit write.

This register is not affected by D3HOT to D0 reset or FLR.

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW/L	**SID (SID)** These RW bits have no functionality. Locked when FNCFG.BCLD = 1.

Capability Pointer (CAPPTR) – Offset 34

Bit Range	Default	Access	Field Name and Description
7:0	50h	RO	**Capability Pointer (CAPPTR)** Indicates that the first capability pointer offset is offset 50h (Power Management Capability).

Interrupt Line (INTLN) – Offset 3c

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**Interrupt Line (INTLN)** Hardware does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

Interrupt Pin (INTPN) – Offset 3d

This register is not affected by D3HOT to D0 reset or FLR.

Bit Range	Default	Access	Field Name and Description
6:4	-	-	**Reserved**
3:0	1h	RW/L	**Interrupt Pin (INTPN)** Identifies the interrupt pin the function uses.{br]0h: No interrupt pin 1h: INTA 2h: INTB 3h: INTC 4h: INTD 5h - Fh: reserved Locked when FNCFG.BCLD = 1.

Power Gating Control (PGCTL) – Offset 44

D3PGD are meant for the Intel HD Audio driver software to control whether the Intel HD Audio subsystem should be power gated or not in D3.

Note that the power gating will only be initiated when out of platform reset, if conditions are met.

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4	0b	RW	**LP SRAM Retention Module Disable (LSRMD)** Register is used to disable the LP SRAM retention mode capbility of the L2 SRAMs.
3	0b	RW	**HP SRAM Retention Module Disable (HSRMD)** Register is used to disable the HP SRAM retention mode capbility of the L2 SRAMs.
2	-	-	**Reserved**
1	0b	RW	**D3 Power Gating Disable (CTLPGD)** Register is used to disable the power gating capbility during D3 state.
0	0b	RW	**Low Power Audio Power Gating Disable (LPAPGD)** Register is used to disable the power gating capbility of the Primary well (gated-controller) domain.

Clock Gating Control (CGCTL) – Offset 48

The trunk clock gating enable and local clock gating enables are meant for BIOS or driver to enable or disable the HW capability to detect idle condition and clock gate accordingly. HW should treat these clock gate enable register bits as 0 if FNCFG.CGD = 1.

Note that the clock gating will only be initiated when out of platform reset, if conditions are met.

Bit Range	Default	Access	Field Name and Description
30:21	-	-	**Reserved**
20	1b	RW	**IOSF Sideband Trunk Gate Enable (IOSFSTCGE)** Enable IOSF trunk clock gating functionality on IOSF interface. When set, IOSF Sideband interface clock request can de-assert to allow trunk clock gating.
19	1b	RW	**IOSF Backbone Trunk Gate Enable (IOSFBTCGE)** Enable IOSF trunk clock gating functionality on IOSF interface. When set, IOSF Primary interface clock request can de-assert to allow trunk clock gating.
18	-	-	**Reserved**
17	1b	RW	**XTAL Oscillator Trunk Clock Gating Enable (XOTCGE)** Set to 1 to enable trunk clock gating. If enabled, HW will trunk clock gate when no logic are using this clock (i.e. all local clock gating condition is true).
16	1b	RW	**Audio PLL Trunk Clock Gating Enable (APTCGE)** Set to 1 to enable trunk clock gating. If enabled, HW will trunk clock gate when no logic are using this clock (i.e. all local clock gating condition is true).
15:9	-	-	**Reserved**
8	1b	RW	**IOSF Sideband Dynamic Clock Gate Enable (IOSFSDCGE)** Enable IOSF dynamic clock gating functionality inside IOSF interface. When set, IOSF Sideband clock gating functionality is enabled.
7	1b	RW	**IOSF Backbone Dynamic Clock Gate Enable (IOSFBDCGE)** Enable IOSF dynamic clock gating functionality inside IOSF interface. When set, IOSF Primary clock gating functionality is enabled.

Bit Range	Default	Access	Field Name and Description
6	1b	RW	**Miscellaneous Backbone Dynamic Clock Gating Enable (MISCBDCGE)** This controls dynamic clock gating of backbone (Command/data) clocks to the rest of the Intel HD Audio controller (i.e. other than the IOSF, Input DMA engine, and Output DMA engine). When this bit is asserted, dynamic clock gating logic is enabled for backbone clocks to the rest of the Intel HD Audio controller.
5	1b	RW	**IDMA Backbone Dynamic Clock Gating Enable (IDMABDCGE)** This controls dynamic clock gating of backbone (Command/data) clocks to each Input DMA engine. When this bit is asserted, dynamic clock gating logic is enabled for backbone clocks to each Input DMA engine.
4	1b	RW	**ODMA Backbone Dynamic Clock Gating Enable (ODMABDCGE)** This controls dynamic clock gating of backbone (Command/data) clocks to each Output DMA engines. When this bit is asserted, dynamic clock gating logic is enabled for backbone clocks to each Output DMA engine.
3	1b	RW	**HD Audio Link Dynamic Clock Gating Enable (HDALDCGE)** This controls dynamic clock gating of bitclk to Link Layer and each Input/Output DMA engine. When this bit is asserted, dynamic clock gating logic is enabled for bitclk.
2:1	-	-	**Reserved**
0	1b	RW	**Memory Dynamic Clock Gating Enable (MEMDCGE)** When set to 1, it allows HW to automatically detect for idle condition and clock gate Memory block. When clear to 0, it disables this HW auto detect idle clock gating.

PCI Power Management Capability ID (PID) – Offset 50

Bit Range	Default	Access	Field Name and Description
15:8	60h	RW/L	**Next Capability (NEXT)** Points to the next capability structure (MSI). Locked when FNCFG.BCLD = 1.
7:0	01h	RO	**Cap ID (CAP)** Indicates that this pointer is a PCI power management capability

Power Management Capabilities (PC) – Offset 52

Bit Range	Default	Access	Field Name and Description
15:11	18h	RW/L	**PME_Support (PMES)** Indicates PME# can be generated from D3 and D0 states. Programmable by BIOS for the option to declare SUS well wake is supported or not: 19h (SUS well wake supported) or 09h (SUS well wake not supported). Locked when FNCFG.BCLD = 1
10	0b	RO	**D2_Support (D2S)** The D2 state is not supported.
9	0b	RO	**D1_Support (D1S)** The D1 state is not supported.

Bit Range	Default	Access	Field Name and Description
8:6	001b	RW/L	**Aux_Current (AC)** Reports 55 mA maximum Suspend well current required when in the D3cold state. Programmable by BIOS for the option to declare SUS well wake is supported or not: 001b (SUS well wake supported) or 000b (SUS well wake not supported). Locked when FNCFG.BCLD = 1.
5	0b	RO	**Device Specific Initialization (DSI)** Indicates that no device-specific initialization is required.
4	-	-	**Reserved**
3	0b	RO	**PME Clock (PMEC)** Does not apply. Hardwired to 0.
2:0	011b	RW/L	**Version (VS)** Indicates support for Revision 1.2 of the PCI Power Management Specification. Programmable by BIOS to older revision if compatibility issue is found. Locked when FNCFG.BCLD = 1.

Power Management Control And Status (PCS) – Offset 54

PMES and PMEE bits reside in Resume well, and reset by resume reset.

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO	**Data (DT)** Does not apply. Hardwired to 0's.
23	0b	RO	**Bus Power/Clock Control Enable (BPCCE)** Does not apply. Hardwired to0.
22	0b	RO	**B2/B3 Support (B23)** Does not apply. Hardwired to 0.

Bit Range	Default	Access	Field Name and Description
21:16	-	-	**Reserved**
15	0b	RW/1C/V	**PME Status (PMES)** This bit is set when the Intel HD Audio controller would normally assert the PME# signal independent of the state of the PME bit. This bit is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
14:9	-	-	**Reserved**
8	0b	RW	**PME Enable (PMEE)** When set, and if corresponding PMES is also set, the Intel HD Audio subsystem send PME to PMC. This bit is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
7:4	-	-	**Reserved**
3	1b	RW/L	

Bit Range	Default	Access	Field Name and Description
			No Soft Reset (NSR) When set (1), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When clear (0), devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. Locked when FNCFG.BCLD = 1.
2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1:0	00b	RW	**Power State (PS)** This field is used both to determine the current power state of the HD Audio subsystem and to set a new power state. 00: D0 state 11: D3HOT state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3HOT states, the HD Audio subsystem's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. When software changes this value from the D3HOT state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.

Message Signal Interrupt Message Control (MMC) – Offset 62

Bit Range	Default	Access	Field Name and Description
14:8	-	-	**Reserved**
7	1b	RO	**64b Address Capability (ADD64)** RO. Hardwired to 1. Indicates the ability to generate a 64-bitmessage address
6:4	000b	RO	**Multiple Message Enable (MME)** Normally this is a R/W register. Howeversince only 1 message is supported, these bits are hardwired to 000 = 1 message.
3:1	000b	RO	**Multiple Message Capable (MMC)** Hardwired to 0 indicating request for 1 message.
0	0b	RW	**MSI Enable (ME)** R/W. 0 = An MSI may not be generated. 1 = an MSI will be generated instead of an INTx signal.

MSI Message Lower Address (MMLA) – Offset 64

Bit Range	Default	Access	Field Name and Description
31:2	0000000 0h	RW	**MSI Message Lower Address (MMLA)** Lower Address used for MSI Message.
1:0	-	-	**Reserved**

MSI Message Upper Address (MMUA) – Offset 68

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**MSI Message Upper Address (MMUA)** Upper 32 bits of address used for MSIMessage.

MSI Message Data (MMD) – Offset 6c

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW	**MSI Message Data (MMD)** Data used for MSI Message.

PCI Express Capability ID (PXID) – Offset 70

Bit Range	Default	Access	Field Name and Description
15:8	00h	RO	**Next Capability (NEXT)** Indicates that this is the last capability structure inthe list.
7:0	10h	RO	**Cap ID (CAP)** Indicates that this pointer is a PCI Express capability structure.

PCI Express Capabilities (PXC) – Offset 72

Bit Range	Default	Access	Field Name and Description
14	-	-	**Reserved**
13:9	00h	RO	**Interrupt Message Number (IMN)** Hardwired to 0.
8	0b	RO	**Slot Implemented (SI)** Hardwired to 0.
7:4	9h	RO	**Device/Port Type (DPT)** Indicates that this is a Root Complex IntegratedEndpoint Device.
3:0	1h	RO	**Capability Version (CV)** Indicates version #1 PCI Express capability

Device Capabilities (DEVCAP) – Offset 74

This register is not affected by D3HOT to D0 reset or FLR.

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**
28	1b	RW/L	**Functional Level Reset (FLR)** A 1 indicates that the Intel HD Audio subsystem supports the Function Level Reset capability. Locked when FNCFG.BCLD = 1.
27:26	00b	RO	**Captured Slot Power Limit Scale (SPLS)** Hardwired to 0.
25:18	00h	RO	**Captured Slot Power Limit Value (SPLV)** Hardwired to 0.

Bit Range	Default	Access	Field Name and Description
17:15	-	-	**Reserved**
14	0b	RO	**Power Indicator Present (PIP)** Hardwired to 0.
13	0b	RO	**Attention Indicator Present (AIP)** Hardwired to 0.
12	0b	RO	**Attention Button Present (ABP)** Hardwired to 0.
11:9	000b	RW/L	**Endpoint L1 Acceptable Latency (L1CAP)** This bit is a RW/L. It will appear as RO to WHQL testing while allowing BIOS to write a value at boot that is determined by system testing. Locked when FNCFG.BCLD = 1.
8:6	000b	RW/L	**Endpoint L0s Acceptable Latency (L0SCAP)** This bit is a RW/L. It will appear as RO to WHQL testing while allowing BIOS to write a value at boot that is determined by system testing. Locked when FNCFG.BCLD = 1.
5	0b	RO	**Extended Tag Field Support (ETCAP)** Indicates 5 bit tag supported.
4:3	00b	RO	**Phantom Functions Supported (PFCAP)** Indicates phantom functions notsupported.
2:0	000b	RO	**Max Payload Size Supported (MPCAP)** Indicates 128B maximum payloadsize capability.

Device Control (DEVC) – Offset 78

NSNPEN bit is not affected by D3HOT to D0 reset or FLR.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
15	0b	WO	**Initiate FLR (IF)** Used to initiate FLR transition. A write of 1 initiates FLR transition. Since hardware must not respond to any cycles until FLR completion, the read value by software from this bit is 0 .
14:12	010b	RW	**Max Read Request Size (MRRS)** This field sets the maximum Read Request size for the Function as a Requester. The Function must not generate Read Requests with size exceeding the set value. Defined encodings for this field are: 000: 128 B 001: 256 B 010: 512 B 011: 1024 B 100: 2048 B 101: 4096 B 110 - 111: Reserved
11	1b	RW	**Enable No Snoop (NSNPEN)** When set to 1 (or EM2.FNSNPEN = 1) the Intel HD Audio controller is permitted to set the No Snoop bit in the Requester Attributes of a bus master transaction. In this case VC0, VCp, or VC1 may be used for isochronous transfers. When set to 0 (and EM2.FNSNPEN = 0) the Intel HD Audio controller will not set the No Snoop bit. In the case isochronous transfers will not use VC1(VCi) even if it is enabled since VC1 is never snooped. Isochronous transfers will use either VCp or VC0. This bit is not affected by D3HOT to D0 reset or FLR.

Bit Range	Default	Access	Field Name and Description
10	0b	RO	**Auxiliary (AUX) Power PM Enable (AUXPEN)** Hardwired to 0 indicating Intel HD Audio device does not draw AUX power.
9	0b	RO	**Phantom Functions Enable (PFEN)** Hardwired to 0 disabling phantom functions.
8	0b	RO	**Extended Tag Field Enable (ETEN)** Hardwired to 0 enabling 5-bit tag.
7:5	000b	RO	**Max Payload Size (MAXPAY)** Hardwired to 000 indicating 128 B.
4	0b	RO	**Enable Relaxed Ordering (ROEN)** Hardwired to 0 disabling relaxed ordering.
3	0b	RW	**Unsupported Request Reporting Enable (URREN)** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
2	0b	RW	**Fatal Error Reporting Enable (FEREN)** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
1	0b	RW	**Non-Fatal Error Reporting Enable (NFEREN)** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
0	0b	RW	**Correctable Error Reporting Enable (CEREN)** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.

Device Status (DEVS) – Offset 7a

Bit Range	Default	Access	Field Name and Description
14:6	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
5	0b	RO/V	**Transactions Pending (TXP)** A 1 indicates that the Intel HD Audio controller has issued Non-Posted requests which have not been completed. A 0 indicates that Completions for all Non-Posted Requests have been received.
4	1b	RW/L	**AUX Power Detected (AUXDET)** Hardwired to 1 indicating the device is connected to Suspend power. Programmable by BIOS for the option to declare SUS well wake is supported or not: 1b (SUS well wake supported) or 0b (SUS well wake not supported). Locked when FNCFG.BCLD = 1.
3	0b	RO	**Unsupported Request Detected (URDET)** Not implemented. Hardwired to 0.
2	0b	RO	**Fatal Error Detected (FEDET)** Not implemented. Hardwired to 0.
1	0b	RO	**Non-Fatal Error Detected (NFEDET)** Not implemented. Hardwired to 0.
0	0b	RO	**Correctable Error Detected (CEDET)** Not implemented. Hardwired to 0.

HPET Memory Mapped Registers

The timer registers are memory mapped directly (rather than indexed) to allow the CPU to access each register without having to use an index register. This ensures accesses are safe for multi-threaded environments. The timer register space is 1024 bytes. The registers are generally aligned on 64-bit boundaries to simplify implementation with IA64 processors.In the PCH, there are 4 possible memory address ranges beginning at 1) FED0_0000h, 2) FED0_1000h, 3) FED0_2000h, 4) FED0_3000h. The choice of address range should be selected by assigning the High Performance Event Timer Configuration (HPTC) register fields in the configuration space of the Primary to Sideband Bridge. All registers are implemented in the Primary power well, and all bits are reset by PLTRST#. Reads to reserved registers or bits will return a

value of 0.

Behavorial Rules:

1. Software can read or write the various bytes in these registers using 32-bit or 64-bit accesses. Software must not attempt to read or write across register boundaries. Forexample, a 32-bit access should be to offset x0h, x4h, x8h, or xCh. 32-bit accessesshould not be to 01h, 02h, 03h, 05h, 06h, 07h, 09h, 0Ah, 0Bh, 0Dh, 0Eh, or 0Fh.Any accesses to these offsets will result in an unexpected behavior, and may result in a master abort. However, these accesses should not result in system hangs. 64-bit accesses can only be to x0h and must not cross 64-bit boundaries.

2. Software should not write to read-only registers.

3. Software should not expect any particular or consistent value when readingreserved registers or bits.

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
fed00000h	8	General Capabilities and ID Register (GEN_CAP_ID)	27BC86B8086A701h
fed00010h	8	General Config Register (GEN_CFG)	0h
fed00020h	8	General Interrupt Status Register (GEN_INT_STS)	0h
fed000f0h	8	Main Counter Value (MAIN_CNTR)	0h
fed00100h	8	Timer n Config and Capabilities (TMRn_CNF_CAP)	0h
fed00108h	8	Timer n Comparator Value (TMRn_CMP_VAL)	FFFFFFFFFFFFFFFFh

General Capabilities and ID Register (GEN_CAP_ID) – Offset fed00000

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
63:32	027BC86Bh	RO	**Main Counter Tick Period (COUNTER_CLK_PER_CAP)** This read-only field indicates the period at which the counter increments in femtoseconds (10^-15 seconds). The PCH HPET timers use a 24 MHz clock, which has a period of 41,666,667 femtoseconds. Therefore this register will always return 027BC86Bh when read.
31:16	8086h	RO	**Vendor ID (VENDOR_ID_CAP)** These bits will return 8086h when read to reflect Intel as the vendor.
15	1b	RO	**Legacy Rout Capable (LEG_RT_CAP)** This bit will always be 1 when read, indicating support for the Legacy Interrupt Rout.
14	-	-	**Reserved**
13	1b	RO	**Counter Size (COUNT_SIZE_CAP)** This bit will return 1 when read to indicate support for 64-bit counters allowing 64 or 32-bit mode operation.
12:8	00111b	RO	**Number of Timers (NUM_TIM_CAP)** This value in this field will be 07h to indicate support for 8 timers in the timer block.
7:0	01h	RO	**Revision ID (REV_ID)** This field indicates which revision of the function isimplemented. Default value will be 01h.

General Config Register (GEN_CFG) – Offset fed00010

Bit Range	Default	Access	Field Name and Description
62:2	-	-	**Reserved**
1	0b	RW	**Legacy Rout (LEG_RT_CNF)** If the ENABLE_CNF bit and the LEG_RT_CNF bit are both set, the interrupts will be routed as follows: • Timer 0 is routed to IRQ0 in 8259 or IRQ2 in the I/O APIC • Timer 1 is routed to IRQ8 in 8259 or IRQ8 in the I/O APIC • Timer 2-n is routed as per the routing in the timer n Configuration registers. • If the Legacy Replacement Rout bit is set, the individual routing bits for Timers 0 and 1 (APIC) will have no impact. • If the Legacy Replacement Rout bit is not set, the individual routing bits for each of the timers are used. • This bit will default to 0. BIOS can set it to 1 to enable the legacy replacement routing, or 0 todisable the legacy replacement routing.
0	0b	RW	**Overall Enable (ENABLE_CNF)** This bit must be set to enable any of the timers to generateinterrupts. If this bit is 0, then the main counter will halt (will not increment) and no interrupts willbe caused by any of these timers. For level-triggered interrupts, if an interrupt is pending when theENABLE_CNF bit is changed from 1 to 0, the interrupt status indications (in the variousTxx_INT_STS bits) will not be cleared. Software must write to the Txx_INT_ STS bits to clear the interrupts. NOTE: This bit will default to 0. BIOS can set it to 1 or 0.

General Interrupt Status Register (GEN_INT_STS) – Offset fed00020

Bit Range	Default	Access	Field Name and Description
62:8	-	-	**Reserved**
7	0b	RW/1C	**Timer 7 Interrupt Active (T07_INT_STS)** Same functionality as Timer 0.

Bit Range	Default	Access	Field Name and Description
6	0b	RW/1C	**Timer 6 Interrupt Active (T06_INT_STS)** Same functionality as Timer 0.
5	0b	RW/1C	**Timer 5 Interrupt Active (T05_INT_STS)** Same functionality as Timer 0.
4	0b	RW/1C	**Timer 4 Interrupt Active (T04_INT_STS)** Same functionality as Timer 0.
3	0b	RW/1C	**Timer 3 Interrupt Active (T03_INT_STS)** Same functionality as Timer 0.
2	0b	RW/1C	**Timer 2 Interrupt Active (T02_INT_STS)** Same functionality as Timer 0.
1	0b	RW/1C	**Timer 1 Interrupt Active (T01_INT_STS)** Same functionality as Timer 0.
0	0b	RW/1C	**Timer 0 Interrupt Active (T00_INT_STS)** The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer.(default = 0) If set to level-triggered mode:This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. Writes of 0 to this bit will have noeffect. If set to edge-triggered mode: This bit should be ignored by software. Software should always write 0 to this bit. NOTE: Defaults to 0. In edge triggered mode, this bit will always read as 0 and writes will have noeffect.

Main Counter Value (MAIN_CNTR) – Offset fed000f0

Software can read the various bytes in this register using 32-bit or 64-bit accesses.

32-bit accesses may only be done to offset 0F0h or 0F4h. 64-bit accesses may only be

done to 0F0h.

Writes to this register should only be done while the counter is halted.

Reads to this register return the current value of the main counter. If 32-bit software

attempts to read a 64-bit counter, it should first halt the counter. Since this will delay the interrupts for all of the timers, this should be done only if the consequences are understood. It is strongly recommended that 32-bit software only operate the timer in 32-bit mode.

Reads to this register are monotonic. No two consecutive reads will return the same value. The second of two reads will always return a larger value (unless the timer has rolled over to 0)

Bit Range	Default	Access	Field Name and Description
63:0	0000000 0000000 00h	RW/V	**Counter Value (COUNTER_VAL)** Reads return the current value of the counter. Writes load the new value to the counter. NOTES: 1. Writes to this register should only be done while the counter is halted. 2. Reads to this register return the current value of the main counter. 3. 32-bit counters will always return 0 for the upper 32-bits of this register. 4. If 32-bit software attempts to read a 64-bit counter, it should first halt the counter. Since this will delay the interrupts for all of the timers, this should be done only if the consequences are understood. It is strongly recommended that 32-bit software only operate the timer in 32-bit mode. 5. Reads to this register are monotonic. No two consecutive reads will return the same value. The second of two reads will always return a larger value (unless the timer has rolled over to 0)

Timer n Config and Capabilities (TMRn_CNF_CAP) – Offset fed00100

Timer 0: 100–107h,

Timer 1: 120–127h,

Timer 2: 140–147h,

Timer 3: 160–167h,

Timer 4: 180–187h,

Timer 5: 1A0–1A7h,

Timer 6: 1C0–1C7h,

Timer 7: 1E0–1E7h,

The letter n can be 0, 1, 2, 3, 4, 5, 6, or 7 referring to Timer 0, 1, 2, 3, 4, 5, 6, or 7.

Bit Range	Default	Access	Field Name and Description
62:4	-	-	**Reserved**
3	0b	RW	**Timer 0 Type (TIMER0_TYPE_CNF)** Setting this bit to 1 enables the timer to generate a periodic interrupt if it is capable of doing so. If the TIMERn_PER_INT_CAP bit is 0, then this bit will always return 0 when read and writes will have no impact. For timer 0, this bit will be read/write, with default of 0. For timers 1-7, this bit will be read-only, with a fixed value of 0.
2:0	-	-	**Reserved**

Timer n Comparator Value (TMRn_CMP_VAL) – Offset fed00108

Timer 0: 108h – 10Fh

Timer 1: 128h – 12Fh

Timer 2: 148h – 14Fh

Timer 3: 168h – 16Fh

Timer 4: 188h – 18Fh

Timer 5: 1A8h – 1AFh

Timer 6: 1C8h – 1CFh

Timer 7: 1E8h – 1EFh

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
63:0	FFFFFFFF FFFFFFFF h	RW/V	**Timer 0 Comparator Value (TMR0_CMP_VAL)** If the timer is configured to non-periodic mode, when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). The value in this register does not change based on the interrupt being generated. If the timer is configured to periodic mode (supported only for Timer 0), when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). When this time out occurs, the value in this register is increased by the value last written to the register. For example, in periodic mode if the value written to the register is 0000123h: 1. An interrupt will be generated when the main counter reaches 00000123h. 2. The value in this register will then be adjusted by the hardware to 00000246h. 3. Another interrupt will be generated when the main counter reaches 00000246h. 4. The value in this register will then be adjusted by the hardware to 00000369h. As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h The default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer will have a default value of 00000000FFFFFFFFh. A 64-bit timer will have a default value of FFFFFFFFFFFFFFFFh. Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x8h or 1xCh. 64-bit accesses may only be done to 1x8h. Comparator value. Timer 0 is 64-bits wide. Timers 1-7 are 32-bits wide.

I2C Additional Registers

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
204h	4	Soft Reset (RESETS)	0h
210h	4	Active LTR (ACTIVELTR_VALUE)	800h
214h	4	Idle LTR (IDLELTR_VALUE)	800h
218h	4	TX Ack Count (TX_ACK_COUNT)	0h
21ch	4	RX ACK Count (RX_BYTE_COUNT)	0h
220h	4	Interrupt Status for Tx Complete (TX_COMPLETE_INTR_STAT)	0h
224h	4	Tx Complete Interrupt Clear (TX_COMPLETE_INTR_CLR)	0h
228h	4	SW Scratch Register 0 (SW_SCRATCH_0)	0h
22ch	4	SW Scratch Register 1 (SW_SCRATCH_1)	0h
230h	4	SW Scratch Register 2 (SW_SCRATCH_2)	0h
234h	4	SW Scratch Register 3 (SW_SCRATCH_3)	0h
238h	4	Clock Gate (CLOCK_GATE)	0h
240h	4	Remap Address Low (REMAP_ADDR_LO)	0h
244h	4	Remap Address High (REMAP_ADDR_HI)	0h
24ch	4	Device Control (DEVIDLE_CONTROL)	8h
2fch	4	Capabilities (CAPABLITIES)	200h

Soft Reset (RESETS) – Offset 204

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
2	0h	RW	**DMA Software Reset Control (RESET_DMA)** DMA Software Reset Control 0 – DMA is in reset (Reset Asserted) 1 – DMA is NOT at reset (Reset Released)
1:0	0h	RW	**Host Controller Reset (reset_ip)** Used to reset the I2C Host Controller by SW control. All I2C Configuration State and Operational State will be forced to the Default state. There is no timing requirement (SW can assert and de-assert in back to back transactions). This reset does NOT impact the settings by BIOS, the PCI configuration header information, DMA channel configuration and interrupt assignment/mapping/etc. Driver should re-initialize registers related to Driver context following an I2C host controller reset. 00 = I2C Host Controller is in reset (Reset Asserted) 01 = Reserved 10 = Reserved 11 = I2C Host Controller is NOT at reset (Reset Released)

Active LTR (ACTIVELTR_VALUE) – Offset 210

Bit Range	Default	Access	Field Name and Description
31	0h	RO	**Non-Snoop Requirement (non_snoop_requirment)** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
30:29	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
28:26	0h	RO	**Non-Snoop Latency Scale (non_snoop_latency_scale)** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale (1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
25:16	0h	RO	**Non-Snoop Value (non_snoop_value)** 10-bit latency value
15	0h	RW	**Snoop Requirement (snoop_requirment)** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	-	-	**Reserved**
12:10	2h	RW	**Snoop Latency Scale (i2c_sw_ltr_snoop_scale_reg_12_10)** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h	RW	**Snoop Value (snoop_value)** 10-bit latency value

Idle LTR (IDLELTR_VALUE) – Offset 214

Bit Range	Default	Access	Field Name and Description
31	0h	RO	**Non-Snoop Requirement (non_snoop_requirment)** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
30:29	-	-	**Reserved**
28:26	0h	RO	**Non-Snoop Latency Scale (non_snoop_latency_scale)** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale (1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.

Bit Range	Default	Access	Field Name and Description
25:16	0h	RO	**Non-Snoop Value (non_snoop_value)** 10-bit latency value
15	0h	RW	**Snoop Requirement (snoop_requirment)** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	-	-	**Reserved**
12:10	2h	RW	**Snoop Latency Scale (snoop_latency_scale)** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h	RW	**Snoop Value (snoop_value)** 10-bit latency value

TX Ack Count (TX_ACK_COUNT) – Offset 218

Bit Range	Default	Access	Field Name and Description
31	0h	RO	**Tx Count Overflow (tx_ack_count_overflow)** Tx_count_overflow 0= count valid 1= count overflow/invalid
30:24	-	-	**Reserved**
23:0	0h	RO	**TX Ack Count (tx_ack_count)** 24-bit up-counter which counts the number of TX ACKs on the I2C bus. The Counter is forced to be cleared by software Read.

RX ACK Count (RX_BYTE_COUNT) – Offset 21c

Bit Range	Default	Access	Field Name and Description
31	0h	RO	**RX ACK Count Overflow (rx_ack_count_overflow)** Rx ACK count_overflow 0= count valid 1= count overflow/invalid
30:24	-	-	**Reserved**
23:0	0h	RO	**Rx ACK Count (rx_ack_count)** 24-bit readable (MMIO) up-counter which counts the number of RX bytes received on the I2C bus. The Counter is forced to be cleared by software Read

Interrupt Status for Tx Complete (TX_COMPLETE_INTR_STAT) – Offset 220

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1	0h	RW	**TX completion interrupt Mask (tx_intr_stat_mask)** 0 = Unmask 1= Mask
0	0h	RO	**Tx Completion Interrupt (tx_intr_stat)** 0 = Low 1 = High

Tx Complete Interrupt Clear (TX_COMPLETE_INTR_CLR) – Offset 224

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RO	**TX completion interrupt Clear (i2c_tx_complete_intr_clr_0)** Read this register to clear the TX_COMPLETE_INTR_STAT register

SW Scratch Register 0 (SW_SCRATCH_0) – Offset 228

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**SW Scratch Reg 0 (SW_Scratch_0)** Scratch Pad Register for SW to generated Local CMD or DATA for DMA

SW Scratch Register 1 (SW_SCRATCH_1) – Offset 22c

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**SW Scratch Register 1 (SW_Scratch_1)** Scratch Pad Register for SW to generated Local CMD or DATA for DMA.

SW Scratch Register 2 (SW_SCRATCH_2) – Offset 230

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**SW Scratch Register 2 (SW_Scratch_2)** Scratch Pad Register for SW to generated Local CMD or DATA for DMA

SW Scratch Register 3 (SW_SCRATCH_3) – Offset 234

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**SW Scratch Register 3 (SW_Scratch_3)** Scratch Pad Register for SW to generated Local CMD or DATA for DMA

Clock Gate (CLOCK_GATE) – Offset 238

Bit Range	Default	Access	Field Name and Description
30:4	-	-	**Reserved**
3:2	0h	RW	**DMA Clock Control (sw_dma_clk_ctl)** 00 = Dyanamic Clock Gate Enable 01 = Reserved 10 = Force DMA Clock off 11 = Force DMA Clock on
1:0	0h	RW	**Controller Clock Control (sw_ip_clk_ctl)** 00 = Dynamic Clock Gate Enable 01 = Reserved 10 = Force Clocks off 11 = Force Clocks on

Remap Address Low (REMAP_ADDR_LO) – Offset 240

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Remap Address Low (i2c_remap_addr_lo_reg)** Must be programmed to the same value as low 32 bits (0x 010 BAR Low) Note: Must be programed for all I2C controllers configurations (DMA or PIO only)

Remap Address High (REMAP_ADDR_HI) – Offset 244

i2c remap address hi register

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Remap Address High (i2c_remap_addr_hi)** Must be programmed to the same value as low 32 bits (0x 014 BAR High)

Device Control (DEVIDLE_CONTROL) – Offset 24c

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4	0h	RO	**Interrupt Request Capable (intr_req_capable)** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0.
3	1h	RW/1C	**Restore Required (restore_required)** When set (by HW), SW must restore state to the controller. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up. Note: If SW is setting bit 3 together with any other bit of this register, only bit 3 is written; SW is required to do 2 writes in this case : bit 3 first and all other bits second.
2	0h	RW	**Device Idle (DEVIDLE)** SW sets this bit to '1' to move the function into the DevIdle state. Writing this bit to '0' will return the function to the fully active D0 state.
1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	0h	RO	**Command In Progress (cmd_in_progress)** HW sets this bit on a 1->0 or 0->1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. HW clears this bit upon completing the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

Capabilities (CAPABLITIES) – Offset 2fc

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9	1h	RO	**Serial Clock Frequency (serial_clk_freq)** 1 indicates 216 MHz clock.
8	0h	RO	**DMA Present (iDMA_present)** 0= DMA present 1= DMA not present
7:4	0h	RO	**Instant Type (instance_type)** 0000 = I2C 0001 = UART 0010 = SPI 0011 – 1111 = Reserved

Bit Range	Default	Access	Field Name and Description
3:0	0h	RO	**Instant Number (instance_number)** 0h: I2C0 1h: I2C1 2h: I2C2 ... 5h: I2C5[br

I2C DMA Controller Registers

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
800h	4	DMA Transfer Source Address Low (SAR_LO0)	0h
804h	4	DMA Transfer Source Address High (SAR_HI0)	0h
808h	4	DMA Transfer Destination Address Low (DAR_LO0)	0h
ad8h	4	Raw Status for Destination Transaction Interrupts (RawDstTran)	0h
ae0h	4	Raw Status for Error Interrupts (RawErr)	0h
ae8h	4	Interrupt Status (StatusTfr)	0h
80ch	4	DMA Transfer Destination Address High (DAR_HI0)	0h
810h	4	CH 0 Linked List Pointer Low (LLP_LO0)	0h
814h	4	CH 0 Linked List Pointer High (LLP_HI0)	0h
af0h	4	Status for Block Interrupts (StatusBlock)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
af8h	4	Status for Source Transaction Interrupts (StatusSrcTran)	0h
b00h	4	Status for Destination Transaction Interrupts (StatusDstTran)	0h
b08h	4	Status for Error Interrupts (StatusErr)	0h
818h	4	Control Register Low (CTL_LO0)	0h
81ch	4	Control Register High (CTL_HI0)	0h
820h	4	Source Status (SSTAT0)	0h
828h	4	Destination Status (DSTAT0)	0h
830h	4	Source Status Address Low (SSTATAR_LO0)	0h
834h	4	Source Status Address High (SSTATAR_HI0)	0h
838h	4	Destination Status Address Low (DSTATAR_LO0)	0h
83ch	4	Destination Status Address High (DSTATAR_HI0)	0h
840h	4	DMA Transfer Configuration Low (CFG_LO0)	203h
844h	4	DMA Transfer Configuration High (CFG_HI0)	0h
848h	4	Source Gather (SGR0)	0h
850h	4	Destination Scatter (DSR0)	0h
868h	4	CH 1 Linked List Pointer Low (LLP_LO1)	0h
86ch	4	CH 1 Linked List Pointer High (LLP_HI1)	0h
ac0h	4	Raw Interrupt Status (RawTfr)	0h
b10h	4	Mask for Transfer Interrupts (MaskTfr)	0h
b18h	4	Mask for Block Interrupts (MaskBlock)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
b20h	4	Mask for Source Transaction Interrupts (MaskSrcTran)	0h
b28h	4	Mask for Destination Transaction Interrupts (MaskDstTran)	0h
b30h	4	Mask for Error Interrupts (MaskErr)	0h
b38h	4	Clear for Transfer Interrupts (ClearTfr)	0h
b40h	4	Clear for Block Interrupts (ClearBlock)	0h
b48h	4	Clear for Source Transaction Interrupts (ClearSrcTran)	0h
b50h	4	Clear for Destination Transaction Interrupts (ClearDstTran)	0h
b58h	4	Clear for Error Interrupts (ClearErr)	0h
b60h	4	Combined Status register (StatusInt)	0h
ac8h	4	Raw Status for Block Interrupts (RawBlock)	0h
ad0h	4	Raw Status for Source Transaction Interrupts (RawSrcTran)	0h
b98h	4	DMA Configuration (DmaCfgReg)	0h
ba0h	4	DMA Channel Enable (ChEnReg)	0h

DMA Transfer Source Address Low (SAR_LO0) – Offset 800

NOTE: SAR_LO0 is for DMA Channel 0. The same register definition,SAR_LO1, is available for Channel 1 at address 858h.

SAR_LO0 (CH0): offset 800h

SAR_LO1 (CH1): offset 858h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Current Source Address Low (SAR_LO)** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

DMA Transfer Source Address High (SAR_HI0) – Offset 804

NOTE: SAR_HI0 is for DMA Channel 0. The same register definition, SAR_HI1, is available for Channel 1 at address 85Ch.

SAR_HI0 (CH0): offset 804h

SAR_HI1 (CH1): offset 85Ch

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Current Source Address High (SAR_HI)** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

DMA Transfer Destination Address Low (DAR_LO0) – Offset 808

NOTE: DAR_LO0 is for DMA Channel 0. The same register definition, DAR_LO1, is available for Channel 1 at address 860h.

DAR_LO0 (CH0): offset 808h

DAR_LO1 (CH1): offset 860h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Current Destination Address Low (DAR_LO)** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

Raw Status for Destination Transaction Interrupts (RawDstTran) – Offset ad8

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Raw Interrupt Status (RAW)** Bit 0 for channel 0 and bit 1 for channel 1.

Raw Status for Error Interrupts (RawErr) – Offset ae0

Interrupt events are stored in these Raw Interrupt Status registers before masking:

RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt.

Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers

The following RAW registers are available in the DMA

RawTfr - Raw Status for Transfer Interrupts

RawBlock - Raw Status for Block Interrupts Register

RawSrcTran - Raw Status for Source Transaction Interrupts Register

RawDstTran - Raw Status for Destination Transaction Interrupts Register

RawErr - Raw Status for Error Interrupts Register

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Raw Interrupt Status (RAW)** Bit 0 for channel 0 and bit 1 for channel 1.

Interrupt Status (StatusTfr) – Offset ae8

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Interrupt Status (STATUS)** Bit 0 for channel 0 and bit 1 for channel 1.

DMA Transfer Destination Address High (DAR_HI0) – Offset 80c

NOTE: DAR_HI0 is for DMA Channel 0. The same register definition, DAR_HI1, is available for Channel 1 at address 864h.

DAR_HI0 (CH0): offset 80Ch

DAR_HI1 (CH1): offset 864h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Current Destination Address High (DAR_HI)** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

CH 0 Linked List Pointer Low (LLP_LO0) – Offset 810

LLP_LO0 is for DMA Channel 0.

The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Bit Range	Default	Access	Field Name and Description
31:2	0000000 0h	RW	**LLP Address Low (LOC)** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit. Note: SW should avoid a LLP lower 32 bits equal to 0s assigned to 4GB boundary address.
1:0	-	-	**Reserved**

CH 0 Linked List Pointer High (LLP_HI0) – Offset 814

LLP_HI0 is for DMA Channel 0.

The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Bit Range	Default	Access	Field Name and Description
31:2	0000000 0h	RW	**LLP Address High (LOC)** LPP upper address.
1:0	-	-	**Reserved**

Status for Block Interrupts (StatusBlock) – Offset af0

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Interrupt status (STATUS)** Bit 0 for channel 0 and bit 1 for channel 1.

Status for Source Transaction Interrupts (StatusSrcTran) – Offset af8

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Interrupt status (STATUS)** Bit 0 is for channel 0 and bit 1 is for channel 1.

Status for Destination Transaction Interrupts (StatusDstTran) – Offset b00

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Interrupt status (STATUS)** Bit 0 is for channel 0 and bit 1 is for channel 1.

Status for Error Interrupts (StatusErr) – Offset b08

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Interrupt status (STATUS)** Bit 0 is for channel 0 and bit 1 is for channel 1.

Control Register Low (CTL_LO0) – Offset 818

NOTE: CTL_LO0 is for DMA Channel 0. The same register definition, CTL_LO1, is available for Channel 1 at address 870h.

LLP_HI0 (CH0): offset 818h

LLP_LO1 (CH1): offset 870h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**
28	0h	RW	**LLP Source Enable (LLP_SRC_EN)** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h	RW	**LLP Destination Enable (LLP_DST_EN)** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	-	-	**Reserved**
21:20	0h	RW	**Transfer Type and Flow Control (TT_FC)** The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
18	0h	RW	**Destination Scatter Enable (DST_SCATTER_EN)** 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h	RW	**Source Gather Enable (SRC_GATHER_EN)** 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h	RW	**Source Burst Transaction Length (SRC_MSIZE)** Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source.
13:11	0h	RW	**Destination Burst Transaction Length (DEST_MSIZE)** Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h	RW	**Source Address Increment (SINC)** Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	-	-	**Reserved**
8	0h	RW	**Destination Address Increment (DINC)** Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)

Bit Range	Default	Access	Field Name and Description
7	-	-	**Reserved**
6:4	0h	RW	**Source Transfer Width (SRC_TR_WIDTH)** BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
3:1	0h	RW	**Destination Transfer Width (DST_TR_WIDTH)** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
0	0h	RW	**Interrupt Enable (INT_EN)** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

Control Register High (CTL_HI0) – Offset 81c

NOTE: CTL_HI0 is for DMA Channel 0. The same register definition, CTL_HI1, is available for Channel 1 at address 874h.

CTL_HI0 (CH0): offset 81Ch

CTL_HI1 (CH1): offset 874h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Bit Range	Default	Access	Field Name and Description
31:29	0h	RW	**Channel Class (CH_CLASS)** A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.

Bit Range	Default	Access	Field Name and Description
28:18	-	-	**Reserved**
17	0h	RW	**DONE (DONE)** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h	RW	**Block Transfer Size (BLOCK_TS)** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

Source Status (SSTAT0) – Offset 820

NOTE: SSTAT0 is for DMA Channel 0. The same register definition, SSTAT1, is available for Channel 1 at address 878h.

SSTAT0 (CH0): offset 820h

SSTAT1 (CH1): offset 878h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by

the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.

Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Source Status (SSTAT)** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

Destination Status (DSTAT0) – Offset 828

NOTE: DSTAT0 is for DMA Channel 0. The same register definition, DSTAT1, is available for Channel 1 at address 880h.

DSTAT0 (CH0): offset 828h

DSTAT1 (CH1): offset 880h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.

Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Destination Status (DSTAT)** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

Source Status Address Low (SSTATAR_LO0) – Offset 830

NOTE: SSTATAR_LO0 is for DMA Channel 0. The same register definition, SSTATAR_LO1, is available for Channel 1 at address 888h.

SSTATAR_LO0(CH0): offset 830h

SSTATAR_LO1(CH1): offset 888h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Source Status Address (SSTATAR_LO)** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

Source Status Address High (SSTATAR_HI0) – Offset 834

NOTE: SSTATAR_HI0 is for DMA Channel 0. The same register definition, SSTATAR_HI1, is available for Channel 1 at address 88Ch.

SSTATAR_HI0(CH0): offset 834h

SSTATAR_HI1(CH1): offset 88Ch

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Source Status Address (SSTATAR_HI)** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

Destination Status Address Low (DSTATAR_LO0) – Offset 838

NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_LO1, is available for Channel 1 at address 890h.

DSTATAR_LO0(CH0): offset 838h

DSTATAR_LO1(CH1): offset 890h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Destination Status Address (DSTATAR_LO)** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

Destination Status Address High (DSTATAR_HI0) – Offset 83c

NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_HI1, is available for Channel 1 at address 894h.

DSTATAR_HI0(CH0): offset 83Ch

DSTATAR_HI1(CH1): offset 894h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Destination Status Address (DSTATAR_HI)** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

DMA Transfer Configuration Low (CFG_LO0) – Offset 840

NOTE: CFG_LO0 is for DMA Channel 0. The same register definition, CFG_LO1, is available for Channel 1 at address 898h.

CFG_LO0(CH0): offset 840h

CFG_LO1(CH1): offset 898h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Bit Range	Default	Access	Field Name and Description
31	0h	RW	**Automatic Destination Reload (RELOAD_DST)** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h	RW	**Automatic Source Reload (RELOAD_SRC)** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
21	0h	RW	**Optimize Source Burst Length (SRC_OPT_BL)** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h	RW	**Optimize Destination Burst Length (DST_OPT_BL)** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled
19	0h	RW	**Source Handshaking Interface Polarity (SRC_HS_POL)** 0 = Active high 1 = Active low
18	0h	RW	**Destination Handshaking Interface Polarity (DST_HS_POL)** 0 = Active high 1 = Active low
17:11	-	-	**Reserved**
10	0b	RW	**Channel FIFO Drain (CH_DRAIN)** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted

Bit Range	Default	Access	Field Name and Description
9	1b	RO	**(FIFO_EMPTY)** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h	RW	**Channel Suspend (CH_SUSP)** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h	RW	**Source Status Update Enable (SS_UPD_EN)** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h	RW	**Destination Status Update Enable (DS_UPD_EN)** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h	RW	**CTL_HI Update Enable (CTL_HI_UPD_EN)** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3	0h	RW	**Handshake Non-Posted Write (HSHAKE_NP_WR)** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted) This bit must be set to 1 for proper operation
2	0h	RW	**Non Posted Write (ALL_NP_WR)** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h	RW	**Source Burst Align (SRC_BURST_ALIGN)** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h	RW	**Destination Burst Align (DST_BURST_ALIGN)** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

DMA Transfer Configuration High (CFG_HI0) – Offset 844

NOTE: CFG_HI0 is for DMA Channel 0. The same register definition, CFG_HI1, is available for Channel 1 at address 89Ch.

CFG_HI0(CH0): offset 844h

CFG_HI1(CH1): offset 89Ch

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Bit Range	Default	Access	Field Name and Description
30:28	-	-	**Reserved**
27:18	0h	RW	**Write Issue Threshold (WR_ISSUE_THD)** Write Issue Threshold. Used to relax the issue criterion for Writes. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.

Bit Range	Default	Access	Field Name and Description
17:8	0h	RW	**Read Issue Threshold (RD_ISSUE_THD)** Read Issue Threshold. Used to relax the issue criterion for Reads. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_ MSIZE)*TW.
7:4	0h	RW	**Destination Peripheral ID (DST_PER)** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.
3:0	0h	RW	**Source Peripheral ID (SRC_PER)** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

Source Gather (SGR0) – Offset 848

NOTE: SGR0 is for DMA Channel 0. The same register definition, SGR1, is available for Channel 1 at address 8A0h.

SGR0(CH0): offset 848h

SGR1(CH1): offset 8A0h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:20	0h	RW	**SGC (SGC)** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h	RW	**SGI (SGI)** Source gather interval.

Destination Scatter (DSR0) – Offset 850

NOTE: DSR0 is for DMA Channel 0. The same register definition, DSR1, is available for Channel 1 at address 8A8h.

DSR0(CH0): offset 850h

DSR1(CH1): offset 8A8h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Bit Range	Default	Access	Field Name and Description
31:20	0h	RW	**DSC (DSC)** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h	RW	**DSI (DSI)** Destination scatter interval.

CH 1 Linked List Pointer Low (LLP_LO1) – Offset 868

LLP_LO1 is for DMA Channel 1.

The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Bit Range	Default	Access	Field Name and Description
31:2	0000000 0h	RW	**LLP Low Address (LOC)** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit. Note: SW should avoid a LLP lower 32 bits equal to 0s assigned to 4GB boundary address.
1:0	-	-	**Reserved**

CH 1 Linked List Pointer High (LLP_HI1) – Offset 86c

LLP_LH1 is for DMA Channel 1.

The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Bit Range	Default	Access	Field Name and Description
31:2	0000000 0h	RW	**LLP Address High (LOC)** LLP upper address.
1:0	-	-	**Reserved**

Raw Interrupt Status (RawTfr) – Offset ac0

Interrupt events are stored in these Raw Interrupt Status registers before masking:

RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status

register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2

raw transfer complete interrupt.

Each bit in these registers is cleared by writing a 1 to the corresponding

location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers

The following RAW registers are available in the DMA

RawTfr - Raw Status for Transfer Interrupts

RawBlock - Raw Status for Block Interrupts Register

RawSrcTran - Raw Status for Source Transaction Interrupts Register

RawDstTran - Raw Status for Destination Transaction Interrupts Register

RawErr - Raw Status for Error Interrupts Register

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Raw Interrupt Status (RAW)** Bit0 for channel 0 and bit 1 for channel 1.

Mask for Transfer Interrupts (MaskTfr) – Offset b10

The contents of the Raw Status registers are masked with the contents of the

Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr.

Each Interrupt Mask register has a bit allocated per channel, for example,

MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt.

When the source peripheral of DMA channel i is memory, then the source transaction

complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering

of an interrupt on the int_combined signal. Similarly, when the destination peripheral of DMA channel i is memory, then the destination transaction complete interrupt, MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt on the int_combined(_n) signal.

A channel INT_MASK bit will be written only if the corresponding mask write enable bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0), while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged.

Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus allowing the DMA to set the appropriate bit in the Status registers and int_* port signals.

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:8	0h	WO	**Interrupt Mask Write Enable (INT_MASK_WE)** 0 = write disabled 1 = write enabled
7:2	-	-	**Reserved**
1:0	0h	RW	**Interrupt mask (INT_MASK)** 0-mask 1-unmask

Mask for Block Interrupts (MaskBlock) – Offset b18

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:8	0h	WO	**Interrupt Mask Write Enable (INT_MASK_WE)** 0 = write disabled 1 = write enabled
7:2	-	-	**Reserved**
1:0	0h	RW	**Interrupt mask (INT_MASK)** 0-mask 1-unmask

Mask for Source Transaction Interrupts (MaskSrcTran) – Offset b20

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:8	0h	WO	**Interrupt Mask Write Enable (INT_MASK_WE)** 0 = write disabled 1 = write enabled
7:2	-	-	**Reserved**
1:0	0h	RW	**Interrupt mask (INT_MASK)** 0-mask 1-unmask

Mask for Destination Transaction Interrupts (MaskDstTran) – Offset b28

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:8	0h	WO	**Interrupt Mask Write Enable (INT_MASK_WE)** 0 = write disabled 1 = write enabled
7:2	-	-	**Reserved**
1:0	0h	RW	**Interrupt mask (INT_MASK)** 0-mask 1-unmask

Mask for Error Interrupts (MaskErr) – Offset b30

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:8	0h	WO	**Interrupt Mask Write Enable (INT_MASK_WE)** 0 = write disabled 1 = write enabled
7:2	-	-	**Reserved**
1:0	0h	RW	**Interrupt mask (INT_MASK)** 0-mask 1-unmask

Clear for Transfer Interrupts (ClearTfr) – Offset b38

Each bit in the Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	WO	**Interrupt Clear (CLEAR)** 0 = no effect 1 = clear interrupt

Clear for Block Interrupts (ClearBlock) – Offset b40

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	WO	**Interrupt Clear (CLEAR)** 0 = no effect 1 = clear interrupt

Clear for Source Transaction Interrupts (ClearSrcTran) – Offset b48

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1:0	0h	WO	**Interrupt clear (CLEAR)** 0 = no effect 1 = clear interrupt

Clear for Destination Transaction Interrupts (ClearDstTran) – Offset b50

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	WO	**Interrupt Clear (CLEAR)** 0 = no effect 1 = clear interrupt

Clear for Error Interrupts (ClearErr) – Offset b58

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	WO	**Interrupt clear (CLEAR)** 0 = no effect 1 = clear interrupt

Combined Status register (StatusInt) – Offset b60

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is ORed to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4	0h	RO	**ERR (ERR)** OR of the contents of StatusErr register.
3	0h	RO	**DSTT (DSTT)** OR of the contents of StatusDst register.
2	0h	RO	**SRCT (SRCT)** OR of the contents of StatusSrcTran register
1	0h	RO	**Block (BLOCK)** OR of the contents of StatusBlock register.
0	0h	RO	**TFR (TFR)** OR of the contents of StatusTfr register.

Raw Status for Block Interrupts (RawBlock) – Offset ac8

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**Raw interrupt status (RAW)** Bit 0 for channel 0 and bit 1 for channel 1.

Raw Status for Source Transaction Interrupts (RawSrcTran) – Offset ad0

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1:0	0h	RO	**Raw Interrupt Status (RAW)** Bit 0 for channel 0 and bit 1 for channel 1.

DMA Configuration (DmaCfgReg) – Offset b98

This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RW	**DMA Enable (DMA_EN)** 0 = DMA Disabled 1 = DMA Enabled

DMA Channel Enable (ChEnReg) – Offset ba0

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority.

All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0.

The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel

write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer.

For example, writing hex 01x1 writes a 1 into ChEnReg(0), while ChEnReg(7:1)

remains unchanged. Writing hex 00xx leaves ChEnReg(7:0) unchanged.

Note that a read-modified write is not required.

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:8	0h	WO	**(CH_EN_WE)** Channel enable write enable.
7:2	-	-	**Reserved**
1:0	0h	RW	**Channel Enable (CH_EN)** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

I2C Memory Mapped Registers

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	I2C Control (IC_CON)	77h
4h	4	I2C Target Address (IC_TAR)	1055h
ch	4	I2C High Speed Master Mode Code Address (IC_HS_MADDR)	1h
10h	4	I2C Rx/Tx Data Buffer and Command (IC_DATA_CMD)	0h
14h	4	Standard Speed I2C Clock SCL High Count (IC_SS_SCL_HCNT)	1F4h
18h	4	Standard Speed I2C Clock SCL Low Count (IC_SS_SCL_LCNT)	24Ch
1ch	4	Fast Speed I2C Clock SCL High Count (IC_FS_SCL_HCNT)	4Bh
20h	4	Fast Speed I2C Clock SCL Low Count (IC_FS_SCL_LCNT)	A3h
24h	4	High Speed I2C Clock SCL High Count (IC_HS_SCL_HCNT)	8h
28h	4	High Speed I2C Clock SCL Low Count (IC_HS_SCL_LCNT)	14h
2ch	4	I2C Interrupt Status (IC_INTR_STAT)	0h
30h	4	I2C Interrupt Mask (IC_INTR_MASK)	8FFh
34h	4	I2C Raw Interrupt Status (IC_RAW_INTR_STAT)	0h
38h	4	I2C Receive FIFO Threshold (IC_RX_TL)	0h
3ch	4	I2C Transmit FIFO Threshold (IC_TX_TL)	0h
40h	4	Clear Combined and Individual Interrupt (IC_CLR_INTR)	0h
44h	4	Clear RX_UNDER Interrupt (IC_CLR_RX_UNDER)	0h
48h	4	Clear RX_OVER Interrupt (IC_CLR_RX_OVER)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4ch	4	Clear TX_OVER Interrupt (IC_CLR_TX_OVER)	0h
50h	4	Clear RD_REQ Interrupt (IC_CLR_RD_REQ)	0h
54h	4	Clear TX_ABRT Interrupt (IC_CLR_TX_ABRT)	0h
58h	4	Clear RX_DONE Interrupt (IC_CLR_RX_DONE)	0h
5ch	4	Clear ACTIVITY Interrupt (IC_CLR_ACTIVITY)	0h
60h	4	Clear STOP_DET Interrupt (IC_CLR_STOP_DET)	0h
64h	4	Clear START_DET Interrupt (IC_CLR_START_DET)	0h
68h	4	Clear GEN_CALL Interrupt (IC_CLR_GEN_CALL)	0h
6ch	4	I2C Enable (IC_ENABLE)	0h
70h	4	I2C Status (IC_STATUS)	6h
74h	4	I2C Transmit FIFO Level (IC_TXFLR)	0h
78h	4	I2C Receive FIFO Level (IC_RXFLR)	0h
7ch	4	I2C SDA Hold Time Length (IC_SDA_HOLD)	1h
80h	4	I2C Transmit Abort Source (IC_TX_ABRT_SOURCE)	0h
88h	4	DMA Control (IC_DMA_CR)	0h
8ch	4	DMA Transmit Data Level (IC_DMA_TDLR)	0h
90h	4	I2C Receive Data Level (IC_DMA_RDLR)	0h
98h	4	I2C ACK General Call (IC_ACK_GENERAL_CALL)	1h
9ch	4	I2C Enable Status (IC_ENABLE_STATUS)	0h
a0h	4	I2C SS and FS Spike Suppression Limit (IC_FS_SPKLEN)	7h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
a8h	4	Clear RESTART_DET Interrupt (IC_CLR_ RESTRART_DET)	0h

I2C Control (IC_CON) – Offset 0

This register can be written only when the I2C is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0h	RW	**TX Empty Control (TX_EMPTY_CTRL)** This bit controls the generation of the TX_EMPTY interrupt, asdescribed in the IC_ RAW_INTR_STAT register.
7	-	-	**Reserved**
6	1h	RW	**IC_SLAVE_DISABLE (IC_SLAVE_DISABLE)** This bit controls whether I2C has its slave disabled.If this bit is set (slave is disabled), the function only works as a master and does not perform any action that requires a slave. 0:Reserved 1: slave is disabled NOTE: For Master Device Configuration Software must ensure that this bit is set to 1, and bit 0 must also be set to 1. Else this will result in configuration error

Bit Range	Default	Access	Field Name and Description
5	1h	RO	**Restart Enable (IC_RESTART_EN)** Determines whether RESTART conditions may be sent when I2C is acting as a master. 0: Restart disable 1: Restart enable When the RESTART is disabled, the IP isincapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple transfers. If the above operations are performed, it will result in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register.
4	1h	RO	**7_10 Bit Addressing (IC_10BITADDR_MASTER_rd_only)** Identifies if I2C operates in 7 or 10 bit addressing. 0: 7-bit addressing 1: 10-bit addressing
3	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
2:1	3h	RW	**Speed (SPEED)** These bits control at which speed the I2C operates. 01: standard mode (0 to 100 kbit/s) 10: fast mode (< = 400 kbit/s) 11: high speed mode (< = 3.4 Mbit/s) Others: reserved
0	1h	RW	**Master Mode (MASTER_MODE)** This bit controls whether I2C master is enabled. 0 = Reserved 1 = Master Enabled Note: For Master Device Configuration Software must ensure that this bit is set to 1, and bit 6 must also be set to 1. Else this will result in configuration error.

I2C Target Address (IC_TAR) – Offset 4

The register should only be updated when the I2C is not enabled (IC_ENABLE=0) or No Master mode operations are active (IC_STATUS[5] = 0 and IC_CON[0] = 1 and IC_STATUS[2] = 1).

Bit Range	Default	Access	Field Name and Description
30:13	-	-	**Reserved**
12	1h	RW	**7_10 Bit Adressing (IC_10BITADDR_MASTER)** This bit controls whether the I2C starts its transfers in 7-or 10-bit addressing mode when acting as a master. 0: 7 bit addressing 1: 10-bit addressing
11	0h	RW	**Special (SPECIAL)** This bit indicates whether software performs a General Call or START BYTE command. 0: ignore bit 10 GC_OR_START and use IC_TAR normally. 1: perform special I2C command as specified in GC_OR_START bit

Bit Range	Default	Access	Field Name and Description
10	0h	RW	**General Call Or START (GC_OR_START)** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call or START byte command is to be performed by the I2C. 0: General Call Address – after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The I2C remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. 1: START BYTE
9:0	55h	RW	**Target Address (IC_TAR)** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

I2C High Speed Master Mode Code Address (IC_HS_MADDR) – Offset c

I2C High Speed Master Mode Code Address Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**
2:0	1h	RW	**High Speed Mode Master Code (IC_HS_MAR)** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2).

I2C Rx/Tx Data Buffer and Command (IC_DATA_CMD) – Offset 10

This register is used by the processor to write to when filling the Tx FIFO and to readfrom when retrieving bytes form Tx FIFO. In order for the I2C controller to continueacknowledging reads, a read command should be written for every byte that is to bereceived; otherwise, the controller will stop acknowledging.

Bit Range	Default	Access	Field Name and Description
30:11	-	-	**Reserved**
10	0h	RW	**Restart (RESTART)** This bit controls whether a RESTART is issued before the byte is sent or received. 1: a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command. 0: a RESTART is issued only if the transfer direction is changing from the previous command
9	0h	RW	**Stop (STOP)** This bit controls whether a STOP is issued after the byte is sent or received. 1: STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. 0: STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.
8	0h	RW	**Command (CMD)** This bit controls whether a read or a write is performed. 1 = Read. 0 = Write When programming this bit, note the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the IC_RAW_INTR_STAT register), unless bit 11(SPECIAL) in the IC_TAR register has been cleared. If a “1” is written to this bit after receiving a RD_REQ interrupt, then a TX_ ABRTinterrupt occurs.
7:0	0h	RW	**Data (DAT)** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the I2C. However, when you read this register, these bits return the value of data received on the I2C interface.

Standard Speed I2C Clock SCL High Count (IC_SS_SCL_HCNT) – Offset 14

This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	1f4h	RW	**Standard Speed Clock High Count (IC_SS_SCL_HCNT)** This register sets the SCL clock high-period countfor standard speed. The value of the registers should be within the range {6, 65525}

Standard Speed I2C Clock SCL Low Count (IC_SS_SCL_LCNT) – Offset 18

This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	024ch	RW	**Standard Speed Clock Low Count (IC_SS_SCL_LCNT)** Standard Speed I2C Clock SCL Low Count Register. The register value should always be >= 8

Fast Speed I2C Clock SCL High Count (IC_FS_SCL_HCNT) – Offset 1c

This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
15:0	004bh	RW	**Fast Speed Clock High Count (IC_FS_SCL_HCNT)** This register sets the SCL clock high-period countfor fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The minimum value of this field is 6.

Fast Speed I2C Clock SCL Low Count (IC_FS_SCL_LCNT) – Offset 20

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing.

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	00a3h	RW	**IC_FS_SCL_LCNT (IC_FS_SCL_LCNT)** This register sets the SCL clock low period count forfast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The register should be programmed with a minimum value of 8.

High Speed I2C Clock SCL High Count (IC_HS_SCL_HCNT) – Offset 24

This register must be set before any I2C bus transaction can take place to ensure proper I/O timing.

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0008h	RW	**High Speed Clock High Count (IC_HS_SCL_HCNT)** This register sets the SCL clock high period count forhigh speed.

High Speed I2C Clock SCL Low Count (IC_HS_SCL_LCNT) – Offset 28

High Speed I2C Clock SCL Low Count Register

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0014h	RW	**High Speed Clock Low Count (IC_HS_SCL_LCNT)** This register sets the SCL clock low period count forhigh speed.

I2C Interrupt Status (IC_INTR_STAT) – Offset 2c

Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13	0h	RO	**R_MST_ON_HOLD (R_MST_ON_HOLD)** Indicates whether a master is holding the bus and the TX FIFO is empty.Enabled only when I2C_DYNAMIC_TAR_UPDATE = 1 andIC_EMPTYFIFO_HOLD_MASTER_EN = 1
12	-	-	**Reserved**
11	0h	RO	**R_GEN_CALL (R_GEN_CALL)** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling the controller or when the processor reads bit 0 of the IC_CLR_GEN_CALL register
10	0h	RO	**R_START_DET (R_START_DET)** Indicates whether a START or RESTART condition has occurred on the I2C interface
9	0h	RO	**R_STOP_DET (R_STOP_DET)** Indicates whether a STOP condition has occurred on the I2C interface.

Bit Range	Default	Access	Field Name and Description
8	0h	RO	**R_ACTIVITY (R_ACTIVITY)** This bit captures the controller activity and stays set until it is cleared. There are four ways to clear it:1. Disabling the controller,2. Reading the IC_CLR_ACTIVITY register,3. Reading the IC_CLR_INTR register,4. System resetNote: Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the controller is idle, this bit remains set until cleared, indicating that there was activity on the bus.
7	-	-	**Reserved**
6	0h	RO	**R_TX_ABRT (R_TX_ABRT)** This bit indicates if the controler, as an I2C transmitter, is unable to completethe intended actions on the contents of the transmit FIFO. When this bit is set to 1, the IC_TX_ABRT_SOURCE register indicates thereason why the transmit abort takes places.NOTE: The controller flushes/resets/empties the TX FIFO whenever thisbit is set. The TX FIFO remains in this flushed state until the registerIC_CLR_TX_ABRT is read. Once this read is performed, the TX FIFO is thenready to accept more data bytes.
5	-	-	**Reserved**
4	0h	RO	**R_TX_EMPTY (R_TX_EMPTY)** The behavior of the TX_EMPTY interrupt status differs based on the TX_EMPTY_CTRL selection in the IC_CON register. - When TX_EMPTY_CTRL = 0:This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. - When TX_EMPTY_CTRL = 1:This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register and the transmission of the address/data from the internal shift register for the most recently popped command is completed. It is automatically cleared by hardware when the buffer level goes above the threshold. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. Then the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer any activity, then with ic_en=0, this bit is set to 0.

Bit Range	Default	Access	Field Name and Description
3	0h	RO	**R_TX_OVER (R_TX_OVER)** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register.
2	0h	RO	**R_RX_FULL (R_RX_FULL)** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. NOTE: If IC_RX_FULL_HLD_BUS_EN=1, then the RX_OVER interrupt isnever set to 1, because the criteria to set this interrupt are never met.
1	0h	RO	**R_RX_OVER (R_RX_OVER)** Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The controller acknowledges this, but any data bytes received after the FIFO is full are lost.
0	0h	RO	**R_RX_UNDER (R_RX_UNDER)** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register.

I2C Interrupt Mask (IC_INTR_MASK) – Offset 30

These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13	0h	RW	**M_MST_ON_HOLD (M_MST_ON_HOLD)**
12	-	-	**Reserved**
11	1h	RW	**M_GEN_CALL (M_GEN_CALL)**

Bit Range	Default	Access	Field Name and Description
10	0h	RW	**M_START_DET (M_START_DET)**
9	0h	RW	**M_STOP_DET (M_STOP_DET)**
8	0h	RW	**M_ACTIVITY (M_ACTIVITY)**
7	1h	RW	**M_RX_DONE (M_RX_DONE)**
6	1h	RW	**M_TX_ABRT (M_TX_ABRT)**
5	1h	RW	**M_RD_REQ (M_RD_REQ)**
4	1h	RW	**M_TX_EMPTY (M_TX_EMPTY)**
3	1h	RW	**M_TX_OVER (M_TX_OVER)**
2	1h	RW	**M_RX_FULL (M_RX_FULL)**
1	1h	RW	**M_RX_OVER (M_RX_OVER)**
0	1h	RW	**M_RX_UNDER (M_RX_UNDER)**

I2C Raw Interrupt Status (IC_RAW_INTR_STAT) – Offset 34

Unlike the IC_INTR_STAT register, these bits are not masked so they always show the true status of the controller

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13	0h	RO	**MST_ON_HOLD (MST_ON_HOLD)** Same as in IC_INTR_STAT.
12	-	-	**Reserved**
11	0h	RO	**GEN_CALL (GEN_CALL)** Same as in IC_INTR_STAT.
10	0h	RO	**START_DET (START_DET)** Same as in IC_INTR_STAT.
9	0h	RO	**STOP_DET (STOP_DET)** Same as in IC_INTR_STAT.
8	0h	RO	**ACTIVITY (ACTIVITY)** Same as in IC_INTR_STAT.
7	0h	RO	**RX_DONE (RX_DONE)** Same as in IC_INTR_STAT.
6	0h	RO	**TX_ABRT (TX_ABRT)** Same as in IC_INTR_STAT.
5	0h	RO	**RD_REQ (RD_REQ)** Same as in IC_INTR_STAT.
4	0h	RO	**TX_EMPTY (TX_EMPTY)** Same as in IC_INTR_STAT.
3	0h	RO	**TX_OVER (TX_OVER)** Same as in IC_INTR_STAT.
2	0h	RO	**RX_FULL (RX_FULL)** Same as in IC_INTR_STAT.

Bit Range	Default	Access	Field Name and Description
1	0h	RO	**RX_OVER (RX_OVER)** Same as in IC_INTR_STAT.
0	0h	RO	**RX_UNDER (RX_UNDER)** Same as in IC_INTR_STAT.

I2C Receive FIFO Threshold (IC_RX_TL) – Offset 38

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	0h	RW	**RX_TL (RX_TL)** Receive FIFO Threshold Level. Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in IC_RAW_INTR_STAT register). The valid range is 0-0x3F. (Values > 0x3F are set to depth of the buffer). A value of 0 sets the threshold for 1 entry, and a value of 63 sets the threshold for64 entries. WARNING: When operating with DMA, the Watermark for I2C RX fifo must be programmed to be equal to M-Size (burst size) of the DMA; Any other programming value will put controller at risk of a deadlock.

I2C Transmit FIFO Threshold (IC_TX_TL) – Offset 3c

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	0h	RW	**TX_TL (TX_TL)** Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-0x3F, (Values > 0x3F are set to depth of the buffer).A value of 0 sets the threshold for 1 entry, and a value of 63 sets the threshold for64 entries.

Clear Combined and Individual Interrupt (IC_CLR_INTR) – Offset 40

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RO	**CLR_INTR (CLR_INTR)** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

Clear RX_UNDER Interrupt (IC_CLR_RX_UNDER) – Offset 44

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RO	**CLR_RX_UNDER (CLR_RX_UNDER)** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

Clear RX_OVER Interrupt (IC_CLR_RX_OVER) – Offset 48

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RO	**CLR_RX_OVER (CLR_RX_OVER)** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

Clear TX_OVER Interrupt (IC_CLR_TX_OVER) – Offset 4c

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RO	**CLR_TX_OVER (CLR_TX_OVER)** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

Clear RD_REQ Interrupt (IC_CLR_RD_REQ) – Offset 50

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RO	**CLR_RD_REQ (CLR_RD_REQ)** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register.

Clear TX_ABRT Interrupt (IC_CLR_TX_ABRT) – Offset 54

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RO	**CLR_TX_ABRT (CLR_TX_ABRT)** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE

Clear RX_DONE Interrupt (IC_CLR_RX_DONE) – Offset 58

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RO	**CLR_RX_DONE (CLR_RX_DONE)** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

Clear ACTIVITY Interrupt (IC_CLR_ACTIVITY) – Offset 5c

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RO	**CLR_ACTIVITY (CLR_ACTIVITY)** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register.

Clear STOP_DET Interrupt (IC_CLR_STOP_DET) – Offset 60

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RO	**CLR_STOP_DET (CLR_STOP_DET)** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_ STAT register.

Clear START_DET Interrupt (IC_CLR_START_DET) – Offset 64

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RO	**CLR_START_DET (CLR_START_DET)** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

Clear GEN_CALL Interrupt (IC_CLR_GEN_CALL) – Offset 68

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RO	**CLR_GEN_CALL (CLR_GEN_CALL)** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register.

I2C Enable (IC_ENABLE) – Offset 6c

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1	0h	RW	**ABORT (ABORT)** Sofware can abort I2C transfer by setting this bit. Hw will clear this ABORT bit once the STOP has been detected

Bit Range	Default	Access	Field Name and Description
0	0h	RW	**ENABLE (ENABLE)** Controls whether the controller is enabled. 0: Disables I2C controller(TX and RX FIFOs are held in an erased state) 1: Enables I2C controller. Software can disable the controller while it is active. However, it is important that care be taken to ensure that the controller is disabled properly. When the controller is disabled, the following occurs: -The TX FIFO and RX FIFO get flushed. -Status bits in the IC_INTR_STAT register are still active until the controller goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the controller stops the current transfer at the end of the current byte and does not acknowledge the transfer.

I2C Status (IC_STATUS) – Offset 70

Bit Range	Default	Access	Field Name and Description
30:6	-	-	**Reserved**
5	0h	RO	**Master Activity Status (MST_ACTIVITY)** When the Master state machine is not in the IDLE state, this bit is set. 0: Master is in IDLE state 1: Master is not in IDLE

Bit Range	Default	Access	Field Name and Description
4	0h	RO	**Receive FIFO Completely Full (RFF)** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0: Receive FIFO is not full 1: Receive FIFO is full
3	0h	RO	**Receive FIFO Not Empty (RFNE)** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. 0: Receive FIFO is empty 1: Receive FIFO is not empty
2	1h	RO	**Transmit FIFO Completely Empty (TFE)** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty
1	1h	RO	**Transmit FIFO Not Full (TFNF)** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0: Transmit FIFO is full 1: Transmit FIFO is not full
0	0h	RO	**ACTIVITY (ACTIVITY)** I2C Activity Status

I2C Transmit FIFO Level (IC_TXFLR) – Offset 74

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
8:0	0h	RO	**Transmit FIFO Level (TXFLR)** Contains the number of valid data entries in the transmit FIFO.

I2C Receive FIFO Level (IC_RXFLR) – Offset 78

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8:0	0h	RO	**Receive FIFO Level (RXFLR)** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

I2C SDA Hold Time Length (IC_SDA_HOLD) – Offset 7c

This register controls the amount of hold time on the SDA signal after a negative edge of SCL, in units of 10 MHz.

The value programmed must be greater than the minimum hold time in each mode for the value to be implemented—one cycle in master mode.

Writes to this register succeed only when IC_ENABLE=0.

The programmed SDA hold time cannot exceed at any time the duration of the low part of SCL. Therefore, the programmed value cannot be larger than N_SCL_LOW-2, where N_SCL_LOW is the duration of the low part of the SCL period measured in ic_clk cycles (10 MHz).

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	1h	RW	**IC_SDA_HOLD (IC_SDA_HOLD)** Sets the required SDA hold time in units of ic_clk period.

I2C Transmit Abort Source (IC_TX_ABRT_SOURCE) – Offset 80

I2C Transmit Abort Source (IC_TX_ABRT_SOURCE) - Offset 80

This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]).

Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Bit Range	Default	Access	Field Name and Description
31:24	0b	RO	**TX_FLUSH_CNT (TX_FLUSH_CNT)** This field preserves the TXFLR value prior to the last TX_ABRT event. It is clearedwhenever I2C is disabled.
23:17	-	-	**Reserved**
16	0h	RO	**ABRT_USER_ABRT (ABRT_USER_ABRT)** Master has detected the user initiated transfer abort (IC_ENABLE[1])
15	0h	RO	**ABRT_SLVRD_INTX (ABRT_SLVRD_INTX)**
14:13	-	-	**Reserved**
12	0h	RO	**ARB_LOST (ARB_LOST)** 1: Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration.
11	0h	RO	**ABRT_MASTER_DIS (ABRT_MASTER_DIS)** 1: User tries to initiate a Master operation with the Master mode disabled.
10	0h	RO	**ABRT_10B_RD_NORSTRT (ABRT_10B_RD_NORSTRT)** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode.

Bit Range	Default	Access	Field Name and Description
9	0h	RO	**ABRT_SBYTE_NORSTRT (ABRT_SBYTE_NORSTRT)** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets re-asserted.
8	0h	RO	**ABRT_HS_NORSTRT (ABRT_HS_NORSTRT)** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode.
7	0h	RO	**ABRT_SBYTE_ACKDET (ABRT_SBYTE_ACKDET)** 1: Master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	0h	RO	**ABRT_HS_ACKDET (ABRT_HS_ACKDET)** 1: Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior).
5	0h	RO	**ABRT_GCALL_READ (ABRT_GCALL_READ)** 1: Controller in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h	RO	**ABRT_GCALL_NOACK (ABRT_GCALL_NOACK)** 1: controller in master mode sent a General Call and no slave on the bus acknowledged the General Call.
3	0h	RO	**ABRT_TXDATA_NOACK (ABRT_TXDATA_NOACK)** 1: This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).
2	0h	RO	**ABRT_10ADDR2_NOACK (ABRT_10ADDR2_NOACK)** 1: Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	0h	RO	**ABRT_10ADDR1_NOACK (ABRT_10ADDR1_NOACK)** 1: Master is in 10-bit address mode and the first 10-bit address byte was notacknowledged by any slave.

Bit Range	Default	Access	Field Name and Description
0	0h	RO	**ABRT_7B_ADDR_NOACK (ABRT_7B_ADDR_NOACK)** 1: Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

DMA Control (IC_DMA_CR) – Offset 88

This register is only valid when the controller is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1).

When the controller is not configured for DMA operation, this register does not exist and writing to the register's address has no effect and reading from this register address will return zero.

The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1	0h	RW	**Transmit DMA Enable (TDMAE)** This bit enables/disables the transmit FIFO DMA channel. 0 = Transmit DMA disabled 1 = Transmit DMA enabled
0	0h	RW	**Receive DMA Enable (RDMAE)** This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled 1 = Receive DMA enabled

DMA Transmit Data Level (IC_DMA_TDLR) – Offset 8c

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	0h	RW	**Transmit Data Level (DMATDL)** This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in thetransmit FIFO is equal to or below this field value, and TDMAE = 1.

I2C Receive Data Level (IC_DMA_RDLR) – Offset 90

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	0h	RW	**DMARDL (DMARDL)** This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

I2C ACK General Call (IC_ACK_GENERAL_CALL) – Offset 98

The register controls whether the controller responds with a ACK or NACK when it receives an I2C General Call address.

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	1h	RW	**ACK_GEN_CALL (ACK_GEN_CALL)** When set to 1, the controller responds with a ACK when it receives a General Call. When set to 0, the controller does not generate General Call interrupts

I2C Enable Status (IC_ENABLE_STATUS) – Offset 9c

The register is used to report the hardware status when the IC_ENABLE register is set from 1 to 0; that is, when the controller is disabled.

If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.

If IC_ENABLE has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as '0'.

When IC_ENABLE has been written with '0,' a delay occurs for bit 0 to be read as '0' because disabling the controller depends on I2C bus activities.

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RO	**I2C Enable Status (IC_EN)** When read as 1, the controller is deemed to be in an enabled state.When read as 0, the controller is deemed completely inactive.

I2C SS and FS Spike Suppression Limit (IC_FS_SPKLEN) – Offset a0

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes.

The relevant I2Crequirement is tSP as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	07h	RW	**IC_FS_SPKLEN (IC_FS_SPKLEN)** This register must be set before any I2C bus transaction can take place toensure stable operation. This register sets the duration, measured in ic_clkcycles, of the longest spike in the SCL or SDA lines that are filtered out bythe spike suppression logic. This register can be written only when the I2C interface is disabled, whichcorresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

Clear RESTART_DET Interrupt (IC_CLR_RESTRART_DET) – Offset a8

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RO	**IC_CLR_RESTART_DET (IC_CLR_RESTART_DET)** Read this register to clear the RESTART_DET interrupt (bit 12) ofthe IC_RAW_INTR_STAT register. This register is present only whenIC_SLV_RESTART_DET_EN = 1.

I2C PCI Congifuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID and Vendor ID (DEVVENDID)	XXXX8086h
4h	4	Status and Command (STATUSCOMMAND)	100000h
8h	4	Revision ID and Class Code (REVCLASSCODE)	C8000XXh
ch	4	Cache Line Latency Header and BIST (CLLATHEADERBIST)	800000h
10h	4	Base Address (BAR)	4h
14h	4	Base Address Register High (BAR_HIGH)	0h
18h	4	Base Address 1 (BAR1)	4h
1ch	4	Base Address 1 High (BAR1_HIGH)	0h
2ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)	0h
34h	4	Capabilities Pointer (CAPABILITYPTR)	80h
3ch	4	Interrupt Register (INTERRUPTREG)	100h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
80h	4	Power Management Capability ID (POWERCAPID)	39001h
84h	4	Power Management Control and Status (PMECTRLSTATUS)	8h
90h	4	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)	F0140009h
98h	4	SW LTR update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)	2101h
9ch	4	Device IDLE Pointer (DEVICE_IDLE_POINTER_REG)	24C1h
a0h	4	Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)	F0800h
b0h	4	General Purpose Read Write 1 (GEN_REGRW1)	0h
b4h	4	General Purpose PCI Read Write 2 (GEN_REGRW2)	0h
b8h	4	General Purpose PCI Read Write 3 (GEN_REGRW3)	0h
bch	4	General Purpose PCI Read Write 4 (GEN_REGRW4)	0h
c0h	4	General Purpose Input (GEN_INPUT_REG)	0h

Device ID and Vendor ID (DEVVENDID) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:16	See Description	RO	**Device Identification (DEVICEID)** This is a 16-bit value assigned to the controller. See the Device and Revision ID Table in Volume 1 for the default value.

Bit Range	Default	Access	Field Name and Description
15:0	8086h	RO	**Vendor ID (VENDORID)** Identifies the manufacturer of the device. 8086h = Intel.

Status and Command (STATUSCOMMAND) – Offset 4

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29	0h	RW/1C	**Received Master Abort (RMA)** S/W writes a '1' to this bit to clear it.
28	0h	RW/1C	**Received Target Abort (RTA)** S/W writes a '1' to this bit to clear it.
27:21	-	-	**Reserved**
20	1h	RO	**Capabilities List (CAPLIST)** Indicates that the controller contains a capabilities pointer list.
19	0h	RO	**Interrupt Status (INTR_STATUS)** This bit reflects state of interrupt in the device.
18:11	-	-	**Reserved**
10	0h	RW	**Interrupt Disable (INTR_DISABLE)** Setting this bit disables INTx assertion. The interrupt disabled is legacy INTx# interrupt. This bit has no connection with interrupt status bit.

Bit Range	Default	Access	Field Name and Description
9	-	-	**Reserved**
8	0h	RW	**SERR Enable (SERR_ENABLE)** Not implemented.
7:3	-	-	**Reserved**
2	0h	RW	**Bus Master Enable (BME)** If this bit is 0, the controller does not generate any new upstream transaction as a master.
1	0h	RW	**Memory Space Enable (MSE)** 0 = Disables memory mapped Configuration space. 1 = Enables memory mapped configuration space.
0	-	-	**Reserved**

Revision ID and Class Code (REVCLASSCODE) – Offset 8

Bit Range	Default	Access	Field Name and Description
31:8	0C8000h	RO	**Class Codes (CLASS_CODES)** Class Code register is read-only and is used to identify the generic function of the device, and in some cases, a specific register-level programming interface
7:0	See Description	RO	**Revision ID (RID)** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

Cache Line Latency Header and BIST (CLLATHEADERBIST) – Offset c

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	1b	RO	**Multi Function Device (MULFNDEV)** 0 = Single Function Device 1 = Multi Function device
22:16	00h	RO	**Header Type (HEADERTYPE)** Implements Type 0 Configuration header.
15:8	00h	RO	**Latency Timer (LATTIMER)** Hardwired to 0.
7:0	00h	RW	**Cache Line Size (CACHELINE_SIZE)**

Base Address (BAR) – Offset 10

Bit Range	Default	Access	Field Name and Description
31:12	00000h	RW	**Base Address (BASEADDR)** Provides system memory base address for the controller.
11:4	00h	RO	**Size Indicator (SIZEINDICATOR)** Always returns 0. The size of this register depends on the size of the memory space.
3	0h	RO	**Prefetchable (PREFETCHABLE)** 0 indicates that this BAR is not prefetchable.
2:1	10b	RO	**Type (TYPE)** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range, If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h	RO	**Memory Space Indicator (MESSAGE_SPACE)** 0 indicates this BAR is present in the memory space.

Base Address Register High (BAR_HIGH) – Offset 14

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Base Address High (BASEADDR_HIGH)**

Base Address 1 (BAR1) – Offset 18

Bit Range	Default	Access	Field Name and Description
31:12	00000h	RW	**Base Address1 (BASEADDR1)** This field is present if BAR1 is enabled.
11:4	00h	RO	**Size Indicator (SIZEINDICATOR1)** Always is 0 as minimum size is 4K
3	0h	RO	**Prefetchable (PREFETCHABLE1)** 0 indicates that this BAR is not prefetchable.
2:1	2h	RO	**Type (TYPE1)** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h	RO	**Memory Space Indicator (MESSAGE_SPACE1)** 0 indicates this BAR is present in the memory space.

Base Address 1 High (BAR1_HIGH) – Offset 1c

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Base Address 1 High (BASEADDR1_HIGH)**

Subsystem Vendor and Subsystem ID (SUBSYSTEMID) – Offset 2c

Subsystem Vendor and Subsystem ID (SUBSYSTEMID) – Offset 2c

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/O	**Subsystem ID (SUBSYSTEMID)** The register, in combinationwith the Subsystem Vendor ID register make it possible for theoperating environment to distinguish one subsystem from theother. This register is a Read Write Once type register.
15:0	0000h	RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID)** The register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from theother. This register is a Read Write Once register.

Capabilities Pointer (CAPABILITYPTR) – Offset 34

Capabilities Pointer register indicates what the next capability is

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	80h	RO	**Capabilities Pointer (CAPPTR_POWER)** Indicates what the next capability is.

Interrupt Register (INTERRUPTREG) – Offset 3c

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO	**Max Latency (MAX_LAT)** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h	RO	**Min Latency (MIN_GNT)** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
11:8	1h	RO	**Interrupt Pin (INTPIN)**
7:0	00h	RW	**Interrupt Line (INTLINE)** It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

Power Management Capability ID (POWERCAPID) – Offset 80

Bit Range	Default	Access	Field Name and Description
31:27	00h	RO	**PME Support (PMESUPPORT)** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for for a bit indicates that the function is not capable of asserting the PME# signal while in that power state. Bit 27 = 1: PME# can be asserted from D0. Bit 30 = 1: PME# can be asserted from D3 hot. Other bits are not used.
26:19	-	-	**Reserved**
18:16	3h	RO	**Version (VERSION)** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h	RO	**Next Capability (NXTCAP)** Points to the next capability structure.
7:0	01h	RO	**Power Management Capability (POWER_CAP)** Indicates power management capability.

Power Management Control and Status (PMECTRLSTATUS) – Offset 84

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15	0h	RW/1C	**PME Status (PMESTATUS)**
14:9	-	-	**Reserved**
8	0h	RW	**PME Enable (PMEENABLE)** 0 = PME message is disabled 1 = PME message is enabled.
7:4	-	-	**Reserved**
3	1h	RO	**No Soft Reset (NO_SOFT_RESET)** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	-	-	**Reserved**
1:0	0h	RW	**Power State (POWERSTATE)** This field is used both todetermine the current power state and to set a new power state.The values are:00 = D0 state11 = D3HOT stateOthers = ReservedNotes: If software attempts to write a value of 01b or 10b in to this field,the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked.

PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD) – Offset 90

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:28	0Fh	RO	**Vendor Capability (VEND_CAP)** Vendor Specific Capability ID
27:24	0h	RO	**Revision ID (REVID)** Revision ID of capability structure
23:16	14h	RO	**Capability Length (CAP_LENGTH)** Vendor Specific Capability Length
15:8	00h	RO	**Next Capability (NEXT_CAP)** Points to the next capabilitystructure. This points to NULL.
7:0	09h	RO	**Capability ID (CAPID)**

SW LTR update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG) – Offset 98

Software location pointer in MMIO space as an offset specified by BAR

Bit Range	Default	Access	Field Name and Description
31:4	0000210h	RO	**Location Pointer Offset (SW_LAT_DWORD_OFFSET)** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h	RO	**Bar Number (SW_LAT_BAR_NUM)** Indicates that the SW LTR update MMIO location is always at BAR0
0	1h	RO	**Valid (SW_LAT_VALID)**

Device IDLE Pointer (DEVICE_IDLE_POINTER_REG) – Offset 9c

Device IDLE pointer register giving details on Device MMIO offset location , BAR NUM and D0i3 Valid Strap

Bit Range	Default	Access	Field Name and Description
31:4	000024Ch	RO	**Device Idle Pointer (DWORD_OFFSET)** Contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR
3:1	0h	RO	**Bar Number (BAR_NUM)** Indicates that the D0i3 MMIO location is always at BAR0.
0	1h	RO	**Valid (VALID)** 0 = Not valid1 = Valid

Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG) – Offset a0

Bit Range	Default	Access	Field Name and Description
30:20	-	-	**Reserved**
19	1b	RW	**Sleep Enable (SLEEP_EN)**
18	1b	RW	**Power Gate Enable (PGE)** If clear, the controller will never request a PG. If 1, then the function will power gate when idle and the DevIdle bit is set.
17	1b	RW	**D3-Hot Enable (I3_ENABLE)** If 1, then function will power gate when idle and the POWERSTATE bits in the function = 11 (D3).
16	1b	RW	**PMC Request Enable (PMCRE)** If this bit is set to '1', thefunction will power gate when idle.
15:13	-	-	**Reserved**
12:10	2h	RW/O	**Power On Latency Scale (POW_LAT_SCALE)** This value is written by BIOS to communicate to the Driver.

Bit Range	Default	Access	Field Name and Description
9:0	000h	RW/O	**Power On Latency value (POW_LAT_VALUE)** This value is written by BIOS to communicate to the Driver.

General Purpose Read Write 1 (GEN_REGRW1) – Offset b0

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**General Purpose PCI (GEN_REG_RW1)** General purpose read write PCI register.

General Purpose PCI Read Write 2 (GEN_REGRW2) – Offset b4

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**General Purpose PCI (GEN_REG_RW2)** General purpose read write PCI register.

General Purpose PCI Read Write 3 (GEN_REGRW3) – Offset b8

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**General Purpose PCI (GEN_REG_RW3)** General purpose read write PCI register.

General Purpose PCI Read Write 4 (GEN_REGRW4) – Offset bc

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**General Purpose PCI (GEN_REG_RW4)** General purpose read write PCI register.

General Purpose Input (GEN_INPUT_REG) – Offset c0

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RO	**General Purpose Input (GEN_REG_INPUT_RW)** General purpose input register.

IDE Redirect PCI Configuration (D22:F2) Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID (IDE_HOST_DID_VID)	XXXX8086h
4h	4	Status And Command (IDE_HOST_STS_CMD)	B00000h
8h	4	Class Code And Revision ID (IDE_HOST_CC_RID)	1018500h
ch	4	BIST, Header Type, Latency Timer, And Cache Line Size (IDE_HOST_BIST_HTYPE_LT_CLS)	800000h
10h	4	IDE Primary Command Block IO BAR (IDE_HOST_PCMDIOBAR)	1h
14h	4	IDE Primary Control Block IO BAR (IDE_HOST_PCTLIOBAR)	1h
18h	4	IDE Secondary Command Block IO BAR (IDE_HOST_SCMDIOBAR)	1h
1ch	4	IDE Secondary Control Block IO BAR (IDE_HOST_SCTLIOBAR)	1h
20h	4	IDE Bus Master Block IO BAR (IDE_HOST_BMIOBAR)	1h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2ch	4	Subsystem ID And Subsystem Vendor ID (IDE_HOST_SID_SVID)	8086h
34h	4	Capabilities List Pointer (IDE_HOST_CAPP)	40h
3ch	4	Maximum Latency, Minimum Grant, Interrupt Pin And Interrupt Line (IDE_HOST_MAXL_MING_INTP_INTL)	0h
40h	4	MSI Message Control, Next Pointer And Capability ID (IDE_HOST_MSIMC_MSINP_MSICID)	805005h
44h	4	MSI Message Address (IDE_HOST_MSIMA)	0h
48h	4	MSI Message Upper Address (IDE_HOST_MSIMUA)	0h
4ch	4	MSI Message Data (IDE_HOST_MSIMD)	0h
50h	4	Power Management Capabilities, Next Pointer And Capability ID (IDE_HOST_PMCAP_PMNP_PMCID)	230001h
54h	4	Power Management Data, Control/Status Register Bridge Support Extensions, Control And Status (IDE_HOST_PMD_PMCSRBSE_PMCSR)	8h

Device ID And Vendor ID (IDE_HOST_DID_VID) – Offset 0

This register contains the device ID and vendor ID values.

Bit Range	Default	Access	Field Name and Description
31:16	See Description	RO/V	**Device ID (DID)** This field identifies the particular device. Refer to the Device and Revision ID Table in Volume 1 for default value.
15:0	8086h	RO	**Vendor ID (VID)** This field identifies the manufacturer of the device. The value of 0x8086 indicates Intel.

Status And Command (IDE_HOST_STS_CMD) – Offset 4

This register contins the PCI status and command registers.

Bit Range	Default	Access	Field Name and Description
31	0b	RO	**Detected Parity Error (DPE)** Not implemented. Hardwired to 0.
30	0b	RO	**Signaled System Error (SSE)** Not implemented. Hardwired to 0.
29	0b	RW/1C/V	**Received Master Abort (RMA)** This bit must be set by a master device whenever its transaction (except for Special Cycle) is completed with Unsupported Request Completion Status (a.k.a. Master-Abort). All master devices must implement this bit.
28	0b	RW/1C/V	**Received Target Abort (RTA)** This bit must be set by a master device whenever its transaction is completed with Completer Abort Completion Status (a.k.a. Target-Abort). All master devices must implement this bit.
27	0b	RW/1C/V	**Signaled Target Abort (STA)** This bit must be set by a target device whenever it completes a Posted or Non-Posted transaction with a Completer Abort (a.k.a. Target-Abort) error. Devices that will never signal Completer Abort (a.k.a. Target-Abort) do not need to implement this bit.

Bit Range	Default	Access	Field Name and Description
26:25	00b	RO	**Devsel Timing (DEVT)** These bits encode the timing of DEVSEL#. There are three allowable timings for assertion of DEVSEL# as described below: 00b: fast; 01b: medium; 10b: slow; 11b: reserved. These bits are read-only and must indicate the slowest time that a device asserts DEVSEL# for any bus command except Configuration Read and Configuration Write. Hardwired to 00b.
24	0b	RO	**Master Data Parity Error (MDPE)** Not implemented. Hardwired to 0.

Bit Range	Default	Access	Field Name and Description
23	1b	RO	**Fast Back To Back Capable (FBTBC)** This bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. This bit can be set to 1 if the device can accept these transactions and must be set to 0 otherwise. Hardwired to 1.
22	-	-	**Reserved**
21	1b	RO	**66 Mhz Capable (MCAP)** This bit indicates whether or not this device is capable of running at 66 MHz. A value of 0 indicates 33 MHz. A value of 1 indicates that the device is 66 MHz capable. Hardwired to 1.

Bit Range	Default	Access	Field Name and Description
20	1b	RO	**Capabilities List (CAPL)** This optional read-only bit indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. A value of zero indicates that no New Capabilities linked list is available. A value of one indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities.
19	0b	RO	**Interrupt Status (INTS)** This read-only bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. Read-only and hardwired to 0 for a device that does NOT support pin-based interrupt.
18:11	-	-	**Reserved**
10	0b	RW	**Interrupt Disable (INTD)** This bit disables the device/function from asserting INTx#. A value of 0 enables the assertion of its INTx# signal. A value of 1 disables the assertion of its INTx# signal. This bit's state after RST# is 0.
9	0b	RO	**Fast Back To Back Enable (FBTBEN)** Not implemented. Hardwired to 0.
8	0b	RO	**System Error Enable (SERREN)** Not implemented. Hardwired to 0.
7	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
6	0b	RO	**Parity Error Response (PERRR)** Not implemented. Hardwired to 0.
5	0b	RO	**VGA Palette Snoop (VGAPS)** Not implemented. Hardwired to 0.
4	0b	RO	**Memory Write And Invalidate Enable (MWRIEN)** Not implemented. Hardwired to 0.
3	0b	RO	**Special Cycles (SPCYC)** Not implemented. Hardwired to 0.
2	0b	RW	**Bus Master Enable (BME)** This bit controls the PCI device's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transactioncommands.
1	0b	RO	**Memory Space Enable (MSE)** Read-only and hardwired to 0 because IDE does NOT support Memory Space accesses.
0	0b	RW	**IO Space Enable (IOSE)** Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after RST# is 0.

Class Code And Revision ID (IDE_HOST_CC_RID) – Offset 8

This register contains the class code and revision ID values.

Bit Range	Default	Access	Field Name and Description
31:24	01h	RO	**Base Class Code (BCC)** Identifies the Base Class Code of an external IDE controller device driver.
23:16	01h	RO	**Sub-Class Code (SCC)** Identifies the Sub-Class Code of an external IDE controller device driver.

Bit Range	Default	Access	Field Name and Description
15:8	85h	RO	**Programming Interface (PI)** Identifies the Programming Interface of an IDE controller device driver.
7:0	See Description	RO/V	**Revision ID (RID)** This register specifies a device specific revision identifier. Refer to Device and Revision ID table in Vol1 for specific value.

BIST, Header Type, Latency Timer, And Cache Line Size (IDE_HOST_BIST_HTYPE_LT_CLS) – Offset c

This register contains the BIST, header type, latency timer, and cache line size values.

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO	**Built In Self Test (BIST)** Not implemented. Hardwired to 0.
23	1b	RO/V	**Header Type 1 (HTYPE1)** This bit identifies whether or not the device contains multiple functions. - If the bit is 0, then the device is single function. - If the bit is 1, then the device has multiple functions.
22:16	00h	RO	**Header Type 0 (HTYPE0)** Hardwired to 0 to identify the non-bridge Configuration Space Header.
15:8	00h	RO	**Latency Timer (LT)** Not implemented. Hardwired to 0.
7:0	00h	RO	**Cache Line Size (CLS)** Not implemented. Hardwired to 0.

IDE Primary Command Block IO BAR (IDE_HOST_PCMDIOBAR) – Offset 10

This is the IO space base address register.

Bit Range	Default	Access	Field Name and Description
31:3	0000_0000h	RW	**IO BAR (IOBAR)** Software programs this space with the base address of the device's IO region
2	0b	RO	**IO Size (IOSIZE)** Hardwired to 0 to indicate 8B of IO space
1	-	-	**Reserved**
0	1b	RO	**IO Space Indicator (IOSPACE)** Hardwired to 1 to identify an IO BAR.

IDE Primary Control Block IO BAR (IDE_HOST_PCTLIOBAR) – Offset 14

This is the IO space base address register.

Bit Range	Default	Access	Field Name and Description
31:2	0000_0000h	RW	**IO BAR (IOBAR)** Software programs this space with the base address of the device's IO region
1	-	-	**Reserved**
0	1b	RO	**IO Space Indicator (IOSPACE)** Hardwired to 1 to identify an IO BAR.

IDE Secondary Command Block IO BAR (IDE_HOST_SCMDIOBAR) –

Offset 18

This is the IO space base address register.

Bit Range	Default	Access	Field Name and Description
31:3	0000_0000h	RW	**IO BAR (IOBAR)** Software programs this space with the base address of the device's IO region
2	0b	RO	**IO Size (IOSIZE)** Hardwired to 0 to indicate 8B of IO space
1	-	-	**Reserved**
0	1b	RO	**IO Space Indicator (IOSPACE)** Hardwired to 1 to identify an IO BAR.

IDE Secondary Control Block IO BAR (IDE_HOST_SCTLIOBAR) – Offset 1c

This is the IO space base address register.

Bit Range	Default	Access	Field Name and Description
31:2	0000_0000h	RW	**IO BAR (IOBAR)** Software programs this space with the base address of the device's IO region
1	-	-	**Reserved**
0	1b	RO	**IO Space Indicator (IOSPACE)** Hardwired to 1 to identify an IO BAR.

IDE Bus Master Block IO BAR (IDE_HOST_BMIOBAR) – Offset 20

This is the IO space base address register.

Bit Range	Default	Access	Field Name and Description
31:4	000_0000h	RW	**IO BAR (IOBAR)** Software programs this space with the base address of the device's IO region
3:2	00b	RO	**IO Size (IOSIZE)** Hardwired to 0 to indicate 16B of IO space
1	-	-	**Reserved**
0	1b	RO	**IO Space Indicator (IOSPACE)** Hardwired to 1 to identify an IO BAR.

Subsystem ID And Subsystem Vendor ID (IDE_HOST_SID_SVID) – Offset 2c

These registers are used to uniquely identify the add-in card or subsystem where the PCI device resides. They provide a mechanism for add-in card vendors to distinguish their add-in cards from one another even though the add-in cards may have the same PCI controller on them (and, therefore, the same Vendor ID and Device ID).

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/O	**Subsystem ID (SID)** Value of this field is vendor-specific. This is written by BIOS. No hardware action will be taken on this value.
15:0	8086h	RW/O	**Subsystem Vendor ID (SVID)** This field identifies the vendor of the add-in card or subsystem. This is written by BIOS. No hardware action will be taken on this value.

Capabilities List Pointer (IDE_HOST_CAPP) – Offset 34

This register contains the capabilities list pointer.

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	40h	RO	**Capabilities Pointer (CAPP)** Indicates the pointer for the first entry in the capabilities list which is the MSI Capability.

Maximum Latency, Minimum Grant, Interrupt Pin And Interrupt Line (IDE_HOST_MAXL_MING_INTP_INTL) – Offset 3c

This register contains the maximum latency, minumum grand, interrupt pin and interrupt level registers.

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO	**Maximum Latency (MAXL)** Not implemented. Hardwired to 0.
23:16	00h	RO	**Minimum Grant (MING)** Not implemented. Hardwired to 0.
15:8	00h	RO/V	**Interrupt Pin (INTP)** This register specifies which interrupt pin IDE uses in PCI interrupt mode. Value Decoding 00h The function does NOT use an interrupt pin. 01h INTA 02h INTB 03h INTC 04h INTD 05h - FFh Reserved.
7:0	00h	RW	**Interrupt Line (INTL)** The value written in this register indicates which input of thesystem interrupt controller, the device's interrupt pin is connected to. This value is used by theoperating system and the device driver, and has no affect on the hardware

MSI Message Control, Next Pointer And Capability ID (IDE_HOST_MSIMC_MSINP_MSICID) – Offset 40

This register contains the MSI message control, next pointer And capability ID values.

Bit Range	Default	Access	Field Name and Description
30:25	-	-	**Reserved**
24	0b	RO	**Per Vector Masking Capable (PVMC)** Not implemented. Hardwired to 0 to indicate the function does NOT support MSI per-vector masking.
23	1b	RO	**64 Bit Address Capable (XAC)** Hardwired to 1 to indicate the function is capable of sending a 64-bit message address.
22:20	000b	RW	**Multiple Message Enable (MMEN)** Encoded number of interrupt vectors allocated by SW. This field is RW for software compatibility, but only one interrupt vector is ever sent by the function.
19:17	000b	RO	**Multiple Message Capable (MMC)** Encoded number of interrupt vectors requested by a device. Hardwired to 0 to indicate one requested interrupt vector.
16	0b	RW	**MSI Enable (MSIE)** If set, MSI interrupt delivery is enabled whereas pin-based interrupt delivery SHALL be disabled. If cleared, prior to returning the configuration write (that clears this field) completion, the function must send any pending MSI(s).

Bit Range	Default	Access	Field Name and Description
15:8	50h	RO	**Next Item Pointer (NP)** Indicates the pointer for the next entry in the capabilities list. Hardwired to 50h to point to the PM Capability list
7:0	05h	RO	**Capability ID (CID)** Hardwired to 05h to indicate the linked list item as the MSI Capability registers

MSI Message Address (IDE_HOST_MSIMA) – Offset 44

This register contains the MSI message address value.

Bit Range	Default	Access	Field Name and Description
31:2	0000_0000h	RW	**Message Address (MA)** 32-bit DW-aligned MSI message address.
1:0	-	-	**Reserved**

MSI Message Upper Address (IDE_HOST_MSIMUA) – Offset 48

This register contains the MSI message upper address value.

Bit Range	Default	Access	Field Name and Description
31:0	0000_0000h	RW	**Message Upper Address (MUA)** Upper 32-bit of a 64-bit DW-aligned MSI message address.

MSI Message Data (IDE_HOST_MSIMD) – Offset 4c

This register contains the MSI message data register.

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0000h	RW	**Message Data (MD)** MSI Message Data

Power Management Capabilities, Next Pointer And Capability ID (IDE_HOST_PMCAP_PMNP_PMCID) – Offset 50

This register contains the power management capabilities, next pointer And capability ID values.

Bit Range	Default	Access	Field Name and Description
31:27	00000b	RO	**PME Support (PMES)** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(27) X XXX1b - PME# can be asserted from D0 bit(28) X XX1Xb - PME# can be asserted from D1 bit(29) X X1XXb - PME# can be asserted from D2 bit(30) X 1XXXb - PME# can be asserted from D3hot bit(31) 1 XXXXb - PME# can be asserted from D3cold
26	0b	RO	**D2 Support (D2S)** Hardwired to 0 to indicate that this device does not support D2

Bit Range	Default	Access	Field Name and Description
25	0b	RO	**D1 Support (D1S)** Hardwired to 0 to indicate that this device does not support D1
24:22	000b	RO	**Aux Current (AUXC)** Not implemented. Hardwired to 0.
21	1b	RO	**Device Specific Initialization (DSI)** indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. A 1 indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state. Hardwired to 1 to indicate Device Specific Initialization is required.
20	-	-	**Reserved**
19	0b	RO	**PME Clock (PMECLK)** Not implemented. Hardwired to 0.
18:16	011b	RO	**Version (VER)** Hardwired to value of 011b indicates that this function complies with rev 1.2 of PCI Power Management Interface Spec
15:8	00h	RO	**Next Item Pointer (NP)** Indicates the pointer for the next entry in the capabilities list. Hardwired to 0 to indicate no more linked list item.
7:0	01h	RO	**Capability ID (CID)** Hardwired to 01h to indicate the linked list item as the PCI Power Management registers

Power Management Data, Control/Status Register Bridge Support Extensions, Control And Status (IDE_HOST_PMD_PMCSRBSE_PMCSR) – Offset 54

This register contains the power management data, control and status register bridge support extensions, control and status registers.

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO	**Data (Data)** Not implemented. Hardwired to 0.
23:16	00h	RO	**Control/Status Register Bridge Support Extensions (CSRBSE)** Not implemented. Hardwired to 0.
15	0b	RO	**PME Status (PMESTS)** Not implemented. Hardwired to 0.
14:13	00b	RO	**Data Scale (DS)** Not implemented. Hardwired to 0.
12:9	0000b	RO	**Data Select (DSEL)** Not implemented. Hardwired to 0.
8	0b	RO	**PME Enable (PMEEN)** Not implemented. Hardwired to 0.
7:4	-	-	**Reserved**
3	1b	RO	**No Soft Reset (NSR)** When set to 1, this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.

Bit Range	Default	Access	Field Name and Description
2	-	-	**Reserved**
1:0	00b	RW	**Power State (PWRST)** This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below: 00b - D0 01b - D1 10b - D2 11b - D3hot If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs.

Integrated Clock (ICC) Configuration Registers

The Integrated Clock Controller Configuration Registers are distributed within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface using the following Target Port (Destination Port) Identification:

Target Port (Destination Port) Identification = 0xAD

For complete details on how to use the PCH Sideband Interface to access these PCH Private Configuration Registers reference the latest CNL Platform Controller Hub BIOS Specification.

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
22e4h	4	CMU_ONE_DWORD25 (cmu_one_dword25)	543210h

CMU_ONE_DWORD25 (cmu_one_dword25) – Offset 22e4

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:20	5h	RW	**SRCCLKREQ# Select For CLKOUT_PCIE5 (CRQSELSRC5)** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE5 0000: SRCCLKREQ#_0 controls CLKOUT_PCIE5 0001: SRCCLKREQ#_1 controls CLKOUT_PCIE5 0010: SRCCLKREQ#_2 controls CLKOUT_PCIE5 0011: SRCCLKREQ#_3 controls CLKOUT_PCIE5 0100: SRCCLKREQ#_4 controls CLKOUT_PCIE5 0101: SRCCLKREQ#_5 controls CLKOUT_PCIE5(default) 0110-1111: Reserved

Bit Range	Default	Access	Field Name and Description
19:16	4h	RW	**SRCCLKREQ# Select For CLKOUT_PCIE4 (CRQSELSRC4)** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE4 0000: SRCCLKREQ#_0 controls CLKOUT_PCIE4 0001: SRCCLKREQ#_1 controls CLKOUT_PCIE4 0010: SRCCLKREQ#_2 controls CLKOUT_PCIE4 0011: SRCCLKREQ#_3 controls CLKOUT_PCIE4 0100: SRCCLKREQ#_4 controls CLKOUT_PCIE4(default) 0101: SRCCLKREQ#_5 controls CLKOUT_PCIE4 0110-1111: Reserved
15:12	3h	RW	**SRCCLKREQ# Select For CLKOUT_PCIE3 (CRQSELSRC3)** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE3 0000: SRCCLKREQ#_0 controls CLKOUT_PCIE3 0001: SRCCLKREQ#_1 controls CLKOUT_PCIE3 0010: SRCCLKREQ#_2 controls CLKOUT_PCIE3 0011: SRCCLKREQ#_3 controls CLKOUT_PCIE3(default) 0100: SRCCLKREQ#_4 controls CLKOUT_PCIE3 0101: SRCCLKREQ#_5 controls CLKOUT_PCIE3 0110-1111: Reserved

Bit Range	Default	Access	Field Name and Description
11:8	2h	RW	**SRCCLKREQ# Select For CLKOUT_PCIE2 (CRQSELSRC2)** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE2 0000: SRCCLKREQ#_0 controls CLKOUT_PCIE2 0001: SRCCLKREQ#_1 controls CLKOUT_PCIE2 0010: SRCCLKREQ#_2 controls CLKOUT_PCIE2(default) 0011: SRCCLKREQ#_3 controls CLKOUT_PCIE2 0100: SRCCLKREQ#_4 controls CLKOUT_PCIE2 0101: SRCCLKREQ#_5 controls CLKOUT_PCIE2 0110-1111: Reserved
7:4	1h	RW	**SRCCLKREQ# Select For CLKOUT_PCIE1 (CRQSELSRC1)** SRCCLKREQ# Select for CLKOUT_PCIE1 (CRQSELSRC1): Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE1 0000: SRCCLKREQ#_0 controls CLKOUT_PCIE1 0001: SRCCLKREQ#_1 controls CLKOUT_PCIE1(default) 0010: SRCCLKREQ#_2 controls CLKOUT_PCIE1 0011: SRCCLKREQ#_3 controls CLKOUT_PCIE1 0100: SRCCLKREQ#_4 controls CLKOUT_PCIE1 0101: SRCCLKREQ#_5 controls CLKOUT_PCIE1 0110-1111: Reserved

Bit Range	Default	Access	Field Name and Description
3:0	0h	RW	**SRCCLKREQ# Select For CLKOUT_PCIE0 (CRQSELSRC0)** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE0 0000: SRCCLKREQ#_0 controls CLKOUT_PCIE0 (default) 0001: SRCCLKREQ#_1 controls CLKOUT_PCIE0 0010: SRCCLKREQ#_2 controls CLKOUT_PCIE0 0011: SRCCLKREQ#_3 controls CLKOUT_PCIE0 0100: SRCCLKREQ#_4 controls CLKOUT_PCIE0 0101: SRCCLKREQ#_5 controls CLKOUT_PCIE0 0110-1111: Reserved

Intel RST for PCIe Storage (Remapping) PCI Configuration (D24:F0) Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
24h	4	AHCI Base Address (ABAR)	0h
300h	4	General Configuration Register (GCR)	2h
304h	4	General Status Register (GSR)	1Eh
308h	4	Configuration Access Index Register (CAIR)	0h
30ch	4	Configuration Access Data Register (CADR)	0h
310h	4	Memory BAR Remap Configuration (MBRC)	90009h
320h	4	I/O Remap Source Configuration (IOBRSC)	48h
338h	4	AHCI Index/Data Pair Capability Remap Configuration (AIDPCRC)	A800A8h
33ch	4	MSI-X Capability Remap Configuration (MXCRC)	D000D0h
340h	4	MSI-X Table Remap Configuration (MXTRC)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
344h	4	MSI-X Table Base Address Register (MXTBAR)	0h
348h	4	MSI-X PBA Remap Configuration (MXPRC)	0h
34ch	4	MSI-X PBA Base Address (MXPBAR)	0h
350h	4	NVM Remapping Device:Function (NRDF)	C00000h
354h	4	Extended General Configuration Register (EGCR)	0h
358h	4	Shadowed AHCI Ports Implemented (SAPI)	0h
368h	2	Remapping Host Device Function (RHDF)	0h
fc0h	4	Cycle Router Global Control (CRGC)	0h
fc4h	4	Fuse DW0 (FDW0)	0h

AHCI Base Address (ABAR) – Offset 24

This register represents a memory BAR allocating space for the AHCI memory registers. Note that bit[31:16] of this register must be programmed to a value greater than 0 to ensure the memory is mapped to an address of 1 MBytes and greater (i.e. ABAR must be 00010000h or greater). Otherwise, memory cycle targeting the ABAR range may not be accepted.. The Memory space size is determined by BIOS by making bit 15:11 Read-Only '1' or Read-Write '0' based on SATAGC.ASSEL[1:0].

Bit Range	Default	Access	Field Name and Description
31:19	0h	RW	**Base Address (BA)** Base address of register memory space.
18	0h	RW	**Base Address Bit 18 (BAB18)** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 256K, this bit is Read Only '0' else it's Read Write '0'.
17	0h	RW	**Base Address Bit 17 (BAB17)** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 128K, this bit is Read Only '0' else it's Read Write '0'.

Bit Range	Default	Access	Field Name and Description
16	0h	RW	**Base Address Bit 16 (BAB16)** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 64K, this bit is Read Only '0' else it's Read Write '0'.
15	0h	RW	**Base Address Bit 15 (BAB15)** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 32K, this bit is Read Only '0' else it's Read Write '0'.
14	0h	RW	**Base Address Bit 14 (BAB14)** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 16K, this bit is Read Only '0' else it's Read Write '0'.
13:11	0h	RW	**Base Address Bit 13-11 (BAB1311)** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 2K, this bit is Read Only '0' else it's Read Write '0'.
10:4	-	-	**Reserved**
3	0h	RO	**Prefetchable (PF)** Indicates that this range is not pre-fetchable
2:1	0h	RO	**Type (TP)** Indicates that this range can be mapped anywhere in 32-bit address space
0	0h	RO	**Resource Type Indicator (RTE)** Indicates a request for register memory space.

General Configuration Register (GCR) – Offset 300

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**Cycle Router Enable Lockdown (CREL)** When this bit is set to '1', the GCR.CRE bit is locked down and cannot be written by any subsequent cycles. Once set to '1', this bit is only cleared by PLTRST#.

Bit Range	Default	Access	Field Name and Description
30	0b	RW/L	**Remapping Configuration Lockdown (RCL)** When this bit is set to '1', the following registers are locked down and cannot be written. Once set to '1', this bit is only cleared by PLTRST#. Memory BAR Remap Configuration (MBRC) I/O BAR Remap Source Configuration (IOBRSC) I/O BAR Remap Target Configuration (IOBRTC) Power Management Capability Remap Configuration (PMCRC) MSI Capability Remap Configuration Remap (MCRC) AHCI Index/Data Pair Capability Remap Configuration (AIDPCRC) MSI-X Capability Remap Configuration (MXCRC) MSI-X Table Remap Configuration (MXTRC) MSI-X Table Base Address Register (MXTBAR) MSI-X PBA Remap Configuration (MXPRC) MSI-X PBA Base Address Register (MXPBAR) NVM Remapping Device:Function (NRDF) Shadowed AHCI Ports Implemented (SAPI)
29	0b	RW/L	**Configuration Access Index/Data Lockdown (CAIDL)** When this bit is set to '1', the following configuration access index/data registers are locked down and cannot be written. Once set to '1', this bit is only cleared by PLTRST#. Configuration Access Index Register (CAIR) Configuration Access Data Register (CADR)
28:21	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
20:1	0000000 0000000 000001b	RW	**PCIe Lane Selected (PLS)** This field is bit significant, and it corresponds to PCIe Lane [20:1]. It selects the PCIe lane(s) associated with this Cycle Router when enabled. This field must be valid when GCR.CRE bit is set to '1'. Only PCIe lane(s) that are remap capable as indicated by GSR.PLRC shall be selected. This shall be the lane(s) where PCIe SSD device is discovered during the initialization process. The number of '1' in this field indicates the PCIe lane width configured for this Cycle Router. They must be contiguous and begin at the appropriate lane that supporting the lane width associated with the PCIe root-port configuration. GCR bit[1] (GCR.PLS[0]) corresponds to the first lane of the first PCIe root-port, i.e. PCIe Port 1 Lane [0], and so on.
0	0b	RW/L	**Cycle Router Enable (CRE)** When set to '1', Cycle Router is enabled. When this bit is '0', Cycle Router is disabled and will not respond to cycles except accesses to the extended configuration registers in 300h-3FFh. This bit enables the path between Cycle Router and the PCIe Root-port as well as between Cycle Router and the AHCI controller. This bit is locked down and cannot be written when GCR.CREL bit is set to '1'. When GSR.PCCS is a '1', HW inhibits the write to set GCR.CRE bit to '1' due to a mismatch port configuration detected. After correcting the port configuration, BIOS is required to clear the GSR.PCCS bit before the attempt to set the GCR.CRE bit again.

General Status Register (GSR) – Offset 304

Bit Range	Default	Access	Field Name and Description
31	0b	RW	**Port Configuration Check Disable (PCCD)** When this bit is set to '1', internal port configuration check is disabled. When this bit is '0' (reset default), internal port configuration check is enabled. When enabled, port configuration check is performed by comparing the following. A mismatch detected will prevent the GCR.CRE bit from being set to 1. - Cycle Router x1, x2 or x4 soft strap - PCIe x1, x2 or x4 capability for the lane(s) selected by GCR.PLS and the associated PCIe root-port configuration

Bit Range	Default	Access	Field Name and Description
30	0b	RW/1C	**Port Configuration Check Status (PCCS)** This bit is set to '1' by hardware when internal port configuration check is enabled (GSR.PCCD='0') and a mismatch is detected. The bit is cleared to '0' by software writing a '1' to this bit position. This bit may be set (due to mismatch) before PCIe port configuration is configured correctly after reset. BIOS is required to examine and clear this bit accordingly before setting the GCR.CRE bit.
29:21	-	-	**Reserved**
20:1	0000Fh	RO	**PCIe Lanes Remap Capable (PLRC)** This field is bit significant, and it corresponds to PCIe Lane [20:1]. A '1' indicates the corresponding PCIe lane is remap capable with the option to select Cycle Router functionality on this lane. Lane [1] corresponds to the first lane of the first PCIe root-port, i.e. PCIe Port 1 Lane [0], and so on. Cycle Router#1 - 0000Fh Cycle Router#2 - 000F0h Cycle Router#3 - 00F00h
0	-	-	**Reserved**

Configuration Access Index Register (CAIR) – Offset 308

The Configuration Access Index/Data pair allows explicit access to the configuration space of the PCIe SSD device after Cycle Router is enabled.

This register is locked down and cannot be written when GCR.CAIDL bit is set to '1'.

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
11:0	000h	RW/L	**Configuration Register Offset (CRO)** This field specifies the configuration register offset for the access. The 12-bit offset allows access to the entire 4KB configuration space of the PCIe device.

Configuration Access Data Register (CADR) – Offset 30c

This register is locked down and cannot be written when GCR.CAIDL bit is set to '1'.

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW/L	**Configuration Register Data (CRD)** through which data is read or written to the configuration register of the PCIe device pointed by the Index register.

Memory BAR Remap Configuration (MBRC) – Offset 310

This register is locked down and cannot be written when GCR.RCL bit is set to '1'.

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**Remap Enable (RE)** When set to '1', remapping of this memory BAR is enabled. When the bit is '0', remapping of this memory BAR is disabled.
30:21	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
20	0b	RW/L	**Target Type (TT)** Indicates the type of target memory BAR. Bit Description 0: 32-bit BAR 1: 64-bit BAR

Bit Range	Default	Access	Field Name and Description
19:16	9h	RW/L	**Taget Memory BAR (TMB)** This field indicates the target memory BAR that will be remapped by Cycle Router. The field represents an absolute offset (DW increments) into PCI configuration space BAR registers. If the BAR is 64-bit, this field specifies offset of the lower BAR register. Bit Description 0100: 10h (BAR 0) 0101: 14h (BAR 1) 0110: 18h (BAR 2) 0111: 1Ch (BAR 3) 1000: 20h (BAR 4) 1001: 24h (BAR 5) Others: Reserved
15:5	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
4	0b	RO	**Source Type (ST)** Indicates the type of source memory BAR. Bit Description 0: 32-bit BAR 1: 64-bit BAR This bit is hardcoded to '0'. The ABAR of the integrated AHCI controller is a 32-bit BAR.
3:0	9h	RO	**Source Memory BAR (SMB)** This field indicates the source memory BAR that will be remapped by Cycle Router. The field represents an absolute offset (DW increments) into PCI configuration space BAR registers. This field is hardcoded to "1001" (9h). The ABAR of the integrated AHCI controller is implemented as BAR5.

I/O Remap Source Configuration (IOBRSC) – Offset 320

This register is locked down and cannot be written when GCR.RCL bit is set to '1'.

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**Remap Enable (RE)** When set to '1', remapping of this I/O BAR is enabled. When the bit is '0', remapping of this I/O BAR is disabled.
30:18	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
17:4	0000000 0000100 b	RO	**Source BAR Offset (SBO)** This field specifies the offset (DW increments) into Source I/O BAR (SIOB) where AHCI Index/Data pair registers are located. This field is hardcoded to "4h". The IDP of the integrated AHCI controller is implemented at offset 10h (i.e. 4h * 4) of its LBAR.
3:0	8h	RO	**Source I/O BAR (SIOB)** This field indicates the source I/O BAR that will be remapped by Cycle Router. The field represents an absolute offset (DW increments) into PCI configuration space BAR registers. The reset default is BAR 4. Bit Description 0100: 10h (BAR 0) 0101: 14h (BAR 1) 0110: 18h (BAR 2) 0111: 1Ch (BAR 3) 1000: 20h (BAR 4) 1001: 24h (BAR 5) Others: Reserved This field is hardcoded to "1000" (8h). The LBAR of the integrated AHCI controller is implemented as BAR4.

AHCI Index/Data Pair Capability Remap Configuration (AIDPCRC) – Offset 338

This register is locked down and cannot be written when GCR.RCL bit is set to '1'.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**Remap Enable (RE)** When set to '1', remapping of this capability structure is enabled. When the bit is '0', remapping of this capability structure is disabled.
30:24	-	-	**Reserved**
23:16	A8h	RW/L	**Target Capability Structure Offset (TCSO)** This field specifies the starting offset of the target capability structure. It must be DW-aligned.
15:8	-	-	**Reserved**
7:0	A8h	RW/L	**Source Capability Structure Offset (SCSO)** This field specifies the starting offset of the source capability structure. It must be DW-aligned.

MSI-X Capability Remap Configuration (MXCRC) – Offset 33c

This register is locked down and cannot be written when GCR.RCL bit is set to '1'.

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**Remap Enable (RE)** When set to '1', remapping of this capability structure is enabled. When the bit is '0', remapping of this capability structure is disabled.
30:24	-	-	**Reserved**
23:16	D0h	RW/L	**Target Capability Structure Offset (TCSO)** This field specifies the starting offset of the target capability structure. It must be DW-aligned.
15:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	D0h	RW/L	**Source Capability Structure Offset (SCSO)** This field specifies the starting offset of the source capability structure. It must be DW-aligned.

MSI-X Table Remap Configuration (MXTRC) – Offset 340

This register is locked down and cannot be written when GCR.RCL bit is set to '1'.

Bit Range	Default	Access	Field Name and Description
31:3	0000000 0h	RW/L	**Table Offset (TO)** Used as an offset from the address contained by one of the functions Base Address registers to point to the base of the MSI-X Table. The lower three Table BIR bits are masked off (cleared to 000b) by system software to form a 32-bit Qword-aligned offset.
2:0	000b	RW/L	

Bit Range	Default	Access	Table BIR (TBIR) Field Name and Description
			This field indicates which one of a functions Base Address registers, located beginning at 10h in Configuration Space, is used to map the functions MSI-X Table into system memory. BIR Value BAR Offset 0 10h 1 14h 2 18h 3 1Ch 4 20h 5 24h 6 Reserved

MSI-X Table Base Address Register (MXTBAR) – Offset 344

This register is locked down and cannot be written when GCR.RCL bit is set to '1'.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:1	0000000 0000000 0000000 0000000 000b	RW/L	**Table Base Address (TBA)** This is the value of the Base Address [31:01] assigned by BIOS to allocate separate resources for the memory BAR associated with the MSI-X Table on the PCIe SSD device. MSI-X table is located at starting address (MXTBAR.TBA[31:01] & '0' + MXTRC.TO & "000") in this case.
0	0b	RW/L	**Table Base Address Valid (TBAV)** This bit is set to '1' when BIOS has assigned separate resources for the memory BAR associated with the MSI-X Table on the PCIe SSD device and the Table Base Address (TBA) field is valid. This bit is '0' when no separate resources are required for the MSI-X Table, such as in the case MSI-X Table resides under the same memory BAR used by the Host Controller interface on the PCIe SSD device.

MSI-X PBA Remap Configuration (MXPRC) – Offset 348

This register is locked down and cannot be written when GCR.RCL bit is set to '1'.

Bit Range	Default	Access	Field Name and Description
31:3	0000000 0h	RW/L	**PBA Offset (PBAO)** Used as an offset from the address contained by one of the functions Base Address registers to point to the base of the MSI-X PBA. The lower three PBA BIR bits are masked off (cleared to 000b) by software to form a 32-bit Qword-aligned offset.
2:0	000b	RW/L	

Bit Range	Default	Access	PBA BIR (PBIR) Field Name and Description
			This field indicates which one of a functions Base Address registers, located beginning at 10h in Configuration Space, is used to map the functions MSI-X PBA into system memory. BIR Value BAR Offset 0 10h 1 14h 2 18h 3 1Ch 4 20h 5 24h 6 Reserved

MSI-X PBA Base Address (MXPBAR) – Offset 34c

This register is locked down and cannot be written when GCR.RCL bit is set to '1'.

Bit Range	Default	Access	Field Name and Description
31:1	0000000 0000000 0000000 0000000 000b	RW/L	**PBA Base Address (PBA)**) in this case.

Bit Range	Default	Access	Field Name and Description
0	0b	RW/L	**PBA Base Address Valid (PBAV)** This bit is set to '1' when BIOS has assigned separate resources for the memory BAR associated with the target MSI-X PBA of the PCIe SSD device and the PBA Base Address (PBA) field is valid. This bit is '0' when no separate resources are required for the target MSI-X PBA, such as in the case target MSI-X PBA resides under the same memory BAR used by the Host Controller interface of the PCIe SSD device

NVM Remapping Device:Function (NRDF) – Offset 350

This register is locked down and cannot be written when GCR.RCL bit is set to '1'.

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO/V	**Bus Number (BN)** This field reflects the Bus Number used for the PCIe NAND device. It is the captured Bus Number for the integrated AHCI controller as both devices are sitting on the same bus hierarchy.
23:19	18h	RW/L	**Device Number (DN)** This field specifies the reserved Device Number used internally for the communication with the PCIe NAND device. The reset default is Device 24.
18:16	000b	RW/L	**Function Number (FN)** This field specifies the reserved Function Number used internally for the communication with the PCIe NAND device. The reset default is Function 0.
15:0	-	-	**Reserved**

Extended General Configuration Register (EGCR) – Offset 354

Bit Range	Default	Access	Field Name and Description
30:21	-	-	**Reserved**
20	0b	RW	**To SATA CLKREQ Assertion Select (TSCAS)** When this bit is set to '1', internal CLKREQ assertion to SATA is triggered when cycle has been committed to SATA. When this bit is '0', internal CLKREQ assertion to SATA is triggered based on ISM in non-IDLE states.
19:18	-	-	**Reserved**
17	0b	RW	**Cycle Rouster Trunk Clock Gating Enable (CRTCGE)** When this bit is set to '1', trunk clock gating is enabled in Cycle Router. When this bit is '0' (reset default), trunk clock gating is disabled in Cycle Router.
16	0b	RW	**Cycle Router Dynamic Clock Gating Enable (CRDCGE)** When this bit is set to '1', dynamic local clock gating is enabled in Cycle Router. When this bit is '0' (reset default), dynamic local clock gating is disabled in Cycle Router.
15	0b	RW	**Single Remapping Mode (SRM)** When this bit is set to '1', for a downstream non-posted cycle that remap to multiple Cycle Routers or PCIe devices, the remapped non-posted requests to each of the Cycle Routers or PCIe devices are initiated one at a time, with subsequent request initiated only after the prior completion is received. When this bit is '0', the remapped non-posted requests to each of the Cycle Routers or PCIe devices are initiated back-to-back resulting in multiple non-posted pending without waiting for the completion of the prior cycle.
14:12	-	-	**Reserved**
11	0b	RW	**Downstream Configuration Flush Enable (DCFE)** When set to '1', all downstream configuration cycles to AHCI controller unrelated to PCIe device will still be forwarded by HW to the PCIe device with all byte enables inactive to achieve the flushing effect. When this bit is '0', all downstream configuration cycles to AHCI controller unrelated to PCIe device will not be forwarded by HW.

Bit Range	Default	Access	Field Name and Description
10	0b	RW	**Downstream I/O Flush Enable (DIOFE)** When set to '1', all downstream I/O cycles to AHCI controller outside the remapped range of PCIe device will still be forwarded by HW to the PCIe device with all byte enables inactive to achieve the flushing effect. When this bit is '0', all downstream I/O cycles to AHCI controller outside the remapped range of PCIe device will not be forwarded by HW.
9	0b	RW	**Downstream Memory Read Flush Enable (DMRFE)** When set to '1', all downstream memory reads to AHCI controller outside the remapped range of PCIe device will still be forwarded by HW to the PCIe device with all byte enables inactive to achieve the flushing effect. When this bit is '0', all downstream memory reads to AHCI controller outside the remapped range of PCIe device will not be forwarded by HW.
8	0b	RW	**MSI 64-bit Message Address Support (MSI64E)** When set, NAND Cycle Router shall enable the 64-bit message address support for MSI. When clear (default), NAND Cycle Router shall enable the 32-bit message address support for MSI.
7:0	-	-	**Reserved**

Shadowed AHCI Ports Implemented (SAPI) – Offset 358

This register is locked down and cannot be written when GCR.RCL bit is set to '1'.

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	000000b	RW/L	**Shadowed Ports Implemented (SPI)** This register is configured by BIOS to the same value as the Ports Implemented (PI) register at offset 0Ch of the AHCI global registers space. It is used by Cycle Router in the target cycle decoding. The AHCI PI register is also setup by BIOS. When BIOS configures the AHCI PI register, it is required to write the same value to this shadowed register for the proper operation of the Cycle Router.

Remapping Host Device Function (RHDF) – Offset 368

Bit Range	Default	Access	Field Name and Description
14:8	-	-	**Reserved**
7:0	0b	RW/L	**Remapping Host Device Function Number (RHDF)** Device and function number of the remapping host that this Remapped Device is remapped to. Bit 7:3 is the device number, bit 2:0 is the function number.

Cycle Router Global Control (CRGC) – Offset fc0

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1:0	00b	RW	**Cycle Router Accessibility Select (CRAS)** This field selects the Cycle Router instance that maps to (100h FBFh) of the integrated AHCI controller extended configuration space. BIOS writes to this field to select the Cycle Router instance for the accessibility to the corresponding registers. Bit Description 00 Cycle Router #1 01 Cycle Router #2 10 Cycle Router #3 11 Reserved

Fuse DW0 (FDW0) – Offset fc4

Bit Range	Default	Access	Field Name and Description
30:7	-	-	**Reserved**
6	0b	RO	**PCIe Cycle Router #3 Disable (PCR3D)** 0 PCIe Cycle Router #3 (Remapping Device #3) is enabled. 1 PCIe Cycle Router #3 (Remapping Device #3) is disabled.

Bit Range	Default	Access	Field Name and Description
5	0b	RO	**PCIe Cycle Router #2 Disable (PCR2D)** 0 PCIe Cycle Router #2 (Remapping Device #2) is enabled. 1 PCIe Cycle Router #2 (Remapping Device #2) is disabled
4	0b	RO	**PCIe Cycle Router #1 Disable (PCR1D) (PCR1D)** 0 PCIe Cycle Router #1 (Remapping Device #1) is enabled. 1 PCIe Cycle Router #1 (Remapping Device #1) is disabled.
3	-	-	**Reserved**
2	0b	RO	**AHCI Remapping Disable (ARD) (ARD)** 0 AHCI Remapping is enabled. 1 AHCI Remapping is disabled.
1:0	0b	RO	**SATA RAID Configuration (SRC)** 00 - No RAID 01 - RAID 1 Only 10 - RAID 0/1/5/10 11 Premium

Intel RST for PCIe Storage MMIO Registers

These registers are MMIO registers and can be accessed via the ABAR defined in the PCI configuration space.

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
800h	4	Remap Configuration Register (RCR_L)	0h
808h	4	AHCI MSI-X Configuration (AMXC)	0h
80ch	4	Scratch Pad Register (SPR)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
880h	4	Device Class Code (DCC_1)	0h
884h	4	Device Memory BAR Length (DMBL_1)	0h
888h	4	Device MSI-X Configuration (DMXC_L_1)	0h

Remap Configuration Register (RCR_L) – Offset 800

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**
2:0	000b	RW/O	**Number of Remapped Device Supported (NRS)** This field is bit significant. If a bit is set to 1, the corresponding remapping is enabled. If a bit is cleared to 0, the corresponding remapping is disabled and not used.

AHCI MSI-X Configuration (AMXC) – Offset 808

Bit Range	Default	Access	Field Name and Description
30:11	-	-	**Reserved**
10:0	0b	RW/O	**AHCI MSI-X Starting Vector (AMXV)** This field indicates the single MSI-X vector allocated for the integrated AHCI controller.

Scratch Pad Register (SPR) – Offset 80c

Scratch Pad Register

Device Class Code (DCC_1) – Offset 880

Bit Range	Default	Access	Field Name and Description
31	0b	RW/O	**Device Type (DT)** A 0 indicates the PCIe SSD is a NVM Express (NVMe) device, whereas a 1 indicates it is an AHCI device.
30:24	-	-	**Reserved**
23:16	0b	RW/O	**Base Class Code (BCC)** Base Class COde
15:8	0b	RW/O	**Sub Class Code (SCC)** Sub Class Code
7:0	0b	RW/O	**Programming Interface (PI)** Programming Interface

Device Memory BAR Length (DMBL_1) – Offset 884

Bit Range	Default	Access	Field Name and Description
31:0	0b	RW/O	**Memory BAR Length (MBL)** This register indicates the size of the Host Controller interface memory BAR of the remapping device. A 1 in the bit location indicates the corresponding lower memory BAR bit for the PCIe SSD device is a Read/Write (RW) bit.

Device MSI-X Configuration (DMXC_L_1) – Offset 888

Bit Range	Default	Access	Field Name and Description
30:27	-	-	**Reserved**
26:16	0b	RW/O	**MSI-X Ending Vector (MXEV)** This is the ending MSI-X vector used by the PCIe SSD device. It is a 0-based field. This field is only valid when DMXC.ID indicates interrupt delivery using MSI-X.

Bit Range	Default	Access	Field Name and Description
15:11	-	-	**Reserved**
10:0	0b	RW/O	**MSI-X Starting Vector (MXSV)** This is the starting MSI-X vector used by the PCIe SSD device. It is a 0-based field. This field is only valid when DMXC.ID indicates interrupt delivery using MSI-X.

Intel® Management Engine Interface PCI Configuration Registers

The registers in this section apply to the following Intel(R) Management Engine Interfaces (MEI):

MEI 1 at Device 22:Function 0

MEI 2 at Device 22:Function 1

MEI 3 at Device22:Function 4

MEI 4 at Device22:Function 5

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Identifiers (HECI1_ID)	608086h
4h	2	Command (HECI1_CMD)	0h
6h	2	Status (HECI1_STS)	10h
8h	4	Revision ID And Class Code (HECI1_RID_CC)	78000XXh
ch	1	Cache Line Size (HECI1_CLS)	0h
dh	1	Master Latency Timer (HECI1_MLT)	0h
eh	1	Header Type (HECI1_HTYPE)	80h
fh	1	Built In Self-Test (HECI1_BIST)	0h
10h	4	MMIO Base Address Low (HECI1_MMIO_MBAR_LO)	4h
14h	4	MMIO Base Address High (HECI1_MMIO_MBAR_HI)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2ch	4	Sub System Identifiers (HECI1_SS)	0h
34h	4	Capabilities Pointer (HECI1_CAP)	50h
3ch	2	Interrupt Information (HECI1_INTR)	100h
3eh	1	Minimum Grant (HECI1_MGNT)	0h
3fh	1	Maximum Latency (HECI1_MLAT)	0h
40h	4	Host Firmware Status Register 1 (HFSTS1)	0h
48h	4	Host Firmware Status Register 2 (HFSTS2)	0h
4ch	4	Host General Status (HECI1_H_GS1)	0h
50h	2	PCI Power Management Capability ID (HECI1_PID)	8C01h
52h	2	PCI Power Management Capabilities (HECI1_PC)	4003h
54h	2	PCI Power Management Control And Status (HECI1_PMCS)	8h
60h	4	Host Firmware Status Register 3 (HFSTS3)	0h
64h	4	Host Firmware Status Register 4 (HFSTS4)	0h
68h	4	Host Firmware Status Register 5 (HFSTS5)	0h
6ch	4	Host Firmware Status Register 6 (HFSTS6)	0h
70h	4	Host General Status 2 (HECI1_H_GS2)	0h
74h	4	Host General Status 3 (HECI1_H_GS3)	0h
8ch	2	Message Signaled Interrupt Identifiers (HECI1_MID)	A405h
8eh	2	Message Signaled Interrupt Message Control (HECI1_MC)	80h
90h	4	Message Signaled Interrupt Message Address (HECI1_MA)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
94h	4	Message Signaled Interrupt Upper Address (HECI1_MUA)	0h
98h	2	Message Signaled Interrupt Message Data (HECI1_MD)	0h
a0h	1	Interrupt Delivery Mode (HECI1_HIDM)	0h

Identifiers (HECI1_ID) – Offset 0

Identification

Bit Range	Default	Access	Field Name and Description
31:16	60h	RO/V	**Device ID (DID)** Indicates what device number assigned by Intel. Refer to the Device and Revision ID Table in Volume 1 for default value.
15:0	8086h	RO	**Vendor ID (VID)** 16-bit field which indicates Intel is the vendor.

Command (HECI1_CMD) – Offset 4

Command

Bit Range	Default	Access	Field Name and Description
14:11	-	-	**Reserved**
10	0b	RW	**Interrupt Disable (ID)** Disables this device from generating PCI line based interrupts. This bit does not have any effect on MSI operation.

Bit Range	Default	Access	Field Name and Description
9	0b	RO	**Fast Back-to-Back Enable (FBE)** Not implemented, hardwired to 0.
8	0b	RO	**SERR# Enable (SEE)** Not implemented, hardwired to 0.
7	0b	RO	**Wait Cycle Enable (WCC)** Not implemented, hardwired to 0.
6	0b	RO	**Parity Error Response Enable (PEE)** Not implemented, hardwired to 0.
5	0b	RO	**VGA Palette Snooping Enable (VAG)** Not implemented, hardwired to 0.
4	0b	RO	**Memory Write And Invalidate Enable (MWIE)** Not implemented, hardwired to 0.
3	0b	RO	**Special Cycle Enable (SCE)** Not implemented, hardwired to 0.
2	0b	RW	**Bus Master Enable (BME)** Controls the HECI host controller's ability to act as a system memory master for data transfers. When this bit is cleared, HECI bus master activity stops and any active DMA engines return to an idle condition.
1	0b	RW	**Memory Space Enable (MSE)** Controls access to the HECI host controllers memory mapped register space.
0	0b	RO	**I/O Space Enable (IOSE)** Not implemented, hardwired to 0.

Status (HECI1_STS) – Offset 6

Status

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
15	0b	RO	**Detected Parity Error (DPE)** Not implemented, hardwired to 0.
14	0b	RO	**Signaled System Error (SSE)** Not implemented, hardwired to 0.
13	0b	RO	**Received Master-Abort (RMA)** Not implemented, hardwired to 0.
12	0b	RO	**Received Target Abort (RTA)** Not implemented, hardwired to 0.
11	0b	RO	**Signaled Target-Abort (STA)** Not implemented, hardwired to 0.
10:9	00b	RO	**DEVSEL# Timing (DEVT)** Not implemented, hardwired to 0.
8	0b	RO	**Master Data Pariy Error Detected (DPD)** Not implemented, hardwired to 0.
7	0b	RO	**Fast Back-to-Back Capable (FBC)** Not implemented, hardwired to 0.
6	-	-	**Reserved**
5	0b	RO	**66 MHz Capable (C66)** Not implemented, hardwired to 0.
4	1b	RO	**Capabilities List (CL)** Indicates the presence of a capabilities list, hardwired to 1.
3	0b	RO/V	**Interrupt Status (IS)** Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted.This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register). Note that this bit is not set by an MSI.
2:0	-	-	**Reserved**

Revision ID And Class Code (HECI1_RID_CC) – Offset 8

Revision ID And Class Code

Bit Range	Default	Access	Field Name and Description
31:24	07h	RO	**Base Class Code (BCC)** Indicates the base class code of the host controller device.
23:16	80h	RO	**Sub Class Code (SCC)** Indicates the sub class code of the host controller device.
15:8	00h	RO	**Programming Interface (PI)** Indicates the programming interface of the host controller device.
7:0	See Description	RO/V	**Revision ID (RID)** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

Cache Line Size (HECI1_CLS) – Offset c

Cache Line Size

Bit Range	Default	Access	Field Name and Description
7:0	00h	RO	**Cache Line Size (CLS)** Not implemented, hardwired to 0.

Master Latency Timer (HECI1_MLT) – Offset d

Master Latency Timer

Bit Range	Default	Access	Field Name and Description
7:0	00h	RO	**Master Latency Timer (MLT)** Not implemented, hardwired to 0.

Header Type (HECI1_HTYPE) – Offset e

Header Type

Bit Range	Default	Access	Field Name and Description
7	1b	RO	**Multi-Function Device (MFD)** Indicates the host controller is part of a multi- function device.
6:0	0h	RO	**Header Layout (HL)** Indicates that the host controller uses a target device layout.

Built In Self-Test (HECI1_BIST) – Offset f

Built In Self-Test

Bit Range	Default	Access	Field Name and Description
7	0b	RO	**BIST Capable (BC)** Not implemented, hardwired to 0.
6:0	-	-	**Reserved**

MMIO Base Address Low (HECI1_MMIO_MBAR_LO) – Offset 10

HECI MMIO Base Address Low

Bit Range	Default	Access	Field Name and Description
31:12	0h	RW	**Base Address Low (BA_LO)** Lower 32 bits of base address of register memory space.
11:4	0h	RO	**Memory Size (MS)** This field is hardwired to 0 to indicate that HECI device requests 4KB of memory space.
3	0b	RO	**Prefetchable (PF)** Indicates that this range is not pre-fetchable

Bit Range	Default	Access	Field Name and Description
2:1	10b	RO	**Type (TP)** Indicates that this range can be mapped anywhere in 64-bitaddress space.
0	0b	RO	**Resource Type Indicator (RTE)** Indicates a request for register memory space.

MMIO Base Address High (HECI1_MMIO_MBAR_HI) – Offset 14

HECI MMIO Base Address High

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Base Address High (BA_HI)** Upper 32 bits of base address of register memory space.

Sub System Identifiers (HECI1_SS) – Offset 2c

Sub System Identifiers

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/O	**Subsystem ID (SSID)** Indicates the sub- system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only.
15:0	0000h	RW/O	**Subsystem Vendor ID (SSVID)** Indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot- up. Once written, this register becomes Read Only.

Capabilities Pointer (HECI1_CAP) – Offset 34

Capabilities Pointer

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	50h	RO	**Capability Pointer (CP)** Indicates the first capability pointer offset. It points to the PCI power management capability offset.

Interrupt Information (HECI1_INTR) – Offset 3c

Interrupt Information

Bit Range	Default	Access	Field Name and Description
15:8	01h	RO/V	**Interrupt Pin (IPIN)** This field indicates the virtual interrupt pin the host controller uses. A value of 0x1/0x2/0x3/0x4 indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively. When legacy interrupt is not used this register should be set to 0x0.
7:0	0h	RW	**Interrupt Line (ILINE)** Software written value to indicate which interrupt line (vector) theinterrupt is connected to. No hardware action is taken on this field.

Minimum Grant (HECI1_MGNT) – Offset 3e

Minimum Grant

Bit Range	Default	Access	Field Name and Description
7:0	0h	RO	**Grant (GNT)** Not implemented, hardwired to 0.

Maximum Latency (HECI1_MLAT) – Offset 3f

Maximum Latency

Bit Range	Default	Access	Field Name and Description
7:0	0h	RO	**Latency (LAT)** Not implemented, hardwired to 0.

Host Firmware Status Register 1 (HFSTS1) – Offset 40

Host Firmware Status

Bit Range	Default	Access	Field Name and Description
31:0	0000000h	RO/V	**Host Firmware Status (FS_HA)** Indicates current status of the firmware for the controller. This field is the host's read only access to the FS field in the ME Firmware Status register. This field is reset during CSE partition reset flow.

Host Firmware Status Register 2 (HFSTS2) – Offset 48

General Status Shadow 1

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO/V	**Host Firmware Status (GSS1)** This field is host side shadow of General Status 1 (CSE_GS1) register. This field is reset during ME partition reset flow.

Host General Status (HECI1_H_GS1) – Offset 4c

Host General Status

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Host General Status (H_GS1)** General status of Host. This field is not used by hardware.

PCI Power Management Capability ID (HECI1_PID) – Offset 50

PCI Power Management Capability ID

Bit Range	Default	Access	Field Name and Description
15:8	8Ch	RO	**Next Capability (NEXT)** Indicates the location of the next capability item in the list. This is the Message Signaled Interrupts capability.
7:0	01h	RO	**Cap ID (CID)** Indicates that this pointer is a PCI power management.

PCI Power Management Capabilities (HECI1_PC) – Offset 52

PCI Power Management Capabilities

Bit Range	Default	Access	Field Name and Description
15:11	01000b	RO	**PME Support (PSUP)** Indicates the states that can generate PME#. The controller can assert PME# from D3hot only.
10	0b	RO	**D2 Support (D2S)** The D2 state is not supported for the host controller.
9	0b	RO	**D1_Support (D1S)** The D1 state is not supported for the host controller.
8:6	000b	RO	**Aux Current (AUXC)** Reports the maximum Suspend well current required when in the D3COLD state. Value of 0 is reported.
5	0b	RO	**Device Specific Initialization (DSI)** Indicates whether device-specific initialization is required.
4	-	-	**Reserved**
3	0b	RO	**PME Clock (PMEC)** Indicates that PCI clock is not required to generate PME#.

Bit Range	Default	Access	Field Name and Description
2:0	011b	RO	**Version (VS)** Indicates support for Revision 1.2 of the PCI Power Management Specification.

PCI Power Management Control And Status (HECI1_PMCS) – Offset 54

PCI Power Management Control And Status

Bit Range	Default	Access	Field Name and Description
15	0b	RW/1C/V	**PME Status (PMES)** The PME Status bit can be set to '1' by the FW. This bit is cleared by host CPU writing a '1' to it. FW cannot clear this bit. Host CPU writes with value '0' have no effect on this bit.
14:9	-	-	**Reserved**
8	0b	RW	**PME Enable (PMEE)** When set, PME_assert and PME_deassert messages are sent over Sideband to PMC based on the PMES bit. When reset these messages may not be sent.
7:4	-	-	**Reserved**
3	1b	RO	**No Soft Reset (NSR)** This bit indicates that when the controller is transitioning from D3hot to D0 due to power state command, it does not perform and internal reset.
2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1:0	00b	RW	**Power State (PS)** This field is used both to determine the current power state of the controller and to set a new power state. The values are: 00 - D0 state 11 - D3HOT state. The D1 and D2 states are not supported for this controller. If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs. When in the D3HOT state, the HBA's configuration space is available, but the registers memory space is not. Additionally, interrupts are blocked.

Host Firmware Status Register 3 (HFSTS3) – Offset 60

General Status Shadow 2

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO/V	**Host Firmware Status (GSS2)** This field is host side shadow of ME General Status 2 (CSE_GS2). This field is reset during ME partition reset flow.

Host Firmware Status Register 4 (HFSTS4) – Offset 64

General Status Shadow 3

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RO/V	**Host Firmware Status (GSS3)** This field is host side shadow of CSE General Status 3 (CSE_GS3). This field is reset during ME partition reset flow.

Host Firmware Status Register 5 (HFSTS5) – Offset 68

General Status Shadow 4

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RO/V	**Host Firmware Status (GSS4)** This field is host side shadow of ME General Status 4 (CSE_GS4). This field is reset during ME partition reset flow.

Host Firmware Status Register 6 (HFSTS6) – Offset 6c

General Status Shadow 5

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RO/V	**Host Firmware Status (GSS5)** This field is host side shadow of ME General Status 5 (CSE_GS5). This field is reset during ME partition reset flow.

Host General Status 2 (HECI1_H_GS2) – Offset 70

Host General Status 2

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**Host General Status 2 (H_GS2)** General status of Host. This field is not used by hardware.

Host General Status 3 (HECI1_H_GS3) – Offset 74

Host General Status 3

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Host General Status 3 (H_GS3)** General status of Host. This field is not used by hardware.

Message Signaled Interrupt Identifiers (HECI1_MID) – Offset 8c

Message Signaled Interrupt Identifiers

Bit Range	Default	Access	Field Name and Description
15:8	A4h	RO	**Next Pointer (NEXT)** Indicates the next item in the list. This can be other capability pointers (such as PCI-X or PCI- Express) or it can be the last item in the list.
7:0	05h	RO	**Capability ID (CID)** Indicates MSI.

Message Signaled Interrupt Message Control (HECI1_MC) – Offset 8e

Message Signaled Interrupt Message Control

Bit Range	Default	Access	Field Name and Description
14:8	-	-	**Reserved**
7	1b	RO	**64 Bit Address Capable (C64)** Specifies whether capable of generating 64-bit messages.
6:4	000b	RO	**Multiple Message Enable (MME)** Not implemented, hardwired to 0.

Bit Range	Default	Access	Field Name and Description
3:1	000b	RO	**Multiple Message Capable (MMC)** Not implemented, hardwired to 0.
0	0b	RW	**MSI Enable (MSIE)** If set, MSI is enabled and INTx virtual wires are not used to generate interrupts.

Message Signaled Interrupt Message Address (HECI1_MA) – Offset 90

Message Signaled Interrupt Message Address

Bit Range	Default	Access	Field Name and Description
31:2	0000000 0h	RW	**Address (ADDR)** Lower 32 bits of the system specified message address, always DW aligned.
1:0	-	-	**Reserved**

Message Signaled Interrupt Upper Address (HECI1_MUA) – Offset 94

Message Signaled Interrupt Upper Address

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**Upper Address (UADDR)** Upper 32 bits of the system specified message address. This register is optional and only implemented if MC.C64=1.

Message Signaled Interrupt Message Data (HECI1_MD) – Offset 98

Message Signaled Interrupt Message Data

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW	**Data (DATA)** This 16-bit field is programmed by system software if MSI is enabled.

Interrupt Delivery Mode (HECI1_HIDM) – Offset a0

HECI Interrupt Delivery Mode

Bit Range	Default	Access	Field Name and Description
6:3	-	-	**Reserved**
2	0b	RW/1S/V	**HIDM Lock (HIDM_L)** Writing 1 to this bit locks the HIDM field.
1:0	00b	RW/L	**HECI Interrupt Delivery Mode (HIDM)** These bits control what type of interrupt the controller will send when ME FW writes to set the CSE_IG bit. They are interpreted as follows: 00 - Generate Legacy or MSI interrupt; 01 - Generate SCI; 10 - Generate SMI; This field may be locked by writing 1 to HIDM_L bit.

Intel® MEI MMIO Registers

The registers in this section apply to the following Intel(R) Management Engine Interfaces (MEI):

MEI 1 at Device 22:Function 0

MEI 2 at Device 22:Function 1

MEI 3 at Device22:Function 4

MEI 4 at Device22:Function 5

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
800h	4	DEVIDLE Control (HECI1_DEVIDLEC)	0h

DEVIDLE Control (HECI1_DEVIDLEC) – Offset 800

This register allows host to configure the power mode using D0i0/D0i3 support.

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**
2	0b	RW	**DevIdle (DEVIDLE)** SW sets this bit to 1'b1 to move the function into the DevIdle state. Writing this bit to 1'b0 will return the function to the fully active D0 state (D0i0).
1	0b	RW	**Interrupt Request (IR)** SW sets this bit to 1'b1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register. When this bit is set to 1'b1, Command-in-Progress deassertion is captured in H_CSR.H_DEVIDLEC_IS. If H_CSR.H_DEVIDLEC_IE is 1b1 as well, host interrupt will be initiated.
0	0b	RO/V	**Command-in-Progress (CIP)** HW sets this bit on a 1'b1->1'b0 or 1'b0->1'b1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. HW clears this bit when CSE FW clears its own DevIdle interrupt status bit indicating completion of the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

Intel® Trace Hub Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Vendor ID (VID)	9638086h
4h	4	Command (CMD)	100000h
8h	4	Revision ID (RID)	13000001h
ch	4	Header Type (HT)	0h
10h	4	Trace Buffer Lower BAR (MTB_LBAR)	4h
14h	4	Trace Buffer Upper BAR (MTB_UBAR)	0h
18h	4	Software Lower BAR (SW_LBAR)	4h
1ch	4	Software Upper BAR (SW_UBAR)	0h
20h	4	RTIT Lower BAR (RTIT_LBAR)	0h
24h	4	RTIT Upper BAR (RTIT_UBAR)	0h
2ch	4	Subsystem Vendor ID (SVID)	0h
34h	4	Capabilities Pointer (CAP)	40h
3ch	4	Interrupt Line (INTL)	1FFh
40h	4	MSI Capability ID (MSICID)	860000h
44h	4	MSI Lower Message Address (MSILMA)	0h
48h	4	MSI Upper Message Address (MSIUMA)	0h
4ch	4	MSI Message Data (MSIMD)	0h
70h	4	(FW_LBAR)	4h
74h	4	(FW_UBAR)	0h
80h	4	Device Specific Control (NPKDSC)	0h
b4h	4	Power Control Enable Register (DEVIDLEPCE)	8h

Vendor ID (VID) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:16	0963h	RO	**(DID)** The value that uniquely identifies the Intel Trace Hub.
15:0	8086h	RO	**Vendor ID (VID)** 8086 is Intel Vendor Identification code.

Command (CMD) – Offset 4

Bit Range	Default	Access	Field Name and Description
30	0h	RW/1C	**Signaled System Error (SSE)** This bit is set when the device has detected an un-correctable error and reported it via SERR message over sideband. This requires SERR Enable bit to be set in Command register.
29	0h	RW/1C	**Received Master Abort Status (RMA)** This bit is set when device receives a Completion transaction with Unsupported Request completion status. No error will be reported.
28	0h	RW/1C	**Received Target Abort Status (RTA)** This bit is set when device receives a Completion transaction with Completer Abort completion status. No error will be reported
27	0h	RW/1C	**Signaled Target Abort Status (STA)** Set by the device when aborting a request that violates the device programming model. When SERR Enable is set SERR message will be send over sideband.
26:21	-	-	**Reserved**
20	1h	RO	**Capabilities List (CLIST)** Indicates the controller contains a capabilities pointer list and the capability pointer register is implemented at offset 0x40 in the configuration space

Bit Range	Default	Access	Field Name and Description
19	0h	RO	**Interrupt Status (INSTAT)** Reflects the state of the interrupt pin at the input of the enable/disable circuit. When the interrupt is asserted, and cleared when the interrupt is cleared (independent of the state of Interrupt Disable bit in command register. This bit is only associated with the INTx messages and has no meaning if the device is using MSI.
18:11	-	-	**Reserved**
10	0h	RW	**Interrupt Disable (IntDis)** Disables the function to generate INTx interrupt. A value of 0 enables the function to generate INTA messages on IOSF sideband. Note: this bit has no effect on MSI generation.
9	-	-	**Reserved**
8	0h	RW	**System Error Enable (SERREn)** Setting this bit enables the generation of System Error message, when required through sideband interface.
7:3	-	-	**Reserved**
2	0h	RW	**Bus Master Enable (BME)** When set enables the ability to issue Memory or IO requests, including MSI.
1	0h	RW	**Memory Space Enable (MEM)** When set, Memory Space Decoding is enabled and memory transactions targeting the device are accepted. Note: The MSE has to be set to accept any memory transaction on the primary interface targeting any of Trace Hub's BARs.
0	-	-	**Reserved**

Revision ID (RID) – Offset 8

Bit Range	Default	Access	Field Name and Description
31:8	130000h	RO	**Class Code (Class)** Class Code
7:0	See Description	RO	**Revision ID (RID)** Indicates the device specific revision identifier.

Header Type (HT) – Offset c

Bit Range	Default	Access	Field Name and Description
30:23	-	-	**Reserved**
22:16	00h	RO	**Header Type (HT)** Implements a Type 0 configuration header
15:0	-	-	**Reserved**

Trace Buffer Lower BAR (MTB_LBAR) – Offset 10

Bit Range	Default	Access	Field Name and Description
31:20	000h	RW	**Lower Base Address (ADDR)** Lower programmable Base Address.
19:4	-	-	**Reserved**
3	0h	RO	**Prefetchable (PF)** Value of 0 indicates the BAR cannot be prefetched.
2:1	2h	RO	**Address Range (ADRNG)** Value of 0x2 indicates that the BAR is located anywhere system memory space (i.e. 64-bit addressing)

Bit Range	Default	Access	Field Name and Description
0	0h	RO	**Space Type (SPTY)** Value of 0 indicates the BAR is located in memory space.

Trace Buffer Upper BAR (MTB_UBAR) – Offset 14

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Upper Base Address (ADDR)** Upper programmable Base Address.

Software Lower BAR (SW_LBAR) – Offset 18

Bit Range	Default	Access	Field Name and Description
31:23	000h	RW	**Lower Base Address (ADDR)** Lower programmable Base Address.
22:4	-	-	**Reserved**
3	0h	RO	**Prefetchable (PF)** Value of 0 indicates the BAR cannot be prefetched.
2:1	2h	RO	**Address Range (ADRNG)** Value of 0x2 indicates that the BAR is located anywhere system memory space (i.e. 64-bit addressing)
0	0h	RO	**Space Type (SPTY)** Value of 0 indicates the BAR is located in memory space

Software Upper BAR (SW_UBAR) – Offset 1c

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**Upper Base Address (ADDR)** Upper programmable Base Address.

RTIT Lower BAR (RTIT_LBAR) – Offset 20

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RO	**Lower Base Address (ADDR)** Lower Base Address: Lower programmable Base Address

RTIT Upper BAR (RTIT_UBAR) – Offset 24

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**Upper Base Address (ADDR)** Upper Base Address: Upper programmable Base Address

Subsystem Vendor ID (SVID) – Offset 2c

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW	**Subsystem ID (SID)** Writable only once
15:0	0000h	RW	**Subsystem Vendor ID (SVID)** Be set once by BIOS then becomes RO.

Capabilities Pointer (CAP) – Offset 34

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	40h	RO	**Capability Pointer: (CAPPTR)** Pointer to first capability structure at 40h.

Interrupt Line (INTL) – Offset 3c

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:8	01h	RW/O	**Interrupt Pin (INTPIN)** Trace Hub uses a single INTx interrupt bonded to INTA.
7:0	FFh	RW	**Interrupt Line (INTL)** Hardware does not use this field. Rather it is programmed by system software and device drivers to communicate interrupt line routing information.

MSI Capability ID (MSICID) – Offset 40

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	1h	RO	**Multiple Message Capable (AC64b)** Value of 0 indicates the device only support single interrupt message.
22:20	0h	RW	**MSI Enable (MME)** If set, MSI is enabled and the legacy interrupts messages (over IOSF sideband) will not be generated

Bit Range	Default	Access	Field Name and Description
19:17	3h	RO	**MSI Next Capability Pointer (MMC)** Value of 0 indicates there are no further capabilities (i.e. the capability linked list is ended)
16	0h	RW	**MSI Capability ID (MSIE)** MSI Capability ID with a value of 05h indicating the presence of the MSI capability register set
15:8	00h	RO	**64-bit Address Capable (MSINCP)** Trace Hub is capable of generating 64-bit memory addresses
7:0	-	-	**Reserved**

MSI Lower Message Address (MSILMA) – Offset 44

Bit Range	Default	Access	Field Name and Description
31:2	0000000 0h	RW	**MSI Message Lower Address (MSILMA)** Lower 32-bits of system software assigned message address to the device with bits[1:0] always cleared indicating message address has to always be DW aligned.
1:0	-	-	**Reserved**

MSI Upper Message Address (MSIUMA) – Offset 48

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**MSI Message Upper Address (MSIUMA)** Upper 32 bits of system software assigned message address to the device.

MSI Message Data (MSIMD) – Offset 4c

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0000h	RW	**MSI Message Data (MSIMD)** 16 bit message data pattern assigned by the system software to the device. When MSI is generated the actual data is 32 bit and the upper 16 bits are always 0.

(FW_LBAR) – Offset 70

Firmware Lower Bar

Bit Range	Default	Access	Field Name and Description
31:21	000h	RW	**(ADDR)** Lower Base Address: Lower programmable Base Address
20:4	-	-	**Reserved**
3	0h	RO	**(PF)** Prefetchable: Value of 0 indicates the BAR cannot be prefetched
2:1	2h	RO	**Address Range (TYPE)** Address Range: Value of 0x2 indicates that the BAR is located anywhere system memory space (i.e. 64-bit addressing)
0	0h	RO	**Space Type (MEM)** Space Type: Value of 0 indicates the BAR is located in memory space

(FW_UBAR) – Offset 74

Firmware Upper Bar

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**(UADDR)** Upper Base Address: Upper programmable Base Address

Device Specific Control (NPKDSC) – Offset 80

Bit Range	Default	Access	Field Name and Description
30:11	-	-	**Reserved**
10	0h	RW/1C	**Unsupported Request Detect (URD)** This bit is set when an unsupported request is detected.
9:4	-	-	**Reserved**
3	0h	RW	**Unsupported Request Reporting Enable (URRE)** When set, this bit enables the reporting unsupported requests as system errors
2	0h	RW/1C	**Capture Done Interrupt Status (CDINTS)** Formerly Legacy Interrupt Asserted. Equivalent to MSUSTS.MSU_INT, for software compatibility. This this bit indicates when the capture done event has occurred. Software can clear the capture done interrupt event by writing a 1 to this bit, or writing a 1 to the MSUSTS.MSU_INT bit
1	0h	RW	**Software Reset: (FLR)** Writing a 1 to this bit will assert the reset signals. Reading this bit will always return a zero.
0	-	-	**Reserved**

Power Control Enable Register (DEVIDLEPCE) – Offset b4

Bit Range	Default	Access	Field Name and Description
30:4	-	-	**Reserved**
3	1h	RW	**Sleep Enable (SE)** If clear, Trace Hub will never assert sleep. If set, it will assert sleep during power gating

Bit Range	Default	Access	Field Name and Description
2	-	-	**Reserved**
1	0h	RO	**Device Idle Enable (DEVIDLEN)** It set, Trace Hub will power gate when idle and D0I3C[2] is programmed to 1h (D0I3C[2] = 0x1)
0	-	-	**Reserved**

Intel® HD Audio PCR Registers

These registers are within the PCH Private Configuration Space which is accessiblethrough the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID+ Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
530h	4	Function Configuration (FNCFG)	28h

Function Configuration (FNCFG) – Offset 530

Bit Range	Default	Access	Field Name and Description
30:6	-	-	**Reserved**
5	1b	RW	**Power Gating Disable (PGDIS)** When cleared, it allows power gating to take place per their associated enable and idle conditions. When set, it globally disables all power gating.
4	0b	RW/O/L	**BIOS Configuration Lock Down (BCLD)** When cleared, it allows power gating to take place per their associated enable and idle conditions. When set, it globally disables all power gating.

Bit Range	Default	Access	Field Name and Description
3	1b	RW	**Clock Gating Disable (CGD)** Clock Gating Disabled (CGD): When cleared, it allows local / dynamic clock gating and trunk clock gating to take place per their associated enable and idle conditions. When set, it globally disables all clock gating.
2	0b	RW/L	**Audio DSP Disable (ADSPD)** Audio DSP Disable (ADSPD): When set, the Audio DSP is disabled and all register access associated with Audio DSP are treated as unsupported request, and return UR response if it is non-posted cycle. This bit does not affect cycles from IOSF Sideband Interface. Locked when FNCFG.BCLD = 1.
1	-	-	**Reserved**
0	0b	RW/L	**HD Audio Subsystem Disable (HDASD)** HD Audio Subsystem Disable (HDASD): When set, the Intel HD Audio subsystem (including Audio DSP) is disabled and all register access are treated as an unsupported request and a return UR response if it is non-posted cycle. This bit does not affect cycles from IOSF Sideband Interface. Locked when FNCFG.BCLD = 1.

Interrupt Registers

Summary of Bus:, Device:, Function: (IO)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
20h	1	Master Initialization Command Word 1 (MICW1)	11h
21h	1	Master Initialization Command Word 2 (MICW2)	0h
21h	1	Master Initialization Command Word 3 (MICW3)	7h
21h	1	Master Initialization Command Word 4 (MICW4)	0h
21h	1	Master Operational Control Word 1 (MOCW1)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
20h	1	Master Operational Control Word 2 (MOCW2)	0h
20h	1	Master Operational Control Word 3 (MOCW3)	8h
a0h	1	Slave Initialization Command Word 1 (SICW1)	11h
a1h	1	Slave Initialization Command Word 2 (SICW2)	0h
a1h	1	Slave Initialization Command Word 3 (SICW3)	7h
a1h	1	Slave Initialization Command Word 4 (SICW4)	0h
a1h	1	Slave Operational Control Word 1 (SOCW1)	0h
a0h	1	Slave Operational Control Word 2 (SOCW2)	0h
a0h	1	Slave Operational Control Word 3 (SOCW3)	8h
4d0h	1	Master Edge/Level Control (ELCR1)	0h
4d1h	1	Slave Edge/Level Control (ELCR2)	0h

Master Initialization Command Word 1 (MICW1) – Offset 20

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:

1. The Interrupt Mask register is cleared.

2. IRQ7 input is assigned priority 7.

3. The slave mode address is set to 7.

4. Special Mask Mode is cleared and Status Read is set to IRR.

Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Bit Range	Default	Access	Field Name and Description
7:5	000b	WO	**ICW/OCW select (ICW_OCW_SLT1)** These bits are MCS-85 specific, and not needed. Should be programmed to 000
4	1b	WO	**ICW/OCW select (ICW_OCW_SLT2)** This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	0b	WO	**Edge/Level Bank Select (LTIM)** Disabled. Replaced by the edge/level triggered control registers (ELCR).
2	0b	WO	**ADI-IGNORED (ADI)** Ignored for PCH. Should be programmed to 0.
1	0b	WO	**Single or Cascade (SNGL)** Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	1b	WO	**ICW4 Write Required (IC4)** This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

Master Initialization Command Word 2 (MICW2) – Offset 21

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Bit Range	Default	Access	Field Name and Description
7:3	00000b	WO	**Interrupt Vector Base Address (IVBA)** Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.

Bit Range	Default	Access	Field Name and Description
2:0	000b	WO	**Interrupt Request Level (IRL)** When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

Master Initialization Command Word 3 (MICW3) – Offset 21

Bit Range	Default	Access	Field Name and Description
7:3	00000b	WO	**MICW3 [7:3] (MICW3_7_3)** These bits must be programmed to zero.
2	1b	WO	**Cascaded Controller Connection (CCC)** This bit must always be programmed to a 1 to indicate the slave controller for interrupts 8 - 15 is cascaded on IRQ2.
1:0	11b	WO	**MICW [1:0] (MICW3_1_0)** These bits must be programmed to zero.

Master Initialization Command Word 4 (MICW4) – Offset 21

Bit Range	Default	Access	Field Name and Description
6:5	-	-	**Reserved**
4	0b	WO	**Special Fully Nested Mode (SFNM)** Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0b	WO	**Buffered Mode (BUF)** Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0b	WO	**Master/Slave in Buffered Mode (MSBM)** Not used. Should always be programmed to 0.
1	0b	WO	**Automatic End of Interrupt (AEOI)** This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.
0	0b	WO	**Microprocessor Mode (MM)** This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.1

Master Operational Control Word 1 (MOCW1) – Offset 21

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**Interrupt Request Mask (IRM)** When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

Master Operational Control Word 2 (MOCW2) – Offset 20

]Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Bit Range	Default	Access	Field Name and Description
7:5	000b	WO	

Bit Range	Default	Access	Field Name and Description
			R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 Rotate in Auto EOI Mode (Clear) 001 Non-specific EOI command 010 No Operation 011 *Specific EOI Command 100 Rotate in Auto EOI Mode (Set) 101 Rotate on Non-Specific EOI Command 110 *Set Priority Command 111 *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	00b	WO	**OCW2 Select (O2S)** When selecting OCW2, bits 4:3 = 00
2:0	000b	WO	**Interrupt Level Select (L2, L1, L0) (ILSLT)** L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function, programming L2, L1 and L0 to 0 is sufficient in this case.

Master Operational Control Word 3 (MOCW3) – Offset 20

Bit Range	Default	Access	Field Name and Description
6	0b	WO	**Enable Special Mask Mode (ESMM)** When set, the SMM bit is enabled to set or reset the Special Mask Mode. When cleared, the SMM bit becomes a 'don't care'.
5	0b	WO	**Special Mask Mode (SMM)** If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.
4:3	01b	WO	**OCW3 Select (O3S)** When selecting OCW3, bits 4:3 = 01
2	0b	WO	**Poll Mode Command (PMC)** When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.

Bit Range	Default	Access	Field Name and Description
1:0	00b	WO	**Register Read Command (RRC)** . To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. Value Command 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

Slave Initialization Command Word 1 (SICW1) – Offset a0

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:

1. The Interrupt Mask register is cleared.

2. IRQ7 input is assigned priority 7.

3. The slave mode address is set to 7.

4. Special Mask Mode is cleared and Status Read is set to IRR.

Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Bit Range	Default	Access	Field Name and Description
7:5	000b	WO	**ICW/OCW select (ICW_OCW_SLT1)** These bits are MCS-85 specific, and not needed. Should be programmed to 000
4	1b	WO	**ICW/OCW select (ICW_OCW_SLT2)** This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	0b	WO	**Edge/Level Bank Select (LTIM)** Disabled. Replaced by the edge/level triggered control registers (ELCR).
2	0b	WO	**ADI-IGNORED (ADI)** Ignored for PCH. Should be programmed to 0.
1	0b	WO	**Single or Cascade (SNGL)** Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	1b	WO	**ICW4 Write Required (IC4)** This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

Slave Initialization Command Word 2 (SICW2) – Offset a1

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Bit Range	Default	Access	Field Name and Description
7:3	00000b	WO	**Interrupt Vector Base Address (IVBA)** Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.

Bit Range	Default	Access	Field Name and Description
2:0	000b	WO	**Interrupt Request Level (IRL)** When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

Slave Initialization Command Word 3 (SICW3) – Offset a1

Bit Range	Default	Access	Field Name and Description
6:3	-	-	**Reserved**
2:0	111b	WO	**Slave Identification Code (SIC)** This field must be programmed to 02h to match the code broadcast by the master controller during the INTA# sequence.

Slave Initialization Command Word 4 (SICW4) – Offset a1

Bit Range	Default	Access	Field Name and Description
6:5	-	-	**Reserved**
4	0b	WO	**Special Fully Nested Mode (SFNM)** Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0b	WO	**Buffered Mode (BUF)** Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0b	WO	**Master/Slave in Buffered Mode (MSBM)** Not used. Should always be programmed to 0.
1	0b	WO	**Automatic End of Interrupt (AEOI)** This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.
0	0b	WO	**Microprocessor Mode (MM)** This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.1

Slave Operational Control Word 1 (SOCW1) – Offset a1

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**Interrupt Request Mask (IRM)** When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

Slave Operational Control Word 2 (SOCW2) – Offset a0

Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Bit Range	Default	Access	Field Name and Description
7:5	000b	WO	

Bit Range	Default	Access	Field Name and Description
			R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 Rotate in Auto EOI Mode (Clear) 001 Non-specific EOI command 010 No Operation 011 *Specific EOI Command 100 Rotate in Auto EOI Mode (Set) 101 Rotate on Non-Specific EOI Command 110 *Set Priority Command 111 *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	00b	WO	**OCW2 Select (O2S)** When selecting OCW2, bits 4:3 = 00
2:0	000b	WO	**Interrupt Level Select (L2, L1, L0) (ILSLT)** L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function, programming L2, L1 and L0 to 0 is sufficient in this case.

Slave Operational Control Word 3 (SOCW3) – Offset a0

Bit Range	Default	Access	Field Name and Description
6	0b	WO	**Enable Special Mask Mode (ESMM)** When set, the SMM bit is enabled to set or reset the Special Mask Mode. When cleared, the SMM bit becomes a 'don't care'.
5	0b	WO	**Special Mask Mode (SMM)** If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.
4:3	01b	WO	**OCW3 Select (O3S)** When selecting OCW3, bits 4:3 = 01
2	0b	WO	**Poll Mode Command (PMC)** When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.

Bit Range	Default	Access	Field Name and Description
1:0	00b	WO	**Register Read Command (RRC)** . To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. Value Command 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

Master Edge/Level Control (ELCR1) – Offset 4d0

Master Edge/Level Control Register

Bit Range	Default	Access	Field Name and Description
7:3	00000b	RW	**Edge Level Control (ELC_7_3)** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level.
2:0	-	-	**Reserved**

Slave Edge/Level Control (ELCR2) – Offset 4d1

Slave Edge/Level Control Register

Bit Range	Default	Access	Field Name and Description
7:6	00b	RW	**Edge Level Control (ELC_15_14)** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 7 applies to IRQ15, and bit 6 to IRQ14.
5	0b	RW	**Edge Level Control (ELC_13)** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. This bit applies to IRQ13.
4:1	0000b	RW	**Edge Level Control (ELC_12_9)** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 4 applies to IRQ12, bit 3 to IRQ11, bit 2 to IRQ10, and bit 1 to IRQ9.
0	-	-	**Reserved**

Interrupt PCR Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3100h	1	PIRQA Routing Control (PARC)	80h
3101h	1	PIRQB Routing Control (PBRC)	80h
3102h	1	PIRQC Routing Control (PCRC)	80h
3103h	1	PIRQD Routing Control (PDRC)	80h
3104h	1	PIRQE Routing Control (PERC)	80h
3105h	1	PIRQF Routing Control (PFRC)	80h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3106h	1	PIRQG Routing Control (PGRC)	80h
3107h	1	PIRQH Routing Control (PHRC)	80h
3140h	2	PCI Interrupt Route 0 (PIR0)	3210h
3142h	2	PCI Interrupt Route 1 (PIR1)	0h
3144h	2	PCI Interrupt Route 2 (PIR2)	0h
3146h	2	PCI Interrupt Route 3 (PIR3)	0h
3148h	2	PCI Interrupt Route 4 (PIR4)	0h
314ah	2	PCI Interrupt Route 5 (PIR5)	0h
31fch	4	General Interrupt Control (GIC)	0h
3200h	4	Interrupt Polarity Control 0 (IPC0)	FF0000h
3204h	4	Interrupt Polarity Control 1 (IPC1)	0h
3208h	4	Interrupt Polarity Control 2 (IPC2)	0h
320ch	4	Interrupt Polarity Control 3 (IPC3)	0h
3300h	4	ITSS Power Reduction Control (ITSSPRC)	0h
3330h	4	NMI Control (NMI)	0h
3334h	2	Master Message Control (MMC)	0h

PIRQA Routing Control (PARC) – Offset 3100

PIRQA Routing Control Register

Bit Range	Default	Access	Field Name and Description
7	1b	RW	**Interrupt Routing Enable (REN)** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.

Bit Range	Default	Access	Field Name and Description
6:4	-	-	**Reserved**
3:0	0h	RW	**IRQ Routing (IR)** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

PIRQB Routing Control (PBRC) – Offset 3101

Bit Range	Default	Access	Field Name and Description
7	1b	RW	**Interrupt Routing Enable (REN)** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3:0	0h	RW	**IRQ Routing (IR)** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

PIRQC Routing Control (PCRC) – Offset 3102

Bit Range	Default	Access	Field Name and Description
7	1b	RW	**Interrupt Routing Enable (REN)** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3:0	0h	RW	**IRQ Routing (IR)** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

PIRQD Routing Control (PDRC) – Offset 3103

Bit Range	Default	Access	Field Name and Description
7	1b	RW	**Interrupt Routing Enable (REN)** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3:0	0h	RW	**IRQ Routing (IR)** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

PIRQE Routing Control (PERC) – Offset 3104

Bit Range	Default	Access	Field Name and Description
7	1b	RW	**Interrupt Routing Enable (REN)** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3:0	0h	RW	**IRQ Routing (IR)** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

PIRQF Routing Control (PFRC) – Offset 3105

Bit Range	Default	Access	Field Name and Description
7	1b	RW	**Interrupt Routing Enable (REN)** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3:0	0h	RW	**IRQ Routing (IR)** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

PIRQG Routing Control (PGRC) – Offset 3106

Bit Range	Default	Access	Field Name and Description
7	1b	RW	**Interrupt Routing Enable (REN)** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3:0	0h	RW	**IRQ Routing (IR)** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

PIRQH Routing Control (PHRC) – Offset 3107

Bit Range	Default	Access	Field Name and Description
7	1b	RW	**Interrupt Routing Enable (REN)** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3:0	0h	RW	**IRQ Routing (IR)** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

PCI Interrupt Route 0 (PIR0) – Offset 3140

This register applies to Device 31 functions.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
14:12	011b	RW	**Interrupt D Pin Route (IDR)** Indicates which PIRQ in PCH is connected to the INTD# pin reported for device 31 functions: Bits Pin Bits Pin 0h PIRQA# 4h PIRQE# 1h PIRQB# 5h PIRQF# 2h PIRQC# 6h PIRQG# 3h PIRQD# 7h PIRQH#
11	-	-	**Reserved**
10:8	010b	RW	**Interrupt C Pin Route (ICR)** See the IDR description. This field applies to INTC#
7	-	-	**Reserved**
6:4	001b	RW	**Interrupt B Pin Route (IBR)** See the IDR description. This field applies to INTB#.
3	-	-	**Reserved**
2:0	000b	RW	**Interrupt A Pin Route (IAR)** See the IDR description. This field applies to INTA#.

PCI Interrupt Route 1 (PIR1) – Offset 3142

Same definition as PIR0, except this register applies to Device 29 functions.

PCI Interrupt Route 2 (PIR2) – Offset 3144

Same definition as PIR0, except this register applies to Device 28 functions.

PCI Interrupt Route 3 (PIR3) – Offset 3146

Same definition as PIR0, except this register applies to Device 23 functions.

PCI Interrupt Route 4 (PIR4) – Offset 3148

Same definition as PIR0, except this register applies to Device 22 functions.

PCI Interrupt Route 5 (PIR5) – Offset 314a

Same definition as PIR0, except this register applies to Device 20 and 18 functions.

General Interrupt Control (GIC) – Offset 31fc

Note: FEC10000h - FEC3FFFFh is allocated to PCIe when Port I/OxApic Enable (PAE) bit is set.

Bit Range	Default	Access	Field Name and Description
30:18	-	-	**Reserved**
17	0b	RW	**Alternate Access Mode Enable (AME)** When set, read only registers can be written, and write only registers can be read.
16	0b	RW	**Shutdown Policy Select (SDPS)** When cleared (default) the PCH will update INIT# in response to the shutdown Vendor Defined Message (VDM). When set to 1, PCH will treat the shutdown VDM similar to receiving a CF9h I/O write, and will drive PLTRST# active. This register is reset any time PLTRST# asserts.

Bit Range	Default	Access	Field Name and Description
15:9	0000000b	RW	**MAX_IRQ_ENTRY_SIZE (MAXIRQSIZE)** This field indicates the size of the IOAPIC entry. The default size is 120 entries. 0000000: 120 entry size 0000001: 24 entry size (Legacy mode) 0000010 - 1111111: Reserved
8:1	-	-	**Reserved**
0	0b	RO/P	**CPU Shutdown Status (CPUSDSTS)** This bit is set to 1 if the CPU sends the Shutdown Special cycle message. The Shutdown Message is recognized as an INIT# event if the Shutdown Policy Select = 0, else PCH shall treat the Shutodwn Special cycle as a request for CF9 Hard Reset. This is a sticky Read Only bit that is only reset by a loss of core power.

Interrupt Polarity Control 0 (IPC0) – Offset 3200

Interrupt Polarity Control 0 Register

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	00FF0000h	RW	**IRQ 31-0 Active High Polarity Disable (IPC0_IRQxAHPOLDIS)** When set to 1, the interrupt polarity associated with IRQ31 down to IRQ0 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

Interrupt Polarity Control 1 (IPC1) – Offset 3204

Interrupt Polarity Control 1 Register

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**IRQ 63-32 Active High Polarity Disable (IPC1_IRQAHPOLDIS)** When set to 1, the interrupt polarity associated with IRQ63 down to IRQ32 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

Interrupt Polarity Control 2 (IPC2) – Offset 3208

Interrupt Polarity Control 2 Register

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**IRQ 95-64 Active High Polarity Disable (IPC2_IRQAHPOLDIS)** When set to 1, the interrupt polarity associated with IRQ95 down to IRQ64 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

Interrupt Polarity Control 3 (IPC3) – Offset 320c

Interrupt Polarity Control 3 Register

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
23:0	000000h	RW	**IRQ 119-96 Active High Polarity Disable (IPC3_IRQAHPOLDIS)** When set to 1, the interrupt polarity associated with IRQ119 down to IRQ96 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

ITSS Power Reduction Control (ITSSPRC) – Offset 3300

Power controls for the entire interrupt and timer subsystem.

Bit Range	Default	Access	Field Name and Description
30:4	-	-	**Reserved**
3	0b	RW	**HPET Dynamic Clock Gating Enable (HPETDCGE)** When set, the HPET enables dynamic clock gating.
2	0b	RW	**8254 Static Clock Gating Enable (CGE8254)** When set, the 8254 timer is disabled statically. This bit shall be set by BIOS if the 8254 feature is not needed in the system or before BIOS hands off the system that supports C11. Normal operation of 8254 requires this bit to 0.
1	0b	RW	**Sideband Dynamic Clock Gating Enable (SBDCGE)** Setting this bit will enable all dynamic clock gating of the Sideband Clock domain.
0	0b	RW	**PCI Dynamic Clock Gating Enable (PCIDCGE)** Setting this bit will enable dynamic clock gating for the Interrupt and Timer Sub System Core Logic.

NMI Control (NMI) – Offset 3330

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
4	0b	RO/V	**NMI Status (NMI_STS)** RO status bit indicating the current NMI status. The bit will be set to (1b1) if any NMI source is asserted and NMI2SMI_EN is set to (1b0).
3	0b	RO/V	**NMI-to-SMI Status (NMI2SMI_STS)** RO status bit indicating the current NMI2SMI status. The bit will be set (1b1) if any NMI source is asserted and NMI2SMI_EN is set (1b1).
2	0b	RW	**NMI-to-SMI Enable (NMI2SMI_EN)** Setting to 1b1 causes NMIs to be sent as ASSERT_SMI/DEASSERT_SMI messages to PMC instead of the regular NMI messages. Setting to 1b0 maintains the regular NMI routing (as VLW and VM).Bits NMI_NOW and NMI2SMI_EN can't be configurated on same cycle.
1	0b	RO/V	**NMI NOW Status (NMI_NOW_STS)** RO status bit indicating the current state of NMI_NOW. See NMI_NOW.
0	0b	WO	**NMI Now Command (NMI_NOW)** Writing 1b1 to NMI_NOW inverts the NMI NOW Status (NMI_NOW_STS) value. The first time NMI_NOW is written sets the NMI_NOW_STS and initiates an NMI. The next write clears the NMI_NOW_STS and allows initiating NMI by the next write to NMI_NOW. Writing 1b0 to NMI_NOW has no effect.Bits NMI_NOW and NMI2SMI_EN can't be configurated on same cycle.

Master Message Control (MMC) – Offset 3334

Master Message Control Register

Bit Range	Default	Access	Field Name and Description
14:1	-	-	**Reserved**
0	0b	RW/V	**Master Message Enable (MSTRMSG_EN)** When set, allows Interrupt and Timer Subsystem (ITSS) to release any pending/in progress IOAPIC memory write, HPET memory write, virtual wire event or error messages to the IO frabic. When cleared, ITSS prevents these messages from being issued to the IO frabic.

IO Trap Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1d00h	4	PSTH Control Register (PSTHCTL)	0h
1e00h	4	Trap Status Register (TRPSTS)	0h
1e10h	4	Trapped Cycle Register (TRPCYC1)	0h
1e18h	4	Trapped Write Data Register (TRPWRDATA1)	0h
1e80h	4	I/O Trap Registers 1 (IOTRP1_1)	0h
1e84h	4	I/O Trap Registers 1 (IOTRP1_2)	0h
1e88h	4	I/O Trap Registers 2 (IOTRP2_1)	0h
1e8ch	4	I/O Trap Registers 2 (IOTRP2_2)	0h
1e90h	4	I/O Trap Registers 3 (IOTRP3_1)	0h
1e94h	4	I/O Trap Registers 3 (IOTRP3_2)	0h
1e98h	4	I/O Trap Registers 4 (IOTRP4_1)	0h
1e9ch	4	I/O Trap Registers 4 (IOTRP4_2)	0h

PSTH Control Register (PSTHCTL) – Offset 1d00

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**
2	0b	RW	**PSTH IOSF Primary Clock Gating Enable (PSTHIOSFPTCGE)** 0 = Disable 1 = Enable

Bit Range	Default	Access	Field Name and Description
1	0b	RW	**PSTH IOSF Sideband Clock Gating Enable (PSTHIOSFSTCGE)** 0 = Disable 1 = Enable
0	0b	RW	**PSTH Dynamic Clock Gating Enable (PSTHDCGE)** 0 = Disable 1 = Enable

Trap Status Register (TRPSTS) – Offset 1e00

Bit Range	Default	Access	Field Name and Description
30:4	-	-	**Reserved**
3:0	0h	RW/1C/V	**Cycle Trap SMI# Status (SMISTAT)** These bits are set by hardware when the corresponding Cycle Trap register is enabled and a matching cycle is received (and trapped). These bits are OR'ed together to create a single status bit in the Power Management register space.Note that the SMI# and trapping must be enabled in order to set these bits. This is because, in order to do the cycle comparison, packets must be delayed by several clocks from the DMI pins to the internal receiver. This delay is only enabled when at least one of the trap ranges is enabled. These bits are set before the completion is generated for the trapped cycle, thereby guaranteeing that the processor can enter the SMI# handler when the instruction completes. Each status bit is cleared by writing a '1' to the corresponding bit location in this register.

Trapped Cycle Register (TRPCYC1) – Offset 1e10

This register saves information about the I/O Cycle that was trapped and generated the SMI# for software to read.

Bit Range	Default	Access	Field Name and Description
30:25	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
24	0b	RO/V	**Read-Write (TRPRWR)** 1 = Read, 0 = Write
23:20	-	-	**Reserved**
19:16	0h	RO/V	**Active-High Byte Enables (TRPBE)** This is the DWord-aligned byte enables associated with the trapped cycle. A 1 in any bit location indicates that the corresponding byte is enabled in the cycle.
15:2	00000000000000b	RO/V	**IO Address (TRPADDR)** This is the DWord-aligned address of the trapped cycle.
1:0	-	-	**Reserved**

Trapped Write Data Register (TRPWRDATA1) – Offset 1e18

This register saves the data from I/O write cycles that are trapped for software to read

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO/V	**Data (TRPDATA)** DWord of I/O write data. This field is undefined after trapping a read cycle.

I/O Trap Registers 1 (IOTRP1_1) – Offset 1e80

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
23:18	000000b	RW	**Address Mask (TRP1ADDRM)** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	-	-	**Reserved**
15:2	00000000000000b	RW	**Address (TRP1ADDR)** DWord-aligned address
1	-	-	**Reserved**
0	0b	RW	**Trap and SMI Enable (TRP1EN)** When this bit is set to 1, then the trapping logic specified in this register is enabled.

I/O Trap Registers 1 (IOTRP1_2) – Offset 1e84

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Bit Range	Default	Access	Field Name and Description
30:18	-	-	**Reserved**
17	0b	RW	**Read-Write Mask (TRP1RWM)** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0b	RW	**Read/Write (TRP1RW)** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:4	0h	RW	**Byte Enable Mask (TRP1BEM)** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h	RW	**Byte Enables (TRP1BE)** Active-high, DWord-aligned byte enables

I/O Trap Registers 2 (IOTRP2_1) – Offset 1e88

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:18	000000b	RW	**Address Mask (TRP2ADDRM)** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	-	-	**Reserved**
15:2	00000000000000b	RW	**Address (TRP2ADDR)** DWord-aligned address
1	-	-	**Reserved**
0	0b	RW	**Trap and SMI Enable (TRP2EN)** When this bit is set to 1, then the trapping logic specified in this register is enabled.

I/O Trap Registers 2 (IOTRP2_2) – Offset 1e8c

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Bit Range	Default	Access	Field Name and Description
30:18	-	-	**Reserved**
17	0b	RW	**Read-Write Mask (TRP2RWM)** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0b	RW	**Read/Write (TRP2RW)** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	-	-	**Reserved**
7:4	0h	RW	**Byte Enable Mask (TRP2BEM)** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h	RW	**Byte Enables (TRP2BE)** Active-high, DWord-aligned byte enables

I/O Trap Registers 3 (IOTRP3_1) – Offset 1e90

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:18	000000b	RW	**Address Mask (TRP3ADDRM)** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
15:2	0000000 0000000 b	RW	**Address (TRP3ADDR)** DWord-aligned address
1	-	-	**Reserved**
0	0b	RW	**Trap and SMI Enable (TRP3EN)** When this bit is set to 1, then the trapping logic specified in this register is enabled.

I/O Trap Registers 3 (IOTRP3_2) – Offset 1e94

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Bit Range	Default	Access	Field Name and Description
30:18	-	-	**Reserved**
17	0b	RW	**Read-Write Mask (TRP3RWM)** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0b	RW	**Read/Write (TRP3RW)** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	-	-	**Reserved**
7:4	0h	RW	**Byte Enable Mask (TRP3BEM)** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h	RW	**Byte Enables (TRP3BE)** Active-high, DWord-aligned byte enables

I/O Trap Registers 4 (IOTRP4_1) – Offset 1e98

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:18	000000b	RW	**Address Mask (TRP4ADDRM)** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	-	-	**Reserved**
15:2	00000000000000b	RW	**Reserved (TRP4ADDR)** DWord-aligned address
1	-	-	**Reserved**
0	0b	RW	**Trap and SMI Enable (TRP4EN)** When this bit is set to 1, then the trapping logic specified in this register is enabled.

I/O Trap Registers 4 (IOTRP4_2) – Offset 1e9c

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Bit Range	Default	Access	Field Name and Description
30:18	-	-	**Reserved**
17	0b	RW	**Read-Write Mask (TRP4RWM)** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0b	RW	**Read/Write (TRP4RW)** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:4	0h	RW	**Byte Enable Mask (TRP4BEM)** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h	RW	**Byte Enables (TRP4BE)** Active-high, DWord-aligned byte enables

ISH Registers

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
34h	4	ISH Host Firmware Status (ISH_HOST_FWSTS)	0h
38h	4	Host Communication (HOST_COMM)	0h
48h	4	Inbound Doorbell Host To ISH (HOST2ISH_DOORBELL)	0h
54h	4	Outbound Doorbell ISH to Host (ISH2HOST_DOORBELL)	0h
60h	4	Outbound ISH to Host Message (ISH2HOST_MSG1)	0h
e0h	4	Inbound Host to ISH Message (HOST2ISH_MSG1)	0h
360h	4	Remap 0 (REMAP0)	0h
6d0h	4	D0I3 Control (IPC_d0i3C_reg)	8h

ISH Host Firmware Status (ISH_HOST_FWSTS) – Offset 34

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**ISH Host Firmware Status (ISH_HOST_FWSTS)** This is a 32 bit register which is set to 0x0000 on a system reset or a wakeup from D3Cold. As the firmware comes up after the reset or power cycle it sets bits of this register to indicate its status.

Host Communication (HOST_COMM) – Offset 38

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**Host Communication Register (HOST_COMM)** This is a 32 bit register which is set to 0x0000 on a system reset or a wakeup from D3Cold. The Host sets bits of this register to 1b1 to communicate with the ISH

Inbound Doorbell Host To ISH (HOST2ISH_DOORBELL) – Offset 48

Inbound doorbell register, host core to interrupt ISH. Data 30:0 is 31 bit message payload used for backward compatibility.

Bit Range	Default	Access	Field Name and Description
31	0h	RW	**Doorbell Busy Bit (BUSY)** When this bit is cleared, the ISH CPU is ready to accept a new message.
30:0	0000000 0h	RW	**31 Bit Payload (PAYLOAD_31BIT)** 31 bit message payload for backward compatibility.

Outbound Doorbell ISH to Host (ISH2HOST_DOORBELL) – Offset 54

Outbound doorbell register for the ISH to interrupt the host. Setting bit 31 of this register causes the host to receive a IRQn interrupt. Data 30:0 is 31 bit message payload used for backward compatibility.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31	0h	RW	**Doorbell Busy Bit (BUSY)** When this bit is cleared, the host CPU is ready to accept a new message.
30:0	0000000 0h	RW	**31 Bit Payload (PAYLOAD_31BIT)** 31 bit message payload for backward compatibility.

Outbound ISH to Host Message (ISH2HOST_MSG1) – Offset 60

Inter-process message registers for ISH core to communicate to the host. These are thirty-two 32 bit registers that hold the message payload from the ISH to host.

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**Message 1 from ISH to Host (MSG)** Inter-process message registers for ISH core to communicate to the host. These are thirty-two 32 bit registers that hold the message payload from the ISH to host.

Inbound Host to ISH Message (HOST2ISH_MSG1) – Offset e0

Inter-process message registers for host to communicate to the ISH. These are thirty-two 32 bit registers that hold the message payload from the host to ISH.

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**Message 1 from Host to ISH (MSG)** Inter-process message registers for host to communicate to the ISH. These are thirty-two 32 bit registers that hold the message payload from the host to ISH.

Remap 0 (REMAP0) – Offset 360

At boot time, the host can write these registers with any dynamically allocated address spaces that ISH will have to access.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Remap 0 (REMAP0)** At boot time, the host can write these registers with any dynamically allocated address spaces that ISH will have to access.

D0I3 Control (IPC_d0i3C_reg) – Offset 6d0

This is a 32 bit register which is set to 0 on a system reset or a wakeup from D3Cold. When ME writes to any of these bits with 1, an interrupt is generated. The Interrupt is then cleared by writing 1 `b1 to this register after the appropriate ISR is serviced.

Bit Range	Default	Access	Field Name and Description
30:4	-	-	**Reserved**
3	1h	RW/1C	**Restore Required (ISH_IPC_d0i3C_reg3)** Restore Required bit.
2	0h	RW	**D0i3 (ISH_IPC_d0i3C_reg2)** SW sets this bit to '1' to move the controller into the D0i3 state.Writing this bit to '0' will return the controller to the fully active D0 state (D0i0).Note that this bit is treated by ISH FW as an D0i3 allow indication from SW. Thismeans that if this bit is set to 1, then ISH may be in D0i3 state and if this bit is set to0, then ISH is precluded from being in D0i3 state.
1	0h	RW	**Interrupt Request (ISH_IPC_d0i3C_reg1)** SW sets this bit to '1' to ask for an interrupt to begenerated on completion of the command. SW must clear or set this on each write to this register.
0	0h	RW/1C	**Command-in-Progress (ISH_IPC_d0i3C_reg0)** HW sets this bit on a 1->0 or 0->1 transition of bit2. While set, the other bits in this register are not valid and it is illegal for SW towrite to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit.ISH FW will clear this bit, upon internal logging of the D0i3 allow/disallow (1 or 0state of bit2) indication.

ISH PCH Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID and Vendor ID (DEVVENDID)	22D88086h
4h	4	Status and Command (STATUSCOMMAND)	100000h
8h	4	Revision ID and Class Code (REVCLASSCODE)	6h
ch	4	Cache Line Latency Header and BIST (CLLATHEADERBIST)	0h
10h	4	Base Address Register (BAR)	4h
14h	4	Base Address Register High (BAR_HIGH)	0h
18h	4	Base Address Register1 (BAR1)	0h
1ch	4	Base Address Register1 High (BAR1_HIGH)	0h
2ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)	0h
34h	4	Capabilities Pointer (CAPABILITYPTR)	80h
3ch	4	Interrupt Register (INTERRUPTREG)	0h
80h	4	PowerManagement Capability ID (POWERCAPID)	48039001h
84h	4	Power Management Control and Status (PMECTRLSTATUS)	8h

Device ID and Vendor ID (DEVVENDID) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:16	See Description	RO	**Device Identification (DEVICEID)** This is a 16-bit value assigned to the PCH ISH. Refer to the Device and Revision ID Table in Volume 1 for the default value.
15:0	8086h	RO	**Vendor Identification (VENDORID)** This is a 16-bit value assigned to Intel. Intel VID = 8086h

Status and Command (STATUSCOMMAND) – Offset 4

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29	0h	RW/1C	**Received Master Abort (RMA)**
28	0h	RW/1C	**Received Target Abort (RTA)**
27:21	-	-	**Reserved**
20	1h	RO	**Capabilities List (CAPLIST)** Indicates that the controller contains a capabilities pointer list
19	0h	RO	**Interrupt Status: (INTR_STATUS)** This bit reflects state of interrupt in the device
18:11	-	-	**Reserved**
10	0h	RW	**Interrupt Disable (INTR_DISABLE)**
9	-	-	**Reserved**
8	0h	RW	**SERR Enable (SERR_ENABLE)** Not implemented
7:3	-	-	**Reserved**
2	0h	RW	**Bus Master Enable (BME)**

Bit Range	Default	Access	Field Name and Description
1	0h	RW	**Memory Space Enable (MSE)** 0 = Disables memory mapped configuration space. 1 = Enables memory mapped configuration space
0	-	-	**Reserved**

Revision ID and Class Code (REVCLASSCODE) – Offset 8

Bit Range	Default	Access	Field Name and Description
31:8	000000h	RO	**Class Code (CLASS_CODES)** Class Code register is read-only and is used to identify the generic function of the device, and in some cases, a specific register-level programming interface
7:0	See Description	RO	**Revision ID (RID)** Indicates stepping of the host controller. Refer to Device andRevision ID table in Vol1 for specific value.

Cache Line Latency Header and BIST (CLLATHEADERBIST) – Offset c

Cache Line size as RW with def 0, Latency timer RW with def 0, Header type with Type 0 configuration header and Reserved BIST register

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0h	RO	**Multi-Function Device (MULFNDEV)**
22:16	00h	RO	**Header Type (HEADERTYPE)** Implements Type 0 Configuration header

Bit Range	Default	Access	Field Name and Description
15:8	00h	RO	**Latency Timer (LATTIMER)**
7:0	00h	RW	**Cache Line Size (CACHELINE_SIZE)**

Base Address Register (BAR) – Offset 10

Bit Range	Default	Access	Field Name and Description
31:13	00000h	RW	**Base Address (BASEADDR)** Provides system memory base address.
12:4	00h	RO	**Size Indicator (SIZEINDICATOR)** Always returns. 0 The size of this register depends on the size of the memory space
3	0h	RO	**Prefetchable (PREFETCHABLE)** Indicates that this BAR is not prefetchable
2:1	2h	RO	**Type (TYPE)** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range, If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h	RO	**Memory Space Indicator (MESSAGE_SPACE)** 0 indicates this BAR is present in the memory space.

Base Address Register High (BAR_HIGH) – Offset 14

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Base Address high (BASEADDR_HIGH)**

Base Address Register1 (BAR1) – Offset 18

Bit Range	Default	Access	Field Name and Description
31:12	00000h	RW	**Base Address 1 (BASEADDR1)** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	00h	RO	**Size Indicator (SIZEINDICATOR1)** Always is 0 as minimum size is 4K
3	0h	RO	**Prefetchable (PREFETCHABLE1)** Indicates that this BAR is not prefetchable.
2:1	0h	RO	**Type (TYPE1)** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range. When BAR1_disable bit in Private config space is 1 by default, this field returns 0 on read irrespective of BAR_64b_EN setting
0	0h	RO	**Memory Space Indicator (MESSAGE_SPACE1)** 0 Indicates this BAR is present in the memory space.

Base Address Register1 High (BAR1_HIGH) – Offset 1c

Base Address Register1 High enabled only if [2:1] of BAR1 register is 10

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Base Address 1 High (BASEADDR1_HIGH)**

Subsystem Vendor and Subsystem ID (SUBSYSTEMID) – Offset 2c

SVID register along with SID register is to distinguish subsystem from another

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/O	**Subsystem ID (SUBSYSTEMID)** This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0000h	RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID)** This register must be implemented for any function that can be instantiated more than once in a given system

Capabilities Pointer (CAPABILITYPTR) – Offset 34

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	80h	RO	**Capabilities Pointer (CAPPTR_POWER)** Indicates what the next capability is.

Interrupt Register (INTERRUPTREG) – Offset 3c

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO	**Max Latency (MAX_LAT)** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h	RO	**Min Latency (MIN_GNT)** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	-	-	**Reserved**
11:8	0h	RO	**Interrupt Pin (INTPIN)**

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**Interrupt Line (INTLINE)** It is used to communicate to software, the interrupt line to which the interrupt pin is connected

PowerManagement Capability ID (POWERCAPID) – Offset 80

PowerManagement Capability ID register points to next capability structure and power mgmnt capability , with Power management capabilities register for PME support and version

Bit Range	Default	Access	Field Name and Description
31:27	09h	RO	**PME Support (PMESUPPORT)** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	-	-	**Reserved**
18:16	3h	RO	**Version (VERSION)** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h	RO	**Next Capability (NXTCAP)** Points to the next capability structure.
7:0	01h	RO	**Power Management Capability (POWER_CAP)** Indicates this is power management capability.

Power Management Control and Status (PMECTRLSTATUS) – Offset 84

Power management control and status register to set and read PME status, PME enable, No Soft reset and power state

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
15	0h	RW/1C	**PME Status (PMESTATUS)**
14:9	-	-	**Reserved**
8	0h	RW	**PME Enable (PMEENABLE)**
7:4	-	-	**Reserved**
3	1h	RO	**No Soft Reset (NO_SOFT_RESET)** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	-	-	**Reserved**
1:0	0h	RW	**Power State (POWERSTATE)** This field is used both to determine the current power state and to set a new power state.

ISH PCR Registers

These registers are within the PCH Private Configuration Space which is accessiblethrough the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID+ Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1d0h	4	Power Management Control (PMCTL)	0h

Power Management Control (PMCTL) – Offset 1d0

BIOS may program this register which is used for power management control (clock gating).

Keyboard and Text (KT) Additional Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
54h	4	Power Management Control and Status (KT_CSXE_PMD_PMCSRBSE_PMCSR)	8h

Power Management Control and Status (KT_CSXE_PMD_PMCSRBSE_PMCSR) – Offset 54

Bit Range	Default	Access	Field Name and Description
30:4	-	-	**Reserved**
3	1b	RO	**No Soft Reset (NSR)** When set to 1, this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.
2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1:0	00b	RW	**Power State (PWRST)** This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below: 00b - D0 01b - D1 10b - D2 11b - D3hot If software attempts to write an unsupported, optional state to this field, the write operation will complete normally on the bus; however, the data is discarded and no state change occurs.

Keyboard and Text (KT) PCI Configuration (D22:F3) Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID And Vendor ID (KT_HOST_DID_VID)	638086h
4h	4	Status And Command (KT_HOST_STS_CMD)	B00000h
8h	4	Class Code And Revision ID (KT_HOST_CC_RID)	70002XXh
ch	4	BIST, Header Type, Latency Timer, And Cache Line Size (KT_HOST_BIST_HTYPE_LT_CLS)	800000h
10h	4	KT IO BAR (KT_HOST_IOBAR)	1h
14h	4	KT Memory BAR (KT_HOST_MEMBAR)	0h
28h	4	Cardbus CIS Pointer (KT_HOST_CCP)	0h
30h	4	Expansion ROM Base Address (KT_HOST_XRBAR)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
34h	4	Capabilities List Pointer (KT_HOST_CAPP)	40h
3ch	4	Maximum Latency, Minimum Grant, Interrupt Pin And Interrupt Line (KT_HOST_MAXL_MING_INTP_INTL)	0h
40h	4	MSI Message Control, Next Pointer And Capability ID (KT_HOST_MSIMC_MSINP_MSICID)	805005h
44h	4	MSI Message Address (KT_HOST_MSIMA)	0h
48h	4	MSI Message Upper Address (KT_HOST_MSIMUA)	0h
4ch	4	MSI Message Data (KT_HOST_MSIMD)	0h
50h	4	Power Management Capabilities, Next Pointer And Capability ID (KT_HOST_PMCAP_PMNP_PMCID)	230001h
54h	4	Power Management Data, Control/Status Register Bridge Support Extensions, Control And Status (KT_HOST_PMD_PMCSRBSE_PMCSR)	8h
2ch	4	Subsystem ID And Subsystem Vendor ID (KT_HOST_SID_SVID)	8086h

Device ID And Vendor ID (KT_HOST_DID_VID) – Offset 0

This register contains the device ID and vendor ID values.

Bit Range	Default	Access	Field Name and Description
31:16	0063h	RO/V	**Device ID (DID)** This field identifies the particular device. See the Device and Version ID Table in Volume 1 for the default value.
15:0	8086h	RO	**Vendor ID (VID)** This field identifies the manufacturer of the device. The value of 0x8086 indicates Intel.

Status And Command (KT_HOST_STS_CMD) – Offset 4

This register contins the PCI status and command registers.

Bit Range	Default	Access	Field Name and Description
31	0b	RO	**Detected Parity Error (DPE)** Not implemented. Hardwired to 0.
30	0b	RO	**Signaled System Error (SSE)** Not implemented. Hardwired to 0.
29	0b	RW/1C/V	**Received Master Abort (RMA)** This bit must be set by a master device whenever its transaction (except for Special Cycle) is completed with Unsupported Request Completion Status (a.k.a. Master-Abort). All master devices must implement this bit.
28	0b	RW/1C/V	**Received Target Abort (RTA)** This bit must be set by a master device whenever its transaction is completed with Completer Abort Completion Status (a.k.a. Target-Abort). All master devices must implement this bit.
27	0b	RW/1C/V	**Signaled Target Abort (STA)** This bit must be set by a target device whenever it completes a Posted or Non-Posted transaction with a Completer Abort (a.k.a. Target-Abort) error. Devices that will never signal Completer Abort (a.k.a. Target-Abort) do not need to implement this bit.

Bit Range	Default	Access	Field Name and Description
26:25	00b	RO	**Devsel Timing (DEVT)** These bits encode the timing of DEVSEL#. There are three allowable timings for assertion of DEVSEL# as described below: 00b: fast; 01b: medium; 10b: slow; 11b: reserved. These bits are read-only and must indicate the slowest time that a device asserts DEVSEL# for any bus command except Configuration Read and Configuration Write. Hardwired to 00b.
24	0b	RO	**Master Data Parity Error (MDPE)** Not implemented. Hardwired to 0.

Bit Range	Default	Access	Field Name and Description
23	1b	RO	**Fast Back To Back Capable (FBTBC)** This bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. This bit can be set to 1 if the device can accept these transactions and must be set to 0 otherwise. Hardwired to 1.
22	-	-	**Reserved**
21	1b	RO	**66 Mhz Capable (MCAP)** This bit indicates whether or not this device is capable of running at 66 MHz. A value of 0 indicates 33 MHz. A value of 1 indicates that the device is 66 MHz capable. Hardwired to 1.

Bit Range	Default	Access	Field Name and Description
20	1b	RO	**Capabilities List (CAPL)** This optional read-only bit indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. A value of zero indicates that no New Capabilities linked list is available. A value of one indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities.
19	0b	RO	**Interrupt Status (INTS)** This read-only bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. Read-only and hardwired to 0 for a device that does NOT support pin-based interrupt.
18:11	-	-	**Reserved**
10	0b	RW	**Interrupt Disable (INTD)** This bit disables the device/function from asserting INTx#. A value of 0 enables the assertion of its INTx# signal. A value of 1 disables the assertion of its INTx# signal. This bit's state after RST# is 0.
9	0b	RO	**Fast Back To Back Enable (FBTBEN)** Not implemented. Hardwired to 0.
8	0b	RO	**System Error Enable (SERREN)** Not implemented. Hardwired to 0.
7	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
6	0b	RO	**Parity Error Response (PERRR)** Not implemented. Hardwired to 0.
5	0b	RO	**VGA Palette Snoop (VGAPS)** Not implemented. Hardwired to 0.
4	0b	RO	**Memory Write And Invalidate Enable (MWRIEN)** Not implemented. Hardwired to 0.
3	0b	RO	**Special Cycles (SPCYC)** Not implemented. Hardwired to 0.
2	0b	RW	**Bus Master Enable (BME)** Controls the ability of a PCI device to issue Memory and I/O Read/Write Requests, and the ability of a PCI bridge to forward Memory and I/O Read/Write Requests in the Upstream direction. Devices: When this bit is Set, the PCI device function is allowed to issue Memory or I/O Requests. When this bit is Clear, the PCI device function is not allowed to issue any Memory or I/O Requests. Note that as MSI/MSI-X interrupt Messages are in-band memory writes, setting the Bus Master Enable bit to 0b disables MSI/MSI-X interrupt Messages as well. Requests other than Memory or I/O Requests are not controlled

Bit Range	Default	Access	Field Name and Description
			by this bit. Default value of this bit is 0b. This bit is hardwired to 0b if a PCI device function does not generate Memory or I/O Requests. Bridges: This bit controls forwarding of Memory or I/O Requests by a bridge in the Upstream direction. When this bit is 0b, Memory and I/O Requests received at the Downstream side of a bridge must be handled as Unsupported Requests (UR), and for Non-Posted Requests a Completion with UR completion status must be returned. This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O Requests is not controlled by this bit. Default value of this bit is 0b.

Bit Range	Default	Access	Field Name and Description
1	0b	RW	**Memory Space Enable (MSE)** Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. State after RST# is 0.
0	0b	RW	**IO Space Enable (IOSE)** Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after RST# is 0.

Class Code And Revision ID (KT_HOST_CC_RID) – Offset 8

This register contains the class code and revision ID values.

Bit Range	Default	Access	Field Name and Description
31:24	07h	RO	**Base Class Code (BCC)** Identifies the Base Class Code of an external 16550-compatible serial controller device driver.
23:16	00h	RO	**Sub-Class Code (SCC)** Identifies the Sub-Class Code of an external 16550-compatible serial controller device driver.
15:8	02h	RO	**Programming Interface (PI)** Identifies the Programming Interface of an external 16550-compatible serial controller device driver.
7:0	See Description	RO/V	**Revision ID (RID)** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

BIST, Header Type, Latency Timer, And Cache Line Size (KT_HOST_BIST_HTYPE_LT_CLS) – Offset c

This register contains the BIST, header type, latency timer, and cache line size values.

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO	**Built In Self Test (BIST)** Not implemented. Hardwired to 0.
23	1b	RO/V	**Header Type 1 (HTYPE1)** This bit identifies whether or not the device contains multiple functions. - If the bit is 0, then the device is single function. - If the bit is 1, then the device has multiple functions.
22:16	00h	RO	

Bit Range	Default	Access	Header Type 0 (HTYPE0) Field Name and Description
			This field identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space). - The encoding 00h specifies the non-bridge Configuration Space Header. - The encoding 01h specifies the PCI-to-PCI bridge Configuration Space Header. - The encoding 02h specifies the CardBus bridge Configuration Space Header. - All other encodings are reserved. Hardwired to 0 to identify the non-bridge Configuration Space Header.
15:8	00h	RO	**Latency Timer (LT)** Not implemented. Hardwired to 0.
7:0	00h	RO	**Cache Line Size (CLS)** Not implemented. Hardwired to 0.

KT IO BAR (KT_HOST_IOBAR) – Offset 10

This is the IO space base address register.

Bit Range	Default	Access	Field Name and Description
31:3	0000_0000h	RW	**IO BAR (IOBAR)** Software programs this space with the base address of the device's IO region

Bit Range	Default	Access	Field Name and Description
2	0b	RO	**IO Size (IOSIZE)** Hardwired to 0 to indicate 8B of IO space
1	-	-	**Reserved**
0	1b	RO	**IO Space Indicator (IOSPACE)** Hardwired to 1 to identify an IO BAR.

KT Memory BAR (KT_HOST_MEMBAR) – Offset 14

This is the IO space base address register.

Bit Range	Default	Access	Field Name and Description
31:12	0_0000h	RW	**Memory BAR (MEMBAR)** Software programs this register with the base address of the device's memory region
11:4	00h	RO	**Memory Size (MEMSIZE)** Hardwired to 0 to indicate 4KB of memory space
3	0b	RO	**Prefetchable (PREFETCH)** A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables. Hardwired to 0 to indicate the device's memory space as non-prefetchable.
2:1	00b	RO	**Type (TYP)** Hardwired to 0 to indicate that Base register is 32 bits wide and mapping can be done anywhere in the 32-bit Memory Space.
0	0b	RO	**Memory Space Indicator (MEMSPACE)** Hardwired to 0 to identify a Memory BAR.

Cardbus CIS Pointer (KT_HOST_CCP) – Offset 28

This register contains the cardbus CIS pointer.

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO	**Cardbus CIS Pointer (CCP)** Not implemented. Hardwired to 0.

Expansion ROM Base Address (KT_HOST_XRBAR) – Offset 30

This register contains the expansion read-only memory base address.

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO	**Expansion ROM Base Address (XRBAR)** Not implemented. Hardwired to 0.

Capabilities List Pointer (KT_HOST_CAPP) – Offset 34

This register contains the capabilities list pointer.

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	40h	RO	**Capabilities Pointer (CAPP)** Indicates the pointer for the first entry in the capabilities list which is the MSI Capability.

Maximum Latency, Minimum Grant, Interrupt Pin And Interrupt Line (KT_HOST_MAXL_MING_INTP_INTL) – Offset 3c

This register contains the maximum latency, minumum grand, interrupt pin and interrupt level registers.

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO	**Maximum Latency (MAXL)** Not implemented. Hardwired to 0.
23:16	00h	RO	**Minimum Grant (MING)** Not implemented. Hardwired to 0.

Bit Range	Default	Access	Field Name and Description
15:8	00h	RO/V	**Interrupt Pin (INTP)** This register specifies which interrupt pin KT uses in PCI interrupt mode. Value Decoding 00h The function does NOT use an interrupt pin. 01h INTA 02h INTB 03h INTC 04h INTD 05h - FFh Reserved. Note: this field shadows the KTHIPINR.IPIN field in the PTIO Host private CR space which is configured by BIOS over IOSF SB.

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**Interrupt Line (INTL)** This register is used to communicate interrupt line routing information. POST software will write the routing information into this register as it initializes and configures the system. The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value, rather it is used by device drivers and operating systems. Device drivers and operating systems can use this information to determine priority and vector information. Values in this register are system architecture specific.

MSI Message Control, Next Pointer And Capability ID (KT_HOST_MSIMC_MSINP_MSICID) – Offset 40

This register contains the MSI message control, next pointer And capability ID values.

Bit Range	Default	Access	Field Name and Description
30:25	-	-	**Reserved**
24	0b	RO	**Per Vector Masking Capable (PVMC)** Not implemented. Hardwired to 0 to indicate the function does NOT support MSI per-vector masking.
23	1b	RO	**64 Bit Address Capable (XAC)** Hardwired to 1 to indicate the function is capable of sending a 64-bit message address.

Bit Range	Default	Access	Field Name and Description
22:20	000b	RW	**Multiple Message Enable (MMEN)** Encoded number of interrupt vectors allocated by SW. This field is RW for software compatibility, but only one interrupt vector is ever sent by the function.
19:17	000b	RO	**Multiple Message Capable (MMC)** Encoded number of interrupt vectors requested by a device. Hardwired to 0 to indicate one requested interrupt vector.
16	0b	RW	**MSI Enable (MSIE)** If set, MSI interrupt delivery is enabled whereas pin-based interrupt delivery SHALL be disabled. If cleared, prior to returning the configuration write (that clears this field) completion, the function must send any pending MSI(s).
15:8	50h	RO	**Next Item Pointer (NP)** Indicates the pointer for the next entry in the capabilities list. Hardwired to 50h to point to the PM Capability list
7:0	05h	RO	**Capability ID (CID)** Hardwired to 05h to indicate the linked list item as the MSI Capability registers

MSI Message Address (KT_HOST_MSIMA) – Offset 44

This register contains the MSI message address value.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:2	0000_0000h	RW	**Message Address (MA)** 32-bit DW-aligned MSI message address.
1:0	-	-	**Reserved**

MSI Message Upper Address (KT_HOST_MSIMUA) – Offset 48

This register contains the MSI message upper address value.

Bit Range	Default	Access	Field Name and Description
31:0	0000_0000h	RW	**Message Upper Address (MUA)** Upper 32-bit of a 64-bit DW-aligned MSI message address.

MSI Message Data (KT_HOST_MSIMD) – Offset 4c

This register contains the MSI message data register.

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0000h	RW	**Message Data (MD)** MSI Message Data

Power Management Capabilities, Next Pointer And Capability ID (KT_HOST_PMCAP_PMNP_PMCID) – Offset 50

This register contains the power management capabilities, next pointer And capability ID values.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:27	00000b	RO	**PME Support (PMES)** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(27) X XXX1b - PME# can be asserted from D0 bit(28) X XX1Xb - PME# can be asserted from D1 bit(29) X X1XXb - PME# can be asserted from D2 bit(30) X 1XXXb - PME# can be asserted from D3hot bit(31) 1 XXXXb - PME# can be asserted from D3cold
26	0b	RO	**D2 Support (D2S)** Hardwired to 0 to indicate that this device does not support D2
25	0b	RO	**D1 Support (D1S)** Hardwired to 0 to indicate that this device does not support D1
24:22	000b	RO	**Aux Current (AUXC)** Not implemented. Hardwired to 0.

Bit Range	Default	Access	Field Name and Description
21	1b	RO	**Device Specific Initialization (DSI)** indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. A 1 indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state. Hardwired to 1 to indicate Device Specific Initialization is required.
20	-	-	**Reserved**
19	0b	RO	**PME Clock (PMECLK)** Not implemented. Hardwired to 0.
18:16	011b	RO	**Version (VER)** Hardwired to value of 011b indicates that this function complies with rev 1.2 of PCI Power Management Interface Spec
15:8	00h	RO	**Next Item Pointer (NP)** Indicates the pointer for the next entry in the capabilities list. Hardwired to 0 to indicate no more linked list item.
7:0	01h	RO	**Capability ID (CID)** Hardwired to 01h to indicate the linked list item as the PCI Power Management registers

Power Management Data, Control/Status Register Bridge Support Extensions, Control And Status (KT_HOST_PMD_PMCSRBSE_PMCSR) – Offset 54

This register contains the power management data, control and status register bridge support extensions, control and

status registers.

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO	**Data (Data)** Not implemented. Hardwired to 0.
23:16	00h	RO	**Control/Status Register Bridge Support Extensions (CSRBSE)** Not implemented. Hardwired to 0.
15	0b	RO	**PME Status (PMESTS)** This bit is set when the function would normally assert the PME signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the function to stop asserting a PME (if enabled). Writing a 0 has no effect. If the function supports PME from D3cold, then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded. Not implemented. Hardwired to 0.
14:13	00b	RO	**Data Scale (DS)** Not implemented. Hardwired to 0.
12:9	0000b	RO	**Data Select (DSEL)** Not implemented. Hardwired to 0.

Bit Range	Default	Access	Field Name and Description
8	0b	RO	**PME Enable (PMEEN)** A 1 enables the function to assert PME. When 0, PME assertion is disabled. This bit defaults to 0 if the function does not support PME generation from D3cold. If the function supports PME from D3cold then this bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded. Not implemented. Hardwired to 0.
7:4	-	-	**Reserved**
3	1b	RO	**No Soft Reset (NSR)** When set to 1, this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.
2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1:0	00b	RW	**Power State (PWRST)** This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below: 00b - D0 01b - D1 10b - D2 11b - D3hot If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs.

Bit Range	Default	Access	Field Name and Description

Subsystem ID And Subsystem Vendor ID (KT_HOST_SID_SVID) – Offset 2c

These registers are used to uniquely identify the add-in card or subsystem where the PCI device resides. They provide a mechanism for add-in card vendors to distinguish their add-in cards from one another even though the add-in cards may have the same PCI controller on them (and, therefore, the same Vendor ID and Device ID).

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/O	**Subsystem ID (SID)** Value of this field is vendor-specific. This is written by BIOS. No hardware action will be taken on this value. Implementation Note: The Write-Once lock must be implemented per field. SID should have its own lock.
15:0	8086h	RW/O	**Subsystem Vendor ID (SVID)** This field identifies the vendor of the add-in card or subsystem. This is written by BIOS. No hardware action will be taken on this value. Implementation Note: The Write-Once lock must be implemented per field. SVID should have its own lock.

LPC Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Identifiers (IDTF)	XXXX8086h
4h	2	Device Command (CMD)	7h
6h	2	Status (STS)	200h
8h	1	Revision ID (RID)	XXh
9h	4	Class Code (CC)	60100h
eh	1	Header Type (HTYPE)	80h
2ch	4	Sub System Identifiers (SS)	0h
34h	1	Capability List Pointer (CAPP)	0h
64h	1	Serial IRQ Control (SCNT)	10h
80h	2	I/O Decode Ranges (IOD)	0h
82h	2	I/O Enables (IOE)	0h
84h	4	LPC Generic IO Range 1 (LGIR1)	0h
88h	4	LPC Generic IO Range 2 (LGIR2)	0h
8ch	4	LPC Generic IO Range 3 (LGIR3)	0h
90h	4	LPC Generic IO Range 4 (LGIR4)	0h
94h	4	USB Legacy Keyboard/Mouse Control (ULKMC)	0h
98h	4	LPC Generic Memory Range (LGMR)	0h
d0h	4	FWH ID Select 1 (FS1)	112233h
d4h	2	FWH ID Select 2 (FS2)	4567h
d8h	2	BIOS Decode Enable (BDE)	FFCFh
dch	1	BIOS Control (BC)	20h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
e0h	4	PCI Clock Control (PCCTL)	0h

Identifiers (IDTF) – Offset 0

Identifiers.

Bit Range	Default	Access	Field Name and Description
31:16	See Description	RO/V	**Device Identification (DID)** This is a 16-bit value assigned to the PCH LPC bridge. See the Device and Revision ID Table in Volume 1 for the default value.
15:0	8086h	RO	**Vendor Identification (VID)** Indicates Intel.

Device Command (CMD) – Offset 4

Device Command.

Bit Range	Default	Access	Field Name and Description
14:10	-	-	**Reserved**
9	0b	RO	**Fast Back to Back Enable (FBE)** Reserved as 0 per PCI-Express spec.
8	0b	RW	**SERR# Enable (SEE)** The LPC bridge generates SERR# if this bit is set.
7	0b	RO	**Wait Cycle Control (WCC)** Reserved as 0 per PCI-Express spec.
6	0b	RW	**Parity Error Response Enable (PERE)** When this bit is set to 1, it enables the LPC bridge to response to parity errors detected on backbone interface.

Bit Range	Default	Access	Field Name and Description
5	0b	RO	**VGA Palette Snoop (VGA_PSE)** Reserved as 0 per PCI-Express spec.
4	0b	RO	**Memory Write and Invalidate Enable (MWIE)** Reserved as 0 per PCI-Express spec.
3	0b	RO	**Special Cycle Enable (SCE)** Reserved as 0 per PCI-Express spec.
2	1b	RO	**Bus Master Enable (BME)** Bus Masters cannot be disabled.
1	1b	RO	**Memory Space Enable (MSE)** Memory space cannot be disabled on LPC.
0	1b	RO	**I/O Space Enable (IOSE)** I/O space cannot be disabled on LPC.

Status (STS) – Offset 6

Status.

Bit Range	Default	Access	Field Name and Description
15	0b	RW/1C	**Detected Parity Error (DPE)** Set when the bridge detects a parity error on the internal backbone. This bit gets set even if CMD.PERE is not set.
14	0b	RW/1C	**Signaled System Error (SSE)** Set when the LPC bridge signals a system error to the internal SERR# logic.
13	0b	RO	**Received Master Abort (RMA)** Set when the bridge receives a completion with unsupported request status from the backbone. LPC is a target only controller.
12	0b	RO	**Received Target Abort (RTA)** Set when the bridge receives a completion with completer abort status from the backbone. LPC is a target only controller.

Bit Range	Default	Access	Field Name and Description
11	0b	RW/1C	**Signalled Target Abort (STA)** Set when the bridge generates a completion packet with target abort status on the backbone.
10:9	01b	RO	**DEVSEL# Timing Status (DTS)** Indicates medium timing, although this has no meaning on the backbone.
8	0b	RW/1C	**Data Parity Error Detected (DPD)** Set when the bridge receives a completion packet from the backbone from a previous request, and detects a parity error, and CMD.PERE is set.
7	0b	RO	**Fast Back to Back Capable (FBC)** Reserved.
6	-	-	**Reserved**
5	0b	RO	**66 MHz Capable (C66)** Reserved.
4	0b	RO	**Capabilities List (CLIST)** There is a capabilities list in the LPC bridge.
3:0	-	-	**Reserved**

Revision ID (RID) – Offset 8

Bit Range	Default	Access	Field Name and Description
7:0	See Description	RO/V	**Revision ID (RID)** Indicates the PCH revision. Refer to Device andRevision ID table in Vol1 for specific value.

Class Code (CC) – Offset 9

Class Code.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:16	06h	RO	**Base Class Code (BCC)** Indicates the device is a bridge device.
15:8	01h	RO	**Sub-Class Code (SCC)** Indicates the device a PCI to ISA bridge.
7:0	00h	RO	**Programming Interface (PI)** The LPC bridge has no programming interface.

Header Type (HTYPE) – Offset e

Header Type.

Bit Range	Default	Access	Field Name and Description
7	1b	RO	**Multi-function Device (MFD)** This bit is 1 to indicate a multifunction device.
6:0	00h	RO	**Header Type (HTYPE)** Identifies the header layout of the configuration space, which is a generic device.

Sub System Identifiers (SS) – Offset 2c

This register is initialized to logic 0 by the assertion of PLTRST#. This register can be written only once after PLTRST# de-assertion.

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/O	**Subsystem ID (SSID)** This is written by BIOS. No hardware action taken on this value.
15:0	0000h	RW/O	**Subsystem Vendor ID (SSVID)** This is written by BIOS. No hardware action taken on this value.

Capability List Pointer (CAPP) – Offset 34

Capability List Pointer.

Bit Range	Default	Access	Field Name and Description
7:0	00h	RO	**Capability Pointer (CP)** Indicates the offset of the first Capability Item.

Serial IRQ Control (SCNT) – Offset 64

Serial IRQ Control.

Bit Range	Default	Access	Field Name and Description
7	0b	RW	**Enable (EN)** When set, serial IRQs will be recognized.
6	0b	RW	**Mode (MD)** When set, the serial IRQ machine will be in continuous mode. When cleared, the serial IRQ machine will be in quiet mode. When setting the EN bit, this bit must also be written as a one to guarantee that the first action of the serial IRQ machine will be a start frame.
5:2	4h	RO	**Frame Size (FS)** Fixed field that indicates the size of the SERIRQ frame as 21 frames.

Bit Range	Default	Access	Field Name and Description
1:0	00b	RW	**Start Frame Pulse Width (SFPW)** This is the number of 33 MHz clocks that the SERIRQ pin will be driven low by the Serial IRQ controller to signal a start frame. In continuous mode, the controller will drive the start frame for the number of clocks specified. In quiet mode, the controller will drive the start frame for the number of clocks specified minus one, as the first clock was driven by the peripheral. Bits Clocks 00 4 01 6 10 8 11 Reserved

I/O Decode Ranges (IOD) – Offset 80

I/O Decode Ranges.

Bit Range	Default	Access	Field Name and Description
14:13	-	-	**Reserved**
12	0b	RW	**FDD Range (FDD)** The following table describes which range to decode for the FDD Port Bits Decode Range 0 3F0h - 3F5h, 3F7h (Primary) 1 370h - 375h, 377h (Secondary)
11:10	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
9:8	00b	RW	**LPT Range (LPT)** The following table describes which range to decode for the LPT Port: Bits Decode Range 00 378h - 37Fh and 778h - 77Fh 01 278h - 27Fh (port 279h is read only) and 678h - 67Fh 10 3BCh - 3BEh and 7BCh - 7BEh 11 Reserved
7	-	-	**Reserved**
6:4	000b	RW	**ComB Range (CB)** The following table describes which range to decode for the COMB Port Bits Decode Range 000 3F8h - 3FFh (COM 1) 001 2F8h - 2FFh (COM 2) 010 220h - 227h 011 228h - 22Fh 100 238h - 23Fh 101 2E8h - 2EFh (COM 4) 110 338h - 33Fh 111 3E8h - 3EFh (COM 3)
3	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
2:0	000b	RW	**ComA Range (CA)** The following table describes which range to decode for the COMA Port Bits Decode Range 000 3F8h - 3FFh (COM 1) 001 2F8h - 2FFh (COM 2) 010 220h - 227h 011 228h - 22Fh 100 238h - 23Fh 101 2E8h - 2EFh (COM 4) 110 338h - 33Fh 111 3E8h - 3EFh (COM 3)

I/O Enables (IOE) – Offset 82

I/O Enables.

Bit Range	Default	Access	Field Name and Description
14	-	-	**Reserved**
13	0b	RW	**Microcontroller Enable #2 (ME2)** Enables decoding of I/O locations 4Eh and 4Fh to LPC.
12	0b	RW	**SuperI/O Enable (SE)** Enables decoding of I/O locations 2Eh and 2Fh to LPC.
11	0b	RW	**Microcontroller Enable #1 (ME1)** Enables decoding of I/O locations 62h and 66h to LPC.
10	0b	RW	**Keyboard Enable (KE)** Enables decoding of the keyboard I/O locations 60h and 64h to LPC.
9	0b	RW	**High Gameport Enable (HGE)** Enables decoding of the I/O locations 208h to 20Fh to LPC.

Bit Range	Default	Access	Field Name and Description
8	0b	RW	**Low Gameport Enable (LGE)** Enables decoding of the I/O locations 200h to 207h to LPC.
7:4	-	-	**Reserved**
3	0b	RW	**Floppy Drive Enable (FDE)** Enables decoding of the FDD range to LPC. Range is selected by LIOD.FDE
2	0b	RW	**Parallel Port Enable (PPE)** Enables decoding of the LPT range to LPC. Range is selected by LIOD.LPT.
1	0b	RW	**Com Port B Enable (CBE)** Enables decoding of the COMB range to LPC. Range is selected LIOD.CB.
0	0b	RW	**Com Port A Enable (CAE)** Enables decoding of the COMA range to LPC. Range is selected LIOD.CA.

LPC Generic IO Range 1 (LGIR1) – Offset 84

LPC Generic IO Range 1.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:18	00h	RW	**Address[7:2] Mask (ADDRESS_7_2_MASK)** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	-	-	**Reserved**
15:2	0000h	RW	**Address[15:2] (ADDRESS_15_2)** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.

Bit Range	Default	Access	Field Name and Description
1	-	-	**Reserved**
0	0b	RW	**LPC Decode Enable (LPC_DECODE_ENABLE)** When this bit is set to 1, then the range specified in this register is enabled for decoding to LPC.

LPC Generic IO Range 2 (LGIR2) – Offset 88

Same bit definition as Generic I/O Range #1 (LGIR1).

LPC Generic IO Range 3 (LGIR3) – Offset 8c

Same bit definition as Generic I/O Range #1 (LGIR1).

LPC Generic IO Range 4 (LGIR4) – Offset 90

Same bit definition as Generic I/O Range #1 (LGIR1).

USB Legacy Keyboard/Mouse Control (ULKMC) – Offset 94

USB Legacy Keyboard/Mouse Control.

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15	0b	RW/1C	**SMI Caused by End of Pass-through (SMIBYENDPS)** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 7, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
14:12	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
11	0b	RW/1C	**SMI Caused by Port 64 Write (TRAPBY64W)** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 3, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch. Note that the A20Gate Pass-Through Logic allows specific port 64h Writes to complete without setting this bit.
10	0b	RW/1C	**SMI Caused by Port 64 Read (TRAPBY64R)** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 2, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
9	0b	RW/1C	**SMI Caused by Port 60 Write (TRAPBY60W)** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 1, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch. Note that the A20Gate Pass-Through Logic allows specific port 60h Writes to complete without setting this bit.
8	0b	RW/1C	**SMI Caused by Port 60 Read (TRAPBY60R)** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 0, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
7	0b	RW	**SMI at End of Pass-through Enable (SMIATENDPS)** May need to cause SMI at the end of a pass-through. Can occur if an SMI is generated in the middle of a pass through, and needs to be serviced later.
6	0b	RO	**Pass Through State (PSTATE)** This read-only bit indicates that the state machine is in the middle of an A20GATE pass-through sequence. If software needs to reset this bit, it should set Bit 5 0.
5	0b	RW	**A20Gate Pass-Through Enable (A20PASSEN)** When enabled, allows A20GATE sequence Pass-Through function. When enabled, a specific cycle sequence involving writes to port 60h and port 64h does not result in the setting of the SMI status bits.SMI# will not be generated, even if the various enable bits are set.
4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3	0b	RW	**SMI on Port 64 Writes Enable (S64WEN)** When set, a 1 in bit 11 will cause an SMI event.
2	0b	RW	**SMI on Port 64 Reads Enable (S64REN)** When set, a 1 in bit 10 will cause an SMI event.
1	0b	RW	**SMI on Port 60 Writes Enable (S60WEN)** When set, a 1 in bit 9 will cause an SMI event.
0	0b	RW	**SMI on Port 60 Reads Enable (S60REN)** When set, a 1 in bit 8 will cause an SMI event.

LPC Generic Memory Range (LGMR) – Offset 98

LPC Generic Memory Range.

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW	**Memory Address[31:16] (MA_31_16)** This field specifies a 64KB memory block anywhere in the 4GB memory space that will be decoded to LPC as standard LPC Memory Cycle if enabled.
15:1	-	-	**Reserved**
0	0b	RW	**LPC Memory Range Decode Enable (LMRD_EN)** When this bit is set to 1, then the range specified in this register is enabled for decoding to LPC.

FWH ID Select 1 (FS1) – Offset d0

This register contains the IDSEL fields the LPC Bridge uses for memory cycles going to the FWH.

Bit Range	Default	Access	Field Name and Description
31:28	0h	RO	**F8-FF IDSEL (IF8)** IDSEL to use in FWH cycle for range enabled by BDE.EF8.

Bit Range	Default	Access	Field Name and Description
27:24	0h	RW	**F0-F7 IDSEL (IF0)** IDSEL to use in FWH cycle for range enabled by BDE.EF0.
23:20	1h	RW	**E8-EF IDSEL (IE8)** IDSEL to use in FWH cycle for range enabled by BDE.EE8.
19:16	1h	RW	**E0-E7 IDSEL (IE0)** IDSEL to use in FWH cycle for range enabled by BDE.EE0.
15:12	2h	RW	**D8-DF IDSEL (ID8)** IDSEL to use in FWH cycle for range enabled by BDE.ED8.
11:8	2h	RW	**D0-D7 IDSEL (ID0)** IDSEL to use in FWH cycle for range enabled by BDE.ED0.
7:4	3h	RW	**C8-CF IDSEL (IC8)** IDSEL to use in FWH cycle for range enabled by BDE.EC8.
3:0	3h	RW	**C0-C7 IDSEL (IC0)** IDSEL to use in FWH cycle for range enabled by BDE.EC0.

FWH ID Select 2 (FS2) – Offset d4

This register contains the additional IDSEL fields the LPC Bridge uses for memory cycles going to the FWH.

Bit Range	Default	Access	Field Name and Description
15:12	4h	RW	**70-7F IDSEL (I70)** IDSEL to use in FWH cycle for range enabled by BDE.E70.
11:8	5h	RW	**60-6F IDSEL (I60)** IDSEL to use in FWH cycle for range enabled by BDE.E60.
7:4	6h	RW	**50-5F IDSEL (I50)** IDSEL to use in FWH cycle for range enabled by BDE.E50.
3:0	7h	RW	**40-4F IDSEL (I40)** IDSEL to use in FWH cycle for range enabled by BDE.E40.

BIOS Decode Enable (BDE) – Offset d8

Note that this register effects the BIOS decode regardless of whether the BIOS is resident on LPC or SPI. The concept of Feature Space does not apply to SPI-based flash. PCH simply decodes these ranges as memory accesses when enabled for the SPI flash interface.

Bit Range	Default	Access	Field Name and Description
15	1b	RO	**F8-FF Enable (EF8)** Enables decoding of 512K of the following BIOS range: - Data space: FFF80000h - FFFFFFFFh - Feature space: FFB80000h - FFBFFFFFh
14	1b	RW	**F0-F8 Enable (EF0)** Enables decoding of 512K of the following BIOS range: - Data space: FFF00000h - FFF7FFFFh - Feature space: FFB00000h - FFB7FFFFh
13	1b	RW	**E8-EF Enable (EE8)** Enables decoding of 512K of the following BIOS range: - Data space: FFE80000h - FFEFFFFFh - Feature space: FFA80000h - FFAFFFFFh
12	1b	RW	**E0-E8 Enable (EE0)** Enables decoding of 512K of the following BIOS range: - Data space: FFE00000h - FFE7FFFFh - Feature Space: FFA00000h - FFA7FFFFh
11	1b	RW	**D8-DF Enable (ED8)** Enables decoding of 512K of the following BIOS range: - Data space: FFD80000h - FFDFFFFFh - Feature space: FF980000h - FF9FFFFFh

Bit Range	Default	Access	Field Name and Description
10	1b	RW	**D0-D7 Enable (ED0)** Enables decoding of 512K of the following BIOS range: - Data space: FFD00000h - FFD7FFFFh - Feature space: FF900000h - FF97FFFFh
9	1b	RW	**C8-CF Enable (EC8)** Enables decoding of 512K of the following BIOS range: - Data space: FFC80000h - FFCFFFFFh - Feature space: FF880000h - FF8FFFFFh
8	1b	RW	**C0-C7 Enable (EC0)** Enables decoding of 512K of the following BIOS range: - Data space: FFC00000h - FFC7FFFFh Feature space: FF800000h - FF87FFFFh
7	1b	RW	**Legacy F Segment Enable (LFE)** This enables the decoding of the legacy 64KB range at F0000h - FFFFFh. Note that decode for the BIOS legacy F segment is enabled by the LFE bit only.
6	1b	RW	**Legacy E Segment Enable (LEE)** This enables the decoding of the legacy 64KB range at E0000h - EFFFFh. Note that decode for the BIOS legacy E segment is enabled by the LEE bit only.
5:4	-	-	**Reserved**
3	1b	RW	**70-7F Enable (E70)** Enables decoding of 1MB of the following BIOS range: - Data space: FF700000h - FF7FFFFFh - Feature space: FF300000h - FF3FFFFFh
2	1b	RW	**60-6F Enable (E60)** Enables decoding of 1MB of the following BIOS range: - Data space: FF600000h - FF6FFFFFh Feature Space: FF200000h - FF2FFFFFh

Bit Range	Default	Access	Field Name and Description
1	1b	RW	**50-5F Enable (E50)** Enables decoding of 1MB of the following BIOS range: - Data space: FF500000h - FF5FFFFFh - Feature space: FF100000h - FF1FFFFFh
0	1b	RW	**40-4F Enable (E40)** Enables decoding of 1MB of the following BIOS range: - Data space: FF400000h - FF4FFFFFh - Feature space: FF000000h - FF0FFFFFh

BIOS Control (BC) – Offset dc

BIOS Control.

Bit Range	Default	Access	Field Name and Description
7	0b	RW/1L	**BIOS Interface Lock-Down (BILD)** When set, prevents BC.TS and BC.BBS from being changed. This bit can only be written from 0 to 1 once. BIOS Note: This bit is not backed up in the RTC well. This bit should also be set in the BUC register in the RTC device to record the last state of this value following a cold reset.
6	0b	RW/L	**Boot BIOS Destination (BBS)** This field determines the destination of accesses to the BIOS memory range. For the default, Functional Strap section of Signal Description chapter for details. 0: SPI 1: LPC When SPI or LPC is selected, the range that is decoded is further qualified by other configuration bits described in the respective sections. The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down is not set.

Bit Range	Default	Access	Field Name and Description
5	1b	RW/L	**Enable InSMM.STS (EISS)** When this bit is set, the BIOS region is not writable until SMM sets the InSMM.STS bit. Today BIOS Flash is writable if WPD is a 1. If this bit [5] is set, then WPD must be a 1 and InSMM.STS (0xFED3_0880[0]) must be 1 also. If this bit [5] is clear, then BIOS is writable based only on WPD = 1 and the InSMM.STS is a dont care.
4	0b	RO	**Top Swap (TS)** When set, PCH will invert either A16, A17, A18, A19 or A20 for cycles going to the BIOS space (but not the feature space). When cleared, PCH will not invert the lines. If booting from LPC (FWH), then the Boot Blook size is 64KB and A16 is inverted if Top Swap is enabled. If booting from SPI, then the BOOT_BLOCK_SIZE soft strap determines if A16, A17, A18, A19 or A20 should be inverted if Top Swap is enabled. If PCH is strapped for Top-Swap is low at rising edge of PWROK, then this bit cannot be cleared by software. The strap jumper should be removed and the system rebooted. BIOS Note: 1) This bit provides a read-only path to view the state of the Top Swap strap. It is backed up and driven from the RTC well. Bios will need to program the corresponding register in the RTC Controller (in RTC well), which will be reflected in this register. 2) The Register portion of the Top Swap is lockable by the Bios Interface Lockdown Bit (BC.BILD)
3:2	-	-	**Reserved**
1	0b	RW/1L	**Lock Enable (LE)** When set, setting the WP bit will cause SMI. When cleared, setting the WP bit will not cause SMI. Once set, this bit can only be cleared by a PLTRST#. When this bit is set, EISS - bit [5] of this register is locked down.

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**Write Protect Disable (WPD)** When set, access to the BIOS space is enabled for both read and write cycles to BIOS. When cleared, only read cycles are permitted to the FWH or SPI flash. When this bit is written from a 0 to a 1 and the LE bit is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

PCI Clock Control (PCCTL) – Offset e0

PCI Clock Control.

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9	0b	RO/V	**CLKRUN# Buffer Enable Override (CLKRUN_EN_OVR)** When set to '1', SW is in control of the CLKRUN# buffer enable and the value in CLKRUN_EN_VAL will be propagated to the output buffer enable. When this bit is '0', HW will determine the value of the buffer enable.
8	0b	RO/V	**CLKRUN# Override (CLKRUN_OVR)** When set to '1', SW is in control of the CLKRUN# pin and the value in CLKRUN_VAL will be propagated to the output pin. When this bit is '0', HW will determine the value of the pin.
7	0b	RO/V	**CLKRUN# Buffer Enable Value (CLKRUN_EN_VAL)** Either HW or SW may own control of the CLKRUN# pin. This bit provides the value to drive on the active low CLKRUN# buffer enable if CLKRUN_EN_OVR is set to '1'.
6	0b	RO/V	**CLKRUN# Pin Output Value (CLKRUN_VAL)** Either HW or SW may own control of the CLKRUN# pin. This bit provides the value to drive on the pin if CLKRUN_OVR is set to '1'.

Bit Range	Default	Access	Field Name and Description
5	0b	RO/V	**Stop PCI# Value (STP_PCI_VAL)** Either Hardware or Software may own control of the internal STP_PCI#. This bit provides the value to drive on the STP_PCI# if STP_PCI_OVR is set to 1. Note: SW cannot control the STP_PCI# pin while PLTRST# is asserted (the pin will be at its reset default value).
4	0b	RO/V	**Stop PCI# Override (STP_PCI_OVR)** When set to 1, Firmware is in control of the STP_PCI# and the value in STP_PCI_VAL will be propagated to the internal STP_PCI#. When this bit is '0', HW will determine the value of the pin. Note:Bios cannot control the STP_PCI# pin while PLTRST# is asserted (the pin will be at its reset default value).
3:2	00b	RW	**LPC Clock Valid Configuration (PCLKVLD_CFG)** This field determines the relationship between the internally broadcast indication of the external LPC clock being valid vs. the STP_PCI# pin. Encodings: 00: 1 flop stage of delay from STP_PCI# (default) 01: No delay (edges match STP_PCI# 10: 2 flop stages of delay from STP_PCI# 11: Tie high (indicate that LPC clock is always valid)
1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**Clock Run Enable (CLKRUN_EN)** Enables the CLKRUN# logic to stop the LPC clocks. If the SLP_EN bit is set, then the Intel PCH will drive CLKRUN# low. This will keep the LPC and LPC clocks running on the way to the sleeping state. This is required to meet an LPC specification. This does not necessarily mean that the CLKRUN_EN bit is forced low when SLP_EN is set. Even though the CLKRUN# signal will be low when SLP_EN is set, the state of the CLKRUN_EN bit is ignored when SLP_EN bit is set. This gives flexibility in the implementation.

LPC PCR Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3418h	4	General Control And Function Disable (GCFD)	0h

General Control And Function Disable (GCFD) – Offset 3418

General Control And Function Disable.

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1	0b	RO/V	**eSPI Enable Pin Strap (ESPIEN)** This field determines the destination of accesses to the D31:F0 and related Fixed and Variable IO and Memory decode ranges, including BIOS memory range. 1'b0: LPC is the D31:F0 target. 1'b1: eSPI is the D31:F0 target. Note: This field, along with BC.BBS strap setting determines the final Bios Boot Location.

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**LPC Bridge Disable (LPC_BD)** When set, the LPC bridge is disabled. When disabled the following spaces will no longer be decoded by the LPC bridge: 1) D31:F0 PCI Configuration space 2) Memory cycles below 16MB (1000000h) 3) I/O cycles below 64kB (10000h)

OPI PCR Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2014h	4	Virtual Channel 0 Resource Control (V0CTL)	80000000h
2018h	4	Virtual Channel 0 Resource Status (V0STS)	0h
2020h	4	Virtual Channel 1 Resource Control (V1CTL)	0h
2024h	4	Virtual Channel 1 Resource Status (V1STS)	0h
2040h	4	ME Virtual Channel (VCm) Resource Control (VMCTL)	0h
2044h	4	ME Virtual Channel (VCm) Resource Status (VMSTS)	0h
2084h	4	Uncorrectable Error Status (UES)	0h
2088h	4	Uncorrectable Error Mask (UEM)	0h
208ch	4	Uncorrectable Error Severity (UEV)	0h
2090h	4	Correctable Error Status (CES)	0h
2094h	4	Correctable Error Mask (CEM)	2000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
20ach	4	Root Error Command (REC)	0h
20b0h	4	Root Error Status (RES)	0h
20b4h	4	Error Source Identification (ESID)	0h
2234h	4	DMI Control Register (DMIC)	0h
223ch	4	IOSF Primary Control And Status (IPCS_ IOSFSBCS)	0h
2304h	4	DMI Port Link Control (DMILINKC)	0h
2320h	4	DMI PLL Shutdown (DMIPLLDOWN)	0h
2334h	4	DMI Power Management Control (DMIPMCTL)	0h
2608h	4	Target Link Speed (TLS)	0h
2618h	4	Link Configuration (LCFG)	0h
2730h	4	LPC Generic I/O Range 1 (LPCLGIR1)	0h
2734h	4	LPC Generic I/O Range 2 (LPCLGIR2)	0h
2738h	4	LPC Generic I/O Range 3 (LPCLGIR3)	0h
273ch	4	LPC Generic I/O Range 4 (LPCLGIR4)	0h
2740h	4	LPC Generic Memory Range (LPCGMR)	0h
2744h	4	LPC BIOS Decode Enable (LPCBDE)	FFCFh
274ch	4	General Control and Status (GCS)	0h
2750h	4	I/O Trap Register 1 low (IOT1_LOW)	0h
2754h	4	I/O Trap Register 1 high (IOT1_HIGH)	0h
2770h	4	LPC I/O Decode Range (LPCIOD)	0h
2774h	4	LPC I/O Enable (LPCIOE)	0h
2778h	4	TCO Base Address (TCOBASE)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
27ach	4	PM Base Address (PMBASEA)	0h
27b0h	4	PM Base Control (PMBASEC)	0h
27b4h	4	ACPI Base Address (ACPIBA)	0h
27b8h	4	ACPI Base Destination ID (ACPIBDID)	0h

Virtual Channel 0 Resource Control (V0CTL) – Offset 2014

Bit Range	Default	Access	Field Name and Description
31	1b	RO	**Virtual Channel Enable (EN)** Enables the VC when set. Disables the VC when cleared.
30:27	-	-	**Reserved**
26:24	000b	RO	**Virtual Channel Identifier (ID)** Indicates the ID to use for this virtual channel
23:16	-	-	**Reserved**
15:10	00h	RW/L	**Extended TC/VC Map (ETVM)** Defines the upper 8-bits of the VC0 16-bit TC/VC mapping registers. These registers use the PCI Express reserved TC[3] traffic class bit.This register is locked down if the TCA1.TCLOCKDN register is Read-Only if DMIC.SRL field is set.
9:7	-	-	**Reserved**
6:1	00h	RW/L	**Transaction Class / Virtual Channel Map (TVM)** Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. This register is Read-Only if DMIC.SRL field is set.
0	-	-	**Reserved**

Virtual Channel 0 Resource Status (V0STS) – Offset 2018

Bit Range	Default	Access	Field Name and Description
30:18	-	-	**Reserved**
17	0b	RO/V	**VC Negotiation Pending (NP)** When set, indicates the virtual channel is still being negotiated with ingress ports.
16:0	-	-	**Reserved**

Virtual Channel 1 Resource Control (V1CTL) – Offset 2020

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**Virtual Channel Enable (EN)** Enables the VC when set. Disables the VC when cleared.
30:28	-	-	**Reserved**
27:24	0h	RW/L	**Virtual Channel Identifier (ID)** Indicates the ID to use for this virtual channel. Note: BIOS is required to program VCID[3] to 0 when operating at DMI2.
23:16	-	-	**Reserved**
15:10	00h	RW/L	**Extended TC/VC Map (ETVM)** Defines the upper 8-bits of the VC1 16-bit TC/VC mapping registers. These registers use the PCI Express reserved TC[3] traffic class bit. This register is Read-Only if the DMIC.SRL field is set. If VC1 is not enabled, the register output sent to the users of this register is forced to 0.

Bit Range	Default	Access	Field Name and Description
9:8	-	-	**Reserved**
7:1	00h	RW/L	**Transaction Class / Virtual Channel Map (TVM)** Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. This register is Read-Only if the DMIC.SRL field is set. If VC1 is not enabled, the register output sent to the users of this register is forced to 0.
0	-	-	**Reserved**

Virtual Channel 1 Resource Status (V1STS) – Offset 2024

Offset 2026h: V1STS Virtual Channel 1 Resource Status

Bit Range	Default	Access	Field Name and Description
30:18	-	-	**Reserved**
17	0b	RO/V	**VC Negotiation Pending (NP)** When set, indicates the virtual channel is still being negotiated with ingress ports.
16:0	-	-	**Reserved**

ME Virtual Channel (VCm) Resource Control (VMCTL) – Offset 2040

Offset 2040h: VMCTL ME Virtual Channel (VCm) Resource Control

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**Virtual Channel Enable (EN)** Enables the VC when set. Disables the VC when cleared.

Bit Range	Default	Access	Field Name and Description
30:28	-	-	**Reserved**
27:24	0h	RW/L	**Virtual Channel Identifier (ID)** Indicates the ID to use for this virtual channel.Note: BIOS is required to program VCID[3] to 0 when operating at DMI2.
23:16	-	-	**Reserved**
15:10	00h	RW/L	**Extended TC/VC Map (ETVM)** Defines the upper 8-bits of the VCm 16-bit TC/VC mapping registers. These registers use the PCI Express reserved TC[3] traffic class bit. This register is Read-Only if the DMIC.SRL field is set. If VCm is not enabled, the register output sent to the users of this register is forced to 0.
9:8	-	-	**Reserved**
7:1	00h	RW/L	**Transaction Class / Virtual Channel Map (TVM)** Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. This register is Read-Only if the DMIC.SRL field is set. If VCm is not enabled, the register output sent to the users of this register is forced to 0.
0	-	-	**Reserved**

ME Virtual Channel (VCm) Resource Status (VMSTS) – Offset 2044

Offset 2046h: VMSTS ME Virtual Channel Resource Status

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30:18	-	-	**Reserved**
17	0b	RO/V	**VC Negotiation Pending (NP)** When set, indicates the virtual channel is still being negotiated with ingress ports.
16:0	-	-	**Reserved**

Uncorrectable Error Status (UES) – Offset 2084

Offset 2084h: UES Uncorrectable Error Status

These registers are reset by core PWROK

Bit Range	Default	Access	Field Name and Description
30:21	-	-	**Reserved**
20	0b	RW/1C/V/P	**Unsupported Request Error Status (URE)** Indicates an unsupported request was received.
19	-	-	**Reserved**
18	0b	RW/1C/V/P	**Malformed TLP Status (MT)** Indicates a malformed TLP was received.
17	0b	RW/1C/V/P	**Receiver Overflow Status (RO)** Indicates a receiver overflow occurred.
16	0b	RO	**Unexpected Completion Status (UC)** Reserved, not supported.
15	0b	RW/1C/V/P	**Completer Abort Status (CA)** Indicates a completer abort was received.
14	0b	RO	**Completion Timeout Status (CT)** Reserved, not supported.

Bit Range	Default	Access	Field Name and Description
13	0b	RO	**Flow Control Protocol Error Status (FCPE)** Reserved, not supported.
12	0b	RW/1C/V/P	**Poisoned TLP Status (PT)** Indicates a poisoned TLP was received.
11:1	-	-	**Reserved**
0	0b	RO	**Training Error Status (TE)** Not supported.

Uncorrectable Error Mask (UEM) – Offset 2088

Offset 2088h: UEM Uncorrectable Error Mask

When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled.

These registers are reset by core PWROK

Bit Range	Default	Access	Field Name and Description
30:21	-	-	**Reserved**
20	0b	RW/P	**Unsupported Request Error Mask (URE)** Mask for uncorrectable errors.
19	0b	RO	**ECRC Error Mask (EE)** ECRC is not supported.
18	0b	RW/P	**Malformed TLP Mask (MT)** Mask for malformed TLPs.
17	0b	RW/P	**Receiver Overflow Mask (RO)** Mask for receiver overflows.
16	0b	RO	**Unexpected Completion Mask (UC)** Reserved, Not supported.

Bit Range	Default	Access	Field Name and Description
15	0b	RW/P	**Completer Abort Mask (CM)** Mask for completer abort.
14	0b	RO	**Completion Timeout Mask (CT)** Reserved, not supported.
13	0b	RO	**Flow Control Protocol Error Mask (FCPE)** Not supported.
12	0b	RW/P	**Poisoned TLP Mask (PT)** Mask for poisoned TLPs.
11:5	-	-	**Reserved**
4	0b	RW/P	**Data Link Protocol Error Mask (DLPE)** Mask for data link protocol errors.
3:1	-	-	**Reserved**
0	0b	RO	**Training Error Mask (TE)** Not supported.

Uncorrectable Error Severity (UEV) – Offset 208c

These registers are reset by core PWROK

Bit Range	Default	Access	Field Name and Description
30:21	-	-	**Reserved**
20	0b	RW/P	**Unsupported Request Error Severity (URE)** Severity for unsupported request reception.
19	0b	RO	**ECRC Error Severity (EE)** Not Supported.

Bit Range	Default	Access	Field Name and Description
18	0b	RW/P	**Malformed TLP Severity (MT)** Severity for malformed TLP reception.
17	0b	RW/P	**Receiver Overflow Severity (RO)** Severity for receiver overflow occurrences.
16	0b	RO	**Unexpected Completion Severity (UC)** Not supported.
15	0b	RW/P	**Completer Abort Severity (CA)** Severity for completer.
14	0b	RO	**Completion Timeout Severity (CT)** Not supported.
13	0b	RO	**Flow Control Protocol Error Severity (FCPE)** Not supported.
12	0b	RW/P	**Poisoned TLP Severity (PT)** Severity for poisoned TLP reception.
11:5	-	-	**Reserved**
4	0b	RW/P	**Data Link Protocol Error Severity (DLPE)** Severity for data link protocol errors.
3:1	-	-	**Reserved**
0	0b	RW/P	**Training Error Severity (TE)** TE not supported. This bit is RW for ease of implementation.

Correctable Error Status (CES) – Offset 2090

These registers are reset by core PWROK

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13	0b	RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES)** When set, indicates that a Advisory Non-Fatal Error occurred.
12	0b	RW/1C/V/P	**Replay Timer Timeout Status (RTT)** Indicates the replay timer timed out.
11:9	-	-	**Reserved**
8	0b	RW/1C/V/P	**Replay Number Rollover Status (RNR)** Indicates the replay number rolled over.
7	0b	RW/1C/V/P	**Bad DLLP Status (BD)** Indicates a bad DLLP was received.
6	0b	RW/1C/V/P	**Bad TLP Status (BT)** Indicates a bad TLP was received.
5:1	-	-	**Reserved**
0	0b	RW/1C/V/P	**Receiver Error Status (RE)** Indicates a receiver error occurred.

Correctable Error Mask (CEM) – Offset 2094

Offset 2094h: CEM Correctable Error Mask

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled.

These registers are reset by core PWROK

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
13	1b	RW/P	**Advisory Non-Fatal Error Mask (ANFEM)** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0b	RW/P	**Replay Timer Timeout Mask (RTT)** Mask for replay timer timeout.
11:9	-	-	**Reserved**
8	0b	RW/P	**Replay Number Rollover Mask (RNR)** Mask for replay number rollover.
7	0b	RW/P	**Bad DLLP Mask (BD)** Mask for bad DLLP reception.
6	0b	RW/P	**Bad TLP Mask (BT)** Mask for bad TLP reception.
5:1	-	-	**Reserved**
0	0b	RW/P	**Receiver Error Mask (RE)** Mask for receiver errors.

Root Error Command (REC) – Offset 20ac

Offset 20ACh: REC Root Error Command

In an exposed AER capability, this register allows errors to generate interrupts. For this implementation, and for RCRBs in general, interrupts cannot be generated, so this register is reserved.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31	0b	RW	**Drop Poisoned Downstream Packets (DPDP)** When set to a '1': if downstream packet on OPI is received with the EP bit set, this packet and all subsquent packets with data received on DMI for any VC will have their Unsupported Transaction (UT) field set causing them to be forwarded to the Error Handler. When cleared to a '0', downstream packets from OPI with the EP bit set are forwarded onto the downstream backbone normally.
30	0b	RW	**Unsupported Transaction Policy Bit (UTPB)** When set to 1, the Unsupported Transactions detected on OPI will not set the UES.URE bit. This subsequently ensures that SERR will never be signaled in response to Unsupported Transactions regardless of UEV.URE. When set to 0, the Unsupported Transactions detected on OPI will set the UES.URE bit.
29:0	-	-	**Reserved**

Root Error Status (RES) – Offset 20b0

Offset 20B0h: RES Root Error Status

In an exposed AER capability, this register can track more than one error and set the "multiple" bits if a second or subsequent error occurs and the first has not been serviced. For this implementation, only one error will be captured.

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**
2	0b	RW/1C/V	**ERR_FATAL/NONFATAL Received (ENR)** Set when either a fatal or a non-fatal error message is received or an internal fatal error is detected (all internal uncorrectable errors are fatal).
1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	0b	RW/1C/V	**ERR_COR Received (CR)** Set when a correctable error message is received or an internal correctable error is detected.

Error Source Identification (ESID) – Offset 20b4

Offset 20B4h: ESID Error Source Identification

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RO/V	**ERR_FATAL/NONFATAL Source Identification (EFNFSID)** Loaded with the requester ID indicated in the received ERR_FATAL or ERR_ NONFATAL message when RES.ENR is first set, or the internal requestor ID if an internally detected error.
15:0	0000h	RO/V	**ERR_COR Source Identification (ECSID)** Loaded with the requester ID indicated in the received ERR_COR message when RES.CR is first set, or the internal requester ID if an internally detected error

DMI Control Register (DMIC) – Offset 2234

Offset 2234h: DMIC DMI Control Register (Common)

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**Secured Register Lock (SRL)** When this bit is set, all the secured registers will be locked and will be Read-Only.
30:5	-	-	**Reserved**
4	0b	RW	**Partition/Trunk Oscillator Clock Gate Enable (PTOCGE)** When set, this bit allows the oscillator clock to be gated at the partition/trunk level when the conditions are met. When cleared, the oscillator clock gating at the partition/trunk level is disabled.
3	0b	RW	**DMI Link CLKREQ Enable (DMILCLKREQEN)** When set, this bit enables DMI to de-assert the DMI link CLKREQ. When cleared, DMI link CLKREQ is not allowed to de-assert.

Bit Range	Default	Access	Field Name and Description
2	0b	RW	**DMI Backbone CLKREQ Enable (DMIBBCLKREQEN)** When set, this bit enables DMI to de-assert the Primary backbone CLKREQ. When cleared, DMI Primary backbone CLKREQ is not allowed to de-assert.
1	0b	RW	**DMI Link Dynamic Clock Gate Enable (DMILCGEN)** When set, this bit enables dynamic clock gating on the DMI Link clock domain logic. When cleared, dynamic clock gating on the DMI Link clock domain is disabled.
0	0b	RW	**DMI Backbone Dynamic Clock Gate Enable (DMIBCGEN)** When set, this bit enables dynamic clock gating on the DMI backbone domain logic. When cleared, dynamic clock gating on the DMI backbone clock domain is disabled.

IOSF Primary Control And Status (IPCS_IOSFSBCS) – Offset 223c

Offset 223Ch: IPCS IOSF Primary Control And Status (Common)

Offset 223Eh: IOSFSBCS: IOSF Sideband Control and Status (Common)

Bit Range	Default	Access	Field Name and Description
30:15	-	-	**Reserved**
14:12	000b	RW	**IOSF Primary ISM Idle Counter (PRIC)** BIOS may need to program this register field.
11:0	-	-	**Reserved**

DMI Port Link Control (DMILINKC) – Offset 2304

BIOS may need to program this register.

DMI PLL Shutdown (DMIPLLDOWN) – Offset 2320

BIOS may need to program this register.

DMI Power Management Control (DMIPMCTL) – Offset 2334

BIOS may need to program this register.

Target Link Speed (TLS) – Offset 2608

Offset 2608h: TLS Target Link Speed

Bit Range	Default	Access	Field Name and Description
30:4	-	-	**Reserved**
3:0	0000b	RO/V	**Target Link Speed (TLS)** Specifies the Target link speed that should be used if speed change is supported. Bit Description 0000 SPEED0: 100 Mb/s per-lane 0001 SPEED1: 1 Gb/s per-lane 0010 SPEED2: 2 Gb/s per-lane 0011-1111 Reserved Note: The default value of this field is defined by soft strap. This field is Read-only (RO) with TLS value defined by soft-strap.

Link Configuration (LCFG) – Offset 2618

Offset 2618h: LCFG Link Configuration

Bit Range	Default	Access	Field Name and Description
30:26	-	-	**Reserved**
25	0b	RW/L	**Secure Register Lock (SRL)** When set, the secured register will be locked.
24:0	-	-	**Reserved**

LPC Generic I/O Range 1 (LPCLGIR1) – Offset 2730

Offset 2730h: LPCLGIR1 LPC Generic I/O Range 1

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
23:18	000000b	RW/L	**Address Mask (ADDRMASK)** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
17:16	-	-	**Reserved**
15:2	0000000 0000000 b	RW/L	**Address (ADDR)** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
1	-	-	**Reserved**
0	0b	RW/L	**LPC Decode Enable (LPCDEN)** LPC Decode Enable (LPCDE): When this bit is set to 1 and ISHDE==0, then the range specified in this register is enabled for decoding to LPC. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.

LPC Generic I/O Range 2 (LPCLGIR2) – Offset 2734

Same description as LPCLGIR1 register.

LPC Generic I/O Range 3 (LPCLGIR3) – Offset 2738

Same description as LPCLGIR1 register.

LPC Generic I/O Range 4 (LPCLGIR4) – Offset 273c

Same description as LPCLGIR1 register.

LPC Generic Memory Range (LPCGMR) – Offset 2740

Offset 2740h: LPCGMR LPC Generic Memory Range

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/L	**Memory Address (MEMADDR)** This field specifies a 64KB memory block anywhere in the 4GB memory space that will be decoded to LPC as standard LPC Memory Cycle if enabled. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
15:1	-	-	**Reserved**
0	0b	RW/L	**LPC Memory Range Decode Enable (LPCMRDEN)** When this bit is set to 1, then the range specified in this register is enabled for decoding to LPC. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.

LPC BIOS Decode Enable (LPCBDE) – Offset 2744

Offset 2744h: LPCBDE LPC BIOS Decode Enable

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15	1b	RO	**F8-FF Enable (EF8)** Enables decoding of 512K of the following BIOS range: Data space: FFF80000h – FFFFFFFFh Feature space: FFB80000h – FFBFFFFFh Register Attribute: Static.

Bit Range	Default	Access	Field Name and Description
14	1b	RW/L	**F0-F8 Enable (EF0)** Enables decoding of 512K of the following BIOS range: Data space: FFF00000h – FFF7FFFFh Feature space: FFB00000h – FFB7FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
13	1b	RW/L	**E8-EF Enable (EE8)** Enables decoding of 512K of the following BIOS range: Data space: FFE80000h – FFEFFFFFh Feature space: FFA80000h – FFAFFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
12	1b	RW/L	**E0-E8 Enable (EE0)** Enables decoding of 512K of the following BIOS range: Data space: FFE00000h – FFE7FFFFh Feature Space: FFA00000h – FFA7FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
11	1b	RW/L	**D8-DF Enable (ED8)** Enables decoding of 512K of the following BIOS range: Data space: FFD80000h – FFDFFFFFh Feature space: FF980000h – FF9FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.

Bit Range	Default	Access	Field Name and Description
10	1b	RW/L	**D0-D7 Enable (ED0)** Enables decoding of 512K of the following BIOS range: Data space: FFD00000h – FFD7FFFFh Feature space: FF900000h – FF97FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
9	1b	RW/L	**C8-CF Enable (EC8)** Enables decoding of 512K of the following BIOS range: Data space: FFC80000h – FFCFFFFFh Feature space: FF880000h – FF8FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
8	1b	RW/L	**C0-C7 Enable (EC0)** Enables decoding of 512K of the following BIOS range: Data space: FFC00000h – FFC7FFFFh Feature space: FF800000h – FF87FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
7	1b	RW/L	**Legacy F Segment Enable (LFE)** This enables the decoding of the legacy 64KB range at F0000h – FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
6	1b	RW/L	**Legacy E Segment Enable (LEE)** This enables the decoding of the legacy 64KB range at E0000h – EFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
5:4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3	1b	RW/L	**70-7F Enable (E70)** Enables decoding of 1MB of the following BIOS range: Data space: FF700000h – FF7FFFFFh Feature space: FF300000h – FF3FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
2	1b	RW/L	**60-6F Enable (E60)** Enables decoding of 1MB of the following BIOS range: Data space: FF600000h – FF6FFFFFh Feature Space: FF200000h – FF2FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
1	1b	RW/L	**50-5F Enable (E50)** Enables decoding of 1MB of the following BIOS range: Data space: FF500000h – FF5FFFFFh Feature Space: FF100000h – FF1FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
0	1b	RW/L	**40-4F Enable (E40)** Enables decoding of 1MB of the following BIOS range: Data space: FF400000h – FF4FFFFFh Feature space: FF000000h – FF0FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.

General Control and Status (GCS) – Offset 274c

Offset 274Ch: GCS General Control and Status

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/L	**RPR Destination ID (RPRDID)** This field specifies the PCIe port Destination ID that is the target of the I/O ranges specified in the RPR field.Only one PCIe root port at a time can be enabled for Port 8xh support.This field is only valid when GCS.RPR field is set.BIOS must program the bits which are not used to zeros.This register is Read-Only if the DMIC.SRL field is set.Register Attribute: Static.
15:12	-	-	**Reserved**
11	0b	RW/L	**Reserved Page Route (RPR)** Determines where to send the reserved page registers. These addresses are sent to PCIe Root Port or LPC/eSPI for the purpose of generating POST codes. The I/O addresses modified by this field are: 80h - 8Fh. When cleared, DMI will not perform source decode on the I/O ranges specified above. The cycles hitting these ranges will end up in P2SB which will then forward the cycle to LPC or eSPI through IOSF Sideband. When set, access to the I/O ranges specified above will be forwarded to PCIe Root Port with the destination ID specified in GCS.RPRDID using DMI source decode. The aliases for these registers, at 90h, 94h, 95h, 96h, 98h, 9Ch, 9Dh, and 9Eh, are never source decoded by DMI. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
10	0b	RW/V/L	**Boot BIOS Strap (BBS)** This field determines the destination of accesses to the BIOS memory range. Bits Description 0 SPI 1 LPC/eSPI When SPI or LPC/eSPI is selected, the range that is decoded is further qualified by other configuration bits described in the respective sections. The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down (bit 0) and DMIC.SRL are not set. Register Attribute: Static.

Bit Range	Default	Access	Field Name and Description
9:1	-	-	**Reserved**
0	0b	RW/O	**BIOS Interface Lock-Down (BILD)** BIOS Interface Lock-Down (BILD): When set, prevents GCS.BBS from being changed. This bit can only be written from 0 to 1 once. Register Attribute: Static.

I/O Trap Register 1 low (IOT1_LOW) – Offset 2750

Offset 2750h: IOT1 I/O Trap Register 1 Low

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:18	000000b	RW	**Address Mask (ADDRMASK)** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	-	-	**Reserved**
15:2	00000000000000b	RW	**Address (ADDR)** DWord-aligned address.
1	-	-	**Reserved**
0	0b	RW	**Trap and SMI# Enable (TNSMIEN)** When this bit is set to 1, then the trapping logic specified in this register is enabled.

I/O Trap Register 1 high (IOT1_HIGH) – Offset 2754

Offset 2754h: IOT1 I/O Trap Register 1 High

Bit Range	Default	Access	Field Name and Description
30:18	-	-	**Reserved**
17	0b	RW	**Read/Write Mask (RWMASK)** When this bit is 1, the trapping logic will operate on both read and write cycles. When this bit is 0, the cycle must match the type specified in bit 16.
16	0b	RW	**Read/Write# (RW)** 1 = Read 0 = Write The value in this field does not matter if bit 17 is set.
15:8	-	-	**Reserved**
7:4	0h	RW	**Byte Enable Mask (BEMASK)** A 1 in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h	RW	**Byte Enables (BE)** Active-high, DWord-aligned byte enables.

LPC I/O Decode Range (LPCIOD) – Offset 2770

Offset 2770h: LPCIOD LPC I/O Decode Ranges

Bit Range	Default	Access	Field Name and Description
30:13	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
12	0b	RW/L	**FDD Range (FDD)** The following table describes which range to decode for the FDD Port. Bits Decode Range 0 3F0h – 3F5h, 3F7h (Primary) 1 370h – 375h, 377h (Secondary) This register is Read-Only if the DMIC.SRL field is set.
11:10	-	-	**Reserved**
9:8	00b	RW/L	**LPT Range (LPT)** The following table describes which range to decode for the LPT Port. Bits Decode Range 00 378h - 37Fh and 778h – 77Fh 01 278h – 27Fh (port 279h is read only) and 678h – 67Fh 10 3BCh – 3BEh and 7BCh – 7BEh 11 Reserved This register is Read-Only if the DMIC.SRL field is set.
7	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
6:4	000b	RW/L	**ComB Range (CB)** The following table describes which range to decode for the COMB Port. Bits Decode Range 000 3F8h – 3FFh (COM1) 001 2F8h – 2FFh (COM2) 010 220h – 227h 011 228h – 22Fh 100 238h – 23Fh 101 2E8h – 2EFh (COM 4) 110 338h – 33Fh 111 3E8h – 3EFh (COM 3) This register is Read-Only if the DMIC.SRL field is set.
3	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
2:0	000b	RW/L	**ComA Range (CA)** The following table describes which range to decode for the COMA Port. Bits Decode Range 000 3F8h – 3FFh (COM1) 001 2F8h – 2FFh (COM2) 010 220h – 227h 011 228h – 22Fh 100 238h – 23Fh 101 2E8h – 2EFh (COM 4) 110 338h – 33Fh 111 3E8h – 3EFh (COM 3) This register is Read-Only if the DMIC.SRL field is set.

LPC I/O Enable (LPCIOE) – Offset 2774

Offset 2774h: LPCIOE LPC I/O Enables

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9	0b	RW/L	**High Gameport Enable (HGE)** Enables decoding of the I/O locations 208h to 20Fh to LPC. This register is Read-Only if the DMIC.SRL field is set.
8	0b	RW/L	**Low Gameport Enable (LGE)** Enables decoding of the I/O locations 200h to 207h to LPC.This register is Read-Only if the DMIC.SRL field is set.

Bit Range	Default	Access	Field Name and Description
7:4	-	-	**Reserved**
3	0b	RW/L	**Floppy Drive Enable (FDE)** Enables decoding of the FDD range to LPC. Range is selected by LIOD.FDE. This register is Read-Only if the DMIC.SRL field is set.
2	0b	RW/L	**Parallel Port Enable (PPE)** Enables decoding of the LPT range to LPC. Range is selected by LIOD.LPT. This register is Read-Only if the DMIC.SRL field is set.
1	0b	RW/L	**Com Port B Enable (CBE)** Enables decoding of the COMB range to LPC. Range is selected by LIOD.CB. This register is Read-Only if the DMIC.SRL field is set.
0	0b	RW/L	**Com Port A Enable (CAE)** Enables decoding of the COMA range to LPC. Range is selected by LIOD.CA. This register is Read-Only if the DMIC.SRL field is set.

TCO Base Address (TCOBASE) – Offset 2778

Offset 2778h: TCOBASE TCO Base Address

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:5	000h	RW/L	**TCO Base Address (TCOBA)** Provides the 32 bytes of I/O space for TCO logic, that can be map anywhere in the 64k I/O space on 32-byte boundaries. This register is Read-Only if the DMIC.SRL field is set.
4:2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1	0b	RW/L	**TCO Enable (TCOEN)** When set, decode of the I/O range specified by the TCO base address. This register is Read-Only if the DMIC.SRL field is set.
0	-	-	**Reserved**

PM Base Address (PMBASEA) – Offset 27ac

Offset 27ACh: PMBASEA PM Base Address

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/L	**PM Base Address Memory Range Limit (PMBAMRL)** This field specifies limit address bits[31:16] for the PM Base Address memory range. Bits [15:0] are assumed to be FFFFh. This register is Read-Only if the DMIC.SRL field is set.
15:0	0000h	RW/L	**PM Base Address Memory Range Base (PMBAMRB)** This field specifies base address bits[31:16] for the PM Base Address memory range. Bits [15:0] are assumed to be 0000h. This register is Read-Only if the DMIC.SRL field is set.

PM Base Control (PMBASEC) – Offset 27b0

Offset 27B0h: PMBASEC PM Base Control

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**PM Base Address Memory Range Decode Enable (PMBAMRDE)** When enabled, memory cycles that falls within the PMBASEADDR.PMBAMRB and PMBASEADDR.PMBAMRL range inclusive will be forwarded using source decode to the destination ID specified in PMBASEC.PMBDID field. This register is Read-Only if the DMIC.SRL field is set.

Bit Range	Default	Access	Field Name and Description
30:0	0000000 0h	RW/L	**PM Base Destination ID (PMBDID)** The destination ID to be used to forward the cycle decoded to hit the PM Base Address range. BIOS must program the bits which are not used to zeros. Hardware will ignore the unused bits. This register is Read-Only if the DMIC.SRL field is set.

ACPI Base Address (ACPIBA) – Offset 27b4

Offset 27B4h: ACPIBA ACPI Base Address

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:18	000000b	RW/L	**Address[7:2] Mask (ADDR72MASK)** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size. This register is Read-Only if the DMIC.SRL field is set.
17:16	-	-	**Reserved**
15:2	0000h	RW/L	**Address[15:2] (ADDR)** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level. This register is Read-Only if the DMIC.SRL field is set.
1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	0b	RW/L	**ACPI Base Address Decode Enable (ACPIBADE)** When this bit is set to 1, then the range specified in this register is enabled for decoding to the destination ID specified in ACPIBDID register. This register is Read-Only if the DMIC.SRL field is set.

ACPI Base Destination ID (ACPIBDID) – Offset 27b8

Offset 27B8h: ACPIBDID ACPI Base Destination ID

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW/L	**ACPI Base Destination ID (ACPIBDID)** The destination ID to be used to forward the cycle decoded to hit the ACPI Base Address range. BIOS must program the bits which are not used to zeros. Hardware will ignore the unused bits. This register is Read-Only if the DMIC.SRL field is set.

P2SB PCI Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	PCI Identifier (PCIID)	XXXX8086h
4h	2	PCI Command (PCICMD)	4h
8h	1	Revision ID (PCIRID)	0h
9h	4	Class Code (PCICC)	58000h
eh	1	PCI Header Type (PCIHTYPE)	0h
10h	4	Sideband Register Access BAR (SBREG_BAR)	4h
14h	4	Sideband Register BAR High DWORD (SBREG_BARH)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2ch	4	PCI Subsystem Identifiers (PCIHSS)	0h
50h	2	VLW Bus:Device:Function (VBDF)	F8h
52h	2	ERROR Bus:Device:Function (EBDF)	F8h
54h	4	Routing Configuration (RCFG)	C700h
60h	1	High Performance Event Timer Configuration (HPTC)	0h
64h	2	IOxAPIC Configuration (IOAC)	0h
6ch	2	IOxAPIC Bus:Device:Function (IBDF)	F8h
70h	2	HPET Bus:Device:Function (HBDF)	F8h
c0h	4	Display Bus:Device:Function (DISPBDF)	60010h
c4h	2	ICC Register Offsets (ICCOS)	0h
d0h	4	SBI Address (SBIADDR)	0h
d4h	4	SBI Data (SBIDATA)	0h
d8h	2	SBI Status (SBISTAT)	0h
dah	2	SBI Routing Identification (SBIRID)	0h
dch	4	SBI Extended Address (SBIEXTADDR)	0h
e0h	4	P2SB Control (P2SBC)	0h
e4h	1	Power Control Enable (PCE)	1h
200h	4	Sideband Register Posted 0 (SBREGPOSTED0)	0h
204h	4	Sideband Register Posted 1 (SBREGPOSTED1)	0h
208h	4	Sideband Register Posted 2 (SBREGPOSTED2)	0h
20ch	4	Sideband Register Posted 3 (SBREGPOSTED3)	0h
210h	4	Sideband Register Posted 4 (SBREGPOSTED4)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
214h	4	Sideband Register Posted 5 (SBREGPOSTED5)	0h
218h	4	Sideband Register Posted 6 (SBREGPOSTED6)	0h
21ch	4	Sideband Register Posted 7 (SBREGPOSTED7)	0h
220h	4	Endpoint Mask 0 (EPMASK0)	0h
224h	4	Endpoint Mask 1 (EPMASK1)	0h
228h	4	Endpoint Mask 2 (EPMASK2)	0h
22ch	4	Endpoint Mask 3 (EPMASK3)	0h
230h	4	Endpoint Mask 4 (EPMASK4)	0h
234h	4	Endpoint Mask 5 (EPMASK5)	0h
238h	4	Endpoint Mask 6 (EPMASK6)	0h
23ch	4	Endpoint Mask 7 (EPMASK7)	0h

PCI Identifier (PCIID) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:16	See Description	RO/V	**Device Identification (DID)** This field identifies the particular device. Refer to the Device andRevision ID Table in Volume 1 for default value.
15:0	8086h	RO	**Vendor Identification (VID)** Indicates Intel

PCI Command (PCICMD) – Offset 4

Bit Range	Default	Access	Field Name and Description
14:11	-	-	**Reserved**
10	0b	RO	**Interrupt Disable (INTD)** P2SB does not issue any interrupts on its own behalf
9	0b	RO	**Fast Back to Back Enable (FB2BE)** Not applicable
8:6	-	-	**Reserved**
5	0b	RO	**VGA Palette Snoop (VGA)** Not applicable.
4	0b	RO	**Memory Write & Invalidate Enable (MWIE)** Not applicable.
3	0b	RO	**Special Cycle Enable (SCE)** Not applicable.
2	1b	RO	**Bus Master Enable (BME)** Bus mastering cannot be disabled as this device acts as a proxy for non-PCI devices.
1	0b	RW	**Memory Space Enable (MSE)** Will control the P2SB acceptance of PCI MMIO BARs only. Other legacy regions are unaffected by this bit.
0	0b	RW	**I/O Space Enable (IOSE)** Legacy regions are unaffected by this bit.

Revision ID (PCIRID) – Offset 8

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
7:0	See Description	RO/V	**Revision ID (RID)** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

Class Code (PCICC) – Offset 9

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:16	05h	RO	**Base Class Code (BCC)** Indicates a memory controller device class.
15:8	80h	RO	**Sub-Class Code (SCC)** Indicates an unspecified other memory controller.
7:0	00h	RO	**Programming Interface (PI)** No programming interface.

PCI Header Type (PCIHTYPE) – Offset e

Bit Range	Default	Access	Field Name and Description
7	0b	RO	**Multi-Function Device (MFD)** Indicates that this is part of a multi-function device.
6:0	0000000b	RO	**Header Type (HTYPE)** Indicates a generic device header.

Sideband Register Access BAR (SBREG_BAR) – Offset 10

Bit Range	Default	Access	Field Name and Description
31:24	00h	RW	**Register Base Address (RBA)** Lower DWORD of the base address for the sideband register access BAR.
23:4	-	-	**Reserved**
3	0b	RO	**Prefetchable (PREF)** Indicates this is not prefetchable.
2:1	10b	RO	**Address Type (ATYPE)** Indicates that this can be placed anywhere in 64b space.
0	0b	RO	**Space Type (STYPE)** Indicates memory space

Sideband Register BAR High DWORD (SBREG_BARH) – Offset 14

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Register Base Address (RBAH)** Upper DWORD of the base address for the sideband register access BAR.

PCI Subsystem Identifiers (PCIHSS) – Offset 2c

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/O	**Subsystem ID (SSID)** Written by BIOS. Not used by hardware.
15:0	0000h	RW/O	**Subsystem Vendor ID (SSVID)** Written by BIOS. Not used by hardware.

VLW Bus:Device:Function (VBDF) – Offset 50

This register specifies the bus:device:function ID that will be used for its Requester ID. This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required.

Bit Range	Default	Access	Field Name and Description
15:8	00h	RW	**Bus Number (BUS)** VLW Bus Number
7:3	11111b	RW	**Device Number (DEV)** VLW Device Number
2:0	000b	RW	**Function Number (FUNC)** VLW Function Number

ERROR Bus:Device:Function (EBDF) – Offset 52

This register specifies the bus:device:function ID that the Error Signalling messages will use for its Requester ID. This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required.

Bit Range	Default	Access	Field Name and Description
15:8	00h	RW	**Bus Number (BUS)** ERROR Bus Number
7:3	11111b	RW	**Device Number (DEV)** ERROR Device Number
2:0	000b	RW	**Function Number (FUNC)** ERROR Function Number

Routing Configuration (RCFG) – Offset 54

This register contains information used for routing transactions between primary and sideband interfaces.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:8	C7h	RW	**Reserved Page Register Destination ID (RPRID)** Specifies the IOSF-SB destination ID for sending Reserved Page Register cycles (e.g. Port 80h). By default this will load to the ID of the LPC or eSPI device depending on which has been strapped active in the system.
7:1	-	-	**Reserved**
0	0b	RW	**RTC Shadow Enable (RSE)** When set, all IO writes to the RTC will be also sent to the PMC. This allows cases where the battery backed storage is in an external PMIC.

High Performance Event Timer Configuration (HPTC) – Offset 60

HPET configuration register

Bit Range	Default	Access	Field Name and Description
7	0b	RW	**Address Enable (AE)** When set, the P2SB will decode the High Performance Timer memory address range selected by bits 1:0 below.
6:2	-	-	**Reserved**
1:0	00b	RW	**Address Select (AS)** This 2-bit field selects 1 of 4 possible memory address ranges for the High Performance Timer functionality. The encodings are: 00 : FED0_0000h - FED0_03FFFh 01 : FED0_1000h - FED0_13FFFh 10 : FED0_2000h - FED0_23FFFh 11 : FED0_3000h - FED0_33FFFh

IOxAPIC Configuration (IOAC) – Offset 64

IOAPIC configuration register

Bit Range	Default	Access	Field Name and Description
14:9	-	-	**Reserved**
8	0b	RW	**Address Enable (AE)** When set, the P2SB will decode the IOxAPIC memory address range selected by bits 7:0 below.
7:0	00h	RW	**APIC Range Select (ASEL)** These bits define address bits 19:12 for the IOxAPIC range. The default value of 00h enables compatibility with prior products as an initial value. This value must not be changed unless the IOxAPIC Enable bit is cleared.

IOxAPIC Bus:Device:Function (IBDF) – Offset 6c

This register specifies the bus:device:function ID that the IOxAPIC will use in the following :

As the Requester ID when initiating Interrupt Messages to the CPU

As the Completer ID when responding to the reads targeting the IOxAPICs Memory-Mapped I/O registers

This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required for the internal IOxAPIC.

Bit Range	Default	Access	Field Name and Description
15:8	00h	RW	**Bus Number (BUS)** IOxAPIC Bus Number
7:3	11111b	RW	**Device Number (DEV)** IOxAPIC Device Number
2:0	000b	RW	**Function Number (FUNC)** IOxAPIC Function Number

HPET Bus:Device:Function (HBDF) – Offset 70

This register specifies the bus:device:function ID that the HPET device will use in the following :

As the Requester ID when initiating Interrupt Messages to the CPU

As the Completer ID when responding to the reads targeting the corresponding HPETs Memory-Mapped I/O registers

This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required for the corresponding HPET.

Bit Range	Default	Access	Field Name and Description
15:8	00h	RW	**Bus Number (BUS)** HPET Bus Number
7:3	11111b	RW	**Device Number (DEV)** HPET Device Number
2:0	000b	RW	**Function Number (FUNC)** HPET Function Number

Display Bus:Device:Function (DISPBDF) – Offset c0

This register specifies the bus:device:function ID that the Display initiated upstream RAVDMs will use for its Requester ID. This will also be used for the claiming these Route-by-ID RAVDMs downstream.

Bit Range	Default	Access	Field Name and Description
30:19	-	-	**Reserved**
18:16	110b	RW	**Display Target Block (DTBLK)** This register contains the Target BLK field that will be used when sending RAVDM messages to the CPU Complex North Display.
15:8	00h	RW	**Bus Number (BUS)** The bus number of the Display in the CPU Complex.
7:3	00010b	RW	**Device Number (DEV)** The bus number of the Display in the CPU Complex.
2:0	000b	RW	**Function Number (FUNC)** The function number of the Display in the CPU Complex

ICC Register Offsets (ICCOS) – Offset c4

This register contains the offsets to be used when sending RAVDMs to the Integrated Clock Controller. Each of the two spaces decoded for the ICC have a separate base address that will be used when sending those transactions on IOSF-SB to the ICC.

Bit Range	Default	Access	Field Name and Description
15:8	00h	RW	**Modulator Control Address Offset (MODBASE)** This specifies the upper 8b for the 16b address that will be used for sending RAVDM access that target the Modulator Control range of the ICC (FFF00h - FFFFFh).
7:0	00h	RW	**Buffer Address Offset (BUFBASE)** This specifies the upper 8b for the 16b address that will be used for sending RAVDM access that target the Buffer range of the ICC (FFE00h - FFEFFh).

SBI Address (SBIADDR) – Offset d0

Provides mechanism to send message on IOSF-SB.

Bit Range	Default	Access	Field Name and Description
31:24	00h	RW	**Destination Port ID (DESTID)** The content of this register field is sent in the IOSF Sideband Message Register Access dest field.
23:16	-	-	**Reserved**
15:0	0000h	RW	**Address Offset (OFFSET)** Register address offset. The content of this register field is sent in the IOSF Sideband Message Register Access address(15:0) field.

SBI Data (SBIDATA) – Offset d4

Provides mechanism to send message on IOSFSB

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW/V	**Data (DATA)** The content of this register field is sent on the IOSF sideband Message Register Access data(31:0) field.

SBI Status (SBISTAT) – Offset d8

Provides mechanism to send message on IOSFSB

Bit Range	Default	Access	Field Name and Description
15:8	00h	RW	**Opcode (OPCODE)** This is the Opcode sent in the IOSF sideband message.
7	0b	RW	**Posted (POSTED)** When set to 1, the message will be sent as a posted message instead of non-posted. This should only be used if the receiver is known to support posted operations for the specified operation.
6:3	-	-	**Reserved**
2:1	00b	RW/V	**Response Status (RESPONSE)** 00 - Successful 01 - Unsuccessful / Not Supported 10 - Powered Down 11 - Multi-cast Mixed This register reflects the response status for the previously completed transaction. The value of this register is only meaningful if SBISTAT.INITRDY is zero.
0	0b	RW/1S	**Initiate/ Ready# (INITRDY)** 0: The IOSF sideband interface is ready for a new transaction 1: The IOSF sideband interface is busy with the previous transaction. A write to set this register bit to 1 will trigger an IOSF sideband message on the private IOSF sideband interface. The message will be formed based on the values programmed in the Sideband Message Interface Register Access registers. Software needs to ensure that the interface is not busy (SBISTAT.INITRDY is clear) before writing to this register.

SBI Routing Identification (SBIRID) – Offset da

Provides mechanism to send message on IOSFSB

Bit Range	Default	Access	Field Name and Description
15:12	0h	RW	**First Byte Enable (FBE)** The content of this field is sent in the IOSF Sideband Register Access FBE field.
11	-	-	**Reserved**
10:8	000b	RW	**Base Address Register (BAR)** The contents of this field are sent in the IOSF Sideband Register Access BAR field. This should be zero performing a Memory Mapped operation to a PCI compliant device.
7:0	00h	RW	**Function ID (FID)** The contents of this field are sent in the IOSF Sideband Register access FID field. This field should generally remain at zero unless specifically required by a particular application.

SBI Extended Address (SBIEXTADDR) – Offset dc

Provides mechanism to send message on IOSFSB

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Extended Address (ADDR)** The content of this register field is sent on the IOSF sideband Message Register Access address(48:32) field. This must be set to all 0 if 16b addressing is desired.

P2SB Control (P2SBC) – Offset e0

P2SB general configuration register

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31	0b	RW/O	**SBI register Lock (SBILOCK)** Once written, it will not be writeable until reset. When 1, the bit will lock down access to the P2SB SBI register (P2SB PCI offsets D0h - DFh)
30:18	-	-	**Reserved**
17	0b	RW/O	**Endpoint Mask Lock (MASKLOCK)** Locks the value of the EPMASK[0-7] registers. Once this value is written to a one it may only be cleared by a reset.
16:9	-	-	**Reserved**
8	0b	RW	**Hide Device (HIDE)** When this bit is set, the P2SB will return 1s on any PCI Configuration Read on IOSF-P. All other transactions including PCI Configuration Writes are unaffected by this. This does not affect reads performed on the IOSF-SB interface.
7:0	-	-	**Reserved**

Power Control Enable (PCE) – Offset e4

Power Control Enable register

Bit Range	Default	Access	Field Name and Description
6	-	-	**Reserved**
5	0b	RW	**Hardware Autonomous Enable (HAE)** When set, the P2SB will automatically engage power gating when it has reached its idle condition.

Bit Range	Default	Access	Field Name and Description
4:3	-	-	**Reserved**
2	0b	RO	**D3-Hot Enable (D3HE)** No support for D3 Hot power gating.
1	0b	RO	**I3 Enable (I3E)** No support for S0i3 power gating.
0	1b	RW	**PMC Power Gating Enable (PMCPG_EN)** When set to 1, the P2SB will engage power gating if it is idle (and an internal PMC power gating signal is asserted.)

Sideband Register Posted 0 (SBREGPOSTED0) – Offset 200

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space

Bit Range	Default	Access	Field Name and Description
31:0	00h	RW	**Sideband Register Posted 0 (SBREGPOSTED0)** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 31-0.

Sideband Register Posted 1 (SBREGPOSTED1) – Offset 204

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space

Bit Range	Default	Access	Field Name and Description
31:0	00h	RW	**Sideband Register Posted 1 (SBREGPOSTED1)** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 63-32.

Sideband Register Posted 2 (SBREGPOSTED2) – Offset 208

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space

Bit Range	Default	Access	Field Name and Description
31:0	00h	RW	**Sideband Register Posted 0 (SBREGPOSTED2)** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 95-64.

Sideband Register Posted 3 (SBREGPOSTED3) – Offset 20c

provides a mechanism to send MMIO writes as posted writes on the IOSFSB space

Bit Range	Default	Access	Field Name and Description
31:0	00h	RW	**Sideband Register Posted 3 (SBREGPOSTED3)** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 127-96.

Sideband Register Posted 4 (SBREGPOSTED4) – Offset 210

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space

Bit Range	Default	Access	Field Name and Description
31:0	00h	RW	**Sideband Register Posted 4 (SBREGPOSTED4)** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 159-128.

Sideband Register Posted 5 (SBREGPOSTED5) – Offset 214

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space

Bit Range	Default	Access	Field Name and Description
31:0	00h	RW	**Sideband Register Posted 5 (SBREGPOSTED5)** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 191-160.

Sideband Register Posted 6 (SBREGPOSTED6) – Offset 218

Sideband Register Posted 6 (SBREGPOSTED6) – Offset 218

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space

Bit Range	Default	Access	Field Name and Description
31:0	00h	RW	**Sideband Register Posted 6 (SBREGPOSTED6)** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 223-192.

Sideband Register Posted 7 (SBREGPOSTED7) – Offset 21c

Provides a mechanism to send MMIO writes as posted writes on the IOSFSB space

Bit Range	Default	Access	Field Name and Description
31:0	00h	RW	**Sideband Register Posted 7 (SBREGPOSTED7)** One hot masks for setting SBREG to posted posted for IOSF-SB endpoint IDs 255-224.

Endpoint Mask 0 (EPMASK0) – Offset 220

provide a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW/L	**Endpoint Mask 0 (EPMASK0)** One hot masks for disabling IOSF-SB endpoint IDs 31-0.

Endpoint Mask 1 (EPMASK1) – Offset 224

provide a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW/L	**Endpoint Mask 1 (EPMASK1)** One hot masks for disabling IOSF-SB endpoint IDs 63-32.

Endpoint Mask 2 (EPMASK2) – Offset 228

provide a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW/L	**Endpoint Mask 2 (EPMASK2)** One hot masks for disabling IOSF-SB endpoint IDs 95-64

Endpoint Mask 3 (EPMASK3) – Offset 22c

provide a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW/L	**Endpoint Mask 3 (EPMASK3)** One hot masks for disabling IOSF-SB endpoint IDs 127-96

Endpoint Mask 4 (EPMASK4) – Offset 230

provide a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW/L	**Endpoint Mask 4 (EPMASK4)** One hot masks for disabling IOSF-SB endpoint IDs 128-159

Endpoint Mask 5 (EPMASK5) – Offset 234

provide a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW/L	**Endpoint Mask 5 (EPMASK5)** One hot masks for disabling IOSF-SB endpoint IDs 191-160

Endpoint Mask 6 (EPMASK6) – Offset 238

provide a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW/L	**Endpoint Mask 6 (EPMASK6)** One hot masks for disabling IOSF-SB endpoint IDs 223-192

Endpoint Mask 7 (EPMASK7) – Offset 23c

provide a mechanism for disabling particular IOSF-SB endpoints from being allowed to targeted by transactions from the P2SB

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW/L	**Endpoint Mask 7 (EPMASK7)** One hot masks for disabling IOSF-SB endpoint IDs 255-224

PCI Express* Port Configuration Registers

There are up to sixteen sets of the following configuration registers used for PCH PCI Express* Port Configurations. Each PCH PCI Express* Configuration Register set covers a single PCI Express* Port and maps out as the following Device/Function:

D28/F0 = Port1

D28/F1 = Port2

D28/F2 = Port3

D28/F3 = Port4

D28/F4 = Port5

D28/F5 = Port6

D28/F6 = Port7

D28/F7 = Port8

D29/F0 = Port9

D29/F1 = Port10

D29/F2 = Port11

D29/F3 = Port12

D29/F4 = Port13

D29/F5 = Port14

D29/F6 = Port15

D29/F7 = Port16

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Identifiers (ID)	XXXX8086h
4h	4	Device Command; Primary Status (CMD_PSTS)	0h
8h	4	Revision ID;Class Code (RID_CC)	60400XXh
ch	4	Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)	810000h
18h	4	Bus Numbers; Secondary Latency Timer (BNUM_SLT)	0h
1ch	4	I/O Base and Limit; Secondary Status (IOBL_SSTS)	0h
20h	4	Memory Base and Limit (MBL)	0h
24h	4	Prefetchable Memory Base and Limit (PMBL)	10001h
28h	4	Prefetchable Memory Base Upper 32 Bits (PMBU32)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2ch	4	Prefetchable Memory Limit Upper 32 Bits (PMLU32)	0h
34h	4	Capabilities List Pointer (CAPP)	40h
3ch	4	Interrupt Information; Bridge Control (INTR_BCTRL)	0h
40h	4	Capabilities List; PCI Express Capabilities (CLIST_XCAP)	428010h
44h	4	Device Capabilities (DCAP)	8001h
48h	4	Device Control; Device Status (DCTL_DSTS)	100000h
4ch	4	Link Capabilities (LCAP)	710C00h
50h	4	Link Control; Link Status (LCTL_LSTS)	10000h
54h	4	Slot Capabilities (SLCAP)	40060h
58h	4	Slot Control; Slot Status (SLCTL_SLSTS)	0h
5ch	4	Root Control (RCTL)	0h
60h	4	Root Status (RSTS)	0h
64h	4	Device Capabilities 2 (DCAP2)	80837h
68h	4	Device Control 2; Device Status 2 (DCTL2_DSTS2)	0h
6ch	4	Link Capabilities 2 (LCAP2)	0h
70h	4	Link Control 2; Link Status 2 (LCTL2_LSTS2)	0h
80h	4	Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)	9005h
84h	4	Message Signaled Interrupt Message Address (MA)	0h
88h	4	Message Signaled Interrupt Message Data (MD)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
90h	4	Subsystem Vendor Capability (SVCAP)	A00Dh
94h	4	Subsystem Vendor IDs (SVID)	0h
a0h	4	Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)	C8030001h
a4h	4	PCI Power Management Control And Status (PMCS)	8h
d0h	4	Additional Configuration 1 (CCFG)	0h
d4h	4	Miscellaneous Port Configuration 2 (MPC2)	0h
d8h	4	Miscellaneous Port Configuration (MPC)	1110000h
dch	4	SMI / SCI Status (SMSCS)	0h
100h	4	Advanced Error Extended Reporting Capability Header (AECH)	0h
104h	4	Uncorrectable Error Status (UES)	0h
108h	4	Uncorrectable Error Mask (UEM)	0h
10ch	4	Uncorrectable Error Severity (UEV)	60011h
110h	4	Correctable Error Status (CES)	0h
114h	4	Correctable Error Mask (CEM)	2000h
118h	4	Advanced Error Capabilities and Control (AECC)	0h
12ch	4	Root Error Command (REC)	0h
130h	4	Root Error Status (RES)	0h
134h	4	Error Source Identification (ESID)	0h
144h	4	ACS Capability Register (ACSCAPR)	Fh
148h	4	ACS Control Register (ACSCTLR)	0h
200h	4	L1 Sub-States Extended Capability Header (L1SECH)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
204h	4	L1 Sub-States Capabilities (L1SCAP)	28281Fh
208h	4	L1 Sub-States Control 1 (L1SCTL1)	0h
20ch	4	L1 Sub-States Control 2 (L1SCTL2)	28h
220h	4	Secondary PCI Express Extended Capability Header (SPEECH)	0h
224h	4	Link Control 3 (LCTL3)	0h
22ch	4	Lane 0 and Lane 1 Equalization Control (L01EC)	7F7F7F7Fh
230h	4	Lane 2 and Lane 3 Equalization Control (L23EC)	7F7F7F7Fh
300h	4	PCI Express Replay Timer Policy 1 (PCIERTP1)	A64F96h
304h	4	PCI Express Replay Timer Policy 2 (PCIERTP2)	1BC00B86h
324h	4	PCI Express Configuration (PCIEDBG)	2000000h
338h	4	PCI Express Additional Link Control (PCIEALC)	0h
400h	4	Additional Configuration 2 (LTROVR)	0h
404h	4	Additional Configuration 3 (LTROVR2)	0h
418h	4	Thermal and Power Throttling (TNPT)	930h
420h	4	Additional Configuration 4 (PCIEPMECTL)	0h
450h	4	Equalization Configuration 1 (EQCFG1)	0h
454h	4	Remote Transmitter Preset/Coefficient List 1 (RTPCL1)	0h
458h	4	Remote Transmitter Preset/Coefficient List 2 (RTPCL2) (RTPCL2)	0h

Identifiers (ID) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:16	See Description	RO/V	**Device Identification (DID)** The value of this ID is product specific. Refer to the Device and Revision ID Table in Volume 1 for default value.
15:0	8086h	RO	**Vendor Identification (VID)** Indicates Intel

Device Command; Primary Status (CMD_PSTS) – Offset 4

Bit Range	Default	Access	Field Name and Description
30:11	-	-	**Reserved**
10	0b	RW/V2	**Interrupt Disable (ID)** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above.
9	0b	RO	**Fast Back to Back Enable (FBE)** Reserved per PCI-Express spec.
8	0b	RW	**SERR# Enable (SEE)** When set, enables the root port to generate an SERR# message when PSTS.SSE is set.
7	0b	RO	**Wait Cycle Control (WCC)** Reserved per PCI-Express spec.

Bit Range	Default	Access	Field Name and Description
6	0b	RW	**Parity Error Response Enable (PERE)** Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0b	RO	**VGA Palette Snoop (VGA_PSE)** Reserved per PCI-Express spec.
4	0b	RO	**Memory Write and Invalidate Enable (MWIE)** Reserved per PCI-Express spec.
3	0b	RO	**Special Cycle Enable (SCE)** Reserved per PCI-Express and PCI bridge spec.
2	0b	RW	**Bus Master Enable (BME)** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit.
1	0b	RW	**Memory Space Enable (MSE)** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone.
0	0b	RW	**I/O Space Enable (IOSE)** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone..

Revision ID;Class Code (RID_CC) – Offset 8

Bit Range	Default	Access	Field Name and Description
31:24	06h	RO	**Base Class Code (BCC)** Indicates the device is a bridge device.

Bit Range	Default	Access	Field Name and Description
23:16	04h	RO/V	**Sub-Class Code (SCC)** The default indicates the device is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1 for a Host Bridge, this register reads 00h.
15:8	00h	RO/V	**Programming Interface (PI)** The value reported in this register is a function of the Decode Control.Subtractive Decode Enable (SDE) register. SDE Value reported in this register 0: 00h 1: 01h
7:0	See Description	RO/V	**Revision ID (RID)** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE) – Offset c

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	1b	RO	**Multi-function Device (MFD)** This bit is '1 to indicate a multi-function device.
22:16	01h	RO/V	**Header Type (HTYPE)** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.BT register is set to a '1 for a Host Bridge, this register reads 00h.
15:11	00h	RO	**Latency Count (CT)** Reserved per PCI-Express spec
10:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**Line Size (LS)** This is read/write but contains no functionality, per PCI-Express spec

Bus Numbers; Secondary Latency Timer (BNUM_SLT) – Offset 18

Bit Range	Default	Access	Field Name and Description
31:24	00h	RW/V2	**Secodary Latency Timer (SLT)** For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is a RW register; else this register is RO and returns 0. This register does not affect the behavior of any HW logic.
23:16	00h	RW	**Subordinate Bus Number (SBBN)** Indicates the highest PCI bus number below the bridge.
15:8	00h	RW	**Secondary Bus Number (SCBN)** Indicates the bus number the port.
7:0	00h	RW	**Primary Bus Number (PBN)** Indicates the bus number of the backbone.

I/O Base and Limit; Secondary Status (IOBL_SSTS) – Offset 1c

Bit Range	Default	Access	Field Name and Description
31	0b	RW/1C/V	**Detected Parity Error (DPE)** Set when the port receives a poisoned TLP.
30	0b	RW/1C/V	**Received System Error (RSE)** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device.
29	0b	RW/1C/V	**Received Master Abort (RMA)** Set when the port receives a completion with DUnsupported Request status from the device.

Bit Range	Default	Access	Field Name and Description
28	0b	RW/1C/V	**Received Target Abort (RTA)** Set when the port receives a completion with DCompletion Abort status from the device.
27	0b	RW/1C/V	**Signaled Target Abort (STA)** Set when the port generates a completion with DCompletion Abort status to the device.
26:25	00b	RO/V	**Secondary DEVSEL# Timing Status (SDTS)** Reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b.
24	0b	RW/1C/V	**Data Parity Error Detected (DPD)** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side.
23	0b	RO/V	**Secondary Fast Back to Back Capable (SFBC)** Reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b.
22	-	-	**Reserved**
21	0b	RO	**Secondary 66 MHz Capable (SC66)** Reserved per PCI Express spec
20:16	-	-	**Reserved**
15:12	0h	RW	**I/O Address Limit (IOLA)** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	0h	RO	**I/O Limit Address Capability (IOLC)** Indicates that the bridge does not support 32-bit I/O addressing.

Bit Range	Default	Access	Field Name and Description
7:4	0h	RW	**I/O Base Address (IOBA)** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	0h	RO	**I/O Base Address Capability (IOBC)** Indicates that the bridge does not support 32-bit I/O addressing.

Memory Base and Limit (MBL) – Offset 20

Bit Range	Default	Access	Field Name and Description
31:20	000h	RW	**Memory Limit (ML)** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	-	-	**Reserved**
15:4	000h	RW	**Memory Base (MB)** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	-	-	**Reserved**

Prefetchable Memory Base and Limit (PMBL) – Offset 24

Bit Range	Default	Access	Field Name and Description
31:20	000h	RW	**Prefetchable Memory Limit (PML)** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	1h	RO	**64-bit Indicator (I64L)** Indicates support for 64-bit addressing.

Bit Range	Default	Access	Field Name and Description
15:4	000h	RW	**Prefetchable Memory Base (PMB)** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	1h	RO	**64-bit Indicator (I64B)** Indicates support for 64-bit addressing.

Prefetchable Memory Base Upper 32 Bits (PMBU32) – Offset 28

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Prefetchable Memory Base Upper Portion (PMBU)** Upper 32-bits of the prefetchable address base.

Prefetchable Memory Limit Upper 32 Bits (PMLU32) – Offset 2c

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Prefetchable Memory Limit Upper Portion (PMLU)** Upper 32-bits of the prefetchable address limit.

Capabilities List Pointer (CAPP) – Offset 34

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	40h	RW/O	**Capabilities Pointer (PTR)** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) OffsetCapability Next Pointer 40h PCI Express 80h 80h Message Signaled Interrupt (MSI) 90h 90h Subsystem Vendor A0h A0h PCI Power Management 00h Extended PCIe Capability Linked List OffsetCapability Next Pointer 100h Advanced Error Reporting 000h

Interrupt Information; Bridge Control (INTR_BCTRL) – Offset 3c

Bit Range	Default	Access	Field Name and Description
30:28	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
27	0b	RW/V2	**Discard Timer SERR# Enable (DTSE)** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
26	0b	RO	**Discard Timer Status (DTS)** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set.
25	0b	RW/V2	**Secondary Discard Timer (SDT)** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
24	0b	RW/V2	**Primary Discard Timer (PDT)** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
23	0b	RO	**Fast Back to Back Enable (FBE)** Reserved per Express spec.
22	0b	RW	**Secondary Bus Reset (SBR)** Triggers a Hot Reset on the PCI-Express port.
21	0b	RW/V2	**Master Abort Mode (MAM)** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
20	0b	RW	**VGA 16-Bit Decode (V16)** When set, indicates that the I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled. 0: Execute 10-bit address decode on VGA I/O accesses. 1: Execute 16-bit address decode on VGA I/O accesses.

Bit Range	Default	Access	Field Name and Description
19	0b	RW	**VGA Enable (VE)** When set, the following ranges will be claimed off the backbone by the root port: Memory ranges A0000h-BFFFFh I/O ranges 3B0h C 3BBh and 3C0h C 3DFh, and all aliases of bits 15:10 in any combination of 1s
18	0b	RW	**ISA Enable (IE)** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh).
17	0b	RW	**SERR# Enable (SE)** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not.
16	0b	RW	**Parity Error Response Enable (PERE)** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD.
15:8	00h	RO/V	**Interrupt Pin (IPIN)** Indicates the interrupt pin driven by the root port. 0000 0001 = INTA# 0000 0010 = INTB# 0000 0011 = INTC# 0000 0100 = INTD# Others = Reserved
7:0	00h	RW	**Interrupt Line (ILINE)** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

Capabilities List; PCI Express Capabilities (CLIST_XCAP) – Offset 40

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29:25	00h	RO	**Interrupt Message Number (IMN)** The root port does not have multiple MSI interrupt numbers.
24	0b	RW/O	**Slot Implemented (SI)** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
23:20	4h	RO	**Device / Port Type (DT)** Indicates this is a PCI-Express root port
19:16	2h	RO	**Capability Version (CV)** Version 2.0 indicates devices compliant to the PCI Express 2.0 specification which incorporates the Register Expansion ECN.
15:8	80h	RW/O	**Next Capability (NEXT)** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	10h	RO	**Capability ID (CID)** Indicates this is a PCI Express capability

Device Capabilities (DCAP) – Offset 44

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**
28	0b	RO	**Function Level Reset Capable (FLRC)** Not supported in Root Ports

Bit Range	Default	Access	Field Name and Description
27:26	00b	RO	**Captured Slot Power Limit Scale (CSPS)** Not supported
25:18	00h	RO	**Captured Slot Power Limit Value (CSPV)** Not supported
17:16	-	-	**Reserved**
15	1b	RO	**Role Based Error Reporting (RBER)** When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions.
14:12	-	-	**Reserved**
11:9	000b	RO	**Endpoint L1 Acceptable Latency (E1AL)** Reserved for root ports.
8:6	000b	RO	**Endpoint L0 Acceptable Latency (E0AL)** Reserved for Root port.
5	0b	RO	**Extended Tag Field Supported (ETFS)** The root port never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags.
4:3	00b	RO	**Phantom Functions Supported (PFS)** No phantom functions supported

Bit Range	Default	Access	Field Name and Description
2:0	001b	RW/O	**Max Payload Size Supported (MPS)** BIOS should write to this field during system initialization. Only Max Payload Size of up to 256B is supported. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface.

Device Control; Device Status (DCTL_DSTS) – Offset 48

Bit Range	Default	Access	Field Name and Description
30:22	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
21	0b	RO	**Transactions Pending (TDP)** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID.
20	1b	RO	**AUX Power Detected (APD)** The root port contains AUX power for wakeup
19	0b	RW/1C/V	**Unsupported Request Detected (URD)** Indicates an unsupported request was detected.
18	0b	RW/1C/V	**Fatal Error Detected (FED)** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed tlp
17	0b	RW/1C/V	**Non-Fatal Error Detected (NFED)** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned tlp, unexpected completions, unsupported requests, completor abort, or completer timeout
16	0b	RW/1C/V	**Correctable Error Detected (CED)** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, tlp crc error, dllp crc error, replay num rollover, replay timeout.
15	-	-	**Reserved**
14:12	000b	RO	**Max Read Request Size (MRRS)** Hardwired to 0. This field applies only to the PCIe link interface.
11	0b	RO	**Enable No Snoop (ENS)** Not supported. The root port will never issue non-snoop requests.
10	0b	RW/P	**Aux Power PM Enable (APME)** The OS will set this bit to '1 if the device connected has detected aux power.
9	0b	RO	**Phantom Functions Enable (PFE)** Not supported
8	0b	RO	**Extended Tag Field Enable (ETFE)** Not supported

Bit Range	Default	Access	Field Name and Description
7:5	000b	RW	**Max Payload Size (MPS)** The root port only supports up to 256B max payload. Programming this field to any values other than 128B or 256B max payload size will result in aliasing to 128B max payload size. If the DCAP.MPS indicates 128B max payload size support, programming this field to any values other than 128B will result in aliasing to 128B max payload size. Programming this field to any values greater than DCAP.MPS will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME.
4	0b	RO	**Enable Relaxed Ordering (ERO)** Not supported
3	0b	RW	**Unsupported Request Reporting Enable (URE)** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.

Bit Range	Default	Access	Field Name and Description
2	0b	RW	**Fatal Error Reporting Enable (FEE)** enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	0b	RW	**Non-Fatal Error Reporting Enable (NFE)** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	0b	RW	**Correctable Error Reporting Enable (CEE)** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

Link Capabilities (LCAP) – Offset 4c

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO/V	**Port Number (PN)** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h 4 04h
23	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
22	1b	RW/O	**ASPM Optionality Compliance (ASPMOC)** ASPM Optionality Compliance(ASPMOC): This bit must be set to 1b for PCIe 3.0 compliant port. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests.
21	1b	RO	**Link Bandwidth Notification Capability (LBNC)** This port supports Link Bandwidth Notification status and interrupt mechanisms.
20	1b	RO	**Link Active Reporting Capable (LARC)** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	0b	RO	**Surprise Down Error Reporting Capable (SDERC)** Set to '0 to indicate the root port does not support Surprise Down Error Reporting
18	0b	RO	**Clock Power Management (CPM)** '0 Indicates that root ports do not support the CLKREQ# mechanism.

Bit Range	Default	Access	Field Name and Description
17:15	010b	RW/O	**L1 Exit Latency (EL1)** Indicates an exit latency of 2us to 4us. 000b C Less than 1 us 001b C 1 us to less than 2 us 010b C 2 us to less than 4 us 011b C 4 us to less than 8 us 100b C 8 us to less than 16 us 101b C 16 us to less than 32 us 110b C 32 us to 64 us 111b C More than 64 us Note: If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency.
14:12	000b	RO/V	**L0s Exit Latency (EL0)** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL
11:10	11b	RW/O	**Active State Link PM Support (APMS)** Indicates the level of active state power management on this link Bits Definition 00 No ASPM Supported 01 L0s Supported 10 L1 Supported 11 L0s and L1 supported

Bit Range	Default	Access	Field Name and Description
9:4	000000b	RO/V	**Maximum Link Width (MLW)** For the root ports, several values can be taken, based upon the value of the chipset configuration register field RPC.PC1 for ports 1-4: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h
3:0	0h	RO/V	**Max Link Speeds (MLS)** Indicates the supported link speeds of the Root Port 0001b = 2.5 GT/s Link speed supported 0010b = 5.0 GT/s and 2.5GT/s Link speeds supported Max Link Speeds (MLS): This field indicates the maximum Link speed of the associated Port. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the maximum Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved.

Bit Range	Default	Access	Field Name and Description

Link Control; Link Status (LCTL_LSTS) – Offset 50

Bit Range	Default	Access	Field Name and Description
31	0b	RW/1C/V	**Link Autonomous Bandwidth Status (LABS)** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b.

Bit Range	Default	Access	Field Name and Description
30	0b	RW/1C/V	**Link Bandwidth Management Status (LBMS)** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b.
29	0b	RO/V	**Link Active (LA)** Set to 1b when the Data Link Control and Management State Machine is in the DL_ Active state, 0b otherwise.
28	0b	RO/V	**Slot Clock Configuration (SCC)** In normal mode, root port uses the same reference clock as on the platform and does not generate its own clock. Note: The default of this register bit is dependent on the DPCIe Non-Common Clock With SSC Mode Enable Strap. If the strap enables non-common clock with SSC support, this bit shall default to '0. Otherwise, this bit shall default to '1.
27	0b	RO/V	**Link Training (LT)** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training.
26	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
25:20	00h	RO/V	**Negotiated Link Width (NLW)** For the root ports, this register could take on several values: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h The value of this register is undefined if the link has not successfully trained.

Bit Range	Default	Access	Field Name and Description
19:16	1h	RO/V	**Current Link Speed (CLS)** 0001b Link is 2.5Gb/s Link 0010b 5.0 GT/s Link This field indicates the negotiated Link speed of the given link. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. The value of this field is undefined if the link is not up.
15:12	-	-	**Reserved**
11	0b	RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE)** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set.

Bit Range	Default	Access	Field Name and Description
10	0b	RW	**Link Bandwidth Management Interrupt Enable (LBMIE)** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b.
9	0b	RW	**Hardware Autonomous Width Disable (HAWD)** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Default value of this bit is 0b. Note: When operating as PCI Express, this bit defines the value of the Link Upconfigure Capability in TS2 Ordered Sets.
8	0b	RO	**Enable Clock Power Management (ECPM)** Reserved. Not supported on Root Ports.
7	0b	RW	**Extended Synch (ES)** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. Note: This functionality is not applicable for Mobile Express.
6	0b	RW	**Common Clock Configuration (CCC)** When set, indicates that the root port and device are operating with a distributed common reference clock.
5	0b	WO	**Retrain Link (RL)** When set, the root port will train its downstream link. This bit always returns '0 when read. Software uses LSTS.LT to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	0b	RW	**Link Disable (LD)** When set, the root port will disable the link by directing the LTSSM to the Disabled state.

Bit Range	Default	Access	Field Name and Description
3	0b	RW/O	**Read Completion Boundary Control (RCBC)** Indicates the read completion boundary is 64 bytes.
2	-	-	**Reserved**
1:0	00b	RW	**Active State Link PM Control (ASPM)** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used.

Slot Capabilities (SLCAP) – Offset 54

Bit Range	Default	Access	Field Name and Description
31:24	00h	RW/O	**Physical Slot Number (PSN__31_24)** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
23:19	00h	RW/O	**Physical Slot Number (PSN__23_19)** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
18	1b	RO	**No Command Completed Support (NCCS)** Set to '1 as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes.
17	0b	RO	**Electromechanical Interlock Present (EMIP)** Set to 0 to indicate that no electro-mechanical interlock is implemented.

Bit Range	Default	Access	Field Name and Description
16:15	00b	RW/O	**Slot Power Limit Scale (SLS)** specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:8	00h	RW/O	**Slot Power Limit Value (SLV__14_8)** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
7	0b	RW/O	**Slot Power Limit Value (SLV__7_7)** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	1b	RW/O	**Hot Plug Capable (HPC)** When set, Indicates that hot plug is supported.
5	1b	RW/O	**Hot Plug Surprise (HPS)** When set, indicates the device may be removed from the slot without prior notification.
4	0b	RO	**Power Indicator Present (PIP)** Indicates that a power indicator LED is not present for this slot.
3	0b	RO	**Attention Indicator Present (AIP)** Indicates that an attention indicator LED is not present for this slot.
2	0b	RO	**MRL Sensor Present (MSP)** Indicates that an MRL sensor is not present
1	0b	RO	**Power Controller Present (PCP)** Indicates that a power controller is not implemented for this slot
0	0b	RO	**Attention Button Present (ABP)** Indicates that an attention button is not implemented for this slot.

Slot Control; Slot Status (SLCTL_SLSTS) – Offset 58

Bit Range	Default	Access	Field Name and Description
30:25	-	-	**Reserved**
24	0b	RW/1C/V	**Data Link Layer State Changed (DLLSC)** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
23	0b	RO	**Electromechanical Interlock Status (EMIS)** Reserved as this port does not support and electromechanical interlock.
22	0b	RO/V	**Presence Detect State (PDS)** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected ('1) or empty ('0). If XCAP.SI is cleared, this bit is a '1.
21	0b	RO	**MRL Sensor State (MS)** Reserved as the MRL sensor is not implemented.
20	0b	RO	**Command Completed (CC)** This register is RO as this port does not implement a Hot Plug Controller..
19	0b	RW/1C/V	**Presence Detect Changed (PDC)** This bit is set by the root port when the SLSTS.PDS bit changes state.
18	0b	RO	**MRL Sensor Changed (MSC)** Reserved as the MRL sensor is not implemented.
17	0b	RO	**Power Fault Detected (PFD)** Reserved as a power controller is not implemented.
16	0b	RO	**Attention Button Pressed (ABP)** This register is RO as this port does not implement an attention button
15:13	-	-	**Reserved**
12	0b	RW	**Data Link Layer State Changed Enable (DLLSCE)** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed

Bit Range	Default	Access	Field Name and Description
11	0b	RO	**Electromechanical Interlock Control (EMIC)** Reserved as this port does not support an Electromechanical Interlock.
10	0b	RO	**Power Controller Control (PCC)** This bit has no meaning for module based hot plug.
9:8	00b	RO	**Power Indicator Control (PIC)** This register is RO as this port does not implement a Hot Plug Controller..
7:6	00b	RO	**Attention Indicator Control (AIC)** This register is RO as this port does not implement a Hot Plug Controller..
5	0b	RW	**Hot Plug Interrupt Enable (HPE)** When set, enables generation of a hot plug interrupt on enabled hot plug events.
4	0b	RO	**Command Completed Interrupt Enable (CCE)** This register is RO as this port does not implement a Hot Plug Controller..
3	0b	RW	**Presence Detect Changed Enable (PDE)** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state.
2	0b	RO	**MRL Sensor Changed Enable (MSE)** This register is RO as this port does not implement a Hot Plug Controller..
1	0b	RO	**Power Fault Detected Enable (PFE)** This register is RO as this port does not implement a Hot Plug Controller...
0	0b	RO	**Attention Button Pressed Enable (ABE)** This register is RO as this port does not implement a Hot Plug Controller..

Root Control (RCTL) – Offset 5c

Bit Range	Default	Access	Field Name and Description
30:4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3	0b	RW	**PME Interrupt Enable (PIE)** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0 to '1 transition, or due to this bit being set with RSTS.PS already set).
2	0b	RW	**System Error on Fatal Error Enable (SFE)** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set.
1	0b	RW	**System Error on Non-Fatal Error Enable (SNE)** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set.
0	0b	RW	**System Error on Correctable Error Enable (SCE)** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set.

Root Status (RSTS) – Offset 60

Bit Range	Default	Access	Field Name and Description
30:18	-	-	**Reserved**
17	0b	RO/V	**PME Pending (PP)** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. Root ports have a one deep PME pending queue.
16	0b	RW/1C/V	**PME Status (PS)** Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RO/V	**PME Requestor ID (RID)** Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set. Root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped.

Device Capabilities 2 (DCAP2) – Offset 64

Bit Range	Default	Access	Field Name and Description
30:20	-	-	**Reserved**
19:18	10b	RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS)** 00b - OBFF is not supported. 01b - OBFF is supported using Message signaling only. 10b - OBFF is supported using WAKE# signaling only. 11b - OBFF is supported using WAKE# and Message signaling. BIOS shall program this field to 00b since OBFF messaging is not supported.
17:12	-	-	**Reserved**
11	1b	RW/O	**LTR Mechanism Supported (LTRMS)** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1 or a '0 to enable/disable the root port from declaring support for the LTR capability.
10:6	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
5	1b	RO	**ARI Forwarding Supported (AFS)** ARI Forwarding Supported (AFS): Applicable only to Switch Downstream Ports and Root Ports; must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. Note: This bit is not made RWO to simplify implementation, since there is a requirement that the ARI Forwarding Enable bit must be hardwired to 0b if ARI Forwarding Supported bit is 0b. It is low risk to keep this risk 1b.
4	1b	RO	**Completion Timeout Disable Supported (CTDS)** A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	7h	RO	**Completion Timeout Ranges Supported (CTRS)** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A and B 0110b Ranges B and C 0111b Ranges A, B, and C (This is what the PCH supports) 1110b Ranges B, C and D 1111b Ranges A, B, C, and D All other values are reserved.

Device Control 2; Device Status 2 (DCTL2_DSTS2) – Offset 68

Bit Range	Default	Access	Field Name and Description
30:11	-	-	**Reserved**
10	0b	RW	**LTR Mechanism Enable (LTREN)** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect.
9:6	-	-	**Reserved**
5	0b	RW	**ARI Forwarding Enable (AFE)** ARI Forwarding Enable (AFE): When set, the Downstream Port disables its traditional Device Number field being 0b enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port.
4	0b	RW	**Completion Timeout Disable (CTD)** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.
3:0	0h	RW	**Completion Timeout Value (CTV)** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to

Bit Range	Default	Access	Field Name and Description
			0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. The root port targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50 s to 100 s) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either when this value was changed or when each request was issued.

Link Capabilities 2 (LCAP2) – Offset 6c

Bit Range	Default	Access	Field Name and Description
30:23	-	-	**Reserved**
22:16	00h	RO	**Lower SKP OS Reception Supported Speeds Vector (LSOSRSS)** Lower SKP OS Reception Supported Speeds Vector(LSOSRSS): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
15:9	00h	RO	**Lower SKP OS Generation Supported Speeds Vector (LSOSGSSV)** Lower SKP OS Generation Supported Speeds Vector(LSOSGSSV): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
8	0b	RO	**Crosslink Supported (CS)** Crosslink Supported (CS): No support for Crosslink.

Bit Range	Default	Access	Field Name and Description
7:1	0000000b	RO/V	**Supported Link Speeds Vector (SLSV)** Supported Link Speeds Vector (SLSV): This field indicates the supported Link speed of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. Bit definitions within this field are: Bit 0: 2.5 GT/s. Bit 1: 5.0 GT/s. Bit 2: 8.0 GT/s. Bits 6:3: Reserved. .
0	-	-	**Reserved**

Link Control 2; Link Status 2 (LCTL2_LSTS2) – Offset 70

Bit Range	Default	Access	Field Name and Description
30:22	-	-	**Reserved**
21	0b	RW/1C/V/P	**Link Equalization Request (LER)** Link Equalization Request (LER): This bit is set by hardware to request the Link equalization process to be performed on the Link. Register Attribute: Dynamic.
20	0b	RO/V/P	**Equalization Phase 3 Successful (EQP3S)** Equalization Phase 3 Successful (EQP3S): When set to 1, this bit indicates that Phase 3 of the Transmitter Equalization procedure has successfully completed.

Bit Range	Default	Access	Field Name and Description
19	0b	RO/V/P	**Equalization Phase 2 Successful (EQP2S)** Equalization Phase 2 Successful (EQP2S): When set to 1, this bit indicates that Phase 2 of the Transmitter Equalization procedure has successfully completed.
18	0b	RO/V/P	**Equalization Phase 1 Successful (EQP1S)** Equalization Phase 1 Successful (EQP1S): When set to 1, this bit indicates that Phase 1 of the Transmitter Equalization procedure has successfully completed.
17	0b	RO/V/P	**Equalization Complete (EqC)** Equalization Complete (EC): When set to 1, this bit indicates that the Transmitter Equalization procedure has completed
16	0b	RO/V	**Current De-emphasis Level (CDL)** When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed.

Bit Range	Default	Access	Field Name and Description
15:12	0000b	RW/P	**Compliance Preset/De-emphasis (CD)** For 8.0 GT/s Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. For 5.0 GT/s Data Rate: This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 0001b -3.5 dB 0000b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. The default value of this field is 0000b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value.
11	0b	RW/P	**Compliance SOS (CSOS)** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only.
10	0b	RW/P	**Enter Modified Compliance (EMC)** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.

Bit Range	Default	Access	Field Name and Description
9:7	000b	RW/P	**Transmit Margin (TM)** This field controls the value of the nondeemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see PCI Express Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the components Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.

Bit Range	Default	Access	Field Name and Description
6	0b	RW/P	**Selectable De-emphasis (SD)** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.
5	0b	RO	**Hardware Autonomous Speed Disable (HASD)** Reserved. This port cannot autonomously change speeds.
4	0b	RW/P	**Enter Compliance (EC)** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value.
3:0	0h	RW/V/P	

Bit Range	Default	Access	Field Name and Description
			Target Link Speed (TLS) Target Link Speed (TLS): This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. The encoded value specifies a bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. Defined encodings are: 0001b: Supported Link Speeds Vector field bit 0. 0010b: Supported Link Speeds Vector field bit 1. 0011b: Supported Link Speeds Vector field bit 2. 0100b: Supported Link Speeds Vector field bit 3. 0101b: Supported Link Speeds Vector field bit 4. 0110b: Supported Link Speeds Vector field bit 5. 0111b: Supported Link Speeds Vector field bit 6. All other encodings are reserved. If a value is written to this field that does not correspond to a supported speed, as indicated by the Supported Link Speeds Vector, the result is undefined. The default value of this field is GEN1. Note: This register field could be used by REUT software to limit the link speed to 2.5 GT/s or 5 GT/s data rate.

Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC) – Offset 80

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RO	**64-Bit Address Capable (C64)** Capable of generating a 32-bit message only.
22:20	000b	RW	**Multiple Message Enable (MME)** These bits are RW for software compatibility, but only one message is ever sent by the root port.
19:17	000b	RO	**Multiple Message Capable (MMC)** Only one message is required.
16	0b	RW	**MSI Enable (MSIE)** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.
15:8	90h	RW/O	**Next Pointer (NEXT)** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	05h	RO	**Capability ID (CID)** Capabilities ID indicates MSI.

Message Signaled Interrupt Message Address (MA) – Offset 84

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:2	0000000 0h	RW	**Address (ADDR)** Lower 32 bits of the system specified message address, always DW aligned.
1:0	-	-	**Reserved**

Message Signaled Interrupt Message Data (MD) – Offset 88

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0000h	RW	**Data (DATA)** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[15:0]) during the data phase of the MSI memory write transaction.

Subsystem Vendor Capability (SVCAP) – Offset 90

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:8	A0h	RW/O	**Next Capability (NEXT)** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	0Dh	RO	**Capability Identifier (CID)** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

Subsystem Vendor IDs (SVID) – Offset 94

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/O	**Subsystem Identifier (SID)** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	0000h	RW/O	**Subsystem Vendor Identifier (SVID)** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC) – Offset a0

Bit Range	Default	Access	Field Name and Description
31:27	11001b	RO	**PME Support (PMES)** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy Microsoft operating systems to enable PME# in devices connected behind this root port.
26	0b	RO	**D2_Support (D2S)** The D2 state is not supported.
25	0b	RO	**D1_Support (D1S)** The D1 state is not supported.
24:22	000b	RO	**Aux_Current (AC)** Reports 0mA (self-powered), as use of this controller does not add to suspect well power consumption.
21	0b	RO	**Device Specific Initialization (DSI)** Indicates that no device-specific initialization is required.
20	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
19	0b	RO	**PME Clock (PMEC)** Indicates that PCI clock is not required to generate PME#.
18:16	011b	RO	**Version (VS)** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h	RO	**Next Capability (NEXT)** Indicates this is the last item in the list.
7:0	01h	RO	**Capability Identifier (CID)** Value of 01h indicates this is a PCI power management capability.

PCI Power Management Control And Status (PMCS) – Offset a4

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO	**Data (DTA)** Reserved
23	0b	RO	**Bus Power / Clock Control Enable (BPCE)** Reserved per PCI Express specification
22	0b	RO	**B2/B3 Support (B23S)** Reserved per PCI Express specification.
21:16	-	-	**Reserved**
15	0b	RO	**PME Status (PMES)** Indicates a PME was received on the downstream link.
14:13	00b	RO	**Data Scale (DSC)** Reserved
12:9	0h	RO	**Data Select (DSEL)** Reserved

Bit Range	Default	Access	Field Name and Description
8	0b	RW/P	**PME Enable (PMEE)** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy Microsoft operating systems to enable PME# on devices connected to this root port.
7:4	-	-	**Reserved**
3	1b	RW/O	**No Soft Reset (NSR)** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	-	-	**Reserved**
1:0	00b	RW	**Power State (PS)** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 C D0 state 11 C D3HOT state When in the D3HOT state, the controllers configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10 or '01 to these bits, the write will be ignored.

Additional Configuration 1 (CCFG) – Offset d0

BIOS may need to program this register.

Miscellaneous Port Configuration 2 (MPC2) – Offset d4

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4	0b	RW	**ASPM Control Override Enable (ASPMCOEN)** When set to '1', the PCIe Root Port will use the values in the ASPM Control Override registers instead of ASPM Registers in the Link Control register. This register allows BIOS to control the DMI ASPM settings instead of the OS.
3:2	00b	RW	**ASPM Control Override (ASPMCO)** Provides BIOS control of whether root port should enter L0s or L1 or both. 00 = Disabled 01 = L0s Entry Enabled 10 = L1 Entry Enabled 11 = L0s and L1 Entry Enabled.
1	0b	RW	**EOI Forwarding Disable (EOIFD)** 0 = Broadcast EOI messages that are sent on the backbone are claimed by this port and forwarded across the PCIe* link.{br]1 = Broadcast EOI messages are not claimed on the backbone by this port and will not be forwarded across the PCIe* Link.
0	0b	RW	**L1 Completion Timeout Mode (L1CTM)** 0 = PCI Express* Specification Compliant. Completion timeout is disabled during software initiated L1, and enabled during ASPM initiate L1. 1 = Completion timeout is enabled during L1, regardless of how L1 entry was initiated.

Miscellaneous Port Configuration (MPC) – Offset d8

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31	0b	RW	**Power Management SCI Enable (PMCE)** 0 = SCI generation based on a power management event is disabled. 1 = Enables the root port to generate SCI whenever a power management event is detected.
30	0b	RW	**Hot Plug SCI Enable (HPCE)** 0 = SCI generation based on a hot-plug event is disabled. 1 = Enables the root port to generate SCI whenever a hot-plug event is detected.
29	0b	RW/L	**Link Hold Off (LHO)** When set, the port will not take any TLP. This is used during loopback mode to fill up the downstream queue.
28	0b	RW/L	**Address Translater Enable (ATE)** Used to enable address translation via the AT bits in this register during loopback mode. 0: Disable 1: Enable
27	-	-	**Reserved**
26	0b	RW/L	**Port8xh Decode Enable (P8XDE)** When set, allows PCIe Root Port to claim I/O cycles within the range from 80h - 8Fh inclusive and forwarding the cycle to the link. The claiming of these cycles are independent of I/O Base/Limit and IO Space Enable bits. BIOS must ensure that at any one time, no more than one PCIe Root Port are enabled to claim Port 8xh cycles.
25	0b	RW/L	**Invalid Receive Range Check Enable (IRRCE)** When set, the receive transaction layer will treat the TLP as an Unsupported Request error if the address range of a Memory request does not fall outside the range between prefetchable and non-prefetchable base and limit. Messages, IO, Config, and Completions are never checked for valid address ranges This register bit is Read-Only when the MPC.SRL bit is set.

Bit Range	Default	Access	Field Name and Description
24	1b	RW/L	**BME Receive Check Enable (BMERCE)** When set, the receive transaction layer will treat the TLP as an Unsupported Request error if a memory or I/O read or write request is received and the Bus Master Enable bit is not set. Messages, Config, and Completions are never checked for BME.
23	0b	RW/O	**Secured Register Lock (SRL)** When this bit is set, all the secured registers will be locked and will be Read-Only.
22	0b	RW/L	**Detect Override (FORCEDET)** 0: Normal operation. Detect output from AFE is sampled for presence detection. 1: Override mode. Ignores AFE detect output and Link Training proceeds as if a device were detected.
21	0b	RW	**Flow Control During L1 Entry (FCDL1E)** br]0: No flow control update DLLPs sent during L1 Ack transmission 1: Flow control update DLLPs sent during L1 Ack transmission as required to meet the 30us periodic flow control update.
20:18	100b	RW	**Unique Clock Exit Latency (UCEL)** This value represents the L0s Exit Latency for unique-clock configurations (LCTL.CCC = '0). It defaults to 512ns to less than 1s, but may be overridden by BIOS.
17:15	010b	RW	**Common Clock Exit Latency (CCEL)** This value represents the L0s Exit Latency for common-clock configurations (LCTL.CCC = '1). It defaults to 128ns to less than 256ns, but may be overridden by BIOS.

Bit Range	Default	Access	Field Name and Description
14:13	00b	RW	**PCIe MEx Speed Disable (PCIEMEXSD)** When operating as PCI Express: 00: PCIe supported data rate is as defined by the Supported Link Speed and Target Link Speed register. 01: PCIe supported data rate is limited to just 2.5 GT/s. Supported Link Speed field will reflect 0000001b. Max Link Speed field will reflect 0001b. 10: PCIe supported data rate is limited to 2.5 GT/s and 5.0 GT/s. Supported Link Speed register will reflect 0000011b. Max Link Speed field will reflect 0010b. 11: Reserved. When operating as Mobile Express: 00: MEx supported data rate is as defined by the Supported Link Speed and Target Link Speed register. 01: MEx supported data rate is limited to just HS-G1. Supported Link Speed field will reflect 0000001b. Max Link Speed field will reflect 0000b. 10: PCIe supported data rate is limited to HS-G1 and HS-G2. Supported Link Speed register will reflect 0000001b. Max Link Speed field will reflect 0000b. 11: Reserved. When this bit is changed, link retrain needs to be performed for the change to be effective.
12:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7	0b	RW	**Port I/OxApic Enable (PAE)** When set, a range is opened through the bridge for the following memory addresses: Port# Address 1 FEC1_0000h - FEC1_7FFFh 2 FEC1_8000h - FEC1_FFFFh 3 FEC2_0000h - FEC2_7FFFh 4 FEC2_8000h - FEC2_FFFFh 5 FEC3_0000h - FEC3_7FFFh 6 FEC3_8000h - FEC3_FFFFh 7 FEC4_0000h - FEC4_7FFFh 8 FEC4_8000h - FEC4_FFFFh When cleared, the hole is disabled.
6:3	-	-	**Reserved**
2	0b	RW/O	**Bridge Type (BT)** This register can be used to modify the Base Class and Header Type fields from the default PCI-to-PCI bridge to a Host Bridge. Having the root port appear as a Host Bridge is useful in some server configurations. 0 = The root port bridge type is a PCI-to-PCI Bridge, Header Sub-Class = 04h, and Header Type = Type 1. 1 = The root port bridge type is a PCI-to-PCI Bridge, Header Sub-Class = 00h, and Header Type = Type 0.
1	0b	RW	**Hot Plug SMI Enable (HPME)** 0 = SMI generation based on a hot-plug event is disabled. 1 = Enables the root port to generate SMI whenever a hot-plug event is detected.
0	0b	RW	**Power Management SMI Enable (PMME)** 0 = SMI generation based on a power management event is disabled. 1 = Enables the root port to generate SMI whenever a power management event is detected.

SMI / SCI Status (SMSCS) – Offset dc

Bit Range	Default	Access	Field Name and Description
31	0b	RW/1C/V	**Power Management SCI Status (PMCS)** This bit is set if the root port PME control logic needs to generate an interrupt, and this interrupt has been routed to generate an SCI.
30	0b	RW/1C/V	**Hot Plug SCI Status (HPCS)** This bit is set if the hot plug controller needs to generate an interrupt, and has this interrupt been routed to generate an SCI.
29:5	-	-	**Reserved**
4	0b	RW/1C/V	**Hot Plug Link Active State Changed SMI Status (HPLAS)** This bit is set when SLSTS.DLLSC transitions from '0' to '1', and MPC.HPME is set. When this bit is set, an SMI# will be generated.
3:2	-	-	**Reserved**
1	0b	RW/1C/V	**Hot Plug Presence Detect SMI Status (HPPDM)** This bit is set when SLSTS.PDC transitions from '0' to'1', and MPC.HPME is set. When this bit is set, an SMI# will be generated.
0	0b	RW/1C/V	**Power Management SMI Status (PMMS)** This bit is set when RSTS.PS transitions from '0' to'1', and MPC.PMME is set.

Advanced Error Extended Reporting Capability Header (AECH) – Offset 100

The AER capability can optionally be included or excluded from the capabilities list. The full AER is supported.

Bit Range	Default	Access	Field Name and Description
31:20	000h	RW/O	**Next Capability Offset (NCO)** Set to 000h as this is the last capability in the list.

Bit Range	Default	Access	Field Name and Description
19:16	0h	RW/O	**Capability Version (CV)** For systems that support AER, BIOS should write a 1h to this register else it should write 0
15:0	0000h	RW/O	**Capability ID (CID)** For systems that support AER, BIOS should write a 0001h to this register else it should write 0

Uncorrectable Error Status (UES) – Offset 104

This register must maintain its state through a platform reset. It loses its state upon loss of core power.

Bit Range	Default	Access	Field Name and Description
30:22	-	-	**Reserved**
21	0b	RW/1C/V/P	**ACS Violation Status (AVS)** Indicates an ACS Violation is logged
20	0b	RW/1C/V/P	**Unsupported Request Error Status (URE)** Indicates an unsupported request was received.
19	0b	RO	**ECRC Error Status (EE)** ECRC is not supported.
18	0b	RW/1C/V/P	**Malformed TLP Status (MT)** Indicates a malformed TLP was received.
17	0b	RW/1C/V/P	**Receiver Overflow Status (RO)** Indicates a receiver overflow occurred.
16	0b	RW/1C/V/P	**Unexpected Completion Status (UC)** Indicates an unexpected completion was received.
15	0b	RW/1C/V/P	**Completor Abort Status (CA)** Indicates a completer abort was received

Bit Range	Default	Access	Field Name and Description
14	0b	RW/1C/V/P	**Completion Timeout Status (CT)** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value
13	0b	RO	**Flow Control Protocol Error Status (FCPE)** Not supported.
12	0b	RW/1C/V/P	**Poisoned TLP Status (PT)** Indicates a poisoned TLP was received.
11:6	-	-	**Reserved**
5	0b	RO	**Surprise Down Error Status (SDE)** Surprise Down is not supported.
4	0b	RW/1C/V/P	**Data Link Protocol Error Status (DLPE)** Indicates a data link protocol error occurred.
3:1	-	-	**Reserved**
0	0b	RO	**Training Error Status (TE)** Not supported.

Uncorrectable Error Mask (UEM) – Offset 108

When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Bit Range	Default	Access	Field Name and Description
30:22	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
21	0b	RW/P	**ACS Violation Mask (AVM)** Mask for ACS Violation errors
20	0b	RW/P	**Unsupported Request Error Mask (URE)** Mask for uncorrectable errors.
19	0b	RO	**ECRC Error Mask (EE)** ECRC is not supported.
18	0b	RW/P	**Malformed TLP Mask (MT)** Mask for malformed TLPs
17	0b	RW/P	**Receiver Overflow Mask (RO)** Mask for receiver overflows.
16	0b	RW/P	**Unexpected Completion Mask (UC)** Mask for unexpected completions.
15	0b	RW/P	**Completor Abort Mask (CM)** Mask for completer abort.
14	0b	RW/P	**Completion Timeout Mask (CT)** Mask for completion timeouts.
13	0b	RO	**Flow Control Protocol Error Mask (FCPE)** Not supported.
12	0b	RW/P	**Poisoned TLP Mask (PT)** Mask for poisoned TLPs.
11:6	-	-	**Reserved**
5	0b	RO	**Surprise Down Error Mask (SDE)** Surprise Down is not supported.
4	0b	RW/P	**Data Link Protocol Error Mask (DLPE)** Mask for data link protocol errors.
3:1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	0b	RO	**Training Error Mask (TE)** Not supported.

Uncorrectable Error Severity (UEV) – Offset 10c

This register gives the option to make an uncorrectable error fatal or non-fatal. An error is fatal if the bit is set. An error is non-fatal if the bit is cleared. This register is only reset by a loss of core power.

Bit Range	Default	Access	Field Name and Description
30:22	-	-	**Reserved**
21	0b	RW/P	**ACS Violation Severity (AVS)** Severity for ACS violation.
20	0b	RW/P	**Unsupported Request Error Severity (URE)** Severity for unsupported request reception.
19	0b	RO	**ECRC Error Severity (EE)** ECRC is not supported.
18	1b	RW/P	**Malformed TLP Severity (MT)** Severity for malformed TLP reception.
17	1b	RW/P	**Receiver Overflow Severity (RO)** Severity for receiver overflow occurrences.
16	0b	RW/P	**Unexpected Completion Severity (UC)** Severity for unexpected completion reception.
15	0b	RW/P	**Completor Abort Severity (CA)** Severity for completer abort.
14	0b	RW/P	**Completion Timeout Severity (CT)** Severity for completion timeout.
13	0b	RO	**Flow Control Protocol Error Severity (FCPE)** Not supported.

Bit Range	Default	Access	Field Name and Description
12	0b	RW/P	**Poisoned TLP Severity (PT)** Severity for poisoned TLP reception.
11:6	-	-	**Reserved**
5	0b	RO	**Surprise Down Error Severity (SDE)** Surprise Down is not supported.
4	1b	RW/P	**Data Link Protocol Error Severity (DLPE)** Severity for data link protocol errors.
3:1	-	-	**Reserved**
0	1b	RO	**Training Error Severity (TE)** TE not supported. This bit is left as RO=1 for ease of implementation..

Correctable Error Status (CES) – Offset 110

This register is only reset by a loss of core power

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13	0b	RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES)** When set, indicates that an Advisory Non-Fatal Error occurred.
12	0b	RW/1C/V/P	**Replay Timer Timeout Status (RTT)** Indicates the replay timer timed out.
11:9	-	-	**Reserved**
8	0b	RW/1C/V/P	**Replay Number Rollover Status (RNR)** Indicates the replay number rolled over.

Bit Range	Default	Access	Field Name and Description
7	0b	RW/1C/V/P	**Bad DLLP Status (BD)** Indicates a bad DLLP was received.
6	0b	RW/1C/V/P	**Bad TLP Status (BT)** Indicates a bad TLP was received.
5:1	-	-	**Reserved**
0	0b	RW/1C/V/P	**Receiver Error Status (RE)** Indicates a receiver error occurred.

Correctable Error Mask (CEM) – Offset 114

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13	1b	RW/P	**Advisory Non-Fatal Error Mask (ANFEM)** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0b	RW/P	**Replay Timer Timeout Mask (RTT)** Mask for replay timer timeout.
11:9	-	-	**Reserved**
8	0b	RW/P	**Replay Number Rollover Mask (RNR)** Mask for replay number rollover.
7	0b	RW/P	**Bad DLLP Mask (BD)** Mask for bad DLLP reception.

Bit Range	Default	Access	Field Name and Description
6	0b	RW/P	**Bad TLP Mask (BT)** Mask for bad TLP reception.
5:1	-	-	**Reserved**
0	0b	RW/P	**Receiver Error Mask (RE)** Mask for receiver errors.

Advanced Error Capabilities and Control (AECC) – Offset 118

This register is only reset by a loss of core power.

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0b	RO	**ECRC Check Enable (ECE)** ECRC is not supported.
7	0b	RO	**ECRC Check Capable (ECC)** ECRC is not supported.
6	0b	RO	**ECRC Generation Enable (EGE)** ECRC is not supported.
5	0b	RO	**ECRC Generation Capabile (EGC)** ECRC is not supported.
4:0	00000b	RO/V/P	**First Error Pointer (FEP)** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register.

Root Error Command (REC) – Offset 12c

This register allows errors to generate interrupts.

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**
2	0b	RW	**Fatal Error Reporting Enable (FERE)** When set, the root port will generate an interrupt when a fatal error is reported by the attached device.
1	0b	RW	**Non-fatal Error Reporting Enable (NERE)** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device.
0	0b	RW	**Correctable Error Reporting Enable (CERE)** When set, the root port will generate an interrupt when a correctable error is reported by the attached device.

Root Error Status (RES) – Offset 130

This register can track more than one error and set the Dmultiple bits if a second or subsequent error occurs and the first has not been serviced. This register is only reset by a loss of core power.

Bit Range	Default	Access	Field Name and Description
31:27	00h	RO	**Advanced Error Interrupt Message Number (AEMN)** Reserved. There is only one error interrupt allocated.
26:7	-	-	**Reserved**
6	0b	RW/1C/V/P	**Fatal Error Message Received (FEMR)** Set when one or more Fatal Uncorrectable Error Messages have been received.
5	0b	RW/1C/V/P	**Non-Fatal Error Messages Received (NFEMR)** Set when one or more Non-Fatal Uncorrectable error messages have been received
4	0b	RW/1C/V/P	**First Uncorrectable Fatal (FUF)** Set when the first Uncorrectable Error message received is for a fatal error.
3	0b	RW/1C/V/P	**Multiple ERR_FATAL/NONFATAL Received (MENR)** Set when either a fatal or a non-fatal error is received and the ENR bit is already set.

Bit Range	Default	Access	Field Name and Description
2	0b	RW/1C/V/P	**ERR_FATAL/NONFATAL Received (ENR)** Set when either a fatal or a non-fatal error message is received.
1	0b	RW/1C/V/P	**Multiple ERR_COR Received (MCR)** Set when a correctable error message is received and the CR bit is already set.
0	0b	RW/1C/V/P	**ERR_COR Received (CR)** Set when a correctable error message is received.

Error Source Identification (ESID) – Offset 134

Identifies the source (Requester ID) of the first correctable and uncorrectable (Non-Fatal / Fatal) errors reported in the Root Error Status register. This register is only reset by a loss of core power.

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID)** Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message with the ERR_FATAL/NONFATAL Received register is not already set.
15:0	0000h	RO/V/P	**ERR_COR Source Identification (ECSID)** Loaded with the Requester ID indicated in the received ERR_COR Message with the ERR_COR Received register is not already set.

ACS Capability Register (ACSCAPR) – Offset 144

Bit Range	Default	Access	Field Name and Description
30:7	-	-	**Reserved**
6	0b	RO	**ACS Direct Translated P2P (T)** ACS Direct Translated P2P (T): ACS Direct Translated P2P is not supported.

Bit Range	Default	Access	Field Name and Description
5	0b	RO	**ACS P2P Egress Control (E)** ACS P2P Egress Control (E): ACS P2P Egress Control is not supported.
4	0b	RO	**ACS Upstream Forwarding (U)** ACS Upstream Forwarding (U): ACS Upstream Forwarding is not supported.
3	1b	RW/O	**ACS P2P Completion Redirect (C)** ACS P2P Completion Redirect (C): Required for all Functions that support ACS P2P Request Redirect; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Completion Redirect.
2	1b	RW/O	**ACS P2P Request Redirect (R)** ACS P2P Request Redirect (R): Required for Root Ports that support peer-to-peer traffic with other Root Ports; required for Switch Downstream Ports; required for multi-function device Functions that support peer-to-peer traffic with other Functions; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Request Redirect.
1	1b	RW/O	**ACS Translation Blocking (B)** ACS Translation Blocking (B): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Translation Blocking.
0	1b	RW/O	**ACS Source Validation (V)** ACS Source Validation (V): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Source Validation.

ACS Control Register (ACSCTLR) – Offset 148

Bit Range	Default	Access	Field Name and Description
30:7	-	-	**Reserved**
6	0b	RO	**ACS Direct Translated P2P Enable (T)** ACS Direct Translated P2P Enable (T): ACS Direct Translated P2P is not supported.

Bit Range	Default	Access	Field Name and Description
5	0b	RO	**ACS P2P Egress Control Enable (E)** ACS P2P Egress Control Enable (E): ACS P2P Egress Control is not supported.
4	0b	RO	**ACS Upstream Forwarding Enable (U)** ACS Upstream Forwarding Enable (U): ACS Upstream Forwarding is not supported.
3	0b	RW	**ACS P2P Completion Redirect (C)** ACS P2P Completion Redirect (C): Determines when the component redirects peer-to-peer Completions upstream; applicable only to Read Completions whose Relaxed Ordering Attribute is clear.
2	0b	RW	**ACS P2P Request Redirect (R)** ACS P2P Request Redirect (R): Determines when the component redirects peer-to-peer memory Requests targeting another peer port upstream. I/O, Configuration, VDM Messages and Completions are never affected by ACS P2P Request Redirect.
1	0b	RW	**ACS Translation Blocking (B)** ACS Translation Blocking (B): When set, the component blocks all upstream Memory Requests whose Address Translation (AT) field is not set to the default value. I/O, Configuration, Completions and Messages are never affected by ACS Translation Blocking.
0	0b	RW	**ACS Source Validation (V)** ACS Source Validation (V): When set, the component validates the Bus Number from the Requester ID of upstream Requests against the secondary / subordinate Bus Numbers. I/O, Configuration and Completions are never affected by ACS Source Validation.

L1 Sub-States Extended Capability Header (L1SECH) – Offset 200

Note: When operating in Mobile Express mode, this capability should not be enabled.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:20	000h	RW/O	**Next Capability Offset (NCO)** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h	RW/O	**Capability Version (CV)** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 1h
15:0	0000h	RW/O	**PCI Express Extended Capability ID (PCIEEC)** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 001Eh. .

L1 Sub-States Capabilities (L1SCAP) – Offset 204

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
23:19	00101b	RW/O	**Port Tpower_on Value (PTV)** Along with the Port T_POWER_ON Scale Field in the L1 Substates Capabilities register sets theTime (in us) that this Port requires the port on the opposite side of Link to wait in L1.OFF_EXIT after sampling CLKREQ# asserted before actively driving the interface. Port Tpower_on is calculated by multiplying the value in this field by the value in the Port Tpower_on scale field in the L1 Sub-States Capabilities 2 register. Required for all Ports that support L1.OFF.
18	-	-	**Reserved**
17:16	00b	RW/O	**Port Tpower_on Scale (PTPOS)** Specifies the scale used for Tpower_on value field in the L1 Substates Capabilities register. D00b: 2 us D01b: 10 us D10b: 100 us D11b: Reserved Required for all Ports that support L1.OFF.
15:8	28h	RW/O	**Port Common Mode Restore Time (PCMRT)** This is the time (in us) required for this Port to re-establish common mode. Required for all ports that support L1.OFF.
7:5	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
4	1b	RW/O	**L1 PM Substates Supported (L1PSS)** When Set this bit indicates that this Port supports L1 PM Substates. For compatibility with possible future extensions, software must not enable L1 PM Substates unless this bit is set. This RWO field must be programmed prior to enabling ASPM.
3	1b	RW/O	**ASPM L1.1 Substates Supported (AL11S)** When set, this bit indicates that this port supports L1 substates for ASPM L1.SNOOZ. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
2	1b	RW/O	**ASPM L1.2 Supported (AL12S)** When set, this bit indicates that ASPM_L1.OFF is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
1	1b	RW/O	**PCI-PM L1.1 Supported (PPL11S)** When set, this bit indicates that L1.SNOOZ sub-state is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
0	1b	RW/O	**PCI-PM L1.2 Supported (PPL12S)** When set, this bit indicates that L1.OFF power management feature is supported. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static

L1 Sub-States Control 1 (L1SCTL1) – Offset 208

Bit Range	Default	Access	Field Name and Description
31:29	000b	RW	**L1.2 LTR Threshold Latency ScaleValue (L12LTRTLSV)** This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular PCIe root port. The value in this field, together with L12LTRTLV is compared against both the snoop and non-snoop LTR values of the device. 000: L12LTRSTLV times 1 ns 001: L12LTRSTLV times 32 ns 010: L12LTRSTLV times 1024 ns 011: L12LTRSTLV times 32768 ns 100: L12LTRSTLV times 1048576 ns 101: L12LTRSTLV times 33554432 ns Others: Not Permitted. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
28:26	-	-	**Reserved**
25:16	0000000000b	RW	**L1.2 LTR Threshold Latency Value (L12OFFLTRTLV)** This field contains the L1.2 LTR Threshold Latency Value for this particular PCIe root port. The value in this field, together with L12LTRTLSV is compared against both the snoop and non-snoop LTR values of the device. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static

Bit Range	Default	Access	Field Name and Description
15:8	00h	RW	**Common Mode Restore Time (CMRT)** This is the Tcommon_mode time the PCIe root port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
7:4	-	-	**Reserved**
3	0b	RW	**ASPM L1.1 Enabled (AL11E)** When set, this bit indicates that ASPM L1.SNOOZ substates are enabled for ASPM. Required for both upstream and downstream ports. Register Attribute: Dynamic
2	0b	RW	**ASPM L1.2 Enable (AL12E)** When set, this bit indicates that ASPM L1.OFF substates are enabled for PCI-PM. Required for both upstream and downstream ports. Register Attribute: Dynamic
1	0b	RW	**PCI-PM L1.SNOOZ Enable (PPL11E)** When set, this bit indicates that PCI-PM L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled. This field must be programmed prior to enabling ASPM L1. Register Attribute: Dynamic
0	0b	RW	**PCI-PM L1.2 Enabled (PPL12E)** When set, this bit indicates that PCI-PM L1.OFF power management feature is enabled. L1.OFF can only be enabled if the platform supports bi-directional CLKREQPLUS#. This field must be programmed prior to enabling ASPM L1. Ports that support L1.OFF shall support Latency Tolerance Reporting. Register Attribute: Dynamic

L1 Sub-States Control 2 (L1SCTL2) – Offset 20c

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:3	00101b	RW	**Power On Wait Time (POWT)** Along with the Tpower_on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# is sampled asserts in L1.OFF state. Tpower_on value is calculated by multiplying the value in this field by the value in the TPOS field. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
2	-	-	**Reserved**
1:0	00b	RW	**Tpower_on Scale (TPOS)** Specifies the scale used for Tpower_on value. D00b: 2 us D01b: 10 us D10b: 100us D11b: Reserved. Required for all Ports that support L1.OFF. Register Attribute: Static

Secondary PCI Express Extended Capability Header (SPEECH) – Offset 220

Note: When operating in Mobile Express mode, this capability should not be enabled.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:20	000h	RW/O	**Next Capability Offset (NCO)** Next Capability Offset (NCO): This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h	RW/O	**Capability Version (CV)** Capability Version (CV): This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 1h to this register else it should write 0
15:0	0000h	RW/O	**PCI Express Extended Capability ID (PCIEECID)** PCI Express Extended Capability ID (PCIEECID): This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 0019h to this register else it should write 0.

Link Control 3 (LCTL3) – Offset 224

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
15:9	0000000b	RO	**Enable Lower SKP OS Generation Vector (ELSOSGV)** Enable Lower SKP OS Generation Vector(ELSOSGV): When the Link is in L0 and the bit in this field corresponding to the current Link speed is Set, SKP Ordered Sets are scheduled at the rate defined for SRNS, overriding the rate required based on the clock tolerance architecture. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is Set in this field and the corresponding bit in the Lower SKP OS Generation Supported Speeds Vector is not set.
8:2	-	-	**Reserved**
1	0b	RW	**Link Equalization Request Interrupt Enable (LERIE)** Link Equalization Request Interrupt Enable (LERIE): When set, this bit enables the generation of an interrupt to indicate that the Link Equalization Request bit has been set.
0	0b	RW	**Perform Equalization (PE)** Perform Equalization (PE): When this bit is 1b and Link Retrain bit is set with the Target Link Speed field set to 8 GT/s, the Downstream Port must perform Link Equalization. This bit is cleared by Root Port upon entry to Link Equalization

Lane 0 and Lane 1 Equalization Control (L01EC) – Offset 22c

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.

Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Bit Range	Default	Access	Field Name and Description
30:28	111b	RW	**Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH)** Upstream Port Lane 1 Receiver Preset Hint (UPL1RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
27:24	Fh	RW	**Upstream Port Lane 1 Transmitter Preset (UPL1TP)** Upstream Port Lane 1 Transmitter Preset (UPL1TP): Field contains the Transmit Preset value sent or received during Link Equalization.
23	-	-	**Reserved**
22:20	111b	RW	**Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH)** Downstream Port Lane 1 Receiver Preset Hint (DPL1RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh	RW	**Downstream Port Lane 1 Transmitter Preset (DPL1TP)** Downstream Port Lane 1 Transmitter Preset (DPL1TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	-	-	**Reserved**
14:12	111b	RW	**Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH)** Upstream Port Lane 0 Receiver Preset Hint (UPL0RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh	RW	**Upstream Port Lane 0 Transmitter Preset (UPL0TP)** Upstream Port Lane 0 Transmitter Preset (UPL0TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	-	-	**Reserved**
6:4	111b	RW	**Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH)** Downstream Port Lane 0 Receiver Preset Hint (DPL0RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.

Bit Range	Default	Access	Field Name and Description
3:0	Fh	RW	**Downstream Port Lane 0 Transmitter Preset (DPL0TP)** Downstream Port Lane 0 Transmitter Preset (DPL0TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

Lane 2 and Lane 3 Equalization Control (L23EC) – Offset 230

Each entry contains the values for the Lane with the corresponding default Lane number which is invariant to Link width and Lane reversal negotiation that occurs during Link training.

Based on the Port Configuration setting, if the maximum link width of the port is less than x4, the upper lane status bits should be ignored

Bit Range	Default	Access	Field Name and Description
30:28	111b	RW	**Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH)** Upstream Port Lane 3 Receiver Preset Hint (UPL3RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
27:24	Fh	RW	**Upstream Port Lane 3 Transmitter Preset (UPL3TP)** Upstream Port Lane 3 Transmitter Preset (UPL3TP): Field contains the Transmit Preset value sent or received during Link Equalization.
23	-	-	**Reserved**
22:20	111b	RW	**Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH)** Downstream Port Lane 3 Receiver Preset Hint (DPL3RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
19:16	Fh	RW	**Downstream Port Lane 3 Transmitter Preset (DPL3TP)** Downstream Port Lane 3 Transmitter Preset (DPL3TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.
15	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
14:12	111b	RW	**Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH)** Upstream Port Lane 2 Receiver Preset Hint (UPL2RPH): Field contains the Receiver Preset Hint value sent or received during Link Equalization.
11:8	Fh	RW	**Upstream Port Lane 2 Transmitter Preset (UPL2TP)** Upstream Port Lane 2 Transmitter Preset (UPL2TP): Field contains the Transmit Preset value sent or received during Link Equalization.
7	-	-	**Reserved**
6:4	111b	RW	**Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH)** Downstream Port Lane 2 Receiver Preset Hint (DPL2RPH): Receiver Preset Hint may be used as a hint for receiver equalization by this Port when the Port is operating as a Downstream Port.
3:0	Fh	RW	**Downstream Port Lane 2 Transmitter Preset (DPL2TP)** Downstream Port Lane 2 Transmitter Preset (DPL2TP): Transmitter Preset used for equalization by this Port when the Port is operating as a Downstream Port. This field is ignored when the Port is operating as an Upstream Port.

PCI Express Replay Timer Policy 1 (PCIERTP1) – Offset 300

The Replay Timer controlled by the Replay Timeout field is started when the Retry Buffer is empty and a TLP is placed into it or an Ack/Nak DLLP is received and there are still non-acknowledged packets within the Retry Buffer. The counter continues to count until the next valid Ack DLLP or a NAK DLLP that acknowledges unacknowledged TLPs is received, or it reaches the timeout value specified by this register. When a valid Ack/Nak DLLP is received, the timer is reset to zero and restarted if there are still non-acknowledged packets within the Retry Buffer. Otherwise if the Retry Buffer is empty, the counter is just reset to zero. If the timer reaches the timeout value, the non-acknowledged packets within the Retry Buffer will be replayed.

The default for this register is dependant on the MAX_PAYLOAD_SIZE , the NEGOTIATED_WIDTH, and the NEGOTIATED_SPEED.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
23:20	Ah	RW	**Gen 2 x1 (G2X1)** Gen 2 x1 (G2X1): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 7) * 64 link clocks. For PCIE Gen 2 speed and x1 width For Mobile Express HS-Gear 3 speed and x1 width.
19:16	6h	RW	**Gen 2 x2 (G2X2)** Gen 2 x2 (G2X2): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 4) * 64 link clocks. For PCIe Gen 2 speed and x2 width. For Mobile Express HS-Gear 3 speed and x2 width.

Bit Range	Default	Access	Field Name and Description
15:12	4h	RW	**Gen 2 x4 (G2X4)** Gen 2 x4 (G2X4): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For PCIe Gen 2 speed and x4 width. For Mobile Express HS-Gear 3 speed and x4 width.
11:8	Fh	RW	**Gen 1 x1 (G1X1)** Gen 1 x1 (G1X1): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 10) * 64 link clocks. For 512B MPS: (nnn + 17) * 64 link clocks. For PCIe Gen 1 speed and x1 width. For Mobile Express HS-Gear 2 speed and x1 width.

Bit Range	Default	Access	Field Name and Description
7:4	9h	RW	**Gen 1 x2 (G1X2)** Gen 1 x2 (G1X2): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 8) * 64 link clocks. For PCIe Gen 1 speed and x2 width. For Mobile Express HS-Gear 2 speed and x2 width.
3:0	6h	RW	**Gen 1 x4 (G1X4)** Gen 1 x4 (G1X4): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For PCIe Gen 1 speed and x4 width. For Mobile Express HS-Gear 2 speed and x4 width.

PCI Express Replay Timer Policy 2 (PCIERTP2) – Offset 304

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:30	00b	RW	**Lane 0 Lane Number (L0LN)** Lane 0 Lane Number(L0LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 0 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
29:28	01b	RW	**Lane 1 Lane Number (L1LN)** Lane 1 Lane Number(L1LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 1 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
27:26	10b	RW	**Lane 2 Lane Number (L2LN)** Lane 2 Lane Number(L2LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 2 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
25:24	11b	RW	**Lane 3 Lane Number (L3LN)** Lane 3 Lane Number(L3LN): This field specifies the lane number to be used in the per-lane GEN3 scrambling/descrambling logic for lane 3 when entering Loopback from Configuration state, prior to Link width negotiation and for GEN3 Polling Compliance entry where the lane number is not available. This field should never be used on all other cases, including entry to Loopback from L0.
23	1b	RW	**Loopback Master EQ TS1 Enable (LMEQTS1E)** Loopback Master EQ TS1 Enable(LMEQTS1E): When set, the Loopback Master will use EQ TS1 Ordered Sets to direct the Loopback Slave into Loopback from Configuration.Linkwidth.Start. The Preset field of the EQ TS1 Ordered Sets will be specified by Upstream Port Lane X Transmitter Preset and Upstream Port Lane X Receiver Preset Hint fields in the Lane Equalization Control registers.

Bit Range	Default	Access	Field Name and Description
22	1b	RW	**Loopback Master EQ Change Enable (LMEQCE)** Loopback Master EQ Change Enable(LMEQCE): This field is applicable to the case where Loopback is entered from Recovery state. When set, the Loopback Master will set the EC field of the GEN3 TS1 Ordered Sets to the appropriate value based on the ports direction(10b or 11b) to direct the Loopback Slave into Loopback from Recovery state. The Preset field of the GEN3 TS1 Ordered Sets will be specified by Upstream Port Lane X Transmitter Preset and Upstream Port Lane X Receiver Preset Hint fields in the Lane Equalization Control registers.
21:12	-	-	**Reserved**
11:8	Bh	RW	**Gen 3 x1 (G3X1)** Gen 3 x1 (G3X1): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 8) * 64 link clocks. For Gen 3 speed and x1 width
7:4	8h	RW	**Gen 3 x2 (G3X2)** Gen 3 x2 (G3X2): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For Gen 3 speed and x2 width

Bit Range	Default	Access	Field Name and Description
3:0	6h	RW	**Gen 3 x4 (G3X4)** Gen 3 x4 (G3X4): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 1) * 64 link clocks. For 512B MPS: (nnn + 2) * 64 link clocks. For Gen 3 speed and x4 width

PCI Express Configuration (PCIEDBG) – Offset 324

Bit Range	Default	Access	Field Name and Description
31:29	000b	RW	**Transmit nFTS Adder (TXNFTSADD)** This field specifies the 1-based number of additional nFTS sets to be transmitted to the opposite device on TXL0s exit on top of the actual number of nFTS sets. 000: No additional nFTS to be transmitted on top of actual nFTS. 001: 1 additional nFTS to be transmitted on top of actual nFTS. 010: 2 additional nFTS to be transmitted on top of actual nFTS. : : 111: 7 additional nFTS to be transmitted on top of actual nFTS.
28:26	-	-	**Reserved**
25:24	10b	RW	**Configuration Field (LGCLKSQEXITDBTIMERS)** BIOS may program this register bit.
23:15	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
14	0b	RW	**Configuration Field (CTONFAE)** BIOS may program this register bit.
13:8	-	-	**Reserved**
7	0b	RW	**Configuration Field (SQOL0)** BIOS may program this register bit.
6	-	-	**Reserved**
5	0b	RW	**Configuration Field (SPCE)** BIOS may program this register bit.
4	0b	RO/V	**Lane Reversal (LR)** This register reflects the PCIe* Lane Reversal Configuration soft strap. It defines if the Root Port associated with a PCIe* Controller is configured with Lane Reversal enabled or disabled 0 = Disabled 1 = Enabled
3:0	-	-	**Reserved**

PCI Express Additional Link Control (PCIEALC) – Offset 338

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
29	0b	RW	**Initialize Transaction Layer Receiver Control on Link Down (ITLRCLD)** When set, the transaction layer receive control logic will be re-initialized when the link goes down. This is a survivability mode to recover the system from hang on surprise removal. Only the value from Port 1 is used for ports 1-4. Note: For each x4 instance, only the value from Port 0 is used.
28:27	-	-	**Reserved**
26	0b	RW/P	**Block Detect.Quiet->Detect.Active (BLKDQDA)** 0: Allow transition (Normal Operation) 1: Block transition. Prevents the present state from leaving the Detect.Quiet state. Note that this bit has no effect unless the present state is in the Detect.Quiet state. It will not force the present state into Detect.Quiet from any other state. Typically a warm reset of the platform is required after this bit is set.
25:0	-	-	**Reserved**

Additional Configuration 2 (LTROVR) – Offset 400

BIOS may need to program this register.

Additional Configuration 3 (LTROVR2) – Offset 404

BIOS may need to program this register.

Thermal and Power Throttling (TNPT) – Offset 418

Bit Range	Default	Access	Field Name and Description
31:24	00h	RW	**Throttle Period (TP)** Throttle Period (TP): If any of the TNPT.DRXLTE or TNPT.DTXLTE bit is 1, this field defines the duration in milliseconds that defines the Throttling Window. When TNPT.TTG is set to 0, the effective Throttling Period is: 00h: 1 ms 01h: 2 ms : : FFh: 256 ms Note: The Throttle Period will have an uncertainty of +/-1 ms. When TNPT.TTG is set to 1, the effective Throttling Period is: 00h: 100 us 01h: 200 us : : FFh: 25.6 ms Note: The Throttle Period will have an uncertainty of +/-100 us. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling. Note: If TNPT.TT is programmed to a value bigger than TNPT.TP, the hardware behavior is undefined.
23:16	00h	RW	

Bit Range	Default	Access	Throttle Time (TT) Field Name and Description
			Throttle Time (TT): If any of the TNPT.DRXLTE or TNPT.DTXLTE bit is 1, this field defines the period of the Throttling Zone within the Throttling Window specified by TNPT.TP. The value specified in this field will be multiplied by the respective multiplier in TNPT.TSLxM fields depending on the throttling severity indication received together with the Throttling State change indication. When TNPT.TTG is set to 0, the effective Throttle Time is: 00h: 1 ms 01h: 2 ms : 3Fh: 64 ms Others: Alias to 3Fh. Note: The Throttle Period will have an uncertainty of +/-1 ms. When TNPT.TTG is set to 1, the effective Throttle Time is: 00h: 100 us 01h: 200 us : 3Fh: 6.4 ms Note: The Throttle Period will have an uncertainty of +/-100 us. Note: If the reserved encoding is programmed to this field, hardware will behave the same as if the field is programmed to 3Fh. Note: Since the design is using a 1 ms tick for this timer, the Throttle Time will have an uncertainty of +/-1 ms. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling. Note: If TNPT.TT is programmed to a value bigger than TNPT.TP, the hardware behavior is undefined.

Bit Range	Default	Access	Field Name and Description
15:12	-	-	**Reserved**
11:10	10b	RW	**Throttling Severity Level 3 Multiplier (TSL3M)** Throttling Severity Level 3 Multiplier (TSL3M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: Always throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.
9:8	01b	RW	**Throttling Severity Level 2 Multiplier (TSL2M)** Throttling Severity Level 2 Multiplier (TSL2M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: Always throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.

Bit Range	Default	Access	Field Name and Description
7:6	00b	RW	**Throttling Severity Level 1 Multiplier (TSL1M)** Throttling Severity Level 1 Multiplier (TSL1M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: No throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the link throttling
5:4	11b	RW	**Throttling Severity Level 0 Multiplier (TSL0M)** Throttling Severity Level 0 Multiplier (TSL0M): This register determines the multiplier to be used together with the TNPT.TT field to specify the period of the Throttling Zone within the Throttling Window. 00b: x1 01b: x2 10b: x4 11b: No throttling. Note: To change the Link Throttling control bits, the DRXLTE and DTXLTE bits must be disabled first, change the value, and then re-enable the Link throttling.
3:2	-	-	**Reserved**
1	0b	RW	**Dynamic RX Link Throttling Enable (DRXLTE)** Dynamic RX Link Throttling Enable (DRXLTE): 0b: Dynamic Link RX Throttling mechanism is disabled. 1b: Dynamic Link RX Throttling mechanism is enabled. PCIe Root Port will induce the link to enter RXL0s. The duty cycle of the throttling window is configurable based on the throttling severity. Note: This field can only be set if the remote component supports TXL0s.

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**Dynamic TX Link Throttling Enable (DTXLTE)** Dynamic TX Link Throttling Enable (DTXLTE): 0b: Dynamic Link TX Throttling mechanism is disabled. 1b: Dynamic Link TX Throttling mechanism is enabled. PCIe Root Port will induce the link to enter TXL0s. The duty cycle of the throttling window is configurable based on the throttling severity. Note: This field can only be set if the remote component supports TXL0s.

Additional Configuration 4 (PCIEPMECTL) – Offset 420

BIOS may need to program this register.

Equalization Configuration 1 (EQCFG1) – Offset 450

Note: This register must be configured prior to enabling 8.0 GT/s data rate

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15	0b	RW	**Remote Transmitter Preset/Coefficient Override Enable (RTPCOE): (RTPCOE)** 0 = Reserved 1 = Enables Set Preset/Coefficient values specified by the fields in RTPCL1 and RTPCL2
14:0	-	-	**Reserved**

Remote Transmitter Preset/Coefficient List 1 (RTPCL1) – Offset 454

Note: This register must be configured prior to enabling 8.0 GT/s data rate

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31	0b	RW	**Preset/Coefficient Mode (PCM)** This bit defines whether the Preset values or Coefficient values should be sent to the remote TX to adjust the remote TX settings used in Phase 3 of Link Equalization 0 = Preset Mode is enabled 1 = Coefficient Mode is enabled
30	0b	RO	**Reserved (RSVD)** Reserved
29:24	00h	RW	**Remote Transmitter Pre-Cursor Coefficient List 2/Preset List 4 (RTPRECL2PL4)** Remote Transmitter Pre-Cursor Coefficient List 2/Preset List 4 (RTPRECL2PL4): For Downstream Port: This field defines the pre-cursor coefficient List 2 or Preset List 4 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 2 or Preset List 4 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
23:18	00h	RW	**Remote Transmitter Post-Cursor Coefficient List 1/Preset List 3 (RTPOSTCL1PL3)** If RTPCL1.PCM = 0 these bits represent the PCIe* Controller Lane 3 Preset value If RTPCL1.PCM = 1 these bits represent the PCIe* Controller Lane 1 Post-Cursor Coefficient value
17:12	00h	RW	**Remote Transmitter Pre-Cursor Coefficient List 1/Preset List 2 (RTPRECL1PL2)** If RTPCL1.PCM = 0 these bits represent the PCIe* Controller Lane 2 Preset value If RTPCL1.PCM = 1 these bits represent the PCIe* Controller Lane 1 Pre-Cursor Coefficient value

Bit Range	Default	Access	Field Name and Description
11:6	00h	RW	**Remote Transmitter Post-Cursor Coefficient List 0/Preset List 1 (RTPOSTCL0PL1)** If RTPCL1.PCM = 0 these bits represent the PCIe* Controller Lane 1 Preset value If RTPCL1.PCM = 1 these bits represent the PCIe* Controller Lane 0 Post-Cursor Coefficient value
5:0	00h	RW	**Remote Transmitter Pre-Cursor Coefficient List 0/Preset List 0 (RTPRECL0PL0)** If RTPCL1.PCM = 0 these bits represent the PCIe* Controller Lane 0 Preset value If RTPCL1.PCM = 1 these bits represent the PCIe* Controller Lane 0 Pre-Cursor Coefficient value

Remote Transmitter Preset/Coefficient List 2 (RTPCL2) (RTPCL2) – Offset 458

Note: This register must be configured prior to enabling 8.0 GT/s data rate

Bit Range	Default	Access	Field Name and Description
31:30	00b	RO	**Reserved (RSVD)** Reserved
29:24	00h	RW	**Remote Transmitter Post-Cursor Coefficient List 4/Preset List 9 (RTPOSTCL4PL9)** Remote Transmitter Post-Cursor Coefficient List 4/Preset List 9(RTPOSTCL4PL9): For Downstream Port: This field defines the post-cursor coefficient List 4 or Preset List 9 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 4 or Preset List 9 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default	Access	Field Name and Description
23:18	00h	RW	**Remote Transmitter Pre-Cursor Coefficient List 4/Preset List 8 (RTPRECL4PL8)** Remote Transmitter Pre-Cursor Coefficient List 4/Preset List 8 (RTPRECL4PL8): For Downstream Port: This field defines the pre-cursor coefficient List 4 or Preset List 8 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 4 or Preset List 8 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.
17:12	00h	RW	**Remote Transmitter Post-Cursor Coefficient List 3/Preset List 7 (RTPOSTCL3PL7)** Remote Transmitter Post-Cursor Coefficient List 3/Preset List 7 (RTPOSTCL3PL7): For Downstream Port: This field defines the post-cursor coefficient List 3 or Preset List 7 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 3 or Preset List 7 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default	Access	Field Name and Description
11:6	00h	RW	**Remote Transmitter Pre-Cursor Coefficient List 3/Preset List 6 (RTPRECL3PL6)** Remote Transmitter Pre-Cursor Coefficient List 3/Preset List 6 (RTPRECL3PL6): For Downstream Port: This field defines the pre-cursor coefficient List 3 or Preset List 6 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the pre-cursor coefficient List 3 or Preset List 6 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

Bit Range	Default	Access	Field Name and Description
5:0	00h	RW	**Remote Transmitter Post-Cursor Coefficient List 2/Preset List 5 (RTPOSTCL2PL5)** Remote Transmitter Post-Cursor Coefficient List 2/Preset List 5 (RTPOSTCL2PL5): For Downstream Port: This field defines the post-cursor coefficient List 2 or Preset List 5 to be used for the remote TX in Phase 3. For Upstream Port: This field defines the post-cursor coefficient List 2 or Preset List 5 to be used for the remote TX in Phase 2. When the remote TX has successfully applied the coefficient or preset, the local RX will then perform Receiver Eye Width Margining to check the margin. The list of coefficient or preset is traversed sequentially starting from List 0 to List N, where N is the most significant coefficient or preset in the list. This field is treated as Preset or Coefficient based on RTPCL1.PCM bit when EQCFG1.RTPCOE = 0. If EQCFG1.RTPCOE = 1, the definition of this field is described in the EQCFG1.RTPCOE description. The value of coefficient programmed into this field assumes FS=64. Hardware will scale the coefficient accordingly based on the remote device FS value.

PMC I/O Based Registers

The ACPI power management I/O registers are accessed based upon offsets from PM Base Address, BAR2, defined in PCI Device 31: Function 2.

Summary of Bus:, Device:, Function: (IO)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Power Management 1 Enables and Status (PM1_EN_STS)	0h
4h	4	Power Management 1 Control (PM1_CNT)	0h
8h	4	Power Management 1 Timer (PM1_TMR)	0h
30h	4	SMI Control and Enable (SMI_EN)	2h
34h	4	SMI Status Register (SMI_STS)	0h
40h	4	General Purpose Event Control (GPE_CTRL)	0h
44h	4	Device Activity Status Register (DEVACT_STS)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50h	4	PM2a Control Block (PM2A_CNT_BLK)	0h
54h	4	Over-Clocking WDT Control (OC_WDT_CTL)	2000h
60h	4	General Purpose Event 0 Status [31:0] (GPE0_STS_31_0)	0h
64h	4	General Purpose Event 0 Status [63:32] (GPE0_STS_63_32)	0h
68h	4	General Purpose Event 0 Status [95:64] (GPE0_STS_95_64)	0h
6ch	4	General Purpose Event 0 Status [127:96] (GPE0_STS[127:96])	0h
70h	4	General Purpose Event 0 Enable [31:0] (GPE0_EN_31_0)	0h
74h	4	General Purpose Event 0 Enable [63:32] (GPE0_EN_63_32)	0h
78h	4	General Purpose Event 0 Enable [95:64] (GPE0_EN_95_64)	0h
7ch	4	General Purpose Event 0 Enable [127:96] (GPE0_EN[127:96])	0h

Power Management 1 Enables and Status (PM1_EN_STS) – Offset 0

Bit Range	Default	Access	Field Name and Description
30	0b	RW	**PCI Express Wake Disable (PCIEXP_WAKE_DIS)** This bit disables the inputs to the PCIEXP_WAKE_STS bit in the PM1 Status register from waking the system. Modification of this bit has no impact on the value of the PCIEXP_WAKE_STS bit. This bit is reset by DSW_PWROK de-assertion.
29:27	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
26	0b	RW/V	**RTC Alarm Enable (RTC_EN)** This is the RTC alarm enable bit. It works in conjunction with the SCI_EN bit: RTC_EN SCI_EN Effect when RTC_STS is set 0 X No SMI# or SCI. If system was in S3-S5, no wake even occurs. 1 0 SMI#. If system was in S3-S5, then a wake event occurs before the SMI#. 1 1 SCI. If system was in S3-S5, then a wake event occurs before the SCI. Note: This bit is in the RTC well and is reset by RTCRST# assertion, to allow an RTC event to wake after a power failure.
25	-	-	**Reserved**
24	0b	RW/V	**Power Button Enable (PWRBTN_EN)** This bit is the power button enable. It works in conjunction with the SCI_EN bit PWRBTN_EN SCI_EN Effect when PWRBTN_STS is set 0 X No SMI# or SCI. 1 0 SMI#. 1 1 SCI. NOTE: PWRBTN_EN has no effect on the PWRBTN_STS bit being set by the assertion of the power button. The Power Button is always enabled as a Wake event.
23:22	-	-	**Reserved**
21	0b	RW	**Global Enable (GBL_EN)** Global enable bit. When both the GBL_EN and the GBL_STS are set, PCH generates an SCI. This bit is reset by PLTRST# assertion.
20:17	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
16	0b	RW	**Timer Overflow Interrupt Enable (TMROF_EN)** This is the timer overflow interrupt enable bit. It works in conjunction with the SCI_EN bit: TMROF_EN SCI_EN Effect when TMROF_STS is set 0 X No SMI# or SCI. 1 0 SMI#. 1 1 SCI. This bit is reset by PLTRST# assertion.
15	0b	RW/1C/V	**Wake Status (WAK_STS)** This bit is set when the system is in one of the Sleep states (via the SLP_EN bit) and an enabled Intel PCH Wake event occurs. Upon setting this bit, the Intel PCH will transition the system to the ON state. This bit can only be set by hardware and can only be cleared by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST#. If a power failure occurs (such as removed batteries) without the SLP_EN bit set, the WAK_STS bit will not be set when the power returns if the AFTER_G3 bit is 0. If the AFTER_G3 bit is 1, then the WAK_STS bit will be set after waking from a power failure. If necessary, the BIOS can clear the WAK_STS bit in this case.
14	0b	RW/1C/V	**PCI Express Wake Status (PCIEXP_WAKE_STS)** This bit is set by hardware to indicate that the system woke due to a PCI Express wakeup event. This event can be caused by the PCI Express WAKE# pin being active, or one or more of the PCI Express ports being in beacon state, or recept of a PCI Express PME message at root port. This bit should only be set when one of these events causes the system to transition from a non-S0 system power state to the S0 system power state. This bit is set independant of the PCIEXP_WAKE_DIS bit. Software writes a 1 to clear this bit. If WAKE# pin is still active during the write or one or more PCI Express ports is in the beacon state or PME message received indication is not cleared in the root port, then the bit will remain active (i.e. all inputs to this bit are level sensitive) Note: This bit does not itself cause a wake event or prevent entry to a sleeping state. Thus if the bit is 1 and the system is put into a sleeping state, the system will not automatically wake.

Bit Range	Default	Access	Field Name and Description
13:12	-	-	**Reserved**
11	0b	RW/1C/V	**Power Button Override (PWRBTNOR_STS)** This bit is set any time a Power Button Override Event occurs (i.e. the power button is pressed for at least 4 consecutive seconds), the corresponding bit is received in the SMBus slave message, the ME-Initiated Power Button Override bit is set, the ME-Initiated Host Reset with Power Down is set, or due to an internal thermal sensor catastrophic condition. These events cause an unconditional transition to the S5 state. The BIOS or SCI handler clears this bit by writing a 1 to it. This bit is not affected by hard resets via CF9h writes, and is not reset by RSMRST#. Thus, this bit is on RTC well and is preserved through power failures (reset by RTCRST#). Note that this bit is still asserted when the global SCI_EN is set to '1' then an SCI will be generated.
10	0b	RW/1C/V	**RTC Status (RTC_STS)** This bit is set when the RTC generates an alarm (assertion of the IRQ8# signal), and is not affected by any other enable bit. See RTC_EN for the effect when RTC_STS goes active. This bit is only set by hardware and can only be reset by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by DSW_PWROK de-assertion.
9	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
8	0b	RW/1C/V	**Power Button Status (PWRBTN_STS)** This bit is set when the PWRBTN# signal is asserted (low), independent of any other enable bit. See PWRBTN_EN for the effect when PWRBTN_STS goes active. PWRBTN_STS is always a wake event. This bit is only set by hardware and can be cleared by software writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by DSW_PWROK de-assertion. If the PWRBTN# signal is held low for more than 4 seconds, the Intel PCH clears the PWRBTN_STS bit, sets the PWRBTNOR_STS bit, the system transitions to the S5 state, and only PWRBTN# is enabled as a wake event. If PWRBTN_STS bit is cleared by software while the PWRBTN# pin is still held low, this will not cause the PWRBTN_STS bit to be set. The PWRBTN# signal must go inactive and active again to set the PWRBTN_STS bit. Note that the SMBus Unconditional Powerdown message, the CPU Thermal Trip and the Internal Thermal Sensors' Catastrophic Condition result in behavior matching the Powerbutton Override, which includes clearing this bit.
7:6	-	-	**Reserved**
5	0b	RW/1C/V	**GBL Status (GBL_STS)** This bit is set when an SCI is generated due to the BIOS wanting the attention of the SCI handler. BIOS has a corresponding bit, BIOS_RLS, which will cause an SCI and set this bit. The SCI handler should then clear this bit by writing a 1 to it. This bit will not cause wake events or SMI#. This bit is not effected by SCI_EN. Note: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place. This bit is reset by PLTRST# assertion.
4	0b	RW/1C/V	**Bus Master Status (BM_STS)** This bit is set to 1 by the Intel PCH when a PCH-visible bus master requests access to memory or the BM_BUSY# signal is active. This bit is cleared by the Processor writing a 1 to this bit position. This bit will not cause a wake event, SCI, or SMI. This bit is reset by PLTRST# assertion.
3:1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	0b	RW/1C/V	**Timer Overflow Status (TMROF_STS)** This is the timer overflow status bit. This bit gets set anytime bit 22 of the 24 bit timer goes low (bits are counted from 0 to 23). This will occur every 2.3435 seconds. See TMROF_EN for the effect when TMROF_STS goes active. Software clears this bit by writing a 1 to it. This bit is reset by PLTRST# assertion.

Power Management 1 Control (PM1_CNT) – Offset 4

Lockable: No

Usage: ACPI or Legacy

Power Well: Bits 0-9, 13-31: Primary, Bits 10-12: RTC

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13	0b	WO	**Sleep Enable (SLP_EN)** This is a write-only bit and reads to it always return a zero. Setting this bit causes the system to sequence into the Sleep state defined by the SLP_TYP field. This bit is reset by PLTRST# assertion.

Bit Range	Default	Access	Field Name and Description
12:10	000b	RW	**Sleep Type (SLP_TYP)** This 3-bit field defines the type of Sleep the system should enter when the SLP_EN bit is set to 1. Bits Mode Typical Mapping 000 ON S0 001 Reserved 010 Reserved 011 Reserved 100 Reserved 101 Suspend-To-RAM S3 110 Suspend-To-Disk S4 111 Soft Off S5 These bits are reset by RTCRST# only.
9:3	-	-	**Reserved**
2	0b	WO	**Global Release (GBL_RLS)** This bit always reads as 0. ACPI software writes a '1' to this bit to raise an event to the BIOS. BIOS sfotware has corresponding enable and status bits to control its ability to receive ACPI events.

Bit Range	Default	Access	Field Name and Description
1	-	-	**Reserved**
0	0b	RW	**SCI Enable (SCI_EN)** Selects the SCI interrupt or the SMI# for various events. 0 = These events will generate an SMI#. 1 = These events will generate an SCI. This bit is reset by PLTRST# assertion.

Power Management 1 Timer (PM1_TMR) – Offset 8

Lockable: No

Usage: ACPI

Power Well: Primary

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:0	000000h	RO/V	**Timer Value (TMR_VAL)** This read-only field returns the running count of the PM timer. This counter runs off a 3.579545 MHz clock (derived from 14.31818 MHz divided by 4). It is reset (to 0) during a PCI reset, and then continues counting as long as the system is in the S0 state. Anytime bit 22 of the timer goes HIGH to LOW (bits referenced from 0 to 23), the TMROF_STS bit is set. The High-to-Low transition will occur every 2.3435 seconds. Writes to this register have no effect.

SMI Control and Enable (SMI_EN) – Offset 30

Lockable: No

Usage: ACPI or Legacy

Power Well: Primary

Note: This register is symmetrical to the SMI Status Register.

Bit Range	Default	Access	Field Name and Description
31	0b	RW	**XHCI SMI Enable (XHCI_SMI_EN)** Software sets this bit to enable XHCI SMI events. This bit is reset by PLTRST# assertion.
30	0b	RW	**ME SMI Enable (ME_SMI_EN)** Software sets this bit to enable ME SMI# events. This bit is reset by PLTRST# assertion.
29	-	-	**Reserved**
28	0b	RW/L	**eSPI SMI Enable (ESPI_SMI_EN)** Software sets this bit to enable eSPI SMI events. This bit is reset by PLTRST# assertion.
27	0b	RW/1S	**GPIO Unlock SMI Enable (GPIO_UNLOCK_SMI_EN)** Setting this bit will cause the Intel PCH to generate an SMI# when the GPIO_UNLOCK_SMI_STS bit is set in the SMI_STS register. Once written to '1', this bit can only be cleared by PLTRST# assertion.
26:18	-	-	**Reserved**
17	0b	RW	**Legacy USB 2 SMI# Enable (LEGACY_USB2_EN)** Enables legacy USB2 logic to cause SMI#.
16:15	-	-	**Reserved**
14	0b	RW	**Periodic Enable (PERIODIC_EN)** Setting this bit will cause the Intel PCH to generate an SMI# when the PERIODIC_STS bit is set in the SMI_STS register. This bit is reset by PLTRST# assertion.

Bit Range	Default	Access	Field Name and Description
13	0b	RW/L	**TCO Enable (TCO_EN)** 1 = Enables the TCO logic to generate SMI#. 0 = Disables TCO logic from generating an SMI#. If the NMI2SMI_EN bit is set, then SMI's that are caused by NMI's (i.e. rerouted) will not be gated by the TCO_EN bit . Even if the TCO_EN bit is 0, the NMI's will still be routed to cause the SMI#. NOTE: This bit can not be written once the TCO_LOCK bit (at offset 08h of TCO I/O Space) is set. This prevents unauthorized software from disabling the generation of TCO-based SMI's. This bit is reset by PLTRST# assertion.
12	-	-	**Reserved**
11	0b	RW	**Microcontroller SMI Enable (MCSMI_EN)** Software sets this bit to 1 to enables Intel PCH to trap access to the microcontroller range (62h or 66h). A 'trapped' cycles will be claimed by Intel PCH, but not forwarded to LPC. An SMI# will also be generated. This bit is reset by PLTRST# assertion.
10:8	-	-	**Reserved**
7	0b	WO	**BIOS Release (BIOS_RLS)** Enables the generation of an SCI interrupt for ACPI software when a '1' is written to this bit position by BIOS software. This bit always reads a '0'. NOTE: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place. This bit is reset by PLTRST# assertion.

Bit Range	Default	Access	Field Name and Description
6	0b	RW	**Software SMI Timer Enable (SWSMI_TMR_EN)** Software sets this bit to a '1' to start the Software SMI# Timer. When the timer expires (depending on the SWSMI_RATE_SEL bits), it will generate an SMI# and set the SWSMI_TMR_STS bit. The SWSMI_TMR_EN bit will remain at 1 until software sets it back to 0. Clearing the SWSMI_TMR_EN bit before the timer expires will reset the timer and the SMI# will not be generated. The default for this bit is 0. This bit is reset by PLTRST# assertion.
5	0b	RW	**APMC Enable (APMC_EN)** If set, this enables writes to the APM_CNT register to cause an SMI#. This bit is reset by PLTRST# assertion.
4	0b	RW	**SMI On Sleep Enable (SMI_ON_SLP_EN)** If this bit is set, the Intel PCH will generate an SMI# when a write access attempts to set the SLP_EN bit (in the PM1_CNT register). Furthermore, the Intel PCH will not put the system to a sleep state. It is expected that the SMI# handler will turn off the SMI_ON_SLP_EN bit before actually setting the SLP_EN bit. This bit is reset by PLTRST# assertion.
3	0b	RW	**Legacy USB Enable (LEGACY_USB_EN)** Enables legacy USB circuit to cause SMI#. This bit is reset by PLTRST# assertion.
2	0b	RW	**BIOS Enable (BIOS_EN)** Enables the generation of SMI# when ACPI software writes a 1 to the GBL_RLS bit. Note that if the BIOS_STS bit, which gets set when software writes a 1 to GBL_RLS bit, is already a 1 at the time that BIOS_EN becomes 1, an SMI# will be generated when BIOS_EN gets set. This bit is reset by PLTRST# assertion.

Bit Range	Default	Access	Field Name and Description
1	1b	RW/1S/V	**End of SMI (EOS)** This bit controls the arbitration of the SMI signal to the processor. This bit must be set in order for Intel PCH to assert SMI# low to the processor after SMI# has been asserted previously. Once Intel ICH asserts SMI# low, the EOS bit is automatically cleared. In the SMI handler, the CPU should clear all pending SMIs (by servicing them and then clearing their respective status bits), set the EOS bit, and exit SMM. This will allow the SMI arbiter to reassert SMI upon detection of an SMI event and the setting of a SMI status bit. The SMI# signal will go inactive for 4 PCI clocks. This bit is reset by PLTRST# assertion.
0	0b	RW/L	**Global SMI Enable (GBL_SMI_EN)** 0 = No SMI# will be generated by PCH. 1 = Enables the generation of SMI# in the system upon any enabled SMI event. NOTE: When the SMI_LOCK bit is set, this bit cannot be changed. This bit is reset by PLTRST# assertion.

SMI Status Register (SMI_STS) – Offset 34

Lockable: No

Usage: ACPI or Legacy

Power Well: Primary

Note: If the corresponding _EN bit is set when the _STS bit is set, the Intel PCH will cause an SMI# (except bits 8-10, which don't cause SMI#)

Bit Range	Default	Access	Field Name and Description
31	0b	RO/V	**XHCI SMI Status (XHCI_SMI_STS)** This bit will be set when any USB3 (XHCI) Host Controller is requesting an SMI.
30	0b	RO/V	**ME SMI Status (ME_SMI_STS)** This bit will be set when ME is requesting an SMI#.
29	0b	RW/1C/V	**Intel Serial I/O SMI Status (LPSS_SMI_STS)** This bit gets set when Intel Serial I/O agent is requesting SMI #. This bit is set by hardware and cleared by software writing a 1 to this bit position.

Bit Range	Default	Access	Field Name and Description
28	0b	RO/V	**eSPI SMI Status (ESPI_SMI_STS)** This bit is set if an eSPI agent is requesting an SMI#. This bit is set by hardware and cleared when the PCH receives an eSPI SMI deassertion from an eSPI device.
27	0b	RW/1C/V	**GPIO Unlock SMI Status (GPIO_UNLOCK_SMI_STS)** This bit will be set of the GPIO registers lockdown logic is requesting an SMI#. Writing a '1' to this bit position clears this bit to '0'. This bit is reset by PLTRST# assertion.
26	0b	RO/V	**SPI SMI Status (SPI_SMI_STS)** This bit will be set when the SPI logic is requesting an SMI#. This bit is read only because the sticky status and enable bits associated with this function are located in the SPI registers.
25	0b	RW/1C/V	**SCC SMI Status (SDX_SMI_STS)** This bit gets set when SCC agent is requesting SMI#.This bit is set by hardware and cleared by software writing a 1 to this bit position
24:22	-	-	**Reserved**
21	0b	RO/V	**Monitor Status (MONITOR_STS)** This bit will be set if the Trap/SMI logic has caused the SMI. This will occur when the CPU or a bus master accesses an assigned register (or a sequence of accesses).
20	0b	RO/V	**PCI_EXP_SMI Status (PCI_EXP_SMI_STS)** 1- PCI Express SMI event occurred. This could be due to a PCI Express PME event or Hot Plug Event.
19:17	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
16	0b	RW/1C/V	**SMBus SMI Status (SMBUS_SMI_STS)** 0 = This bit is set from the 64 KHz clock domain used by the SMBus. Software must wait at least 15.63 microseconds after initial assertion of this bit before clearing it. This bit is sticky and is cleared by writing a 1 to this bit position. 1 = Indicates that the SMI# was caused by: 1.The SMBus Slave receiving a message that an SMI# should be caused, or 2. The SMBALERT# signal goes active and the SMB_SMI_EN bit is set and the SMBALERT_DIS bit is cleared, or 3. The SMBus Slave receiving a HOST_NOTIFY message and the HOST_NOTIFY_INTREN and the SMB_SMI_EN bits are set, or 4. The SMBus Slave receiving a "SMI in S0" message. This bit is reset by PLTRST# assertion.
15	0b	RO/V	**SERIRQ_SMI Status (SERIRQ_SMI_STS)** 1 = Indicates the SMI# was caused by the SERIRQ decoder. 0 = SMI# not caused by SERIRQ decoder. NOTE: this bit is not sticky. Writes to this bit will have no effect.
14	0b	RW/1C/V	**Periodic Status (PERIODIC_STS)** This bit will be set at the rate determined by the PER_SMI_SEL bits. If the PERIODIC_EN bit is also set, the Intel PCH will generate an SMI#. This bit is cleared by writing a 1 to this bit position. This bit is reset by PLTRST# assertion.
13	0b	RW/1C/V	**TCO Status (TCO_STS)** 0 = SMI not caused by TCO logic. 1 = Indicates SMI was caused by the TCO logic. NOTE: Will not cause wake event. This bit is cleared by writing a 1 to this bit position. This bit is reset by PLTRST# assertion.
12	0b	RO/V	**DEVMON Status (DEVMON_STS)** This read-only bit is set when bit 0 in the DEVTRAP_STS register is set. It is not sticky, so writes to this bit will have no effect.

Bit Range	Default	Access	Field Name and Description
11	0b	RW/1C/V	**Microcontroller SMI Status (MCSMI_STS)** This bit is set if there is an access to the power management microcontroller range (62h or 66h). If this bit is set, and the MCSMI_EN bit is also set, the Intel PCH will generate an SMI#. This bit is set by hardware and cleared by software writing a 1 to its bit position. This bit is reset by PLTRST# assertion.
10	0b	RO/V	**GPIO SMI Status (GPIO_SMI_STS)** This bit will be a 1 if any GPIO that is enabled to trigger SMI is asserted. GPIOs that are not routed to cause an SMI will have no effect on this bit. This bit is NOT sticky. Writes to this bit will have no effect. Note: See the GPIO chapter for the individual GPIO SMI status, enable, and routing bit definitions.
9	0b	RO/V	**GPE0 Status (GPE0_STS)** There are several status/enable bit pairs in GPE0_STS/EN_127_96 that are capable of triggering SMI#s. This bit is a logical OR of all of those pairs (i.e. this bit is asserted whenever at least one of those pairs has both the status and enable bit asserted). This bit is NOT sticky. Writes to this bit will have no effect. Note: The setting of this bit does not cause the SMI#. The following bit pairs are included in this logical OR: - GPE0_STS/EN_127_96 [18, 17, 16, 13, 11, 10, 8, 2]
8	0b	RO/V	**PM1 Status Register (PM1_STS_REG)** This is an OR of the bits (except for bits 5 and 4) in the ACPI PM1 Status Reg. Not sticky. Writes to this bit have no effect. Note: The setting of this bit does not cause the SMI#.
7	-	-	**Reserved**
6	0b	RW/1C/V	**Software SMI Timer Status (SWSMI_TMR_STS)** This bit will be set to 1 by the hardware when the Software SMI# Timer expires. This bit will remain 1 until the software writes a 1 to this bit. This bit is reset by PLTRST# assertion.

Bit Range	Default	Access	Field Name and Description
5	0b	RW/1C/V	**APM Status (APM_STS)** SMI# was generated by a write access to the APM control register and if the APMC_EN bit is set. This bit is cleared by writing a one to its bit position. This bit is reset by PLTRST# assertion.
4	0b	RW/1C/V	**SMI_ON_SLP_EN Status (SMI_ON_SLP_EN_STS)** This bit will be set by the Intel PCH when a write access attempts to set the SLP_EN bit. This bit is cleared by writing a 1 to this bit position. This bit is reset by PLTRST# assertion.
3	0b	RO/V	**Legacy USB Status (LEGACY_USB_STS)** This non-sticky read-only bit is a logical OR of each of the SMI status bits in the USB Legacy Keybd Register ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect.
2	0b	RW/1C/V	**BIOS Status (BIOS_STS)** This bit gets set by hardware when a 1 is written by software to the GBL_RLS bit. When both BIOS_EN and the BIOS_STS bit are set, an SMI# will be generated. The BIOS_STS bit is cleared when software writes a 1 to this bit position. This bit is reset by PLTRST# assertion.
1:0	-	-	**Reserved**

General Purpose Event Control (GPE_CTRL) – Offset 40

Lockable: No

Usage: ACPI or Legacy

Power Well: Primary

Bit Range	Default	Access	Field Name and Description
30:18	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
17	0b	RW/V	**Software GPE Control (SWGPE_CTRL)** This bit allows software to control the assertion of SWGPE_STS bit. This bit is used by hardware as the level input signal for the SWGPE_STS bit in the GPE0_STS register. When SWGPE_CTRL is 1, SWGPE_STS will be set to 1, and writes to SWGPE_STS with a value of 1 to clear SWGPE_STS will result in SWGPE_STS being set back to 1 by hardware. When SWGPE_CTRL is 0, writes to SWGPE_STS with a value of 1 will clear SWGPE_STS to 0. This bit is reset by RSMRST# assertion.
16:0	-	-	**Reserved**

Device Activity Status Register (DEVACT_STS) – Offset 44

Each bit indicates if an access has occured to the corresponding device's trap range, or for bits 6:9, if the corresponding PCI interrupt is active. This register is used in conjunction with the Periodic SMI# timer to detect any system activity for legacy power management. The periodic SMI# timer indicates if it is the right time to read the DEVACT_STS register.

Note, software clears bits that are set in this register by writing a 1 to the bit position.

Bit Range	Default	Access	Field Name and Description
30:6	-	-	**Reserved**
5	0b	RW/1C/V	**D5 Trap Status (D5_TRP_STS)** 0 = The corresponding I/O have not been accessed. 1 = The following are accessed (as determined by the I/O ranges in the LPC decoder and even if the LPC forwarding is not enabled): SP1, SP2, PP, FDC. Clear this bit by writing a 1 to the bit location. This bit is cleared by PLTRST# assertion.
4:0	-	-	**Reserved**

PM2a Control Block (PM2A_CNT_BLK) – Offset 50

Lockable: No

Usage: ACPI or Legacy

Power Well: Primary

Note: BIOS must describe this register as 1 byte wide to the OS.

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0b	RW	**Arbiter Disable (ARB_DIS)** This bit is a scratchpad bit for legacy software compatibility. This bit is reset by PLTRST# assertion.

Over-Clocking WDT Control (OC_WDT_CTL) – Offset 54

This register controls the operation of the PCH Over-Clocking Watchdog Timer.

Bit Range	Default	Access	Field Name and Description
31	0b	WO	**Over-Clocking WDT Reload (OC_WDT_RLD)** Software can write a '1' to this bit to reload ("ping") the PCH over-clocking watchdog timer while it is running. A write of '0' to this bit has no effect. A write of '1' to this bit while OC_WDT_EN=0, or with the clearing of OC_WDT_EN, does not start or reload the WDT (i.e. OC_WDT_EN takes precedence). The value in OC_WDT_TOV may be changed by software along with its setting of this bit. On a WDT reload, the current (potentially new) value in OC_WDT_TOV is loaded into the WDT as the new timeout value.
30:26	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
25	0b	RW/1C/V	**Over-Clocking WDT ICC Survivability Mode Timeout Status (OC_WDT_ICCSURV_STS)** This bit is set to '1' if the over-clocking WDT has timed out and triggered a global reset while running in a mode that has ICC survivability impact (OC_WDT_ICCSURV=1). It is cleared by a software write of '1' or by RSMRST# assertion.
24	0b	RW/1C/V	**Over-Clocking WDT Non-ICC Survivability Mode Timeout Status (OC_WDT_NO_ICCSURV_STS)** This bit is set to '1' if the over-clocking WDT has timed out and triggered a global reset while running in a mode that does not have ICC survivability impact (OC_WDT_ICCSURV=0). It is cleared by a software write of '1' or by RSMRST# assertion.
23:16	00h	RW	**Over-Clocking WDT Scratchpad (OC_WDT_SCRATCH)** This field is available as scratchpad space for software and has no effect on PCH HW operation. This bit is reset by RSMRST# assertion.
15	0b	RW/L	**Over-Clocking WDT Force All (OC_WDT_FORCE_ALL)** GATE_BIT:OC_WDT_CTL.OC_WDT_CTL_LCK.HIGH When this bit is set to '1' and the OC_WDT is running, any included global reset source will behave as though the OC_WDT expired. This bit is reset by RSMRST# assertion or CF9 reset.
14	0b	RW/V/L	**Over-Clocking WDT Enable (OC_WDT_EN)** Software sets this bit to '1' to enable the PCH over-clocking watchdog timer. While the counter is running, if it expires before being reloaded by software via the OC_WDT_RLD bit or halted by software clearing this bit, then one of the status bits will be set (which one depends on the WDT operating mode at the time - see the OC_WDT_ICCSURV bit description), and a global reset will be triggered. This bit is also set by the hardware when conditions allow the OC_WDT to self-start at power cycle reboot (effectively changes the default of this bit as seen by software).

Bit Range	Default	Access	Field Name and Description
13	1b	RW/L	**Over-Clocking WDT ICC Survivability Impact (OC_WDT_ICCSURV)** This bit determines whether OC_WDT expiration will have an impact on ICC (Integrated Clock Controller) bootstrap survivability. OC_WDT_ICCSURV=1 (default) An OC_WDT timeout while operating in this mode causes certain ICC hardware auto-recovery actions to take place. A timeout in this mode will set OC_WDT_ICCSURV_STS.OC_WDT_ICCSURV=0 Software should configure the OC_WDT to this mode if no ICC hardware auto-recovery actions are desired in the event of a timeout. A timeout in this mode will set OC_WDT_NO_ICCSURV_STS
12	0b	RW/L	**OC_WDT_CTL Register Lock (OC_WDT_CTL_LCK)** This bit controls write-ability to this register. Encodings: 0: All fields of register OC_WDT_CTL operate as normal and can be updated by software. Reads to the register operate as normal. 1: All RW/L fields of register OC_WDT_CTL, including this lock control bit, are locked. Writes to these register fields have no effect and the register fields retain their current states. Reads to the register operate as normal. Once this bit is set, it can only be cleared by Primary well power loss (via RSMRST# assertion).
11:10	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
9:0	000h	RW/V/L	**Over-Clocking WDT Timeout Value (OC_WDT_TOV)** Software programs the desired over-clocking WDT timeout value into this register. This timer is zero-based and has a granularity of 1 second. Example timeout values: 000h: 1 second 001h: 2 seconds ... 3FFh: ~17 minutes (1024 seconds) The value of OC_WDT_TOV may be changed by software along with its setting of the OC_WDT_RLD bit. On a WDT reload, the current (potentially new) value in OC_WDT_TOV is loaded into the WDT as the new timeout value. This field is also updated by the hardware when conditions allow the OC_WDT to self-start at power cycle reboot (effectively changes the default of this field as seen by software).

General Purpose Event 0 Status [31:0] (GPE0_STS_31_0) – Offset 60

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/1C/V	**General Purpose Event 0 Status [31:0] (GPE0_STS_31_0)** These bits are set any time the corresponding GPIO is setup as an input and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPE0_EN_31_0 register, then when the GPE0_STS_31_0 bit is set: - If system is in an S3-S5 state, the event will also wake the system. - If system is in an S0 state (or upon waking back to S0), an SCI will be caused, depending on the GPIROUTSCI bit for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position. Note: The GPP/GPD group mapped to this GPE0_STS_31_0 is configured via GPIO_CFG.DW0 and MISCCFG.DW0. Both GPIO_CFG.DW0 and MISCCFG.DW0 must be programmed to the same value.

General Purpose Event 0 Status [63:32] (GPE0_STS_63_32) – Offset 64

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/1C/V	**General Purpose Event 0 Status [63:32] (GPE0_STS_63_32)** These bits are set any time the corresponding GPIO is setup as an input and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPE0_EN_63_32 register, then when the GPE0_STS_63_32 bit is set: - If system is in an S3-S5 state, the event will also wake the system. - If system is in an S0 state (or upon waking back to S0), an SCI will be caused, depending on the GPIROUTSCI bit for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position. Note: The GPP/GPD group mapped to this GPE0_STS_63_32 is configured via GPIO_CFG.DW1 and MISCCFG.DW1. Both GPIO_CFG.DW1 and MISCCFG.DW1 must be programmed to the same value.

General Purpose Event 0 Status [95:64] (GPE0_STS_95_64) – Offset 68

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/1C/V	**General Purpose Event 0 Status [95:64] (GPE0_STS_95_64)** These bits are set any time the corresponding GPIO is setup as an input and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPE0_EN_95_64 register, then when the GPE0_STS_95_64 bit is set: - If system is in an S3-S5 state, the event will also wake the system. - If system is in an S0 state (or upon waking back to S0), an SCI will be caused, depending on the GPIROUTSCI bit for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position. Note: The GPP/GPD group mapped to this GPE0_STS_95_64 is configured via GPIO_CFG.DW2 and MISCCFG.DW2. Both GPIO_CFG.DW2 and MISCCFG.DW2 must be programmed to the same value.

General Purpose Event 0 Status [127:96] (GPE0_STS[127:96]) – Offset 6c

Note: This register is symmetrical to the General Purpose Event 0 Enable [127:96] Register. Unless indicated otherwise below, if the corresponding _EN bit is set, then when the STS bit get set, the Intel PCH will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the Intel PCH will also generate an SCI if the SCI_EN

bit is set, or an SMI# if the SCI_EN bit is not set and GBL_SMI_EN is set.

Note that GPE0_STS bits 95:0 are claimed by the GPIO register block.

Bit Range	Default	Access	Field Name and Description
30:19	-	-	**Reserved**
18	0b	RW/1C/V	**Wake Alarm Device Timer Status (WADT_STS)** This bit is set whenever the any of the wake alarm device timers signal a timer expiration. This bit is reset by RSMRST# assertion.
17:16	-	-	**Reserved**
15	0b	RW/1C/V	**GPIO Tier2 SCI Status (GPIO_TIER2_SCI_STS)** This bit is a logical OR of sci_wake from tier 2 GPIO's.
14	0b	RW/1C/V	**eSPI SCI Status (ESPI_SCI_STS)** This bit will be set when an agent attached to eSPI is requesting an SCI. Note: This source is not able to cause a wake event. This bit is reset by RSMRST# assertion.

Bit Range	Default	Access	Field Name and Description
13	0b	RW/1C/V	**Power Management Event Bus 0 Status (PME_B0_STS)** This bit will be set to 1 by the Intel PCH when any internal device with PCI Power Management capabilities on bus 0 asserts the equivalent of the PME# signal. Additionally, if the PME_B0_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the PME_B0_STS bit will generate an SCI (or SMI# if SCI_EN is not set). If the PME_B0_EN bit is set, and the system is in an S3-S4 state (or S5 state due to SLP_TYP and SLP_EN), then the setting of the PME_B0_STS bit will generate a wake event. If the system is in an S5 state due to power button override, then the PME_B0_STS bit will not cause a wake event or SCI. This bit is cleared by a software write of '1'. Internal devices which can set this bit: - Integrated LAN - HD Audio/Audio DSP - SATA - XHCI - CNVi - ME Maskable Host Wake This bit is reset by RSMRST# assertion.

Bit Range	Default	Access	Field Name and Description
12	0b	RW/1C/V	**ME SCI Status (ME_SCI_STS)** This bit will be set when ME is requesting an SCI. Software must clear the ME source of the SCI before clearing this bit. Note: This source is not able to cause a wake event. This bit is reset by RSMRST# assertion.
11	0b	RW/1C/V	**Power Management Event Status (PME_STS)** This bit will be set to 1 by hardware when the PME# signal goes active. Additionally, if the PME_EN and SCI_EN bits are set, and system is in an S0 state, then the setting of the PME_STS bit will generate an SCI (or SMI# if SCI_EN is not set). If the PME_EN bit is set, and the system is in an S3-S4 state (or S5 state due to SLP_TYP and SLP_EN), then the setting of the PME_STS bit will generate a wake event. If the system is in an S5 state due to power button override, then PME_STS will not cause a wake event or SCI. This bit is cleared by writing a 1 to this bit position or RSMRST# assertion.
10	0b	RW/1C/V	**Battery Low Status (BATLOW_STS)** In Mobile Mode this bit will be set to 1 by hardware when the BATLOW# signal goes low. Software clears the bit by writing a 1 to the bit position. In Desktop Mode, this bit will be treated as Reserved. This bit is reset by RSMRST# assertion.
9	0b	RW/1C/V	**PCI Express Status (PCI_EXP_STS)** This bit will be set to 1 by hardware to indicate that: - The PME event message was received on one or more of the PCI-Express Ports - An Assert PMEGPE message received from the MCH via DMI Note: The PCI WAKE# pin and the PCI-Express Beacons have no impact on this bit. Software attempts to clear this bit by writing a 1 to this bit position. If the PCI_EXP_STS bit went active due to an Assert PMEGPE message, then a Deassert PMEGPE message must be received prior to the software write in order for the bit to be cleared. If the bit is not cleared and the corresponding PCI_EXP_EN bit is set, the leveltriggered SCI will remain active. Note that a race condition exists where the PCI Express device sends another PME message because the PCI Express device was not serviced within the time when it must resend the message. This may result in a spurious interrupt, and this is comprehended and approved by the PCI Express specification. The window for this race condition is approximately 95-105 milliseconds. This bit is reset by RSMRST# assertion.

Bit Range	Default	Access	Field Name and Description
8	-	-	**Reserved**
7	0b	RW/1C/V	**SMBus Wake Status (SMB_WAK_STS)** This bit is set to 1 by the hardware to indicate that the wake event was caused by the PCH's SMBus logic. This could be due to either the SM Bus slave unit receiving a message or the SMBALERT# signal going active. NOTES: 1. The SMBus controller will independently cause an SMI# so this bit does not need to do so (unlike the other bits in this register). 2. This bit is set by the SMBus slave command 01h (Wake/SMI#) even when the system is in the S0 state. Therefore, to avoid an instant wake on subsequent transitions to sleep states, software must clear this bit after each reception of the Wake/SMI# command or just prior to entering the sleep state. 3. The SMBALERT_STS bit (D31:F3:I/O Offset 00h:bit 5) should be cleared by software before clearing this bit. This bit is reset by RSMRST# assertion.
6	0b	RW/1C/V	**TCOSCI Status (TCOSCI_STS)** This bit will be set to 1 by hardware when the TCO logic or Thermal Sensor logic causes an SCI. This bit can be reset by writing a one to this bit position or by RSMRST# assertion.
5:3	-	-	**Reserved**
2	0b	RW/1C/V	**Software GPE Status (SWGPE_STS)** The SWGPE_CTRL bit (bit 1 of GPE_CTRL reg) acts as a level input to this bit. This bit is reset by RSMRST# assertion.

Bit Range	Default	Access	Field Name and Description
1	0b	RW/1C/V	**Hot Plug Status (HOT_PLUG_STS)** Enables PCH to cause an SCI when the HOT_PLUG_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to hot-plug events. The following events cause HOT_PLUG_STS bit to set - Assert GPE message received from any of the PCIE ports in PCH - Assert HPGPE message received from any of the PCIE ports in PCH - Assert GPE message received downstream from processor - Assert HPGPE message received downstream from processor. This bit is reset by RSMRST# assertion.
0	-	-	**Reserved**

General Purpose Event 0 Enable [31:0] (GPE0_EN_31_0) – Offset 70

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**General Purpose Event 0 Enable [31:0] (GPE0_EN_31_0)** These bits enable the corresponding GPE0_STS[31:0] bits being set to cause an SCI and/or wake event. Note: The GPP/GPD group mapped to this GPE0_EN_31_0 is configured via GPIO_CFG.DW0 and MISCCFG.DW0. Both GPIO_CFG.DW0 and MISCCFG.DW0 must be programmed to the same value.

General Purpose Event 0 Enable [63:32] (GPE0_EN_63_32) – Offset 74

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**General Purpose Event 0 Enable [63:32] (GPE0_EN_63_32)** These bits enable the corresponding GPE0_STS[63:32] bits being set to cause an SCI and/or wake event. Note: The GPP/GPD group mapped to this GPE0_EN_63_32 is configured via GPIO_CFG.DW1 and MISCCFG.DW1. Both GPIO_CFG.DW1 and MISCCFG.DW1 must be programmed to the same value.

General Purpose Event 0 Enable [95:64] (GPE0_EN_95_64) – Offset 78

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**General Purpose Event 0 Enable [95:64] (GPE0_EN_95_64)** These bits enable the corresponding GPE0_STS[95:64] bits being set to cause an SCI and/or wake event. Note: The GPP/GPD group mapped to this GPE0_EN_95_64 is configured via GPIO_CFG.DW2 and MISCCFG.DW2. Both GPIO_CFG.DW2 and MISCCFG.DW2 must be programmed to the same value.

General Purpose Event 0 Enable [127:96] (GPE0_EN[127:96]) – Offset 7c

Note: This register is symmetrical to the General Purpose Event 0 Status [127:96] Register.

Note that GPE0_STS bits 95:0 are claimed by the GPIO register block.

Bit Range	Default	Access	Field Name and Description
30:19	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
18	0b	RW	**Wake Alarm Device Timer Enable (WADT_EN)** Used to enable the setting of the WADT_STS bit to generate Wake/SMI#/SCI. This bit is reset by DSW_PWROK de-assertion.
17	-	-	**Reserved**
16	0b	RW	**GPIO[27] Enable (LANWAKE_EN)** Used to enable the setting of the LANWAKE_STS bit to generate wake/SMI#/SCI. Host wake events from the PHY through LANWAKE cannot be disabled by clearing this bit. This bit is in the RTC well.
15	0b	RW/V	**GPIO Tier2 SCI EN (GPIO_TIER2_SCI_EN)** Used to enable the setting of GPIO_TIER2_SCI_STS to generate wake/SCI#.
14	0b	RW/V	**eSPI SCI Enable (ESPI_SCI_EN)** Used to enable the setting of the ESPI_SCI_STS bit to generate a SCI.
13	0b	RW/V	**PME_B0 Enable (PME_B0_EN)** Enables the setting of the PME_B0_STS bit to generate a wake event and/or an SCI or SMI#. This bit is reset by RTCRST# assertion.
12	0b	RW/V	**ME SCI Enable (ME_SCI_EN)** Used to enable the setting of the ME_SCI_STS bit to generate a SCI.
11	0b	RW/V	**Power Management Event Enable (PME_EN)** Enables the setting of the PME_STS to generate a wake event and/or an SCI. This bit is reset by RTCRST# assertion.
10	0b	RW/V	**Low Battery Enable (BATLOW_EN)** In Mobile Mode, this bit enables the BATLOW# signal to cause an SMI# or SCI (depending on the SCI_EN bit) when it goes low.This bit does not prevent the BATLOW# signal from inhibiting the wake event. In Desktop Mode this bit will be treated as Reserved. This bit is reset by RTCRST# assertion.

Bit Range	Default	Access	Field Name and Description
9	0b	RW/V	**PCI Express Enable (PCI_EXP_EN)** Enables PCH to cause an SCI when PCI_EXP_STS bit is set. This is used to allow the PCI Express ports, including the link to the MCH, to cause an SCI due to wake/PME events.
8:7	-	-	**Reserved**
6	0b	RW/V	**TCOSCI Enable (TCOSCI_EN)** When TCOSCI_EN and TCOSCI_STS are both set, an SCI will be generated. This bit is reset by RSMRST# assetion.
5:3	-	-	**Reserved**
2	0b	RW/V	**Software GPE Enable (SWGPE_EN)** This bit, when set to 1, enables the SW GPE function. If SWGPE_CTRL is written to a 1, hardware will set SWGPE_STS (acts as a level input) If SWGPE_STS, SWGPE_EN, and SCI_EN are all 1's, an SCI will be generated If SWGPE_STS = 1, SWGPE_EN = 1, SCI_EN = 0, and GBL_SMI_EN = 1 then an SMI# will be generated
1	0b	RW/V	**Hot Plug Enable (HOT_PLUG_EN)** Enables PCH to cause an SCI when the HOT_PLUG_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to hot-plug events. The following events cause HOT_PLUG_STS bit to set - Assert GPE message received from any of the PCIE ports in PCH - Assert HPGPE message received from any of the PCIE ports in PCH - Assert GPE message received downstream from CPU - Assert HPGPE message received downstream from CPU
0	-	-	**Reserved**

PMC Memory Mapped Registers

The PMC memory mapped registers are accessed based upon offsets from PM Base Address (PWRMBASE) defined in PCI

Device 31: Function 2.

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1910h	4	Last TSC Alarm Value[31:0] (TSC_ALARM_LO)	0h
1914h	4	Last TSC Alarm Value[63:32] (TSC_ALARM_HI)	0h
1920h	4	GPIO Configuration (GPIO_CFG)	432h
1924h	4	Global Reset Causes (GBLRST_CAUSE0)	0h
1928h	4	Global Reset Causes Register 1 (GBLRST_CAUSE1)	0h
192ch	4	Host Partition Reset Causes (HPR_CAUSE0)	0h
1020h	4	General PM Configuration A (GEN_PMCON_A)	20014000h
1024h	4	General PM Configuration B (GEN_PMCON_B)	4h
1030h	4	Configured Revision ID (CRID)	0h
1048h	4	Extended Test Mode Register 3 (ETR3)	0h
104ch	4	SET_STRAP_MSG_LOCK (SSML)	0h
1050h	4	SET_STRAP_MSG_CONTROL (SSMC)	0h
1054h	4	SET_STRAP_MSG_DATA (SSMD)	0h
1930h	4	LATENCY_LIMIT_RESIDENCY_0 (LAT_LIM_RES_0)	0h
1934h	4	LATENCY_LIMIT_RESIDENCY_1 (LAT_LIM_RES_1)	0h
1938h	4	LATENCY_LIMIT_RESIDENCY_2 (LAT_LIM_RES_2)	0h
193ch	4	SLP S0 RESIDENCY (SLP_S0_RES)	0h
1940h	4	LATENCY LIMIT CONTROL (LLC)	0h
1b24h	4	Chipset Initialization Register 324 (CIR324)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1b28h	4	Chipset Initialization Register B28 (CIRB28)	0h
10b0h	4	Configured Revision ID (CRID_UIP)	0h
10c0h	4	HSIO Power Management Configuration 1 (MODPHY_PM_CFG1)	0h
10c4h	4	HSIO Power Management Configuration 2 (MODPHY_PM_CFG2)	FFFFh
10c8h	4	HSIO Power Management Configuration 3 (MODPHY_PM_CFG3)	0h
10cch	4	HSIO Power Management Configuration 4 (MODPHY_PM_CFG4)	0h
10d0h	4	HSIO Power Management Configuration Reg 5 (MODPHY_PM_CFG5)	0h
1b40h	4	Chipset Initialization Register B40 (CIRB40)	0h
1b44h	4	Chipset Initialization Register B44 (CIRB44)	0h
1ba8h	4	Chipset Initialization Register BA8 (CIRBA8)	0h
1bach	4	Chipset Initialization Register BAC (CIRBAC)	0h
1bb0h	4	Last PM_SYNC Message [31:0] (PM_SYNC_DATA_0)	0h
1bb4h	4	Last PM_SYNC Message [63:32] (PM_SYNC_DATA_1)	0h
1bd4h	4	CWB MDID Status Register (CWBMDIDSTATUS)	0h
1bd8h	4	ACPI Control (ACTL)	0h
1be0h	4	PMC Throttling 1 (PMC_THROT_1)	0h
1be8h	4	Chipset Initialization Register 3E8 (CS_SD_CTL1)	0h
1bech	4	Chipset Initialization Register 3EC (CS_SD_CTL2)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1d00h	4	PGD Priority Agent Mapping Register 0 (PPAMR0)	0h
1d04h	4	PGD Priority Agent Mapping Register 1 (PPAMR1)	0h
1d08h	4	PGD Priority Agent Mapping Register 2 (PPAMR2)	0h
1d0ch	4	PGD Priority Agent Mapping Register 3 (PPAMR3)	0h
1d10h	4	PGD Priority Agent Mapping Register 4 (PPAMR4)	0h
1d14h	4	PGD Priority Agent Mapping Register 5 (PPAMR5)	0h
1d18h	4	PGD Priority Agent Mapping Register 6 (PPAMR6)	0h
1d1ch	4	PGD Priority Agent Mapping Register 7 (PPAMR7)	0h
1d20h	4	PGD Priority Agent Mapping Register 8 (PPAMR8)	0h
1d24h	4	PGD Priority Agent Mapping Register 9 (PPAMR9)	0h
1d28h	4	PGD Priority Agent Mapping Register 10 (PPAMR10)	0h
1d2ch	4	PGD Priority Agent Mapping Register 11 (PPAMR11)	0h
1d30h	4	PGD Priority Agent Mapping Register 12 (PPAMR12)	0h
1d34h	4	PGD Priority Agent Mapping Register 13 (PPAMR13)	0h
1d38h	4	PGD Priority Agent Mapping Register 14 (PPAMR14)	0h
1d3ch	4	PGD Priority Agent Mapping Register 15 (PPAMR15)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1d80h	4	Chipset Initialization Register 580 (CIR580)	0h
1d84h	4	PGD PG_ACK Status Register 1 (PPASR1)	0h
1d90h	4	PFET Enable Ack Register 0 (PPFEAR0)	0h
1d94h	4	PFET Enable Ack Register 1 (PPFEAR1)	0h
1da0h	4	Chipset Initialization Register DA0 (CIRDA0)	6000606h
1db0h	4	PGD Misc Control Register (PMCR)	0h
1dd0h	4	Host SW PG Control Register 1 (HSWPGCR1)	0h
1de0h	4	PGD PG_REQ Status Register 0 (PPRSR0)	0h
1de4h	4	PGD PG_REQ Status Register 1 (PPRSR1)	0h
1e20h	4	Static PG Function Disable 1 (ST_PG_FDIS1)	0h
1e24h	4	Static Function Disable Control 2 (ST_PG_FDIS2)	0h
1e28h	4	Non-Static PG Related Function Disable Register 1 (NST_PG_FDIS_1)	0h
1200h	4	Always Running Timer Value 31:0 (ARTV_31_0)	0h
1204h	4	Always Running Timer Value 31:0 (ARTV_63_32)	0h
1210h	4	Timed GPIO Control 0 (TGPIOCTL0)	0h
1220h	4	Timed GPIO 0 comparator Value 31:0 (TGPIOCOMPV0_31_0)	0h
1224h	4	Timed GPIO comparator Value 63:32 (TGPIOCOMPV0_63_32)	0h
1228h	4	Timed GPIO0 periodic Interval Value 31_0 (TGPIOPIV0_31_0)	0h
122ch	4	Timed GPIO 0 periodic Interval Value 63_32 (TGPIOPIV0_63_32)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1230h	4	Timed GPIO Time Capture register 31_0 (TGPIOTCV0_31_0)	0h
1234h	4	Timed GPIO0 Time Capture register 63_32 (TGPIOTCV0_63_32)	0h
1238h	4	Timed GPIO0 Event Counter Capture register 31_0 (TGPIOECCV0_31_0)	0h
123ch	4	Timed GPIO0 Event Counter Capture register 63_32 (TGPIOECCV0_63_32)	0h
1240h	4	Timed GPIO0 Event Counter Register 31_0 (TGPIOEC0_31_0)	0h
1244h	4	Timed GPIO0 Event Counter Register 63_32 (TGPIOEC0_63_32)	0h
1310h	4	Timed GPIO Control 1 (TGPIOCTL1)	0h
1320h	4	Timed GPIO 1 comparator Value 31:0 (TGPIOCOMPV1_31_0)	0h
1324h	4	Timed GPIO comparator Value 63:32 (TGPIOCOMPV1_63_32)	0h
1328h	4	Timed GPIO1 periodic Interval Value 31_0 (TGPIOPIV1_31_0)	0h
132ch	4	Timed GPIO 1 periodic Interval Value 63_32 (TGPIOPIV1_63_32)	0h
1330h	4	Timed GPIO Time Capture register 31_0 (TGPIOTCV1_31_0)	0h
1334h	4	Timed GPIO Time Capture register 63_32 (TGPIOTCV1_63_32)	0h
1338h	4	Timed GPIO0 Event Counter Capture register 31_0 (TGPIOECCV1_31_0)	0h
133ch	4	Timed GPIO0 Event Counter Capture register 63_32 (TGPIOECCV1_63_32)	0h
1340h	4	Timed GPIO1 Event Counter Register 31_0 (TGPIOEC1_31_0)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1344h	4	Timed GPIO Event Counter Register 63_32 (TGPIOEC1_63_32)	0h
1670h	4	ART to RTC Ratio (ART_RTC_RATIO)	0h
1800h	4	Wake Alarm Device Timer: AC (WADT_AC)	FFFFFFFFh
1804h	4	Wake Alarm Device Timer: DC (WADT_DC)	FFFFFFFFh
1808h	4	Wake Alarm Device Expired Timer: AC (WADT_EXP_AC)	FFFFFFFFh
180ch	4	Wake Alarm Device Expired Timer: DC (WADT_EXP_DC)	FFFFFFFFh
1810h	4	Power and Reset Status (PRSTS)	0h
1818h	4	Power Management Configuration Reg 1 (PM_CFG)	20h
1824h	4	PCH Power Management Status (PCH_PM_STS2)	0h
1828h	4	S3 Power Gating Policies (S3_PWRGATE_POL)	0h
182ch	4	S4 Power Gating Policies (S4_PWRGATE_POL)	0h
1830h	4	S5 Power Gating Policies (S5_PWRGATE_POL)	0h
1834h	4	DeepSx Configuration (DSX_CFG)	0h
183ch	4	Power Management Configuration Reg 2 (PM_CFG2)	0h
1848h	4	Chipset Initialization Register 48 (CIR48)	0h
184ch	4	Chipset Initialization Register 4C (CIR4C)	0h
1850h	4	Chipset Initialization Register 50 (CIR50)	0h
1854h	4	Chipset Initialization Register 54 (CIR54)	0h
1858h	4	Chipset Initialization Register 58 (CIR58)	0h
1868h	4	Chipset Initialziation Register 68 (CIR68)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1880h	4	Chipset Initialization Register 80 (CIR80)	0h
1884h	4	Chipset Initialization Register 84 (CIR84)	0h
1888h	4	Chipset Initialization Register 88 (CIR88)	0h
188ch	4	Chipset Initialization Register 8C (CIR8C)	0h
1898h	4	Chipset Initialization Register 98 (CIR98)	0h
18a8h	4	Chipset Initizaliation Register A8 (CIRA8)	0h
18ach	4	Chipset Initizaliation Register AC (CIRAC)	0h
18b0h	4	Chipset Initialization Register B0 (CIRB0)	0h
18b4h	4	Chipset Initialization Register B4 (CIRB4)	0h
18c0h	4	Chipset Initialization Register C0 (CIRC0)	0h
18c4h	4	PMSYNC Thermal Power Reporting Configuration (PMSYNC_TPR_CFG)	0h
18c8h	4	PM_SYNC Miscellaneous Configuration (PM_SYNC_MISC_CFG)	0h
18d0h	4	Chipset Initialization Register D0 (CIRD0)	0h
18d4h	4	Chipset Initialization Register D4 (CIRD4)	0h
18e0h	4	Power Management Configuration Reg 3 (PM_CFG3)	0h
18e4h	4	Chipset Initialization Register E4 (CIRE4)	0h
18e8h	4	Power Management Configuration Reg 4 (PM_CFG4)	8000h
18ech	4	CPU Early Power-on Configuration (CPU_EPOC)	0h
18fch	4	ACPI Timer Control (ACPI_TMR_CTL)	0h
1e40h	4	Capability Disable Status 1 (N_STPG_FUSE_SS_DIS_RD_1)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
1e44h	4	Capability Disable Status 2 (STPG_FUSE_SS_DIS_RD_2)	0h
10b4h	4	SLP_S0# Debug 0 (SLP_S0_DBG_0)	0h
10b8h	4	SLP_S0# Debug 1 (SLP_S0_DBG_1)	0h
10bch	4	SLP_S0# Debug 2 (SLP_S0_DBG_2)	0h
1900h	4	VR Miscellaneous Control (VR_MISC_CTL)	1000h

Last TSC Alarm Value[31:0] (TSC_ALARM_LO) – Offset 1910

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO/V	**Last TSC Alarm Value [31:0] (TSC_ALARM_VAL_LO)** This field contains bits 31:0 of the last TSC alarm value received from the CPU. This field is reset by PLTRST# assertion.

Last TSC Alarm Value[63:32] (TSC_ALARM_HI) – Offset 1914

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO/V	**Last TSC Alarm Value [63:32] (TSC_ALARM_VAL_HI)** This field contains bits 63:32 of the last TSC alarm value received from the CPU. This field is reset by PLTRST# assertion.

GPIO Configuration (GPIO_CFG) – Offset 1920

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
11:8	0100b	RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2)** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 1h = GPP_B[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 2h = GPP_G[7:0] mapped to GPE[71:64]; GPE[95:72] not used. 3h = Reserved. 4h = GPP_D[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 5h = GPP_F[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 6h = GPP_H[23:0] mapped to GPE[87:64]; GPE[95:88] not used. 7h - 9h = Reserved Ah = GPD[11:0] mapped to GPE[75:64]; GPE[95:76] not used Bh - Ch = Reserved Dh = GPP_C[23:0] mapped to GPE[87:64]; GPE[95:88] not used. Eh = GPP_E[23:0] mapped to GPE[87:64]; GPE[95:88] not used. Fh = Reserved
7:4	0011b	RW	

Bit Range	Default	Access	GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1) Field Name and Description
			This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 1h = GPP_B[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 2h = GPP_G[7:0] mapped to GPE[7:0]; GPE[31:8] not used. 3h = Reserved. 4h = GPP_D[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 5h = GPP_F[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 6h = GPP_H[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 7h - 9h = Reserved Ah = GPD[11:0] mapped to GPE[11:0]; GPE[31:12] not used Bh - Ch = Reserved Dh = GPP_C[23:0] mapped to GPE[23:0]; GPE[31:24] not used Eh = GPP_E[23:0] mapped to GPE[23:0]; GPE[31:24] not used Fh = Reserved

Bit Range	Default	Access	Field Name and Description
3:0	0010b	RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0)** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_A[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 1h = GPP_B[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 2h = GPP_G[7:0] mapped to GPE[7:0]; GPE[31:8] not used. 3h = Reserved. 4h = GPP_D[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 5h = GPP_F[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 6h = GPP_H[23:0] mapped to GPE[23:0]; GPE[31:24] not used. 7h - 9h = Reserved Ah = GPD[11:0] mapped to GPE[11:0]; GPE[31:12] not used Bh - Ch = Reserved Dh = GPP_C[23:0] mapped to GPE[23:0]; GPE[31:24] not used Eh = GPP_E[23:0] mapped to GPE[23:0]; GPE[31:24] not used Fh = Reserved

Global Reset Causes (GBLRST_CAUSE0) – Offset 1924

This register logs causes of host partition resets.

Bit Range	Default	Access	Field Name and Description
30:21	-	-	**Reserved**
20	0b	RW/1C/V	**Over-Clocking WDT Expiration In ICC Survivability Mode (OC_WDT_EXP_ICCSURV)** This bit is set to 1 by hardware when a global reset is triggered by the expiration of the over-clocking watchdog timer while running in a mode that has ICC survivability impact (OC_WDT_ICCSURV=1). This bit is reset by DSW_PWROK de-assertion.

Bit Range	Default	Access	Field Name and Description
19	0b	RW/1C/V	**Over-Clocking WDT Expiration In Non-ICC Survivability Mode (OC_WDT_EXP_NO_ICCSURV)** This bit is set to 1 by hardware when a global reset is triggered by the expiration of the over-clocking watchdog timer while running in a mode that does not have ICC survivability impact (OC_WDT_ICCSURV=0). This bit is reset by DSW_PWROK de-assertion.
18	-	-	**Reserved**
17	0b	RW/1C/V	**Intel ME HW Uncorrectable Error (ME_UNCOR_ERR)** This bit is set to '1' by hardware when a global reset is triggered by Intel ME hardware due to the detection of an uncorrectable ECC or parity error on a data read from one of its SRAMs. This bit is reset by DSW_PWROK de-assertion.
16	0b	RW/1C/V	**CPU Thermal Runaway Watchdog Timer (CPU_THRM_WDT)** This bit is set to '1' by hardware when a global reset is triggered by the expiration of the CPU Thermal Runaway Watchdog Timer.
15:13	-	-	**Reserved**
12	0b	RW/1C/V	**SYS_PWROK Failure (SYSPWR_FLR)** This bit is set to '1' by hardware when a global reset is triggered by an unexpected loss of SYS_PWROK. This bit is reset by DSW_PWROK de-assertion.
11	0b	RW/1C/V	**PCH_PWROK Failure (PCHPWR_FLR)** This bit is set to '1' by hardware when a global reset is triggered by an unexpected loss of PCH_PWROK. This bit is reset by DSW_PWROK de-assertion.
10	0b	RW/1C/V	**PMC Firmware Global Reset (PMC_FW)** This bit is set to '1' by hardware when a global reset is triggered by a request from PMC firmware (i.e. a write of '1' to the GBLRST_CTL.TRIG_GBL bit).

Bit Range	Default	Access	Field Name and Description
9	0b	RW/1C/V	**Intel Management Engine Watchdog Timer (ME_WDT)** This bit is set to '1' by hardware when a global reset is triggered by the second expiration of the Intel® Management Engine watchdog timer. This bit is reset by DSW_PWROK de-assertion.
8	0b	RW/1C/V	**Power Management Controller Watchdog Timer (PMC_WDT)** This bit is set to '1' by hardware when a global reset is triggered by the second expiration of the PMC watchdog timer. This bit is reset by DSW_PWROK de-assertion.
7	-	-	**Reserved**
6	0b	RW/1C/V	**ME-Initiated Global Reset (ME_GBL)** This bit is set to '1' by hardware when a global reset is triggered by Intel ME FW. This bit is reset by DSW_PWROK de-assertion.
5	0b	RW/1C/V	**CPU Thermal Trip (CPU_TRIP)** This bit is set to '1' by hardware when a global reset is triggered by a CPU thermal trip event (i.e. an assertion of the THRMTRIP# pin).
4	0b	RW/1C/V	**ME-Initiated Power Button Override (ME_PBO)** This bit is set to '1' by hardware when a global reset is triggered by ME-Initiated Power Button Override. This bit is reset by DSW_PWROK de-assertion.
3	0b	RW/1C/V	**ICH Catastrophic Temperature Event (ICH_CAT_TMP)** This bit is set to '1 by hardware when a global reset is triggered by a catastrophic temperature event from the ICH internal thermal sensor.
2	0b	RW/1C/V	**PMC SUS RAM Uncorrectable Error (PMC_UNC_ERR)** This bit is set to '1' by hardware when a global reset is triggered due to an uncorrectable parity error on a data read from one of the PMC SUS well register files. This bit is reset by DSW_PWROK de-assertion.

Bit Range	Default	Access	Field Name and Description
1	0b	RW/1C/V	**Power Button Override (PB_OVR)** This bit is set to '1' by hardware when a global reset is triggered by a power button override (i.e. an assertion of the PWRBTN# pin for 5 seconds). This bit is reset by DSW_PWROK de-assertion.
0	-	-	**Reserved**

Global Reset Causes Register 1 (GBLRST_CAUSE1) – Offset 1928

This register logs causes of host partition resets.

Bit Range	Default	Access	Field Name and Description
30:6	-	-	**Reserved**
5	0b	RW/1C/V	**ME Set Power Button Status (ME_SET_PBO_STS)** If this bit is set, the cause of the previous global reset was ME FW setting the power button override status. This bit is reset by DSW_PWROK de-assertion.
4	-	-	**Reserved**
3	0b	RW/1C/V	**Host SMBus Message (HSMB_MSG)** If this bit is set, the cause of the previous global reset was a global reset request received over the host SMBus interface.
2	0b	RW/1C/V	**Host Partition Reset Promotion (HOST_RST_PROM)** If this bit is set, the cause of the previous global reset was a host partition reset that was promoted to a global reset either due to ME or host policy. This bit is reset by DSW_PWROK de-assertion.
1	0b	RW/1C/V	**Sx Entry Timeout (SX_ENTRY_TIMEOUT)** If this bit is set, the cause of the previous global reset was an expiration of the timer that runs during Sx entry. This bit is reset by DSW_PWROK de-assertion.

Bit Range	Default	Access	Field Name and Description
0	0b	RW/1C/V	**Host Partition Reset Timeout (HOST_RESET_TIMEOUT)** If this bit is set, the cause of the previous global reset was an expiration of the timer that runs during host partition resets. This bit is reset by DSW_PWROK de-assertion.

Host Partition Reset Causes (HPR_CAUSE0) – Offset 192c

This register logs causes of host partition resets.

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13	0b	RO/V	**Host SMBUS Host Reset With Power Cycle (HSMB_HRPC)** SMBus initiated host partition reset with power cycle.
12	0b	RO/V	**Host SMBUS Host Reset Without Power Cycle (HSMB_HR)** SMBus initiated host partition reset without power cycle.
11	-	-	**Reserved**
10	0b	RO/V	**ME-Initiated Host Reset With Power Down (MI_HRPD)** ME initiated host reset with power down.
9	0b	RO/V	**ME-Initiated Host Reset With Power Cycle (MI_HRPC)** ME initiated host reset with power cycle.
8	0b	RO/V	**ME-Initiated Host Reset Without Power Cycle (MI_HR)** ME initiated host reset without power cycle.
7	-	-	**Reserved**
6	0b	RO/V	**Host TCO Watchdog Timer Second Expiration (TCO_WDT)** Host TCO watchdog timer reached zero for the second time.

Bit Range	Default	Access	Field Name and Description
5:3	-	-	**Reserved**
2	0b	RO/V	**SYS_RESET# (SYSRST_ES)** Assertion of the SYS_RESET# pin after the 16 ms HW debounce.
1	0b	RO/V	**Write to CF9 (CF9_ES)** This bit will be set when Host software writes a value of 6h or Eh to the CF9 register. Note: The shutdown special cycle from the CPU will also set this bit.
0	-	-	**Reserved**

General PM Configuration A (GEN_PMCON_A) – Offset 1020

Bit Range	Default	Access	Field Name and Description
30	0b	RW	**DC PHY Power Disable (DC_PP_DIS)** This bit determines the Host software contribution to whether the LAN PHY remains powered in Sx/MOFF or DeepSx while on battery.
29	1b	RW	**Deep-Sx PHY Power Disable (DSX_PP_DIS)** This bit determines the Host software contribution to whether the LAN PHY remains powered in DeepSx. If this bit is cleared, for the PHY to be powered in deep-Sx state, SX_PP_EN must be set to 1.
28	0b	RW	**After G3 PHY Power Enable (AG3_PP_EN)** This bit determines the Host software contribution to whether the LAN PHY is powered up after exiting G3 (to either Sx/MOFF or DeepSx).
27	0b	RW	**Sx PHY Power Enable (SX_PP_EN)** This bit determines the Host software contribution to whether the LAN PHY remains powered in an Sx/MOFF state that was entered from S0 (rather than from G3).
26:25	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
24	0b	RW/1C/V	**Global Reset Status (GBL_RST_STS)** This bit is set after a global reset (not G3 or DeepSx) occurs. See the GEN_PMCON_B.HOST_RST_STS bit for potential usage models.
23	0b	RW	**DRAM Initialization Scratchpad Bit (DISB)** This bit does not effect hardware functionality in any way. It is provided as a scratchpad bit that is maintained through main power well resets and CF9h-initiated resets. BIOS is expected to set this bit prior to starting the DRAM initialization sequence and to clear this bit after completing the DRAM initialization sequence. BIOS can detect that a DRAM initialization sequence was interrupted by a reset by reading this bit during the boot sequence. If the bit is 1, then the DRAM initialization was interrupted. This bit is reset by the assertion of the RSMRST# pin.
22	-	-	**Reserved**
21	0b	RO/V	**Memory Placed in Self-Refresh (MEM_SR)** This bit will be set to 1 if DRAM should have remained powered and held in Self-Refresh through the last power state transition (i.e. the last time the system left S0). The scenarios where this should be the case are: - successful S3 entry & exit - successful Host partition reset without power cycle These scenarios both involve a handshake between the PCH and the CPU. The acknowledge from the CPU back to the PCH is assumed to imply that memory was successfully placed into Self-Refresh (the PCH has no way to verify whether that actually occurred). This bit will be cleared whenever the PCH begins a transition out of S0.
20:19	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
18	0b	RW/1C/V	**Minimum SLP_S4# Assertion Width Violation Status (MS4V)** Hardware sets this bit when the SLP_S4# assertion width is less than the time programmed in the SLP_S4# Minimum Assertion Width field (D31.F0.A4h.5:4). The PCH begins the timer when SLP_S4# pin (including ME override logic) is asserted during S4/S5 entry, or when the RSMRST# input is deasserted during SUS well power-up. The status bit is cleared by software writing a 1 to the bit. Note that this bit is functional regardless of the value in the SLP_S4# Assertion Stretch Enable and the Disable SLP_X Stretching After SUS Power Failure bits. This bit is reset by the assertion of the RSMRST# pin, but can be set in some cases before the default value is readable.
17	0b	RW	**Allow L1.LOW Entry with OPI Voltage On (ALLOW_L1LOW_OPI_ON)** When this bit is 0, the PMC only allows L1.LOW entry if the OPI voltage is off. When this bit is 1, the PMC allows L1.LOW entry regardless of whether the OPI voltage is on/off.
16	1b	RW/1C	**SUS Well Power Failure (SUS_PWR_FLR)** This bit is set to '1' whenever SUS well power is lost, as indicated by RSMRST# assertion. Software writes a 1 to this bit to clear it. This bit is in the SUS well, and defaults to '1' based on RSMRST# assertion (not cleared by any type of reset).

Bit Range	Default	Access	Field Name and Description
15	0b	RW	**PME B0 S5 Disable (PME_B0_S5_DIS)** When set to '1', this bit blocks wake events from PME_B0_STS in S5, regardless of the state of PME_B0_EN. When cleared (default), wake events from PME_B0_STS are allowed in S5 if PME_B0_EN = '1'. Wakes from power states other than S5 are not affected by this policy bit. The net effect of setting PME_B0_S5_DIS = '1' is described by the truth table below: Y = Wake N = Don't wake B0 = PME_B0_EN OV = WOL Enable Override B0/OV | S1/S3/S4 | S5 00 | N | N 01 | N | Y (LAN only) 11 | Y (all PME B0 sources) | Y (LAN only) 10 | Y (all PME B0 sources) | N This bit is cleared by the RTCRST# pin.
14	1b	RW/1C	**PWR_FLR (PF)** 1 = Indicates that the trickle current (from the main battery or trickle supply) was removed or failed. 0 = Indicates that the trickle current has not failed since the last time the bit was cleared. Software writes a 1 to this bit to clear it. This bit is in the DSW well, and defaults to '1' based on DSW_PWROK deassertion (not cleared by any type of reset).
13	0b	RW	**Allow L1.LOW Entry with CPU BCLK REQ Asserted (ALLOW_L1LOW_BCLKREQ_ON)** When this bit is 0, the PMC only allows L1.LOW entry if the CPUs BCLK request is de-asserted. When this bit is 1, the PMC allows L1.LOW entry regardless of whether the CPUs BCLK request is asserted/de-asserted.

Bit Range	Default	Access	Field Name and Description
12	0b	RW/L	**Disable SLP_X Stretching After SUS Well Power Up (DIS_SLP_X_STRCH_SUS_UP)** 1 = All SLP_* pin stretching is disabled when powering up after a SUS well power loss. 0 = SLP_* stretching will be performed after SUS power failure as enabled in various other fields. Note that if this bit is a 0, SLP_* stretch timers start on SUS well power up (the PCH has no ability to count stretch time while the SUS well is powered down). Setting this bit can therefore prevent long delays after SUS power loss, while still allowing for the full power cycling during S3, S4 and S5 states. If the platform guarantees minimum SUS power down residence in other ways, an additional PCH-induced delay is not needed or wanted. Note: This policy bit has a different effect on SLP_SUS# stretching than on the other SLP_* pins, since SLP_SUS# is the control signal for one of the scenarios where SUS well power is lost (DeepSx). The effect of setting this bit to '1' on: - SLP_S3#, SLP_S4#, SLP_A# and SLP_LAN# stretching: disabled after any SUS power loss - SLP_SUS# stretching: disabled after G3, but no impact on DeepSx This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by the RTCRST# pin.

Bit Range	Default	Access	Field Name and Description
11:10	00b	RW/L	**SLP_S3# Minimum Assertion Width (SLP_S3_MIN_ASST_WDTH)** This 2-bit value indicates the minimum assertion width of the SLP_S3# signal to guarantee that the Main power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00: 60 usec 01: 1 ms 10: 50 ms 11: 2 sec This field is not writable when the SLP_Sx# Stretching Policy Lock- Down bit is set. This bit is cleared by the RSMRST# pin.

Bit Range	Default	Access	Field Name and Description
9	0b	RW/1C/V	**Host Reset Status (HOST_RST_STS)** This bit is set by hardware when a host partition reset (not a global reset, DeepSx, or G3) occurs. This bit is an optional tool to help BIOS determine when a host partition reset might have collided with a wake from a valid sleep state. A possible usage model would be to consult and then write a '1' to clear this bit during the boot flow before determining what action to take based on reading PM1_STS.WAK_STS = '1'. If HOST_RST_STS = '1' and/or GEN_PMCON_A.GBL_RST_STS = '1', the cold reset boot path could be followed rather than the resume path, regardless of the setting of WAK_STS. This bit does not affect PCH operation in any way, and can therefore be left set if BIOS chooses not to use it.
8	0b	RW/L	**ESPI SMI Lock (ESPI_SMI_LOCK)** When this bit is set, writes to the ESPI_SMI_EN bit will have no effect. Once the ESPI_SMI_LOCK bit is set, writes of 0 to ESPI_SMI_LOCK bit will have no effect.
7:6	-	-	**Reserved**
5:4	00b	RW/L	

Bit Range	Default	Access	Field Name and Description
			SLP_S4# Minimum Assertion Width (S4MAW) This 2-bit value indicates the minimum assertion width of the SLP_S4# signal to guarantee that the DRAMs have been safely power-cycled. This value may be modified per platform depending on DRAM types, power supply capacitance, etc. Valid values are: 11: 1 second 10: 2 seconds 01: 3 seconds 00: 4 seconds This value is used in two ways: 1. If the SLP_S4# assertion width is ever shorter than this time, a status bit (D31.F0.A2h.2) is set for BIOS to read when S0 is entered 2. If enabled by bit 3 in this register, the hardware will prevent the SLP_S4# signal from deasserting within this minimum time period after asserting. Note that the logic that measures this time is in the suspend power well. Therefore, when leaving a G3 or DeepSx state, the minimum time is measured from the deassertion of the internal suspend well reset (unless the Disable SLP_X Stretching After SUS Power Failure bit is set). This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. RTCRST# forces this field to the conservative default state (00b).
3	0b	RW/L	**SLP_S4# Assertion Stretch Enable (S4ASE)** When set to 1, the SLP_S4# pin (which includes the ME override logic) will minimally assert for the time specified in bits 5:4 of this register. When 0, the minimum assertion time for SLP_S4# is the same as the timing defined in the Platform Design Guide. This bit is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by RTCRST#.

Bit Range	Default	Access	Field Name and Description
2:1	00b	RW	**Period SMI Select (PER_SMI_SEL)** Software sets these bits to control the rate at which the periodic SMI# is generated: 00 = 64 seconds (default) 01 = 32 seconds 10 = 16 seconds 11 = 8 seconds Tolerance for the timer is +/- 1 second.
0	0b	RW	**AFTERG3_EN (AG3E)** Determines what state to go to when power is reapplied after a power failure (G3 state). 0 = System will return to an S0 state (boot) after power is re-applied. 1 = System will return to the S5 state (except if it was in S4, in which case it will return to S4-like state). In the S5 state, the only enabled wake-up event is the Power Button or any enabled wake event that was preserved through the power failure. This bit is in the RTC well.

General PM Configuration B (GEN_PMCON_B) – Offset 1024

Bit Range	Default	Access	Field Name and Description
30:19	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
18	0b	RW/L	**SLP_Sx# Stretching Policy Lock-Down (SLPSX_STR_POL_LOCK)** When set to 1, this bit locks down the following fields: - GEN_PMCON.DIS_SLP_X_STRCH_SUSPF - GEN_PMCON.SLP_S3_MIN_ASST_WDTH - GEN_PMCON.S4MAW - GEN_PMCON.S4ASE - PM_CFG.SLP_A_MIN_ASST_WDTH - PM_CFG.SLP_LAN_MIN_ASST_WDTH - PM_CFG.PWR_CYC_DUR Those bits become read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset. This lockdown bit is available in both desktop and mobile.
17	-	-	**Reserved**
16	0b	RW/L	**PM_DATA_BAR Disable (PM_DATA_BAR_DIS)** When set t0 1, this bit disables all accesses to the MMip range pointed to by the PM_DATA_BAR. THis does not affect the BAR value itself, which can still be changed after this bit is set. But once this bit is set, PMC will drop writes to the data region pointed to by PM_DATA_BAR and reads will return 0. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset.

Bit Range	Default	Access	Field Name and Description
15:14	-	-	**Reserved**
13	0b	RW	**WOL Enable Override (WOL_EN_OVRD)** When this bit is set to 1, the integrated LAN is enabled to wake the system from S5 regardless of the value in the PME_B0_EN bit in the GPE0_EN register. This allows the system BIOS to enable Wake-On-LAN regardless of the policies selected through the operating system. This bit is maintained in the RTC power well, therefore permitting WOL following a surprise power failure even in cases in which the system may have been running in S0 without the PME Enables set. (Note that the LAN NVRAM configuration must support WOL after SUS power loss.) When this bit is cleared to 0, the wake-on-LAN policies are determined by OS-visible bits. This bit has no effect on wakes from S1, S3, or S4. This bit is cleared by the RTCRST# pin
12:11	-	-	**Reserved**
10	0b	RW	**BIOS PCI Express Enable (BIOS_PCI_EXP_EN)** This bit acts as a global enable for the SCI associated with the PCI express ports. If this bit is not set, then the various PCI Express ports cannot cause the PCI_EXP_STS bit to go active.

Bit Range	Default	Access	Field Name and Description
9	0b	RO/V	**Power Button Level (PWRBTN_LVL)** This read-only bit indicates the current state of the PWRBTN# signal. 1= High, 0 = Low. The value reflected in this bit is dependent upon PM_CFG1.PB_DB_MODE. The PB_DB_MODE bit's value causes the following behavior: - '0': PWRBTN_LVL is taken from the debounced PWRBTN# pin value that is seen at the output of a 16ms debouncer. - '1': PWRBTN_LVL is taken from the raw PWRBTN# pin (before the debouncer).
8:5	-	-	**Reserved**
4	0b	RW/L	**SMI Lock (SMI_LOCK)** When this bit is set, writes to the GLB_SMI_EN bit will have no effect. Once the SMI_LOCK bit is set, writes of 0 to SMI_LOCK bit will have no effect (i.e. once set, this bit can only be cleared by RSMRST#).
3	-	-	**Reserved**
2	1b	RW	**RTC_PWR_STS (RPS)** The PCH will set this bit to 1 when RTCRST# indicates a weak or missing battery. The bit will remain set until the software clears it by writing a 0 back to this bit position. This bit is not cleared by any type of reset.
1:0	-	-	**Reserved**

Configured Revision ID (CRID) – Offset 1030

Configured revision ID Register

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**CRID Lock (CRID_LK)** BIOS writes to this bit to lock this register (a specific lock bit is preferable over a write-based self-lock for the RID_SEL field). When this bit is written to 1, the entire register becomes RO (writes have no effect, reads return actual value) until the next assertion of RSMRST#.
30:2	-	-	**Reserved**
1:0	0h	RW/L	**RID Select (RID_SEL) (rid_sel)** Software writes this field to select Revision ID reflected in PCI Config space. The decoding is: 00 - Revision ID 01 - CRID 0 10 - CRID 1 11 - CRID 2 Once written, this field can only be cleared by RSMRST#. BIOS should write to this bit on all boots, (HOST_RST/platform.)

Extended Test Mode Register 3 (ETR3) – Offset 1048

This register resides in the primary well.

Bit Range	Default	Access	Field Name and Description
31	0b	RW/V/L	**CF9h Lockdown (CF9LOCK)** When set, this bit will lock the CF9h Global Reset bit and this register. This register is reset by a CF9h reset.
30:21	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
20	0b	RW/L	**CF9h Global Reset (CF9GR)** 1 = a CF9h write of 6h or Eh will cause a Global Reset of both the Host and the ME partitions. 0 = a CF9h write of 6h or Eh will only reset the Host partition. It is recommended that BIOS should set this bit early on in the boot sequence, and then clear it and set the CF9LOCK bit prior to loading the OS in both an ME Enabled and a ME Disabled system. This register is locked by the CF9 Lockdown (CF9LOCK) bit. This register is not reset by a CF9h reset.
19:0	-	-	**Reserved**

SET_STRAP_MSG_LOCK (SSML) – Offset 104c

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0b	RW/L	**Set_Strap Lock (SSL)** When set to 1, all of SSML, SSMC and SSMD is locked, including this Lock bit. Note that this bit is reset on host partition reset

SET_STRAP_MSG_CONTROL (SSMC) – Offset 1050

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0b	RW/L	**Set_Strap Mux Select (SSMS)** When set to 1, the Set strap message bits [47:32] come from the Set_Strap Msg Data register. This bit is reset by the RSMRST# pin only. When 0, the Set-Strap data continues to come from the soft straps themselves.This register field is locked by the Set Strap Lock (SSML.SSL) bit.

SET_STRAP_MSG_DATA (SSMD) – Offset 1054

This register is used to provide a BIOS programmable sticky register which contains data that will be used in the Set-Strap type 1 msg on subsequent resets. The bits in the message control certain CPU features, for which see the CPU spec. These bits are in the resume well, so only reset on G3. The usage model is that on each reset BIOS will check the state of the CPU. If the state is correct, then BIOS continues. If not, then BIOS writes the SSMD and SSMC registers and does a CF9 reset. On the reset the value of what was written to SSMD takes effect. Note that some mobile platforms force G3 on S5 requests. For those platforms, if the user/BIOS wants to have these bits set, there will be 2 resets on every power-on. If the platform accepts the default of 0 for these controls, then there is only one reset. The bits are in DSW and not RTC well because this allows a user upgrade, assuming the user unplugged the system before doing the upgrade, to revert to a setting of 0. This should reduce any interoperability concerns regarding user upgrades. The DSW bits are all cleared by DSW_PWROK, and must not be cleared by CF9h resets.

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0b	RW/L	**Set_Strap DATA (SSD)** When SSMS is 1, then this data is sent in the Set-Strap msg Type 1 upon reset. This data is sent i//n the 2nd DW of data, bits 15:0. This register field is locked by the Set Strap Lock SSML.SSL bit.

LATENCY_LIMIT_RESIDENCY_0 (LAT_LIM_RES_0) – Offset 1930

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO/V	**LATENCY_LIMIT_RESIDENCY (LLR0)** This field contains the amount of time (in 100us granularity) for the corresponding 0/1/2 counter in the LATENCY_LIMIT_CONTROL register that the appropriate counter is limiting the memory LTR request to the CPU. Note that this counter can wrap and that should not be of any concern. This register will reset to 0 anytime the corresponding enable for the register transitions from a 0->1. Note that on a 1->0 transition, the counter should hold its previous value

LATENCY_LIMIT_RESIDENCY_1 (LAT_LIM_RES_1) – Offset 1934

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RO/V	**LATENCY_LIMIT_RESIDENCY (LLR1)** This field contains the amount of time (in 100us granularity) for the corresponding 0/1/2 counter in the LATENCY_LIMIT_CONTROL register that the appropriate counter is limiting the memory LTR request to the CPU. Note that this counter can wrap and that should not be of any concern. This register will reset to 0 anytime the corresponding enable for the register transitions from a 0->1. Note that on a 1->0 transition, the counter should hold its previous value

LATENCY_LIMIT_RESIDENCY_2 (LAT_LIM_RES_2) – Offset 1938

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RO/V	**LATENCY_LIMIT_RESIDENCY (LLR2)** This field contains the amount of time (in 100us granularity) for the corresponding 0/1/2 counter in the LATENCY_LIMIT_CONTROL register that the appropriate counter is limiting the memory LTR request to the CPU. Note that this counter can wrap and that should not be of any concern. This register will reset to 0 anytime the corresponding enable for the register transitions from a 0->1. Note that on a 1->0 transition, the counter should hold its previous value

SLP S0 RESIDENCY (SLP_S0_RES) – Offset 193c

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RO/V	**RESIDENCY_IN_S0 (RESIDENCY_IN_S0)** This field contains the amount of time that the SLP_S0 has been asserted before. Note that this counter can wrap and that should not be of any concern. It will also count in 100us granularity

LATENCY LIMIT CONTROL (LLC) – Offset 1940

Bit Range	Default	Access	Field Name and Description
30:23	-	-	**Reserved**
22	0b	RW	**CTR2_ENABLE (CTR2_ENABLE)** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0
21	0b	RW	**CTR2_EA_CTL (CTR2_EA_CTL)** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0
20:16	0h	RW	

Bit Range	Default	Access	Field Name and Description
			CTR2_DEVICE (CTR2_DEVICE) Encoding of the LTR device to be monitored 0 - PCIe Controller A 1 - PCIe Controller B 2 - PCIe Controller C 3 - SATA 4 - GbE 5 - XHCI 6 - ME 7 - Reserved 8 - HD Audio 9 - ESPI 10 - I2C, UART, GSPI 11-13 - Reserved 14 - SCC 15 - ISH 16 - CNVi
15	-	-	**Reserved**
14	0b	RW	**CTR1_ENABLE (CTR1_ENABLE)** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0

Bit Range	Default	Access	Field Name and Description
13	0b	RW	**CTR1_EA_CTL (CTR1_EA_CTL)** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0

Bit Range	Default	Access	Field Name and Description
12:8	0h	RW	**CTR1_DEVICE (CTR1_DEVICE)** Encoding of the LTR device to be monitored 0 - PCIe Controller A 1 - PCIe Controller B 2 - PCIe Controller C 3 - SATA 4 - GbE 5 - XHCI 6 - ME 7 - Reserved 8 - HD Audio 9 - ESPI 10 - I2C, UART, GSPI 11-13 - Reserved 14 - SCC 15 - ISH

Bit Range	Default	Access	Field Name and Description
7	0b	RW	Reserved
6	0b	RW	**CTR0_ENABLE (CTR0_ENABLE)** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0
5	0b	RW	**CTR0_EA_CTL (CTR0_EA_CTL)** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0

Bit Range	Default	Access	Field Name and Description
4:0	0h	RW	**CTR0_DEVICE (CTR0_DEVICE)** Encoding of the LTR device to be monitored 0 - PCIe Controller A 1 - PCIe Controller B 2 - PCIe Controller C 3 - SATA 4 - GbE 5 - XHCI 6 - ME 7 - Reserved 8 - HD Audio 9 - ESPI 10 - I2C, UART, GSPI 11-13 - Reserved 14 - SCC 15 - ISH

Chipset Initialization Register 324 (CIR324) – Offset 1b24

BIOS may program this register.

Chipset Initialization Register B28 (CIRB28) – Offset 1b28

BIOS may program this register.

Configured Revision ID (CRID_UIP) – Offset 10b0

Configured revision ID Register

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0b	RW/V	**CRID Update in Progress (CRID_UIP)** PMC HW sets this bit to indicate that SetID broadcast flow has been requested by BIOS. This bit is cleared by PMC FW only when the completion/s for the multicast non-posted SetIDVal message is received by PMC. BIOS is required to read this bit as cleared before writing to the CRID register (to request a CRID update). BIOS is also required to poll on reads to this bit until it sees the bit as cleared after BIOS has written to the CRID register. 0 Any previously requested CRID Update is complete. 1 the most recently requested CRID update is still in progress.

HSIO Power Management Configuration 1 (MODPHY_PM_CFG1) – Offset 10c0

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW	**HSIO Lane S0 SUS Well Power Gating Policy [15:0] (MLS0SWPGP)** This is a bit per lane that controls SUS Well Power Gating for a HSIO lane to be used for S0 and S0ix. Bit 0: Corresponds to HSIO Lane 0 Bit 1: Corresponds to HSIO Lane 1 Bit 2: Corresponds to HSIO Lane 2 : : Bit 15: Corresponds to HSIO Lane 15 For each lane: 0: Lane power gating not permitted in S0. 1: Lane power gating is permitted in S0. Note that strap information/PCIe Lane reversal information will be factored by BIOS when programming these bits in the configuration registers. Note that it is not allowed for SW programming to have a bit location to be 1 in this field and the corresponding bit position to be 0 in MLSXSWPGP

HSIO Power Management Configuration 2 (MODPHY_PM_CFG2) – Offset 10c4

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
15:0	FFFFh	RW	**HSIO Lane Sx SUS Well Power Gating Policy [15:0] (MLSXSWPGP)** This is a bit per lane that controls SUS Well Power Gating for a HSIO lane when system is in Sx. Bit 0: Corresponds to HSIO Lane 0 Bit 1: Corresponds to HSIO Lane 1 Bit 2: Corresponds to HSIOLane 2 : : Bit 15: Corresponds to HSIO Lane 15 For each lane: 0: Lane power gating not permitted in Sx. 1: Lane power gating is permitted in Sx. Note that strap information/PCIe Lane reversal information will be factored by BIOS when programming these bits in the configuration registers. For ease of PMC implementation, this field will be used to manage Sx policies even in S0. In other words, the earlier restriction that BIOS does not have to program this field if MLSPDDGE is 1 does not apply any more. BIOS shall set this field appropriately for all cases.

HSIO Power Management Configuration 3 (MODPHY_PM_CFG3) – Offset 10c8

This register contains misc. fields used to configure the PCH's power management behavior with respect to the HSIO.

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**C10 qualifier for MPHY power gating (C10_QUAL_MPHYPG)** C10 qualification for MPHY power gating 1: C10 is not required for mPHY Sus power gating 0: C10 is required for mPHY Sus power gating

HSIO Power Management Configuration 4 (MODPHY_PM_CFG4) – Offset 10cc

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29:0	0000000h	RW	**ASL Over-rides (ASLOR)** This field provides ASL code to take over SPD power gating control. If ASL code sets a bit corresponding to a controller, it implies that PMC shall ignore any other inputs from that controller and assume that the controller is ready for SPD power gating. 0 in a bit position: Use HW interfaces for the controller to manage SPD gating/wake-up. 1 in a bit position: Ignore HW interfaces for the controller, rely only on MSPDRTReq field thats managed by ASL code. Bit 0: Corresponds to PCIe Controller A, Function 0 Bit 1: Corresponds to PCIe Controller A, Function 1 Bit 2: Corresponds to PCIe Controller A, Function 2 Bit 3: Corresponds to PCIe Controller A, Function 3 Bit 4: Corresponds to PCIe Controller B, Function 0 Bit 5: Corresponds to PCIe Controller B, Function 1 Bit 6: Corresponds to PCIe Controller B, Function 2 Bit 7: Corresponds to PCIe Controller B, Function 3 Bit 8: Corresponds to PCIe Controller C, Function 0 Bit 9: Corresponds to PCIe Controller C, Function 1

Bit Range	Default	Access	Field Name and Description
			Bit 10: Corresponds to PCIe Controller C, Function 2 Bit 11: Corresponds to PCIe Controller C, Function 3 Bit 12: Corresponds to SATA Controller Bit 13: Corresponds to Gbe Controller Bit 14: Corresponds to xHCI Controller Bit 15: Corresponds to xDCI Controller Bit 16: Reserved Bit 17: Corresponds to PCIe Controller D, Function 0 Bit 18: Corresponds to PCIe Controller D, Function 1 Bit 19: Corresponds to PCIe Controller D, Function 2 Bit 20: Corresponds to PCIe Controller D, Function 3 Bit 21: Corresponds to PCIe Controller E, Function 0 Bit 22: Corresponds to PCIe Controller E, Function 1 Bit 23: Corresponds to PCIe Controller E, Function 2 Bit 24: Corresponds to PCIe Controller E, Function 3 Bit 25: Corresponds to DMI Controller Others: Reserved This field is going to be used in conjunction with MSPDRTReq and MSPDRTRAck fields above. If ASL code intends to over-ride HW decisions, it will set the corresponding bit for a controller/function to 1 in ASLOR and use MSPDRTReq bits to power-up/power-down SPD.

HSIO Power Management Configuration Reg 5 (MODPHY_PM_CFG5) – Offset 10d0

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29:0	0000000 0h	RW	**Controller SPD RTD3 Request (MSPDRTREQ)** This field represents ASL code trigger request for ModPHY SPD gating. If this bit is set (to 1) for a controller, it implies that ASL code provides consent for SPD to be

Bit Range	Default	Access	Field Name and Description
			gated for the corresponding controllers lanes. Note that this bit could also be more statically used by BIOS to set this to 1 for a controller where SPD will only be managed through other interfaces implying ASL code does not exist for a controller. This is not a POR mode of operation if a function is enabled ASL code will exist for all controllers that are enabled. However, the controllers that are not enabled (Function Disabled), this field will be statically set by BIOS to activate ASL component in SPD gating equations. Bit 0: Corresponds to PCIe Controller A, Function 0 Bit 1: Corresponds to PCIe Controller A, Function 1 Bit 2: Corresponds to PCIe Controller A, Function 2 Bit 3: Corresponds to PCIe Controller A, Function 3 Bit 4: Corresponds to PCIe Controller B, Function 0 Bit 5: Corresponds to PCIe Controller B, Function 1 Bit 6: Corresponds to PCIe Controller B, Function 2 Bit 7: Corresponds to PCIe Controller B, Function 3 Bit 8: Corresponds to PCIe Controller C, Function 0 Bit 9: Corresponds to PCIe Controller C, Function 1 Bit 10: Corresponds to PCIe Controller C, Function 2 Bit 11: Corresponds to PCIe Controller C, Function 3 Bit 12: Corresponds to SATA Controller Bit 13: Corresponds to Gbe Controller Bit 14: Corresponds to xHCI Controller Bit 15: Corresponds to xDCI Controller Bit 16: Reserved Bit 17: Corresponds to PCIe Controller D, Function 0 Bit 18: Corresponds to PCIe Controller D, Function 1 Bit 19: Corresponds to PCIe Controller D, Function 2 Bit 20: Corresponds to PCIe Controller D, Function 3 Bit 21: Corresponds to PCIe Controller E, Function 0 Bit 22: Corresponds to PCIe Controller E, Function 1

Bit Range	Default	Access	Field Name and Description
			Bit 23: Corresponds to PCIe Controller E, Function 2 Bit 24: Corresponds to PCIe Controller E, Function 3 Bit 25: Corresponds to DMI Controller ; Bit 26: Reserved

Chipset Initialization Register B40 (CIRB40) – Offset 1b40

BIOS may program this register.

Chipset Initialization Register B44 (CIRB44) – Offset 1b44

BIOS may program this register.

Chipset Initialization Register BA8 (CIRBA8) – Offset 1ba8

BIOS may program this register.

Chipset Initialization Register BAC (CIRBAC) – Offset 1bac

BIOS may program this register.

Last PM_SYNC Message [31:0] (PM_SYNC_DATA_0) – Offset 1bb0

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO/V	**PM_SYNC Data [31:0] (PM_SYNC_DATA_VAL_0)** This field contains bits 31:0 of the last PM_SYNC message sent by the PMC.

Last PM_SYNC Message [63:32] (PM_SYNC_DATA_1) – Offset 1bb4

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO/V	**PM_SYNC Data [63:32] (PM_SYNC_DATA_VAL_1)** This field contains bits 63:32 of the last PM_SYNC message sent by the PMC.

CWB MDID Status Register (CWBMDIDSTATUS) – Offset 1bd4

Bit Range	Default	Access	Field Name and Description
31	0b	RO/V	**CWB Status (CWB_STS)** When set , DMI Central Write Buffer is enabled. Reflects DMI's np_pmc_cwb_en_ack status. 1: CWB on 0: CWB off
30:18	-	-	**Reserved**
17:9	000h	RW/V	**DMI MDID Value (DMI_MDID)** DMI sent MDID value.
8:0	000h	RW/V	**CNVi MDID Value (CNVI_MDID)** CNVi sent MDID value.

ACPI Control (ACTL) – Offset 1bd8

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**
2:0	000b	RW	

Bit Range	Default	Access	SCI IRQ Select (SCIS) Field Name and Description
			Specifies on which IRQ the SCI will internally appear. If not using the APIC, the SCI must be routed to IRQ[9-11], and that interrupt is not sharable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the SCI can also be mapped to IRQ20-23, and can be shared with other interrupts. Bits - SCI Map ---- - ------- 000 - IRQ9 001 - IRQ10 010 - IRQ11 011 - Reserved 100 - IRQ20 (only if APIC is enabled) 101 - IRQ21 (only if APIC is enabled) 110 - IRQ22 (only if APIC is enabled) 111 - IRQ23 (only if APIC is enabled) When the interrupt is mapped to APIC interrupts 9, 10 or 11, the APIC should be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, the APIC should be programmed for active-low reception.

Bit Range	Default	Access	Field Name and Description

PMC Throttling 1 (PMC_THROT_1) – Offset 1be0

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15	0b	RW/L	**PMC_THROT Lock (PMC_THROT_LOCK)** When set to 1 this entire register is locked.
14:1	-	-	**Reserved**
0	0b	RW/L	**VRAlert# Enable (VRALERT_EN)** 1: When VRAlert# pin is '0', the PMC requests throttling to a T3 Tstate to the PCH throttling unit. 0: VRAlert# pin is not used and does not initiate any throttling requests.

Chipset Initialization Register 3E8 (CS_SD_CTL1) – Offset 1be8

BIOS may program this register.

Chipset Initialization Register 3EC (CS_SD_CTL2) – Offset 1bec

BIOS may program this register.

PGD Priority Agent Mapping Register 0 (PPAMR0) – Offset 1d00

BIOS may program this register. The register is locked by PMCR.PDG_LOCk.

PGD Priority Agent Mapping Register 1 (PPAMR1) – Offset 1d04

BIOS may program this register. The register is locked by PMCR.PDG_LOCk.

PGD Priority Agent Mapping Register 2 (PPAMR2) – Offset 1d08

BIOS may program this register. The register is locked by PMCR.PDG_LOCk.

PGD Priority Agent Mapping Register 3 (PPAMR3) – Offset 1d0c

BIOS may program this register. The register is locked by PMCR.PDG_LOCk.

PGD Priority Agent Mapping Register 4 (PPAMR4) – Offset 1d10

BIOS may program this register. The register is locked by PMCR.PDG_LOCk.

PGD Priority Agent Mapping Register 5 (PPAMR5) – Offset 1d14

BIOS may program this register. The register is locked by PMCR.PDG_LOCk.

PGD Priority Agent Mapping Register 6 (PPAMR6) – Offset 1d18

BIOS may program this register. The register is locked by PMCR.PDG_LOCk.

PGD Priority Agent Mapping Register 7 (PPAMR7) – Offset 1d1c

BIOS may program this register. The register is locked by PMCR.PDG_LOCk.

PGD Priority Agent Mapping Register 8 (PPAMR8) – Offset 1d20

BIOS may program this register. The register is locked by PMCR.PDG_LOCk.

PGD Priority Agent Mapping Register 9 (PPAMR9) – Offset 1d24

BIOS may program this register. The register is locked by PMCR.PDG_LOCk.

PGD Priority Agent Mapping Register 10 (PPAMR10) – Offset 1d28

BIOS may program this register. The register is locked by PMCR.PDG_LOCk.

PGD Priority Agent Mapping Register 11 (PPAMR11) – Offset 1d2c

BIOS may program this register. The register is locked by PMCR.PDG_LOCk.

PGD Priority Agent Mapping Register 12 (PPAMR12) – Offset 1d30

BIOS may program this register. The register is locked by PMCR.PDG_LOCk.

PGD Priority Agent Mapping Register 13 (PPAMR13) – Offset 1d34

BIOS may program this register. The register is locked by PMCR.PDG_LOCk.

PGD Priority Agent Mapping Register 14 (PPAMR14) – Offset 1d38

BIOS may program this register. The register is locked by PMCR.PDG_LOCk.

PGD Priority Agent Mapping Register 15 (PPAMR15) – Offset 1d3c

BIOS may program this register. The register is locked by PMCR.PDG_LOCk.

Chipset Initialization Register 580 (CIR580) – Offset 1d80

Bit Range	Default	Access	Field Name and Description
31	0b	RO/V	**CSME Domain 6 Power Gate Ack Status (AGT31_PG_ACK_STS)** Same definition as bit 2.
30	0b	RO/V	**CSME Domain 5 Power Gate Ack Status (AGT30_PG_ACK_STS)** Same definition as bit 2.
29	0b	RO/V	**CSME Domain 4 Power Gate Ack Status (AGT29_PG_ACK_STS)** Same definition as bit 2.
28	0b	RO/V	**CSME Domain 3 Power Gate Ack Status (AGT28_PG_ACK_STS)** Same definition as bit 2.
27	0b	RO/V	**CSME Domain 2 Power Gate Ack Status (AGT27_PG_ACK_STS)** Same definition as bit 2.
26	0b	RO/V	**DCI Power Gate Ack Status (AGT26_PG_ACK_STS)** Same definition as bit 2.
25	0b	RO/V	**xDCI Power Gate Ack Status (AGT25_PG_ACK_STS)** Same definition as bit 2.
24:21	-	-	**Reserved**
20	0b	RO/V	**SDXC Power Gate Ack Status (AGT20_PG_ACK_STS)** Same definition as bit 2.
19	0b	RO/V	**Intel Trace Hub Power Gate Ack Status (AGT19_PG_ACK_STS)** Same definition as bit 2.

Bit Range	Default	Access	Field Name and Description
18	-	-	**Reserved**
17	0b	RO/V	**ISH Power Gate Ack Status (AGT17_PG_ACK_STS)** Same definition as bit 2.
16	0b	RO/V	**SMBus Power Gate Ack Status (AGT16_PG_ACK_STS)** Same definition as bit 2.
15	0b	RO/V	**LPC Power Gate Ack Status (AGT15_PG_ACK_STS)** Same definition as bit 2.
14	0b	RO/V	**Intel Serial I/O Power Gate Ack Status (AGT14_PG_ACK_STS)** Same definition as bit 2.
13	-	-	**Reserved**
12	0b	RO/V	**ADSP Domain 3 Power Gate Ack Status (AGT12_PG_ACK_STS)** Same definition as bit 2.
11	0b	RO/V	**ADSP Domain 2 Power Gate Ack Status (AGT11_PG_ACK_STS)** Same definition as bit 2.
10	0b	RO/V	**ADSP Domain 1 Power Gate Ack Status (AGT10_PG_ACK_STS)** Same definition as bit 2.
9	0b	RO/V	**Legacy Audio Power Gate Ack Status (AGT9_PG_ACK_STS)** Same definition as bit 2.
8	0b	RO/V	**SATA Power Gate Ack Status (AGT8_PG_ACK_STS)** Same definition as bit 2.
7	0b	RO/V	**GbE Power Gate Ack Status (AGT7_PG_ACK_STS)** Same definition as bit 2.
6	0b	RO/V	**PCIe Controller C Power Gate Ack Status (AGT6_PG_ACK_STS)** Same definition as bit 2.

Bit Range	Default	Access	Field Name and Description
5	0b	RO/V	**PCIe Controller B Power Gate Ack Status (AGT5_PG_ACK_STS)** Same definition as bit 2.
4	0b	RO/V	**PCIe Controller A Power Gate Ack Status (AGT4_PG_ACK_STS)** Same definition as bit 2.
3	0b	RO/V	**xHCI Power Gate Ack Status (AGT3_PG_ACK_STS)** Same definition as bit 2.
2	0b	RO/V	**SPI/eSPI Power Gate Status (AGT2_PG_ACK_STS)** This indicates the current powergating status of the controller. 0: Controller may be power gated 1: Controller may not be power gated.
1:0	-	-	**Reserved**

PGD PG_ACK Status Register 1 (PPASR1) – Offset 1d84

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**
28	0b	RO/V	**ADSP Domain 6 Power Gate Ack Status (AGT60_PG_ACK_STS)** Same definition as bit 0.
27	0b	RO/V	**ADSP Domain 5 Power Gate Ack Status (AGT59_PG_ACK_STS)** Same definition as bit 0.
26	0b	RO/V	**ADSP Domain 4 Power Gate Ack Status (AGT58_PG_ACK_STS)** Same definition as bit 0.
25:22	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
21	0b	RO/V	**eMMC Power Gate Ack Status (AGT53_PG_ACK_STS)** Same definition as bit 0.
20	-	-	**Reserved**
19	0b	RO/V	**CNVi WiFi Power Gate Ack Status (AGT51_PG_ACK_STS)** Same description as bit 0.
18:8	-	-	**Reserved**
7	0b	RO/V	**CSME Domain 14 Power Gate Ack Status (AGT39_PG_ACK_STS)** Same description as bit 0.
6	0b	RO/V	**CSME Domain 13 Power Gate Ack Status (AGT38_PG_ACK_STS)** Same description as bit 0.
5	0b	RO/V	**CSME Domain 12 Power Gate Ack Status (AGT37_PG_ACK_STS)** Same description as bit 0.
4	0b	RO/V	**CSME Domain 11 Power Gate Ack Status (AGT36_PG_ACK_STS)** Same description as bit 0.
3	-	-	**Reserved**
2	0b	RO/V	**CSME Domain 9 Power Gate Ack Status (AGT34_PG_ACK_STS)** Same description as bit 0.
1	0b	RO/V	**CSME Domain 8 Power Gate Ack Status (AGT33_PG_ACK_STS)** Same description as bit 0.
0	0b	RO/V	**CSME Domain 7 Power Gate Ack Status (AGT32_PG_ACK_STS)** This indicates the current powergating status. 0: Cotroller may be power gated 1: Controller may not be power gated.

PFET Enable Ack Register 0 (PPFEAR0) – Offset 1d90

Intel(R) ME is power gated when PPFEAR0[31..24]=0xF9 and PPFEAR1[7..0]=0xFF

Bit Range	Default	Access	Field Name and Description
31	0b	RO/V	**Intel(R) ME domain 6 PFET Enable Acknowledge Status (AGT31_PFET_EN_ACK_STS)** WhenAGT31_PFET_EN_ACK_STS = 1, Intel(R) ME domain 6 is powergated.
30	0b	RO/V	**Intel(R) ME domain 5 PFET Enable Acknowledge Status (AGT30_PFET_EN_ACK_STS)** WhenAGT30_PFET_EN_ACK_STS = 1, Intel(R) ME domain 5 is powergated.
29	0b	RO/V	**Intel(R) ME domain 4 PFET Enable Acknowledge Status (AGT29_PFET_EN_ACK_STS)** WhenAGT29_PFET_EN_ACK_STS = 1, Intel(R) ME domain 4 is powergated.
28	0b	RO/V	**Intel(R) ME domain 3 PFET Enable Acknowledge Status (AGT28_PFET_EN_ACK_STS)** WhenAGT28_PFET_EN_ACK_STS = 1, Intel(R) ME domain 3 is powergated.
27	0b	RO/V	**Intel(R) ME domain 2 PFET Enable Acknowledge Status (AGT27_PFET_EN_ACK_STS)** WhenAGT27_PFET_EN_ACK_STS = 1, Intel(R) ME domain 2 is powergated.
26	0b	RO/V	**DCI PFET Enable Acknowledge Status (AGT26_PFET_EN_ACK_STS)** WhenAGT26_PFET_EN_ACK_STS = 1, DCI is power gated.
25	0b	RO/V	**xDCI PFET Enable Acknowledge Status (AGT25_PFET_EN_ACK_STS)** WhenAGT25_PFET_EN_ACK_STS = 1, xDCI is power gated.
24:21	-	-	**Reserved**
20	0b	RO/V	**SD Controller PFET Enable Acknowledge Status (AGT20_PFET_EN_ACK_STS)** WhenAGT20_PFET_EN_ACK_STS = 1, SD controller is powergated.
19	0b	RO/V	**Intel(R) Trace Hub PFET Enable Acknowledge Status (AGT19_PFET_EN_ACK_STS)** WhenAGT19_PFET_EN_ACK_STS = 1, Intel(R) Trace Hub is powergated.
18	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
17	0b	RO/V	**ISH domain PFET Enable Acknowledge Status (AGT17_PFET_EN_ACK_STS)** WhenAGT17_PFET_EN_ACK_STS = 1, ISH domain is power gated.
16	0b	RO/V	**SMB domain PFET Enable Acknowledge Status (AGT16_PFET_EN_ACK_STS)** WhenAGT16_PFET_EN_ACK_STS = 1, SMBus domain is power gated.
15	0b	RO/V	**LPC Enable Acknowledge Status (AGT15_PFET_EN_ACK_STS)** When AGT15_PFET_EN_ACK_STS = 1, LPC domain is power gated.
14	0b	RO/V	**Intel Serial I/O Enable Acknowledge Status (AGT14_PFET_EN_ACK_STS)** When AGT14_PFET_EN_ACK_STS = 1, Intel Serial I/O interfaces domain is power gated.
13	-	-	**Reserved**
12	0b	RO/V	**ADSP domain 3 PFET Enable Acknowledge Status (AGT12_PFET_EN_ACK_STS)** WhenAGT12_PFET_EN_ACK_STS = 1, ADSP domain 3 is power gated.
11	0b	RO/V	**ADSP domain 2 PFET Enable Acknowledge Status (AGT11_PFET_EN_ACK_STS)** WhenAGT11_PFET_EN_ACK_STS = 1, ADSP domain 2 is power gated.
10	0b	RO/V	**ADSP domain 1 PFET Enable Acknowledge Status (AGT10_PFET_EN_ACK_STS)** When AGT10_PFET_EN_ACK_STS = 1, ADSP domain 1 is power gated.
9	0b	RO/V	**Legacy Audio Controller domain PFET Enable Acknowledge (AGT9_PFET_EN_ACK_STS)** When AGT9_PFET_EN_ACK_STS = 1, Legacy Audio Controller domain ispower gated.
8	0b	RO/V	**SATA domain PFET Enable Acknowledge Status (AGT8_PFET_EN_ACK_STS)** When AGT8_PFET_EN_ACK_STS= 1, SATA domain is power gated.
7	0b	RO/V	**GbE domain PFET Enable Acknowledge Status (AGT7_PFET_EN_ACK_STS)** When AGT7_PFET_EN_ACK_STS= 1, GbE domain is power gated.
6	0b	RO/V	**PCIe Controller C domain PFET Enable Acknowledge Status (AGT6_PFET_EN_ACK_STS)** When AGT6_PFET_EN_ACK_STS= 1, PCIe Controller C domain is power gated.

Bit Range	Default	Access	Field Name and Description
5	0b	RO/V	**PCIe Controller B domain PFET Enable Acknowledge Status (AGT5_PFET_EN_ACK_STS)** When AGT5_PFET_EN_ACK_STS = 1, PCIe Controller B domain is power gated.
4	0b	RO/V	**PCIe Controller A domain PFET Enable Acknowledge Status (AGT4_PFET_EN_ACK_STS)** When AGT4_PFET_EN_ACK_STS = 1, PCIe Controller A domain is power gated.
3	0b	RO/V	**xHCI domain PFET Enable Acknowledge Status (AGT3_PFET_EN_ACK_STS)** When AGT3_PFET_EN_ACK_STS = 1, xHCI domain is power gated.
2	0b	RO/V	**SPI/eSPI Enable Acknowledge Status (AGT2_PFET_EN_ACK_STS)** When AGT2_PFET_EN_ACK_STS = 1, SPI/eSPI domain is power gated.
1:0	-	-	**Reserved**

PFET Enable Ack Register 1 (PPFEAR1) – Offset 1d94

Intel(R) ME is power gated when PPFEAR0[31..24]=0xF9 and PPFEAR1[7..0]=0xFF

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**
28	0b	RO/V	**ADSP domain 6 PFET Enable Acknowledge Status (AGT60_PFET_EN_ACK_STS)** WhenAGT60_PFET_EN_ACK_STS = 1, ADSP domain 3 is power gated.
27	0b	RO/V	**ADSP domain 5 PFET Enable Acknowledge Status (AGT59_PFET_EN_ACK_STS)** WhenAGT59_PFET_EN_ACK_STS = 1, ADSP domain 5 is power gated.
26	0b	RO/V	**ADSP domain 4 PFET Enable Acknowledge Status (AGT58_PFET_EN_ACK_STS)** WhenAGT58_PFET_EN_ACK_STS = 1, ADSP domain 4 is power gated.
25:22	-	-	**Reserved**
21	0b	RO/V	**eMMC PFET Enable Acknowledge Status (AGT53_PFET_EN_ACK_STS)** WhenAGT53_PFET_EN_ACK_STS = 1, eMMC is power gated.

Bit Range	Default	Access	Field Name and Description
20	-	-	**Reserved**
19	0b	RO/V	**CNVi_Wifi PFET Enable Acknowledge Status (AGT51_PFET_EN_ACK_STS)** WhenAGT51_PFET_EN_ACK_STS=1 ,CNVi_Wifi is power gated.
18:8	-	-	**Reserved**
7	0b	RO/V	**Intel(R) ME domain 14 PFET Enable Acknowledge Status (AGT39_PFET_EN_ACK_STS)** WhenAGT39_PFET_EN_ACK_STS = 1, Intel(R) ME domain 14 is powergated.
6	0b	RO/V	**Intel(R) ME domain 13 PFET Enable Acknowledge Status (AGT38_PFET_EN_ACK_STS)** WhenAGT38_PFET_EN_ACK_STS = 1, Intel(R) ME domain 13 is powergated.
5	0b	RO/V	**Intel(R) ME domain 12 PFET Enable Acknowledge Status (AGT37_PFET_EN_ACK_STS)** WhenAGT37_PFET_EN_ACK_STS = 1, Intel(R) ME domain 12 is powergated.
4	0b	RO/V	**Intel(R) ME domain 11 PFET Enable Acknowledge Status (AGT36_PFET_EN_ACK_STS)** WhenAGT36_PFET_EN_ACK_STS = 1, Intel(R) ME domain 11 is powergated.
3	-	-	**Reserved**
2	0b	RO/V	**Intel(R) ME domain 9 PFET Enable Acknowledge Status (AGT34_PFET_EN_ACK_STS)** WhenAGT34_PFET_EN_ACK_STS = 1, Intel(R) ME domain 9 is powergated.
1	0b	RO/V	**Intel(R) ME domain 8 PFET Enable Acknowledge Status (AGT33_PFET_EN_ACK_STS)** WhenAGT33_PFET_EN_ACK_STS = 1, Intel(R) ME domain 8 is powergated.
0	0b	RO/V	**Intel(R) ME domain 7 PFET Enable Acknowledge Status (AGT32_PFET_EN_ACK_STS)** WhenAGT32_PFET_EN_ACK_STS = 1, Intel(R) ME domain 7 is powergated

Chipset Initialization Register DA0 (CIRDA0) – Offset 1da0

Bit Range	Default	Access	Field Name and Description
30:28	-	-	**Reserved**
27:24	6h	RW/L	**Power Ungate Stall Latency (PUG_STALL_LTCY)** When power ungating, this is the minimum time required between the deassertion of an Agent's pmc_ip_pg_ack_b signal before starting to handle another Power Gate/Ungate request. For latency times corresponding to the programmed value, refer to PGLSR.PG_ACK_PFETEN_LTCY.
23:12	-	-	**Reserved**
11:8	6h	RW/L	**Power Gate Stall Latency (PG_STALL_LTCY)** When power gating, this is the minimum time required between seeing an Agent's ip_pmc_pfet_en_ack_b signal deassert before starting to handle another Power Gate/Ungate request. For latency times corresponding to the programmed value, refer to PGLSR.PG_ACK_PFETEN_LTCY.
7:4	-	-	**Reserved**
3:0	6h	RW/L	**Power Gate PG Ack to PFET En Latency (PG_PGACK_PFETEN_LTCY)** When power gating, this is the minimum time required between the assertion of an Agent's pmc_ip_pg_ack_b before the deassertion of the Agent's (logical) pmc_ip_pfet_en_b. The latency is based on the value configured in this field according to the table below:

Bit Range	Default	Access	Field Name and Description
			0x0: 33ns 0x1: 66ns 0x2: 100ns 0x3: 133ns 0x4: 200ns 0x5: 266ns 0x6: 400ns 0x7: 533ns 0x8: 800ns 0x9: 1066ns 0xA: 1333ns 0xB: 1600ns 0xC: 1866ns 0xD: 2133ns 0xE: 2666ns

Bit Range	Default	Access	Field Name and Description
			0xF: 3200ns NOTE: the complementary Latency value for PG exit (minimum time between assertion of ip_pmc_pfet_en_ack_b and de-assertion of pmc_ip_pg_ack_b is defined in the PUGLSR* registers (one separate configurable value per PGD).

PGD Misc Control Register (PMCR) – Offset 1db0

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0b	RW/L	**PGD Lock Control (PGD_LOCK)** This control lock bit, once set, will prevent any host software writes from affecting the values of the following PGD group of registers: PPAMR* PGLSR0 PMCR PUGLSR* The lock bit once set, can be reset only on PLTRST# assertion.

Host SW PG Control Register 1 (HSWPGCR1) – Offset 1dd0

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**SW PG Req Control Lock (SW_PG_CTRL_LOCK)** 0: All other bits in this register are RW (can be set or cleared). 1: All bits in this register are locked (including this bit). Note: BIOS is expected to always write to this bit before handing off control to the OS, even if it has not changed any of the values in this register. This is because this Lock bit resets on platform reset, and needs to be set on every boot to S0 (to prevent any post-BIOS s/w from accessing or updating bits in this register).
30:0	-	-	**Reserved**

PGD PG_REQ Status Register 0 (PPRSR0) – Offset 1de0

Bit Range	Default	Access	Field Name and Description
31	0b	RO/V	**CSME Domain 6 Power Gate Req Status (AGT31_PG_REQ_STS)** Same definition as bit 2.
30	0b	RO/V	**CSME Domain 5 Power Gate Req Status (AGT30_PG_REQ_STS)** Same definition as bit 2.
29	0b	RO/V	**CSME Domain 4 Power Gate Req Status (AGT29_PG_REQ_STS)** Same definition as bit 2.
28	0b	RO/V	**CSME Domain 3 Power Gate Req Status (AGT28_PG_REQ_STS)** Same definition as bit 2.
27	0b	RO/V	**CSME Domain 2 Power Gate Req Status (AGT27_PG_REQ_STS)** Same definition as bit 2.
26	0b	RO/V	**DCI Power Gate Req Status (AGT26_PG_REQ_STS)** Same definition as bit 2.

Bit Range	Default	Access	Field Name and Description
25	0b	RO/V	**xDCI Power Gate Req Status (AGT25_PG_REQ_STS)** Same definition as bit 2.
24:21	-	-	**Reserved**
20	0b	RO/V	**SDXC Power Gate Req Status (AGT20_PG_REQ_STS)** Same definition as bit 2.
19	0b	RO/V	**Intel Trace Hub Power Gate Req Status (AGT19_PG_REQ_STS)** Same definition as bit 2.
18	-	-	**Reserved**
17	0b	RO/V	**ISH Power Gate Req Status (AGT17_PG_REQ_STS)** Same definition as bit 2.
16	0b	RO/V	**SMBus Power Gate Req Status (AGT16_PG_REQ_STS)** Same definition as bit 2.
15	0b	RO/V	**LPC Power Gate Req Status (AGT15_PG_REQ_STS)** Same definition as bit 2.
14	0b	RO/V	**Intel Serial I/O Power Gate Req Status (AGT14_PG_REQ_STS)** Same definition as bit 2.
13	-	-	**Reserved**
12	0b	RO/V	**ADSP Domain 3 Power Gate Req Status (AGT12_PG_REQ_STS)** Same definition as bit 2.
11	0b	RO/V	**ADSP Domain 2 Power Gate Req Status (AGT11_PG_REQ_STS)** Same definition as bit 2.
10	0b	RO/V	**ADSP Domain 1 Power Gate Req Status (AGT10_PG_REQ_STS)** Same definition as bit 2.
9	0b	RO/V	**Legacy Audio Power Gate Req Status (AGT9_PG_REQ_STS)** Same definition as bit 2.

Bit Range	Default	Access	Field Name and Description
8	0b	RO/V	**SATA Power Gate Req Status (AGT8_PG_REQ_STS)** Same definition as bit 2.
7	0b	RO/V	**GbE Power Gate Req Status (AGT7_PG_REQ_STS)** Same definition as bit 2.
6	0b	RO/V	**PCIe Controller C Power Gate Req Status (AGT6_PG_REQ_STS)** Same definition as bit 2.
5	0b	RO/V	**PCIe Controller B Power Gate Req Status (AGT5_PG_REQ_STS)** Same definition as bit 2.
4	0b	RO/V	**PCIe Controller A Power Gate Req Status (AGT4_PG_REQ_STS)** Same definition as bit 2.
3	0b	RO/V	**xHCI Power Gate Req Status (AGT3_PG_REQ_STS)** Same definition as bit 2.
2	0b	RO/V	**SPI/eSPI Power Gate Req Status (AGT2_PG_REQ_STS)** 0: Controller is requesting to be power-gated 1: Controller is requesting to be powered-on
1:0	-	-	**Reserved**

PGD PG_REQ Status Register 1 (PPRSR1) – Offset 1de4

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**
28	0b	RO/V	**ADSP Domain 6 Power Gate Req Status (AGT60_PG_REQ_STS)** Same definition as bit 0.
27	0b	RO/V	**ADSP Domain 5 Power Gate Req Status (AGT59_PG_REQ_STS)** Same definition as bit 0.

Bit Range	Default	Access	Field Name and Description
26	0b	RO/V	**ADSP Domain 4 Power Gate Req Status (AGT58_PG_REQ_STS)** Same definition as bit 0.
25:22	-	-	**Reserved**
21	0b	RO/V	**eMMC Power Gate Req Status (AGT53_PG_REQ_STS)** Same definition as bit 0.
20	-	-	**Reserved**
19	0b	RO/V	**CNVi WiFi Power Gate Req Status (AGT51_PG_REQ_STS)** Same definition as bit 0.
18:8	-	-	**Reserved**
7	0b	RO/V	**CSME Domain 14 Power Gate Req Status (AGT39_PG_REQ_STS)** Same definition as bit 0.
6	0b	RO/V	**CSME Domain 13 Power Gate Req Status (AGT38_PG_REQ_STS)** Same definition as bit 0.
5	0b	RO/V	**CSME Domain 12 Power Gate Req Status (AGT37_PG_REQ_STS)** Same definition as bit 0.
4	0b	RO/V	**CSME Domain 11 Power Gate Req Status (AGT36_PG_REQ_STS)** Same definition as bit 0.
3	-	-	**Reserved**
2	0b	RO/V	**CSME Domain 9 Power Gate Req Status (AGT34_PG_REQ_STS)** Same definition as bit 0.
1	0b	RO/V	**CSME Domain 8 Power Gate Req Status (AGT33_PG_REQ_STS)** Same definition as bit 0.

Bit Range	Default	Access	Field Name and Description
0	0b	RO/V	**CSME Domain 7 Power Gate Req Status (AGT32_PG_REQ_STS)** 0: Controller is requesting to be power-gated 1: Controller is requesting to be powered-on

Static PG Function Disable 1 (ST_PG_FDIS1) – Offset 1e20

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**Static Function Disable Lock (ST_FDIS_LK)** Lock control for all ST_PG_FDIS* and NST_PG_FDIS_* registers. Also self-locks when written to 1. This bit is reset by RSMRST# assertion.
30:6	-	-	**Reserved**
5	0b	RW/L	**ISH Function Disable PMC Version (ISH_FDIS_PMC)** BIOS is required to set this bit when ISH function is configured to be function disabled. This bit is reset by RTCRST# assertion.
4:2	-	-	**Reserved**
1	0b	RW/L	**CNVI Function Disable (PMC Version) (CNVI_FDIS_PMC)** BIOS is required to set this bit when CNVi function is configured to be function disabled. This bit is reset by RTCRST# assertion.
0	0b	RW/L	**GBE Function Disable PMC Version (GBE_FDIS_PMC)** BIOS is required to set this bit when GBE function is configured to be function disabled. This bit is reset by RTCRST# assertion.

Static Function Disable Control 2 (ST_PG_FDIS2) – Offset 1e24

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**
11	0b	RW/L	**GSPI Device 2 Function Disable (PMC Version) (LPSS_GSPI2_FDIS_PMC)** BIOS is required to set this bit when this device (single function) is configured to be function disabled.
10	0b	RW/L	**GSPI Device 1 Function Disable (PMC Version) (LPSS_GSPI1_FDIS_PMC)** BIOS is required to set this bit when this device (single function) is configured to be function disabled.
9	0b	RW/L	**GSPI Device 0 Function Disable (PMC Version) (LPSS_GSPI0_FDIS_PMC)** BIOS is required to set this bit when this device (single function) is configured to be function disabled.
8	0b	RW/L	**UART Device 2 Function Disable (PMC Version) (LPSS_UART2_FDIS_PMC)** BIOS is required to set this bit when this device (single function) is configured to be function disabled.
7	0b	RW/L	**UART Device 1 Function Disable (PMC Version) (LPSS_UART1_FDIS_PMC)** BIOS is required to set this bit when this device (single function) is configured to be function disabled.
6	0b	RW/L	**UART Device 0 Function Disable (PMC Version) (LPSS_UART0_FDIS_PMC)** BIOS is required to set this bit when this device (single function) is configured to be function disabled.
5	0b	RW/L	**I2C Device 5 Function Disable (PMC Version) (LPSS_I2C5_FDIS_PMC)** BIOS is required to set this bit when this device (single function) is configured to be function disabled.
4	0b	RW/L	**I2C Device 4 Function Disable (PMC Version) (LPSS_I2C4_FDIS_PMC)** BIOS is required to set this bit when this device (single function) is configured to be function disabled.
3	0b	RW/L	**I2C Device 3 Function Disable (PMC Version) (LPSS_I2C3_FDIS_PMC)** BIOS is required to set this bit when this device (single function) is configured to be function disabled.
2	0b	RW/L	**I2C Device 2 Function Disable (PMC Version) (LPSS_I2C2_FDIS_PMC)** BIOS is required to set this bit when this device (single function) is configured to be function disabled.

Bit Range	Default	Access	Field Name and Description
1	0b	RW/L	**I2C Device 1 Function Disable (PMC Version) (LPSS_I2C1_FDIS_PMC)** BIOS is required to set this bit when this device (single function) is configured to be function disabled.
0	0b	RW/L	**I2C Device 0 Function Disable (PMC Version) (LPSS_I2C0_FDIS_PMC)** BIOS is required to set this bit when this device (single function) is configured to be function disabled.

Non-Static PG Related Function Disable Register 1 (NST_PG_FDIS_1) – Offset 1e28

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29	0b	RW/L	**SDX Function Disable (PMC Version) (SDX_FDIS_PMC)** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled.
28	0b	RW/L	**EMMC Function Disable (PMC Version) (EMMC_FDIS_PMC)** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled.
27	-	-	**Reserved**
26	0b	RW/L	**XDCI Function Disable (PMC Version) (XDCI_FDIS_PMC)** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled.
25	0b	RW/L	**SMB Function Disable (PMC Version) (SMB_FDIS_PMC)** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled.
24	0b	RW/L	**LPC Function Disable (PMC Version) (LPC_FDIS_PMC)** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled.

Bit Range	Default	Access	Field Name and Description
23	0b	RW/L	**ADSP Function Disable (PMC Version) (ADSP_FDIS_PMC)** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled.
22	0b	RW/L	**SATA Controller Function Disable (PMC Version) (ST_FDIS_PMC)** BIOS is required to set this bit when the SATA controller (single function) is configured to be function disabled.
21:18	-	-	**Reserved**
17	0b	RW/L	**PCIe Controller D Port 3 Function Disable [PMC Version] (PCIE_D3_FDIS_PMC)** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
16	0b	RW/L	**PCIe Controller D Port 2 Function Disable [PMC Version] (PCIE_D2_FDIS_PMC)** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
15	0b	RW/L	**PCIe Controller D Port 1 Function Disable [PMC Version] (PCIE_D1_FDIS_PMC)** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
14	0b	RW/L	**PCIe Controller D Port 0 Function Disable [PMC Version] (PCIE_D0_FDIS_PMC)** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
13	0b	RW/L	**PCIe Controller C Port 3 Function Disable (PMC Version) (PCIE_C3_FDIS_PMC)** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
12	0b	RW/L	**PCIe Controller C Port 2 Function Disable (PMC Version) (PCIE_C2_FDIS_PMC)** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.

Bit Range	Default	Access	Field Name and Description
11	0b	RW/L	**PCIe Controller C Port 1 Function Disable (PMC Version) (PCIE_C1_FDIS_PMC)** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
10	0b	RW/L	**PCIe Controller C Port 0 Function Disable (PMC Version) (PCIE_C0_FDIS_PMC)** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
9	0b	RW/L	**PCIe Controller B Port 3 Function Disable (PMC Version) (PCIE_B3_FDIS_PMC)** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
8	0b	RW/L	**PCIe Controller B Port 2 Function Disable (PMC Version) (PCIE_B2_FDIS_PMC)** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
7	0b	RW/L	**PCIe Controller B Port 1 Function Disable (PMC Version) (PCIE_B1_FDIS_PMC)** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
6	0b	RW/L	**PCIe Controller B Port 0 Function Disable (PMC Version) (PCIE_B0_FDIS_PMC)** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
5	0b	RW/L	**PCIe Controller A Port 3 Function Disable (PMC Version) (PCIE_A3_FDIS_PMC)** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
4	0b	RW/L	**PCIe Controller A Port 2 Function Disable (PMC Version) (PCIE_A2_FDIS_PMC)** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
3	0b	RW/L	**PCIe Controller A Port 1 Function Disable (PMC Version) (PCIE_A1_FDIS_PMC)** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
2	0b	RW/L	**PCIe Controller A Port 0 Function Disable (PMC Version) (PCIE_A0_FDIS_PMC)** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	0b	RW/L	**XHCI Function Disable (PMC Version) (XHCI_FDIS_PMC)** BIOS is required to set this bit when this IP block (single logical function) is configured to be function disabled.

Always Running Timer Value 31:0 (ARTV_31_0) – Offset 1200

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO/V	**ART Value (ARTV)** Reads return current value of the ART timer [31:0]. Writes to this register has no effect Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

Always Running Timer Value 31:0 (ARTV_63_32) – Offset 1204

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO/V	**ART Value (ARTV)** Reads return current value of the ART timer [63:32]. Writes to this register has no effect Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

Timed GPIO Control 0 (TGPIOCTL0) – Offset 1210

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
4	0b	RW	**Periodic Mode (PM)** 0:Periodic mode is disabled 1:periodic mode is enabled This bit is only applicable when Timed GPIO is configured as an output
3:2	0b	RW	**Event Polarity (EP)** 00:Rising Edge 01:Falling Edge 10:Toggle Edge 11:Reserved
1	0b	RW	**Direction (DIR)** 0: Output 1: Input
0	0b	RW	**Enable (EN)** 0: Timed GPIO is disabled 1: Timed GPIO is enabled Note: a. When Enabled, xtal clock turnoff is disabled. This may also disable SLP_S0 assertion b. All other Timed GPIO configuration bits must be programmed before enable bit is set and must not change while the enable is 1

Timed GPIO 0 comparator Value 31:0 (TGPIOCOMPV0_31_0) – Offset 1220

Timed GPIO 0 comparator Value 31:0

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Comparator Value (COMPV)** This register is only applicable when Timed GPIO is configured as an output. If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. For example, in periodic mode if the value written to this register is 00000100h, and Periodic Interval register has the value of 200h. 1. A Timed GPIO event will be generated when ART reaches 00000100h. 2. The value in this register will then be adjusted by the hardware to 00000300h. 3. Another Timed GPIO event will be generated when the ART reaches 00000300h. 4. The value in this register will then be adjusted by the hardware to 00000500h As such when periodic Timed GPIO event occurs, the value in this register will increment. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

Timed GPIO comparator Value 63:32 (TGPIOCOMPV0_63_32) – Offset 1224

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Comparator Value (COMPV)** This register is only applicable when Timed GPIO is configured as an output. If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. For example, in periodic mode if the value written to this register is 00000100h, and Periodic Interval register has the value of 200h. 1. A Timed GPIO event will be generated when ART reaches 00000100h. 2. The value in this register will then be adjusted by the hardware to 00000300h. 3. Another Timed GPIO event will be generated when the ART reaches 00000300h. 4. The value in this register will then be adjusted by the hardware to 00000500h As such when periodic Timed GPIO event occurs, the value in this register will increment. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

Timed GPIO0 periodic Interval Value 31_0 (TGPIOPIV0_31_0) – Offset 1228

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Periodic Interval Value [31:0] (PIV)** This register is only applicable when Timed GPIO is configured as an output, and Periodic Mode is enabled.The value in this register is written by SW to set the interval for the periodic Timed GPIO event

Timed GPIO 0 periodic Interval Value 63_32 (TGPIOPIV0_63_32) – Offset 122c

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Periodic Interval Value [63:32] (PIV)** This register is only applicable when Timed GPIO is configured as an output, and Periodic Mode is enabled.The value in this register is written by SW to set the interval for the periodic Timed GPIO event

Timed GPIO Time Capture register 31_0 (TGPIOTCV0_31_0) – Offset 1230

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO/V	**Time Capture Value [31:0] (TCV)** When Timed GPIO event triggers, HW captures the current ART time into this register. This register is applicable to both when Timed GPIO is configured as an input or an output. When Timed GPIO is configured as an output, the Time Capture Value in this register is the Comparator Value (COMPV) when a match with ART time happens and a Timed GPIO output event generated. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

Timed GPIO0 Time Capture register 63_32 (TGPIOTCV0_63_32) – Offset 1234

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO/V	**Time Capture Value [63:32] (TCV)** When Timed GPIO event triggers, HW captures the current ART time into this register.This register is applicable to both when Timed GPIO is configured as an input or an output.When Timed GPIO is configured as an output, the Time Capture Value in this register is the Comparator Value (COMPV) when a match with ART time happens and a Timed GPIO output event generated.Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

Timed GPIO0 Event Counter Capture register 31_0 (TGPIOECCV0_31_0) – Offset 1238

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO/V	**Event Counter Capture Value [31:0] (ECCV)** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register. A read to the Time Capture Value (TGPIOTCV0_31_0) register triggers HW to load the Event Counter value into this register. Note: The load signal is the same register read signal that returns the Time Capture Value to the SW. SW must first perform a read to the Time Capture Value (TGPIOTCV0_31_0) register, followed by a read to this Event Counter Capture Value (ECCV) register such that these two values are associated with each others, despite they are obtained thru 2 separate register read operations one after another. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

Timed GPIO0 Event Counter Capture register 63_32 (TGPIOECCV0_63_32) – Offset 123c

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO/V	**Event Counter Capture Value [63:32] (ECCV)** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value (TGPIOTCV0_31_0) register. A read to the Time Capture Value (TGPIOTCV0_31_0) register triggers HW to load the Event Counter value into this register. Note: The load signal is the same register read signal that returns the Time Capture Value to the SW. SW must first perform a read to the Time Capture Value (TCV_31_0) register, followed by a read to this Event Counter Capture Value (ECCV) register such that these two values are associated with each others, despite they are obtained thru 2 separate register read operations one after another. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

Timed GPIO0 Event Counter Register 31_0 (TGPIOEC0_31_0) – Offset 1240

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO/V	**Event Counter Register [31:0] (EC)** Event Counter (EC):After Timed GPIO is enabled, event counter operates as follow: When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. Note: The signal to increment the count is the same signal that captures the ART time into the TCV register. For Timed GPIO configured as output with Periodic Mode enabled, it is also the same signal that updates the Comparator Value for the subsequent match.When Timed GPIO is disabled, event counter is reset to 0x0.Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

Timed GPIO0 Event Counter Register 63_32 (TGPIOEC0_63_32) –

Offset 1244

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO/V	**Event Counter Register [31:0] (EC)** Event Counter (EC):After Timed GPIO is enabled, event counter operates as follow: When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. Note: The signal to increment the count is the same signal that captures the ART time into the TCV register. For Timed GPIO configured as output with Periodic Mode enabled, it is also the same signal that updates the Comparator Value for the subsequent match.When Timed GPIO is disabled, event counter is reset to 0x0.Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

Timed GPIO Control 1 (TGPIOCTL1) – Offset 1310

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4	0b	RW	**Periodic Mode (PM)** 0:Periodic mode is disabled 1:periodic mode is enabled This bit is only applicable when Timed GPIO is configured as an output
3:2	0b	RW	**Event Polarity (EP)** 00:Rising Edge 01:Falling Edge 10:Toggle Edge 11:Reserved
1	0b	RW	**Direction (DIR)** 0: Output 1: Input

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**Enable (EN)** 0: Timed GPIO is disabled 1: Timed GPIO is enabled Note: a. When Enabled, xtal clock turnoff is disabled. This may also disable SLP_S0 assertion b. All other Timed GPIO configuration bits must be programmed before enable bit is set and must not change while the enable is 1

Timed GPIO 1 comparator Value 31:0 (TGPIOCOMPV1_31_0) – Offset 1320

Timed GPIO 1 comparator Value 31:0

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Comparator Value (COMPV)** This register is only applicable when Timed GPIO is configured as an output.If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change.If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. For example, in periodic mode if the value written to this register is 00000100h, and Periodic Interval register has the value of 200h.1. A Timed GPIO event will be generated when ART reaches 00000100h.2. The value in this register will then be adjusted by the hardware to 00000300h.3. Another Timed GPIO event will be generated when the ART reaches 00000300h.4. The value in this register will then be adjusted by the hardware to 00000500hAs such when periodic Timed GPIO event occurs, the value in this register will increment. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

Timed GPIO comparator Value 63:32 (TGPIOCOMPV1_63_32) –

Offset 1324

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Comparator Value (COMPV)** This register is only applicable when Timed GPIO is configured as an output.If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change.If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. For example, in periodic mode if the value written to this register is 00000100h, and Periodic Interval register has the value of 200h.1. A Timed GPIO event will be generated when ART reaches 00000100h.2. The value in this register will then be adjusted by the hardware to 00000300h.3. Another Timed GPIO event will be generated when the ART reaches 00000300h.4. The value in this register will then be adjusted by the hardware to 00000500hAs such when periodic Timed GPIO event occurs, the value in this register will increment. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

Timed GPIO1 periodic Interval Value 31_0 (TGPIOPIV1_31_0) – Offset 1328

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Periodic Interval Value [31:0] (PIV)** This register is only applicable when Timed GPIO is configured as an output, and Periodic Mode is enabled.The value in this register is written by SW to set the interval for the periodic Timed GPIO event

Timed GPIO 1 periodic Interval Value 63_32 (TGPIOPIV1_63_32) – Offset 132c

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Periodic Interval Value [63:32] (PIV)** This register is only applicable when Timed GPIO is configured as an output, and Periodic Mode is enabled.The value in this register is written by SW to set the interval for the periodic Timed GPIO event

Timed GPIO Time Capture register 31_0 (TGPIOTCV1_31_0) – Offset 1330

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO/V	**Time Capture Value [31:0] (TCV)** When Timed GPIO event triggers, HW captures the current ART time into this register.This register is applicable to both when Timed GPIO is configured as an input or an output.When Timed GPIO is configured as an output, the Time Capture Value in this register is the Comparator Value (COMPV) when a match with ART time happens and a Timed GPIO output event generated.Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

Timed GPIO Time Capture register 63_32 (TGPIOTCV1_63_32) – Offset 1334

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO/V	**Time Capture Value [63:32] (TCV)** When Timed GPIO event triggers, HW captures the current ART time into this register.This register is applicable to both when Timed GPIO is configured as an input or an output.When Timed GPIO is configured as an output, the Time Capture Value in this register is the Comparator Value (COMPV) when a match with ART time happens and a Timed GPIO output event generated.Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

Timed GPIO0 Event Counter Capture register 31_0 (TGPIOECCV1_31_0) – Offset 1338

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO/V	**Event Counter Capture Value [31:0] (ECCV)** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register. A read to the Time Capture Value (TCV1_31_0) register triggers HW to load the Event Counter value into this register. Note: The load signal is the same register read signal that returns the Time Capture Value to the SW. SW must first perform a read to the Time Capture Value (TCV1_31_0) register, followed by a read to this Event Counter Capture Value (ECCV) register such that these two values are associated with each others, despite they are obtained thru 2 separate register read operations one after another. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

Timed GPIO0 Event Counter Capture register 63_32 (TGPIOECCV1_63_32) – Offset 133c

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO/V	**Event Counter Capture Value [63:32] (ECCV)** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value (TGPIOTCV0_31_0) register. A read to the Time Capture Value (TCV) register triggers HW to load the Event Counter value into this register. Note: The load signal is the same register read signal that returns the Time Capture Value to the SW. SW must first perform a read to the Time Capture Value (TCV1_31_0) register, followed by a read to this Event Counter Capture Value (ECCV) register such that these two values are associated with each others, despite they are obtained thru 2 separate register read operations one after another. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

Timed GPIO1 Event Counter Register 31_0 (TGPIOEC1_31_0) – Offset 1340

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO/V	**Event Counter Register [31:0] (EC)** Event Counter (EC):After Timed GPIO is enabled, event counter operates as follow: When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. Note: The signal to increment the count is the same signal that captures the ART time into the TCV register. For Timed GPIO configured as output with Periodic Mode enabled, it is also the same signal that updates the Comparator Value for the subsequent match.When Timed GPIO is disabled, event counter is reset to 0x0.Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

Timed GPIO Event Counter Register 63_32 (TGPIOEC1_63_32) – Offset 1344

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO/V	**Event Counter Register [31:0] (EC)** Event Counter (EC):After Timed GPIO is enabled, event counter operates as follow: When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. Note: The signal to increment the count is the same signal that captures the ART time into the TCV register. For Timed GPIO configured as output with Periodic Mode enabled, it is also the same signal that updates the Comparator Value for the subsequent match.When Timed GPIO is disabled, event counter is reset to 0x0.Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

ART to RTC Ratio (ART_RTC_RATIO) – Offset 1670

The ratio between the ART crystal clock and the RTC crystal clock is reflected here. Note that this register is only updated after calibration is complete. The register will be updated from its default of 0x00000000 once the calibration is complete.

This register is in the CORE power well and is reset by cpupwrgd_pmcc_rst_b.

Bit Range	Default	Access	Field Name and Description
30:28	-	-	**Reserved**
27:18	000h	RO/V	**ART to RTC Ratio Integer Component (ART_RTC_RATIO_INT)** This field reflects the integer component of the ratio between the ART and RTC clocks.
17:0	000h	RO/V	**ART to RTC Ratio Fractional Component (ART_RTC_RATIO_FRAC)** This field reflects the fractional component of the ratio between the ART and RTC clocks.

Wake Alarm Device Timer: AC (WADT_AC) – Offset 1800

Bit Range	Default	Access	Field Name and Description
31:0	FFFFFFFFh	RW/V	**Wake Alarm Device Timer Value for AC Mode (WADT_AC_VAL)** This field contains the 32-bit wake alarm device timer value (granularity 1s) for AC power. The timer begins decrementing when written to a value other than FFFFFFFFh (regardless of the power source when the write occurs). Upon counting down to 0: - If on AC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. - If the power source is DC at this time, the status bit is not set. However, if AC power subsequently returns to the platform, the AC Expired Timer begins running. See the WADT_EXP_AC register for details. - The timer returns to its default value of FFFFFFFFh. This bit is reset by DSW_PWROK de-assertion.

Wake Alarm Device Timer: DC (WADT_DC) – Offset 1804

Bit Range	Default	Access	Field Name and Description
31:0	FFFFFFFFh	RW/V	**Wake Alarm Device Timer Value for DC Mode (WADT_DC_VAL)** This field contains the 32-bit wake alarm device timer value (granularity 1s) for DC power. The timer begins decrementing when written to a value other than FFFFFFFFh (regardless of the power source when the write occurs). Upon counting down to 0: - If on DC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. - If the power source is AC at this time, the status bit is not set. However, if DC power subsequently returns to the platform, the DC Expired Timer begins running. See the WADT_EXP_DC register for details. - The timer returns to its default value of FFFFFFFFh. This bit is reset by DSW_PWROK de-assertion.

Wake Alarm Device Expired Timer: AC (WADT_EXP_AC) – Offset 1808

Bit Range	Default	Access	Field Name and Description
31:0	FFFFFFFFh	RW/V	**Wake Alarm Device Expired Timer Value for AC Mode (WADT_EXP_AC_VAL)** This field contains the 32-bit wake alarm device "Expired Timer" value (granularity 1s) for AC power. The timer begins decrementing after switching from DC to AC power. In the case where the WADT_AC timer has already expired while the platform was on DC power, this timer only decrements while operating on AC power. So if the power source switches back to DC power, the timer will stop (but not reset). When AC power returns, the timer will again begin decrementing. Note: This timer will only begin decrementing under the conditions described above if this field has been configured for something other than its default value of FFFFFFFFh (i.e. FFFFFFFFh = disabled). Upon expiration of this timer: - If on AC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. - BOTH the AC and DC Expired Timers return to their defaults value of FFFFFFFFh. This bit is reset by DSW_PWROK de-assertion.

Wake Alarm Device Expired Timer: DC (WADT_EXP_DC) – Offset 180c

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	FFFFFFFFh	RW/V	**Wake Alarm Device Expired Timer Value for DC Mode (WADT_EXP_DC_VAL)** This field contains the 32-bit wake alarm device "Expired Timer" value (granularity 1s) for DC power.The timer begins decrementing after switching from AC to DC power. In the case where the WADT_DC timer has already expired while the platform was on AC power, this timer only decrements while operating on DC power. So if the power source switches back to AC power, the timer will stop (but not reset). When DC power returns, the timer will again begin decrementing. Note: This timer will only begin decrementing under the conditions described above if this field has been configured for something other than its default value of FFFFFFFFh (i.e. FFFFFFFFh = disabled). Upon expiration of this timer: - If on DC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. - BOTH the AC and DC Expired Timers return to their defaults value of FFFFFFFFh. This bit is reset by DSW_PWROK de-assertion.

Power and Reset Status (PRSTS) – Offset 1810

Bit Range	Default	Access	Field Name and Description
30:6	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
5	0b	RW/1C/V	**Wake On LAN Override Wake Status (WOL_OVR_WK_STS)** This bit gets set when integrated LAN Signals a Power Management Event AND the system is in S5. BIOS can read this status bit to determine this wake source. Software clears this bit by writing a 1 to it.
4:1	-	-	**Reserved**
0	0b	RW/1C/V	**ME_HOST_WAKE_STS (ME_HOST_WAKE_STS)** This bit is set when the ME generates a non-maskable wake event and is not affected by any other enable bit. When this bit is set, the host power management logic wakes to S0.

Power Management Configuration Reg 1 (PM_CFG) – Offset 1818

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29	0b	RW	**Allow 24MHz Crystal Oscillator Shutdown (ALLOW_24_OSC_SD)** When this bit is '0', the 24MHz crystal oscillator will always be running while in S0. When this bit is '1', the 24MHz crystal oscillator may be shut down in S0 (Cx only) if all other conditions allow.
28:26	-	-	**Reserved**
25	0b	RW	**Allow USB2 PHY Core Power Gating (ALLOW_USB2_CORE_PG)** When this bit is '0' (default), USB2 PHY power gating is disabled. When this bit is '1', USB2 PHY power gating can occur if all other required conditions are met.

Bit Range	Default	Access	Field Name and Description
24	0b	RW/L	**Energy Reporting Lock (ER_LOCK)** When this bit is written to 1, it will remain 1 until the next RSMRST# assertion. While this bit is 1, GEN_PMCON_A.ER_EN value cannot be changed. BIOS should write 1b1 to this bit only AFTER writing to GEN_PMCON_A.ER_EN.
23:22	-	-	**Reserved**
21	0b	RW	**RTC Wake from DeepSx Disable (RTC_DSX_WAKE_DIS)** When set, this bit disables RTC wakes from waking the system from DeepSx. This bit is reset by RTCRST# assertion.
20	-	-	**Reserved**
19:18	00b	RW/L	**SLP_SUS# Minimum Assertion Width (SLP_SUS_MIN_ASST_WDTH)** This 2-bit value indicates the minimum assertion width of the SLP_SUS# signal to guarantee that the SUS well power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00 = 0 ms (i.e. stretching disabled - default) 01 = 500ms 10 = 1s 11 = 4s This field is not writable when the SLP_Sx# Stretching Policy Lock- Down bit is set. This field is ignored when exiting a G3 state if the "Disable SLP_X Stretching After SUS Power Failure" bit is set. Note that unlike with all other SLP_* pin stretching, this disable bit only impacts SLP_SUS# stretching during G3 exit rather than both G3 and DeepSx exit. SLP_SUS# stretching always applies to DeepSx regardless of the disable bit. Programming Note: For platforms that enable DeepSx, BIOS must program SLP_SUS# stretching to be greater than or equal to the largest stretching value on any other SLP_* pin (SLP_S3#, SLP_S4#, SLP_LAN#, or SLP_A#). This bit is cleared by the RTCRST# pin.

Bit Range	Default	Access	Field Name and Description
17:16	00b	RW/L	**SLP_A# Minimum Assertion Width (SLP_A_MIN_ASST_WDTH)** This 2-bit value indicates the minimum assertion width of the SLP_A# signal to guarantee that the ASW power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00 = 0 ms (i.e. stretching disabled - default) 01 = 4 s 10 = 98 ms 11 = 2 s This field is not writable when the SLP_Sx# Stretching Policy Lock- Down bit is set. This field is ignored when exiting a G3 or Deep Sx state if the "Disable SLP_X Stretching After SUS Power Failure" bit is set. This bit is cleared by the RTCRST# pin.
15:14	00b	RW/L	**SLP_LAN# Minimum Assertion Width (SLP_LAN_MIN_ASST_WDTH)** This 2-bit value indicates the minimum assertion width of the SLP_LAN# signal to guarantee that the power to the PHY has been fully power-cycled. This value may be modified per platform depending on power supply, capacitance, board capacitance, power failure detection circuits, etc. This field is not writable when the SLP_Sx# Stretching Policy Lock Down bit is set to 1. This bit is reset by RTCRST# assertion.

Bit Range	Default	Access	Field Name and Description
13	0b	RW	**After G3 Last State Enable (AG3_LS_EN)** When PM_CFG.AG3E is '0', AG3_LS_EN determines whether the PCH will consider the platform's previous state when determining whether to power-up after G3. Encodings: 0: PCH power-up policies after G3 do not depend on the platform's state when the G3 occurred. (default) 1: PCH power-up policies after G3 depend on the platform's state when the G3 occurred. - If the power failure occurred while the platform was in S0 or while in the process of going to S0, the platform will power-up to S0 upon exiting G3. - If the power failure occurred while the platform was in Sx or while in the process of going to Sx, the platform will stay in S4/S5 upon exiting G3. Note: This bit applies only when GEN_PMCON_3.AG3E is '0'. If AG3E is '1', the platform will always stay in S4/S5 after G3 regardless of the value of AG3_LS_EN.

Bit Range	Default	Access	Field Name and Description
12	0b	RW	**After Type 8 Global Reset Last State Enable (A8GR_LS_EN)** AGR_LS_EN determines whether the PCH will consider the platform's previous state when determining whether to power-up after non-thermal and non-explicitly requested type 8 global resets. Encodings: 0 (default): PCH power-up policies after a global reset do not depend on the platform's state when the reset occurred. 1: PCH power-up policies after a global reset depend on the platform's state when the reset occurred. If the global reset occurred while the platform was in S0 or while in the process of going to S0, the platform will power-up to S0 after the reset. If the global reset occurred while the platform was in Sx or while in the process of going to Sx, the platform will stay in S5 upon exiting G3.
11	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
10	0b	RW	**Power Button Debounce Mode (PB_DB_MODE)** This bit controls when interrupts (SMI#, SCI) are generated in response to assertion of the PWRBTN# pin. This bit's values cause the following behavior: - '0': The 16ms debounce period applies to all usages of the PWRBTN# pin (legacy behavior). - '1': When a falling edge occurs on the PWRBTN# pin, an interrupt is generated and the 16ms debounce timer starts. Subsequent interrupts are masked while the debounce timer is running. Note: Power button override logic always samples the post-debounce version of the pin. This bit is reset by RTCRST# assertion.

Bit Range	Default	Access	Field Name and Description
9:8	00b	RW/L	**Reset Power Cycle Duration (PWR_CYC_DUR)** The value in this register determines the minimum time a platform will stay in reset (SLP_S3#, SLP_S4#, SLP_S5# asserted and also SLP_A# and SLP_LAN# asserted if applicable) during a host partition reset with power cycle or a global reset. The duration programmed in this register takes precedence over the applicable SLP_# stretch timers in these reset scenarios. This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. Note that the duration programmed in this register should never be smaller than the stretch duration programmed in the following registers - - GEN_PMCON_3.SLP_S3_MIN_ASST_WDTH - GEN_PMCON_3.S4MAW - PM_CFG.SLP_A_MIN_ASST_WDTH - PM_CFG.SLP_LAN_MIN_ASST_WDTH This bit is reset by RTCRST# assertion. 00 = 4 - 5 seconds 01 = 3 - 4 seconds 10 = 2 - 3 seconds 11 = 1 - 2 seconds
7:6	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
5	1b	RW/V	**CPU OC Strap (COCS)** SW programs this pin with the value that should be reflected to the GPIO8_OCS pin, when the pin is in native mode. Hardware also sets this bit when the over-clocking watchdog timer expires. This bit is reset by RSMRST# assertion.
4:3	-	-	**Reserved**
2	0b	RW/L	**Energy Reporting Enable (ER_EN)** When this bit is 1, the PCH will periodically calculate and report its energy consumption to the CPU via PM_SYNC. When this bit is 0, the PCH will neither calculate nor report its energy consumption.

Bit Range	Default	Access	Field Name and Description
1:0	00b	RW/V	**Timing t581 (TIMING_T581)** This field configures the t581 timing involved in the power down flow (CPUPWRGD inactive to ICC_ICLK_INIT inactive). Encodings (all min timings): 00: 10 us (default) 01: 100 us 10: 1 ms 11: 10 ms reset_type=host_deep_rst_b

PCH Power Management Status (PCH_PM_STS2) – Offset 1824

This register contains misc. fields used to record events pertaining to PCH power management. Unless otherwise indicated, all RWC bits are cleared with a write of '1' by software.

Bit Range	Default	Access	Field Name and Description
30:15	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
14	0b	RW/1C/V	**CPU Reset Done Failure (CRD)** CPU Reset Done message did not arrive from the CPU.
13	0b	RW/1C/V	**ME Host Boot Prep Done Failure (ME_HBPD)** ME Host Boot Preparation did not complete.
12	0b	RW/1C/V	**PINSTOP Acknowledge Failure (PINSTOP_ACK)** The GbE PHY did not respond to the PINSTOP message.
11	-	-	**Reserved**
10	0b	RW/1C/V	**SMT Reset Acknowledge Failure (SMT_RST_ACK)** One or more SMT controllers did not respond to the CSME bus reset warning.
9	0b	RW/1C/V	**EXI State Transition Acknowledge Failure (EXI_STATE_TRANS_ACK)** EXI state transition ACK did not arrive.
8	0b	RW/1C/V	**SPI Common Prep Handshake Failure (SPI_HRHS)** The SPI controller did not complete the host partition reset/Sx entry handshake.
7	0b	RW/1C/V	**XCK Common Prep Handshake Failure (XCK_HRHS)** The integrated clocking unit did not complete the host partition reset/Sx entry handshake.
6	0b	RW/1C/V	**CPU S345/Reset Warn Acknowledge Failure (CPU_S345RW_ACK)** The CPU did not respond to the GO_S345 or RESET_WARN message.
5	0b	RW/1C/V	**CPU S1 Acknowledge Failure (CPU_S1_ACK)** The CPU did not respond to the GO_S1_XXX message.
4	0b	RW/1C/V	**DMI L23 Entry Failure (DMI_L23)** The DMI interface did not respond to the request to entry L23.
3	0b	RW/1C/V	**SMBus Host Reset Handshaking Failure (SMB_SRHS)** The host SMBus controller did not complete the host partition reset handshake.
2	0b	RW/1C/V	**South Port L23 Entry Failure (SP_L23)** The PCH PCI Express ports did not complete the host partition reset/Sx entry handshake.

Bit Range	Default	Access	Field Name and Description
1	0b	RW/1C/V	**XHCI Common Prep Handshake Failure (XHCI_HRHS)** The XHCI controller did not complete the host partition reset/Sx entry handshake.
0	-	-	**Reserved**

S3 Power Gating Policies (S3_PWRGATE_POL) – Offset 1828

This register contains policy bits to configure various power gating options while the system is in S3. Note that setting any of these policies to "enabled" may not directly result in power gating - in some cases other HW qualifications may be dynamically applied.

This register is in the RTC power well and is reset by RTCRST# assertion.

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1	0b	RW	**S3 Power Gate Enable in DC Mode: SUS Well (S3DC_GATE_SUS)** A '1' in this bit enables power gating of the SUS well in S3 while operating on DC power (based on the AC_PRESENT pin value).
0	0b	RW	**S3 Power Gate Enable in AC Mode: SUS Well (S3AC_GATE_SUS)** A '1' in this bit enables power gating of the SUS well in S3 while operating on AC power (based on the AC_PRESENT pin value).

S4 Power Gating Policies (S4_PWRGATE_POL) – Offset 182c

This register contains policy bits to configure various power gating options while the system is in S4. Note that setting any of these policies to "enabled" may not directly result in power gating - in some cases other HW qualifications may be dynamically applied.

This register is in the RTC power well and is reset by RTCRST# assertion.

Bit Range	Default	Access	Field Name and Description
31:2	00000000h	RO	**Reserved (RSVD)**

Bit Range	Default	Access	Field Name and Description
1	0b	RW	**S4 Power Gate Enable in DC Mode: SUS Well (S4DC_GATE_SUS)** A '1' in this bit enables power gating of the SUS well in S4 while operating on DC power (based on the AC_PRESENT pin value).
0	0b	RW	**S4 Power Gate Enable in AC Mode: SUS Well (S4AC_GATE_SUS)** A '1' in this bit enables power gating of the SUS well in S4 while operating on AC power (based on the AC_PRESENT pin value).

S5 Power Gating Policies (S5_PWRGATE_POL) – Offset 1830

This register contains policy bits to configure various power gating options while the system is in S5. Note that setting any of these policies to "enabled" may not directly result in power gating - in some cases other HW qualifications may be dynamically applied.

This register is in the RTC power well and is reset by RTCRST# assertion.

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15	0b	RW	**S5 Power Gate Enable in DC Mode: SUS Well (S5DC_GATE_SUS)** A '1' in this bit enables power gating of the SUS well in S5 while operating on DC power (based on the AC_PRESENT pin value).
14	0b	RW	**S5 Power Gate Enable in AC Mode: SUS Well (S5AC_GATE_SUS)** A '1' in this bit enables power gating of the SUS well in S5 while operating on AC power (based on the AC_PRESENT pin value).
13:0	-	-	**Reserved**

DeepSx Configuration (DSX_CFG) – Offset 1834

This register contains misc. fields used to configure the PCH's power management behavior.

This register is in the RTC power well and is reset by RTCRST# assertion.

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4	0b	RW	**Require CNV Wake Disabled for DeepSx Entry/SUSPWRDNACK (REQ_CNV_NOWAKE_DSX)** If this bit is 0, the state of connectivity wake enable is not considered when making DeepSx entry decisions. If this bit is 1, connectivity wake must be disabled to allow DeepSx entry or SUSPWRDNACK assertion, and even then all other conditions must be satisfied.
3	0b	RW	**Require BATLOW# Assertion for DeepSx Entry/SUSPWRDNACK (REQ_BATLOW_DSX)** If this bit is 0, the state of the BATLOW# pin is not considered when making DeepSx entry and SUSPWRDNACK decisions. If this bit is 1, BATLOW# must be asserted to allow DeepSx entry or SUSPWRDNACK assertion, and even then all other entry conditions must be satisfied.
2	0b	RW	**WAKE# Pin DeepSx Enable (WAKE_PIN_DSX_EN)** When this bit is 1, the PCI Express WAKE# pin is monitored while in Deep Sx, supporting waking from Deep Sx due to assertion of this pin. In this case, the platform must externally pull up the pin to the DSW (instead of pulling up to the SUS as has historically been the case). When this bit is 0: - DeepSx enabled configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. -Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled Note: Deep Sx disabled configurations must leave this bit at 0.

Bit Range	Default	Access	Field Name and Description
1	0b	RW	**AC_PRESENT Pin Pulldown in DeepSx Disable (ACPRES_PD_DSX_DIS)** When this bit is 1, the internal pull-down on the ACPRESENT pin is disabled. However, the pulldown is not necessarily enabled if the bit is '0'. This bit must be left at '0' for Deep Sx disabled configurations, and the pulldown is disabled for those configurations even though the bit is '0'. To support ME wakes from Deep Sx, the pin is always monitored regardless of the value of this host policy bit. When this bit is '0': DeepSx enabled configurations: The PCH internal pull-down on ACPRESENT is enabled in Deep Sx and during G3 exit. Deep Sx disabled configurations: The PCH internal pull-down on ACPRESENT is always disabled.
0	0b	RW	**LANWAKE Pin DeepSx Enable (LANWAKE_PIN_DSX_EN)** When this bit is 1, the LANWAKE pin is monitored while in DeepSx, supporting waking from DeepSx due to assertion of this pin. In this case, the platform must drive the pin to the correct value while in DeepSx. DeepSx disabled configurations must leave this bit at 0. When this bit is 0: DeepSx enabled configurations: The PCH internal pull-down on LANWAKE pin is enabled in deep-Sx and during G3 exit and the pin is not monitored during this time. DeepSx disabled configurations: The PCH internal pull-down is never enabled

Power Management Configuration Reg 2 (PM_CFG2) – Offset 183c

Bit Range	Default	Access	Field Name and Description
31:29	000b	RW	**Power Button Override Period (PBOP)** This field determines, while the power button remains asserted, how long the PMC will wait before initiating a global reset. Encoding: 000b - 4 seconds 001b - 6 seconds 010b - 8 seconds 011b - 10 seconds 100b - 12 seconds 101b - 14 seconds Others - Reserved This bit is reset by DSW_PWROK de-assertion.
28	0b	RW/L	**Power Button Native Mode Disable (PB_DIS)** When this bit is '0' (default), the PMC's power button logic will act upon the input value from the GPIO unit, as normal. When this bit is set to '1', the PMC must force its internal version of the power button pin to '1'. This will result in the PMC logic constantly seeing the pin as de-asserted. This bit is reset by RTCRST# assertion.
27	-	-	**Reserved**
26	0b	RW/V	**DRAM_RESET# Control (DRAM_RESET_CTL)** BIOS uses this bit to control the DRAM_RESET# pin from the PCH, which is routed to the reset pin on the DRAM. Encoding: 0 = DRAM_RESET# output is asserted (driven low) 1 = DRAM_RESET# output is tri-stated. Note: This bit is cleared to '0' by HW when SLP_S4# goes low. This bit is reset by DSW_PWROK de-assertion.

Bit Range	Default	Access	Field Name and Description
25:0	-	-	**Reserved**

Chipset Initialization Register 48 (CIR48) – Offset 1848

BIOS may program this register.

Chipset Initialization Register 4C (CIR4C) – Offset 184c

BIOS may program this register.

Chipset Initialization Register 50 (CIR50) – Offset 1850

BIOS may program this register.

Chipset Initialization Register 54 (CIR54) – Offset 1854

BIOS may program this register.

Chipset Initialization Register 58 (CIR58) – Offset 1858

BIOS may program this register.

Chipset Initialziation Register 68 (CIR68) – Offset 1868

BIOS may program this register.

Chipset Initialization Register 80 (CIR80) – Offset 1880

BIOS may program this register.

Chipset Initialization Register 84 (CIR84) – Offset 1884

BIOS may program this register.

Chipset Initialization Register 88 (CIR88) – Offset 1888

BIOS may program this register.

Chipset Initialization Register 8C (CIR8C) – Offset 188c

BIOS may program this register.

Chipset Initialization Register 98 (CIR98) – Offset 1898

BIOS may program this register.

Chipset Initizaliation Register A8 (CIRA8) – Offset 18a8

BIOS may program this register.

Chipset Initizaliation Register AC (CIRAC) – Offset 18ac

BIOS may program this register.

Chipset Initialization Register B0 (CIRB0) – Offset 18b0

BIOS may program this register.

Chipset Initialization Register B4 (CIRB4) – Offset 18b4

BIOS may program this register.

Chipset Initialization Register C0 (CIRC0) – Offset 18c0

BIOS may program this register.

PMSYNC Thermal Power Reporting Configuration (PMSYNC_TPR_CFG) – Offset 18c4

This register contains configuration bits that apply to PCH reporting of thermal and power status to the Processor.

Power Well: Primary.

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**PCH-to-CPU Thermal Power Reporting Configuration Lockdown (PCH2CPU_TPR_CFG_LOCK)** When set to 1b, this bit prevents writes from changing the value of this 32-bit register.
30:27	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
26	0b	RW/L	**PCH-to-CPU Thermal Throttle Enable (PCH2CPU_TT_EN)** When this bit is set to '1' the PCH is enabled to set the thermal throttle request to the PROC using the PMSYNC PCH_THERM_STATUS bit. When this bit is '0', the PCH-to-CPU Thermal Throttling request is disabled.
25:24	00b	RW/L	**PCH-to-CPU Thermal Throttle State (PCH2CPU_TT_STATE)** This field specifies the PCH T-State level at which the PMC asserts the Thermal Throttle (PCH_THERM_STATUS) bit to the PROC. The PMC requests thermal throttling when the T-State, which is reported from the Thermal Sensor cluster, is greater than or equal to this state. Note: Refer to BIOS specification on the supported setting.
23:0	-	-	**Reserved**

PM_SYNC Miscellaneous Configuration (PM_SYNC_MISC_CFG) – Offset 18c8

This register is used to configure miscellaneous aspects of the PM_SYNC pin.

This register is in the CORE power well and is reset by PLTRST#.

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15	0b	RW/L	**PM_SYNC Configuration Lock (PM_SYNC_LOCK)** The bit is used to lock down the settings of several PM_SYNC-related configuration bits. This bit is self-locking (i.e. once written to '1', it can only be cleared by PLTRST#).
14:12	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
11	0b	RW/L	**GPIO_D Pin Selection (GPIO_D_SEL)** There are two possible GPIOs that can be routed to the GPIO_D PM_SYNC state. This bit selects between them: 0: CPU_GP_3 (default) 1: CPU_GP_2 This field is not writeable when PM_SYNC_LOCK=1.
10	0b	RW/L	**GPIO_C Pin Selection (GPIO_C_SEL)** There are two possible GPIOs that can be routed to the GPIO_C PM_SYNC state. This bit selects between them: 0: CPU_GP_0 (default) 1: CPU_GP_1 This field is not writeable when PM_SYNC_LOCK=1.
9	0b	RW/L	**GPIO_B Pin Selection (GPIO_B_SEL)** There are two possible GPIOs that can be routed to the GPIO_B PM_SYNC state. This bit selects between them: 0: CPU_GP_2 (default) 1: CPU_GP_0 This field is not writeable when PM_SYNC_LOCK=1.
8	0b	RW/L	**GPIO_A Pin Selection (GPIO_A_SEL)** There are two possible GPIOs that can be routed to the GPIO_A PM_SYNC state. This bit selects between them: 0: CPU_GP_1 (default) 1: CPU_GP_3 This field is not writeable when PM_SYNC_LOCK=1.
7:0	-	-	**Reserved**

Chipset Initialization Register D0 (CIRD0) – Offset 18d0

BIOS may program this register.

Chipset Initialization Register D4 (CIRD4) – Offset 18d4

BIOS may program this register.

Power Management Configuration Reg 3 (PM_CFG3) – Offset 18e0

Bit Range	Default	Access	Field Name and Description
30:18	-	-	**Reserved**
17	0b	RW	**Host Wireless LAN Phy Power Enable (HOST_WLAN_PP_EN)** This policy bit is set by Host software when it desires the wireless LAN PHY to be powered in Sx power states for wakes over wireless LAN (WoWLAN). This bit is reset by DSW_PWROK de-assertion.
16	0b	RW	**Deep Sx WLAN Phy Power Enable (DSX_WLAN_PP_EN)** When set to '1, PMC will keep SLP_WLAN# high in deep-Sx to enable WoWLAN. Note: 1. This policy bit will be applied for Deep Sx entry from S3, S4 and S5. 2. This bit does not affect SLP_WLAN# behaviour in Sx after G3 or after a global reset 3. HOST_WLAN_PP_EN must be set when this bit is set. This bit is reset by DSW_PWROK de-assertion.
15:0	-	-	**Reserved**

Chipset Initialization Register E4 (CIRE4) – Offset 18e4

BIOS may program this register.

Power Management Configuration Reg 4 (PM_CFG4) – Offset 18e8

Bit Range	Default	Access	Field Name and Description
30	0b	RW	**USB2 PHY SUS Well Power Gating Enable (U2_PHY_PG_EN)** If this bit is 1, dynamic power gating of the USB2 PHY SUS well is enabled. Note: This bit prevents HW from initiating power gating entry. However, the USB2 PHY SUS well is power gated by default while in Sx after global_rst_b assertion. So HW will not spontaneously exit power gating while in Sx just because this bit is 0.
29:16	-	-	**Reserved**
15:12	8h	RW	**VccST Ramp Timer (VCCST_TMR)** This field determines the time from when SLP_S0# de-asserts until the CPU's VccST gated rail has ramped back up after being gated in C10. This timer starts when SLP_S0# asserts and has the effect of delaying any transactions on PM_SYNC until it expires. Encoding: 0h: 0us(disabled) 1h: 30us 2h: 35us 3h: 40us ... Fh: 100us Note: If the VccST bit in the CPU shutdown overrides virtual register is set to '1', the VccST gated domain will never be shut down (SLP_S0# will remain at '1' in C10). And so this timer will never start, allowing the PMC to send PM_SYNC traffic without waiting for this timer during C10 exit. This field is reset by PLTRST# assertion.
11:9	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
8:0	000h	RW	**CPU I/O VR Ramp Duration (CPU_IOVR_RAMP_DUR)** This value is used in the CPU I/O VR ramp timer and has a 10us granularity. Encoding: 000h: reserved 001h: 10us 002h: 20us 003h: 30us ... 1FFh: 5.1ms This field is reset by PLTRST# assertion.

CPU Early Power-on Configuration (CPU_EPOC) – Offset 18ec

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:3	00h	RW	**EPOC Data [7:3] (EPOC_DATA_7_3)**
2	-	-	**Reserved**
1:0	00b	RW	**EPOC Data [1:0] (EPOC_DATA_1_0)**

ACPI Timer Control (ACPI_TMR_CTL) – Offset 18fc

This register allows software to disable the ACPI Timer, which could result in power savings for the PCH.

This register is in the CORE power well and is reset by PLTRST#

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1	0b	RW	**ACPI Timer Disable (ACPI_TIM_DIS)** This bit determines whether the ACPI Timer is enabled to run. - 0: ACPI Timer is enabled (default) - 1: ACPI Timer is disabled (halted at the current value) Even when enabled, the timer only runs during S0. This bit must only be set to "1" if the operating system can tolerate disabling the 14.31818 MHz ACPI PM Timer. Note: 1.Some operating systems may only tolerate disabling the timer during entry into deep idle states. In such cases, the bit must be set to "1" during entry into those states and cleared to "0" during exit. This bit is reset by PLTRST# assertion.
0	0b	RW/1S/V	**ACPI Timer Clear (ACPI_TIM_CLR)** Writing a 1 to this bit will clear the ACPI Timer to all 0s. Hardware will automatically clear the bit back to 0 once the timer clear operation has completed. Writing a 0 to this bit has no effect. Implementation Note: The PCH must be capable of honoring this bit even while ACPI_TIM_DIS=1. This bit is reset by PLTRST# assertion.

Capability Disable Status 1 (N_STPG_FUSE_SS_DIS_RD_1) – Offset 1e40

Bit Range	Default	Access	Field Name and Description
30:18	-	-	**Reserved**
17	0b	RO/V	**PCIe Controller D Port 3 Disable ()** RO bit indicating if this PCIE port (single function) is disabled.
16	0b	RO/V	**PCIe Controller D Port 2 Disable ()** RO bit indicating if this PCIE port (single function) is disabled.
15	0b	RO/V	**PCIe Controller D Port 1 Disable ()** RO bit indicating if this PCIE port (single function) is disabled.
14	0b	RO/V	**PCIe Controller D Port 0 Disable ()** RO bit indicating if this PCIE port (single function) is disabled.
13	0b	RO/V	**PCIe Controller C Port 3 Disable ()** RO bit indicating if this PCIE port (single function) is disabled.
12	0b	RO/V	**PCIe Controller C Port 2 Disable ()** RO bit indicating if this PCIE port (single function) is disabled.
11	0b	RO/V	**PCIe Controller C Port 1 Disable ()** RO bit indicating if this PCIE port (single function) is disabled.
10	0b	RO/V	**PCIe Controller C Port 0 Disable ()** RO bit indicating if this PCIE port (single function) is disabled.
9	0b	RO/V	**PCIe Controller B Port 3 Disable ()** RO bit indicating if this PCIE port (single function) is disabled.
8	0b	RO/V	**PCIe Controller B Port 2 Disable ()** RO bit indicating if this PCIE port (single function) is disabled.
7	0b	RO/V	**PCIe Controller B Port 1 Disable ()** RO bit indicating if this PCIE port (single function) is disabled.
6	0b	RO/V	**PCIe Controller B Port 0 Disable ()** RO bit indicating if this PCIE port (single function) is disabled.

Bit Range	Default	Access	Field Name and Description
5	0b	RO/V	**PCIe Controller A Port 3 Disable ()** RO bit indicating if this PCIE port (single function) is disabled.
4	0b	RO/V	**PCIe Controller A Port 2 Disable ()** RO bit indicating if this PCIE port (single function) is disabled.
3	0b	RO/V	**PCIe Controller A Port 1 Disable ()** RO bit indicating if this PCIE port (single function) is disabled.
2	0b	RO/V	**PCIe Controller A Port 0 Disable ()** RO bit indicating if this PCIE port (single function) is disabled.
1:0	-	-	**Reserved**

Capability Disable Status 2 (STPG_FUSE_SS_DIS_RD_2) – Offset 1e44

Bit Range	Default	Access	Field Name and Description
30:20	-	-	**Reserved**
19	0b	RO/V	**XDCI Disable ()** RO bit indicating if XDCI function is disabled.
18:17	-	-	**Reserved**
16	0b	RO/V	**DSP Disable ()** RO bit indicating if DSP function is disabled.
15:14	-	-	**Reserved**
13	0b	RO/V	**LPC Disable ()** RO bit indicating if LPC function is disabled.

Bit Range	Default	Access	Field Name and Description
12:10	-	-	**Reserved**
9	0b	RO/V	**SMB Disable ()** RO bit indicating if SMB function is disabled.
8:7	-	-	**Reserved**
6	0b	RO/V	**Intel Serial I/O Disable ()** RO bit indicating if Intel Serial I/O function is disabled.
5	0b	RO/V	**EMMC Disable ()** RO bit indicating if EMMC function is disabled.
4	0b	RO/V	**CNVI Disable ()** RO bit indicating if CNVI function is disabled.
3	-	-	**Reserved**
2	0b	RO/V	**SD Controller Disable ()** RO bit indicating if SD Controller function is disabled.
1	0b	RO/V	**ISH Disable ()** RO bit indicating if ISH function is disabled.
0	0b	RO/V	**GBE Disable ()** RO bit indicating if GBE function is disabled.

SLP_S0# Debug 0 (SLP_S0_DBG_0) – Offset 10b4

This register captures the state of low power events involved in SLP_S0# entry to assist with debug. The status is captured as part of C10 entry(once CPU has entered package C10).

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
8	0b	RO	**eMMC D3 status (RSVD_EMMC_D3_STS)** This bit when 1 indicates that eMMC controller is in D3 state (taking static/function disables into account as well)
7:6	-	-	**Reserved**
5	0b	RO/V	**SATA controller D3 status (SATA_D3_STS)** This bit when 1 indicates that SATA controller is in D3 state (taking static/function disables into account as well)
4	0b	RO/V	**SD controller D3 status (SDX_D3_STS)** This bit when 1 indicates that SDX controller is in D3 state (taking static/function disables into account as well)
3	0b	RO/V	**I2C_UART_GSPI Controllers D3 status (LPIO_D3_STS)** This bit when 1 indicates that Intel(R) Serial I/O interface controller is in D3 state (taking static/function disables into account as well)
2	0b	RO/V	**xHCI controller D3 status (xHCI_D3_STS)** This bit when 1 indicates that XHCI controller is in D3 state (taking static/function disables into account as well)
1	0b	RO/V	**xDCI controller D3 status (OTG_D3_STS)** This bit when 1 indicates that OTG controller is in D3 state (taking static/function disables into account as well)
0	0b	RO/V	**Audio DSP (ADSP) controller D3 status (AUDIO_D3_STS)** This bit when 1 indicates that Audio DSP controller is in D3 state (taking static/function disables into account as well)

SLP_S0# Debug 1 (SLP_S0_DBG_1) – Offset 10b8

This register captures the state of low power events involved in SLP_S0# entry to assist with debug. The status is captured as part of C10 entry(once CPU has entered package C10).

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7	0b	RO/V	**PCIe external CLKREQs deasserted (PCIE_CLKREQS_OFF_STS)** This bit when 1 indicates that all external PCIe clock request pins are inactive.
6	0b	RO/V	**LPC output clocks gated status (LPC_CLKS_GATED_STS)** This bit when 1 indicates that external LPC clocks are gated.
5	0b	RO/V	**Crystal OFF Status (XOSC_OFF_STS)** This bit when 1 indicates that crystal oscillator has shut down .
4	0b	RO/V	**Root PLLs off (MAIN_PLL_OFF_STS)** This bit when 1 indicates that main PLL is off
3	0b	RO/V	**CPU BCLK PLL off (OC_PLL_OFF_STS)** This bit when 1 indicates that OC PLL is off
2	0b	RO/V	**Audio PLL OFF Status (AUDIO_PLL_OFF_STS)** This bit when 1 indicates that Audio PLL is off
1	0b	RO/V	**USB2 PLL OFF Status (USB2_PLL_OFF_STS)** This bit when 1 indicates that USB2 PLL is off
0	-	-	**Reserved**

SLP_S0# Debug 2 (SLP_S0_DBG_2) – Offset 10bc

This register captures the state of low power events involved in SLP_S0# entry to assist with debug. The status is captured as part of C10 entry(once CPU has entered package C10).

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13	0b	RO/V	**Platform Aggregated System Latency Tolerance value is greater than the Threshold (ASLT_GT_THRES_STS)** This bit when 1 indicates that the platform ASLT is greater than threashold

Bit Range	Default	Access	Field Name and Description
12	0b	RO/V	**PCH to CPU wake not pending. (PMSYNC_STATE_IDLE_STS)** This bit when 1 indicates that PMSYNC requests are not active.
11	-	-	**Reserved**
10	0b	RO/V	**CNVi specific wake request (CNV_VNN_REQ_STS)** This bit when 1 indicates that CNV VNN Req is active.
9	-	-	**Reserved**
8	0b	RO/V	**ISH specific wake request (ISH_VNN_REQ_STS)** This bit when 1 indicates that ISH Vnn Req is active.
7	-	-	**Reserved**
6	0b	RO/V	**PCIe Low Power Status (PCIE_LP_STS)** PCIe Root Port controllers are in low power state (power gated)
5	-	-	**Reserved**
4	0b	RO/V	**Gbe connection status (GBE_NO_LINK_STS)** This bit when 1 indicates that the GBE interface is disconected.
3:2	-	-	**Reserved**
1	0b	RO/V	**ME Power Gated Status (CSME_PG_STS)** This bit when 1 indicates that all power gated domains in Intel(R) ME are turned off.
0	0b	RO/V	**High Speed IO logic power gated status (MPHY_CORE_PG_STS)** This bit when 1 indicates that mphy core and data lanes are off.

VR Miscellaneous Control (VR_MISC_CTL) – Offset 1900

This register allows software to program various VR modes for the PCH. This register is in the PRIMARY power well and is

reset by RSMRST# assertion.

Bit Range	Default	Access	Field Name and Description
30:20	-	-	**Reserved**
19:18	0b	RO/V	**VCC_PRIM_0P85 Low Voltage Mode (VCC_PRIM_0P85_LVMT)** This bit indicates the the VCC_PRIM_0P85 Low Voltage Mode: 11 VCC_PRIM_0P85 Low Voltage Mode capability is Disabled 10 0.80V 01 0.75V 00 0.7V
17	-	-	**Reserved**
16	0b	RO/V	**VCC_PRIM_1P0 Low Voltage Mode Disable (VCC_PRIM_1P0_LVMDIS)** This bit indicates the VCC_PRIM_1P0 Low Voltage Mode Disable: 1 = VCC_PRIM_1P0 Low Voltage Mode capability is Disabled 0 = VCC_PRIM_1P0 Low Voltage Mode (0.9V) capability is Enabled
15:13	-	-	**Reserved**
12	1b	RO/V	**CORE VR Allowed (CORE_VR_ALLOWED)** This field reports the Separate Core VR support. 0 = PCH does not support a separate core VR. 1 = PCH supports a separate core VR
11:10	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
9:8	0b	RO/V	**CORE Voltage ID (CORE_VID)** This field reports the core voltage ID. 00 = 0.85V 01 = 0.90V 10 = 0.95V 11 = 1.00V These bits are only valid when CORE_VR_ALLOWED is 1.
7:4	-	-	**Reserved**
3	0b	RW	**VID status override enable (VIDSOVEN)** When set to 1 the bits in Primary VID Status Override (VIDSOV) are valid. This bit is reset by RSMRST# assertion.

Bit Range	Default	Access	Field Name and Description
2:0	0b	RW	**Primary VID status override (VIDSOV)** SW can program this register to reflect the actual voltage of the core power rail, VCCPRIM_CORE, if the system is not using the PCH VID control mechanism, CORE_VID1 and CORE_VID0. The accurate voltage is required for PCH power reporting. 000: 1.0V 001: 0.95V 010: 0.90V 011: 0.85V 100-111: Reserved The value in these bits is only used by PCH HW/FW when bit 3 of this register is set. This field is reset by RSMRST# assertion.

PMC SSRAM PCI Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device Vendor ID (DEVVENDID)	XXXX8086h
4h	4	Status and Command (STATUSCOMMAND)	0h
8h	4	Revision ID and Class Code (REVCLASSCODE)	5000000h
ch	4	Cache Line Latency Header and BIST (CLLATHEADERBIST)	0h
10h	4	32-bit Base Address Register (BAR)	0h
14h	4	BAR HIGH (BAR_HIGH)	0h
18h	4	32-bit Base Address Register1 (BAR1)	0h
1ch	4	BAR1 HIGH (BAR1_HIGH)	0h
2ch	4	Subsystem Identifiers (SUBSYSTEMID)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
34h	4	Capabilities Pointer (CAPABILITYPTR)	80h
3ch	4	Interrupt Register (INTERRUPTREG)	100h
80h	4	Power Management Capability ID (POWERCAPID)	48030001h
84h	4	PME Control and Status (PMECTRLSTATUS)	8h
90h	4	PCI Device Capability Record (PCIDEVIDLE_CAP_RECORD)	F0140009h
98h	4	D0I3_CONTROL_SW_LTR_MMIO_REG (D0I3_CONTROL_SW_LTR_MMIO_REG)	0h
9ch	4	Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)	0h
a0h	4	Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)	800h

Device Vendor ID (DEVVENDID) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:16	See Description	RO	**Device Identification (DEVICEID)** Indicates the value assigned to the controller. Refer to Device and Revision ID Table in Vol1 for default value.
15:0	8086h	RO	**Vendor Identification (VENDORID)** Indicates Intel

Status and Command (STATUSCOMMAND) – Offset 4

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29	0b	RW/1C	**Received Master Abort (RMA)**
28	0b	RW/1C	**Received Target Abort (RTA)**
27:20	-	-	**Reserved**
19	0b	RO	**Interrupt Status (INTR_STATUS)**
18:11	-	-	**Reserved**
10	0b	RW	**Interrupt Disable (INTR_DISABLE)**
9	-	-	**Reserved**
8	0b	RW/1C	**SERR# Enable (SERR_ENABLE)**
7:3	-	-	**Reserved**
2	0b	RW	**Bus Master Enable (BME)**
1	0b	RW	**Memory Space Enable (MSE)**
0	-	-	**Reserved**

Revision ID and Class Code (REVCLASSCODE) – Offset 8

Bit Range	Default	Access	Field Name and Description
31:8	050000h	RO	**Class Code (CLASS_CODES)** The register is read-only and is used to identify thegeneric function of the device.
7:0	See Description	RO	**Revision ID (RID)** Indicates stepping of the controller. Refer to the Device and Revision ID Table in Vol1 for specific value.

Cache Line Latency Header and BIST (CLLATHEADERBIST) – Offset c

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RO	**Multifunction Device (MULFNDEV)** 0 = Single Function Device 1 = Multi Function device
22:16	00h	RO	**Header Type (HEADERTYPE)**
15:8	00h	RO	**Latency Timer (LATTIMER)** Hard wired to 00h.
7:0	00h	RW	**Cache Line Size (CACHELINE_SIZE)**

32-bit Base Address Register (BAR) – Offset 10

Bit Range	Default	Access	Field Name and Description
30:12	00000h	RW	**Base Address (BASEADDR)** Software programs this register with the base address of the device's memory region

Bit Range	Default	Access	Field Name and Description
12:4	00h	RO	**Size Indicator (SIZEINDICATOR)** Hardwired to 0 to indicate 16KB of memory space
3	0b	RO	**Prefetchable (PREFETCHABLE)** Hardwired to 0 to indicate the device's memory space as notprefetchable.
2:1	00b	RO	**Type (TYPE)** Hardwired to 0 to indicate that Base register is 32 bits wide and mapping can be done anywhere in the 32-bit Memory Space.
0	0b	RO	**Memory Space Indicator (MESSAGE_SPACE)** Hardwired to 0 to identify a Memory BAR.

BAR HIGH (BAR_HIGH) – Offset 14

BAR -Base Address Register High

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Base Address HIGH (BASEADDR_HIGH)**

32-bit Base Address Register1 (BAR1) – Offset 18

Bit Range	Default	Access	Field Name and Description
31:12	00000h	RW	**BAR1 (BASEADDR1)** Software programs this register with the base address of the device's memory region
11:4	00h	RO	**Size Indicator (SIZEINDICATOR1)** Hardwired to 0 to indicate 16KB of memory space
3	0b	RO	**Prefetchable (PREFETCHABLE1)** Hardwired to 0 to indicate the device's memory space as notprefetchable.

Bit Range	Default	Access	Field Name and Description
2:1	00b	RO	**Type (TYPE1)** Hardwired to 0 to indicate that Base register is 32 bits wide and mapping can be done anywhere in the 32-bit Memory Space.
0	0b	RO	**Memory Space Indicator (MESSAGE_SPACE1)** Hardwired to 0 to identify a Memory BAR.

BAR1 HIGH (BAR1_HIGH) – Offset 1c

BAR1 -Base Address Register High

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Base Address HIGH (BASEADDR1_HIGH)**

Subsystem Identifiers (SUBSYSTEMID) – Offset 2c

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/O	**Subsystem ID (SUBSYSTEMID)** Written by BIOS. Not used by hardware.
15:0	0000h	RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID)** Written by BIOS.Not used by hardware.

Capabilities Pointer (CAPABILITYPTR) – Offset 34

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	80h	RO	**Capabilities Pointer (CAPPTR_POWER)** Indicates what the next capability is.This capability points to the PM Capability (0x80) structure.

Interrupt Register (INTERRUPTREG) – Offset 3c

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO	**Max Latency (MAX_LAT)** Value of 0 indicates device has no major requirementsfor the settings of latency timers
23:16	00h	RO	**Min Latency (MIN_GNT)** Value of 0 indicates device has no major requirementsfor the settings of latency timers
15:12	-	-	**Reserved**
11:8	1h	RO	**Interrupt Pin (INTPIN)**
7:0	00h	RW	**Interrupt Line (INTLINE)** Used to communicate to software the interrupt line that the interrupt pin is connected to.

Power Management Capability ID (POWERCAPID) – Offset 80

Bit Range	Default	Access	Field Name and Description
31:27	09h	RO	**PME Support (PMESUPPORT)**
26:19	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
18:16	3h	RW/1C	**Version (VERSION)** Indicates support for Revision 1.2 of the PCI PowerManagement Specification
15:8	00h	RO	**Next Capability (NXTCAP)** Points to the next capability structure. This points toNULL.
7:0	01h	RO	**Power Management Capability (POWER_CAP)** Indicates power managementcapability.

PME Control and Status (PMECTRLSTATUS) – Offset 84

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15	0h	RW/1C	**PME Status (PMESTATUS)**
14:9	-	-	**Reserved**
8	0h	RW	**PME Enable (PMEENABLE)**
7:4	-	-	**Reserved**
3	1h	RO	**No Soft Reset (NO_SOFT_RESET)** When set, this bit indicates that devicestransitioning from D3hot to D0 because of PowerState commands do not perform aninternal reset. Configuration Context is preserved.
2	-	-	**Reserved**
1:0	0h	RW	**Power State (POWERSTATE)** This field is used both to determine the currentpower state and to set a new power state.

PCI Device Capability Record (PCIDEVIDLE_CAP_RECORD) – Offset 90

Bit Range	Default	Access	Field Name and Description
31:28	Fh	RO	**Vendor Capability (VEND_CAP)** Indicates this is Vendor Specific capability.
27:24	0h	RO	**Revision ID (REVID)** Revision ID of capability structure
23:16	14h	RO	**Length (CAP_LENGTH)** Indicates the number of bytes in the capability structure.
15:8	00h	RO	**Next Capability (NEXT_CAP)** Points to the next capability structure. This points toNULL.
7:0	09h	RO	**Capability ID (CAPID)**

D0I3_CONTROL_SW_LTR_MMIO_REG (D0I3_CONTROL_SW_LTR_MMIO_REG) – Offset 98

SW LTR Update MMIO Location Register

Bit Range	Default	Access	Field Name and Description
31:4	0000000h	RO	**Location Pointer Offset (SW_LAT_DWORD_OFFSET)** This register contains thelocation pointer to the SW LTR register in MMIO space, as an offset from the specified BAR. The value of this register is a don't care, if the Valid bit is not set.
3:1	0h	RO	**Bar Number (SW_LAT_BAR_NUM)** Indicates that the SW LTR update MMIOlocation is always at BAR0.
0	0b	RO	**Valid (SW_LAT_VALID)** 0= not valid1= valid

Device IDLE pointer register (DEVICE_IDLE_POINTER_REG) – Offset 9c

Bit Range	Default	Access	Field Name and Description
31:4	0000000h	RO	**Device Idle Pointer (DWORD_OFFSET)** This register contains the location pointer tothe DevIdle register in MMIO space, as an offset from the specified BAR. The value ofthis register is a don't care, if the Valid bit is not set.
3:1	0h	RO	**BAR Number (BAR_NUM)** Indicates that the DevIdle update MMIO location isalways at BAR0
0	0b	RO	**Valid (VALID)** 0= not valid1= valid

Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG) – Offset a0

Bit Range	Default	Access	Field Name and Description
30:22	-	-	**Reserved**
21	0b	RW	**HAE (HAE)**
20	-	-	**Reserved**
19	0b	RW	**Sleep Enable (SLEEP_EN)**
18	0b	RW	**PG Enable (PGE)** If clear, then the controller will never request a PG. If set, thenthe controller may request PG when proper conditions are met. Note: This Bit mustbe set by BIOs for PG to function

Bit Range	Default	Access	Field Name and Description
17	0b	RW	**I3 Enable (I3_ENABLE)** If '1', then the function will power gate when idle and theDevIdle register (DevIdleC[2] = '1') is set.
16	0b	RW	**PME Request Enable (PMCRE)** If this bit is set to '1', the function will power gatewhen idle.
15:13	-	-	**Reserved**
12:10	2h	RW/O	**Power On Latency Scale (POW_LAT_SCALE)**
9:0	000h	RW/O	**Power On Latency Value (POW_LAT_VALUE)** This value is written by BIOS tocommunicate to the Driver.

Power Management Configuration Registers

The power management registers are distributed within the PCI Device 31: Function 2 space, with dedicated I/O and memory-mapped spaces.

Bits not explicitly defined in each register are assumed to be reserved. Writes to reserved bits must retain their previous values. Other than a read/modify/write, software should not attempt to use the value read from a reserved bit, as it may not be consistently 1 or 0.

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device Vendor ID (DEVVENDID)	XXXX8086h
4h	4	Status and Command (STATUSCOMMAND)	0h
8h	4	Class Code and Revision ID (REVCLASSCODE)	5800000h
ch	4	Cache Line Latency Header and BIST (CLLATHEADERBIST)	0h
10h	4	PWRMBASE (BAR)	0h
14h	4	PWRMBASE HIGH (BAR_HIGH)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
20h	4	BAR 2 (BAR2)	0h
2ch	4	Subsystem Identifiers (SUBSYSTEMID)	0h
34h	4	Capabilities Pointer (CAPABILITYPTR)	80h
3ch	4	Interrupt Register (INTERRUPTREG)	100h
80h	4	Power Management Capability ID (POWERCAPID)	48000001h
84h	4	PME Control Status (PMECTRLSTATUS)	8h
90h	4	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)	F0140009h
98h	4	SW LTR Update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)	0h
9ch	4	Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)	0h
a0h	4	D0I3_MAX_POW_LAT_PG_CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG)	800h

Device Vendor ID (DEVVENDID) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:16	See Description	RO	**Device Identification (DEVICEID)** This field identifies the particular device. Refer to the Device andRevision ID Table in Volume 1 for default value.
15:0	8086h	RO	**Vendor Identification (VENDORID)** This is a 16-bit value assigned to Intel. Intel VID=8086h.

Status and Command (STATUSCOMMAND) – Offset 4

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29	0b	RW/1C	**Received Master Abort (RMA)** Set when the bridge receives a completion with unsupported request status from the backbone. This bit is reset by PLTRST# assertion.
28	0b	RW/1C	**Received Target Abort (RTA)** Set when the bridge receives a completion with completer abort status from the backbone. This bit is reset by PLTRST# assertion.
27:20	-	-	**Reserved**
19	0b	RO	**Interrupt Status (INTR_STATUS)** This bit reflects state of interrupt in the device.
18:11	-	-	**Reserved**
10	0b	RW	**Interrupt Disable (INTR_DISABLE)** Setting this bit disable INTx assertion. The interrupt disabled is legacy INTx interrupt.
9	-	-	**Reserved**
8	0b	RW	**SERR Enable (SERR_ENABLE)** Not implemented.
7:3	-	-	**Reserved**
2	0b	RW	**Bus Master Enable (BME)** Bus master Enable does not apply to messages sent out by PMC. This bit is reset by PLTRST# assertion.

Bit Range	Default	Access	Field Name and Description
1	0b	RW	**Memory Space Enable (MSE)** Controls a device's response to Memory Space accesses. This bit controls whether the host to PMC MMIO BAR is enabled or not. This bit is reset by PLTRST# assertion.
0	-	-	**Reserved**

Class Code and Revision ID (REVCLASSCODE) – Offset 8

Bit Range	Default	Access	Field Name and Description
31:8	058000h	RO	**Class Code (CLASS_CODES)** Class Codes
7:0	See Description	RO	**Revision ID (RID)** Indicates stepping of the host controller. Refer to the Device and Revision ID Table in Volume 1 for specific value. This field is reset by PLTRST# assertion.

Cache Line Latency Header and BIST (CLLATHEADERBIST) – Offset c

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RO	**Multi-Function Device (MULFNDEV)** Indicates that this is part of a multi-function device.

Bit Range	Default	Access	Field Name and Description
22:16	00h	RO	**Header Type (HEADERTYPE)** Indicates a generic device header.
15:8	00h	RO	**Latency Timer (LATTIMER)** Hardwired to 0.
7:0	00h	RW	**Cache Line Size (CACHELINE_SIZE)**

PWRMBASE (BAR) – Offset 10

Base Address for MMIO Registers.

Bit Range	Default	Access	Field Name and Description
30:12	00000h	RW	**BAR (BASEADDR)** Software programs this register with the base address of the device's memory region
12:4	00h	RO	**Size Indicator (SIZEINDICATOR)** Hardwired to 0 to indicate 16KB of memory space
3	0b	RO	**Prefetchable (PREFETCHABLE)** A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables. Hardwired to 0 to indicate the device's memory space as notprefetchable.
2:1	00b	RO	**Type (TYPE)** Hardwired to 0 to indicate that Base register is 32 bits wide and mapping can be done anywhere in the 32-bit Memory Space.
0	0b	RO	**Memory Space Indicator (MESSAGE_SPACE)** Hardwired to 0 to identify a Memory BAR.

PWRMBASE HIGH (BAR_HIGH) – Offset 14

Base Address High for MMIO Registers.

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Base Address HIGH (BASEADDR_HIGH)** Base address high-MSB.

BAR 2 (BAR2) – Offset 20

Base Address for IO Space Registers.

Bit Range	Default	Access	Field Name and Description
31:7	0000000h	RW	**Base Address (BASEADDR)** This field is present if BAR is enabled.
6:1	-	-	**Reserved**
0	0h	RO	**Message Space (MESSAGE_SPACE)** 0 indicates this BAR is present in the memory space.

Subsystem Identifiers (SUBSYSTEMID) – Offset 2c

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/O	**Subsystem ID (SUBSYSTEMID)** Written by BIOS. Not used by hardware.
15:0	0000h	RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID)** Written by BIOS.Not used by hardware.

Capabilities Pointer (CAPABILITYPTR) – Offset 34

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	80h	RO	**Power Management Capability Pointer (CAPPTR_POWER)** Indicates what the next capability is.

Interrupt Register (INTERRUPTREG) – Offset 3c

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**
11:8	1h	RO	**Interrupt Pin (INTPIN)** Interrupt Pin Value in this register is reflected from IPIN value in the private configuration space. For a single function device, this ideally is INTA.
7:0	00h	RW	**Interrupt Line (INTLINE)** It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

Power Management Capability ID (POWERCAPID) – Offset 80

Bit Range	Default	Access	Field Name and Description
31:27	09h	RO	**PME Support (PMESUPPORT)** This 5-bit field indicates the power states in which the function can assert the PME#.
26:16	-	-	**Reserved**
15:8	00h	RO	**Next Capability (NXTCAP)** Points to the next capability structure.
7:0	01h	RO	**Power Management Capability (POWER_CAP)** Indicates this is power management capability.

PME Control Status (PMECTRLSTATUS) – Offset 84

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15	0h	RW/1C	**PME Status (PMESTATUS)** This bit indicates the PME status.
14:9	-	-	**Reserved**
8	0h	RW	**PME Enable (PMEENABLE)** This bit has no impact to HW.
7:4	-	-	**Reserved**
3	1h	RO	**No Software Reset (NO_SOFT_RESET)**
2	-	-	**Reserved**
1:0	0h	RW	**Power State (POWERSTATE)** This field is used both to determine the current power state and to set a new power state.

PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD) – Offset 90

Bit Range	Default	Access	Field Name and Description
31:28	Fh	RO	**Vendor Capability (VEND_CAP)** Vendor Specific Capability ID.
27:24	0h	RO	**Revision ID (REVID)** Revision ID of capability structure.

Bit Range	Default	Access	Field Name and Description
23:16	14h	RO	**Capability Length (CAP_LENGTH)** Vendor Specific capability Length.
15:8	00h	RO	**Next Capability (NEXT_CAP)** Points to the next capability structure.
7:0	09h	RO	**Capability ID (CAPID)** Indicates PCI Device Idle Capability ID.

SW LTR Update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG) – Offset 98

Bit Range	Default	Access	Field Name and Description
31:4	0000000h	RO	**Location Pointer Offset (SW_LAT_DWORD_OFFSET)** SW LTR Update MMIO Offset Location
3:1	0h	RO	**Bar Number (SW_LAT_BAR_NUM)** Indicates that the SW LTR update MMIO location is always at BAR0.
0	0b	RO	**Valid (SW_LAT_VALID)** This value is reflected from the SW LTR valid strap at the top level.

Device IDLE pointer register (DEVICE_IDLE_POINTER_REG) – Offset 9c

Bit Range	Default	Access	Field Name and Description
31:4	0000000h	RO	**Device Idle Pointer (DWORD_OFFSET)** Contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR.
3:1	0h	RO	**Bar Number (BAR_NUM)** Indicates that the D0i3 MMIO location is always at BAR0.

Bit Range	Default	Access	Field Name and Description
0	0b	RO	**VALID (VALID)** 0 = Not valid 1 = Valid

D0I3_MAX_POW_LAT_PG_CONFIG (D0I3_MAX_POW_LAT_PG_CONFIG) – Offset a0

DEVICE PG CONFIG

Bit Range	Default	Access	Field Name and Description
30:22	-	-	**Reserved**
21	0b	RW	**Hardware Autonomous Enable (HAE)** If set, then the PGCB may request a PG whenever it is idle.
20	-	-	**Reserved**
19	0b	RW	**Sleep Enable (SLEEP_EN)** If clear, then IP will never asset Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing.
18	0b	RW	**PG Enable (PGE)** If clear, then IP will never request a PG. If set, then IP may request PG when proper conditions are met.
17	0b	RW	**D3-Hot Enable (I3_ENABLE)** If 1, then function will power gate when idle and the POWERSTATE bits in the function = 11(D3).
16	0b	RW	**PMC Request Enable (PMCRE)** If this bit is set to '1', the function will power gate when idle.
15:13	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
12:10	2h	RW/O	**Power On Latency Scale (POW_LAT_SCALE)** This value is written by BIOS to communicate to the driver.
9:0	000h	RW/O	**Power On Latency Value (POW_LAT_VALUE)** This value is written by BIOS to communicate to the driver.

Processor Interface Memory Registers

Summary of Bus:, Device:, Function: (IO)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
61h	1	NMI Status and Control (NMI_STS_CNT)	0h
70h	1	NMI Enable (and Real Time Clock Index) (NMI_EN)	80h
92h	1	Init Register (PORT92)	0h
cf9h	1	Reset Control Register (RST_CNT)	0h

NMI Status and Control (NMI_STS_CNT) – Offset 61

NMI Status and Control Register

Bit Range	Default	Access	Field Name and Description
7	0b	RO	**SERR# NMI Source Status (SERR_NMI_STS)** This bit is set by any of the sources of the internal SERR on the PCH backbone, this includes SERR assertions forwarded from the secondary PCI bus, error from a PCIe port, Do_SERR or standard PCIe error message from DMI, or internal Bus 0 functions that generate SERR#. Bit 2 must be cleared in this register in order for this bit to be set. This interrupt source is enabled by setting bit 2 to 0. To reset the interrupt, set bit 2 to 1 and then set it to 0. This bit is read-only. When writing to port 61h, this bit must be 0.

Bit Range	Default	Access	Field Name and Description
6	0b	RO	**IOCHK# NMI Source Status (IOCHK_NMI_STS)** This bit is set if an ISA agent (via SERIRQ) asserts IOCHK# and bit 3 is cleared in this register. This interrupt source is enabled by setting bit 3 to 0. To reset the interrupt, set bit 3 to 1 and then set it to 0. This bit is read-only. When writing to port 61h, this bit must be a 0.
5	0b	RO	**Timer Counter 2 OUT Status (TMR2_OUT_STS)** This bit reflects the current state of the 8254 counter 2 output. Counter 2 must be programmed following any PCI reset for this bit to have a determinate value. When writing to port 61h, this bit must be a 0.
4	-	-	**Reserved**
3	0b	RW	**IOCHK# NMI Enable (IOCHK_NMI_EN)** When this bit is a 1, IOCHK# NMIs are disabled and cleared. When this bit is a 0, IOCHK# NMIs are enabled.
2	0b	RW	**PCI SERR# Enable (PCI_SERR_EN)** When this bit is a 1, the SERR# NMIs are disabled and cleared. When this bit is a 0, SERR# NMIs are enabled.
1	0b	RW	**Speaker Data Enable (SPKR_DAT_EN)** When this bit is a 0, the SPKR output is a 0. When this bit is a 1, the SPKR output is equivalent to the Counter 2 OUT signal value.
0	0b	RW	**Timer Counter 2 Enable (TIM_CNT2_EN)** When this bit is a 0, Counter 2 counting is disabled. Counting is enabled when this bit is 1.

NMI Enable (and Real Time Clock Index) (NMI_EN) – Offset 70

This register is write-only for normal operation. In Alt-Access mode, this register can be read to find the NMI Enable status and the RTC index value.

*Read/Write (Special), Use RW/V because there is no equivalent register access attribute in RDL

Bit Range	Default	Access	Field Name and Description
7	1b	RW/V	**NMI_EN# (NMI_EN)** When this bit is a 1, all NMI sources are disabled. When this bit is a 0, NMI sources are enabled.
6:0	0000000b	RW/V	**Real Time Clock Index (Address) (RTC_INDX)** This data goes to the RTC to select which register or CMOS RAM address is being accessed.

Init Register (PORT92) – Offset 92

Bit Range	Default	Access	Field Name and Description
6:1	-	-	**Reserved**
0	0b	RW	**INIT NOW (INIT_NOW)** When this bit transitions from a 0 to a 1, the PCH will force INIT# active for 16 PCI clocks.

Reset Control Register (RST_CNT) – Offset cf9

Bit Range	Default	Access	Field Name and Description
6:4	-	-	**Reserved**
3	0b	RW	**Full Reset (FULL_RST)** When this bit is set to 1 and bit 1 is set to 1 (indicating Hard Reset, not Soft Reset), and the RST_CPU bit (bit 2) is written from 0 to 1, the PCH will do a full reset, including driving SLP_S3#, SLP_S4# and SLP_S5# active (low) for at least 3 (and no more than 5) seconds. When this bit is set, it also causes the full power cycle (SLP_S3/4/5# assertion) in response to SYSRESET#, PWROK#, and Watchdog timer reset sources.

Bit Range	Default	Access	Field Name and Description
2	0b	RW	**Reset CPU (RST_CPU)** This bit will cause either a hard or soft reset to the CPU depending on the state of the SYS_RST bit (bit 1 in this same register). The software will cause the reset by setting bit 2 from a 0 to a 1.
1	0b	RW	**System Reset (SYS_RST)** Ths bit determines the type of reset caused via RST_CPU (bit 2 of this register). If SYS_RST is 0 when RST_CPU goes from 0 to 1, then the PCH will force INIT# active for 16 PCI clocks. If SYS_RST is 1 when RST_CPU goes from 0 to 1, then the PCH will force PCI reset active for about 1 ms, however the SLP_S3#, SLP_S4# and SLP_S5# signals assertion is dependent on the value of the FULL_RST (bit3 of this register).
0	-	-	**Reserved**

PSF1 Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
31ch	4	D22:F0 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F0_OFFSET3)	0h
41ch	4	D22:F1 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F1_OFFSET4)	0h
51ch	4	D22:F2 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_PTIO_RS0_D22_F2_OFFSET5)	0h
61ch	4	D22:F3 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_PTIO_RS0_D22_F3_OFFSET6)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
71ch	4	D22:F4 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F4_OFFSET7)	0h
81ch	4	D22:F5 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F5_OFFSET8)	0h
a1ch	4	D18:F0 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_KVMCC_RS3_D18_F0_OFFSET10)	0h
1f1ch	4	D23:F0 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_VR_RS0_D23_F0_OFFSET31)	0h
203ch	4	D28:F0 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F0_OFFSET32)	0h
213ch	4	D28:F1 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F1_OFFSET33)	0h
223ch	4	D28:F2 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F2_OFFSET34)	0h
233ch	4	D28:F3 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F3_OFFSET35)	0h
243ch	4	D28:F4 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F4_OFFSET36)	0h
253ch	4	D28:F5 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F5_OFFSET37)	0h
263ch	4	D28:F6 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F6_OFFSET38)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
273ch	4	D28:F7 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F7_OFFSET39)	0h
283ch	4	D29:F0 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F0_OFFSET40)	0h
293ch	4	D29:F1 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F1_OFFSET41)	0h
2a3ch	4	D29:F2 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F2_OFFSET42)	0h
2b3ch	4	D29:F3 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F3_OFFSET43)	0h
2c3ch	4	D29:F4 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPD_RS0_D29_F4_OFFSET44)	0h
2d3ch	4	D29:F5 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPD_RS0_D29_F5_OFFSET45)	0h
2e3ch	4	D29:F6 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPD_RS0_D29_F6_OFFSET46)	0h
2f3ch	4	D29:F7 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPD_RS0_D29_F7_OFFSET47)	0h
4020h	4	PSF Port 0 Configuration 0 (PSF_1_PSF_PORT_CONFIG_PG0_PORT0)	0h
4024h	4	PSF Port 0 Configuration 1 (PSF_1_PSF_PORT_CONFIG_PG1_PORT0)	0h
4028h	4	PSF Port 1 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT1)	0h
402ch	4	PSF Port 2 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT2)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4030h	4	PSF Port 3 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT3)	0h
4034h	4	PSF Port 4 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT4)	0h
4038h	4	PSF Port 5 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT5)	0h
403ch	4	PSF Port 6 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT6)	0h
4040h	4	PSF Port 7 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT7)	0h
4044h	4	PSF Port 8 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT8)	0h
4048h	4	PSF Port 9 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT9)	0h
406ch	4	Destination ID (PSF_1_PSF_MC_AGENT_MCAST0_RS0_TGT2_EOI)	0h

D22:F0 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F0_OFFSET3) – Offset 31c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable. (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D22:F1 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F1_OFFSET4) – Offset 41c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable. (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D22:F2 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_PTIO_RS0_D22_F2_OFFSET5) – Offset 51c

Controls the T0 PCI memory and IO space settings

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D22:F3 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_PTIO_RS0_D22_F3_OFFSET6) – Offset 61c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable. (FunDis)** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through IOSF SB interface only.
7:0	-	-	**Reserved**

D22:F4 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F4_OFFSET7) – Offset 71c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable. (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D22:F5 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F5_OFFSET8) – Offset 81c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable. (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D18:F0 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_KVMCC_RS3_D18_F0_OFFSET10) – Offset a1c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable. (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D23:F0 PCI Configuration Space Enable (PSF_1_AGNT_T0_SHDW_PCIEN_VR_RS0_D23_F0_OFFSET31) – Offset 1f1c

Controls the T0 PCI memory and IO space settings

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable. (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D28:F0 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F0_OFFSET32) – Offset 203c

Controls the T1 PCI memory and IO space settings

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable. (FunDis)** Default value=0x0. This bit is writable through both SB interface and through cfgWr transactions.
7:2	-	-	**Reserved**
1	0x0	RW	**Memory Space Enable. (MemEn)** Default value=0x0. This bit is writable through both SB interface and through cfgWr transactions.
0	0x0	RW	**IO Space Enable. (IOEn)** Default value=0x0. This bit is writable through both SB interface and through cfgWr transactions.

D28:F1 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F1_OFFSET33) – Offset 213c

Same definition as D28:F0 PCI Configuration Space Enable.

D28:F2 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F2_OFFSET34) – Offset 223c

Same definition as D28:F0 PCI Configuration Space Enable.

D28:F3 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPA_RS0_D28_F3_OFFSET35) – Offset 233c

Same definition as D28:F0 PCI Configuration Space Enable.

D28:F4 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F4_OFFSET36) – Offset 243c

Same definition as D28:F0 PCI Configuration Space Enable.

D28:F5 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F5_OFFSET37) – Offset 253c

Same definition as D28:F0 PCI Configuration Space Enable.

D28:F6 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F6_OFFSET38) – Offset 263c

Same definition as D28:F0 PCI Configuration Space Enable.

D28:F7 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPB_RS0_D28_F7_OFFSET39) – Offset 273c

Same definition as D28:F0 PCI Configuration Space Enable.

D29:F0 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F0_OFFSET40) – Offset 283c

Same definition as D28:F0 PCI Configuration Space Enable.

D29:F1 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F1_OFFSET41) – Offset 293c

Same definition as D28:F0 PCI Configuration Space Enable.

D29:F2 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F2_OFFSET42) – Offset 2a3c

Same definition as D28:F0 PCI Configuration Space Enable.

D29:F3 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPC_RS0_D29_F3_OFFSET43) – Offset 2b3c

Same definition as D28:F0 PCI Configuration Space Enable.

D29:F4 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPD_RS0_D29_F4_OFFSET44) – Offset 2c3c

Same definition as D28:F0 PCI Configuration Space Enable.

D29:F5 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPD_RS0_D29_F5_OFFSET45) – Offset 2d3c

Same definition as D28:F0 PCI Configuration Space Enable.

D29:F6 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPD_RS0_D29_F6_OFFSET46) – Offset 2e3c

Same definition as D28:F0 PCI Configuration Space Enable.

D29:F7 PCI Configuration Space Enable (PSF_1_AGNT_T1_SHDW_PCIEN_SPD_RS0_D29_F7_OFFSET47) – Offset 2f3c

Same definition as D28:F0 PCI Configuration Space Enable.

PSF Port 0 Configuration 0 (PSF_1_PSF_PORT_CONFIG_PG0_PORT0) – Offset 4020

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**
2	0x0	RW	**Egress Force Relax Ordering (EgressFRO)** If set, IOSF relaxed ordering will be forced for outgoing transactions, regardless of the relaxed ordering (RO) attribute on the IOSF interface. Egress Force Relax Ordering is only applicable for PSF port types with buffering.
1	0x0	RW	**Ingress Force Relax Ordering (IngressFRO)** If set, IOSF relaxed ordering will be forced for incoming transactions, regardless of the relaxed ordering (RO) attribute on the IOSF interface.
0	-	-	**Reserved**

PSF Port 0 Configuration 1 (PSF_1_PSF_PORT_CONFIG_PG1_PORT0) – Offset 4024

Applied to Port 0. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 1 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT1) – Offset 4028

Applied to Port 1. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 2 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT2) – Offset 402c

Applied to Port 2. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 3 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT3) – Offset 4030

Applied to Port 3. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 4 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT4) – Offset 4034

Applied to Port 4. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 5 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT5) – Offset 4038

Applied to Port 5. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 6 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT6) – Offset 403c

Applied to Port 6. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 7 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT7) – Offset 4040

Applied to Port 7. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 8 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT8) – Offset 4044

Applied to Port 8. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 9 Configuration (PSF_1_PSF_PORT_CONFIG_PG1_PORT9) – Offset 4048

Applied to Port 9. Same definition as PSF Port 0 Configuration register at offset 4020h.

Destination ID (PSF_1_PSF_MC_AGENT_MCAST0_RS0_TGT2_EOI) – Offset 406c

This register specifies a full PSF port destination ID in the format psf_id:port_group_id:port_id:channel_id.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30:15	-	-	**Reserved**
14:8	0x0	RW	**Port ID (PortID)** Default value=0x0, Since 1'b0 indicates source-decode, the port ID needs to be larger than 0
7:0	0x0	RW	**Channel ID (ChannelID)** Default value=0x0,

PSF2 Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4028h	4	PSF Port 1 Configuration (PSF_2_PSF_PORT_CONFIG_PG1_PORT1)	0h
402ch	4	PSF Port 2 Configuration (PSF_2_PSF_PORT_CONFIG_PG1_PORT2)	0h
4030h	4	PSF Port 3 Configuration (PSF_2_PSF_PORT_CONFIG_PG1_PORT3)	0h
4034h	4	PSF Port 4 Configuration (PSF_2_PSF_PORT_CONFIG_PG1_PORT4)	0h
4038h	4	PSF Port 5 Configuration (PSF_2_PSF_PORT_CONFIG_PG1_PORT5)	0h
11ch	4	D18:F0 PCI Configuration Space Enable (PSF_2_AGNT_T0_SHDW_PCIEN_TRH_RS0_D18_F0_OFFSET1)	0h
21ch	4	D18:F5 PCI Configuration Space Enable (PSF_2_AGNT_T0_SHDW_PCIEN_UFSX2_RS0_D18_F5_OFFSET2)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
31ch	4	D20:F0 PCI Configuration Space Enable (PSF_2_AGNT_T0_SHDW_PCIEN_XHCI_RS0_D20_F0_OFFSET3)	0h
41ch	4	D20:F1 PCI Configuration Space Enable (PSF_2_AGNT_T0_SHDW_PCIEN_XDCI_RS0_D20_F1_OFFSET4)	0h
51ch	4	D20:F4 PCI Configuration Space Enable (PSF_2_AGNT_T0_SHDW_PCIEN_NPK_RS0_D20_F4_OFFSET5)	0h
61ch	4	D26:F0 PCI Configuration Space Enable (PSF_2_AGNT_T0_SHDW_PCIEN_EMMC_RS0_D26_F0_OFFSET6)	0h
71ch	4	D31:F7 PCI Configuration Space Enable (PSF_2_AGNT_T0_SHDW_PCIEN_NPK_RS0_D31_F7_OFFSET7)	0h
403ch	4	PSF Port 6 Configuration (PSF_2_PSF_PORT_CONFIG_PG1_PORT6)	0h
4040h	4	PSF Port 7 Configuration (PSF_2_PSF_PORT_CONFIG_PG1_PORT7)	0h
4014h	4	Rootspace Configuration (PSF_2_ROOTSPACE_CONFIG_RS0)	2h
4020h	4	PSF Port 0 Configuration 0 (PSF_2_PSF_PORT_CONFIG_PG0_PORT0)	0h
4024h	4	PSF Port 0 Configuration 1 (PSF_2_PSF_PORT_CONFIG_PG1_PORT0)	0h

PSF Port 1 Configuration (PSF_2_PSF_PORT_CONFIG_PG1_PORT1) – Offset 4028

Applied to Port 1. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 2 Configuration (PSF_2_PSF_PORT_CONFIG_PG1_PORT2) – Offset 402c

Applied to Port 2. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 3 Configuration (PSF_2_PSF_PORT_CONFIG_PG1_PORT3) – Offset 4030

Applied to Port 3. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 4 Configuration (PSF_2_PSF_PORT_CONFIG_PG1_PORT4) – Offset 4034

Applied to Port 4. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 5 Configuration (PSF_2_PSF_PORT_CONFIG_PG1_PORT5) – Offset 4038

Applied to Port 5. Same definition as PSF Port 0 Configuration register at offset 4020h.

D18:F0 PCI Configuration Space Enable (PSF_2_AGNT_T0_SHDW_PCIEN_TRH_RS0_D18_F0_OFFSET1) – Offset 11c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable. (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D18:F5 PCI Configuration Space Enable (PSF_2_AGNT_T0_SHDW_PCIEN_UFSX2_RS0_D18_F5_OFFSET2) – Offset 21c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
8	0x0	RW	**Function Disable. (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D20:F0 PCI Configuration Space Enable (PSF_2_AGNT_T0_SHDW_PCIEN_XHCI_RS0_D20_F0_OFFSET3) – Offset 31c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable. (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D20:F4 PCI Configuration Space Enable (PSF_2_AGNT_T0_SHDW_PCIEN_NPK_RS0_D20_F4_OFFSET5) – Offset 51c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
8	0x0	RW	**Function Disable. (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

PSF Port 6 Configuration (PSF_2_PSF_PORT_CONFIG_PG1_PORT6) – Offset 403c

Applied to Port 6. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 7 Configuration (PSF_2_PSF_PORT_CONFIG_PG1_PORT7) – Offset 4040

Applied to Port 7. Same definition as PSF Port 0 Configuration register at offset 4020h.

Rootspace Configuration (PSF_2_ROOTSPACE_CONFIG_RS0) – Offset 4014

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1	0x1	RW	**Enable Address-based Peer-to-Peer (EnAddrP2p)** Default value=0x1, If set, address-based p2p transactions are allowed for this root space.
0	0x0	RW	**VT-D Enable (VtdEn)** Default value=0x0, If set Intel Virtualization Technology for Directed I/O is enabled for this root space. This bit should reflect the system-wide vt-d setting, and is typically maintained by BIOS

PSF Port 0 Configuration 0 (PSF_2_PSF_PORT_CONFIG_PG0_PORT0) – Offset 4020

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**
2	0x0	RW	**Egress Force Relax Ordering (EgressFRO)** If set, IOSF relaxed ordering will be forced for outgoing transactions, regardless of the relaxed ordering (RO) attribute on the IOSF interface. Egress Force Relax Ordering is only applicable for PSF port types with buffering.
1	0x0	RW	**Ingress Force Relax Ordering (IngressFRO)** If set, IOSF relaxed ordering will be forced for incoming transactions, regardless of the relaxed ordering (RO) attribute on the IOSF interface.
0	-	-	**Reserved**

PSF Port 0 Configuration 1 (PSF_2_PSF_PORT_CONFIG_PG1_PORT0) – Offset 4024

Applied to Port 0. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF3 Registers

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
121ch	4	D31:F0 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_SPI_RS0_D31_F0_OFFSET18)	0h
131ch	4	D31:F1 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_P2S_RS0_D31_F1_OFFSET19)	0h
1400h	4	Offset 1400h: PCI BAR (PSF_3_AGNT_T0_SHDW_BAR0_PMC_RS0_D31_F2_OFFSET20)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
141ch	4	D31:F2 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_PMC_RS0_D31_F2_OFFSET20)	0h
151ch	4	D31:F3 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_AUD_RS0_D31_F3_OFFSET21)	0h
161ch	4	D31:F4 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_SMB_RS0_D31_F4_OFFSET22)	0h
171ch	4	D31:F5 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_SPI_RS0_D31_F5_OFFSET23)	0h
11ch	4	D18:F6 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D18_F6_OFFSET1)	0h
21ch	4	D19:F0 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_ISH_RS0_D19_F0_OFFSET2)	0h
31ch	4	D20:F2 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_PMC_RS0_D20_F2_OFFSET3)	0h
41ch	4	D20:F3 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_CNVI_RS0_D20_F3_OFFSET4)	0h
51ch	4	D20:F5 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_SDX_RS0_D20_F5_OFFSET5)	0h
61ch	4	D21:F0 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F0_OFFSET6)	0h
71ch	4	D21:F1 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F1_OFFSET7)	0h
181ch	4	D31:F6 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_GBE_RS0_D31_F6_OFFSET24)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
191ch	4	D19:F0 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_ISH_RS1_D19_F0_OFFSET25)	0h
4020h	4	PSF Port 0 Configuration (PSF_3_PSF_PORT_CONFIG_PG0_PORT0)	0h
4024h	4	PSF Port 0 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT0)	0h
4028h	4	PSF Port 1 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT1)	0h
402ch	4	PSF Port 2 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT2)	0h
81ch	4	D21:F2 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F2_OFFSET8)	0h
91ch	4	D21:F3 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F3_OFFSET9)	0h
a1ch	4	D25:F0 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F0_OFFSET10)	0h
b1ch	4	D25:F1 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F1_OFFSET11)	0h
c1ch	4	D25:F2 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F2_OFFSET12)	0h
d1ch	4	D30:F0 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F0_OFFSET13)	0h
e1ch	4	D30:F1 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F1_OFFSET14)	0h
4030h	4	PSF Port 3 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT3)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4034h	4	PSF Port 4 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT4)	0h
4038h	4	PSF Port 5 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT5)	0h
403ch	4	PSF Port 6 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT6)	0h
4040h	4	PSF Port 7 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT7)	0h
4044h	4	PSF Port 8 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT8)	0h
4048h	4	PSF Port 9 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT9)	0h
404ch	4	PSF Port 10 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT10)	0h
4050h	4	PSF Port 11 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT11)	0h
4054h	4	PSF Port 12 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT12)	0h
f1ch	4	D30:F2 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F2_OFFSET15)	0h
101ch	4	D30:F3 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F3_OFFSET16)	0h

D31:F0 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_SPI_RS0_D31_F0_OFFSET18) – Offset 121c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D31:F1 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_P2S_RS0_D31_F1_OFFSET19) – Offset 131c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

Offset 1400h: PCI BAR (PSF_3_AGNT_T0_SHDW_BAR0_PMC_RS0_D31_F2_OFFSET20) – Offset 1400

PCI Base Address Register

Bit Range	Default	Access	Field Name and Description
31:13	0x0	RW	**Address Base (AddrBase)** PCI base address.

Bit Range	Default	Access	Field Name and Description
12:0	-	-	**Reserved**

D31:F2 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_PMC_RS0_D31_F2_OFFSET20) – Offset 141c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D31:F3 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_AUD_RS0_D31_F3_OFFSET21) – Offset 151c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D31:F4 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_SMB_RS0_D31_F4_OFFSET22) – Offset 161c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D31:F5 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_SPI_RS0_D31_F5_OFFSET23) – Offset 171c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D18:F6 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D18_F6_OFFSET1) – Offset 11c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D19:F0 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_ISH_RS0_D19_F0_OFFSET2) – Offset 21c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D20:F2 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_PMC_RS0_D20_F2_OFFSET3) – Offset 31c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D20:F3 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_CNVI_RS0_D20_F3_OFFSET4) – Offset 41c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D20:F5 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_SDX_RS0_D20_F5_OFFSET5) – Offset 51c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D21:F0 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F0_OFFSET6) – Offset 61c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D21:F1 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F1_OFFSET7) – Offset 71c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D31:F6 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_GBE_RS0_D31_F6_OFFSET24) – Offset 181c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D19:F0 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_ISH_RS1_D19_F0_OFFSET25) – Offset 191c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

PSF Port 0 Configuration (PSF_3_PSF_PORT_CONFIG_PG0_PORT0) – Offset 4020

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**
2	0x0	RW	**Egress Force Relax Ordering (EgressFRO)** If set, IOSF relaxed ordering will be forced for outgoing transactions, regardless of the relaxed ordering (RO) attribute on the IOSF interface. Egress Force Relax Ordering is only applicable for PSF port types with buffering.
1	0x0	RW	**Ingress Force Relax Ordering (IngressFRO)** If set, IOSF relaxed ordering will be forced for incoming transactions, regardless of the relaxed ordering (RO) attribute on the IOSF interface.
0	-	-	**Reserved**

PSF Port 0 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT0) – Offset 4024

Applied to Port 0. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 1 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT1) – Offset 4028

Applied to Port 1. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 2 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT2) – Offset 402c

Applied to Port 2. Same definition as PSF Port 0 Configuration register at offset 4020h.

D21:F2 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F2_OFFSET8) – Offset 81c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D21:F3 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F3_OFFSET9) – Offset 91c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D25:F0 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F0_OFFSET10) – Offset a1c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D25:F1 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F1_OFFSET11) – Offset b1c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D25:F2 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F2_OFFSET12) – Offset c1c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D30:F0 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F0_OFFSET13) – Offset d1c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D30:F1 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F1_OFFSET14) – Offset e1c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

PSF Port 3 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT3) – Offset 4030

Applied to Port 3. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 4 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT4) – Offset 4034

Applied to Port 4. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 5 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT5) – Offset 4038

Applied to Port 5. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 6 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT6) – Offset 403c

Applied to Port 6. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 7 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT7) – Offset 4040

Applied to Port 7. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 8 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT8) – Offset 4044

Applied to Port 8. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 9 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT9) – Offset 4048

Applied to Port 9. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 10 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT10) – Offset 404c

Applied to Port 10. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 11 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT11) – Offset 4050

Applied to Port 11. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 12 Configuration (PSF_3_PSF_PORT_CONFIG_PG1_PORT12) – Offset 4054

Applied to Port 12. Same definition as PSF Port 0 Configuration register at offset 4020h.

D30:F2 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F2_OFFSET15) – Offset f1c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

D30:F3 PCI Configuration Space Enable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F3_OFFSET16) –

Offset 101c

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0x0	RW	**Function Disable (FunDis)** When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	-	-	**Reserved**

PSF4 Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4020h	4	PSF Port 0 Configuration (PSF_4_PSF_PORT_CONFIG_PG0_PORT0)	0h
4024h	4	PSF Port 0 Configuration (PSF_4_PSF_PORT_CONFIG_PG1_PORT0)	0h
4028h	4	PSF Port 1 Configuration (PSF_4_PSF_PORT_CONFIG_PG1_PORT1)	0h
402ch	4	PSF Port 2 Configuration (PSF_4_PSF_PORT_CONFIG_PG1_PORT2)	0h
4030h	4	PSF Port 3 Configuration (PSF_4_PSF_PORT_CONFIG_PG1_PORT3)	0h
4034h	4	PSF Port 4 Configuration (PSF_4_PSF_PORT_CONFIG_PG1_PORT4)	0h

PSF Port 0 Configuration (PSF_4_PSF_PORT_CONFIG_PG0_PORT0) – Offset 4020

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**
2	0x0	RW	**Egress Force Relax Ordering (EgressFRO)** If set, IOSF relaxed ordering will be forced for outgoing transactions, regardless of the relaxed ordering (RO) attribute on the IOSF interface. Egress Force Relax Ordering is only applicable for PSF port types with buffering.
1	0x0	RW	**Ingress Force Relax Ordering (IngressFRO)** If set, IOSF relaxed ordering will be forced for incoming transactions, regardless of the relaxed ordering (RO) attribute on the IOSF interface.
0	-	-	**Reserved**

PSF Port 0 Configuration (PSF_4_PSF_PORT_CONFIG_PG1_PORT0) – Offset 4024

Applied to Port 0. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 1 Configuration (PSF_4_PSF_PORT_CONFIG_PG1_PORT1) – Offset 4028

Applied to Port 1. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 2 Configuration (PSF_4_PSF_PORT_CONFIG_PG1_PORT2) – Offset 402c

Applied to Port 2. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 3 Configuration (PSF_4_PSF_PORT_CONFIG_PG1_PORT3) – Offset 4030

Applied to Port 3. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 4 Configuration (PSF_4_PSF_PORT_CONFIG_PG1_PORT4) – Offset 4034

Applied to Port 4. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF5 Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4020h	4	PSF Port 0 Configuration (PSF_5_PSF_PORT_CONFIG_PG0_PORT0)	0h
4024h	4	PSF Port 1 Configuration (PSF_5_PSF_PORT_CONFIG_PG0_PORT1)	0h
4028h	4	PSF Port 2 Configuration (PSF_5_PSF_PORT_CONFIG_PG0_PORT2)	0h
402ch	4	PSF Port 3 Configuration (PSF_5_PSF_PORT_CONFIG_PG0_PORT3)	0h
4030h	4	PSF Port 4 Configuration (PSF_5_PSF_PORT_CONFIG_PG0_PORT4)	0h
4034h	4	PSF Port 5 Configuration (PSF_5_PSF_PORT_CONFIG_PG0_PORT5)	0h
4038h	4	PSF Port 6 Configuration (PSF_5_PSF_PORT_CONFIG_PG0_PORT6)	0h
403ch	4	PSF Port Configuration (PSF_5_PSF_PORT_CONFIG_PG1_PORT0)	0h

PSF Port 0 Configuration (PSF_5_PSF_PORT_CONFIG_PG0_PORT0) – Offset 4020

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
2	0x0	RW	**Egress Force Relax Ordering (EgressFRO)** If set, IOSF relaxed ordering will be forced for outgoing transactions, regardless of the relaxed ordering (RO) attribute on the IOSF interface. Egress Force Relax Ordering is only applicable for PSF port types with buffering.
1	0x0	RW	**Ingress Force Relax Ordering (IngressFRO)** If set, IOSF relaxed ordering will be forced for incoming transactions, regardless of the relaxed ordering (RO) attribute on the IOSF interface.
0	-	-	**Reserved**

PSF Port 1 Configuration (PSF_5_PSF_PORT_CONFIG_PG0_PORT1) – Offset 4024

Applied to Port 1. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 2 Configuration (PSF_5_PSF_PORT_CONFIG_PG0_PORT2) – Offset 4028

Applied to Port 2. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 3 Configuration (PSF_5_PSF_PORT_CONFIG_PG0_PORT3) – Offset 402c

Applied to Port 3. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 4 Configuration (PSF_5_PSF_PORT_CONFIG_PG0_PORT4) – Offset 4030

Applied to Port 4. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 5 Configuration (PSF_5_PSF_PORT_CONFIG_PG0_PORT5) – Offset 4034

Applied to Port 5. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port 6 Configuration (PSF_5_PSF_PORT_CONFIG_PG0_PORT6) – Offset 4038

Applied to Port 6. Same definition as PSF Port 0 Configuration register at offset 4020h.

PSF Port Configuration (PSF_5_PSF_PORT_CONFIG_PG1_PORT0) – Offset 403c

Applied to Port 0. Same definition as PSF Port 0 Configuration register at offset 4020h.

RTC Indexed Registers

The RTC contains two sets of indexed registers that are accessed using the two separate Index and Target registers (70h/71h or 72h/73h), as shown in the following table:

RTC (Standard) RAM Bank

Index Name

00h Seconds

01h Seconds Alarm

02h Minutes

03h Minutes Alarm

04h Hours

05h Hours Alarm

06h Day of Week

07h Day of Month

08h Month

09h Year

0Ah Register A

0Bh Register B

0Ch Register D

0Dh Register D

0Bh-7Fh 114 Bytes of User RAM

Summary of Bus:, Device:, Function: (IO)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	1	Seconds (Sec)	0h
1h	1	Seconds Alarm (Sec_Alarm)	0h
2h	1	Minutes (Minutes)	0h
3h	1	Minutes Alarm (Minutes_Alarm)	0h
4h	1	Hours (Hours)	0h
5h	1	Hours Alarm (Hours_Alarm)	0h
6h	1	Day of Week (Day_of_Week)	0h
7h	1	Day of Month (Day_of_Month)	0h
8h	1	Month (Month)	0h
9h	1	Year (Year)	0h
ah	1	Register A (RTC_REGA)	0h
bh	1	Register B - General Configuration (Register_B)	80h
ch	1	Register C - Flag Register (Register_C)	0h
dh	1	Register D - Flag Register (Register_D)	80h

Seconds (Sec) – Offset 0

RTC Index: 00h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current time second

Seconds Alarm (Sec_Alarm) – Offset 1

RTC Index: 01h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores Seconds Alarm

Minutes (Minutes) – Offset 2

RTC Index: 02h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current time Minutes

Minutes Alarm (Minutes_Alarm) – Offset 3

RTC Index: 03h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores Alarm Minutes

Hours (Hours) – Offset 4

RTC Index: 04h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current time Hours

Hours Alarm (Hours_Alarm) – Offset 5

RTC Index: 05h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores Alarm Hours

Day of Week (Day_of_Week) – Offset 6

RTC Index: 06h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current Day of Week

Day of Month (Day_of_Month) – Offset 7

RTC Index: 07h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current Day of Month

Month (Month) – Offset 8

RTC Index: 08h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current Month

Year (Year) – Offset 9

RTC Index: 09h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current Year

Register A (RTC_REGA) – Offset a

This register is used for general configuration of the RTC functions. None of the bits are affected by RSMRST# or any other reset signal.

Bit Range	Default	Access	Field Name and Description
7	0b	RW	**UPDATE IN PROGRESS (UIP)** This bit may be monitored as a status flag. 0 = Update cycle will not start for at least 488 micro-seconds. The time, calendar, and alarm information in RAM is always available when the UIP bit is 0. 1 = The update is soon to occur or is in progress.
6:0	-	-	**Reserved**

Register B – General Configuration (Register_B) – Offset b

Bit Range	Default	Access	Field Name and Description
7	1b	RW	**Update Cycle Inhibit (SET)** Enables/Inhibits the update cycles. 0 = Update cycle occurs normally once each second. 1 = A current update cycle will abort and subsequent update cycles will not occur until SET is returned to zero. When set is one, the BIOS may initialize time and calendar bytes safely. This bit is not affected by RSMRST# nor any other reset signal. Note: Software must ensure this bit is at least transitioned from '1' to '0' once whenever the RTC coin battery is inserted. This is to ensure that the internal RTC time updates occur properly.
6	0b	RW	**Periodic Interrupt Enable (PIE)** 0 = Disabled. 1 = Enabled. Allows an interrupt to occur with a time base set with the RS bits of register A. This bit is cleared by RSMRST# assertion, but not on any other reset.
5	0b	RW	**Alarm Interrupt Enable (AIE)** 0 = Disabled. 1 = Enabled. Allows an interrupt to occur when the AF is set from an alarm match from the update cycle. An alarm can occur once a second, one an hour, once a day, or once a month. This bit is cleared by RTCRST# assertion, but not on any other reset.
4	0b	RW	**Update-ended Interrupt Enable: (UIE)** 0 = Disabled. 1 = Enabled. Allows an interrupt to occur when the update cycle ends. This bit is cleared by RSMRST# assertion, but not on any other reset.
3	0b	RW	**Square Wave Enable (SQWE)** The Square Wave Enable bit serves no function in this device, yet is left in this register bank to provide compatibility with the Motorola 146818B. There is not SQW pin on this device. This bit is cleared by RSMRST# assertion, but not on any other reset.

Bit Range	Default	Access	Field Name and Description
2	0b	RW	**Data Mode (DM)** This bit specifies either binary or BCD data representation. 0 = BCD. 1 = Binary. This bit is not affected by RSMRST# nor any other reset signal.
1	0b	RW	**Hour Format (HOURFORM)** This bit indicates the hour byte format. 0 = Twelve-hour mode is selected.In twelve hour mode, the seventh bit represents AM as zero and PM as one. 1 = Twenty-four hour mode is selected. This bit is not affected by RSMRST# nor any other reset signal.
0	0b	RW	**Daylight Savings Enable (DSE)** The Daylight Savings Enable bit triggers two special hour updates per year when set to one. One is on the first Sunday in April, where time increments from 1:59:59 AM to 3:00:00 AM. The other is the last Sunday in October when the time first reaches 1:59:59 AM, it is changed to 1:00:00 AM. The time mustincrement normally for at least two update cycles (seconds) previous to these conditions for the time change to occur properly. These special update conditions do not occur when the DSE bit is set to zero. The days for the hour adjustment are those specified in United States federal law as of 1987, which is different than previous years. If BUC.SDO bit is set, the DSE bit continues to be a R/W bit, but Daylight Saving is disabled regardless of the DSE bit. This bit is not affected by RSMRST# nor any other reset signal.

Register C - Flag Register (Register_C) – Offset c

Bit Range	Default	Access	Field Name and Description
7	0b	RO	**Interrupt Request Flag (IRQF)** Interrupt Request Flag = (PF * PIE) + (AF * AIE) + (UF * UFE). This also causes the RTC Interrupt to be asserted. This bit is cleared upon RSMRST# assertion or a read of Register C.

Bit Range	Default	Access	Field Name and Description
6	0b	RO	**Periodic Interrupt Flag (PF)** Periodic interrupt Flag will be one when the tap as specified by the RS bits of register A is one. If no taps are specified, this flag bit will remain at zero. This bit is cleared upon RSMRST# assertion or a read of Register C.
5	0b	RO	**Alarm Flag (AF)** Alarm Flag will be high after all Alarm values match the current time. This bit is cleared upon RTCRST# assertion or a read of Register C.
4	0b	RO	**Update-ended Flag (UF)** Updated-ended flag will be high immediately following an update cycle for each second. The bit is cleared upon RSMRST# assertion or a read of Register C.
3:0	-	-	**Reserved**

Register D - Flag Register (Register_D) – Offset d

Bit Range	Default	Access	Field Name and Description
7	1b	RW	**Valid RAM and Time Bit (VRT)** This bit is hard-wired to 1 in the RTC power well. This bit should always be written as a 0 for write cycle, however it will return a 1 for read cycles.
6	-	-	**Reserved**
5:0	000000b	RW	**Date Alarm (Date_Alarm)** These bits store the date of month alarm value. If set to 000000, then a dont care state is assumed. The host must configure the dates alarm for these bits to do anything, yet they can be written at any time. If the date alarm is not enabled, these bits will return zeros to mimic the functionality of the Motorola 146818B. These bits are not affected by any reset assertion.

RTC PCR Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
3400h	4	RTC Configuration (RC)	0h
3414h	1	Backed Up Control (BUC)	0h
3f04h	4	RTC Update In Progress SMI Control (UIPSMI)	0h

RTC Configuration (RC) – Offset 3400

All bits in this register are in the Primary Well and cleared by PLTRST# assertion.

Bit Range	Default	Access	Field Name and Description
31	0b	RW/1L	**Bios Interface Lock-Down (BILD)** When set, prevents RTC version of TS (BUC.TS) from being changed. This bit can only be written from 0 to 1 once. This BILD bit has a different function compared to LPC, SPI and eSPI version but BIOS should set all the corresponding bits after reset in order to lock down the BIOS interface correctly.
30:7	-	-	**Reserved**
6	0b	RW	**RTC High Power Mode HW Disable (HPM_HW_DIS)** 0 = HW control of the RTC internal VRM is disabled. 1 = The internal VRM that generates the rtc well supply voltage in SUS mode is disabled when SLP_S0# is asserted.
5	0b	RW	**RTC High Power Mode SW Disable (HPM_SW_DIS)** 0 = The internal VRM powers the rtc well when RSMRST# is '1'. (default) 1 = The internal VRM that generates the rtc well supply voltage in SUS mode is disabled.
4	0b	RW/1L	**Upper 128 Byte Lock (UL)** When set, bytes 38h-3Fh in the upper 128 byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any guaranteed data. Bit reset on system reset.

Bit Range	Default	Access	Field Name and Description
3	0b	RW/1L	**Lower 128 Byte Lock (LL)** When set, bytes 38h-3Fh in the lower 128 byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any guaranteed data. Bit reset on system reset.
2	0b	RW	**Upper 128 Byte Enable (UE)** When set, the upper 128 byte bank of RTC RAM can be accessed.
1:0	-	-	**Reserved**

Backed Up Control (BUC) – Offset 3414

All bits in this register are in the RTC well and only cleared by RTCRST# assertion.

Bit Range	Default	Access	Field Name and Description
6:5	-	-	**Reserved**
4	0b	RW	**Daylight Savings Override (SDO)** When this bit is a '1', the DSE bit in the RTC Register B bit(0) is a RW bit but has no effect where daylight savings is hard-disabled internally. When this bit is a '0', the DSE bit in the RTC register B bit(0) is a RW bit that is configurable by software to enable the daylight savings. System BIOS shall configure this bit accordingly during the boot process before RTC time is initialized.
3:1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**Top Swap (TS)** 0 = PCH will not invert A16, A17 or A18. 1 = PCH will invert A16, A17 or A18 for cycles going to the BIOS space. If booting from SPI LPC (FWH), then the boot-block size is 64 KB and A16 is inverted if Top Swap is enabled. If booting from SPI, then the Top Swap Block size soft strap determines if A16, A17 or A18 shoudl be inverted if Top Swap is enabled. If PCH is strapped for Top Swap (GPP_B14/SPKR is high at rising edge of PCH_ PWROK), then this bit cannot be cleared by software. The strap jumper should be removed and the system rebooted.

RTC Update In Progress SMI Control (UIPSMI) – Offset 3f04

This register exists in the RTC well.

Bit Range	Default	Access	Field Name and Description
30:18	-	-	**Reserved**
17	0b	RW/1C	**RTC UIP Low-to-High (UIP_L2H)** This sticky status bit is set whenever the RTC Update-In-Progress signal transitions from low to high (i.e., at the start of an update).
16	0b	RW/1C	**RTC UIP High-to-Low (UIP_H2L)** This sticky status bit is set whenever the RTC Update-In-Progress signal transitions from high to low (i.e., at the start of an update).

Bit Range	Default	Access	Field Name and Description
15:2	-	-	**Reserved**
1	0b	RW	**RTC UIP Low-to-High SMI Enable (UIP_L2H_SMI_en)** When this bit is set, a '1' in bit 17 will assert the internal SMI signal to the Power Management SMI logic.
0	0b	RW	**RTC UIP High-to-Low SMI Enable (UIP_H2L_SMI_en)** When this bit is set, a '1' in bit 16 will assert the internal SMI signal to the Power Management SMI logic.

SATA ABAR Registers

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	HBA Capabilities (GHC_CAP)	FF36FF07h
4h	4	Global HBA Control (GHC)	80000000h
8h	4	Interrupt Status Register (IS)	0h
ch	4	Ports Implemented (GHC_PI)	0h
10h	4	AHCI Version (VS)	10301h
1ch	4	Enclosure Management Location (EM_LOC)	1600002h
20h	4	Enclosure Management Control (EM_CTL)	7010000h
24h	4	HBA Capabilities Extended (GHC_CAP2)	3Ch
a0h	4	Vendor Specific (VSP)	48h
a4h	4	Vendor-Specific Capabilities Register (VS_CAP)	1002DEh
c0h	4	RAID Platform ID (RPID)	311C02h
c4h	2	Premium Feature Block (PFB)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
c8h	2	SW Feature Mask (SFM)	3Fh
100h	4	Port 0 Command List Base Address (PxCLB0)	0h
104h	4	Port 0 Command List Base Address Upper 32-bits (PxCLBU0)	0h
108h	4	Port 0 FIS Base Address (PxFB0)	0h
10ch	4	Port 0 FIS Base Address Upper 32-bits (PxFBU0)	0h
110h	4	Port 0 Interrupt Status (PxIS0)	0h
114h	4	Port 0 Interrupt Enable (PxIE0)	0h
118h	4	Port 0 Command (PxCMD0)	4h
120h	4	Port 0 Task File Data (PxTFD0)	9h
124h	4	Port 0 Signature (PxSIG0)	FFFFFFFFh
128h	4	Port 0 Serial ATA Status (PxSSTS0)	0h
12ch	4	Port 0 Serial ATA Status (PxSCTL0)	0h
130h	4	Port 0 Serial ATA Error (PxSERR0)	0h
134h	4	Port [0] Serial ATA Active (PxSACT0)	0h
138h	4	Port 0 Commands Issued (PxCI0)	0h
144h	4	Port 0 Device Sleep (PxDEVSLP0)	1E022852h
180h	4	Port 1 Command List Base Address (PxCLB1)	0h
184h	4	Port 1 Command List Base Address Upper 32-bits (PxCLBU1)	0h
188h	4	Port 1 FIS Base Address (PxFB1)	0h
18ch	4	Port 0 FIS Base Address Upper 32-bits (PxFBU1)	0h
190h	4	Port 1 Interrupt Status (PxIS1)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
194h	4	Port 0 Interrupt Enable (PxIE1)	0h
198h	4	Port 1 Command (PxCMD1)	0h
1a0h	4	Port 1 Task File Data (PxTFD1)	0h
1a4h	4	Port 1 Signature (PxSIG1)	0h
1a8h	4	Port 0 Serial ATA Status (PxSSTS1)	0h
1ach	4	Port 1 Serial ATA Control (PxSCTL1)	0h
1b0h	4	Port 1 Serial ATA Error (PxSERR1)	0h
1b4h	4	Port 1 Serial ATA Active (PxSACT1)	0h
1b8h	4	Port 1 Commands Issued. (PxCI1)	0h
1c4h	4	Port 1 Device Sleep (PxDEVSLP1)	0h
200h	4	Port 2 Command List Base Address (PxCLB2)	0h
204h	4	Port 2 Command List Base Address Upper 32-bits (PxCLBU2)	0h
208h	4	Port 2 FIS Base Address (PxFB2)	0h
20ch	4	Port 2 FIS Base Address Upper 32-bits (PxFBU2)	0h
210h	4	Port 2 Interrupt Status (PxIS2)	0h
214h	4	Port 2 Interrupt Enable (PxIE2)	0h
218h	4	Port 2 Command (PxCMD2)	0h
220h	4	Port 2 Task File Data (PxTFD2)	0h
224h	4	Port 2 Signature (PxSIG2)	0h
228h	4	Port 2 Serial ATA Status (PxSSTS2)	0h
22ch	4	Port 2 Serial ATA Control (PxSCTL2)	0h
230h	4	Port 2 Serial ATA Error (PxSERR2)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
234h	4	Port 2 Serial ATA Active (PxSACT2)	0h
238h	4	Port 2 Commands Issued (PxCI2)	0h
244h	4	Port 2 Device Sleep (PxDEVSLP2)	0h

HBA Capabilities (GHC_CAP) – Offset 0

This register indicates basic capabilities of the HBA to driver software. The RWO bits in this register are only cleared upon PLTRST#. This register is not reset by FLR.

Bit Range	Default	Access	Field Name and Description
31	1h	RW/O	**Supports 64-bit Addressing (S64A)** Indicates that the SATA controller can access 64-bit data structures. The 32-bit upper bits of the port DMA Descriptor, the PRD Base, and each PRD entry are read/write.
30	1h	RW/O	**Supports Native Command Queuing Acceleration (SCQA)** When set to 1, indicates that the SATA controller supports SATA command queuing using the DMA Setup FIS. The PCH handles DMA Setup FISes natively, and can handle auto-activate optimization through that FIS.
29	1h	RW/O	**Supports SNotification Register (SSNTF)** When set to 1, indicates the SATA controller supports the PxSNTF (SNotification) register and its associated functionality. When cleared to 0, the SATA controller does not support the PxSNTF (SNotification) register and its associated functionality.
28	1h	RW/O	**Supports Mechanical Presence Switch (SMPS)** When set to 1, indicates whether the SATA controller supports mechanical presence switches on its ports for use in hot-plug operations. This value is loaded by platform BIOS prior to operating system initialization. If this bit is set, BIOS must also map the SATAGP pins to the SATA controller through GPIO space.

Bit Range	Default	Access	Field Name and Description
27	1h	RW/O	**Supports Staggered Spin-up (SSS)** Indicates whether the SATA controller supports staggered spin-up on its ports, for use in balancing power spikes. This value is loaded by platform BIOS prior to OS initialization. 0 = Staggered spin-up not supported. 1 = Staggered spin-up supported.
26	1h	RW/O	**Supports Aggressive Link Power Management (SALP)** 0 = Software shall treat the PxCMD.ALPEand PxCMD.ASP bits as reserved. 1 = The SATA controller supports auto-generating link requests to the partial or slumber states when there are no commands to process.
25	1h	RW/O	**Supports Activity LED (SAL)** Indicates the SATA controller supports a single output pin (SATALED#) which indicates activity.
24	1h	RW/O	**Supports Command List Override (SCLO)** When set to 1, indicates that the HBA supports the PxCMD.CLO bit and it's associated function. When cleared to 0, The HBA is not capable of clearing the BSY and DRQ bits in the Status register in order to issue a software reset if these bits are still set from a previous operation.

Bit Range	Default	Access	Field Name and Description
23:20	3h	RW/O	**Interface Speed Support (ISS)** Indicates the maximum speed the SATA controller can support on its ports. 1h = 1.5Gb/s 2h = 3Gb/s 3h = 6Gb/s The default of this field is dependent upon the PCH SKU. If at least one PCH SATA port supports 6Gb/s, the default will be 3h. If no PCH SATA ports support 6Gb/s, then the default will be 2h and writes of 3h will be ignored by the PCH. Refer to EDS Vol1 Section 1 for details on 6Gb/s port availability.
19	-	-	**Reserved**
18	1h	RO	**Supports AHCI mode only (SAM)** The SATA controller may optionally support AHCI access mechanism only. 0 = SATA controller supports both IDE and AHCI Modes 1 = SATA controller supports AHCI Mode Only Note: BIOS should program this field as “1” since IDE mode is not supported.
17	1h	RW/O	**Supports Port Multiplier (SPM)** The SATA controller may optionally support command-based switching Port Multipliers. BIOS must clear this bit if Port Multipliers are not supported.

Bit Range	Default	Access	Field Name and Description
16	-	-	**Reserved**
15	1h	RO	**PIO Multiple DRQ Block (PMD)** Hardwired to 1. The SATA controller supports PIO Multiple DRQ Command Block.
14	1h	RW/O	**Slumber State Capable (SSC)** When set to 1, the SATA controller supports the slumber state.
13	1h	RW/O	**Partial State Capable (PSC)** When set to 1, the SATA controller supports the partial state.
12:8	1Fh	RO	**Number of Command Slots (NCS)** Hardwired to 1Fh to indicate support for 32 slots.
7	0h	RO	**Command Completion Coalescing Supported (CCCS)** 0 = Command Completion Coalescing Not Supported 1 = Command Completion Coalescing Supported
6	0h	RW/O/V	**Enclosure Management Supported (EMS)** 0 = Enclosure Management Not Supported 1 = Enclosure Management Supported
5	0h	RW/O	**Supports External SATA (SXS)** 0 = External SATA is not supported on any ports 1 = External SATA is supported on one or more ports When set, software can examine each SATA port's Command register (PxCMD.ESP) to determine which port is routed externally.
4:0	07h	RO/V	**Number of Ports (NP)** Indicates number of supported ports. The number of ports indicated in this field may be more than the number of ports indicated in the PI (ABAR + 0Ch) register. Field value dependent on number of ports available in a given SKU.

Global HBA Control (GHC) – Offset 4

This register controls various global actions of the HBA.

Bit Range	Default	Access	Field Name and Description
31	1h	RO	**AHCI Enable (AE)** When set, indicates that an AHCI driver is loaded and communication to the HBA shall be via AHCI mechanisms. This can be used by an HBA that supports both legacy mechanisms (such as SFF-8038i) and AHCI to know when the HBA is running under an AHCI driver. 0 = Software will only communicate with the HBA using legacy mechanisms. 1 = Software shall only talk to the HBA using AHCI. The HBA will not have to allow command processing via both AHCI and legacy mechanisms. Note: Software shall set this bit to 1 before accessing other AHCI registers. Note: The implementation of this bit is dependent upon the value of the CAP.SAM bit. If CAP.SAM is '0', then GHC.AE should be RW and shall have a reset value of '0'. If CAP.SAM is '1', then GHC.AE shall be read only and shall have a reset value of '1'.
30:3	-	-	**Reserved**
2	0h	RO	

Bit Range	Default	Access	Field Name and Description
			MSI Revert to Single Message (MRSM) When set to 1 by hardware, indicates that the HBA requested more than one MSI vector but has reverted to using the first vector only. When this bit is cleared to 0, the HBA has not reverted to single MSI mode (i.e. hardware is already in single MSI mode, software has allocated the number of messages requested, or hardware is sharing interrupt vectors if MC.MME < MC.MMC). The HBA may revert to single MSI mode when the number of vectors allocated by the host is less than the number requested. This bit shall only be set to 1 when the following conditions hold: MC.MSIE = 1 (MSI is enabled) MC.MMC > 0 (multiple messages requested) MC.MME > 0 (more than one message allocated) MC.MME != MC.MMC (messages allocated not equal to number requested) When this bit is set to 1, single MSI mode operation is in use and software is responsible for clearing bits in the IS register to clear interrupts. This bit shall be cleared to 0 by hardware when any of the four conditions stated is false. This bit is also cleared to 0 when MC.MSIE = 1 and MC.MME = 0h. In this case, the hardware has been programmed to use single MSI mode, and is not reverting to that mode. For PCH, the HBA shall always revert to single MSI mode when the number of vectors allocated by the host is leass than the number requested. Value of MRSM is a don't care when GHC.HR=1.
1	0h	RW	**Interrupt Enable (IE)** This global bit enables interrupts from the PCH. 0 = All interrupt sources from all ports are disabled. 1 = Interrupts are allowed from the AHCI controller.

Bit Range	Default	Access	Field Name and Description
0	0h	RW/1S/V	**HBA Reset (HR)** Resets the PCH AHCI controller. 0 = No effect. 1 = When set by software, this bit causes an internal reset of the PCH AHCI controller. All state machines that relate to data transfers and native command queuing will return to an idle condition, and all ports are re-initialized using COMRESET. Note: For further details, refer to Section 10.4.3 of the Serial ATA Advanced Host Controller Interface specification, revision 1.3.

Interrupt Status Register (IS) – Offset 8

This register indicates which of the ports within the controller have an interrupt pending and require service.

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**
2	0h	RW/1C/V	**Interrupt Pending Status Port 2 (IPS2)** This bit is only applicable to system that has Port 2 physically. 0 = No interrupt pending. 1 = Port 2 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt
1	0h	RW/1C/V	**Interrupt Pending Status Port 1 (IPS1)** This bit is only applicable to system that has Port 1 physically. 0 = No interrupt pending. 1 = Port 1 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.

Bit Range	Default	Access	Field Name and Description
0	0h	RW/1C/V	**Interrupt Pending Status Port 0 (IPS0)** This bit is only applicable to system that has Port 0 physically. 0 = No interrupt pending. 1 = Port 0 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.

Ports Implemented (GHC_PI) – Offset c

This register indicates which ports are exposed to the HBA. It is loaded by platform BIOS. It indicates which ports that the device supports are available for software to use. Any available port may not be implemented.

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**
2	0h	RW/O/V	**Port 2 Implemented (PI2)** 0 = The port is not implemented. 1 = The port is implemented. Note: This bit may be Reserved and is RO '0' depending on if port is available in the given SKU. Refer to EDS Vol1 Section 1 for details if port is available.
1	0h	RW/O/V	**Port 1 Implemented (PI1)** 0 = The port is not implemented. 1 = The port is implemented.
0	0h	RW/O/V	**Port 0 Implemented (PI0)** 0 = The port is not implemented. 1 = The port is implemented.

AHCI Version (VS) – Offset 10

This register indicates the major and minor version of the AHCI specification. It is BCD encoded. The upper two bytes represent the major version number, and the lower two bytes represent the minor version number. Example: Version 3.12 would be represented as 00030102h.

Bit Range	Default	Access	Field Name and Description
31:16	0001h	RO	**Major Version Number (MJR)** Indicates the major version is 1.
15:0	0301h	RO	**Minor Version Number (MNR)** Indicates the minor version is 31.

Enclosure Management Location (EM_LOC) – Offset 1c

The enclosure management location register identifies the location and size of the enclosure management message buffer. This register is not implemented if enclosure management is not supported (i.e. CAP.EMS = 0).

Bit Range	Default	Access	Field Name and Description
31:16	0160h	RO	**Offset (OFST)** The offset of the message buffer in Dwords from the beginning of the ABAR.
15:0	0002h	RO	**Buffer Size (SZ)** Specifies the size of the transmit message buffer area in Dwords. If both transmit and receive buffers are supported, then the transmit buffer begins at ABAR[EM_LOC.OFST*4] and the receive buffer directly follows it. If both transmit and receive buffers are supported, both buffers are of the size indicated in the Buffer Size field. A value of 0 is invalid. The SATA controller only supports transmit buffer.

Enclosure Management Control (EM_CTL) – Offset 20

This register is used to control and obtain status for the enclosure management interface. The register includles information on the attributes of the implementation, enclosure management messages supported, the status of the interface, whether any messages are pending, and is used to initiate sending messages. This register is not implemented if enclosure management is not supported (i.e. CAP.EMS = 0).

Bit Range	Default	Access	Field Name and Description
30:28	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
27	0h	RO	**Port Multiplier Support (ATTR_PM)** The HBA does not support enclosure management messages for devices attached via a Port Multiplier. Software should use the Serial ATA enclosure management bridge that is built into many Port Multipliers for enclosure services with these devices. For more information on Serial ATA enclosure management bridges, refer to the Serial ATA II: Extensions to Serial ATA 1.0a revision 1.2 specification.
26	1h	RW/O	**Activity LED Hardware Driven (ATTR_ALHD)** If set to 1, the HBA drives the activity LED for the LED message type in hardware and does not utilize software settings for this LED. The HBA does not begin transmitting the hardware based activity signal until after software has written CTL.TM=1 after a reset condition.
25	1h	RO	**Transmit Only (ATTR_XMT)** If set to 1, the HBA only supports transmitting messages and does not support receiving messages. If cleared to 0, the HBA supports transmitting and receiving messages.
24	1h	RO	**Single Message Buffer (ATTR_SMB)** If set to 1, the HBA has one message buffer that is shared for messages to transmit and messages received. In this case, unsolicited receive messages are not supported and it is software's responsibility to manage access to this buffer. If cleared to 0, there are separate receive and transmit buffers such that unsolicited messages could be supported.
23:20	-	-	**Reserved**
19	0h	RO	**SGPIO Enclosure Management Messages (SUPP_SGPIO)** If set to 1, the HBA supports the SGPIO register interface message type.
18	0h	RO	**SES-2 Enclosure Management Messages (SUPP_SES2)** If set to 1, the HBA supports the SES-2 message type.
17	0h	RO	**SAF-TE Enclosure Management Messages (SUPP_SAFTE)** If set to 1, the HBA supports the SAF-TE message type.
16	1h	RO	**LED Message Types (SUPP_LED)** If set to 1, the HBA supports the LED message type defined in LED Message Type.
15:10	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
9	0h	RW/1S/V	**Reset (RST)** When set to 1 by software, the HBA shall reset all enclosure management message logic and take all appropriate reset actions to ensure messages can be transmitted/received after the reset. After the HBA completes the reset operation, the HBA shall set the value to 0. A write of 0 by software to this field shall have no effect.
8	0h	RW/1S/V	**Transmit Message (CTL_TM)** When set to 1 by software, the HBA shall transmit the message contained in the message buffer. When the message is completely sent, the HBA shall clear this bit to 0. A write of 0 to this bit by software shall have no effect. Software shall not change the contents of the message buffer while CTL.TM is set to 1.
7:1	-	-	**Reserved**
0	0h	RO	**Message Received (STS_MR)** Message received is not supported.

HBA Capabilities Extended (GHC_CAP2) – Offset 24

This register indicates basic capabilities of the HBA to driver software. The RWO bits in this register are only cleared upon PLTRST#.

Bit Range	Default	Access	Field Name and Description
30:6	-	-	**Reserved**
5	1h	RW/O	**DEVSLP Entrance from Slumber Only (DESO)** This bit specifies that the HBA shall only assert DEVSLP if the interface is in Slumber. 0 = The host may enter DEVSLP from any link state (active, Partial, or Slumber). 1 = The host shall ignore software directed entrance to DEVSLP by means of PxCMD.ICC bit unless PxSSTS.IPM = 6h.

Bit Range	Default	Access	Field Name and Description
4	1h	RW/O/V	**Supports Aggressive DEVSLP Management (SADM)** 0 = Aggressive DEVSLP Management is not supported and software shall treat the PxDEVSLP.ADSE field as reserved. 1 = The host supports hardware assertion of the DEVSLP signal after the idle timeout expires.
3	1h	RW/O/V	**Supports DEVSLP (SDS)** 0 = DEVSLP is not supported. 1 = Supports the DEVSLP feature.
2	1h	RW/O/V	**Automatic Partial to Slumber Transitions (APST)** 0 = Automatic Partial to Slumber Transition is not supported. 1 = Supports Automatic Partial to Slumber Transitions.
1	-	-	**Reserved**
0	0h	RO	**BIOS/OS Handoff (BOH)** Not supported.

Vendor Specific (VSP) – Offset a0

Vendor Specific

Bit Range	Default	Access	Field Name and Description
30:7	-	-	**Reserved**
6	1h	RO	**Software Feature Mask Supported (SFMS)** Set to 1 if the platform is enabled for premium storage features mask (SFM) as described in VS MMIO space at offset ABAR[RPID.(OFST*4)+4].

Bit Range	Default	Access	Field Name and Description
5	0h	RO/V	**Premium Features Supported (PFS)** Set to 1 if the platform is enabled for premium storage features (PFB) as described in VS MMIO space at offset ABAR[RPID.OFST*4]. Set to 0 if the platform is not enabled for premium storage features.
4	0h	RO/V	**Platform Type (PT)** Set to 1 if mobile platform. Clear (0) if desktop.
3	1h	RO	**Supports RAID Platform ID Reporting (SRPIR)** If set to 1, then indicates that the RAID Platform ID is reported via ABAR + C0h. Set to 0 if this ID is not reported via MMIO space.
2:0	-	-	**Reserved**

Vendor-Specific Capabilities Register (VS_CAP) – Offset a4

Vendor-Specific Capabilities Register

Bit Range	Default	Access	Field Name and Description
30:28	-	-	**Reserved**
27:16	010h	RW/O	**NVM Remapped Register Offset (NRMO)** Specifies the offset (in 128B unit) within ABAR as to where the NVM Remap memory BAR register space is remapped. For example, NRMO=1 means ABAR + 128B. This allows the remapped offset to shift between ABAR + 0B, and ABAR + 512KK - 128B, with 128B step. The remapped offset into the AHCI memory space must not overlap with the memory space used for SATA. The remapped offset into the AHCI memory space and the remapped size must not exceed the allocated AHCI memory space of the integrated AHCI controller. Only valid when NRMBE = '1'. The reset default of this field is 10h, this places the start of the PCIe NAND memory BAR register space at ABAR + 2K. This field is not reset by FLR.
15:13	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
12:1	16Fh	RW/O	**Memory Space Limit. (MSL)** This field specifies the size (in 128B unit) of the remapped memory space for the PCIe NAND device. It is a 0-based field. For example, MSL=1 means 256B. This allows the remapped size to shift between 128B and 512K with the step of 128B.Memory BAR offset from 0 to MSL of the PCIe NAND device are remapped under the integrated AHCI controller memory space.The remapped offset into the AHCI memory space and the value programmed in this field must not exceed the allocated AHCI memory space of the integrated AHCI controller. Only valid when NRMBE = 1. The reset default of this field is 16Fh which specifies the size of the remapped memory space as 34k.This field is not reset by FLR.
0	0h	RW/O	**NVM Remap Memory BAR Enable (NRMBE)** Set to 1 if NVM Remap device is present and remapping of its memory BAR register space is enabled. Cleared to 0 if there is no PCIe NAND device present or the remapping of its memory BAR register space is disabled. This bit is not reset by FLR.

RAID Platform ID (RPID) – Offset c0

Bit Range	Default	Access	Field Name and Description
31:16	0031h	RO	**Offset (OFST)** The offset of the Premium Feature Block (PFB) in DWords from the beginning of the ABAR. SFM follows directly after PFB.
15:0	1C02h	RO/V	**RAID Platform ID (RPID)** Specifies the DID value that has been assigned to the platform. This is the same DID that is reported by the SATA controller when SATAGC.AIE is set to 1 except that the DID is always reported through this register, regardless if the programming of SATAGC.AIE.

Premium Feature Block (PFB) – Offset c4

Bit Range	Default	Access	Field Name and Description
14:2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1	0h	RO	**Supports Email Alert (SEA)** Read value is the same as VSP.PFS. If set to 1, then this feature is supported as part of the premium feature set.
0	0h	RO/V	**Supports OEM IOCTL (SOI)** Read value is the same as VSP.PFS. If set to 1, then this feature is supported as part of the premium feature set.

SW Feature Mask (SFM) – Offset c8

The following will be programmed by the BIOS when VS_CAP.SFMS == 1. The feature mask is used by SW to determine which non-premium features shall be supported by SW. These register bits are not reset by FLR since they are programmed by BIOS.

Bit Range	Default	Access	Field Name and Description
14:12	-	-	**Reserved**
11:10	0h	RW/O	**OROM UI Normal Delay. (OROM_UI_Normal_Delay)** Values of these bits specify the delay of the OROM UI Splash Screen in a normal status. 00 = 2 secs (default and previous value); 01 = 4 secs; 10 = 6 secs; 11 = 8 secs. If bit 5 == 0, then these values are disregarded.
9	-	-	**Reserved**
8	0h	RW/O	**RRT Only on ESATA (IRRT_Only_on_ESATA)** If set to 1, then only RRT volumes can span internal and external SATA ports (e.g. eSATA). If cleared to 0, then any RAID volume can span internal and external SATA ports (e.g. eSATA).
7	0h	RW/O	**LED Locate (LED_Locate)** If set to 1, then LED/SGPIO hardware is attached and the ping to locate feature is enabled in the OS.
6	0h	RW/O	**HDDUNLOCK (HDDUNLOCK)** If set to 1, then HDD password unlock is enabled in the OS.

Bit Range	Default	Access	Field Name and Description
5	1h	RW/O	**OROM UI and BANNER (OROM_UI_and_BANNER)** If set to 1, then the OROM UI is displayed. When cleared to 0, the OROM UI and BANNER are not displayed if all disks and volumes have a normal status.
4	1h	RW/O	**RRT (IRRT)** If set to 1, then Rapid Recovery Technology is enabled.
3	1h	RW/O	**R5 (R5)** If set to 1, then RAID5 is enabled
2	1h	RW/O	**R10 (R10)** If set to 1, then RAID10 is enabled
1	1h	RW/O	**R1 (R1)** If set to 1, then RAID1 is enabled
0	1h	RW/O	**R0 (R0)** If set to 1, then RAID0 is enabled

Port 0 Command List Base Address (PxCLB0) – Offset 100

Bit Range	Default	Access	Field Name and Description
31:10	000000h	RW	**Command List Base Address (CLB)** Indicates the 32-bit base for the command list for this port. This base is used when fetching commands to execute. This address must be 1K aligned as indicated by bits 31:10 being read/write. Note that these bits are not reset on a HBA reset.
9:0	-	-	**Reserved**

Port 0 Command List Base Address Upper 32-bits (PxCLBU0) – Offset 104

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**Command List Base Address Upper (CLBU)** Indicates the upper 32-bits for the command list base address for this port. This base is used when fetching commands to execute. These bits are not reset on a HBA reset.

Port 0 FIS Base Address (PxFB0) – Offset 108

Bit Range	Default	Access	Field Name and Description
31:8	0000000 h	RW	**FIS Base Address (FB)** Indicates the 32-bit base for received FISes. This address must be 256-byte aligned as indicated by bits 31:08 being read/write. When FIS-based switching is in use, this structure is 4KB in length and the address shall be 4KB aligned. These bits are not reset on a HBA reset.
7:0	-	-	**Reserved**

Port 0 FIS Base Address Upper 32-bits (PxFBU0) – Offset 10c

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**FIS Base Address Upper (FBU)** Indicates the upper 32-bits for the received FIS base for this port. These bits are not reset on a HBA reset.

Port 0 Interrupt Status (PxIS0) – Offset 110

Bit Range	Default	Access	Field Name and Description
31	0h	RO	**Cold Presence Detect Status (CPDS)** The SATA controller does not support cold presence detect.

Bit Range	Default	Access	Field Name and Description
30	0h	RW/1C/V	**Task File Error Status (TFES)** This bit is set whenever the status register is updated by the device and the error bit (bit 0 of the Status field in the received FIS) is set.
29	0h	RW/1C/V	**Host Bus Fatal Error Status (HBFS)** Indicates that the HBA encountered a host bus error that it cannot recover from, such as a bad software pointer. In PCI, such an indication would be a target or master abort.
28	0h	RW/1C/V	**Host Bus Data Error Status (HBDS)** Indicates that the HBA encountered a data error (uncorrectable ECC / parity) when reading from or writing to system memory.
27	0h	RW/1C/V	**Interface Fatal Error Status (IFS)** Indicates that the HBA encountered an error on the SATA interface which caused the transfer to stop.
26	0h	RW/1C/V	**Interface Non-fatal Error Status (INFS)** Indicates that the HBA encountered an error on the SATA interface but was able to continue operation.
25	-	-	**Reserved**
24	0h	RW/1C/V	**Overflow Status (OFS)** Indicates that the HBA received more bytes from a device than was specified in the PRD table for the command.
23	0h	RW/1C/V	**Incorrect Port Multiplier Status (IPMS)** Indicates that the HBA received a FIS from a device whose port multiplier field did not match what was expected. The IPMS bit may be set during emuneration process. It is recommended that IPMS only be used after enumeration is complete on the Port Multiplier.Port Multiplier is not supported.
22	0h	RO/V	**PhyRdy Change Status (PRCS)** When set to one indicates the internal PhyRdy signal changed state. This bit reflects the state of PxSERR.DIAG.N. This bit is RO and is only cleared when PxSERR.DIAG.N is cleared. The internal PhyRdy signal also transitions when the port interface enters PARTIAL or SLUMBER power management states. PARTIAL and SLUMBER must be disabled when Surprise Removal Notification is desired, otherwise the power management state transitions will appear as false insertion and removal events.
21:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7	0h	RW/1C/V	**Device Mechanical Presence Status (DMPS)** When set, indicates that a platform mechanical presence switch has been opened or closed, which may lead to a change in the connection state of the device. This bit is only valid in systems that support mechanical presence switch (CAP.SMPS and PxCMD.MPSP are set). For systems that do not support mechanical presence switch, this bit will always be 0.
6	0h	RO/V	**Port Connect Change Status (PCS)** This bit reflects the state of PxSERR.DIAG.X. This bit is only cleared when PxSERR.DIAG.X is cleared. 1=Change in Current Connect Status. 0=No change in Current Connect Status.
5	0h	RW/1C/V	**Descriptor Processed (DPS)** A PRD with the I bit set has transferred all of its data.
4	0h	RO/V	**Unknown FIS Interrupt (UFS)** When set to 1 indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by software clearing the PxSERR.DIAG.F bit to 0. Note that this bit does not directly reflect the PxSERR.DIAG.F bit. PxSERR.DIAG.F is set immediately when an unknown FIS is detected, whereas this bit is set when the FIS is posted to memory. Software should wait to act on an unknown FIS until this bit is set to 1 or the two bits may become out of sync.
3	0h	RW/1C/V	**Set Device Bits Interrupt (SDBS)** A Set Device Bits FIS has been received with the I bit set and has been copied into system memory.
2	0h	RW/1C/V	**DMA Setup FIS Interrupt (DSS)** A DMA Setup FIS has been received with the I bit set and has been copied into system memory.
1	0h	RW/1C/V	**PIO Setup FIS Interrupt (PSS)** A PIO Setup FIS has been received with the I bit set, it has been copied into system memory, and the data related to that FIS has been transferred. This bit shall be set even if the data transfer resulted in an error.

Bit Range	Default	Access	Field Name and Description
0	0h	RW/1C/V	**Device to Host Register FIS Interrupt (DHRS)** A D2H register FIS has been received with the I bit set, and has been copied into system memory.

Port 0 Interrupt Enable (PxIE0) – Offset 114

This register enables and disables the reporting of the corresponding interrupt to system software. When a bit is set (1) and the corresponding interrupt condition is active, then an interrupt is generated. Interrupt sources that are disabled (0) are still reflected in the status registers. This register is symmetrical with the Port 0 Status register.

Bit Range	Default	Access	Field Name and Description
31	0h	RO	**Cold Presence Detect Enable (CPDE)** The SATA controller does not support cold presence detect.
30	0h	RW	**Task File Error Enable (TFEE)** When set, GHC.IE is set, and P0S.TFES is set, the HBA shall generate an interrupt.
29	0h	RW	**Host Bus Fatal Error Enable (HBFE)** When set, GHC.IE is set, and P0IS.HBFS is set, the HBA shall generate an interrupt.
28	0h	RW	**Host Bus Data Error Enable (HBDE)** when set, GHC.IE is set, and P0IS.HBDS is set, the HBA shall generate an interrupt.
27	0h	RW	**Interface Fatal Error Enable (IFE)** When set, GHC.IE is set, and P0IS.IFS is set, the HBA shall generate an interrupt.
26	0h	RW	**Interface Non-fatal Error Enable (INFE)** When set, GHC.IE is set, and P0IS.INFS is set, the HBA shall generate an interrupt.
25	-	-	**Reserved**
24	0h	RW	**Overflow Enable (OFE)** When set, and GHC.IE and P0IS.OFS are set, the HBA shall generate an interrupt.
23	0h	RW	**Incorrect Port Multiplier Enable (IPME)** When set, and GHC.IE and P0IS.IPMS are set, the HBA shall generate an interrupt. BIOS is required to program this field to '0'. The same applies to AHCI driver.

Bit Range	Default	Access	Field Name and Description
22	0h	RW	**PhyRdy Change Interrupt Enable (PRCE)** When set, and GHC.IE is set, and PxIS.PRCS is set, the HBA shall generate an interrupt.
21:8	-	-	**Reserved**
7	0h	RW/V	**Device Mechanical Presence Enable (DMPE)** When set, and P0IS.DMPS is set, the HBA shall generate an interrupt.
6	0h	RW	**Port Change Interrupt Enable (PCE)** When set, GHC.IE is set, and P0IS.PCS is set, the HBA shall generate an interrupt.
5	0h	RW	**Descriptor Processed Interrupt Enable (DPE)** When set, GHC.IE is set, and P0IS.DPS is set, the HBA shall generate an interrupt.
4	0h	RW	**Unknown FIS Interrupt Enable (UFE)** When set, GHC.IE is set, and PxIS.UFS is set to 1, the HBA shall generate an interrupt.
3	0h	RW	**Set Device Bits FIS Interrupt Enable (SDBE)** When set, GHC.IE is set, and P0IS.SDBS is set, the HBA shall generate an interrupt.
2	0h	RW	**DMA Setup FIS Interrupt Enable (DSE)** When set, GHC.IE is set, and P0IS.DSS is set, the HBA shall generate an interrupt.
1	0h	RW	**PIO Setup FIS Interrupt Enable (PSE)** When set, GHC.IE is set, and P0IS.PSS is set, the HBA shall generate an interrupt.
0	0h	RW	**Device to Host Register FIS Interrupt Enable (DHRE)** When set, GHC.IE is set, and P0IS.DHRS is set, the HBA shall generate an interrupt.

Port 0 Command (PxCMD0) – Offset 118

Port [0-7] Command

Bit Range	Default	Access	Field Name and Description
30:28	-	-	**Reserved**
27	0h	RW	**Aggressive Slumber Partial (ASP)** When set to 1, and the ALPE bit is set, the HBA shall aggressively enter the Slumber state when it clears a bit in the PxCI or PxSACT register and the register values are then PxCI = 0h and PxSACT = 0h. When cleared, and the ALPE bit is set, the HBA will aggressively enter the Partial state when it clears a bit in the PxCI or PxSACT register and the register values are then PxCI = 0h and PxSACT = 0h. If CAP.SALP is cleard to 0, software shall treat this bit as reserved.
26	0h	RW	**Aggressive Link Power Management Enable (ALPE)** When set, the HBA will aggressively enter a lower link power state (Partial or Slumber) based upon the setting of the ASP bit. Software shall only set this bit to 1 if CAP.SALP is set to 1. If CAP.SALP is cleared to 0, software shall treat this bit as reserved. BIOS is recommeded to program this field to 1.
25	0h	RW	**Drive LED on ATAPI Enable (DLAE)** When set, the HBA will drive the LED pin active for commands regardless of the state of PxCMD.ATAPI. When cleared, the HBA will only drive the LED pin active for commands if PxCMD.ATAPI is set to 0. This bit is set by software
24	0h	RW	**Device is ATAPI (ATAPI)** When set, the connected device is an ATAPI device. This bit is used by the HBA to control whether or not to generate the desktop LED when commands are active.
23	0h	RW	**Automatic Partial to Slumber Transitions Enabled (APSTE)** When set to 1, the HBA may perform Automatic Partial to Slumber Transitions. When cleared to 0 the port shall not perform Automatic Partial to Slumber Transitions. Software shall only set this bit to 1 if CAP2.APST is set to 1; if CAP2.APST is cleared to 0 software shall treat this bit as reserved.
22	0h	RO	**FIS-based Switching Capable Port (FBSCP)** The SATA controller does not support FIS-Based Switching.
21	0h	RW/O	**External SATA Port (ESP)** When set to 1, indicates that this port is routed externally and will be used with an external SATA device. When set to 1, CAP.SXS must also be set to 1. When cleared (0), indicates that this port is not routed externally and supports internal SATA devices only. If ESP is set to 1, then the port may experience hot plug events. Note : This bit is not reset on a HBA reset.
20	0h	RO	**Cold Presence Detection (CPD)** The SATA controller does not support cold presence detect.

Bit Range	Default	Access	Field Name and Description
19	0h	RW/O	**Mechanical Presence Switch Attached to Port (MPSP)** If set to 1, the platform supports a mechanical presence switch attached to this port. If cleared to 0, the platform does not support a mechanical presence switch attached to this port. When this bit is set to 1, PxCMD.HPCP should also be set to 1. The HBA takes no action on the state of this bit, it is for system software only. For example, if this bit is cleared, and an interlock switch toggles, the HBA shall still treat it as a proper interlock switch event. Note that this bit is not reset on a HBA reset.
18	0h	RW/O	**Hot Plug Capable Port (HPCP)** This indicates whether the this port is connected to a device which can be hot plugged. SATA by definition is hot-pluggable, but not all platforms are constructed to allow the device to be removed (it may be screwed into the chassis, for example). This bit can be used by system software to indicate a feature such as eject device to the end-user. The HBA takes no action on the state of this bit, it is for system software only. For example, if this bit is cleared, and a hot plug event occurs, the HBA shall still treat it as a proper hot plug event. This bit is not reset on a HBA reset.
17	0h	RW/V	**Port Multiplier Attached (PMA)** When set, a Port Multiplier is attached to the HBA for this port. When cleared, a Port Multiplier is not attached to the HBA for this port. This bit is a read only 0. when CAP.PMS = 0, and read/write when CAP.PMS = 1. Note that this bit is set by software; hardware does not auto-detect that a Port Multiplier is attached.
16	-	-	**Reserved**
15	0h	RO/V	**Command List Running (CR)** When this bit is set it indicates that the command list DMA engine for the port is running.
14	0h	RO/V	**FIS Receive Running (FR)** When this bit is set it indicates that the FIS Receive DMA engine for the port is running. Note to software: When FR bit stays set, please read the PxIS.PCS and PxSERR.DET.X to service the PCS interrupt accordingly if any
13	0h	RO/V	**Mechanical Presence Switch State (MPSS)** The MPSS bit reports the state of a mechanical presence switch attached to this port. If CAP.SMPS is set to 1 and the mechanical presence switch is closed then this bit is cleared to 0. If CAP.SMPS is set to 1 and the mechanical presence switch is open then this bit is set to 1. If CAP.SMPS is set to 0 then this bit is cleared to 0. Software should only use this bit if both CAP.SMPS and PxCMD.MPSP are set to 1.

Bit Range	Default	Access	Field Name and Description
12:8	00h	RO/V	**Current Command Slot (CCS)** Indicates the current command slot the HBA is processing. This field is valid when the PxCMD.ST bit is set, and is constantly updated by the HBA. This field can be updated as soon as the HBA recognizes an active command slot, or at some point soon after when it begins processing the command. When PxCMD.ST transitions from a 1 to a 0, the HBA will reset this field to 0. After PxCMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is PxCMD.CCS + 1. For example, after the HBA has issued its first command, if PxCMD.CCS = 0h and PxCI is set to 3h, the next command that will be issued is from command slot 1.
7:5	-	-	**Reserved**
4	0h	RW	**FIS Receive Enable (FRE)** When set, the HBA may post received FISes into the FIS receive area pointed to by PxFB and PxFBU. When cleared, received FISes are not accepted by the HBA, except for the first D2H register FIS after the initialization sequence. System software must not set this bit until PxFB and PxFBU have been programmed with a valid pointer to the FIS receive area. If software wishes to move the base, this bit must first be cleared, and software must wait for the PxCMD.FR bit to be cleared before updating PxFB and PxFBU. Software must not clear this bit while PxCMD.ST is set to 1.
3	0h	RW/1S/V	**Command List Override (CLO)** Setting this bit to 1 causes PxTFD.STS.BSY and PxTFD.STS.DRQ to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The HBA sets this bit to 0 when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to 0. A write to this register with a value of 0 shall have no effect. This bit shall only be set to 1 immediately prior to setting the PxCMD.ST bit to 1 from a previous value of 0. Setting this bit to 1 at any other time is not supported and will result in indeterminate behavior. Software must wait for CLO to be cleard to 0 before setting PxCMD.ST to 1.
2	1h	RO	**Power On Device (POD)** The SATA controller does not support cold presence detect.
1	0h	RW/V	**Spin-Up Device (SUD)** This bit is read/write for HBAs that support staggered spin-up via CAP.SSS. This bit is read only 1 for HBAs that do not support staggered spin-up. On an edge detect from 0 to 1, the HBA shall start a COMRESET initializatoin sequence to the device. Clearing this bit causes no action on the interface. Clearing this bit to 0 does not cause any OOB signal to be sent on the interface. When this bit is cleared to 0 and PxSCTL.DET = 0h, the HBA will enter listen mode.

Bit Range	Default	Access	Field Name and Description
0	0h	RW	**Start (ST)** When set, the HBA may process the command list. When cleared, the HBA may not process the command list. Whenever this bit is changed from a 0 to a 1, the HBA starts processing the command list at entry 0. Whenever this bit is changed from a 1 to a 0, the PxCI and PxSACT register is cleared by the HBA upon the HBA putting the controller into an idle state. PxTFD shall be updated also. See section 10.3.1 of the AHCI spec for restrictions on when PxCMD.ST can be set to 1 and cleared to 0.

Port 0 Task File Data (PxTFD0) – Offset 120

This is a 32-bit register that copies specific fields of the task file when FISes are received. The FISes that contain this information are: D2H Register FIS; PIO Setup FIS; Set Device Bits FIS (BSY and DRQ are not updated with this FIS).

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:8	00h	RO/V	**Error (ERR)** Contains the latest copy of the task file error register.
7	0h	RO/V	**Status Busy (STS_BSY)** Status - Indicates the interface is busy.
6:4	-	-	**Reserved**
3	1h	RO/V	**Status Drq (STS_DRQ)** Status - Indicates a data transfer is requested.
2:1	-	-	**Reserved**
0	1h	RO/V	**Status Err (STS_ERR)** Status - Indicates an error during the transfer.

Port 0 Signature (PxSIG0) – Offset 124

This is a 32-bit register that contains the initial signature of an attached device when the first D2H Register FIS is received

from that device. It is updated once after a reset sequence.

Bit Range	Default	Access	Field Name and Description
31:0	FFFFFFFFh	RO/V	**Signature (SIG)** Contains the signature received from a device on the first D2H Register FIS. The bit order is as follows: 31:24 bits represent LBA High Register; 23:16 bits represent LBA Mid Register; 15:8 bits represent LBA Low Register; 7:0 bits represent Sector Count Register.

Port 0 Serial ATA Status (PxSSTS0) – Offset 128

This is a 32-bit register that conveys the current state of the interface and host. The HBA updates it continuously and asynchronously. When the HBA transmits a COMRESET to the device, this register is updated to its reset values.

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**
11:8	0h	RO/V	**Interface Power Management (IPM)** Indicates the current interface state. This field reflects the interface power management state for both device and host initiated power management. If an Automatic Partial to Slumber Transition occurs, PxSSTS.IPM shall reflect that the host has entered Slumber (PxSSTS.IPM = 6h).
7:4	0h	RO/V	**Current Interface Speed (SPD)** Indicates the negotiated interface communication speed.
3:0	0h	RO/V	**Device Detection (DET)** Indicates the interface device detection and Phy state. While the true reset default value of this register is 0h, the value read from this register depends on drive presence and the point in time within the initialization process when the register is read. The means by which the implementation determines device presence may be vendor specific. However, device presence shall always be indicated anytime a COMINIT signal is received.

Port 0 Serial ATA Status (PxSCTL0) – Offset 12c

This is a 32-bit read-write register by which software controls SATA capabilities. Writes to this register result in an action being taken by the host adapter or interface. Reads from the register return the last value written to it.

Bit Range	Default	Access	Field Name and Description
30:20	-	-	**Reserved**
19:16	0h	RW	**Port Multiplier Port (PMP)** This field is not used by AHCI.
15:12	0h	RW	**Select Power Management (SPM)** This field is not used by AHCI.
11:8	0h	RW	**Interface Power Management Transitions Allowed (IPM)** Indicates which power states the HBA is allowed to transition to. If an interface power management state is not allowed via this register field, the HBA will not initiate that state and the HBA will PMNAKP any request from the device to enter that state.
7:4	0h	RW	**Speed Allowed (SPD)** Indicates the highest allowable speed of the interface. If software changes SPD after port has been enabled, software is required to perform a port reset via DET=1h.
3:0	0h	RW	**Device Detection Initialization (DET)** Controls the HBA.s device detection and interface initialization. This field may only be changed when PxCMD.ST is 0. Changing this field while the HBA is running results in undefined behavior. When PxCMD.ST is set to 1, this field should have a value of 0h. It is permissible to implement any of the Serial ATA defined behaviors for transmission of COMRESET when PxSCTL.DET = 1h.

Port 0 Serial ATA Error (PxSERR0) – Offset 130

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/1C/V	**Diagnostics (DIAG)** Contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. Bit 31:27 : Reserved; Bit 26(Exchanged) : When set to one this bit indicates that a change in device presence has been detected since the last time this bit was cleared. The means by which the implementation determines that the device presence has changed is vendor specific. This bit shall always be set to one anytime a COMINIT signal is received. This bit is reflected in the P0IS.PCS bit.; Bit 25(Unrecognized FIS Type) : Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized/known.; Bit 24(Transport state transition error) : Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared.; Bit 23(Link Sequence Error) : Indicates that one or more Link state machine error conditions were encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition.; Bit 22(Handshake Error) : Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.; Bit 21(CRC Error) : Indicates that one or more CRC errors occurred with the Link Layer.; Bit 20(Disparity Error) : This field is not used by AHCI. This bit is not implemented and always read only 0.; Bit 19(10B to 8B Decode Error) : Indicates that one or more 10B to 8B decoding errors occurred.; Bit 18(Comm Wake) : Indicates that a Comm Wake signal was detected by the Phy.; Bit 17(Phy Internal Error) : Indicates that the Phy detected some internal error. This bit is not implemented and always read only 0.; Bit 16(PhyRdy Change) : When set to 1 this bit indicates that the internal PhyRdy signal changed state since the last time this bit was cleared. The state of this bit is reflected in the PxIS.PRCS interrupt status bit and an interrupt will be generated if enabled.

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW/1C/V	**Error (ERR)** The ERR field contains error information for use by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer. Bit 15:12 : Reserved; Bit 11(Internal Error) : The SATA controller failed due to a master or target abort when attempting to access system memory.; Bit 10(Protocol Error) : A violation of the Serial ATA protocol was detected.; Bit 9(Persistent Communication or Data Integrity Error): A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes. This bit is not implemented and always read only 0.; Bit 8(Transient Data Integrity Error) : A data integrity error occurred that was not recovered by the interface.; Bit 7:2 : Reserved; Bit 1(Recovered Communications Error) : Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers.; Bit 0(Recovered Data Integrity Error) : A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

Port [0] Serial ATA Active (PxSACT0) – Offset 134

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW/1S/V	**Device Status (DS)** System software sets this bit for native command queuing commands prior to setting the PxCI.CI bit in the same command slot entry. This field is cleared via the Set Device Bits FIS. This field is also cleared when PxCMD.ST is cleared by software. This field is not cleared by COMRESET or SRST.

Port 0 Commands Issued (PxCI0) – Offset 138

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW/1S/V	**Commands Issued (CI)** This field is set by software to indicate to the HBA that a command has been built in system memory for a command slot and may be sent to the device. When the HBA receives a FIS which clears the BSY, ERR, and DRQ bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to '1' by software when PxCMD.ST is set to '1'. This field is also cleared when PxCMD.ST is written from a 1 to a 0 by software.

Port 0 Device Sleep (PxDEVSLP0) – Offset 144

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**
28:25	Fh	RW/O	**DITO Multiplier (DM)** 0's based value that specifies the DITO multiplier that the HBA applies to the specified DITO value, effectively extending the range of DITO from 1ms to 16368ms. A value of 0h indicates a multiplier of 1. A maximum multiplier of 16 may be applied. The HBA computes the total idle timeout as a product of DM and DITO (i.e. DITO actual = DITO *(DM + 1)). These bits are not reset on an HBA reset.
24:15	004h	RW/V	**DEVSLP Idle Timeout (DITO)** This field specifies the amount of the time (in approximate 1ms granularity) that the HBA shall wait before driving the DEVSLP signal.Hardware reloads its port specific DEVSLP timer with this value each time the port transitions out of DEVSLP state. For example: from DEVSLP to active or PxDEVSLP.ADSE transitions from 0 to a 1. If CAP2.SDS or CAP2.SADM or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0 and PxDEVSLP.ADSE is cleared to 0. These bits are not reset on an HBA reset.
14:10	0Ah	RW/V	**DEVSLP Minimum Assertion Time (MDAT)** This field specifies the minimum amount of time (in 1ms granularity) that the HBA must assert the DEVSLP signal before it may be de-asserted. The nominal value is 10ms and the minimum is 1ms depending on device identification information. If CAP2.SDS is cleared to 0 or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0, PxDEVSLP.ADSE is cleared to 0, and prior to setting PxCMD.ICC to 8h. These bits are not reset on an HBA reset.
9:2	14h	RW/V	**DEVSLP Exit Timeout (DETO)** This field specifies the maximum duration (in approximate 1ms granularity) from DEVSLP de-assertion until the device is ready to accept OOB. The nominal value is 20ms while the max value is 255ms depending on device identification information. If CAP2.SDS is cleared to 0 or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0, PxDEVSLP.ADSE is cleared to 0, and prior to setting PxCMD.ICC to 8h. These bits are not reset on a HBA reset.
1	1h	RW/O	**Device Sleep Present (DSP)** If set to '1', the platform supports DEVSLP on this port. If cleared to '0', the platform does not support DEVSLP on this port. This bit may only be set to '1' if CAP2.SDS is set to '1'.DSP is mutually exclusive with the PxCMD.HPCP bit and PxCMD.ESP bit. BIOS is required to program this field to 1 if the system supports the DEVSLP feature. Note: These bits are not reset on a HBA reset.

Bit Range	Default	Access	Field Name and Description
0	0h	RW/V	**Aggressive DEVSLP Enable (ADSE)** This bit is read/write for HBAs that support aggressive DEVSLP management (CAP2.SADM = 1). When this bit is set to 1, the HBA shall assert the DEVSLP signal after the port has been idle (PxCI = 0h and PxSACT = 0h) for the amount of time specified by the PxDEVSLP.DITO register and the interface is in Slumber (PxSSTS.IPM = 6h). When this bit is cleared to 0, the HBA does not enter DEVSLP unless software directed via PxCMD.ICC. This bit shall only be set to 1 if PxDEVSLP.DSP is set to 1. If this bit is set to 1 and software clears the bit to 0, then the HBA shall de-assert the DEVSLP signal if asserted. These bits are not reset on a HBA reset. BIOS is recommended to program this field to 1 if the platform support the DEVSLP feature. If CAP2.SDS is cleared to 0 or CAP2.SADM is cleared to 0, or if PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved.

Port 1 Command List Base Address (PxCLB1) – Offset 180

Same bit definition as PxCLB0.

Port 1 Command List Base Address Upper 32-bits (PxCLBU1) – Offset 184

Same bit definition as PxCLBU0

Port 1 FIS Base Address (PxFB1) – Offset 188

Same definition as PxFB0.

Port 0 FIS Base Address Upper 32-bits (PxFBU1) – Offset 18c

Same definition as PxFBU0.

Port 1 Interrupt Status (PxIS1) – Offset 190

Same definition as PxIS0.

Port 0 Interrupt Enable (PxIE1) – Offset 194

Same definition as PxIE0.

Port 1 Command (PxCMD1) – Offset 198

Same definition as PxCMD0.

Port 1 Task File Data (PxTFD1) – Offset 1a0

Same definition as PxTFD0.

Port 1 Signature (PxSIG1) – Offset 1a4

Same definition as PxSIG0.

Port 0 Serial ATA Status (PxSSTS1) – Offset 1a8

Same definition as PxSSTS0.

Port 1 Serial ATA Control (PxSCTL1) – Offset 1ac

Same definition as PxSCTL0.

Port 1 Serial ATA Error (PxSERR1) – Offset 1b0

Same definition as PxSERR0.

Port 1 Serial ATA Active (PxSACT1) – Offset 1b4

Same definition as PxSACT0.

Port 1 Commands Issued. (PxCI1) – Offset 1b8

Same definition as PxCI0.

Port 1 Device Sleep (PxDEVSLP1) – Offset 1c4

Same definition as PxDEVSLP0.

Port 2 Command List Base Address (PxCLB2) – Offset 200

Same definition as PxCLB0.

Port 2 Command List Base Address Upper 32-bits (PxCLBU2) – Offset 204

Same definition as PxCLBU0.

Port 2 FIS Base Address (PxFB2) – Offset 208

Same definition as PxFB0.

Port 2 FIS Base Address Upper 32-bits (PxFBU2) – Offset 20c

Same definition as PxFBU0.

Port 2 Interrupt Status (PxIS2) – Offset 210

Same definition as PxIS0.

Port 2 Interrupt Enable (PxIE2) – Offset 214

Same definition as PxIE0.

Port 2 Command (PxCMD2) – Offset 218

Same definition as PxCMD0.

Port 2 Task File Data (PxTFD2) – Offset 220

Same definition as PxTFD0.

Port 2 Signature (PxSIG2) – Offset 224

Same definition as PxSIG0.

Port 2 Serial ATA Status (PxSSTS2) – Offset 228

Same definition as PxSSTS0.

Port 2 Serial ATA Control (PxSCTL2) – Offset 22c

Same definition as PxSCTL0.

Port 2 Serial ATA Error (PxSERR2) – Offset 230

Same definition as PxSERR0.

Port 2 Serial ATA Active (PxSACT2) – Offset 234

Same definition as PxSACT0.

Port 2 Commands Issued (PxCI2) – Offset 238

Same definition as PxCI0.

Port 2 Device Sleep (PxDEVSLP2) – Offset 244

Same definition as PxDEVSLP0.

SATA AIDP Registers

Summary of Bus:, Device:, Function: (IO)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
10h	4	AHCI Index Register (INDEX)	0h
14h	4	AHCI Data Register (DATA)	0h

AHCI Index Register (INDEX) – Offset 10

This registers are only available if CC.SCC is not 01h to index into all memory registers defined in Memory Registers and the message buffer used for enclosure management. If CC.SCC is 01h, these AHCI Index Data Pair registers are not accessible and SINDEX/SDATA register pair shall be used to index into a subset of the memory registers.(See Memory Registers for more information on which registers could be indexed).

Bit Range	Default	Access	Field Name and Description
30:19	-	-	**Reserved**
18:2	0h	RW	**Index (INDEX)** This Index register is used to select the Dword offset of the Memory Mapped AHCI register to be accessed. A Dword, Word or Byte access is specified by the active byte enables of the I/O access to the Data register.
1:0	-	-	**Reserved**

AHCI Data Register (DATA) – Offset 14

This registers are index into all memory registers defined in Memory Registers and the message buffer used for enclosure management.

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Data (DATA)** This Data register is a window through which data is read or written to the memory mapped register pointed to by the Index register. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the default value is the same as the default value of the register pointed to by Index.

SATA Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Identifiers (ID)	XXXX8086h
4h	2	Command (CMD)	0h
6h	2	Device Status (STS)	210h
8h	1	Revision ID (RID)	XXh
9h	1	Programming Interface (PI)	1h
ah	2	Class Code (CC)	106h
ch	1	Cache Line Size (CLS)	0h
dh	1	Master Latency Timer (MLT)	0h
eh	1	Header Type (HTYPE)	0h
10h	4	MSI-X Table Base Address (MXTBA)	0h
14h	4	MSI-X Pending Bit Array Base Address (MXPBA)	0h
20h	4	AHCI Index Data Pair Base Address (AIDPBA)	1h
24h	4	AHCI Base Address (ABAR)	0h
2ch	4	Sub System Identifiers (SS)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
34h	1	Capabilities Pointer (CAP)	80h
3ch	2	Interrupt Information (INTR)	100h
70h	2	PCI Power Management Capability ID (PID)	A801h
72h	2	PCI Power Management Capabilities (PC)	4003h
74h	2	PCI Power Management Control and Status (PMCS)	8h
80h	2	Message Signalled Interrupt Identifier (MID)	7005h
82h	2	Message Signalled Interrupt Message Control (MC)	0h
84h	4	Message Signalled Interrupt Message Address (MA)	0h
88h	2	Message Signalled Interrupt Message Data (MD)	0h
90h	4	Port Mapping Register (MAP)	0h
94h	4	Port Control and Status (PCS)	0h
9ch	4	SATA General Configuration (SATAGC)	0h
a0h	1	SATA Initialization Register Index (SIRI)	0h
a4h	4	SATA Initialization Register Data (SIRD)	0h
a8h	4	Serial ATA Capability Register 0 (SATACR0)	100012h
ach	4	Serial ATA Capability Register 1 (SATACR1)	48h
c0h	4	Scratch Pad (SP)	0h
d0h	2	MSI-X Identifiers (MXID)	11h
d2h	2	MSI-X Message Control (MXC)	0h
d4h	4	MSI-X Table Offset / Table BIR (MXT)	0h
d8h	4	MSI-X PBA Offset / PBA BIR (MXP)	1h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
e0h	4	BIST FIS Control/Status (BFCS)	0h
e4h	4	BIST FIS Transmit Data 1 (BFTD1)	0h
e8h	4	BIST FIS Transmit Data 2 (BFTD2)	0h

Identifiers (ID) – Offset 0

When the MMIO RUN.RUNE=1, read access to this double-word is return with UR.

Bit Range	Default	Access	Field Name and Description
31:16	See Description	RO	**Device ID (DID)** Indicates the Device ID of the SATA controller. Refer to the Device and Revision ID Table in Volume 1 for default value
15:0	8086h	RO	**Vendor ID (VID)** 16-bit field which indicates the company vendor as Intel.

Command (CMD) – Offset 4

Command

Bit Range	Default	Access	Field Name and Description
14:11	-	-	**Reserved**
10	0h	RW	**Interrupt Disable (ID)** This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt and MSI is not enabled. 1 = Internal INTx# messages will not be generated.

Bit Range	Default	Access	Field Name and Description
9	-	-	**Reserved**
8	0h	RW	**SERR# Enable (SEE)** 0 = SERR# messages will not be generated. 1 = SERR# messages are generated if STS.DPD register is set or bit 8 of the SATAGC.URD register is set.
7	-	-	**Reserved**
6	0h	RW	**Parity Error Response Enable (PEE)** 0 = Disabled. SATA controller will not generate PERR# when a data parity error is detected. 1 = Enabled. SATA controller will generate PERR# when a data parity error is detected.
5:3	-	-	**Reserved**
2	0h	RW	**Bus Master Enable (BME)** Controls the SATA Controller's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands.
1	0h	RW	**Memory Space Enable (MSE)** Controls access to the SATA Controller's target memory space (for AHCI). If Fabric Decoding scheme is used, this register bit is shadowed by the Fabric Decoder.
0	0h	RW	**I/O Space Enable (IOSE)** Controls access to the SATA Controller's target I/O space. If Fabric Decoding scheme is used, this register bit is shadowed by the Fabric Decoder.

Device Status (STS) – Offset 6

Device Status

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
15	0h	RW/1C/V	**Detected Parity Error (DPE)** 0 = No parity error detected by SATA controller. 1 = SATA controller detects a parity error on its interface.
14	0h	RW/1C/V	**Signalled System Error (SSE)** 0 = No SERR# detected by SATA controller. 1 = SATA controller detects a SERR# on its interface.
13	0h	RW/1C/V	**Received Master-Abort Status (RMA)** 0 = Master abort not generated. 1 = SATA controller received a master abort.
12	0h	RW/1C/V	**Received Target-Abort Status (RTA)** 0 = Target abort not generated. 1 = SATA controller received a target abort.
11	0h	RW/1C/V	**Signalled Target-Abort Status (STA)** This bit must be set by a target device whenever it terminates a transaction with Target-Abort. Devices that will never signal Target-Abort do not need to implement this bit.
10:9	1h	RO	**DEVSEL# Timing Status (DEVT)** 01 = Hardwired; Controls the device select time for the SATA controller's PCI interface.
8	0h	RW/1C/V	**Master Data Parity Error Detected (DPD)** For PCH, this bit can only be set on read completions received from the bus when there is a parity error. 0 = No data parity error received. 1 = SATA controller, as a master, either detects a parity error or sees the parity error line asserted, and the parity error response bit (bit 6 of the command register) is set.
7:5	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
4	1h	RO	**Capabilities List (CL)** Indicates the presence of a capabilities list. The minimum requirement for the capabilities list must be PCI power management for the SATA Controller.
3	0h	RO/V	**Interrupt Status (IS)** Reflects the state of INTx# messages, IRQ14 or IRQ15. 0 = Interrupt is cleared (independent of the state of CMD.ID). 1 = Interrupt is to be asserted
2:0	-	-	**Reserved**

Revision ID (RID) – Offset 8

Revision ID

Bit Range	Default	Access	Field Name and Description
7:0	See Description	RO	**Revision ID (RID)** Indicates stepping of the host controller hardware. Refer to the Device and Revision ID Table in Volume 1 for default value.

Programming Interface (PI) – Offset 9

Programming Interface

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
7:0	01h	RO	**Interface (IF)** If CC.SCC=06h (AHCI mode), it indicates that this is an AHCI HBA that has a major revision of 1. If CC.SCC=04h (RAID mode), it indicates that there is no programming interface (IF=00h).

Class Code (CC) – Offset a

Class Code

Bit Range	Default	Access	Field Name and Description
15:8	01h	RO	**Base Class Code (BCC)** Indicates that this is a mass storage device.
7:0	06h	RO	**Sub Class Code (SCC)** This field specifies the sub-class code of the controller, per the table below: MAP.SMS SCC Register Value 0b 06h (AHCI Controller) 1b 04h (RAID Controller)

Cache Line Size (CLS) – Offset c

Cache Line Size

Bit Range	Default	Access	Field Name and Description
7:0	00h	RO	**Cache Line Size (CLS)** This register has no meaning for the SATA controller.

Master Latency Timer (MLT) – Offset d

Master Latency Timer

Bit Range	Default	Access	Field Name and Description
7:0	00h	RO	**Master Latency Timer (MLT)** This register has no meaning for the SATA controller.

Header Type (HTYPE) – Offset e

Header Type

Bit Range	Default	Access	Field Name and Description
7	0h	RO	**Multi-function Device (MFD)** 1 indicates this controller is part of a multi-function device. 0 indicates this controller is a single function device. The value of this bit depends on the wire strap istrap_c1_MultiFunctionDevice at the SATA Host Controller top level, driven by SoC.
6:0	00h	RO	**Header Layout (HL)** Indicates that the controller uses a target device layout.

MSI-X Table Base Address (MXTBA) – Offset 10

This BAR is used to allocate 32K, 16K or 8K Memory space for the MSI-X Table. The Memory space size is determined by BIOS by making bit-14 and bit-13 Read-Only '1' or Read-Write '0' based on SATAGC.MSS[1:0].

Bit Range	Default	Access	Field Name and Description
31:15	0h	RW	**Base Address (BA)** Base address of memory space.
14	0h	RW	**Base Address Bit 14 (BAB14)** When SATAGC.MSS[1:0]=00, this bit is Read Only '0' else it's Read Write '0'.
13	0h	RW	**Base Address Bit 13 (BAB13)** When SATAGC.MSS[1:0]=00 or 01, this bit is Read Only '0' else it's Read Write '0'.
12:4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3	0h	RO	**Prefetchable (PF)** Indicates that this range is not pre-fetchable.
2:1	0h	RO	**Type (TP)** Indicates that this range can be mapped anywhere in 32-bit address space.
0	0h	RO	**Resource Type Indicator (RTE)** Indicates a request for Memory space.

MSI-X Pending Bit Array Base Address (MXPBA) – Offset 14

This BAR is used to allocate 256-byte Memory space for the MSI-X PBA.

Bit Range	Default	Access	Field Name and Description
31:8	0h	RW	**Base Address (BA)** Base address of memory space (aligned to 256B).
7:4	-	-	**Reserved**
3	0h	RO	**Prefetchable (PF)** Indicates that this range is not pre-fetchable.
2:1	0h	RO	**Type (TP)** Indicates that this range can be mapped anywhere in 32-bit address space.
0	0h	RO	**Resource Type Indicator (RTE)** Indicates a request for Memory space.

AHCI Index Data Pair Base Address (AIDPBA) – Offset 20

This BAR is used to allocate I/O space for the AHCI index/data pair mechanism.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:5	0h	RW	**Base Address (BA)** Base address of the I/O space.
4:1	-	-	**Reserved**
0	1h	RO	**Resource Type Indicator (RTE)** Indicates a request for IO space.

AHCI Base Address (ABAR) – Offset 24

This register represents a memory BAR allocating space for the AHCI memory registers. If the Fabric Decoding scheme is used, this register is shadowed by the Fabric Decoder. Note that Bit[31:16] of this register must be programmed to a value greater than 0 to ensure the memory is mapped to an address of 1 MBytes and greater (i.e. ABAR must be 00010000h or greater). Otherwise, memory cycle targeting the ABAR range may not be accepted. The Memory space size is determined by BIOS by making bit 15:11 Read-Only 1 or Read-Write 0 based on SATAGC.ASSEL[1:0].

Bit Range	Default	Access	Field Name and Description
31:19	0h	RW	**Base Address (BA)** Base address of register memory space.
18	0h	RW	**Base Address Bit 18 (BAB18)** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 256K, this bit is Read Only '0' else it's Read Write '0'.
17	0h	RW	**Base Address Bit 17 (BAB17)** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 128K, this bit is Read Only '0' else it's Read Write '0'.
16	0h	RW	**Base Address Bit 16 (BAB16)** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 64K, this bit is Read Only '0' else it's Read Write '0'.
15	0h	RW	**Base Address Bit 15 (BAB15)** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 32K, this bit is Read Only '0' else it's Read Write '0'.

Bit Range	Default	Access	Field Name and Description
14	0h	RW	**Base Address Bit 14 (BAB14)** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 16K, this bit is Read Only '0' else it's Read Write '0'.
13:11	0h	RW	**Base Address Bit 13-11 (BAB1311)** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 2K, this bit is Read Only '0' else it's Read Write '0'.
10:4	-	-	**Reserved**
3	0h	RO	**Prefetchable (PF)** Indicates that this range is not pre-fetchable
2:1	0h	RO	**Type (TP)** Indicates that this range can be mapped anywhere in 32-bit address space
0	0h	RO	**Resource Type Indicator (RTE)** Indicates a request for register memory space.

Sub System Identifiers (SS) – Offset 2c

This register is initialized to logic 0 by the assertion of PLTRST#. This register can be written only once after PLTRST# de-assertion.

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/O	**Subsystem ID (SSID)** This is written by BIOS. No hardware action taken on this value.
15:0	0000h	RW/O	**Subsystem Vendor ID (SSVID)** This is written by BIOS. No hardware action taken on this value.

Capabilities Pointer (CAP) – Offset 34

Capabilities Pointer

Bit Range	Default	Access	Field Name and Description
7:0	80h	RW/L	**Capability Pointer (CP)** Indicates that the first capability pointer offset is 80h. Note: Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR.

Interrupt Information (INTR) – Offset 3c

Interrupt Information

Bit Range	Default	Access	Field Name and Description
15:8	01h	RW/O	**Interrupt Pin (IPIN)** This register tells which interrupt pin the device function uses. A value of 1 corresponds to INTA#. A value of 2 corresponds to INTB#. A value of 3 corresponds to INTC#. A value of 4 corresponds to INTD#. This register is not reset by FLR.
7:0	00h	RW	**Interrupt Line (ILINE)** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. Interrupt Line register is not reset by FLR.

PCI Power Management Capability ID (PID) – Offset 70

PCI Power Management Capability ID

Bit Range	Default	Access	Field Name and Description
15:8	A8h	RW/L	**Next Capability (NEXT)** A8h is the location of the Serial ATA capability structure. Note: Refer to the SGC.REGLOCK description in order to lock the register to become RO.
7:0	01h	RO	**Cap ID (CID)** Indicates that this pointer is a PCI power management capability.

PCI Power Management Capabilities (PC) – Offset 72

PCI Power Management Capabilities

Bit Range	Default	Access	Field Name and Description
15:11	08h	RO	**PME_Support (PME_Support)** The default value 01000 which indicates PME# can be generated from the D3HOT state in the SATA controller.
10	0h	RO	**D2_Support (D2_Support)** The D2 state is not supported.
9	0h	RO	**D1_Support (D1_Support)** The D1 state is not supported.
8:6	0h	RO	**Aux_Current (Aux_Current)** PME# from D3COLD state is not supported, therefore this field is 000b.
5	0h	RO	**Device Specific Initialization (DSI)** Indicates that no device-specific initialization is required.
4	-	-	**Reserved**
3	0h	RO	**PME Clock (PMEC)** Indicates that PCI clock is not required to generate PME#.
2:0	3h	RO	**Version (VS)** Indicates support for Revision 1.2 of the PCI Power Management Specification.

PCI Power Management Control and Status (PMCS) – Offset 74

PCI Power Management Control and Status

Bit Range	Default	Access	Field Name and Description
15	0h	RW/1C/V	**PME Status (PMES)** Bit is set when a PME event is to be requested, and if this bit and PMEE is set, a PME# will be generated from the SATA controller.

Bit Range	Default	Access	Field Name and Description
14:9	-	-	**Reserved**
8	0h	RW	**PME Enable (PMEE)** When set, the SATA controller asserts PME# when exiting D3HOT on a wake event. Note: Software is advised to clear PMEE and PMES together prior to changing CC.SCC through MAP.SMS.
7:4	-	-	**Reserved**
3	1h	RO	**No Soft Reset (NSFRST)** These bits are used to indicate whether devices transitioning from D3HOT state to D0 state will perform an internal reset. 0 = Device transitioning from D3HOT state to D0 state perform an internal reset. 1 = Device transitioning from D3HOT state to D0 state do not perform an internal reset. Configuration content is preserved. Upon transition from the D3HOT state to D0 state initialized state, no additional operating system intervention is required to preserve configuration context beyond writing to the PowerState bits. Regardless of this bit, the controller transition from D3HOT state to D0 state by a system or bus segment reset will return to the state D0 uninitialized with only PME context preserved if PME is supported and enabled.
2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1:0	0h	RW	**Power State (PS)** These bits are used both to determine the current power state of the SATA controller and to set a new power state. 00 = D0 state 11 = D3HOT state When in the D3HOTstate, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked.

Message Signalled Interrupt Identifier (MID) – Offset 80

Message Signalled Interrupt Identifier

Bit Range	Default	Access	Field Name and Description
15:8	70h	RW/L	**Next Pointer (NEXT)** Indicates the next item in the list is the PCI power management pointer. BIOS may program this field to A8h indicating that the next item is Serial ATA Capability Structure. Note: Refer the SGC.REGLOCK description in order to lock the register to become RO.
7:0	05h	RO	**Capability ID (CID)** Capabilities ID indicates MSI.

Message Signalled Interrupt Message Control (MC) – Offset 82

Message Signalled Interrupt Message Control

Bit Range	Default	Access	Field Name and Description
14:8	-	-	**Reserved**
7	0h	RO	**64-Bit Address Capable (C64)** Capable of generating a 32-bit message only.
6:4	0h	RO	**Multiple Message Enable (MME)** When this field is cleared to 000 (and MSIE is set), only a single MSI message will be generated for all SATA ports, and bits [15:0] of the message vector will be driven from MD[15:0].
3:1	0h	RO	**Multiple Message Capable (MMC)** Not supported.
0	0h	RW	**MSI Enable (MSIE)** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. Note that CMD.ID bit has not effect on MSI. Software must clear this bit to 0 to disable MSI first before changing the number of messages allocated in the MMC field.

Message Signalled Interrupt Message Address (MA) – Offset 84

Message Signalled Interrupt Message Address

Bit Range	Default	Access	Field Name and Description
31:2	0h	RW	**Address (ADDR)** Lower 32 bits of the system specified message address, always DWORD aligned.
1:0	-	-	**Reserved**

Message Signalled Interrupt Message Data (MD) – Offset 88

Message Signalled Interrupt Message Data

Bit Range	Default	Access	Field Name and Description
15:0	0h	RW	**Data (DATA)** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word of the data bus of the MSI memory write transaction.

Port Mapping Register (MAP) – Offset 90

Port Mapping Register

Bit Range	Default	Access	Field Name and Description
30:19	-	-	**Reserved**
18	0h	RW/O	**SATA Port 2 Disable (SPD2)** Same description as bit 16, except this bit is for Port 2.
17	0h	RW/O	**SATA Port 1 Disable (SPD1)** Same description as bit 16, except this bit is for Port 1.
16	0h	RW/O	**SATA Port 0 Disable (SPD0)** Software programs these bits to disable a SATA port on the controller. 1 = Port 0 is disabled. 0 = Port 0 is enabled. Notes: 1. To ensure a port is properly disabled, BIOS shall configure MAP.SPD first and then configure PCS.PxE. 2. This field is not reset by FLR.
15:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	0h	RW	**Port Clock Disable (PCD)** 0 = All clocks to the associated port logic will operate normally. 1 = The backbone clock driven to the associated port logic is gated and will not toggle. Assignment of the bits is: Bit 7: Port 7 Bit 6: Port 6 Bit 5: Port 5 Bit 4: Port 4 Bit 3: Port 3 Bit 2: Port 2 Bit 1: Port 1 Bit 0: Port 0 If a particular port is not available, software shall set the corresponding bit to 1. Software can also set the corresponding bit(s) to 1 after disabling particular port(s). Software cannot set the PCD [port x]='1' if the corresponding PCS.PxE='1' or AHCI GHC.PI[x]='1'.

Port Control and Status (PCS) – Offset 94

By default, the SATA ports are set (by hardware) to the disabled state (e.g. bits[5:0] == '0') as a result of an initial power on reset. When enabled by software, the ports can transition between the on, partial, and slumber states and can detect devices. When disabled, the port is in the off state and cannot detect any devices. Note: This register is not reset by FLR. Note: AHCI specific notes: If an AHCI-aware or RAID enabled operating system is being booted then system BIOS shall insure that all supported SATA ports are enabled prior to passing control to the OS. Once the AHCI aware OS is booted it becomes the enabling/disabling policy owner for the individual SATA ports. This is accomplished by manipulating a port's PxSCTL.DET and PxCMD.SUD fields. Because an AHCI or RAID aware OS will typically not have knowledge of the PxE bits and because the PxE bits act as master on/off switches for the ports, pre-boot software must insure that these bits are set to '1' prior to booting the OS, regardless as to whether or not a device is currently on the port.

Bit Range	Default	Access	Field Name and Description
30:19	-	-	**Reserved**
18	0h	RO/V	**Port 2 Present (P2P)** Same definition as bit 16 (P0P), except this bit is for Port 2.
17	0h	RO/V	**Port 1 Present (P1P)** Same definition as bit 16 (P0P), except this bit is for Port 1.
16	0h	RO/V	**Port 0 Present (P0P)** This bit is set when COMINIT is received as a response to COMRESET. 0 = No device detected. 1 = The presence of a device on Port 0 has been detected. The status of this bit may change at any time. This bit is cleared when the port is disabled using P0E. This bit is not cleared upon surprise removal of a device.
15:3	-	-	**Reserved**
2	0h	RW/V	**Port 2 Enabled (P2E)** 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. Note: This bit takes precedence over P2CMD.SUD (offset ABAR+218h:bit 1). When MAP.SPD[2] is 1, this is reserved and is read-only 0.
1	0h	RW/V	**Port 1 Enabled (P1E)** 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. Note: This bit takes precedence over P1CMD.SUD (offset ABAR+198h:bit 1). When MAP.SPD[1] is 1, this is reserved and is read-only 0.

Bit Range	Default	Access	Field Name and Description
0	0h	RW/V	**Port 0 Enabled (P0E)** 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. Note: This bit takes precedence over P0CMD.SUD (offset ABAR+118h:bit 1). When MAP.SPD[0] is 1, this is reserved and is read-only 0.

SATA General Configuration (SATAGC) – Offset 9c

SATA General Configuration

Bit Range	Default	Access	Field Name and Description
31	0h	RW/O	**Register Lock (REGLOCK)** 0 = Will not lock CAP.CP, PID.NEXT, MID.NEXT, or SATACR0.NEXT 1 = Setting this bit will lock CAP.CP, PID.NEXT, MID.NEXT, and SATACR0.NEXT. Once locked, these register bits will become RO. BIOS is requested to program this field to '1' prior to OS handoff. Note: This field is not reset by FLR.
30:16	-	-	**Reserved**
15	0h	RW	**Data Phase Parity Error Enable (DPPEE)** When '1', IOSF data phase parity error handling is enabled. When '0', the data phase parity error handling is disabled. Note: This field is not reset by FLR.

Bit Range	Default	Access	Field Name and Description
14:12	0h	RW	**Write Request_Size Select/Max_Payload_Size (WRRSELMPS)** These two bits select the max write request size that SATA host controller will initiate for DMA write to memory. SATA host controller will internally break up larger write request based on these bits. The request is address-aligned to the selected size. Defined encodings for this field are: 000b = 128 address aligned bytes max payload size 111b = 64 address aligned bytes max payload size. All other values are reserved for SATA host controller. Note: This field is not reset by FLR (not supported).
11	0h	RW	**Command Parity Error Enable (CPEE)** When '1', command parity error handing is enable. When '0' the command parity error handling is disabled. Note: This field is not reset by FLR.
10	0h	RW	**SATA Controller Function Disable (SCFD)** BIOS program this bit to 1 to disable the SATA Controller function. When 0, SATA Controller function is enabled. When disable, SATA Host Controller will not claimed the register access targeting its Configuration Space. In IOSF primary Fabric Decode scheme, it's expected BIOS also program the corresponding bit used by the Fabric Decoder accordingly hence both SATA SIP and Fabric Decoder are in sync, and BIOS need to program this bit before programming the one in Fabric Decoder. Once this bit is set, BIOS isnot able to revert it back to Function Enable until next round of platform reset. This register field is not reset by FLR.
9	0h	RW	**Unsupported Request Reporting Enable (URRE)** If set to 1 by software, it allows reporting of an Unsupported Request as a system error. If both URRE and PCI configuration SERR# Enable registers are set to a 1, then the agent must set the Signaled System Error bit in the PCI Status register and send a DO_SERR message in IOSF-SB interface.

Bit Range	Default	Access	Field Name and Description
8	0h	RW/1C/V	**Unsupported Request Detected (URD)** Set to 1 by hardware upon detecting an Unsupported Request on IOSF Primary interface that is not considered Advisory Non-Fatal. Cleared to 0 by SW. URD bit is only set based on IOSF primary bus interface activity. Its not set based on IOSF sideband bus interface activity.
7	0h	RW/O	**Alternate ID Enable (AIE)** 0 = Clearing this bit when in RAID mode, the SATA Controller located at Device 23: Function 0 will report its In-box Compatibility ID. Refer to the Device and Revision ID Table in Vol1 for more info. Clearing this bit is required for the Intel® Rapid Storage Technology driver (including the Microsoft* Windows* operating system in-box version of the driver) to load on the platform. 1 = Setting this bit when in RAID mode, the SATA Controller located at Device 23:Function 0 will report its Device ID other than the In-box Compatibility ID as documented in the Device and Revision ID Table in Vol1. During the Microsoft* Windows* OS installation, the user will be required to “load” (formerly done by pressing the F6 button on the keyboard) the appropriate RAID storage driver that is enabled by this setting. Note: BIOS is recommended to program this bit prior to programming the MAP.SMS field to reflect RAID. This field is reset by PLTRST# and BIOS is required to reprogram the value (either 0 or 1) after resuming from S3, S4 or S5. This insures that the value is properly and cannot be changed during runtime. Note: This field is not reset by FLR (not supported).

Bit Range	Default	Access	Field Name and Description
6	0h	RW/O/V	**AIE0 DevID Selection (DEVIDSEL)** This register allows BIOS to select Device ID when AIE=0. This bit only has effect in Desktop / Server SKU. In Mobile SKU this bit has no effect at all. Refer to config register offset 09h PI for usage. 0 : 2822h 1 : 2826h Note: Server BIOS is required to program this field to 1 together with the write to the AIE bit in a single configuration write cycle. Client BIOS is required to program this bit to 0 together with the write to the AIE bit in a single configuration write cycle. Note: This field is not reset by FLR.
5	0h	RW/O	**FLR Capability Selection (FLRCSSEL)** This allows the FLR Capability to be bypassed. Refer to config offset B0h. BIOS is required to program this bit to 1 and config offset A8h SATACR0.NEXT to 00h. Note: This field is not reset by FLR.

Bit Range	Default	Access	Field Name and Description
4:3	0h	RW/O	**MXTBA Size Select (MSS)** These 2 bits select the size of the Memory space for the MSI-X Table defined in BAR 0 (Configuration space offset 10h). MSS[1:0] MSI-X Table Memory space size 00 32K 01 16K 10 8K 11 Reserved Note: This field is not reset by FLR (not supported).
2:0	0h	RW/O	**ABAR Size Select (ASSEL)** These 3 bits select the size of the Memory space for the ABAR in BAR 5 (Configuration space offset 24h). ASSEL[2:0] ABAR Memory space size 000 2K 001 16K 010 32K 011 64K 100 128K 101 256K 110 512K 111 Reserved Note: This field is not reset by FLR (not supported).

SATA Initialization Register Index (SIRI) – Offset a0

SATA Initialization Register Index

Bit Range	Default	Access	Field Name and Description
7:2	00h	RW	**Index (IDX)** 6-bit index pointer into the 256-byte space. Data is written into the SIRD (DFTD) register and read from the SIRD register. This point to a DWord register. The byte enables on the SIRD register affect what will be written.
1:0	-	-	**Reserved**

SATA Initialization Register Data (SIRD) – Offset a4

SATA Initialization Register Data

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW/V	**Data (DTA)** 32-bit data value that is written to the register pointed to by SIRI, or read from the register pointed to by SIRI.

Serial ATA Capability Register 0 (SATACR0) – Offset a8

The SATACR0.NEXT is not changed from RO to become RWO because there is an existing method (SATAGC.FLRCSSEL bit) to bypass the FLR Capability structure, and since the FLR Capability ID.NEXT is already indicating end of capability structure, it does not need change to be RWO.

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:20	1h	RO	**Major Revision (MAJREV)** Major revision number of the SATA Capability Pointer implemented.

Bit Range	Default	Access	Field Name and Description
19:16	0h	RO	**Minor Revision (MINREV)** Minor revision number of the SATA Capability Pointer implemented.
15:8	00h	RW/L	**Next Capability Pointer (NEXT)** 00h indicating the final item in the Capability List. The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR.
7:0	12h	RO	**Capability ID (CAP)** The value of 12h has been assigned by the PCI SIG to designate the SATA Capability pointer.

Serial ATA Capability Register 1 (SATACR1) – Offset ac

Serial ATA Capability Register 1

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:4	004h	RO	**BAR Offset (BAROFST)** Indicates the offset into the BAR where the Index/Data pair are located (in DWord granularity). The Index and Data I/O registers are located at offset 10h within the I/O space defined by LBAR. A value of 004h indicates offset 10h. 000h = 0h offset 001h = 4h offset 002h = 8h offset 003h = Bh offset 004h = 10h offset ... FFFh = 3FFFh offset (maximum 16KB)

Bit Range	Default	Access	Field Name and Description
3:0	8h	RO	**BAR Location (BARLOC)** Indicates the absolute PCI Configuration register address of the BAR containing the Index/Data pair (in DWord granularity). The Index and Data I/O registers reside within the space defined by LBAR in the SATA controller. A value of 8h indicates offset 20h, which is LBAR. 0000 - 0011b = reserved 0100b = 10h => BAR0 0101b = 14h => BAR1 0110b = 18h => BAR2 0111b = 1Ch => BAR3 1000b = 20h => LBAR 1001b = 24h => BAR5 1010–1110b = reserved 1111b = Index/Data pair in PCI Configuration space. This is not supported in the PCH.

Scratch Pad (SP) – Offset c0

Scratch Pad

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Data (DT)** This is a read/write register that is available for software to use. No hardware action is taken on this register.

MSI-X Identifiers (MXID) – Offset d0

MSI-X Identifiers

Bit Range	Default	Access	Field Name and Description
15:8	0h	RW/L	**Next Pointer (NEXT)** Indicates the next item in the list. This may be other capability pointers or it may be the last item in the list.The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR.
7:0	11h	RO	**Capability ID (CID)** Capabilities ID indicates this is an MSI-X capability.

MSI-X Message Control (MXC) – Offset d2

MSI-X Message Control

Bit Range	Default	Access	Field Name and Description
15	0h	RW	**MSI-X Enable (MXE)** If set to '1' and the MSI Enable bit in the MSI Message Control register is cleared to '0', the function is permitted to use MSI-X to request service and is prohibited from using its INTx# pin (if implemented). If cleared to '0', the function is prohibited from using MSI-X to request service.
14	0h	RW	**Function Mask (FM)** If set to '1', all of the vectors associated with the function are masked, regardless of their per vector Mask bit states. If cleared to '0', each vector's Mask bit determines whether the vector is masked or not. Setting or clearing the MSI-X Function Mask bit has no effect on the state of the per vector Mask bits.
13:11	-	-	**Reserved**
10:0	0h	RO	**Table Size (TS)** This value indicates the size of the MSI-X Table as the value n, which is encoded as n - 1. For example, a returned value of 3h corresponds to a table size of 4..

MSI-X Table Offset / Table BIR (MXT) – Offset d4

MSI-X Table Offset / Table BIR

Bit Range	Default	Access	Field Name and Description
31:3	0h	RW/O	**Table Offset (TO)** Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X Table. The lower three Table BIR bits are masked off (cleared to 000b) by system software to form a 32-bit Qword-aligned offset.
2:0	0h	RO	**Table BIR (TBIR)** This field indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X Table into system memory. A read-only value of '0' means 10h.

MSI-X PBA Offset / PBA BIR (MXP) – Offset d8

MSI-X PBA Offset / PBA BIR

Bit Range	Default	Access	Field Name and Description
31:3	0h	RW/O	**PBA Offset (PBAO)** Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X PBA. The lower three PBA BIR bits are masked off (cleared to 000b) by software to form a 32-bit Qword-aligned offset.
2:0	1h	RO	**PBA BIR (PBIR)** This field indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X PBA into system memory. A read-only value of '1' means 14h.

BIST FIS Control/Status (BFCS) – Offset e0

BIST FIS Control/Status

Bit Range	Default	Access	Field Name and Description
30:13	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
12	0h	RW	**Port 2 BIST FIS Initiate (P2BFI)** When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 2,using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 2 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PCS.P2E prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P2BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully. Note: Bit may be Reserved depending on if port is available in the given SKU. See EDS Vol1 Section 1 for details if port is available.
11	0h	RW/1C/V	**BIST FIS Successful (BFS)** 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a BIST FIS transmitted by PCH receives an R_OK completion status from the device. Note: This bit must be cleared by software prior to initiating a BIST FIS.
10	0h	RW/1C/V	**BIST FIS Failed (BFF)** 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a BIST FIS transmitted by PCH receives an R_ERR completion status from the device. Note: This bit must be cleared by software prior to initiating a BIST FIS.

Bit Range	Default	Access	Field Name and Description
9	0h	RW	**Port 1 BIST FIS Initiate (P1BFI)** When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 1,using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 1 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PCS.P1E prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P1BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully.
8	0h	RW	**Port 0 BIST FIS Initiate (P0BFI)** When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 0,using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 0 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PCS.P0E prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P0BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully.
7:2	0h	RW	**BIST FIS Parameters (BFP)** These 6 bits form the contents of the upper 6 bits of the BIST FIS Pattern Definition in any BIST FIS transmitted by the PCH. This field is not port specific—its contents will be used for any BIST FIS initiated on port 0, port 1, port 2, or port 3. The specific bit definitions are: Bit 7: T – Far End Transmit mode Bit 6: A – Align Bypass mode Bit 5: S – Bypass Scrambling Bit 4: L – Far End Retimed Loopback Bit 3: F – Far End Analog Loopback Bit 2: P – Primitive bit for use with Transmit mode
1:0	-	-	**Reserved**

BIST FIS Transmit Data 1 (BFTD1) – Offset e4

BIST FIS Transmit Data 1

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Data (DATA)** The data programmed into this register will form the contents of the second DW of any BIST FIS initiated by the SATA controller. This register is not port specific - its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the T bit of the BIST FIS is set to indicate Far-End Transmit mode, this register's contents will be transmitted as the BIST FIS 2nd DW regardless of whether or not the T bit is indicated in the BFCS register.

BIST FIS Transmit Data 2 (BFTD2) – Offset e8

BIST FIS Transmit Data 2

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**Data (DATA)** The data programmed into this register will form the contents of the third DW of any BIST FIS initiated by the SATA controller. This register is not port specific - its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the T bit of the BIST FIS is set to indicate Far-End Transmit mode, this register's contents will be transmitted as the BIST FIS 3rd DW regardless of whether or not the T bit is set in the BFCS register.

SATA Initialization (SIR) Index Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
80h	4	Squelch Circuit Disable (PTM1)	0h
8ch	4	SATA Dynamic Clock Gating Enable (PTM4)	0h
90h	4	SATA MPHY Dynamic Power Gating Enable (PTM5)	0h

Squelch Circuit Disable (PTM1) – Offset 80

Bit Range	Default	Access	Field Name and Description
30:19	-	-	**Reserved**
18	0h	RW	**Port 2 Squelch Circuit Disable (P2SQOFFIDLED)** Same as bit 16, except this is for port 2.
17	0h	RW	**Port 1 Squelch Circuit Disable (P1SQOFFIDLED)** Same as bit 16, except this is for port 1.
16	0h	RW	**Port 0 Squelch Circuit Disable (P0SQOFFIDLED)** When this bit is set to 1, port 0 Squelch Circuit is disabled with interface in Slumber state and no AHCI command outstanding. This feature is only applicable if GHC.AE=1. With the squelch circuit disabled, device initiated wake from Slumber is not supported. BIOS may enable this feature if the DEVSLP feature is not supported on this port. This feature shall be mutually exclusive with the DEVSLP feature.
15:0	-	-	**Reserved**

SATA Dynamic Clock Gating Enable (PTM4) – Offset 8c

BIOS may need to program this register.

SATA MPHY Dynamic Power Gating Enable (PTM5) – Offset 90

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**
2	0h	RW	**SATA mphy Dynamic Power Gating Enable for Port 2 (PHYDPGEP2)** Same definition as bit 0, except this is for Port 2.
1	0h	RW	**SATA MPHY Dynamic Power Gating Enable for Port 1 (PHYDPGEP1)** Same definition as bit 0, except this is for Port 1.

Bit Range	Default	Access	Field Name and Description
0	0h	RW	**SATA MPHY Dynamic Power Gating Enable for Port 0 (PHYDPGEP0)** 0 = SATA host controller does not perform dynamic MPhy power gating. 1 = SATA host controller supports MPhy dynamic power gating. For platforms with only internal SSDs or HDDs, set the bit to enable SATAMPhy dynamic power gating flow. Use the default value of 0 if the platform has one ormore of the following: - SATA hot-plug enabled port (PxCMD.HPCP = 1) - SATA external port (PxCMD.ESP = 1) - SATA slimline port with zero-power ODD (ZPODD) attached (or other AN capableODD) Note: BIOS is requested to program this field to 1 if the system supports MPhydynamic power gating for SATA port 0 and SATA port 0 does not require Listen Modeusage. BIOS shall program this field to 1 until after BIOS has enumerated the SATAdevice of this port.

SATA MXPBA Registers

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	MSI-X Pending Bit Array QW 0 (MXPQW0_DW0)	0h

MSI-X Pending Bit Array QW 0 (MXPQW0_DW0) – Offset 0

MSI-X Pending Bit Array QW 0

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	00h	RO/V	**MSI-X vector Pending (MXVP)** For each Pending Bit that is set, the function has a pending message for the associated MSI-X Table entry. Pending bits that have no associated MSI-X Table entry are reserved. After reset, the state of reserved Pending bits must be 0. Software should never write, and should only read Pending Bits. If software writes to Pending Bits, the result is undefined. Each Pending Bit's state after reset is 0 (no message pending).

SATA MXTBA Registers

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	MSI-X Table Entries 0 Message Lower Address (MXTE0MLA)	0h
4h	4	MSI-X Table Entries 0 Message Upper Address (MXTE0MUA)	0h
8h	4	MSI-X Table Entries 0 Message Data (MXTE0MD)	0h
ch	4	MSI-X Table Entries 0 Vector Control (MXTE0VC)	1h
10h	4	MSI-X Table Entries 0 Message Lower Address (MXTE1MLA)	0h
14h	4	MSI-X Table Entries 0 Message Upper Address (MXTE1MUA)	0h
18h	4	MSI-X Table Entries 0 Message Data (MXTE1MD)	0h
1ch	4	MSI-X Table Entries 0 Vector Control (MXTE1VC)	1h
20h	4	MSI-X Table Entries 0 Message Lower Address (MXTE2MLA)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
24h	4	MSI-X Table Entries 0 Message Upper Address (MXTE2MUA)	0h
28h	4	MSI-X Table Entries 0 Message Data (MXTE2MD)	0h
2ch	4	MSI-X Table Entries 0 Vector Control (MXTE2VC)	1h
30h	4	MSI-X Table Entries 0 Message Lower Address (MXTE3MLA)	0h
34h	4	MSI-X Table Entries 0 Message Upper Address (MXTE3MUA)	0h
38h	4	MSI-X Table Entries 0 Message Data (MXTE3MD)	0h
3ch	4	MSI-X Table Entries 0 Vector Control (MXTE3VC)	1h
40h	4	MSI-X Table Entries 0 Message Lower Address (MXTE4MLA)	0h
44h	4	MSI-X Table Entries 0 Message Upper Address (MXTE4MUA)	0h
48h	4	MSI-X Table Entries 0 Message Data (MXTE4MD)	0h
4ch	4	MSI-X Table Entries 0 Vector Control (MXTE4VC)	1h
50h	4	MSI-X Table Entries 0 Message Lower Address (MXTE5MLA)	0h
54h	4	MSI-X Table Entries 0 Message Upper Address (MXTE5MUA)	0h
58h	4	MSI-X Table Entries 0 Message Data (MXTE5MD)	0h
5ch	4	MSI-X Table Entries 0 Vector Control (MXTE5VC)	1h
60h	4	MSI-X Table Entries 0 Message Lower Address (MXTE6MLA)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
64h	4	MSI-X Table Entries 0 Message Upper Address (MXTE6MUA)	0h
68h	4	MSI-X Table Entries 0 Message Data (MXTE6MD)	0h
6ch	4	MSI-X Table Entries 0 Vector Control (MXTE6VC)	1h
70h	4	MSI-X Table Entries 0 Message Lower Address (MXTE7MLA)	0h
74h	4	MSI-X Table Entries 0 Message Upper Address (MXTE7MUA)	0h
78h	4	MSI-X Table Entries 0 Message Data (MXTE7MD)	0h
7ch	4	MSI-X Table Entries 0 Vector Control (MXTE7VC)	1h

MSI-X Table Entries 0 Message Lower Address (MXTE0MLA) – Offset 0

MSI-X Table Entries 0 Message Lower Address

Bit Range	Default	Access	Field Name and Description
31:2	0h	RW	**MSI-X message lower address (MXMLA)** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	-	-	**Reserved**

MSI-X Table Entries 0 Message Upper Address (MXTE0MUA) – Offset 4

MSI-X Table Entries 0 Message Upper Address

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**MSI-X message upper 32-bit address (MXMUA)** Specifies the upper 32-bit of the MSI-X Message.

MSI-X Table Entries 0 Message Data (MXTE0MD) – Offset 8

MSI-X Table Entries 0 Message Data

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**MSI-X message Data (MXMD)** Specifies the 32-bit Data of the MSI-X Message.

MSI-X Table Entries 0 Vector Control (MXTE0VC) – Offset c

MSI-X Table Entries 0 Vector Control

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	1h	RW	**MSI-X vector Mask (MXVM)** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

MSI-X Table Entries 0 Message Lower Address (MXTE1MLA) – Offset 10

MSI-X Table Entries 0 Message Lower Address

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:2	0h	RW	**MSI-X message lower address (MXMLA)** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	-	-	**Reserved**

MSI-X Table Entries 0 Message Upper Address (MXTE1MUA) – Offset 14

MSI-X Table Entries 0 Message Upper Address

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**MSI-X message upper 32-bit address (MXMUA)** Specifies the upper 32-bit of the MSI-X Message

MSI-X Table Entries 0 Message Data (MXTE1MD) – Offset 18

MSI-X Table Entries 0 Message Data

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**MSI-X message Data (MXMD)** Specifies the 32-bit Data of the MSI-X Message.

MSI-X Table Entries 0 Vector Control (MXTE1VC) – Offset 1c

MSI-X Table Entries 0 Vector Control

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	1h	RW	**MSI-X vector Mask (MXVM)** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

MSI-X Table Entries 0 Message Lower Address (MXTE2MLA) – Offset 20

MSI-X Table Entries 0 Message Lower Address

Bit Range	Default	Access	Field Name and Description
31:2	0h	RW	**MSI-X message lower address (MXMLA)** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	-	-	**Reserved**

MSI-X Table Entries 0 Message Upper Address (MXTE2MUA) – Offset 24

MSI-X Table Entries 0 Message Upper Address

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**MSI-X message upper 32-bit address (MXMUA)** Specifies the upper 32-bit of the MSI-X Message

MSI-X Table Entries 0 Message Data (MXTE2MD) – Offset 28

MSI-X Table Entries 0 Message Data

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**MSI-X message Data (MXMD)** Specifies the 32-bit Data of the MSI-X Message.

MSI-X Table Entries 0 Vector Control (MXTE2VC) – Offset 2c

MSI-X Table Entries 0 Vector Control

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	1h	RW	**MSI-X vector Mask (MXVM)** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

MSI-X Table Entries 0 Message Lower Address (MXTE3MLA) – Offset 30

MSI-X Table Entries 0 Message Lower Address

Bit Range	Default	Access	Field Name and Description
31:2	0h	RW	**MSI-X message lower address (MXMLA)** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	-	-	**Reserved**

MSI-X Table Entries 0 Message Upper Address (MXTE3MUA) – Offset 34

MSI-X Table Entries 0 Message Upper Address

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**MSI-X message upper 32-bit address (MXMUA)** Specifies the upper 32-bit of the MSI-X Message

MSI-X Table Entries 0 Message Data (MXTE3MD) – Offset 38

MSI-X Table Entries 0 Message Data

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**MSI-X message Data (MXMD)** Specifies the 32-bit Data of the MSI-X Message.

MSI-X Table Entries 0 Vector Control (MXTE3VC) – Offset 3c

MSI-X Table Entries 0 Vector Control

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	1h	RW	**MSI-X vector Mask (MXVM)** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

MSI-X Table Entries 0 Message Lower Address (MXTE4MLA) – Offset 40

MSI-X Table Entries 0 Message Lower Address

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:2	0h	RW	**MSI-X message lower address (MXMLA)** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	-	-	**Reserved**

MSI-X Table Entries 0 Message Upper Address (MXTE4MUA) – Offset 44

MSI-X Table Entries 0 Message Upper Address

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**MSI-X message upper 32-bit address (MXMUA)** Specifies the upper 32-bit of the MSI-X Message

MSI-X Table Entries 0 Message Data (MXTE4MD) – Offset 48

MSI-X Table Entries 0 Message Data

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**MSI-X message Data (MXMD)** Specifies the 32-bit Data of the MSI-X Message.

MSI-X Table Entries 0 Vector Control (MXTE4VC) – Offset 4c

MSI-X Table Entries 0 Vector Control

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	1h	RW	**MSI-X vector Mask (MXVM)** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

MSI-X Table Entries 0 Message Lower Address (MXTE5MLA) – Offset 50

MSI-X Table Entries 0 Message Lower Address

Bit Range	Default	Access	Field Name and Description
31:2	0h	RW	**MSI-X message lower address (MXMLA)** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	-	-	**Reserved**

MSI-X Table Entries 0 Message Upper Address (MXTE5MUA) – Offset 54

MSI-X Table Entries 0 Message Upper Address

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**MSI-X message upper 32-bit address (MXMUA)** Specifies the upper 32-bit of the MSI-X Message

MSI-X Table Entries 0 Message Data (MXTE5MD) – Offset 58

MSI-X Table Entries 0 Message Data

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**MSI-X message Data (MXMD)** Specifies the 32-bit Data of the MSI-X Message.

MSI-X Table Entries 0 Vector Control (MXTE5VC) – Offset 5c

MSI-X Table Entries 0 Vector Control

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	1h	RW	**MSI-X vector Mask (MXVM)** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

MSI-X Table Entries 0 Message Lower Address (MXTE6MLA) – Offset 60

MSI-X Table Entries 0 Message Lower Address

Bit Range	Default	Access	Field Name and Description
31:2	0h	RW	**MSI-X message lower address (MXMLA)** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	-	-	**Reserved**

MSI-X Table Entries 0 Message Upper Address (MXTE6MUA) – Offset 64

MSI-X Table Entries 0 Message Upper Address

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**MSI-X message upper 32-bit address (MXMUA)** Specifies the upper 32-bit of the MSI-X Message

MSI-X Table Entries 0 Message Data (MXTE6MD) – Offset 68

MSI-X Table Entries 0 Message Data

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**MSI-X message Data (MXMD)** Specifies the 32-bit Data of the MSI-X Message.

MSI-X Table Entries 0 Vector Control (MXTE6VC) – Offset 6c

MSI-X Table Entries 0 Vector Control

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	1h	RW	**MSI-X vector Mask (MXVM)** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

MSI-X Table Entries 0 Message Lower Address (MXTE7MLA) – Offset 70

MSI-X Table Entries 0 Message Lower Address

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:2	0h	RW	**MSI-X message lower address (MXMLA)** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	-	-	**Reserved**

MSI-X Table Entries 0 Message Upper Address (MXTE7MUA) – Offset 74

MSI-X Table Entries 0 Message Upper Address

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**MSI-X message upper 32-bit address (MXMUA)** Specifies the upper 32-bit of the MSI-X Message

MSI-X Table Entries 0 Message Data (MXTE7MD) – Offset 78

MSI-X Table Entries 0 Message Data

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**MSI-X message Data (MXMD)** Specifies the 32-bit Data of the MSI-X Message.

MSI-X Table Entries 0 Vector Control (MXTE7VC) – Offset 7c

MSI-X Table Entries 0 Vector Control

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	1h	RW	**MSI-X vector Mask (MXVM)** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

SDXC (SD Card) PCR Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
600h	4	Dynamic Clock Gating Control (GPPRVRW1)	0h

Dynamic Clock Gating Control (GPPRVRW1) – Offset 600

Bit Range	Default	Access	Field Name and Description
30:11	-	-	**Reserved**
10	0h	RW	**SD Card Functional Clock Gating Enable (sdcard_func)** 1 = Enabed 0 = Disabled
9	0h	RW	**SD Card Synchronous Clock Gating Enable (sdcard_ocp)** 1 = Enabled 0 = Disabled
8:0	-	-	**Reserved**

SDXC Additional Memory Mapped Registers

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
804h	2	Software LTR Value (SW_LTR_val)	800h
808h	2	Auto LTR Value (Auto_LTR_val)	800h
810h	4	Capabilities Bypass Control (Cap_byps)	0h
814h	4	Capabilities Bypass Register I (Cap_byps_reg1)	1040E55Ch
818h	4	Capabilities Bypass Register II (Cap_byps_reg2)	40000C8h
81ch	4	Device Idle D0i3 (reg_D0i3)	8h
820h	4	Tx CMD Delay Control (Tx_CMD_dly)	400h
824h	4	Tx Delay Control 1 (Tx_DATA_dly_1)	A18h
828h	4	Tx Delay Control 2 (Tx_DATA_dly_2)	1C1C1C00h
82ch	4	Rx CMD Data Delay Control 1 (Rx_CMD_Data_dly_1)	1C1C1C00h
834h	4	Rx CMD Data Path Delay Control 2 (Rx_CMD_Data_dly_2)	181Ch
838h	4	Master DLL Software Control (Master_Dll)	1h
840h	4	Auto Tuning Value (Auto_tuning)	0h

Software LTR Value (SW_LTR_val) – Offset 804

Bit Range	Default	Access	Field Name and Description
15	0h	RW	**Snoop Requirment (Snoop_Requirment)** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.

Bit Range	Default	Access	Field Name and Description
14:13	-	-	**Reserved**
12:10	2h	RW	**Snoop Latency Scale (Snoop_latency_scale)** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -) 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	000h	RW	**Snoop Value (Snoop_value)** 10-bit latency value

Auto LTR Value (Auto_LTR_val) – Offset 808

Bit Range	Default	Access	Field Name and Description
15	0h	RW	**Snoop Requirment (Snoop_Requirment)** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	-	-	**Reserved**
12:10	2h	RW	**Snoop Latency Scale (Snoop_latency_scale)** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -) 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	000h	RW	**Snoop Value (Snoop_value)** 10-bit latency value

Capabilities Bypass Control (Cap_byps) – Offset 810

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8:0	000h	RW	**Enable Capabilities Bypass (Enable_Cap_Bypass)** 5Ah – Enable Capabilities Bypass All other – Capabilities Bypass Disable (using default values)

Capabilities Bypass Register I (Cap_byps_reg1) – Offset 814

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**
28	1h	RW	**Timeout Clock Unit (timeout_clock_unit)** 1'b1 to Select MHz Clock1'b0 to Select KHz Clock
27:22	01h	RW	**Timeout Clock Frequency (timeout_clock_freq)**
21	0h	RW	**SPI Mode Support (SPI_mode_support)** 1'b1 – SPI Mode Supported 1'b0 – SPI Mode Not Supported
20:17	0h	RW	**Timer Count for Re-Tuning (timer_count)** This is the Timer Count for Re-Tuning Timer for Re-TuningMode 1 to 3. Setting to 4'b0 disables Re-Tuning Timer
16	0h	RW	**Use Tuning for SDR50 (tuning_for_SDR50)** 1'b1 – Use Tuning 1'b0 – Don't use Tuning

Bit Range	Default	Access	Field Name and Description
15	1h	RW	**DDR50 Support (ddr50_support)** 1'b1 – DDR50 Mode Supported 1'b0 – DDR50 Mode NOT Supported
14	1h	RW	**SDR104 Support (sdr104_support)** 1'b1 – SDR104 Mode Supported 1'b0 – SDR104 Mode NOT Supported
13	1h	RW	**SDR50 Support (sdr50_support)** 1'b1 – SDR50 Mode Supported 1'b0 – SDR50 Mode NOT Supported
12:11	0h	RW	**Slot Type (Slot_Type)** 00 - Removable SD Card Slot 01 - Embedded Slot for One Device 10 - Shared Bus Slot 11 - Reserved
10	1h	RW	**Asynchronous Interrupt Support (Asynchronus_Interrupt_Support)** 1'b1 – Asynchronous Interrupt Supported 1'b0 – Asynchronous Interrupt NOT Supported
9	-	-	**Reserved**
8	1h	RW	**Voltage Support 1.8V (Voltage_Support_1_8V)** 1'b1 – 1.8V Supported 1'b0 – 1.8V NOT Supported
7	0h	RW	**Voltage Support 3.0V (Voltage_Support_3V)** 1'b1 – 3.0V Supported 1'b0 – 3.0V NOT Supported

Bit Range	Default	Access	Field Name and Description
6	1h	RW	**Voltage Support 3.3V (Voltage_Support_3_3V)** 1'b1 – 3.3V Supported 1'b0 – 3.3V NOT Supported
5	0h	RW	**Suspend/Resume Support (Suspend_Resume_Support)** 1'b1 – Suspend/Resume Supported 1'b0 – Suspend/Resume NOT Supported
4	1h	RW	**SDMA Support (SDMA_Support)** 1'b1 – SDMA Mode Supported 1'b0 – SDMA Mode NOT Supported
3	1h	RW	**High Speed Support (High_Speed_support)** 1'b1 – High Speed Mode Supported 1'b0 – High Speed Mode NOT Supported
2	1h	RW	**ADMA2 Support (ADMA2_Support)** 1'b1 – ADMA2 Mode Supported 1'b0 – ADAM2 Mode NOT Supported
1:0	0h	RW	**Max Burst Length (Max_Burst_Length)** Maximum Block Length supported by the Core/Device 00: 512 (Bytes) 01: 1024 10: 2048 11: Reserved

Capabilities Bypass Register II (Cap_byps_reg2) – Offset 818

Bit Range	Default	Access	Field Name and Description
30:27	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
26:21	20h	RW	**Tuning Count Value (tuning_count_val)** Configures the Number of Taps (Phases) of the rxclk_in that is supported. The Tuning State machine uses this information toselect one of the Taps (Phases) of the rxclk_in during the Tuning Procedure
20	0h	RW	**Tuning Disable (tuning_dis)** Disable the 1.5x Tuning count when calculatingtotal tuning count.
19	-	-	**Reserved**
18	0h	RW	**Driver Type D Support (driver_type_D)** 1'b1 – Supported 1'b0 – NOT Supported
17	0h	RW	**Driver Type C Support (driver_type_C)** 1'b1 – Supported 1'b0 – NOT Supported
16	0h	RW	**Driver Type A Support (driver_type_A)** 1'b1 – Supported 1'b0 – NOT Supported
15	-	-	**Reserved**
14	0h	RW	**8-bit Support for Embedded Device (support_8_bit_embedded)** 1'b1 – Supported1'b0 – NOT Supported
13:8	-	-	**Reserved**
7:0	C8h	RW	**Base Clock Frequency for SD Clock (base_sd_clock)**

Device Idle D0i3 (reg_D0i3) – Offset 81c

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4	0h	RO	**Interrupt Request Capable (Interrupt_Request_Capable)** 0 – HW not capable to issue in interrupt on command completion 1 – HW capable to issue an interrupt on command completion
3	1h	RW/1C	**Restore Required (RestoreRequired)** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a '1'. This bit will be set on initial power up.
2	0h	RW	**D0i3 (D0i3)** SW sets this bit to '1' to move the IP into the D0i3 state. Writing this bit to '0' will return the IP to the fully active D0 state (D0i0).
1	-	-	**Reserved**
0	0h	RO	**Command-In-Progress (Cmd_In_Progress)** HW sets this bit on a 1->0 or 0->1 transition of bit [2]. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit. If Interrupt Request bit [1] was set for the current command, HW may clear this bit before the interrupt has been made visible to SW.

Tx CMD Delay Control (Tx_CMD_dly) – Offset 820

Bit Range	Default	Access	Field Name and Description
30:15	-	-	**Reserved**
14:8	04h	RW	**Tx CMD Delay (DDR Mode) (ddr_mode)** 0-39 - Select the required delay, as a multiple of 125pSec.40 – 127 – Reserved
7	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
6:0	00h	RW	**Tx CMD Delay (SDR Mode) (sdr_mode)** 0-39 - Select the required delay, as a multiple of 125pSec. 40 – 127 – Reserved

Tx Delay Control 1 (Tx_DATA_dly_1) – Offset 824

Bit Range	Default	Access	Field Name and Description
30:15	-	-	**Reserved**
14:8	0Ah	RW	**Tx Data Delay (HS400 Mode) (hs400_mode)** 0-79 - Select the required delay, as a multiple of 125pSec.80 – 127 – Reserved
7	-	-	**Reserved**
6:0	18h	RW	**Tx Data Delay (SDR104/HS200 Mode) (sdr104_hs200_mode)** 0-79 - Select the required delay, as a multiple of 125pSec. 80 – 127 – Reserved

Tx Delay Control 2 (Tx_DATA_dly_2) – Offset 828

Tx Delay Control 2 Register

Bit Range	Default	Access	Field Name and Description
30:24	1Ch	RW	**Tx Data Delay (SDR50 Mode) (sdr50_mode)** 0-79 - Select the required delay, as a multiple of 125pSec. 80 – 127 – Reserved
23	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
22:16	1Ch	RW	**Tx Data Delay (DDR50 Mode) (ddr50_mode)** 0-79 - Select the required delay, as a multiple of 125pSec. 80 – 127 – Reserved
15	-	-	**Reserved**
14:8	1Ch	RW	**Tx Data Delay (SDR25/HS50 Mode) (sdr25_hs50_mode)** 0-79 - Select the required delay, as a multiple of 125pSec. 80 – 127 – Reserved
7	-	-	**Reserved**
6:0	00h	RW	**Tx Data Delay (SDR12/Compatibility Mode) (sdr12_comp_mode)** 0-79 - Select the required delay, as a multiple of 125pSec. 80 – 127 – Reserved

Rx CMD Data Delay Control 1 (Rx_CMD_Data_dly_1) – Offset 82c

Bit Range	Default	Access	Field Name and Description
30:24	1Ch	RW	**Rx CMD + Data Delay (SDR50 Mode) (sdr100_mode)** 0-119 - Select the required delay, as a multiple of 125pSec. 120 – 127 – Reserved
23	-	-	**Reserved**
22:16	1Ch	RW	**Rx CMD + Data Delay (DDR50 Mode) (ddr50_mode)** 0-119 - Select the required delay, as a multiple of 125pSec. 120 – 127 – Reserved

Bit Range	Default	Access	Field Name and Description
15	-	-	**Reserved**
14:8	1Ch	RW	**Rx CMD + Data Delay (SDR25/HS50 Mode) (sdr50_hs50_mode)** 0-119 - Select the required delay, as a multiple of 125pSec. 120 – 127 – Reserved
7	-	-	**Reserved**
6:0	00h	RW	**Rx CMD + Data Delay (SDR12/Compatibility Mode) (sdr12_comp_mode)** 0-119 - Select the required delay, as a multiple of 125pSec. 120 – 127 – Reserved

Rx CMD Data Path Delay Control 2 (Rx_CMD_Data_dly_2) – Offset 834

Bit Range	Default	Access	Field Name and Description
30:18	-	-	**Reserved**
17:16	0h	RW	**Clock Source for Rx Path (clk_source)** 00 – Rx Clock after Output Buffer – all modes other than HS200/SDR104/HS400 to match delays. 01 – Rx Clock before Output Buffer – HS200/SDR104/HS400 modes to avoid reflections. 10 – Automatic Selection based on Working mode (HS 200 before buffer, all others after buffer) 11 – Reserved
15:14	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
13:8	18h	RW	**Rx Path PLL #3 Delay value For Auto Tuning Mode (path_pll)** 0-39 - Select the required delay, as a multiple of 125pSec. 40 – 63 – Reserved
7	-	-	**Reserved**
6:0	1Ch	RW	**Rx CMD + Data Delay (SDR104/HS200 Mode) (cmd_data_sdr104_hs200)** 0-119 - Select the required delay, as a multiple of 125pSec. 120 – 127 – Reserved

Master DLL Software Control (Master_Dll) – Offset 838

Bit Range	Default	Access	Field Name and Description
30:25	-	-	**Reserved**
24	0h	RW	**SW reset for Master DLL (SW_reset_dll)** 0 – No SW Reset for Master DLL 1 – Force Reset for Master DLL
23	0h	RO/V	**Master DLL Lock Indication (DLL_lock)**
22:2	-	-	**Reserved**
1	0h	RW	**Master DLL Software Ctrl (Master_DLL_Software_Ctrl)** 0 – Master DLL Automatic Control (SW Control Disabled) 1 – Master DLL Software Control Enabled
0	1h	RW	**Ctrl of Master DLL Ref Clock (Ctrl_of_Mst_DLL_Ref_Clk)** 0 - Clock is Disabled 1 - Clock is Enabled

Auto Tuning Value (Auto_tuning) – Offset 840

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4:0	00h	RO/V	**Auto Tuning Value (auto_tuning_val)** Auto Tuning Value found by host controller

SDXC Memory Mapped Registers

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	SDMA System Address (sdmasysaddr)	0h
4h	2	Block Size (blocksize)	0h
6h	2	Block Count (blockcount)	0h
8h	4	Argument1 (argument1)	0h
ch	2	Transfer Mode (transfermode)	0h
eh	2	Command (command)	0h
10h	4	Response [1-8] (response01)	0h
20h	4	Buffer Data Port (dataport)	0h
24h	4	Present State (presentstate)	1F00000h
28h	1	Host Control 1 (hostcontrol1)	0h
29h	1	Power Control (powercontrol)	0h
2ah	1	Block Gap Control (blockgapcontrol)	0h
2bh	1	Wakeup Control (wakeupcontrol)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
2ch	2	Clock Control (clockcontrol)	0h
2eh	1	Timeout Control (timeoutcontrol)	0h
2fh	1	Software Reset (softwarereset)	0h
30h	2	Normal Interrupt Status (normalintrsts)	0h
32h	2	Error Interrupt Status (errorintrsts)	0h
34h	2	Normal Interrupt Status Enable (normalintrstsena)	0h
36h	2	Error Interrupt Status Enable (errorintrstsena)	0h
38h	2	Normal Interrupt Signal Enable (normalintrsigena)	0h
3ah	2	Error Interrupt Signal Enable (errorintrsigena)	0h
3ch	2	Auto CMD12 Error Status (autocmderrsts)	0h
3eh	2	Host Control 2 (hostcontrol2)	0h
40h	8	Capabilities (capabilities)	73528C881h
48h	8	Maximum Current Capabilities (maxcurrentcap)	0h
50h	2	Force Event Register for AUTO CMD Error Status (ForceEventforAUTOCMDErrorStatus)	0h
52h	2	Force Event Register for Error Interrupt Status (forceeventforerrintsts)	0h
54h	1	ADMA Error Status (admaerrsts)	0h
58h	4	ADMA System Address Register 1 (admasysaddr01)	0h
5ch	2	ADMA System Address Register 2 (admasysaddr2)	0h
60h	2	Preset Value Register for Initialization (presetvalue0)	4h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
62h	2	Preset Value Register for Default Speed (presetvalue1)	0h
64h	2	Preset Value Register for High Speed (presetvalue2)	0h
66h	2	Preset Value Register for SDR12 (presetvalue3)	0h
68h	2	Preset Value Register for SDR25 (presetvalue4)	0h
6ah	2	Preset Value Register for SDR50 (presetvalue5)	0h
6ch	2	Preset Value Register for SDR104 (presetvalue6)	0h
6eh	2	Preset Value Register for DDR50 (presetvalue7)	0h
fch	2	Slot Interrupt Status (slotintrsts)	0h

SDMA System Address (sdmasysaddr) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**SDMA System Address / Argument 2 (sdma_sysaddress)** This register contains the physical system memory address used for DMA transfers or the second argument for the Auto CMD23. 1) SDMA System Address: This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. 2) Argument 2: This register is used with the Auto CMD23 to set a 32-bit block count value to the argument of the CMD23 while executing Auto CMD23.

Block Size (blocksize) – Offset 4

Bit Range	Default	Access	Field Name and Description
14:12	0h	RW	**Host DMA Buffer Size (sdma_bufboundary)** To perform long DMA transfer, System Address register shall be updated at every system boundary during DMA transfer. These bits specify the size of contiguous buffer in the system memory. The DMA transfer shall wait at the every boundary specified by these fields and the HC generates the DMA Interrupt to request the HD to update the System Address register.These bits shall support when the DMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. 000b - 4KB(Detects A11 Carry out) 001b - 8KB(Detects A12 Carry out) 010b - 16KB(Detects A13 Carry out) 011b - 32KB(Detects A14 Carry out) 100b - 64KB(Detects A15 Carry out) 101b -128KB(Detects A16 Carry out) 110b - 256KB(Detects A17 Carry out) 111b - 512KB(Detects A18 Carry out)
11:0	000h	RW	**Transfer Block Size (xfer_blocksize)** This register specifies the block size for block data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. It can be accessed only if no transaction is executing (i.e after a transaction has stopped). Read operations during transfer return an invalid value and write operations shall be ignored. 0000h - No Data Transfer 0001h - 1 Byte 0002h - 2 Bytes 0003h - 3 Bytes 0004h - 4 Bytes --- --- 01FFh - 511 Bytes 0200h - 512 Bytes --- --- 0800h - 2048 Bytes

Block Count (blockcount) – Offset 6

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW	**Block Count (block_cnt_16bit)** This register is enabled when Block Count Enable in the Transfer Mode register is set to 1 and is valid only for multiple block transfers. The HC decrements the block count after each block transfer and stops when the count reaches zero. It can be accessed only if no transaction is executing (i.e. after a transaction has stopped). Read operations during transfer return an invalid value and write operations shall be ignored.When saving transfer context as a result of Suspend command, the number of blocks yet to be transferred can be determined by reading this register. When restoring transfer context prior to issuing a Resume command, the HD shall restore the previously save block count. 0000h - Stop Count 0001h - 1 block 0002h - 2 blocks --- --- FFFFh - 65535 blocks

Argument1 (argument1) – Offset 8

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Argument 1 (command_argument1)** The SD Command Argument is specified as bit39-8 of Command-Format

Transfer Mode (transfermode) – Offset c

Bit Range	Default	Access	Field Name and Description
14:6	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
5	0h	RW	**Multi / Single Block Select (xfermode_multiblksel)** This bit enables multiple block data transfers. 0 - Single Block 1 - Multiple Block.
4	0h	RW	**Data Transfer Direction Select (xfermode_dataxferdir)** This bit defines the direction of data transfers.0 - Write (Host to Device) 1 - Read (Device to Host)
3:2	0h	RW	**Auto CMD Enable (xfermode_autocmdena)** This field determines use of auto command functions. 00b - Auto Command Disabled 01b - Auto CMD12 Enable 10b - Auto CMD23 Enable
1	0h	RW	**Block Count Enable (xfermode_blkcntena)** This bit is used to enable the Block count register, which is only relevant for multiple block transfers. When this bit is 0, the Block Count register is disabled, which is usefulin executing an infinite transfer. 0 - Disable 1 - Enable
0	0h	RW	**DMA Enable (xfermode_dmaenable)** DMA can be enabled only if DMA Support bit in theCapabilities register is set. If this bit is set to 1, a DMA operation shall begin when the HD writes to the upper byte of Command register (00Fh). 0 - Disable 1 - Enable

Command (command) – Offset e

Bit Range	Default	Access	Field Name and Description
14	-	-	**Reserved**
13:8	00h	RW	**Command Index (command_cmdindex)** This bit shall be set to the command number (CMD0-63, ACMD0-63).
7:6	0h	RW	**Command Type (command_cmdtype)** There are three types of special commands. Suspend, Resume and Abort. These bits shall be set to 00b for all other commands. 00b - Normal 01b - Suspend 10b - Resume 11b - Abort
5	0h	RW	**Data Present Select (command_datapresent)** This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. If is set to 0 for the following: 1. Commands using only CMD line(ex. CMD52) 2. Commands with no data transfer but using busy signal on DAT[0] line (R1b or R5b ex. CMD38) 3. Resume Command 0 - No Data Present 1 - Data Present
4	0h	RW	**Command Index Check Enable (command_indexchkena)** If this bit is set to 1, the HC shall check the index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error. If this bit is set to 0, the Index field is not checked.
3	0h	RW	**Command CRC Check Enable (command_crcchkena)** If this bit is set to 1, the HC shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error. If this bit is set to 0, the CRC field is not checked. 0 - Disable 1 – Enable

Bit Range	Default	Access	Field Name and Description
2	-	-	**Reserved**
1:0	0h	RW	**Response Type Select (command_responsetype)** 00 - No Response 01 - Response length 136 10 - Response length 48 11 - Response length 48 checkBusy after response

Response [1-8] (response01) – Offset 10

The response registers contains the 128 bit response received from the External Device.

There are 8 response registers:

Response 1: offset 10h

Response 2: offset 12h

Response 3: offset 14h

Response 4: offset 16h

Response 5: offset 18h

Response 6: offset 1Ah

Response 7: offset 1Ch

Response 8: offset 1Eh

Register details:

Response Register 1&2 = Response [31:0]

Response Register 3&4 = Response [63:32]

Response Register 5&6 = Response [95:64]

Response Register 7&8 = Response [127:96]

Buffer Data Port (dataport) – Offset 20

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Data Port (sdhcdmactrl_piobufrddata)** The Host Controller Buffer can be accessed through this 32-bit Data Port Register.

Present State (presentstate) – Offset 24

Bit Range	Default	Access	Field Name and Description
30:26	-	-	**Reserved**
25	0h	RO	**DAT[7:4] Line Signal Level (host_regu_vol_stb)** This status is used to check DAT line level to recover from errors, and for debugging. Bit 28 - DAT[7] Bit 27 - DAT[6] Bit 26 - DAT[5] Bit 25 - DAT[4]
24	1h	RO	**CMD Line Signal Level (sdif_cmdin_dsync)** This status is used to check CMD line level to recover from errors, and for debugging
23:20	fh	RO	**DAT[3:0] Line Signal Level (sdif_dat0in_dsync)** This status is used to check DAT line level to recover from errors, and for debugging. Bit 23 - DAT[3] Bit 22 - DAT[2] Bit 21 - DAT[1] Bit 20 - DAT[0]

Bit Range	Default	Access	Field Name and Description
19	0h	RO	**Write Protect Switch Pin Level (sdif_wp_dsync)** The Write Protect Switch is supported for memory and combo cards. This bit reflects the SDWP# pin. 0 - Write protected (SDWP# = 0) 1 - Write enabled (SDWP# = 1)
18	0h	RO	**Card Level Detect (sdif_cd_n_dsync)** This bit reflects the inverse value of the SDCD# pin. 0 - No Card present (SDCD# = 1) 1 - Card present (SDCD# = 0)
17	0h	RO	**Card State Stable (sdhccarddet_statestable_dsync)** This bit is used for testing. If it is 0, the Card Detect Pin Level is not stable. If this bit is set to 1, it means the Card Detect Pin Level is stable. The Software Reset For All in the Software Reset Register shall not affect this bit. 0 - Reset of Debouncing 1 - No Card or Inserted
16	0h	RO	**Card Inserted (sdhccarddet_inserted_dsync)** This bit indicates whether a card has been inserted. Changing from 0 to 1 generates a Card Insertion Interrupt in the Normal Interrupt Status register and changing from 1 to 0 generates a Card Removal Interrupt in the Normal Interrupt Status register. The Software Reset For All in the Software Reset register shall not affect this bit. If a Card is removed while its power is on and its clock is oscillating, the HC shall clear SD Bus Power in the Power Control register and SD Clock Enable in the Clock control register. In addition the HD should clear the HC by the Software Reset For All in Software register. The card detect is active regardless of the SD Bus Power. 0 - Reset or Debouncing or No Card 1 - Card Inserted
15:12	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
11	0h	RO	**Buffer Read Enable (sdhcdmactrl_piobufrdena)** This status is used for non-DMA read transfers. This read only flag indicates that valid data exists in the host side buffer status. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when all the block data is ready in the buffer and generates the Buffer Read Ready Interrupt. 0 - Read Disable 1 - Read Enable
10	0h	RO	**Buffer Write Enable (sdhcdmactrl_piobufwrena)** This status is used for non-DMA write transfers. This read only flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer. A change of this bit from 1 to 0 occurs when all the block data is written to the buffer. A change of this bit from 0 to 1 occurs when top of block data can be written to the buffer and generates the Buffer Write Ready Interrupt. 0 - Write Disable 1 - Write Enable.
9	0h	RO	**Read Transfer Active (sdhcdmactrl_rdxferactive)** This status is used for detecting completion of a read transfer. This bit is set to 1 for either of the following conditions: - After the end bit of the read command - When writing a 1 to continue Request in the Block Gap Control register to restart a read transfer. This bit is cleared to 0 for either of the following conditions: - When the last data block as specified by block length is transferred to the system. - When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the Stop At Block Gap Request set to 1. A transfer complete interrupt is generated when this bit changes to 0. 1 - Transferring data 0 - No valid data

Bit Range	Default	Access	Field Name and Description
8	0h	RO	**Write Transfer Active (sdhcdmactrl_wrxferactive)** This status indicates a write transfer is active. If this bit is 0, it means no valid write data exists in the HC. This bit is set in either of the following cases: - After the end bit of the write command. - When writing a 1 to Continue Request in the Block Gap Control register to restart a write transfer. This bit is cleared in either of the following cases: - After getting the CRC status of the last datablock as specified by the transfer count (Single or Multiple) - After getting a CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request. During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0, as a result of the Stop At Block Gap Request being set. This status is useful for the HD in determining when to issue commands during write busy. 1 - transferring data 0 - No valid data
7:4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3	0h	RO	**Re-Tuning Request (sdhcsdctrl_retuningreq_dsync)** Host Controller may request Host Driver to execute re-tuning sequence by setting this bit when the data window is shifted by temperature drift and a tuned sampling point does not have a good margin to receive correct data. This bit is cleared when a command is issued with setting Execute Tuning in the Host Control 2 register.Changing of this bit from 0 to 1 generates Re-Tuning Event. Refer to Normal Interrupt registers for more detail. This bit isn't set to 1 if Sampling Clock Select in the Host Control 2 register is set to 0 (using fixed sampling clock). 1= Sampling clock needs re-tuning 0 = Fixed or well tuned sampling clock
2	0h	RO	**DAT line Active (sdhcdmactrl_datalineactive)** This bit indicates whether one of the DAT line on SD bus is in use. 1 - DAT line active 0 - DAT line inactive
1	0h	RO	**Command Inhibit (DAT)** This status bit is generated if either the DAT Line Active or the Read transfer Active is set to 1. If this bit is 0, it indicates the HC can issue the next SD command. Commands with busy signal belong to Command Inhibit (DAT) (ex. R1b, R5b type). Changing from 1 to 0 generates a Transfer Complete interrupt in the Normal interrupt status register. Note: The SD Host Driver can save registers in the range of 000-00Dh for a suspend transaction after this bit has changed from 1 to 0. 1 - Cannot issue command which uses the DAT line 0 - Can issue command which uses the DAT line

Bit Range	Default	Access	Field Name and Description
0	0h	RO	**Command Inhibit (CMD)** If this bit is 0, it indicates the CMD line is not in use and the HC can issue a SD command using the CMD line. This bit is set immediately after the Command register (00Fh) is written. This bit is cleared when the command response is received. Even if the Command Inhibit (DAT) is set to 1, Commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 generates a Command complete interrupt in the Normal Interrupt Status register. If the HC cannot issue the command because of a command conflict error or because of Command Not Issued By Auto CMD12 Error, this bit shall remain 1 and the Command Complete is not set. Status issuing AutoCMD12 is not read from this bit. Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 operation, Host Controller shall manage to issue two commands: CMD12 and a command set by Command register.

Host Control 1 (hostcontrol1) – Offset 28

Bit Range	Default	Access	Field Name and Description
7	0h	RW	**Card Detect Signal Detection (hostctrl1_cdsigselect)** This bit selects source for card detection. 1- The card detect test level is selected 0 -SDCD# is selected (for normal use)

Bit Range	Default	Access	Field Name and Description
6	0h	RW	**Card Detect Test Level (hostctrl1_cdtestlevel)** This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates card inserted or not. Generates (card ins or card removal) interrupt when the normal int sts enable bit is set. 1 - Card Inserted 0 - No Card
5	0h	RW	**Extended Data Transfer Width (hostctrl1_extdatawidth)** This bit controls 8-bit bus width mode for embedded device. Support of this function is indicated in 8-bit Support for Embedded Device in the Capabilities register. If a device supports 8-bit bus mode, this bit may be set to 1. If this bit is 0, bus width is controlled by Data Transfer Width in the Host Control 1 register. This bit is not effective when multiple devices are installed on a bus slot (Slot Type is set to 10b in the Capabilities register). In this case, each device bus width is controlled by Bus Width Preset field in the Shared Bus register. 1 - 8-bit Bus Width 0 - Bus Width is Selected by Data Transfer Width
4:3	0h	RW	**DMA Select (hostctrl1_dmaselect)** One of supported DMA modes can be selected. The host driver shall check support of DMA modes by referring the Capabilities register. 00 - SDMA is selected 01 - 32-bit Address ADMA1 is selected 10 - 32-bit Address ADMA2 is selected 11 - 64-bit Address ADMA2 is selected.

Bit Range	Default	Access	Field Name and Description
2	0h	RW	**High Speed Enable (hostctrl1_highspeedena)** This bit is optional. Before setting this bit, the HD shall check the High Speed Support in the capabilities register. If this bit is set to 0 (default), the HC outputsCMD line and DAT lines at the falling edge of the SD clock (up to 25 MHz/ 20MHz for MMC). If this bit is set to 1, the HC outputs CMD line and DAT lines at the rising edge of the SD clock (up to 50 MHz for SD/52MHz for MMC)/ 208Mhz (for SD3.0)If Preset Value Enable in the Host Control 2 register is set to 1, Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitches. After setting this field, the Host Driver sets SD Clock Enable again 1 - High Speed Mode 0 - Normal Speed Mode
1	0h	RW	**Data Transfer Width (hostctrl1_datawidth)** This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card. 1 - 4 bit mode 0 - 1 bit mode
0	0h	RW	**LED Control (hostctrl1_ledcontrol)** This bit is used to caution the user not to remove the card while the SD card is being accessed. If the software is going to issue multiple SD commands, this bit can be set during all transactions. It is not necessary to change for each transaction. 1 - LED on 0 - LED off

Power Control (powercontrol) – Offset 29

Bit Range	Default	Access	Field Name and Description
6:4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3:1	0h	RW	**SD Bus Voltage Select (sdbus_voltage_sel_vdd1)** By setting these bits, the HC selects the voltage level for the SD card. Before setting this register, the HC shall check the voltage support bits in the capabilities register. If an unsupported voltage is selected, theHost System shall not supply SD bus voltage 111b - 3.3 Flattop.) 110b - 3.0 V(Typ.) 101b - 1.8 V(Typ.) 100b - 000b – Reserved
0	0h	RW	**SD Bus Power (sdbus_power_vdd1)** Before setting this bit, the SD host driver shall set SD Bus Voltage Select. If the HC detects the No Card State, this bit shall be cleared. 1 - Power on 0 - Power off

Block Gap Control (blockgapcontrol) – Offset 2a

Bit Range	Default	Access	Field Name and Description
6:4	-	-	**Reserved**
3	0h	RW	**Interrupt at Block Gap (intr_at_block_gap)** This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the card.

Bit Range	Default	Access	Field Name and Description
2	0h	RW	**(rd_wait_ctrl)** Read Wait ControlThe read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using DAT[2] line. Otherwise the HC has to stop the SD clock to hold read data, which restricts commands generation. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit shall never be set to 1 otherwise DAT line conflict may occur. If this bit is set to 0, Suspend / Resume cannot be supported 1 - Enable Read Wait Control 0 - Disable Read Wait Control
1	0h	RW	**Continue Request (continue_req)** This bit is used to restart a transaction which was stopped using the Stop At Block Gap Request. To cancel stop at the block gap, set Stop At block Gap Request to 0 and set this bit to restart the transfer. The HC automatically clears this bit in either of the following cases: 1) In the case of a read transaction, the DAT Line Active changes from 0 to 1 as a read transaction restarts. 2) In the case of a write transaction, the Write transfer active changes from 0 to 1 as the write transaction restarts. Therefore it is not necessary for Host driver to set this bit to 0. If Stop At Block Gap Request is set to 1, any write to this bit is ignored. 1 - Restart 0 - Ignored
0	0h	RW	**Stop At Block Gap Request (stopatblkgap_req)** This bit is used to stop executing a transaction at the next block gap for non-DMA,SDMA and ADMA transfers. Until the transfer complete is set to 1, indicating a transfer completion the HD shall leave this bit set to 1. Clearing both the Stop At Block Gap Request and Continue Request shall not cause the transaction to restart. Read Wait is used to stop the read transaction at the block gap. The HC shall honor Stop At Block Gap Request for write transfers, but for read transfers it requires that the SD card support Read Wait. Therefore the HD shall not set this bit during read transfers unless the SD card supports Read Wait and has set Read Wait Control to 1. In case of write transfers in which the HD writes data to the Buffer Data Port register, the HD shall set this bit after all block data is written. If this bit is set to 1, the HD shall not write data to Buffer data port register. This bit affects Read Transfer Active, Write Transfer Active, DAT line active and Command Inhibit (DAT) in the Present State register.

Wakeup Control (wakeupcontrol) – Offset 2b

Bit Range	Default	Access	Field Name and Description
6:3	-	-	**Reserved**
2	0h	RW	**Wakeup Event Enable On SD Card Removal (wkupctrl_cardremoval)** This bit enables wakeup event via Card Removal assertion in the Normal Interrupt Status register.FN_WUS (Wake up Support) in CIS does not affect this bit. 1 - Enable 0 – Disable
1	0h	RW	**Wakeup Event Enable On SD Card Insertion (wkupctrl_cardinsertion)** This bit enables wakeup event via Card Insertion assertion in the Normal Interrupt Status register.FN_WUS (Wake up Support) in CIS does not affect this bit. 1 - Enable 0 – Disable
0	0h	RW	**(wkupctrl_cardinterrupt)** Wakeup Event Enable On Card InterruptThis bit enables wakeup event via Card Interrupt assertion in the Normal Interrupt Status register.This bit can be set to 1 if FN_WUS (Wake Up Support) in CIS is set to 1. 1 - Enable 0 – Disable

Clock Control (clockcontrol) – Offset 2c

Bit Range	Default	Access	Field Name and Description
15:8	00h	RW	**SDCLK Frequency Select (clkctrl_sdclkfreqsel)** This register is used to select the frequency of the SDCLK pin. The frequency is not programmed directly; rather this register holds the divisor of the Base Clock Frequency For SD clock in the capabilities register. Only the following settings are allowed. 1) 8-bit Divided Clock Mode 80h - base clock divided by 256

Bit Range	Default	Access	Field Name and Description
			40h - base clock divided by 128 20h - base clock divided by 64 10h - base clock divided by 32 08h - base clock divided by 16 04h - base clock divided by 8 02h - base clock divided by 4 01h - base clock divided by 2 00h - base clock(10MHz-63MHz) Setting 00h specifies the highest frequency of the SD Clock. When setting multiple bits, the most significant bit is used as the divisor. But multiple bits should not be set. The two default divider values can be calculated by the frequency that is defined by the Base Clock Frequency For SD Clock in the Capabilities register. a) 25 MHz divider value b) 400 KHz divider value The frequency of the SDCLK is set by the following formula: Clock Frequency = (Baseclock) / divisor. Thus choose the smallest possible divisor which results in a clock frequency that is less than or equal to the target frequency. 2) 10-bit Divided Clock Mode Host Controller Version 3.00 supports this mandatory mode instead of the 8-bit Divided Clock Mode. The length of divider is extended to 10 bits and all divider values shall be supported. 3FFh --1/2046 Divided Clock N -------1/2N Divided Clock (Duty 50%) 002h -- 1/4 Divided Clock 001h ---1/2 Divided Clock 000h --- Base Clock (10MHz-254MHz)
7:6	0h	RW	**Upper Bits of SDCLK Frequency Select (clkctrl_sdclkfreqsel_upperbits)** Bit 07-06 is assigned to bit 09-08 of clock divider in SDCLK Frequency Select.

Bit Range	Default	Access	Field Name and Description
5	0h	RW	**Clock Generator Select (clkctrl_clkgensel)** This bit is used to select the clock generator mode in SDCLK Frequency Select.If the Programmable Clock Mode is supported (non-zerovalue is set to Clock Multiplier in the Capabilities register), this bit attribute is RW, and if not supported, this bit attribute is RO and zero is read. This bit depends on the setting of Preset Value Enable in the Host Control 2 register. If the Preset Value Enable = 0, this bit is set by Host Driver. If the Preset Value Enable = 1, this bit is automatically set to a value specified in one of Preset Value registers. 1 = Programmable Clock Mode 0 = Divided Clock Mode
4:3	-	-	**Reserved**
2	0h	RW	**SD Clock Enable (clkctrl_sdclkena)** The HC shall stop SDCLK when writing this bit to 0. SDCLK frequency Select can be changed when this bit is 0. Then, the HC shall maintain the same clock frequency until SDCLK is stopped (Stop at SDCLK = 0). If the HC detects the No Card state, this bit shall be cleared. 1 - Enable 0 – Disable
1	0h	RO	**Internal Clock Stable (sdhcclkgen_intclkstable_dsync)** This bit is set to 1 when SD clock is stable after writing to Internal Clock Enable in this register to 1. The SD Host Driver shall wait to set SD Clock Enable until this bit is set to 1. Note: This is useful when using PLL for a clock oscillator that requires setup time. 1 - Ready 0 - Not Ready

Bit Range	Default	Access	Field Name and Description
0	0h	RW	**Internal Clock Enable (clkctrl_intclkena)** This bit is set to 0 when the HD is not using the HC or the HC awaits a wakeup event. The HC should stop its internal clock to go very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1. When clock oscillation is stable, the HC shall set Internal Clock Stable in this register to 1. This bit shall not affect card detection. 1 - Oscillate 0 - Stop

Timeout Control (timeoutcontrol) – Offset 2e

Bit Range	Default	Access	Field Name and Description
6:4	-	-	**Reserved**
3:0	0h	RW	**Data Timeout Counter Value (data_timeout_cntr_val)** This value determines the interval by which DAT line time-outs are detected. Refer to the Data Time-out Error in the Error Interrupt Status register for information on factors that dictate time-out generation. Time-out clock frequency will be generated by dividing the sd clock TMCLK by this value. When setting this register, prevent inadvertent time-out events by clearing the Data Time-out Error Status Enable (in the Error Interrupt Status Enable register) 1111 - Reserved 1110 - TMCLK * 2^27---------- ---------- 0001 - TMCLK * 2^14 0000 - TMCLK * 2^13

Software Reset (softwarereset) – Offset 2f

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
6:3	-	-	**Reserved**
2	0h	RW	**Software Reset for DAT Line (swreset_for_dat)** Only part of data circuit is reset. The followingregisters and bits are cleared by this bit: Buffer Data Port Register - Buffer is cleared and initialized. Present State register - Buffer read Enable - Buffer write Enable - Read Transfer Active - Write Transfer Active - DAT Line Active - Command Inhibit (DAT) Block Gap Control register - Continue Request - Stop At Block Gap Request Normal Interrupt Status register - Buffer Read Ready - Buffer Write Ready - Block Gap Event - Transfer Complete 1 - Reset 0 - Work

Bit Range	Default	Access	Field Name and Description
1	0h	RW	**Software Reset for CMD Line (swreset_for_cmd)** Only part of command circuit is reset. The following registers and bits arecleared by this bit: Present State register - Command Inhibit (CMD) Normal Interrupt Status register - Command Complete 1 - Reset 0 - Work
0	0h	RW	**Software Reset for All (swreset_for_all)** This reset affects the entire HC except for the card detection circuit. Register bits of type ROC, RW, RW1C, RWAC are cleared to 0. During its initialization, the HD shall set this bit to 1 to reset the HC. The HC shall reset this bit to 0 when capabilities registers are valid and the HD can read them. Additional use of Software Reset For All may not affect the value of the Capabilities registers. If this bit is set to 1, the SD card shall reset itself andmust be re initialized by the HD. 1 - Reset 0 - Work

Normal Interrupt Status (normalintrsts) – Offset 30

Bit Range	Default	Access	Field Name and Description
15	0h	RO	**Error Interrupt Status (reg_errorintrsts)** Error InterruptIf any of the bits in the Register are set, then this bit is set. Therefore the HD can test for an error by checking this bit first. 0 - No Error. 1 – Error
14	0h	RWC1	**Boot terminate Interrupt (Boot_Term_Int)** This status is set if the boot operation get terminated 0 - Boot operation is not terminated. 1 - Boot operation is terminated
13	0h	RW1C	**Boot Acknowlege RCV (FX_event)** This status is set if the boot acknowledge is received from device. 0 - Boot ack is not received. 1 - Boot ack is received.
12	0h	RO	**Re-Tuning Event (normalintrsts_retuningevent)** This status is set if Re-Tuning Request in the Present State register changes from 0 to 1. Host Controller requests Host Driver to performre-tuning for next data transfer. Current data transfer (not large block count) can be completed without re-tuning. 1 Re-Tuning should be performed 0 Re-Tuning is not required
11	0h	RO	**INT_C (normalintrsts_intc)** This status is set if INT_C is enabled and INT_C# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_C interrupt factor
10	0h	RO	**INT_B (normalintrsts_intb)** This status is set if INT_B is enabled and INT_B# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_B interrupt factor
9	0h	RO	**INT_A (normalintrsts_inta)** This status is set if INT_A is enabled and INT_A# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_A interrupt factor

Bit Range	Default	Access	Field Name and Description
8	0h	RO	**Card Interrupt (normalintrsts_cardintsts)** Writing this bit to 1 does not clear this bit. It is cleared by resetting the SD card interrupt factor. In 1-bit mode, the HC shall detect the Card Interrupt without SD Clock to support wakeup. In 4-bit mode, the card interrupt signal is sampled during the interrupt cycle, so there are some sample delays between the interrupt signal from the card and the interrupt to the Host system. when this status has been set and the HD needs to start this interrupt service, Card Interrupt Status Enable in the Normal Interrupt Status register shall be set to 0 in order to clear the card interrupt statuses latched in the HC and stop driving the Host System. After completion of the card interrupt service (the reset factor in the SD card and the interrupt signal may not be asserted), set Card Interrupt Status Enable to 1 and start sampling the interrupt signal again. Interrupt detected by DAT[1] is supported when there is a card per slot. In case of shared bus, interrupt pins are used to detect interrupts. If 000b is set to Interrupt Pin Select in the Shared Bus Control register, this status is effective. Non-zero value is set to Interrupt Pin Select, INT_A, INT_B or INT_C is then used to device interrupts. 0 - No Card Interrupt 1 - Generate Card Interrupt
7	0h	RW/1C	**Card Removal (normalintrsts_cardremsts)** This status is set if the Card Inserted in the Present State register changes from 1 to 0. When the HD writes this bit to 1 to clear this status the status of the Card Inserted in the Present State register should be confirmed. Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated. 0 - Card State Stable or Debouncing 1 - Card Removed

Bit Range	Default	Access	Field Name and Description
6	0h	RW/1C	**Card Insertion (normalintrsts_cardinssts)** This status is set if the Card Inserted in the Present State register changes from 0 to 1.When the HD writes this bit to 1 to clear this status the status of the Card Inserted in the Present State register should be confirmed.Because the card detect may possibly be changed when the HD clear this bit an Interrupt event may not be generated. 0 - Card State Stable or Debouncing 1 - Card Inserted
5	0h	RW/1C	**Buffer Read Ready (normalintrsts_bufrdready)** This status is set if the Buffer Read Enable changes from 0 to 1. Buffer Read Ready is set to 1 for every CMD19 execution in tuning procedure. 0 - Not Ready to read Buffer. 1 - Ready to read Buffer
4	0h	RW/1C	**Buffer Write Ready (normalintrsts_bufwrready)** This status is set if the Buffer Write Enable changes from 0 to 1. 0 - Not Ready to Write Buffer. 1 - Ready to Write Buffer
3	0h	RW/1C	**DMA Interrupt (normalintrsts_dmainterrupt)** This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size Register. 0 - No DMA Interrupt 1 - DMA Interrupt is Generated
2	0h	RW/1C	**Block Gap Event (normalintrsts_blkgapevent)** If the Stop At Block Gap Request in the Block Gap Control Register is set, this bit is set. 0 - No Block Gap Event 1 - Transaction stopped at Block Gap

Bit Range	Default	Access	Field Name and Description
1	0h	RW/1C	**Transfer Complete (normalintrsts_xfercomplete)** This bit is set when a read / write transaction is completed. 0 - No Data Transfer Complete 1 - Data Transfer Complete
0	0h	RW/1C	**Command Complete (normalintrsts_cmdcomplete)** This bit is set when we get the end bit of the command response (Except Auto CMD12 and Auto CMD23) Note: Command Time-out Error has higher priority than Command Complete. If both are set to 1, it can be considered that the response was not received correctly. 0 - No Command Complete 1 - Command Complete

Error Interrupt Status (errorintrsts) – Offset 32

Bit Range	Default	Access	Field Name and Description
14:13	-	-	**Reserved**
12	0h	RW/1C	**Target Response error (target_response_error)** Occurs when detecting ERROR in DMA transaction. 0 - no error 1 – error
11:10	-	-	**Reserved**
9	0h	RW/1C	**ADMA Error (adma_error)** This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status Register. 1- Error 0 -No error

Bit Range	Default	Access	Field Name and Description
8	0h	RW/1C	**Auto CMD Error (auto_cmd_err_sd_mode)** This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register has changed from 0 to 1. In case of Auto CMD12, this bit is set to 1, not only when the errors in Auto CMD12 occur but also when Auto CMD12 is not executed due to the previous command error. 0 - No Error 1 – Error
7	0h	RW/1C	**Current Limit Error (current_limit_err)** By setting the SD Bus Power bit in the Power Control Register, the HC is requested to supply power for the SD Bus. If the HC supports the Current Limit Function, it can be protected from an Illegal card by stopping power supply to the card in which case this bit indicates a failure status. Reading 1 means the HC is not supplying power to SD card due to some failure. Reading 0 means that the HC is supplying power and no error has occurred. This bit shall always set to be 0, if the HC does not support this function. 0 - No Error 1 - Power Fail
6	0h	RW/1C	**Data End Bit Error (data_end_bit_err)** Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status. 0 - No Error 1 – Error
5	0h	RW/1C	**Data CRC Error (data_crc_err_sd_mode)** Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than 010b. 0 - No Error 1 – Error

Bit Range	Default	Access	Field Name and Description
4	0h	RW/1C	**Data Timeout Error (data_timeout_err_sd_mode)** Occurs when detecting one of following timeout conditions:{br]1. Busy Timeout for R1b, R5b type. 2. Busy Timeout after Write CRC status 3. Write CRC status Timeout 4. Read Data Timeout 0 - No Error 1 – Timeout
3	0h	RW/1C	**Command Index Error (cmd_index_err_sd_mode)** Occurs if a Command Index error occurs in the Command Response. 0 - No Error 1 – Error
2	0h	RW/1C	**Command End Bit Error (cmd_end_bit_err_sd_mode)** Occurs when detecting that the end bit of a command response is 0. 0 - No Error 1 - End Bit Error Generated
1	0h	RW/1C	**Command CRC Error (cmd_crc_err_sd_mode)** Command CRC Error is generated in two cases. 1. If a response is returned and the Command Time-out Error is set to 0, this bit is set to 1 when detecting a CRT error in the command response 2. The HC detects a CMD line conflict by monitoring the CMD line when a command is issued. If the HC drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SDCLK edge, then the HC shall abort the command (Stop driving CMD line) and set this bit to 3. The Command Timeout Error shall also be set to 1 to distinguish CMD line conflict. 0 - No Error 1 - CRC Error Generated

Bit Range	Default	Access	Field Name and Description
0	0h	RW/1C	**Command Timeout Error (cmd_timeout_err_sd_mode)** Occurs only if the no response is returned within 64 SDCLK cycles from the end bit of the command. If the HC detects a CMD line conflict, in which case Command CRC Error shall also be set. This bit shall be set without waiting for 64 SDCLK cycles because the command will be aborted by the HC. 0 - No Error 1 – Timeout

Normal Interrupt Status Enable (normalintrstsena) – Offset 34

Bit Range	Default	Access	Field Name and Description
14	0h	RO	**Boot terminate Interrupt Enable (Boot_Term_Int)** This status is set if the boot operation gets terminated. 0 - Masked 1 – Enabled
13	0h	RW	**Boot ack rcv enable (FX_event_sts_enb)** This status is set if the boot acknowledge is received from device. 0 - Masked 1 – Enabled
12	0h	RW	**Re-Tuning Event Status Enable (re_tuning_evnt_sts_enb)** This status is set if Re-Tuning Request in the Present State register changes from 0 to 1. 0 - Masked 1 – Enabled
11	0h	RW	**INT_C Status Enable (int_c_sts_enb)** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_C and may set this bit again after all interrupt requests to INT_C pin are cleared to prevent inadvertent interrupts

Bit Range	Default	Access	Field Name and Description
10	0h	RW	**INT_B Status Enable (int_b_sts_enb)** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_B and mayset this bit again after all interrupt requests to INT_B pin are cleared to prevent inadvertent interrupts
9	0h	RW	**INT_A Status Enable (int_a_sts_enb)** If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_A and may set this bit again after all interrupt requests to INT_A pin are cleared to prevent inadvertent interrupts
8	0h	RW	**Card Interrupt Status Enable (sdhcregset_cardintstsena)** If this bit is set to 0, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1. The HD may clear the Card Interrupt Status Enable before servicing the Card Interrupt and may set this bit again after all Interrupt requests from the card are cleared to prevent inadvertent Interrupts. 0 - Masked 1 - Enabled
7	0h	RW	**Card Removal Status Enable (sdhcregset_cardremstsena)** This status is set if the Card Inserted in the Present State register changes from 1 to 0. 0 - Masked 1 - Enabled
6	0h	RW	**Card Insertion Status Enable (sdhcregset_cardinsstsena)** This status is set if the Card Inserted in the Present State register changes from 0 to 1. 0 - Masked 1 - Enabled

Bit Range	Default	Access	Field Name and Description
5	0h	RW	**Buffer Read Ready Status Enable (buffer_rd_ready_sts_en)** This status is set if the Buffer Read Enable changes from 0 to 1. 0 - Masked 1 - Enabled
4	0h	RW	**Buffer Write Ready Status Enable (buffer_wr_ready_sts_en)** This status is set if the Buffer Write Enable changes from 0 to 1. 0 - Masked 1 – Enabled
3	0h	RW	**DMA Interrupt Status Enable (dma_intr_sts_enb)** This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size register. 0 - Masked 1 – Enabled
2	0h	RW	**Block Gap Event Status Enable (block_gap_event_sts_enb)** If the Stop At Block Gap Request in the BlockGap Control Register is set, this bit is set. 0 - Masked 1 – Enabled
1	0h	RW	**Transfer Complete Status Enable (transfer_complete_sts_enb)** This bit is set when a read / write transaction is completed. 0 - Masked 1 - Enabled
0	0h	RW	**Command Complete Status Enable (cmd_complete_sts_enb)** This bit is set when we get the end bit of the command response. 0 - Masked 1 - Enabled

Error Interrupt Status Enable (errorintrstsena) – Offset 36

Bit Range	Default	Access	Field Name and Description
14:12	-	-	**Reserved**
11	0h	RW	**Reponse Error Status Enable (response_err_sts_enb)** 0 - Masked 1 - Enabled
10	0h	RW	**Tuning error status enable (tuning_err_sts_enb)** 0 - Masked 1 - Enabled
9	0h	RW	**ADMA Error Status Enable (adma_err_sts_enb)** 0 - Masked 1 - Enabled
8	0h	RW	**Auto CMD12 Error Status Enable (auto_cmd_err_sts_enb)** 0 - Masked 1 - Enabled
7	0h	RW	**Current Limit Error Status Enable (current_limit_err_sts_enb)** 0 - Masked 1 - Enabled
6	0h	RW	**Data End Bit Error Status Enable (data_end_bit_err_sts_enb)** 0 - Masked 1 - Enabled
5	0h	RW	**Data CRC Error Status Enable (data_crc_err_sd_mode)** 0 - Masked 1 - Enabled
4	0h	RW	**Data Timeout Error Status Enable (data_timeout_err_sd_mode)** 0 - Masked 1 - Enabled

Bit Range	Default	Access	Field Name and Description
3	0h	RW	**Command Index Error Status Enable (cmd_index_err_sd_mode)** 0 - Masked 1 - Enabled
2	0h	RW	**Command End Bit Error Status Enable (cmd_end_bit_err_sd_mode)** 0 - Masked 1 - Enabled
1	0h	RW	**Command CRC Error Status Enable (cmd_crc_err_sd_mode)** 0 - Masked 1 - Enabled
0	0h	RW	**Command Timeout Error Status Enable (cmd_timeout_err_sd_mode)** 0 - Masked 1 - Enabled

Normal Interrupt Signal Enable (normalintrsigena) – Offset 38

Bit Range	Default	Access	Field Name and Description
14	0h	RO	**Boot Terminate Interrupt Signal Enable (Boot_Term_Int)** 0 - Masked 1 - Enabled
13	0h	RW	**Boot ack rcv Signal Enable (FX_event_sigenb)** 0 - Masked 1 - Enabled
12	0h	RW	**Re-Tuning Event Signal Enable (retung_evnt_intrsig_enb)** 0 - Masked 1 - Enabled

Bit Range	Default	Access	Field Name and Description
11	0h	RW	**INT_C Signal Enable (int_c_sig_enb)** 0 - Masked 1 - Enabled
10	0h	RW	**INT_B Signal Enable (int_b_sig_enb)** 0 - Masked 1 - Enabled
9	0h	RW	**INT_A Signal Enable (int_a_sig_enb)** 0 - Masked 1 - Enabled
8	0h	RW	**Card Interrupt Signal Enable (card_intr_sig_enb)** 0 - Masked 1 - Enabled
7	0h	RW	**Card Removal Signal Enable (card_remove_sig_enb)** 0 - Masked 1 - Enabled
6	0h	RW	**Card Insertion Signal Enable (card_insert_sig_enb)** 0 - Masked 1 - Enabled
5	0h	RW	**Buffer Read Ready Signal Enable (buffer_rd_ready_sig_enb)** 0 - Masked 1 - Enabled
4	0h	RW	**Buffer Write Ready Signal Enable (buffer_wr_ready_sig_enb)** 0 - Masked 1 - Enabled

Bit Range	Default	Access	Field Name and Description
3	0h	RW	**DMA Interrupt Signal Enable (dma_intr_sig_enb)** 0 - Masked 1 - Enabled
2	0h	RW	**Block Gap Event Signal Enable (block_gap_event_sig_enb)** 0 - Masked 1 - Enabled
1	0h	RW	**Transfer Complete Signal Enable (transfer_complete_sig_enb)** 0 - Masked 1 - Enabled
0	0h	RW	**Command Complete Signal Enable (cmd_complete_sig_enb)** 0 - Masked 1 - Enabled

Error Interrupt Signal Enable (errorintrsigena) – Offset 3a

Bit Range	Default	Access	Field Name and Description
14:11	-	-	**Reserved**
10	0h	RW	**Tuning Error Signal Enable (tuning_err_sig_enb)** 0 - Masked 1 - Enabled
9	0h	RW	**ADMA Error Signal Enable (adma_err_sig_enb)** 0 - Masked 1 - Enabled

Bit Range	Default	Access	Field Name and Description
8	0h	RW	**Auto CMD Error Signal Enable (auto_cmd_err_sig_enb)** 0 - Masked 1 - Enabled
7	0h	RW	**Current Limit Error Signal Enable (current_limit_err_sig_enb)** 0 - Masked 1 - Enabled
6	0h	RW	**Data End Bit Error Signal Enable (data_end_bit_err_sig_enb)** 0 - Masked 1 - Enabled
5	0h	RW	**Data CRC Error Signal Enable (data_crc_err_sig_sd_mode)** 0 - Masked 1 - Enabled
4	0h	RW	**Data Timeout Error Signal Enable (data_timeout_err_sig_sd_mode)** 0 - Masked 1 - Enabled
3	0h	RW	**Command Index Error Signal Enable (cmd_index_err_sig_sd_mode)** 0 - Masked 1 - Enabled
2	0h	RW	**Command End Bit Error Signal Enable (cmd_end_bit_err_sig_sd_mode)** 0 - Masked 1 - Enabled
1	0h	RW	**Command CRC Error Signal Enable (cmd_crc_err_sig_sd_mode)** 0 - Masked 1 - Enabled
0	0h	RW	**Command Timeout Error Signal Enable (cmd_timeout_err_sig_sd_mode)** 0 - Masked 1 - Enabled

Auto CMD12 Error Status (autocmderrsts) – Offset 3c

Bit Range	Default	Access	Field Name and Description
14:8	-	-	**Reserved**
7	0h	RO	**Command Not Issued By Auto CMD12 Error (autocmderrsts_nexterror)** Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 error(D04- D01) in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23 0 – No Error 1 – Not Issued
6:5	-	-	**Reserved**
4	0h	RO	**Auto CMD Index Error (autocmderrsts_indexerror)** Occurs if the Command Index error occurs in response to a command. 0 – No Error 1 – Error
3	0h	RO	**Auto CMD End Bit Error (autocmderrsts_endbiterror)** Occurs when detecting that the end bit of command response is 0. 0 – No Error 1 – End Bit Error Generated
2	0h	RO	**Auto CMD CRC Error (autocmderrsts_crcerror)** Occurs when detecting a CRC error in the command response. 0 – No Error 1 – CRC Error Generated
1	0h	RO	**Auto CMD Timeout Error (autocmderrsts_timeouterror)** Occurs if the no response is returned within 64 SDCLK cycles from the end bit of the command. If this bit is set to 1, the other error status bits (D04 - D02) are meaningless. 0 - No Error 1 - Timeout.

Bit Range	Default	Access	Field Name and Description
0	0h	RO	**Auto CMD12 not Executed (autocmderrsts_notexecerror)** If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1 means the HC cannot issue Auto CMD12 to stop memory multiple block transfer due to some error. If this bit is set to 1, other error status bits (D04 - D01) are meaningless. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. 0 - Executed 1 - Not Executed

Host Control 2 (hostcontrol2) – Offset 3e

Bit Range	Default	Access	Field Name and Description
15	0h	RW	**Preset Value Enable (hostctrl2_presetvalueenable)** When Preset Value Enable is set to automatic. This bit enables the functions defined in the Preset Value registers. 1 - Automatic Selection by Preset Value is Enabled 0 - SDCLK and Driver Strength are controlled by Host Driver If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver.If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers
14	0h	RW	**Asynchronous Interrupt Enable (hostctrl2_asynchintrenable)** This bit can be set to 1 if a card support asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode (and zero is set to Interrupt Pin Select in the Shared Bus Control register). If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. 0 – Disabled 1 – Enabled

Bit Range	Default	Access	Field Name and Description
13:8	-	-	**Reserved**
7	0h	RW	**Sampling Clock Select (hostctrl2_samplingclkselect)** This bit is set by tuning procedure when Execute Tuning is cleared. Writing 1 to this bit is meaningless and ignored. Setting 1 means that tuning is completed successfully and setting 0 means that tuning is failed. Host Controller uses this bit to select sampling clock to receive CMD and DAT. This bit is cleared by writing 0. Change of this bit is not allowed while the Host Controller is receiving response or a read data block. 0 - Fixed clock is used to sample data 1 - Tuned clock is used to sample data
6	0h	RW	**Execute Tuning (hostctrl2_executetuning)** This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0 for more detail about tuning procedure. 0 - Not Tuned or Tuning Completed 1 - Execute Tuning
5:4	0h	RW	**Driver Strength Select (hostctrl2_driverstrengthsel)** Host Controller output driver in 1.8V signaling is selected by this bit. In 3.3V signaling, this field is not effective. This field can be set depends on Driver Type A, C and D support bits in the Capabilities register. This bit depends on setting of Preset Value Enable. If Preset Value Enable = 0, this field is set by Host Driver. If Preset Value Enable = 1, this field is automatically set by a value specified in the one of Preset Value registers. 00b Driver Type B is Selected (Default) 01b Driver Type A is Selected 10b Driver Type C is Selected 11b Driver Type D is Selected

Bit Range	Default	Access	Field Name and Description
3	0h	RW	**1.8V Signaling Enable (hostctrl2_1p8vsignallingena)** This bit controls voltage regulator for I/O cell. 3.3V is supplied to the card regardless of signaling voltage. Setting this bit from 0 to 1 starts changing signal oltage from 3.3V to 1.8V.1.8V regulator output shall be stable within 5ms. Host Controller clears this bit if switching to 1.8V signaling fails. Clearing this bit from 1 to 0 starts changing signal voltage from 1.8V to 3.3V.3.3V regulator output shall be stable within 5ms.Host Driver can set this bit to 1 when Host Controller supports 1.8V signaling (One of support bits is set to 1: SDR50, SDR104 or DDR50 in the Capabilities register) and the card or device supports UHS-I. 1 - 1.8V Signaling 0 - 3.3V Signaling

Bit Range	Default	Access	Field Name and Description
2:0	0h	RW	**UHS Mode Select (hostctrl2_uhsmodeselect)** This field is used to select one of UHS-I modes and effective when 1.8V Signaling Enable is set to 1. If Preset Value Enable in the Host Control 2 register is set to 1, Host Controller sets SDCLK Frequency Select, Clock GeneratorSelect in the Clock Control register and Driver StrengthSelect according to Preset Value registers. In this case, one of preset value registers is selected by this field. Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitch. After setting this field, Host Driver sets SD Clock Enable again. 000b - SDR12 001b - SDR25 010b - SDR50 011b - SDR104 100b - DDR50 101b - HS400 110b - 111 Reserved When SDR50, SDR104 or DDR50 is selected for SDIO card, interrupt detection at the block gap shall not be used. Read Wait timing is changed for these modes.

Capabilities (capabilities) – Offset 40

Bit Range	Default	Access	Field Name and Description
63	0h	RO	**HS 400 Support (HS_400)** This field indicates whether HS400 is supported or not. 0 –Not Supported 1 –Supported
62:56	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
55:48	00h	RO	**Clock Multiplier (clk_mult)** This field indicates clock multiplier value of programmable clock generator. Refer to Clock Control register.Setting 00h means that Host Controller does not support programmable clock generator.FFh: Clock Multiplier M = 256.... 02h: Clock Multiplier M = 3 01h: Clock Multiplier M = 2 00h: Clock Multiplier is Not Supported.
47:46	0h	RO	**Re-tuning modes (re_tuning_modes)** This field defines the re-tuning capability of a Host Controller and how to manage the data transfer length and a Re-Tuning Timer by the Host Driver 00 - Mode1 01 - Mode2 10 - Mode3 11 - Reserved There are two re-tuning timings,Re-Tuning Request and expiration of a Re-Tuning Timer. By receiving either timing, the Host Driver executesthe re-tuning procedure just before a next command issue.
45	0h	RO	**Use Tuning for SDR50 (use_tung_sdr50)** If this bit is set to 1, this Host Controller requires tuning to operate SDR50. (Tuning is always required to operate SDR104.) 1 SDR50 requires tuning 0 SDR50 does not require tuning
44	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
43:40	0h	RO	**Timer Count for Re-Tuning (timer_cnt_retung)** This field indicates an initial value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3. 0h - Get information via other source 1h = 1 seconds 2h = 2 seconds 3h = 4 seconds 4h = 8 seconds -- n = 2(n-1) seconds-- Bh = 1024 seconds Fh - Ch = Reserved
39	-	-	**Reserved**
38	0h	RO	**Driver Type D Support (drv_typeD_support)** This bit indicates support of Driver Type D for 1.8 Signaling. 1 Driver Type D is Supported 0 Driver Type D is Not Supported
37	0h	RO	**Driver Type C Support (drvtypeC_support)** This bit indicates support of Driver Type C for 1.8 Signaling. 1: Driver Type C is Supported 0: Driver Type C is Not Supported
36	0h	RO	**Driver Type A Support (drvtypeA_support)** This bit indicates support of Driver Type A for 1.8 Signaling. 1: Driver Type A is Supported 0: Driver Type A is Not Supported
35	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
34	1h	RO	**DDR50 Support (ddr50_support)** This bit indicates whether DDR50 is supported. 0 –Not Supported 1 –Supported
33	1h	RO	**SDR104 Support (sdr104support)** This bit indicates whether SDR104 is supported. 0 –Not Supported 1 –Supported
32	1h	RO	**SDR50 Support (sdr50_support)** This bit indicates whether SDR50 is supported. 0 –Not Supported 1 –Supported
31:30	0h	RO	**Slot Type (slot_type)** This field indicates usage of a slot by a specific Host System. (A host controller register set is defined per slot.) Embedded slot for one device (01b) means that only one on-removable device is connected to a SD bus slot. Shared Bus Slot (10b) can be set if Host Controller supports Shared Bus Control register. The Standard Host Driver controls only a removable card or one embedded device is connected to a SD bus slot. If a slot is configured for shared bus (10b), the Standard Host Driver does not control embedded devices connected to a shared bus. Shared bus slot is controlled by a specific host driver developed by a Host System. 00b: Removable Card Slot 01b: Embedded Slot for One Device{br]10b: Shared Bus Slot{br]11b: Reserved
29	1h	RO	**Asynchronous Interrupt Support (asynch_intr_support)** This bit indicates whether the HC supports Asynchronous Interrupt. 0 –Not Supported 1 –Supported

Bit Range	Default	Access	Field Name and Description
28	1h	RO	**64-bit System Bus Support (sys_addr_64bit_support_v3)** This bit indicates whether the HC supports 64bit System Bus 0 –Not Supported 1 –Supported
27	-	-	**Reserved**
26	1h	RO	**Voltage Support 1.8V (volt1p8_support)** This bit indicates whether the HC supports 1.8V. 0 –Not Supported 1 –Supported
25	0h	RO	**Voltage Support 3.0V (volt3p0_support)** This bit indicates whether the HC supports 3.0V. 0 –Not Supported 1 –Supported
24	1h	RO	**Voltage Support 3.3V (volt3p3_support)** This bit indicates whether the HC supports 3.3V. 0 –Not Supported 1 –Supported
23	0h	RO	**Suspend / Resume Support (susp_resume_support)** This bit indicates whether the HC supports Suspend/Resume functionality. 0 –Not Supported 1 –Supported
22	0h	RO	**SDMA Support (sdma_support)** This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly. (SDMA Mode) 0 –Not Supported 1 –Supported

Bit Range	Default	Access	Field Name and Description
21	1h	RO	**High Speed Support (high_speed_support)** This bit indicates whether the HC and the Host System support High Speed mode. 0 –Not Supported 1 –Supported
20	-	-	**Reserved**
19	1h	RO	**ADMA2 Support (adma2_support)** ADMA2 Not Supported. Hardwired to 1.
18	0h	RO	**8 bit support for embedded device (extd_media_bus)** This bit indicates whether the Host Controller is capable of using 8-bit bus width mode. 0 –Not Supported 1 –Supported
17:16	0h	RO	**Max Block Length (max_blk_length)** This value indicates the maximum block size that the HD can read and write to the buffer in the HC. The buffer shall transfer this block size without wait cycles. Sizes can be defined as indicated below. 00 - 512 byte 01 - 1024 byte 10 - 2048 byte 11 - 4096 byte

Bit Range	Default	Access	Field Name and Description
15:8	C8h	RO	**Base Clock Frequency for SD Clock (base_clk_freq)** 1) 6-bit Base Clock Frequency This mode is supported by the Host Controller Version 1.00 and 2.00. Upper 2-bit is not effective and always 0. Unit values are1MHz. The supported clock rangeis 10MHz to 63MHz. 11xx xxxxb: Not supported 0011 1111b: 63MHz 0000 0010b: 2MHz 0000 0001b: 1MHz 0000 0000b: Get information via another method 2) 8-bit Base Clock Frequency This mode is supported by the Host Controller Version 3.00. Unit values are 1MHz. The supported clock range is 10MHz to 255MHz. FFh: 255MHz 02h: 2MHz 01h: 1MHz 00h: Get information via another method If the real frequency is 16.5MHz, the lager value shall be set 0001 0001b (17MHz) because the Host Driver use this value to calculate the clock divider value (Refer to the SDCLK Frequency Select in the Clock Control register.) and it shall not exceed upper limit of theSD Clock frequency. If these bits are all 0, the Host System has to get information via another method.
7	1h	RO	**Timeout Clock Unit (timeout_clk_unit)** This bit shows the unit of base clock frequency used to detect Data Timeout Error. 0 - KHz 1 - Mhz
6	-	-	**Reserved**
5:0	01h	RO	**Timeout Clock Frequency (timeout_clkf_req)** This bit shows the base clock frequency used to detect Data Timeout Error.Not 0 - 1Khz to 63Khz or 1Mhz to 63Mhz000000b - Get Information via another method.

Maximum Current Capabilities (maxcurrentcap) – Offset 48

Bit Range	Default	Access	Field Name and Description
62:24	-	-	**Reserved**
23:16	00h	RO	**Maximum Current for 1.8V (maxcurrent_1p8v)** Maximum Current for 1.8V 0 – Get value via another method 1 – 4mA 2 – 8mA 3 – 12mA ... 255 – 1020mA
15:8	-	-	**Reserved**
7:0	00h	RO	**Maximum Current for 3.3V (maxcurrent_3p3v)** Maximum Current for 3.3V0 – Get value via another method 1 – 4mA 2 – 8mA 3 – 12mA ... 255 – 1020mA

Force Event Register for AUTO CMD Error Status (ForceEventforAUTOCMDErrorStatus) – Offset 50

Bit Range	Default	Access	Field Name and Description
14:8	-	-	**Reserved**
7	0h	RO	**Force Event for Command Not Issued by AUTO CMD12 Error (forcecmd_ notissuedby_autocmd12_err)** 1 – Interrupt is generated0 – No Interrupt
6:5	-	-	**Reserved**
4	0h	RO	**Force Event for AUTO CMD Index Error (forceautocmdindexerr)** 1 – Interrupt is generated0 – No Interrupt
3	0h	RO	**Force Event for AUTO CMD End Bit Error (forceautocmdendbiterr)** 1 – Interrupt is generated0 – No Interrupt
2	0h	RO	**Force Event for AUTO CMD Timeout Error (forceautocmdcrcerr)** 1 – Interrupt is generated0 – No Interrupt
1	0h	RO	**Force Event for AUTO CMD Timeout Error (forceautocmdtimeouterr)** 1 – Interrupt is generated0 – No Interrupt
0	0h	RO	**Force Event for AUTO CMD12 Not Executed (forceautocmdnotexec)** 1 – Interrupt is generated0 – No Interrupt

Force Event Register for Error Interrupt Status (forceeventforerrintsts) – Offset 52

Bit Range	Default	Access	Field Name and Description
14:11	-	-	**Reserved**
10	0h	WO	**Force Event for Tuning Error (forcetuningerr)** 1 – Interrupt is generated 0 – No Interrupt

Bit Range	Default	Access	Field Name and Description
9	0h	WO	**Force Event for ADMA (forceadmaerr)** 1 – Interrupt is generated 0 – No Interrupt
8	0h	WO	**Force Event for Auto CMD Error (forceautocmderr)** 1 – Interrupt is generated 0 – No Interrupt
7	0h	WO	**Force Event for Current Limit (forcecurrlimerr)** 1 – Interrupt is generated 0 – No Interrupt
6	0h	WO	**Force Event for Data End Bit Error (forcedatendbiterr)** 1 – Interrupt is generated 0 – No Interrupt
5	0h	WO	**Force Event for Data CRC Error (forcedatcrcerr)** 1 – Interrupt is generated 0 – No Interrupt
4	0h	WO	**Force Event for Data Timeout Error (forcedattimeouterr)** 1 – Interrupt is generated 0 – No Interrupt
3	0h	WO	**Force Event for Command Index Error (forcecmdindexerr)** 1 – Interrupt is generated 0 – No Interrupt
2	0h	WO	**Force Event for Command End Bit Error (forcecmdendbiterr)** 1 – Interrupt is generated 0 – No Interrupt
1	0h	WO	**Force Event for Command CRC Error (forcecmdcrcerr)** 1 – Interrupt is generated 0 – No Interrupt

Bit Range	Default	Access	Field Name and Description
0	0h	WO	**Force Event for CMD Timeout Error (forcecmdtimeouterr)** 1 – Interrupt is generated 0 – No Interrupt

ADMA Error Status (admaerrsts) – Offset 54

When the ADMA Error interrupt occur, this register holds the ADMA State in ADMA Error States field and ADMA System Address holds address around the error descriptor

Bit Range	Default	Access	Field Name and Description
6:3	-	-	**Reserved**
2	0h	RO	**ADMA Length Mismatch Error (admaerrsts_admalenmismatcherr)** This error occurs in the following 2 cases. While Block Count Enable being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. Total data length can not be divided by the block length. 1 - Error 0 - No error
1:0	0h	RO	**ADMA Error State (admaerrsts_admaerrorstate)** This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates 10 because ADMA never stops in this state. D01 – D00 : ADMA Error State when error occurred Contents of SYS_SDR register 00 - ST_STOP (Stop DMA) Points to next of the error descriptor 01 - ST_FDS (Fetch Descriptor) Points to the error descriptor 10 - Never set this state (Not used) 11 - ST_TFR (Transfer Data) Points to the next of the error descriptor

ADMA System Address Register 1 (admasysaddr01) – Offset 58

This register contains the physical address used for ADMA data transfer

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**ADMA System Address Register (adma_32bit_sysaddress)** This register holds byte address of executing command of the Descriptor table. 32-bit Address Descriptor uses lower 32-bit of this register.

ADMA System Address Register 2 (admasysaddr2) – Offset 5c

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW	**ADMA System Address (adma_64bit_sysaddress2)** This register holds byte address of executing command of the Descriptor table. 64-bit Address Descriptor uses Upper 32-bit of this register.

Preset Value Register for Initialization (presetvalue0) – Offset 60

Bit Range	Default	Access	Field Name and Description
15:14	0h	RO	**Driver Strength Select Value (DriverStrengthSelectValue)** Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 11b Driver Type D is Selected 10b Driver Type C is Selected 01b Driver Type A is Selected 00b Driver Type B is Selected
13:11	-	-	**Reserved**
10	0h	RO	**Clock Generator Select Value (ClockGeneratorSelectValue)** This bit is effective when Host Controller supports programmable clock generator. 1 Programmable Clock Generator 0 Host Controller Ver2.00 Compatible Clock Generator

Bit Range	Default	Access	Field Name and Description
9:0	004h	RO	**SDCLK Frequency Select Value (SDCLKFrequencySelectValue)** 10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.

Preset Value Register for Default Speed (presetvalue1) – Offset 62

Same definition as Preset Value Register for Initialization.

Preset Value Register for High Speed (presetvalue2) – Offset 64

Same definition as Preset Value Register for Initialization.

Preset Value Register for SDR12 (presetvalue3) – Offset 66

Same definition as Preset Value Register for Initialization.

Preset Value Register for SDR25 (presetvalue4) – Offset 68

Same definition as Preset Value Register for Initialization.

Preset Value Register for SDR50 (presetvalue5) – Offset 6a

Same definition as Preset Value Register for Initialization.

Preset Value Register for SDR104 (presetvalue6) – Offset 6c

Same definition as Preset Value Register for Initialization.

Preset Value Register for DDR50 (presetvalue7) – Offset 6e

Same definition as Preset Value Register for Initialization.

Slot Interrupt Status (slotintrsts) – Offset fc

This register is used to read the interrupt signal for each slot.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
14:8	-	-	**Reserved**
7:1	00h	RO	**Slot Interrup Status (sdhchostif_slotintrstsslot1to8)** These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot.
0	0h	RO	**Slot Interrup Status (sdhchostif_slotintrstsslot0)** These status bits indicate the logical OR of Interrupt signal and Wakeup signal for each slot.

SDXC PCI Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID and Vendor ID (DEVVENDID)	XXXX8086h
4h	4	Status and Command (STATUSCOMMAND)	100000h
8h	4	Rev ID & Class Code (REVCLASSCODE)	80501XXh
ch	4	Cache Line & Latency & Header Type & BIST (CLLATHEADERBIST)	0h
10h	4	Base Address Low (BAR)	4h
14h	4	Base Address Register high (BAR_HIGH)	0h
18h	4	Base Address Register1 (BAR1)	4h
1ch	4	(BAR1_HIGH)	0h
34h	4	Capabilities Pointer (CAPABILITYPTR)	80h
3ch	4	Interrupt Line (INTERRUPTREG)	0h
80h	4	Power Management Capability ID Register (POWERCAPID)	39001h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
84h	4	Power Management Control and Status (PMECTRLSTATUS)	8h
98h	4	SW LTR update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)	8041h
a0h	4	D0I3 Max Power & PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)	290800h
b0h	4	General Purpose Read Write 1 (GEN_REGRW1)	0h
b4h	4	General Purpose Read Write 2 (GEN_REGRW2)	0h
b8h	4	General Purpose Read Write 3 (GEN_REGRW3)	0h
bch	4	General Purpose Read Write 4 (GEN_REGRW4)	0h
c0h	4	General Purpose Input (GEN_INPUT_REG)	0h

Device ID and Vendor ID (DEVVENDID) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:16	See Description	RO	**Device Identification (DEVICEID)** Identifies the device. Refer to the Device and Revision ID Table in Volume 1 for default value.
15:0	8086h	RO	**Vendor Identification (VENDORID)** Intel default value is 8086h

Status and Command (STATUSCOMMAND) – Offset 4

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29	0h	RW/1C	**Received Master Abort (RMA)** The software writes a 1 to this bit to clear it.
28	0h	RW/1C	**Received Target Abort (RTA)** The software writes a 1 to this bit to clear it.
27:21	-	-	**Reserved**
20	1h	RO	**Capabilities List (CAPLIST)** 1 Indicates that the controller contains a capabilitiespointer list.
19	0h	RO	**Interrupt Status (INTR_STATUS)** This bit reflects state of interrupt in the device.
18:11	-	-	**Reserved**
10	0h	RW	**Interrupt Disable (INTR_DISABLE)** Setting this bit disables INTx assertion.
9	-	-	**Reserved**
8	0h	RW	**SERR Enable (SERR_ENABLE)**
7:3	-	-	**Reserved**
2	0h	RW	**Bus Master Enable (BME)** 0 = the Bridge does not generate any new upstreamtransaction on IOSF as a master.
1	0h	RW	**Memory Space Enable (MSE)** 0 = Disabled. No downstream traffic from the bridge is available.
0	-	-	**Reserved**

Rev ID & Class Code (REVCLASSCODE) – Offset 8

Bit Range	Default	Access	Field Name and Description
31:8	080501h	RO	**Class Code (CLASS_CODES)** The Class Code register is read-only and is used to identify the genericfunction of the device, and in some cases, a specific register-levelprogramming interface. The register is broken into 3 Byte-size fields. - The upper Byte (at offset 0Bh) is a base class code that broadlyclassifies the type of function the device performs. - The middle Byte (at offset 0Ah) is a sub-class code that identifiesmore specifically the function of the device. - The lower Byte (at offset 09h) identifies a specific register-levelprogramming interface (if any) so that device independentsoftware can interact with the device. This register is tied to a strap at the top level.
7:0	See Description	RO	**Rev ID (RID)** Revision ID identifies the revision of particular PCI device. Refer to the Device and Revision ID Table in Volume 1 for default value

Cache Line & Latency & Header Type & BIST (CLLATHEADERBIST) – Offset c

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0h	RO	**Multi-Function Device (MULFNDEV)** This bit is 0 or 1 depending upon the value assigned o thetop level strap.
22:16	00h	RO	**Header Type (HEADERTYPE)** Implements Type 0 Configuration header.
15:8	00h	RO	**Latency Timer (LATTIMER)** This register is implemented as R/W with default as 0.

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**Cacheline Size (CACHELINE_SIZE)** This register is implemented as R/W with default as 0.

Base Address Low (BAR) – Offset 10

Bit Range	Default	Access	Field Name and Description
31:12	00000h	RW	**Base Address (BASEADDR)** Base address of the OCP fabric memory space.
11:4	00h	RO	**Size Indicator (SIZEINDICATOR)** Size Indicator Read Only. The size of this register depends on the size of the memory space.
3	0h	RO	**Prefetchable (PREFETCHABLE)** Indicates that this BAR is not prefetchable.
2:1	2h	RO	**Type (TYPE)** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range. If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range.
0	0h	RO	**Memory Space Indicator (MESSAGE_SPACE)** 0 indicates this BAR is present in the memory space.

Base Address Register high (BAR_HIGH) – Offset 14

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Base Address High (BASEADDR_HIGH)**

Base Address Register1 (BAR1) – Offset 18

Bit Range	Default	Access	Field Name and Description
31:12	00000h	RW	**Base Address 1 (BASEADDR1)**
11:4	00h	RO	**Size Indicator (SIZEINDICATOR1)** Always is 0 as minimum size is 4K
3	0h	RO	**Prefetchable (PREFETCHABLE1)** Indicates that this BAR is not prefetchable.
2:1	2h	RO	**Type (TYPE1)**
0	0h	RO	**Base Address Register1 (MESSAGE_SPACE1)** This field is present if BAR1 is enabled through private configuration space.

(BAR1_HIGH) – Offset 1c

BAR1 -Base Address Register1 High

Capabilities Pointer (CAPABILITYPTR) – Offset 34

CAPABILITYPTR - Capabilities Pointer

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	80h	RO	**Capabilities Pointer (CAPPTR_POWER)**

Interrupt Line (INTERRUPTREG) – Offset 3c

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO	**Maximum Latency (MAX_LAT)** Value of 0 indicates device has no major requirements for the settings of latencytimers
23:16	00h	RO	**Minimum Latency (MIN_GNT)** Value of 0 indicates device has no major requirements for the settings of latencytimers
15:12	-	-	**Reserved**
11:8	0h	RO	**Interrupt Pin (INTPIN)** Interrupt Pin Value in this register is reflected from the IPIN value inthe private configuration space. For a single function device, this ideally is INTA.
7:0	00h	RW	**Interrupt Line (INTLINE)** It is used to communicate to software, the interrupt line to which the interrupt pinis connected.

Power Management Capability ID Register (POWERCAPID) – Offset 80

Bit Range	Default	Access	Field Name and Description
31:27	00h	RO	**(PMESUPPORT)** This 5-bit field indicates the power states in which the function can assert the PME#. A value of 0b for any bit indicates that the function is not capable of asserting thePME# signal in that power state. bit 27 = 1: PME# can be asserted from D0 bit28 = 1: PME# can be asserted from D1. bit 29 = 1: PME# can be asserted from D2. bit30 = 1:PME# can be asserted from D3hot bit 31 = 1:PME# can be asserted from D3cold.

Bit Range	Default	Access	Field Name and Description
26:19	-	-	**Reserved**
18:16	3h	RO	**Version (VERSION)** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	90h	RO	**Next Capability (NXTCAP)** Points to the next capability structure. This points to NULL if eitherENABLE_PCI_IDLE_CAP is 0 or if Disable PCI Device Idle capability bit is set as 1in the private space. Else this points to PCI Device Idle capability structure atoffset 90h
7:0	01h	RO	**Power Management Capability (POWER_CAP)** Indicates this is power management capability.

Power Management Control and Status (PMECTRLSTATUS) – Offset 84

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0h	RW	**PME Enable (PMEENABLE)** 1: Enables the function to assert PME#. 0: PME# message on Sideband is disabled.
7:4	-	-	**Reserved**
3	1h	RO	**(NO_SOFT_RESET)** This bit indicates that devices transitioning from D3hot to D0 because ofPowerstate commands do not perform an internal reset.Configuration Context is preserved.
2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1:0	0h	RW	**Power State (POWERSTATE)** This field is used both to determine the current power state and to set a newpower state.The values are: 00 D0 state 11 D3HOT state

SW LTR update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) – Offset 98

Bit Range	Default	Access	Field Name and Description
31:4	0000804h	RO	**(SW_LAT_DWORD_OFFSET)** This register contains the location pointer to the SW LTR register in MMIO space,as an offset from the specified BAR.
3:1	0h	RO	**Bar Number (SW_LAT_BAR_NUM)** Indicates that the SW LTR update MMIO location is always at BAR0.
0	1h	RO	**Valid (SW_LAT_VALID)** This value is reflected from the SW LTR valid strap at the top level.

D0I3 Max Power & PG Config (D0I3_MAX_POW_LAT_PG_CONFIG) – Offset a0

Bit Range	Default	Access	Field Name and Description
30:22	-	-	**Reserved**
21	1h	RW	**Hardware Autonomous Enable (HAE)** If set, then the PGCB may request a PGwhenever it is idle.
20	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
19	1h	RW	**Sleep Enable (SLEEP_EN)** if clear, then IP will never asset Sleep to the retention flops. Ifset, then IP may assert Sleep during PG'ing.
18	0h	RW	**PG Enable (PGE)** If clear, then IP will never request a PG. If set, then IP may requestPG when proper conditions are met.
17	0h	RW	**I3 Enable (I3_ENABLE)** if set, then IP will PG when idle and the D0i3 register (in PGCB) isset. If this bit is set, the IP will not PG unless the IPs D0i3 control bit ='1'. Bit [5] isnot required to be set when this bit is set.
16	1h	RW	**PMC Request Enable (PMCRE)** When bits [1:0] = '11', power gating is enabled whenever either the D3register or the D0i3 register is set.
15:13	-	-	**Reserved**
12:10	2h	RW/O	**Power On Latency Scale (POW_LAT_SCALE)** Support for codes 010 (1us) or 011 (32us) for Exit Latency Scale (1us -) 32mstotal span) only.
9:0	000h	RW/O	**Power On Latency value (POW_LAT_VALUE)** This value is written by BIOS to communicate to the Driver.

General Purpose Read Write 1 (GEN_REGRW1) – Offset b0

This register is for general purpose read and write.

General Purpose Read Write 2 (GEN_REGRW2) – Offset b4

This register is for general purpose read and write.

General Purpose Read Write 3 (GEN_REGRW3) – Offset b8

This register is for general purpose read and write.

General Purpose Read Write 4 (GEN_REGRW4) – Offset bc

This register is for general purpose read and write.

General Purpose Input (GEN_INPUT_REG) – Offset c0

This register is a general Purpose Input register.

SMBus Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	Vendor ID (VID)	8086h
2h	2	Device ID (DID)	XXXXh
4h	2	Command (CMD)	0h
6h	2	Device Status (DS)	280h
8h	1	Revision ID (RID)	0h
9h	1	Programming Interface (PI)	0h
ah	1	Sub Class Code (SCC)	5h
bh	1	Base Class Code (BCC)	Ch
10h	4	SMBus Memory Base Address_31_0 (SMBMBAR_31_0)	4h
14h	4	SMBus Memory Base Address_63_32 (SMBMBAR_63_32)	0h
20h	4	SMB Base Address (SBA)	1h
2ch	2	Subsystem Vendor Identifiers (SVID)	0h
2eh	2	Subsystem Identifiers (SID)	0h
3ch	1	Interrupt Line (INTLN)	0h
3dh	1	Interrupt Pin (INTPN)	1h
40h	1	Host Configuration (HCFG)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
50h	4	TCO Base Address (TCOBASE)	1h
54h	4	TCO Control (TCOCTL)	0h
64h	4	Host SMBus Timing (HTIM)	0h
80h	4	SMBus Power Gating (SMBSM)	40000h

Vendor ID (VID) – Offset 0

Vendor ID

Bit Range	Default	Access	Field Name and Description
15:0	8086h	RO	**Vendor ID (VID)** Value indicates Intel as the vendor

Device ID (DID) – Offset 2

Bit Range	Default	Access	Field Name and Description
15:0	See Description	RO/V	**Device ID (DID)** Indicates the value assigned to the PCH SMBus controller. Refer to the Device and Revision ID Table in Volume 1 for default setting.

Command (CMD) – Offset 4

Command

Bit Range	Default	Access	Field Name and Description
14:11	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
10	0b	RW	**Interrupt Disable (INTD)** 1 = Disables SMBus to assert its PIRQB# signal. Defaults to 0.
9	0b	RO	**Fast Back to Back Enable (FBE)** Reserved as 0. Read Only.
8	0b	RW	**SERR# Enable (SERRE)** 1 = Enables SERR# generation
7	0b	RO	**Wait Cycle Control (WCC)** Reserved as 0. Read Only.
6	0b	RW	**Parity Error Response (PER)** 1 = Sets Detected Parity Error bit when parity error is detected
5	0b	RO	**VGA Palette Snoop (VGAPS)** Reserved as 0. Read Only.
4	0b	RO	**Postable Memory Write Enable (PMWE)** Reserved as 0. Read Only.
3	0b	RO	**Special Cycle Enable (SCE)** Reserved as 0. Read Only.
2	0b	RO	**Bus Master Enable (BME)** Reserved as 0. Read Only.
1	0b	RW	**Memory Space Enable (MSE)** 1= Enables memory mapped config space.
0	0b	RW	**I/O Space Enable (IOSE)** 1= enables access to the SM Bus I/O space registers as defined by the Base Address Register.

Device Status (DS) – Offset 6

Device Status

Bit Range	Default	Access	Field Name and Description
15	0b	RW/1C	**Detected Parity Error (DPE)** 1 = Parity error detected
14	0b	RW/1C	**Signaled System Error (SSE)** 1 = System error detected
13	0b	RO	**Received Master Abort (RMA)** Reserved as 0.
12	0b	RO	**Received Target Abort (RTA)** Reserved as '0'.
11	0b	RW/1C	**Signaled Target-Abort Status (STA)** Reserved as 0.
10:9	01b	RO	**DEVSEL# Timing Status (DEVT)** This 2-bit field defines the timing for DEVSEL# assertion. These read only bits indicate the Intel PCH's DEVSEL# timing when performing a positive decode. Note: Intel PCH generates DEVSEL# with medium time.
8	0b	RO	**Data Parity Error Detected (DPED)** Reserved as 0.
7	1b	RO	**Fast Back-to-Back Capable (FBC)** Reserved as '1'.
6	0b	RO	**User Definable Features (UDF)** Reserved as 0.
5	0b	RO	**66 MHz Capable (C_66M)** Reserved as 0.
4	0b	RO	**Capabilities List Indicator (CLI)** Hardwired to 0 because there are no capability list structures in this function.
3	0b	RO	**Interrupt Status (INTS)** This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the command register.
2:0	-	-	**Reserved**

Revision ID (RID) – Offset 8

Revision ID

Bit Range	Default	Access	Field Name and Description
7:0	See Description	RO	**Revision ID (RID)** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

Programming Interface (PI) – Offset 9

Programming Interface

Bit Range	Default	Access	Field Name and Description
7:0	00h	RO	**Programming Interface (PI)** No programming interface defined.

Sub Class Code (SCC) – Offset a

Sub Class Code

Bit Range	Default	Access	Field Name and Description
7:0	05h	RO	**Sub Class Code (SCC)** A value of 05h indicates that this device is a SM Bus serial controller.

Base Class Code (BCC) – Offset b

Base Class Code

Bit Range	Default	Access	Field Name and Description
7:0	0Ch	RO	**Base Class Code (BCC)** A value of 0Ch indicates that this device is a serial controller

SMBus Memory Base Address_31_0 (SMBMBAR_31_0) – Offset 10

SMBus Memory Base Address_31_0

Bit Range	Default	Access	Field Name and Description
31:8	000000h	RW	**Base Address (BA)** Provides the 32 byte system memory base address for the Intel PCH SMB logic.
7:4	0h	RO	**Hardwired_0 (HARDWIRED_0)** Hardwired to 0.
3	0b	RO	**Prefetchable (PREF)** Hardwired to 0. Indicated that SMBMBAR is not pre- fetchable
2:1	10b	RO	**Address Range (ADDRNG)** Indicates that this SMBMBAR can be located anywhere in 64 bit address space
0	0b	RO	**Memory Space Indicator (MSI)** Indicates that the SMB logic is memory mapped.

SMBus Memory Base Address_63_32 (SMBMBAR_63_32) – Offset 14

SMBus Memory Base Address_63_32

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Base Address (BA)** Bits 63-32 of SMbus Memory Base Address

SMB Base Address (SBA) – Offset 20

SMB Base Address

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:5	0000000 0000b	RW	**Base Address (BA)** Provides the 32 byte t system I/O base address for the SMB logic.
4:1	-	-	**Reserved**
0	1b	RO	**IO Space Indicator (IOSI)** This read-only bit always is 1, indicating that the SMB logic is I/O mapped.

Subsystem Vendor Identifiers (SVID) – Offset 2c

Subsystem Vendor ID

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW/O	**Subsystem Vendor ID (SVID)** BIOS sets the value in this register to identify the Subsystem Vendor ID. The SMBus SVID register, in combination with the SMBus Subsystem ID register, enables the operating system to distinguish each subsystem from the others. Note: The software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

Subsystem Identifiers (SID) – Offset 2e

Subsystem ID

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW/O	**Subsystem ID (SID)** BIOS can write to this register to identify the Subsystem ID. The SID register, in combination with the SVID, enable the operating system to distinguish each subsystem from other(s). Note: The software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

Interrupt Line (INTLN) – Offset 3c

Interrupt Line

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**Interrupt Line (INTLN)** This data is not used by the hardware. It is to communicate to software the interrupt line that the interrupt pin is connected to PIRQB#.

Interrupt Pin (INTPN) – Offset 3d

Bit Range	Default	Access	Field Name and Description
7:0	01h	RO	**Interrupt Pin (INTPN)** This defines the interrupt pin to be used by the SMBus controller. Bits : Pins 0h : No Interrupt 1h : INTA# 2h : INTB# 3h : INTC# 4h : INTD# 5h-Fh : Reserved

Host Configuration (HCFG) – Offset 40

Host Configuration

Bit Range	Default	Access	Field Name and Description
6:5	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
4	0b	RW/1L	**SPD Write Disable (SPDWD)** When this bit is set to 1, writes to SMBus addresses 50h – 57h are disabled.Note: This bit is R/WO and will be reset on PLTRST# assertion. This bit should be set by BIOS to'1'. Software can only program this bit when both the START bitand Host Busy bit are '0'; otherwise, the write may result inundefined behavior.
3	0b	RW	**SSRESET (SSRESET)** Soft SMBUS Reset: When this bit is 1, the SMbus state machine and logic in PCH is reset. The HW will reset this bit to 0 when reset operation is completed.
2	0b	RW	**I2C_EN (I2CEN)** When this bit is 1, the Intel PCH is enabled to communicate with I2C devices. This will change the formatting of some commands. When this bit is 0, behavior is for SMBus.
1	0b	RW	**SMB_SMI_EN (SSEN)** When this bit is set, any source of an SMB interrupt will instead be routed to generate an SMI#.
0	0b	RW	**HST_EN (HSTEN)** When set, the SMB Host Controller interface is enabled to execute commands. The HST_INT_EN bit needs to be enabled in order for the SMB Host Controller to interrupt or SMI#. Additionally, the SMB Host Controller will not respond to any new requests until all interrupt requests have been cleared.

TCO Base Address (TCOBASE) – Offset 50

TCO Base Address

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:5	0000000 0000b	RW/L	**TCO Base Address (TCOBA)** Provides the 32 bytes of I/O space for TCO logic, mappable anywhere in the 64k I/O space on 32-byte boundaries.
4:1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	1b	RO	**I/O Space (IOS)** Indicates an I/O Space

TCO Control (TCOCTL) – Offset 54

TCO Control

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8	0b	RW	**TCO Base Enable (TCO_BASE_EN)** When set, decode of the I/O range pointed to by the TCO base register is enabled.
7:1	-	-	**Reserved**
0	0b	RW/O	**TCO Base Lock (TCO_BASE_LOCK)** When set to 1, this bit locks down the TCO Base Address Register (TCOBASE) at offset 50h. The Base Address Field becomes read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset.

Host SMBus Timing (HTIM) – Offset 64

BIOS may need to program this register.

SMBus Power Gating (SMBSM) – Offset 80

Bit Range	Default	Access	Field Name and Description
30:19	-	-	**Reserved**
18	1b	RW	**SMBus Dynamic Clock Gating (PGCBDCGDIS)** Setting this bit will disable the SMBus dynamic clock gating.

Bit Range	Default	Access	Field Name and Description
17:0	-	-	**Reserved**

SMBus I/O and Memory Mapped I/O Registers

The SMBus registers can be accessed through I/O BAR or Memory BAR registers in PCI configuration space. The offsets are the same for both I/O and Memory Mapped I/O registers.

Summary of Bus:, Device:, Function: (IO)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	1	Host Status Register Address (HSTS)	0h
2h	1	Host Control Register (HCTL)	0h
3h	1	Host Command Register (HCMD)	0h
4h	1	Transmit Slave Address Register (TSA)	0h
5h	1	Data 0 Register (HD0)	0h
6h	1	Data 1 Register (HD1)	0h
7h	1	Host Block Data (HBD)	0h
8h	1	Packet Error Check Data Register (PEC)	0h
9h	1	Receive Slave Address Register (RSA)	44h
ah	2	Slave Data Register (SD)	0h
ch	1	Auxiliary Status (AUXS)	0h
dh	1	Auxiliary Control (AUXC)	0h
eh	1	SMLINK_PIN_CTL Register (SMLC)	4h
fh	1	SMBUS_PIN_CTL Register (SMBC)	4h
10h	1	Slave Status Register (SSTS)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
11h	1	Slave Command Register (SCMD)	0h
14h	1	Notify Device Address Register (NDA)	0h
16h	1	Notify Data Low Byte Register (NDLB)	0h
17h	1	Notify Data High Byte Register (NDHB)	0h

Host Status Register Address (HSTS) – Offset 0

All status bits are set by hardware and cleared by the software writing a one to the particular bit position. Writing a zero to any bit position has no affect.

Bit Range	Default	Access	Field Name and Description
7	0b	RW/1C	**BYTE_DONE_STS (BDS)** This bit will be set to 1 when the host controller has received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands) when the 32-byte buffer is not being used. Note that this bit will be set, even on the last byte of the transfer. Software clears the bit by writing a 1 to the bit position. This bit has no meaning for block transfers when the 32- byte buffer is enabled. Note: When the last byte of a block message is received, the host controller will set this bit. However, it will not immediately set the INTR bit (bit 1 in this register). When the interrupt handler clears the BYTE_DONE_ STS bit, the message is considered complete, and the host controller will then set the INTR bit (and generate another interrupt). Thus, for a block message of n bytes, the Intel PCH will generate n+1 interrupts. The interrupt handler needs to be implemented to handle these cases.
6	0b	RW/1C	**In Use Status (IUS)** After a full PCI reset, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the host controller. This bit has no other effect on the hardware, and is only used as semaphore among various independent software threads that may need to use the Intel PCHs SMBus logic.
5	0b	RW/1C	**SMBALERT_STS (SMSTS)** Intel PCH sets this bit to a 1 to indicates source of the interrupt or SMI# was the SMBAlert# signal. Software resets this bit by writing a 1 to this location. This bit should also be cleared by RSMRST# (but not PLTRST#).

Bit Range	Default	Access	Field Name and Description
4	0b	RW/1C	**Failed (FAIL)** When set, this indicates that the source of the interrupt or SMI# was a failed bus transaction. This is set in response to the KILL bit being set to terminate the host transaction.
3	0b	RW/1C	**Bus Error (BERR)** When set, this indicates the source of the interrupt or SMI# was a transaction collision.
2	0b	RW/1C	**Device Error (DERR)** When set, this indicates that the source of the interrupt or SMI# was due one of the following: Illegal Command Field Unclaimed Cycle (host initiated) Host Device Time-out Error. CRC Error
1	0b	RW/1C	**Interrupt (INTR)** When set, this indicates that the source of the interrupt or SMI# was the successful completion of its last command.
0	0b	RW/1C	**Host Busy (HBSY)** A 1 indicates that the Intel PCH is running a command from the host interface. No SMB registers should be accessed while this bit is set. Exception: The BLOCK DATA REGISTER can be accessed when this bit is set ONLY when the SMB_CMD bits (in Host control register) are programmed for Block command or I2C Read command. This is necessary in order to check the DONE_STS bit.

Host Control Register (HCTL) – Offset 2

Note: A read to this register will clear the pointer in the 32-byte buffer.

Bit Range	Default	Access	Field Name and Description
7	0b	RW	**PEC_EN (PEC_EN)** When set to 1, this bit causes the host controller to perform the SMBus transaction with the Packet Error Checking phase appended. For writes, the value of the PEC byte is transferred from the PEC Register. For reads, the PEC byte is loaded in to the PEC Register. When this bit is cleared to 0, the SMBus host controller does not perform the transaction with the PEC phase appended. This bit must be written prior to the write in which the START bit is set.

Bit Range	Default	Access	Field Name and Description
6	0b	RW	**START (START)** This write-only bit is used to initiate the command described in the SMB_CMD field. All registers should be setup prior to writing a 1 to this bit position. This bit always reads zero. The HOST_BUSY bit in the Host Status register (offset 00h) can be used to identify when the Intel PCH has finished the command.
5	0b	RW	**LAST_BYTE (LAST_BYTE)** This bit is used for I2C Read commands.Software sets this bit to indicate that the next byte will be the last byte to be received for the block. This causes the PCH to send a NACK (instead of an ACK) after receiving the last byte.Note: This bit may be set when the TCO timer causes the SECOND_TO_STS bit to be set. SW should clear the LAST_BYTE bit (if it is set) before starting any new command.Note: In addition to I2C Read Commands, the LAST_BYTE bit will also cause Block Read/Write cycles to stop prematurely (at the end of the next byte).
4:2	000b	RW	

Bit Range	Default	Access	SMB_CMD (SMB_CMD) Field Name and Description
			As shown by the bit encoding below, indicates which command the PCH is to perform. If enabled, the Intel PCH will generate an interrupt or SMI# when the command has completed. If the value is for a non-supported or reserved command, the PCH will set the device error(DEV_ERR) status bit and generate an interrupt when the START bit is set. The PCH will perform no command, and will not operate until DEV_ERR is cleared.Val. 000 - Quick: The slave address and read/write value (bit 0) are stored in the tx slave address register. 001 - Byte: This command uses the transmit slave address and command registers. Bit 0 of the slave address register determines if this is a read or write command. 010 - Byte Data: This command uses the transmit slave address, command, and DATA0 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, the DATA0 register will contain the read data. 011 - Word Data: This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes the DATA0 and DATA1 registers will contain the read data. 100 - Process Call: This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. After the command completes, the DATA0 and DATA1 registers will contain the read data. 101 - Block: This command uses the transmit slave address, command, and DATA0 registers, and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block reads, the count is received and stored in the DATA0 register. Bit 0 of the slave address register selects if this is a read or write command. For writes, data is retrieved from the first n (where n is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. 110 - I2C Read: This command uses the transmit slave address, command, DATA0, DATA1 registers, and the Block Data Byte register. The read data is stored in the Block Data Byte register. The Intel PCH will continue reading data until the NAK is received. 111 - Block-Process: This command uses the transmit slave address, command, DATA0 and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block read, the count is received and stored in the DATA0 register. Bit 0 of the slave address register always indicate a write command. For writes, data is retrieved from the first m (where m is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. Note: E32B bit in the Auxiliary Control Register must be set for this command to work.

Bit Range	Default	Access	Field Name and Description
1	0b	RW	**KILL (KILL)** When set, kills the current host transaction taking place, sets the FAILED status bit, and asserts the interrupt (or SMI#) selected by the SMB_INTRSEL field. This bit, once set, must be cleared to allow the SMB Host Controller to function normally.
0	0b	RW	**INTREN (INTREN)** Enable the generation of an interrupt or SMI# upon the completion of the command.

Host Command Register (HCMD) – Offset 3

Host Command Register

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**Host Command Register (HCMD)** This eight bit field is transmitted by the host controller in the command field of the SMB protocol during the execution of any command.

Transmit Slave Address Register (TSA) – Offset 4

This register is transmitted by the host controller in the slave address field of the SMB protocol. This is the address of the target.

Bit Range	Default	Access	Field Name and Description
7:1	0000000b	RW	**ADDRESS (ADDR)** 7-bit address of the targeted slave. Note: Writes to TSA values of A0h - AEh are blocked depending on the setting of the SPD write disable bit in HCFG - HostConfiguration.
0	0b	RW	**RW (RW)** Direction of the host transfer. 1 = read, 0 = write

Data 0 Register (HD0) – Offset 5

Data 0 Registe

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**DATA0/COUNT (DATA0_COUNT)** This field contains the eight bit data sent in the DATA0 field of the SMB protocol. For block write commands, this register reflects the number of bytes to transfer. This register should be programmed to a value between 1 and 32 for block counts. A count of 0 or a count above 32 will result in unpredictable behavior. The host controller does not check or log illegal block counts.

Data 1 Register (HD1) – Offset 6

Data 1 Register

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**DATA1 (DATA1)** This eight bit register is transmitted in the DATA1 field of the SMB protocol during the execution of any command.

Host Block Data (HBD) – Offset 7

Host Block Data

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**Block Data (BDTA)** This is either a register, or a pointer into a 32- byte block array, depending upon whether the E32B bit is set in the Auxiliary Control register. When the E32B bit is cleared, this is a register containing a byte of data to be sent on a block write or read from on a block read, just as it behaved on the INTEL PCH. When the E32B bit is set, reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array, which is reset to 0 by reading the HCTL register (offset 02h). The index pointer then increments automatically upon each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0. When the E2B bit is set, for writes, software will write up to 32-bytes to this register as part of the setup for the command. After the Host Controller has sent the Address, Command, and Byte Count fields, it will send the bytes in the SRAM pointed to by this register. When the E2B bit is cleared for writes, software will place a single byte in this register. After the host controller has sent the address, command, and byte count fields, it will send the byte in this register. If there is more data to send, software will write the next series of bytes to the SRAM pointed to by this register and clear the DONE_STS bit. The controller will then send the next byte. During the time between the last byte being transmitted to the next byte being transmitted, the controller will insert wait-states on the interface. When the E2B bit is set for reads, after receiving the byte count into the Data0 register, the first series of data bytes go into the SRAM pointed to by this register. If the byte count has been exhausted or the 32-byte SRAM has been filled, the controller will generate an SMI# or interrupt (depending on configuration) and set the DONE_STS bit. Software will then read the data. During the time between when the last byte is read from the SRAM to when the DONE_STS bit is cleared, the controller will insert waitstates on the interface.

Packet Error Check Data Register (PEC) – Offset 8

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**PEC_DATA (PEC_DATA)** This 8-bit register is written with the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software. Software must ensure that the INUSE_STS bit is properly maintained to avoid having this field over-written by a write transaction following a read transaction.

Receive Slave Address Register (RSA) – Offset 9

Receive Slave Address Register

Bit Range	Default	Access	Field Name and Description
6:0	1000100b	RW	**SLAVE_ADDR[6:0] (SA_6_0)** This field is the slave address that the Intel PCH decodes for read and write cycles. The default is not 0 so that it can respond even before the CPU comes up (or if the CPU is dead). This register is reset by RSMRST#, but not by PLTRST#.

Slave Data Register (SD) – Offset a

Slave Data Register

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RO/V	**SLAVE_DATA[15:0] (SD_15_0)** This field is the 16-bit data value written by the external SMBus master. The CPU can then read the value from this register. This register is reset by RSMRST#, but not by PLTRST#. SLAVE_DATA[7:0] corresponds to the Data Message Byte 0 at Slave Write Register 4 in the table. SLAVE_[15:8] corresponds to the Data Message Byte 1 at Slave Write Register 5 in the table.

Auxiliary Status (AUXS) – Offset c

All bits in this register are in the core well.

Bit Range	Default	Access	Field Name and Description
6:1	-	-	**Reserved**
0	0b	RW/1C	**CRC Error (CRCE)** This bit is set if a received message contained a CRC error. When this bit is set, the DERR bit of the host status register will also be set. This bit will be set by the controller if a software abort occurs in the middle of the CRC portion of the cycle or an abort happens after Intel PCH has received the final data bit transmitted by external slave.

Auxiliary Control (AUXC) – Offset d

All bits in this register are in the resume well.

Bit Range	Default	Access	Field Name and Description
6:2	-	-	**Reserved**
1	0b	RW	**Enable 32-byte Buffer (E32B)** When set, the Host Block Data register is a pointer into a 32-byte buffer, as opposed to a single register. This enables the block commands to transfer or receive up to 32-bytes before the Intel PCH generates an interrupt.
0	0b	RW	**Automatically Append CRC (AAC)** When set, the Intel PCH will automatically append the CRC. This bit must not be changed during SM Bus transactions, or undetermined behavior will result. It should be programmed only once during the lifetime of the function.

SMLINK_PIN_CTL Register (SMLC) – Offset e

Note: This register is in the resume well and is reset by RSMRST#

Bit Range	Default	Access	Field Name and Description
6:3	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
2	1b	RW	**SMLINK_CLK_CTL (SMLINK_CLK_CTL)** 0 = Intel PCH will drive the SMLINK[0] pin low, independent of what the other SMLINK logic would otherwise indicate for the SMLINK(0) pin. 1 = The SMLINK[0] pin is Not overdriven low. The other SMLINK logic controls the state of the pin.
1	0b	RO/V	**SMLINK[1]_CUR_STS (SMLINK1_CUR_STS)** This bit has a default value that is dependent on an external signal level. This returns the value on the SMLINK[1] pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.
0	0b	RO/V	**SMLINK[0]_CUR_STS (SMLINK0_CUR_STS)** This bit has a default value that is dependent on an external signal level. This returns the value on the SMLINK[0] pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.

SMBUS_PIN_CTL Register (SMBC) – Offset f

Note: This register is in the resume well and is reset by RSMRST#

Bit Range	Default	Access	Field Name and Description
6:3	-	-	**Reserved**
2	1b	RW	**SMBCLK_CTL (SMBCLK_CTL)** 0 = Intel PCH will drive the SMBCLK pin low, independent of what the other SMB logic would otherwise indicate for the SMBCLK pin. 1 = The SMBCLK pin is Not overdriven low. The other SMBus logic controls the state of the pin.
1	0b	RO/V	**SMBDATA_CUR_STS (SMBDATA_CUR_STS)** This bit has a default value that is dependent on an external signal level. This returns the value on the SMBDATA pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.

Bit Range	Default	Access	Field Name and Description
0	0b	RO/V	**SMBCLK_CUR_STS (SMBCLK_CUR_STS)** This bit has a default value that is dependent on an external signal level. This returns the value on the SMBCLK pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.

Slave Status Register (SSTS) – Offset 10

All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally.

Bit Range	Default	Access	Field Name and Description
6:1	-	-	**Reserved**
0	0b	RW/1C	**HOST_NOTIFY_STS (HNS)** The Intel PCH sets this bit to a 1 when it has completely received a successful Host Notify Command on the SMBus pins. Software reads this bit to determine that the source of the interrupt or SMI# was the reception of the Host Notify Command. Software clears this bit after reading any information needed from the Notify address and data registers by writing a 1 to this bit. Note that the Intel PCH will allow the Notify Address and Data registers to be over-written once this bit has been cleared. When this bit is 1, the Intel PCH will NACK the first byte (host address) of any new Host Notify commands on the SMBus. Writing a 0 to this bit has no effect.

Slave Command Register (SCMD) – Offset 11

All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally. Also, software must confirm the prior written value before writing to the register again.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
6:3	-	-	**Reserved**
2	0b	RW	**SMBALERT_DIS (SMB_D)** Software sets this bit to 1 to block the generation of the interrupt or SMI# due to the SMBALERT# source. This bit is logically inverted and ANDed with the SMBALERT_STS bit. The resulting signal is distributed to the SMI# and/or interrupt generation logic. This bit does not effect the wake logic.
1	0b	RW	**HOST_NOTIFY_WKEN (HNW)** Software sets this bit to 1 to enable the reception of a Host Notify command as a wake event. When enabled this event is ORed in with the other SMBus wake events and is reflected in the SMB_WAK_STS bit of the General Purpose Event 0 Status register.
0	0b	RW	**HOST_NOTIFY_INTREN (HNI)** Software sets this bit to 1 to enable the generation of interrupt or SMI# when HOST_NOTIFY_STS is 1. This enable does not affect the setting of the HOST_ NOTIFY_STS bit. When the interrupt is generated, either PIRQB or SMI# is generated, depending on the value of the SMB_SMI_EN bit (D31, F3, Off40h, B1). If the HOST_NOTIFY_STS bit is set when this bit is written to a 1, then the interrupt (or SMI#) will be generated. The interrupt (or SMI#) is logically generated by ANDing the STS and INTREN bits.

Notify Device Address Register (NDA) – Offset 14

Notify Device Address Register

Bit Range	Default	Access	Field Name and Description
7:1	0000000 b	RO/V	**DEVICE_ADDRESS (DEV_ADDR)** This field contains the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.
0	-	-	**Reserved**

Notify Data Low Byte Register (NDLB) – Offset 16

Notify Data Low Byte Register

Bit Range	Default	Access	Field Name and Description
7:0	00h	RO	**DATA_LOW_BYTE (DLB)** This field contains the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

Notify Data High Byte Register (NDHB) – Offset 17

Notify Data High Byte Register

Bit Range	Default	Access	Field Name and Description
7:0	00h	RO	**DATA_HIGH_BYTE (DHB)** This field contains the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

SMBus PCR Registers

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset). The offsets are DWORD aligned byte addresses.

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	TCO Configuration (TCOCFG)	0h
ch	4	General Control (GC)	0h
10h	4	Power Control Enable (PCE)	9h

TCO Configuration (TCOCFG) – Offset 0

TCO Configuration

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7	0b	RW	**TCO IRQ Enable (IE)** When set, TCO IRQ is enabled, as selected by the TCO_IRQ_SEL field. When cleared, TCO IRQ is disabled.
6:0	-	-	**Reserved**

General Control (GC) – Offset c

General Control

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1	0b	RW	**No Reboot (NR)** This bit is set when the No Reboot strap is sampled high on PWROK. This bit may be set or cleared by software if the strap is sampled low but may not override the strap when it indicates No Reboot. When set, the TCO timer will count down and generate the SMI# on the first timeout, but will not reboot on the second timeout.
0	0b	RW	**Function Disable (FD)** When set to one, this disables the PCI config register space for the SMBus device.

Power Control Enable (PCE) – Offset 10

Power Control Enable

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30:4	-	-	**Reserved**
3	1b	RO	**Sleep Enable (SE)** When this bit is clear, the SMBus will never asset sleep to the controller. If set, then SMBus may assert sleep during power gating.
2	0b	RO	**D3-Hot Enable (D3HE)** No support for D3 Hot power gating.
1	0b	RO	**I3 Enable (I3E)** No support for S0i3 power gating.
0	1b	RW	**PMC Request Enable (PMCRE)** When set to 1, the SMBus will engage power gating if it is idle and other conditions are met.

SMBus TCO I/O Registers

The TCO I/O registers reside in a 32-byte range that starts from the IO Base Address described inthe TCOBAR register in the SMBus PCI Configuration space.

Summary of Bus:, Device:, Function: (IO)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	TCO_RLD Register (TRLD)	4h
2h	1	TCO_DAT_IN Register (TDI)	0h
3h	1	TCO_DAT_OUT Register (TDO)	0h
4h	2	TCO1_STS Register (TSTS1)	0h
6h	2	TCO2_STS Register (TSTS2)	0h
8h	2	TCO1_CNT Register (TCTL1)	0h
ah	2	TCO2_CNT Register (TCTL2)	8h
ch	2	TCO Message Registers (TMSG)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
eh	1	TCO_WDSTATUS Register (TWDS)	0h
10h	1	LEGACY_ELIM Register (LE)	3h
12h	2	TCO_TMR Register (TTMR)	4h

TCO_RLD Register (TRLD) – Offset 0

TCO_RLD Register

Bit Range	Default	Access	Field Name and Description
14:10	-	-	**Reserved**
9:0	0000000 100b	RW	**TCO Reload (TCORLD)** Reading this register will return the current count of the TCO timer. Writing any value to this register will reload the timer to prevent the timeout.

TCO_DAT_IN Register (TDI) – Offset 2

TCO_DAT_IN Register

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**TCO_DAT_IN (TDI)** Data Register for passing commands from the OS to the SMI handler. Writes to this register will cause an SMI and set the OS_TCO_SMI bit in the TCO_STS register.

TCO_DAT_OUT Register (TDO) – Offset 3

TCO_DAT_OUT Register

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**TCO_DAT_OUT (TDO)** Data Register for passing commands from the SMI handler to the OS. Writes to this register will set the TCO_INT_STS bit in the TCO_STS register. It also causes an interrupt, as selected by the TCO_IRQ_SEL bits.

TCO1_STS Register (TSTS1) – Offset 4

Unless otherwise indicated, these bits are sticky and are cleared by writing a 1 to the corresponding bit position.

Bit Range	Default	Access	Field Name and Description
14	-	-	**Reserved**
13	0b	RO	**TCO Slave Select (TCO_SLVSEL)** This register bit indicates the value of TCO Slave Select Soft Strap.
12	0b	RW/1C	**CPUSERR_STS (CPUSERR_STS)** This bit is set to 1 if the CPU complex sends a DMI special cycle message indicating that it wants to cause an SERR#. The software must read the CPU to find out why it wanted the SERR#. Software must write a 1 back to this bit to clear it.
11	-	-	**Reserved**
10	0b	RW/1C	**CPUSMI_STS (CPUSMI_STS)** This bit is set to 1 if the CPU complex sends a DMI special cycle message indicating that it wants to cause an SMI. The software must read the CPU to find out why it wanted the SMI. Software must write a 1 back to this bit to clear it.
9	0b	RW/1C	**(CPUSCI_STS)** This bit is set to 1 if the CPU complex sends a DMI special cycle message indicating that it wants to cause an SCI. The software must read the CPU to find out why it wanted the SCI. Software must write a 1 back to this bit to clear it.

Bit Range	Default	Access	Field Name and Description
8	0b	RW/1C	**(BIOSWR_STS)** Intel PCH sets this bit to 1 and generates an SMI# to indicate an illegal attempt to write to the BIOS located in the FWH that is accessed over the LPC. This occurs when either: a) The BIOSWP bit is changed from 0 to 1 and the LE bit is also set, or b) Any write is attempted to the BIOS and the BIOSWP bit is also set. This bit doesn't get set to 1 when: 1) a or b above occurs on eSPI controller. 2) a or b above occurs on SPI Flash controller. Note: On write cycles attempted to the 4MB lower alias to the BIOS space, the BIOSWR_STS bit will not be set.

Bit Range	Default	Access	Field Name and Description
7	0b	RW/1C	**NEWCENTURY_STS (NEWCENTURY_STS)** This bit will be set when the year rolls over from 1999 to 2000. If the bit is already 1, it will remain 1. This bit can be cleared either by software writing a 1 back to the bit position, or by RTCRST# going active. When this bit is set, an SMI# will be generated. However, this will not be a wake event (i.e. if the system is in a sleeping state when the NEWCENTURY_STS bit is set, the system will not wake up). Note: This bit 7 is not valid when the RTC battery is first put in (or if the RTC battery does not provide sufficient power when the system is unplugged). Software can determine that the RTC well was not maintained by checking the RTC_PWR_STS bit (GEN_PMCON_3 register in the Power Management Controller, D31:F2:A4, bit 2) or by other means (such as doing a checksum on the RTC RAM array). If the RTC well is determined to not have been maintained, the BIOS should set the time to a legal value and then clear the NEWCENTURY_STS bit. Note: This bit may take up to 3 RTCCLKs for the bit to be cleared when a 1 is written to the bit to clear it. After writing a 1 to the NEWCENTURY_STS bit, software should also not exit the SMI handler until after the bit has been cleared. This is to make sure the SMI is not re-entered. BIOS Assumption: When booting, the BIOS checks the NEWCENTURY_STS bit. If set, the BIOS should increment the value in the RTC RAM register associated with the century. The BIOS should then clear the NEWCENTURY_STS bit. This scenario would occur if the system was asleep when the century rolls over. If the system is in an S0 state (not sleeping) and the SMI# occurs with the NEWCENTURY_STS bit sets, the SMI handler should increment the value in the RTC RAM register and clear the NEWCENTURY_STS bit.
6:4	-	-	**Reserved**
3	0b	RW/1C	**TIMEOUT (TIMEOUT)** Bit set to 1 by Intel PCH to indicate that the SMI was caused by TCO timer reaching 0. Note: The SMI handler should clear this bit to prevent an immediate re-entry to the SMI handler.
2	0b	RW/1C	**TCO_INT_STS (TCO_INT_STS)** Bit set to 1 when SMI handler caused the interrupt by writing to the TCO_DAT_OUT register.
1	0b	RW/1C	**(OS_TCO_SMI)** Bit set to 1 when OS code caused an SMI# by writing to the TCO_DAT_IN register.

Bit Range	Default	Access	Field Name and Description
0	0b	RO/V	**(NMI2SMI_STS)** The PCH sets this bit when an SMI# occurs because an event occurred that would otherwise have caused an NMI.

TCO2_STS Register (TSTS2) – Offset 6

TCO2_STS Register

Bit Range	Default	Access	Field Name and Description
14:5	-	-	**Reserved**
4	0b	RW/1C	**(SMLINK_SLAVE_SMI_STS)** The PCH will set this bit to 1 when it receives the SMI message (encoding 08h in the command type) on the SMLinks Slave Interface. Software clears the bit by writing a 1 to this bit position. This bit is in the resume well. It is reset by RSMRST#, but not by the PCI Reset associated with exit from S3-S5 states. This allows the software (presumably BIOS) to get the interrupt, see this new bit set, and decidedly go into the pre-determined (by local policy) sleep state.
3:2	-	-	**Reserved**
1	0b	RW/1C	**(SECOND_TO_STS)** Intel PCH sets this bit to 1 to indicate that the TIMEOUT bit had been (or is currently) set and a second timeout occurred before the TCO_RLD register was written. If this bit is set and the NO_REBOOT config bit is 0, then the Intel PCH will reboot the system after the second timeout. The reboot is done by asserting PLTRST#. This bit is only cleared by writing a 1 to this bit or by a RSMRST#.

Bit Range	Default	Access	Field Name and Description
0	0b	RW/1C	**INTRD_DET (INTRD_DET)** The bit is set to 1 by the PCH to indicate that an intrusion was detected. This bit is cleared by writing a 1 to this bit or by RTCRST#. Note: This bit has a recovery time. After writing a 1 to this bit position (to clear it), the bit may be read back as a 1 for up 65 microseconds before it is read as a 0. Software must be aware of this recovery time when reading this bit after clearing it. Note: If the INTRUDER# signal is active when the software attempts to clear the INTRD_DET bit, the bit will remain as a 1, and the SMI# will be generated again immediately. The SMI handler can clear the INTRD_SEL bits to avoid further SMIs. However, if the INTRUDER# signals goes inactive and then active again, there will not be further SMIs. If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written as a 1, then the INTRD_DET signal will go to a 0 when INTRUDER# input signal goes inactive. Note that this is slightly different than a classic sticky bit, since most sticky bits would remain active indefinitely when the signal goes active and would immediately go inactive when a 1 is written to the bit.

TCO1_CNT Register (TCTL1) – Offset 8

TCO1_CNT Register

Bit Range	Default	Access	Field Name and Description
14:13	-	-	**Reserved**
12	0b	RW	**(TCO_LOCK)** When set to 1, this bit prevents writes from changing the TCO_EN bit (in offset 30h of Power Management I/O space). Once this bit is set to 1, it can not be cleared by software writing a 0 to this bit location. A core-well reset is required to change this bit from 1 to 0. This bit defaults to 0.

Bit Range	Default	Access	Field Name and Description
11	0b	RW	**(TCO_TMR_HALT)** 1 = The TCO timer will halt. It will not count, and thus cannot reach a value that would cause an SMI# or to cause the SECOND_TO_STS bit to be set. This will also prevent rebooting. 0 = The TCO timer is enabled to count. This is the default.
10	-	-	**Reserved**
9	0b	RW	**(NMI2SMI_EN)** This bit is implemented as RW but has no effect on HW. The NMI2SMI_EN bit is moved to the NMI Control register under Interrupt PCR space. Refer to NMI control register for details.
8	0b	RW	**(NMI_NOW)** This bit is implemented as RW but has no effect on HW. The NMI2SMI_EN bit is moved to the NMI Control register under Interrupt PCR space. Refer to NMI control register for details.
7:1	-	-	**Reserved**
0	0b	RW	**NO_REBOOT_MSUS (NR_MSUS)** This bit reflects the No Reboot pin strap state. It is sampled high on PWROK. This bit may be set or cleared by software if the strap is sampled low but may not override the strap when the it indicates No Reboot. When set, the TCO timer will count down and generate the SMI# on the first timeout, but will not reboot on the second timeout.

TCO2_CNT Register (TCTL2) – Offset a

TCO2_CNT Register

Bit Range	Default	Access	Field Name and Description
14:6	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
5:4	00b	RW	**OS_POLICY (OS_POLICY)** OS-based software writes to these bits to select the policy that the BIOS will use after the platform resets due the WDT. The following convention is recommended for the BIOS and OS: 00 Boot normally 01 Shut down 10 Dont load OS. Hold in pre-boot state and use LAN to determine next step 11 Reserved Implementation note: These are just scratch pad bits. They should not be reset when the TCO logic resets the platform due to Watchdog Timer.
3	1b	RW	**(SMB_ALERT_DISABLE)** Disables muxed GPIO/SMBALERT# signal as an alert source for the heartbeats and the SMBus slave. At reset (RSMRST# pin assertion only), this bit is set and the muxed GPIO/SMBALERT# alerts are disabled.
2:1	00b	RW	**INTRD_SEL (INTRD_SEL)** Selects the action to take if the INTRUDER# signal goes active. 11: Reserved 01: Interrupt (as selected by TCO_INT_SEL). 10: SMI# 00 INTRUDER# doesn't cause SMI# or interrupt
0	-	-	**Reserved**

TCO Message Registers (TMSG) – Offset c

TCOBASE+0Ch (MSG1)

TCOBASE+0Dh (MSG2)

BIOS can write into these registers to indicate its boot progress. The external microcontroller can read these registers to monitor the boot progress

Bit Range	Default	Access	Field Name and Description
15:8	00h	RW	**TCO Message2 (MSG2)** TCO Message2
7:0	00h	RW	**TCO Message1 (MSG1)** TCO Message1

TCO_WDSTATUS Register (TWDS) – Offset e

TCO_WDSTATUS Register

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**TCO_WDSTATUS Register (TWDS)** The BIOS or system management software can write into this register to indicate more details on the boot progress. The register will rest to 00h based on a RSMRST# (but not PCI Reset). The external microcontroller can read this register to monitor boot progress.

LEGACY_ELIM Register (LE) – Offset 10

LEGACY_ELIM Register

Bit Range	Default	Access	Field Name and Description
6:2	-	-	**Reserved**
1	1b	RW	**IRQ12_CAUSE (IRQ12_CAUSE)** When software sets the bit to 1, IRQ12 will be high (asserted). When software sets the bit to 0, IRQ12 will be low (not asserted). Default for this bit is 1.
0	1b	RW	**IRQ1_CAUSE (IRQ1_CAUSE)** When software sets the bit to 1, IRQ1 will be high (asserted). When software sets the bit to 0, IRQ1 will be low (not asserted). Default for this bit is 1.

TCO_TMR Register (TTMR) – Offset 12

TCO_TMR Register

Bit Range	Default	Access	Field Name and Description
14:10	-	-	**Reserved**
9:0	0000000 100b	RW	**TCOTMR (TCOTMR)** Value that is loaded into the timer each time the TCO_RLD register is written. Values of 0000h or 0001h will be ignored and should not be attempted. The timer is clocked at approximately 0.6 seconds, and thus allows timeouts ranging from 1.2 second to 613.8 seconds. Note: The timer has an error of +/- 1 tick (0.6s).

SPI Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID and Vendor ID (BIOS_SPI_DID_VID)	XXXX8086h
4h	4	Status and Command (BIOS_SPI_STS_CMD)	400h
8h	4	Revision ID and Class Code (BIOS_SPI_CC_RID)	C8000XXh
ch	4	BIST, Header Type, Latency Timer, Cache Line Size (BIOS_SPI_BIST_HTYPE_LT_CLS)	0h
10h	4	SPI BAR0 MMIO (BIOS_SPI_BAR0)	0h
d0h	4	SPI Unsupported Request Status (BIOS_SPI_UR_STS_CTL)	0h
d8h	4	BIOS Decode Enable (BIOS_SPI_BDE)	FFCFh
dch	4	BIOS Control (BIOS_SPI_BC)	28h

Device ID and Vendor ID (BIOS_SPI_DID_VID) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:16	See Description	RO/V	**Device Identification (DID)** Identifier for the SPI Flash Controller in Host Root Space. Refer to the Device and Version ID Table in Volume 1 for the default value.
15:0	8086h	RO	**Vendor Identification (VID)** This field identifies the manufacturer of the device. 0x8086 indicates Intel

Status and Command (BIOS_SPI_STS_CMD) – Offset 4

Bit Range	Default	Access	Field Name and Description
31	0b	RW/1C/V	**Detected Parity Error (DPE)** Detected Parity Error (DPE): 0 = No parity error detected by the controller. 1 = The controller detects a parity error on its interface.
30	0b	RW/1C/V	**Signaled System Error (SSE)** Signaled System Error (SSE): 0 = No SERR# detected by the controller. 1 = The controller detects a SERR# on its interface.
29	0b	RO	**Received Master Abort (RMA)** Hardwired to 0.
28	0b	RO	**Received Target Abort (RTA)** Hardwired to 0.
27	0b	RW/1C/V	**Signaled Target Abort (STA)**
26:25	-	-	**Reserved**
24	0b	RO	**Master Data Parity Error (MDPE)** Hardwired to 0.

Bit Range	Default	Access	Field Name and Description
23:22	-	-	**Reserved**
21	0b	RO	**66 MHz Capable (MCAP)** Not 66 MHz capable device.
20	0b	RO	**Capabilities List (CAPL)** Hardwired to 0 indicating that a Capabilities List is not present.
19	0b	RO	**Interrupt Status (INTS)** Hardwired to 0.
18:11	-	-	**Reserved**
10	1b	RO	**Interrupt Disable (INTD)** Hardwired to 1. INTx# interrupt is disabled.
9	0b	RO	**Fast Back to Back Enable (FBTBEN)** Hardwired to 0.
8	0b	RW	**System Error Enable (SERREN)** 0 = SERR# generation is disabled.1 = SERR# generation is enabled.
7	-	-	**Reserved**
6	0b	RW	**Parity Error Response (PERRR)** 0 = Disabled. The controller will not generate PERR# when a data parity error is detected.1 = Enabled. The controller will generate PERR# when a data parity error is detected.
5	-	-	**Reserved**
4	0b	RO	**Memory Write and Invalidate Enable (MWRIEN)** Hardwired to 0.
3	0b	RO	**Special Cycle Enable (SPCYC)** Hardwired to 0.

Bit Range	Default	Access	Field Name and Description
2	0b	RW	**Bus Master Enable (BME)** 0 = Disable1 = Enable
1	0b	RW	**Memory Space Enable (MSE)** 0 = Disables memory mappedConfiguration space.1 = Enables memory mapped Configuration space.
0	0b	RO	**IO Space Enable (IOSE)** Hardwired to 0.

Revision ID and Class Code (BIOS_SPI_CC_RID) – Offset 8

Bit Range	Default	Access	Field Name and Description
31:24	0Ch	RO	**Base Class Code (BCC)**
23:16	80h	RO	**Sub-Class Code (SCC)**
15:8	00h	RO	**Programming Interface (PI)**
7:0	See Description	RO/V	**Revision ID (RID)** Revision ID (RID): Indicates the part revision. Refer to the Device and Revision ID Table in Volume 1 for the default value.

BIST, Header Type, Latency Timer, Cache Line Size (BIOS_SPI_BIST_HTYPE_LT_CLS) – Offset c

Bit Range	Default	Access	Field Name and Description
30:23	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
22:16	00h	RO	**Header Type (HTYPE)** Implements Type 0 Configuration.
15:8	00h	RO	**Latency Timer (LT)** Does not apply. Hardwired to 0.
7:0	00h	RO	**Cacheline Size (CLSZ)** Does not apply. Hardwired to 0.

SPI BAR0 MMIO (BIOS_SPI_BAR0) – Offset 10

Bit Range	Default	Access	Field Name and Description
31:12	00000h	RW	**Memory BAR (MEMBAR)** Software programs this register with the base address of the device's memory region. The Host/BIOS MMIO registers in the flash controller are offset from this BAR.
11:4	00h	RO	**Memory Size (MEMSIZE)** Hardwired to 0 to indicate 4KB of memory space
3	0b	RO	**Prefetchable (PREFETCH)** A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables. Hardwired to 1 to indicate the device's memory space as prefetchable.
2:1	00b	RO	**Type (TYP)** Hardwired to 0 to indicate that Base register is 32 bits wide and mapping can be done anywhere in the 32-bit Memory Space.
0	0b	RO	**Memory Space Indicator (MEMSPACE)** Hardwired to 0 to identify a Memory BAR.

SPI Unsupported Request Status (BIOS_SPI_UR_STS_CTL) – Offset d0

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1	0b	RW/1C/V	**Unsupported Request Detected (URD)** Set to 1 by hardware upon detecting an Unspported Request that is not considered an Advisory Non-Fatal error. Cleared to 0 when software writes a 1 to this register.
0	0b	RW	**Unsupported Request Reporting Enabled (URRE)** If set to 1 by software, the flash controller generates a DoSERR sideband message when the URD bit transitions from 0 to 1.

BIOS Decode Enable (BIOS_SPI_BDE) – Offset d8

This register only effects BIOS decode if BIOS is resident on SPI.

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15	1b	RO	**F8-FF Enable (EF8)** Enables decoding of 512K of the following BIOS ranges: FFF80000h - FFFFFFFFh FFB80000h - FFBFFFFFh
14	1b	RW	**F0-F8 Enable (EF0)** Enables decoding of 512K of the following BIOS ranges: FFF00000h - FFF7FFFFh FFB00000h - FFB7FFFFh

Bit Range	Default	Access	Field Name and Description
13	1b	RW	**E8-EF Enable (EE8)** Enables decoding of 512K of the following BIOS ranges: FFE80000h - FFEFFFFFh FFA80000h - FFAFFFFFh
12	1b	RW	**E0-E8 Enable (EE0)** Enables decoding of 512K of the following BIOS ranges: FFE00000h - FFE7FFFFh FFA00000h - FFA7FFFFh
11	1b	RW	**D8-DF Enable (ED8)** Enables decoding of 512K of the following BIOS ranges: FFD80000h - FFDFFFFFh FF980000h - FF9FFFFFh
10	1b	RW	**D0-D7 Enable (ED0)** Enables decoding of 512K of the following BIOS ranges: FFD00000h - FFD7FFFFh FF900000h - FF97FFFFh

Bit Range	Default	Access	Field Name and Description
9	1b	RW	**C8-CF Enable (EC8)** Enables decoding of 512K of the following BIOS ranges: FFC80000h - FFCFFFFFh FF880000h - FF8FFFFFh
8	1b	RW	**C0-C7 Enable (EC0)** Enables decoding of 512K of the following BIOS ranges: FFC00000h - FFC7FFFFh FF800000h - FF87FFFFh
7	1b	RW	**Legacy F Segment Enable (LFE)** Legacy F Segment Enable (LFE): This enables the decoding of the legacy 64KB range at F0000h - FFFFFh
6	1b	RW	**Legacy E Segment Enable (LEE)** Legacy E Segment Enable (LFE): This enables the decoding of the legacy 64KB range at E0000h - EFFFFh
5:4	-	-	**Reserved**
3	1b	RW	**70-7F Enable (E70)** Enables decoding of 1MB of the following BIOS ranges: FF700000h - FF7FFFFFh FF300000h - FF3FFFFFh

Bit Range	Default	Access	Field Name and Description
2	1b	RW	**60-6F Enable (E60)** Enables decoding of 1MB of the following BIOS ranges: FF600000h - FF6FFFFFh FF200000h - FF2FFFFFh
1	1b	RW	**50-5F Enable (E50)** Enables decoding of 1MB of the following BIOS ranges: FF500000h - FF5FFFFFh FF100000h - FF1FFFFFh
0	1b	RW	**40-4F Enable (E40)** Enables decoding of 1MB of the following BIOS ranges: FF400000h - FF4FFFFFh FF000000h - FF0FFFFFh

BIOS Control (BIOS_SPI_BC) – Offset dc

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
11	0b	RW/L	**Async SMI Enable for BIOS Write Protection (ASE_BWP)** When set to '1' the flash controller will generate an SMI when it blocks a BIOS write or erase due to WPD = 0. The value in this field can be written by software as long as the BIOS Interface Lock-Down (BILD) is not set.
10	0b	RO/V	**Asynchronous SMI Status (SPI_ASYNC_SS)** Status indication that the SPI Flash Controller has asserted an asynchronous SMI. Hardware clears the bit when it sends the De-assert SMI message. 0 : default state 1 : SPI flash controller asserted asynchronous SMI
9	-	-	**Reserved**
8	0b	RW/1C/V	**Synchronous SMI Status (SPI_SYNC_SS)** Status indication that the SPI Flash Controller has asserted a synchronous SMI. Hardware clears the bit when it sends the De-assert Synchronous SMI message. 0 : default state 1 : SPI flash controller asserted Synchronous SMI
7	0b	RW/L	**BIOS Interface Lock-Down (BILD)** When set, prevents TS and BBS from being changed. This bit can only be written from 0 to 1 once.
6	0b	RW/V/L	**Boot BIOS Strap (BBS)** This field determines the destination of accesses to the BIOS memory range. 0 = SPI 1 = LPC When SPI or LPC is selected, the range that is decoded is further qualified by BIOS Decode Enable. The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down (BILD) is not set

Bit Range	Default	Access	Field Name and Description
5	1b	RW/L	**Enable InSMM.STS (EISS)** When this bit is set, the BIOS region is not writable until the CPU sets the InSMM.STS bit. If this bit [5] is set, then WPD must be a '1' and InSMM.STS(0xFED3_0880[0]) must be '1' also in order to write to BIOS region of SPI Flash. If this bit [5] is clear, then the InSMM.STS is a don't care. This bit is locked by LE
4	0b	RO/V	**Top Swap Status (TSS)** This bit provides a read-only path to view the state of the Top Swap bit. It is duplicated here to be consistent with the LPC version of the BC register.
3:2	10b	RW	**SPI Read Configuration (SRC)** These bits are located in PCI Config space to allow them to be set early in the boot flow. This 2-bit field controls two policies related to BIOS reads on the SPI interface: Bit 3- Prefetch Enable Bit 2- Cache Disable Settings are summarized below: 00 = No prefetching, but caching enabled. Direct Memory reads load the read buffer cache with valid data, allowing repeated reads to the same range to complete quickly 01 = No prefetching and no caching. One-to-one correspondence of host BIOS reads to SPI cycles. This value can be used to invalidate the cache. 10 = Prefetching and Caching enabled. This mode is used for long sequences of short reads to consecutive addresses (i.e. shadowing) 11 = Illegal. Caching must be enabled when Prefetching is enabled.
1	0b	RW/L	**Lock Enable (LE)** When set, setting the WPD bit will cause SMI. When cleared, setting the WPD bit will not cause SMI. Once set, this bit can only be cleared by a PLTRST#. When this bit is set, EISS - bit [5] of this register is locked down.

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**Write Protect Disable (WPD)** When set, access to the BIOS space is enabled for both read and write cycles to BIOS. When cleared, only read cycles are permitted to the FWH or SPI flash. When this bit is written from a '0' to a '1' and the LE bit is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

SPI Memory Mapped Registers

The SPI memory mapped registers are accessed based upon offsets from SPI_BAR0 (in PCI config SPI_BAR0 register).

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	BIOS Flash Primary Region (BIOS_BFPREG)	0h
4h	4	Hardware Sequencing Flash Status and Control (BIOS_HSFSTS_CTL)	2000h
8h	4	Flash Address (BIOS_FADDR)	0h
ch	4	Discrete Lock Bits (BIOS_DLOCK)	0h
10h	4	Flash Data 0 (BIOS_FDATA0)	0h
14h	4	Flash Data 1 (BIOS_FDATA1)	0h
18h	4	Flash Data 2 (BIOS_FDATA2)	0h
1ch	4	Flash Data 3 (BIOS_FDATA3)	0h
20h	4	Flash Data 4 (BIOS_FDATA4)	0h
24h	4	Flash Data 5 (BIOS_FDATA5)	0h
28h	4	Flash Data 6 (BIOS_FDATA6)	0h
2ch	4	Flash Data 7 (BIOS_FDATA7)	0h
30h	4	Flash Data 8 (BIOS_FDATA8)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
34h	4	Flash Data 9 (BIOS_FDATA9)	0h
38h	4	Flash Data 10 (BIOS_FDATA10)	0h
3ch	4	Flash Data 11 (BIOS_FDATA11)	0h
40h	4	Flash Data 12 (BIOS_FDATA12)	0h
44h	4	Flash Data 13 (BIOS_FDATA13)	0h
48h	4	Flash Data 14 (BIOS_FDATA14)	0h
4ch	4	Flash Data 15 (BIOS_FDATA15)	0h
50h	4	Flash Region Access Permissions (BIOS_FRACC)	42C2h
54h	4	Flash Region 0 (BIOS_FREG0)	0h
58h	4	Flash Region 1 (BIOS_FREG1)	7FFFh
5ch	4	Flash Region 2 (BIOS_FREG2)	7FFFh
60h	4	Flash Region 3 (BIOS_FREG3)	7FFFh
64h	4	Flash Region 4 (BIOS_FREG4)	7FFFh
68h	4	Flash Region 5 (BIOS_FREG5)	7FFFh
84h	4	Flash Protected Range 0 (BIOS_FPR0)	0h
88h	4	Flash Protected Range 1 (BIOS_FPR1)	0h
8ch	4	Flash Protected Range 2 (BIOS_FPR2)	0h
90h	4	Flash Protected Range 3 (BIOS_FPR3)	0h
94h	4	Flash Protected Range 4 (BIOS_FPR4)	0h
98h	4	Global Protected Range 0 (BIOS_GPR0)	0h
b0h	4	Secondary Flash Region Access Permissions (BIOS_SFRACC)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
b4h	4	Flash Descriptor Observability Control (BIOS_FDOC)	0h
b8h	4	Flash Descriptor Observability Data (BIOS_FDOD)	0h
c0h	4	Additional Flash Control (BIOS_AFC)	0h
c4h	4	Vendor Specific Component Capabilities for Component 0 (BIOS_SFDP0_VSCC0)	2000h
c8h	4	Vendor Specific Component Capabilities for Component 1 (BIOS_SFDP1_VSCC1)	2000h
cch	4	Parameter Table Index (BIOS_PTINX)	0h
d0h	4	Parameter Table Data (BIOS_PTDATA)	0h
d4h	4	SPI Bus Requester Status (BIOS_SBRS)	0h

BIOS Flash Primary Region (BIOS_BFPREG) – Offset 0

Bit Range	Default	Access	Field Name and Description
30:16	0h	RO/V	**BIOS Flash Primary Region Limit (PRL)** This specifies address bits 26:12 for the Primary Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit, or the Flash Descriptor.FLREG6.Region Limit depending on the BFPREG.SBRS bit.
15	-	-	**Reserved**
14:0	0h	RO/V	**BIOS Flash Primary Region Base (PRB)** This specifies address bits 26:12 for the Primary Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base, or the Flash Descriptor.FLREG6.Region Base depending on the BFPREG.SBRS bit.

Hardware Sequencing Flash Status and Control (BIOS_HSFSTS_CTL) – Offset 4

Bit Range	Default	Access	Field Name and Description
31	0b	RW	**Flash SPI SMI# Enable (FSMIE)** When set to 1, the SPI asserts an SMI# request whenever the Flash Cycle Done bit is 1.
30	-	-	**Reserved**
29:24	0h	RW	**Flash Data Byte Count (FDBC)** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The contents of this register are 0s based with 0b representing 1 byte and 3Fh representing 64 bytes. The number of bytes transferred is the value of this field plus 1. This field is ignored for the Block Erase command.
23:22	-	-	**Reserved**
21	0b	RW	**Write Enable Type (WET)** 0: Use 06h as the write enable instruction 1: Use 50h as the write enable instruction. Note that this setting is not supported as no supported flash devices require the 50h opcode to enable a non-volatile status register write.

Bit Range	Default	Access	Field Name and Description
20:17	0000b	RW	**Flash Cycle (FCYCLE)** This field defines the Flash SPI cycle type generated to the FLASH when the FGO bit is set as defined below: 0 Read (1 up to 64 bytes by setting FDBC) 1 Reserved 2 Write (1 up to 64 bytes by setting FDBC) 3 4k Block Erase 4 64k Sector erase 5 Read SFDP 6 Read JEDEC ID 7 write status 8 read status 9 RPMC Op1 A RPMC Op2 Flash controller hardware automatically inserts a write enable opcode prior to Write and erase operations. Hardware automatically polls for device not-busy using read status after write and erase operations. If the device does not support 64k erase size (or if it doesn't support SFDP) then only 4k is allowed. Note: if reserved 1 is programmed to this field, flash controller will handle it as if it is 0 (Read)

Bit Range	Default	Access	Field Name and Description
16	0b	RW/1S/V	**Flash Cycle Go (FGO)** A write to this register with a 1 in this bit initiates a request to the Flash SPI Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the SPI arbiter to run the cycle on the SPI bus. When the cycle is complete, the FDONE bit is set. Software is forbidden to write to any register in the HSFLCTL register between the FGO bit getting set and the FDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit always returns 0 on reads.
15	0b	RW/L	**Flash Configuration Lock-Down (FLOCKDN)** When set to 1, those Flash Program Registers that are locked down by this FLOCKDN bit cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
14	0b	RO/V	**Flash Descriptor Valid (FDV)** This bit is set to a 1 if the Flash Controller read the correct Flash Descriptor Signature. If the Flash Descriptor Valid bit is not 1 , software cannot use the Hardware Sequencing registers, but must use the software sequencing registers. Any attempt to use the Hardware Sequencing registers will result in the FCERR bit being set
13	1b	RO/V	**Flash Descriptor Override Pin-Strap Status (FDOPSS)** This register reflects the value the Flash Descriptor Override Pin-Strap. '1': No override '0': The Flash Descriptor Override strap is set
12	0b	RW/L	**PRR3 PRR4 Lock-Down (PRR34_LOCKDN)** When set to 1, the BIOS PRR3 and PRR4 registers cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.

Bit Range	Default	Access	Field Name and Description
11	0b	RW/L	**Write Status Disable (WRSDIS)** 0 = Write status operation may be issued using Hardware Sequencing. 1 = Write status is not allowed as a Hardware Sequencing operation. The flash controller will block the operation and set the FCERR bit when software sets the 'go' bit. This bit is locked when FLOCKDN is set.
10:9	-	-	**Reserved**
8	0b	RW/1C/V	**SAF ctype error (H_SAF_CE)** Hardware sets this bit to 1 when a transaction is returned from the eSPI controller with ctype error.
7	0b	RO/V	**SAF Mode Active (H_SAF_MODE_ACTIVE)** 0 : indicates flash is attached directly to the PCH via the SPI bus 1 : indicates flash is attached to the EC/BMC and is accessed via tunneled eSPI commands.
6	0b	RW/1C/V	**SAF link Error (H_SAF_LE)** Hardware sets this bit to 1 when a transaction is returned from the eSPI channel with link error.
5	0b	RO/V	**SPI Cycle In Progress (H_SCIP)** Hardware sets this bit when software sets the Flash Cycle Go (FGO) bit in the Hardware Sequencing Flash Control register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.
4	0b	RW/1C/V	**SAF Data length Error (H_SAF_DLE)** Hardware sets this bit to 1 when a transaction is returned from the eSPI channel with an incorrect data length.
3	0b	RW/1C/V	**SAF Error (H_SAF_ERROR)** Hardware sets this bit to 1 when a transaction is requested that is not supported by slave-attached flash, e.g. read status.

Bit Range	Default	Access	Field Name and Description
2	0b	RW/1C/V	**Access Error Log (H_AEL)** Hardware sets this bit to a 1 when an attempt was made to access the BIOS region using the direct access method or an access to the BIOS Program Registers that violated the security restrictions. This bit is simply a log of an access security violation. This bit is cleared by software writing a '1'.
1	0b	RW/1C/V	**Flash Cycle Error (FCERR)** Hardware sets this bit to 1 when a program register access is blocked to the FLASH due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or until hardware reset occurs. Software must clear this bit before setting the FLASH Cycle GO bit in this register.
0	0b	RW/1C/V	**Flash Cycle Done (FDONE)** The PCH sets this bit to 1 when the SPI Cycle completes after software previously set the FGO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.

Flash Address (BIOS_FADDR) – Offset 8

Bit Range	Default	Access	Field Name and Description
30:27	-	-	**Reserved**
26:0	0h	RW	**Flash Linear Address (FLA)** The FLA is the starting byte linear address of a SPI Read or Write cycle or an address within a Block for the Block Erase command. The Flash Linear Address must fall within a region for which BIOS has access permissions. Hardware must convert the FLA into a Flash Physical Address (FPA) before running this cycle on the SPI bus.

Discrete Lock Bits (BIOS_DLOCK) – Offset c

Lockable BIOS registers may be locked by either the global FLOCKDN bit or by the individual DLOCK bit. Each lockable bit in this register is locked either by itself or by the FLOCKDN bit.

Bit Range	Default	Access	Field Name and Description
30:17	-	-	**Reserved**
16	0b	RW/L	**SSEQ Lock-Down (SSEQLOCKDN)** BIOS Software Sequencing registers are locked when the logical OR of this bit and FLOCKDN is true. The affected registers are SSFSTS_CTL.SCF, PREOP_OPTYPE, OPMENU0, and OPMENU1. Once set to 1 this register is only cleared by host partition reset.
15	0b	RW/L	**Spare1 (SPARE1)** Once set to 1 this register is only cleared by host partition reset.
14	0b	RW/L	**Spare2 (SPARE2)** Once set to 1 this register is only cleared by host partition reset.
13	0b	RW/L	**Spare3 (SPARE3)** Once set to 1 this register is only cleared by host partition reset.
12	0b	RW/L	**PR4 Lock-Down (PR4LOCKDN)** BIOS PR4 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset.
11	0b	RW/L	**PR3 Lock-Down (PR3LOCKDN)** BIOS PR3 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset.
10	0b	RW/L	**PR2 Lock-Down (PR2LOCKDN)** BIOS PR2 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset.
9	0b	RW/L	**PR1 Lock-Down (PR1LOCKDN)** BIOS PR1 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset.

Bit Range	Default	Access	Field Name and Description
8	0b	RW/L	**PR0 Lock-Down (PR0LOCKDN)** BIOS PR0 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset.
7	0b	RW/L	**Spare4 (SPARE4)** Once set to 1 this register is only cleared by host partition reset.
6	0b	RW/L	**Spare5 (SPARE5)** Once set to 1 this register is only cleared by host partition reset.
5	0b	RW/L	**Spare6 (SPARE6)** Once set to 1 this register is only cleared by host partition reset.
4	0b	RW/L	**Spare7 (SPARE7)** Once set to 1 this register is only cleared by host partition reset.
3	0b	RW/L	**SBMRAG Lock-Down (SBMRAGLOCKDN)** BIOS SFRACC.BMRAG register bits are locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by host partition reset.
2	0b	RW/L	**SBMWAG Lock-Down (SBMWAGLOCKDN)** BIOS SFRACC.BMWAG register bits are locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by host partition reset.
1	0b	RW/L	**BMRAG Lock-Down (BMRAGLOCKDN)** BIOS FRACC.BMRAG register bits are locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by host partition reset.
0	0b	RW/L	**BMWAG Lock-Down (BMWAGLOCKDN)** BIOS FRACC.BMWAG register bits are locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by host partition reset.

Flash Data 0 (BIOS_FDATA0) – Offset 10

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Flash Data 0 (FD0)** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13-...8-23-22-...16-31...24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

Flash Data 1 (BIOS_FDATA1) – Offset 14

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Flash Data 1 (FD1)** Similar definition as Flash Data 0. However, this register does not begin shifting until FD0 has completely shifted in/out.

Flash Data 2 (BIOS_FDATA2) – Offset 18

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Flash Data 2 (FD2)** Similar definition as Flash Data 0. However, this register does not begin shifting until FD1 has completely shifted in/out.

Flash Data 3 (BIOS_FDATA3) – Offset 1c

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Flash Data 3 (FD3)** Similar definition as Flash Data 0. However, this register does not begin shifting until FD2 has completely shifted in/out.

Flash Data 4 (BIOS_FDATA4) – Offset 20

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Flash Data 4 (FD4)** Similar definition as Flash Data 0. However, this register does not begin shifting until FD3 has completely shifted in/out.

Flash Data 5 (BIOS_FDATA5) – Offset 24

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Flash Data 5 (FD5)** Similar definition as Flash Data 0. However, this register does not begin shifting until FD4 has completely shifted in/out.

Flash Data 6 (BIOS_FDATA6) – Offset 28

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Flash Data 6 (FD6)** Similar definition as Flash Data 0. However, this register does not begin shifting until FD5 has completely shifted in/out.

Flash Data 7 (BIOS_FDATA7) – Offset 2c

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Flash Data 7 (FD7)** Similar definition as Flash Data 0. However, this register does not begin shifting until FD6 has completely shifted in/out.

Flash Data 8 (BIOS_FDATA8) – Offset 30

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Flash Data 8 (FD8)** Similar definition as Flash Data 0. However, this register does not begin shifting until FD7 has completely shifted in/out.

Flash Data 9 (BIOS_FDATA9) – Offset 34

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Flash Data 9 (FD9)** Similar definition as Flash Data 0. However, this register does not begin shifting until FD8 has completely shifted in/out.

Flash Data 10 (BIOS_FDATA10) – Offset 38

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Flash Data 10 (FD10)** Similar definition as Flash Data 0. However, this register does not begin shifting until FD9 has completely shifted in/out.

Flash Data 11 (BIOS_FDATA11) – Offset 3c

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Flash Data 11 (FD11)** Similar definition as Flash Data 0. However, this register does not begin shifting until FD10 has completely shifted in/out.

Flash Data 12 (BIOS_FDATA12) – Offset 40

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW/V	**Flash Data 12 (FD12)** Similar definition as Flash Data 0. However, this register does not begin shifting until FD11 has completely shifted in/out.

Flash Data 13 (BIOS_FDATA13) – Offset 44

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Flash Data 13 (FD13)** Similar definition as Flash Data 0. However, this register does not begin shifting until FD12 has completely shifted in/out.

Flash Data 14 (BIOS_FDATA14) – Offset 48

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Flash Data 14 (FD14)** Similar definition as Flash Data 0. However, this register does not begin shifting until FD13 has completely shifted in/out.

Flash Data 15 (BIOS_FDATA15) – Offset 4c

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW/V	**Flash Data 15 (FD15)** Similar definition as Flash Data 0. However, this register does not begin shifting until FD14 has completely shifted in/out.

Flash Region Access Permissions (BIOS_FRACC) – Offset 50

Bit Range	Default	Access	Field Name and Description
31:24	00h	RW/L	**BIOS Master Write Access Grant (BMWAG)** BIOS Master Write Access Grant (BMWAG): Each bit [31:24] corresponds to Master[7:0]. BIOS can grant one or more masters write access to the BIOS region 1 overriding the permissions in the Flash Descriptor. The contents of this register are locked by the FLOCKDN bit.
23:16	00h	RW/L	**BIOS Master Read Access Grant (BMRAG)** BIOS Master Read Access Grant (BMRAG): Each bit [23:16] corresponds to Master[7:0]. BIOS can grant one or more masters read access to the BIOS region 1 overriding the read permissions in the Flash Descriptor. The contents of this register are locked by the FLOCKDN bit

Bit Range	Default	Access	Field Name and Description
15:8	42h	RO/V	**BIOS Region Write Access (BRWA)** BIOS Region Write Access (BRWA): Each bit [15:8] corresponds to Regions [7:0]. If the bit is set, this master can erase and write that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS write permissions in their Master Write Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS always have the write access to its own Region 1 and Region 6 by default.
7:0	C2h	RO/V	**BIOS Region Read Access (BRRA)** BIOS Region Read Access (BRRA): Each bit [7:0] corresponds to Regions [7:0]. If the bit is set, this master can read that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS read permissions in their Master Read Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS always have the read access to its own Region 1 and Region 6 by default.

Flash Region 0 (BIOS_FREG0) – Offset 54

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30:16	0h	RO/V	**Region Limit (RL)** This specifies address bits 26:12 for the Region 0 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Limit.
15	-	-	**Reserved**
14:0	0h	RO/V	**Region Base (RB)** This specifies address bits 26:12 for the Region 0 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Base.

Flash Region 1 (BIOS_FREG1) – Offset 58

Bit Range	Default	Access	Field Name and Description
30:16	0h	RO/V	**Region Limit (RL)** This specifies address bits 26:12 for the Region 1 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit.
15	-	-	**Reserved**
14:0	7FFFh	RO/V	**Region Base (RB)** This specifies address bits 26:12 for the Region 1 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base.

Flash Region 2 (BIOS_FREG2) – Offset 5c

Bit Range	Default	Access	Field Name and Description
30:16	0h	RO/V	**Region Limit (RL)** This specifies address bits 26:12 for the Region 2 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Limit.
15	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
14:0	7FFFh	RO/V	**Region Base (RB)** This specifies address bits 26:12 for the Region 2 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Base.

Flash Region 3 (BIOS_FREG3) – Offset 60

Bit Range	Default	Access	Field Name and Description
30:16	0h	RO/V	**Region Limit (RL)** This specifies address bits 26:12 for the Region 3 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Limit.
15	-	-	**Reserved**
14:0	7FFFh	RO/V	**Region Base (RB)** This specifies address bits 26:12 for the Region 3 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base.

Flash Region 4 (BIOS_FREG4) – Offset 64

Bit Range	Default	Access	Field Name and Description
30:16	0h	RO/V	**Region Limit (RL)** This specifies address bits 26:12 for the Region 4 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Limit.
15	-	-	**Reserved**
14:0	7FFFh	RO/V	**Region Base (RB)** This specifies address bits 26:12 for the Region 4 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Base.

Flash Region 5 (BIOS_FREG5) – Offset 68

Bit Range	Default	Access	Field Name and Description
30:16	0h	RO/V	**Region Limit (RL)** This specifies address bits 26:12 for the Region 5 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG5.Region Limit.
15	-	-	**Reserved**
14:0	7FFFh	RO/V	**Region Base (RB)** This specifies address bits 26:12 for the Region 5 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG5.Region Base.

Flash Protected Range 0 (BIOS_FPR0) – Offset 84

This register cannot be written when the FLOCKDN bit is set to 1.

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**Write Protection Enable (WPE)** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h	RW/L	**Protected Range Limit (PRL)** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0b	RW/L	**Read Protection Enable (RPE)** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h	RW/L	**Protected Range Base (PRB)** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

Flash Protected Range 1 (BIOS_FPR1) – Offset 88

This register cannot be written when the FLOCKDN bit is set to 1.

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**Write Protection Enable (WPE)** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h	RW/L	**Protected Range Limit (PRL)** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0b	RW/L	**Read Protection Enable (RPE)** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h	RW/L	**Protected Range Base (PRB)** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

Flash Protected Range 2 (BIOS_FPR2) – Offset 8c

This register cannot be written when the FLOCKDN bit is set to 1.

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**Write Protection Enable (WPE)** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h	RW/L	**Protected Range Limit (PRL)** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.

Bit Range	Default	Access	Field Name and Description
15	0b	RW/L	**Read Protection Enable (RPE)** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h	RW/L	**Protected Range Base (PRB)** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

Flash Protected Range 3 (BIOS_FPR3) – Offset 90

This register cannot be written when the PRR34_LOCKDN bit is set to 1

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**Write Protection Enable (WPE)** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h	RW/L	**Protected Range Limit (PRL)** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0b	RW/L	**Read Protection Enable (RPE)** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h	RW/L	**Protected Range Base (PRB)** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

Flash Protected Range 4 (BIOS_FPR4) – Offset 94

This register cannot be written when the PRR34_LOCKDN bit is set to 1

Bit Range	Default	Access	Field Name and Description
31	0b	RW/L	**Write Protection Enable (WPE)** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h	RW/L	**Protected Range Limit (PRL)** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0b	RW/L	**Read Protection Enable (RPE)** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h	RW/L	**Protected Range Base (PRB)** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

Global Protected Range 0 (BIOS_GPR0) – Offset 98

This register is initialized via softstraps. This protected range applies globally to all masters / flash requesters.

Bit Range	Default	Access	Field Name and Description
31	0b	RO/V	**Write Protection Enable (WPE)** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h	RO/V	**Protected Range Limit (PRL)** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. Note: If either Write or Read protection is enabled, then Limit must be configured greater than or equal to Base.

Bit Range	Default	Access	Field Name and Description
15	0b	RO/V	**Read Protection Enable (RPE)** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h	RO/V	**Protected Range Base (PRB)** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. Note: If either Write or Read protection is enabled, then Limit must be configured greater than or equal to Base.

Secondary Flash Region Access Permissions (BIOS_SFRACC) – Offset b0

Bit Range	Default	Access	Field Name and Description
31:24	00000000b	RW/L	**Secondary BIOS Master Write Access Grant (SECONDARYBIOS_MWAG)** Each bit 31:29 corresponds to Master7:0. BIOS can grant one or more masters write access to the Secondary BIOS region 6 overriding the permissions in the Flash Descriptor. Bits for unassigned masters are reserved. The contents of this register are locked by the FLOCKDN bit.
23:16	00000000b	RW/L	**Secondary BIOS Master Read Access Grant (SECONDARYBIOS_MRAG)** Each bit 28:16 corresponds to Master7:0. BIOS can grant one or more masters read access to the Secondary BIOS region 6 overriding the read permissions in the Flash Descriptor. Bits for unassigned masters are reserved. The contents of this register are locked by the FLOCKDN bit.
15:0	-	-	**Reserved**

Flash Descriptor Observability Control (BIOS_FDOC) – Offset b4

Bit Range	Default	Access	Field Name and Description
30:15	-	-	**Reserved**
14:12	000b	RW	**Flash Descriptor Section Select (FDSS)** Selects which section within the loaded Flash Descriptor to observe. 000: Flash Signature and Descriptor Map 001: Component 010: Region 011: Master Others: Reserved
11:2	0h	RW	**Flash Descriptor Section Index (FDSI)** Selects the DW offset within the Flash Descriptor Section to observe.
1:0	-	-	**Reserved**

Flash Descriptor Observability Data (BIOS_FDOD) – Offset b8

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO/V	**Flash Descriptor Section Data (FDSD)** Returns the DW of data to observe as selected in the Flash Descriptor Observability Control.

Additional Flash Control (BIOS_AFC) – Offset c0

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	0b	RW/V/P	**Stop Prefetch on Flush Pending (SPFP)** When set to 1, the in progress of a prefetch will be ended if subsequence access from the master of the same interface is detected to be a cache-miss and read cache will be flushed. When set to 0, the prefetch will be allowed to complete prior to flushing.

Vendor Specific Component Capabilities for Component 0 (BIOS_SFDP0_VSCC0) – Offset c4

Bit Range	Default	Access	Field Name and Description
31	0b	RO/V	**Component Property Parameter Table Valid (CPPTV)** This bit is set to a 1 if the Flash Controller detects a valid SFDP Component Property Parameter Table in Component 0. Note: If this bit is set software must not overwrite bits that were initialized by hardware via SFDP discovery.
30	0b	RW/L	**Vendor Component Lock (VCL)** 0: The lock bit is not set 1: The Vendor Component Lock bit is set. This register locks itself when set.
29	0b	RW/V/L	**64k Erase Valid (EO_64k_VALID)** 0: The EO_64k opcode is not valid. 1: The EO_64k opcode is valid.
28	0b	RW/V/L	**4k Erase Valid (EO_4k_VALID)** 0: The EO_4k opcode is not valid. 1: The EO_4k opcode is valid.

Bit Range	Default	Access	Field Name and Description
27	0b	RW/L	**RPMC Supported (RPMC_SUPPORTED)** 0: The device does not support RPMC. 1: The device supports RPMC.
26	0b	RW/V/L	**Deep Powerdown Supported (DEEP_PWRDN_SUPPORTED)** 0: The device does not support Deep Powerdown. 1: The device supports Deep Powerdown.
25	0b	RW/V/L	**Suspend/Resume Supported (SUSPEND_RESUME_SUPPORTED)** 0: The device does not support Suspend/Resume. 1: The device supports Suspend/Resume.
24	0b	RW/V/L	**Soft Reset Supported (SOFT_RST_SUPPORTED)** 0: The device does not support Soft Reset. 1: The device supports Soft Reset.
23:16	00000000b	RW/V/L	**64k Erase Opcode (EO_64k)** This register is programmed with the Flash 64k sector erase instruction opcode for component 0. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
15:8	20h	RW/V/L	**4k Erase Opcode (EO_4k)** This register is programmed with the Flash 64k sector erase instruction opcode for component 0. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.

Bit Range	Default	Access	Field Name and Description
7:5	000b	RW/V/L	**Quad Enable Requirements (QER)** 000 = Part does not require a Quad Enable bit to be set, either because Quad is not supported or because the manufacturer somehow permanently enables Quad capability. 001 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to status register clears all bits in register 2, therefore status register writes MUST be two bytes. 010 = Part requires bit 6 of status register 1 to be set to enable quad IO. 011 = Part requires bit 7 of the configuration register to be set to enable Quad. 100 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to the status register does not clear the second byte. This register is locked by the Vendor Component Lock (VCL) bit. If the SFDP table contains this information, the flash controller loads these bits from the table. The flash controller uses this information to prevent clearing the QE bit in the flash device's status register when WSR=1.
4	0b	RW/V/L	**Write Enable on Write Status (WEWS)** 0 = 50h is the opcode to enable a status register write 1 : 06h is the opcode to enable a status register write This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. Note: Hardware ignores the state of this bit.

Bit Range	Default	Access	Field Name and Description
3	0b	RW/V/L	**Write Status Required (WSR)** 0 = No requirement to write to the Write Status Register prior to a write 1 = A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. Note: Hardware ignores the state of this bit.
2	0b	RW/V/L	**Write Granularity (WG)** 0 : Reserved 1 : 64 Byte This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. Note: Hardware ignores the state of this bit.
1:0	-	-	**Reserved**

Vendor Specific Component Capabilities for Component 1 (BIOS_SFDP1_VSCC1) – Offset c8

This register pertain to cycles targeting addresses outside of Component 0. The lockable bits in this register are locked when either CPPTV is set to 1 by hardware or when VCL is 1.

Bit Range	Default	Access	Field Name and Description
31	0b	RO/V	**Component Property Parameter Table Valid (CPPTV)** This bit is set to a 1 if the Flash Controller detects a valid SFDP Component Property Parameter Table in Component 1. Note: If this bit is set software must not overwrite bits that were initialized by hardware via SFDP discovery RO
30	-	-	**Reserved**
29	0b	RW/V/L	**64k Erase Valid (EO_64k_VALID)** 0: The EO_64k opcode is not valid. 1: The EO_64k opcode is valid.

Bit Range	Default	Access	Field Name and Description
28	0b	RW/V/L	**4k Erase Valid (EO_4k_VALID)** 0: The EO_4k opcode is not valid. 1: The EO_4k opcode is valid.
27	0b	RW/L	**RPMC Supported (RPMC_SUPPORTED)** 0 The device does not support RPMC. 1 The device supports RPMC.
26	0b	RW/V/L	**Deep Powerdown Supported (DEEP_PWRDN_SUPPORTED)** 0 The device does not support Deep Powerdown. 1 The device supports Deep Powerdown.
25	0b	RW/V/L	**Suspend/Resume Supported (SUSPEND_RESUME_SUPPORTED)** 1 the device supports Suspend/Resume
24	0b	RW/V/L	**Soft Reset Supported (SOFT_RST_SUPPORTED)** 0: The device does not support Soft Reset. 1: The device supports Soft Reset.
23:16	00000000b	RW/V/L	**64k Erase Opcode (EO_64k)** This register is programmed with the Flash 64k sector erase instruction opcode for component 1. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
15:8	20h	RW/V/L	**4k Erase Opcode (EO_4k)** This register is programmed with the Flash 4k subsector erase instruction opcode for component 1. Software must program this register if the SFDP table for this component does not show 4 kByte erase capability. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.

Bit Range	Default	Access	Field Name and Description
7:5	000b	RW/V/L	**Quad Enable Requirements (QER)** 000 = Part does not require a Quad Enable bit to be set, either because Quad is not supported or because the manufacturer somehow permanently enables Quad capability. 001 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to status register clears all bits in register 2, therefore status register writes MUST be two bytes. 010 = Part requires bit 6 of status register 1 to be set to enable quad IO. 011 = Part requires bit 7 of the configuration register to be set to enable Quad. 100 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to the status register does not clear the second byte. This register is locked by the Vendor Component Lock (VCL) bit. If the SFDP table contains this information, the flash controller loads these bits from the table. The flash controller uses this information to prevent clearing the QE bit in the flash device's status register when WSR=1.
4	0b	RW/V/L	**Write Enable on Write Status (WEWS)** 0 : 50h is the opcode to enable a status register write 1 : 06h is the opcode to enable a status register write This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
3	0b	RW/V/L	**Write Status Required (WSR)** 0: No requirement to write to the Write Status Register prior to a write 1: A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.

Bit Range	Default	Access	Field Name and Description
2	0b	RW/V/L	**Write Granularity (WG)** 0 : Reserved 1 : 64 Byte This register is locked by the Vendor Component Lock (VCL) bit orthe CPPTV bit. Note: Hardware ignores the state of this bit.
1:0	-	-	**Reserved**

Parameter Table Index (BIOS_PTINX) – Offset cc

Observability control for Component Property Tables. Note: The PTINX and PTDATA registers do not have any meaning in slave-attach flash mode because the SPI controller does not perform SFDP discovery.

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:14	00b	RW	**Supported Parameter Table (SPT)** Selects which supported parameter table to observe. 00 : Component 0 Property Parameter Table 01 : Component 1 Property Parameter Table 10 - 11 : Reserved
13:12	00b	RW	**Header or Data (HORD)** Select parameter table header DW vs Data DW. 00 : SFDP Header 01 : Parameter Table Header 10 : Data 11 : Reserved
11:2	0000000000b	RW	**Parameter Table DW Index (PTDWI)** Selects the DW offset within the parameter table to observe.

Bit Range	Default	Access	Field Name and Description
1:0	-	-	**Reserved**

Parameter Table Data (BIOS_PTDATA) – Offset d0

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO/V	**Parameter Table DW Data (PTDWD)** Returns the DW of data to observe as selected in the Parameter Table Index register. Note: The returned value of reserved fields in the SFDP header or table must be ignored by software. The flash controller may return either 0 or 1 for these fields.

SPI Bus Requester Status (BIOS_SBRS) – Offset d4

Bit Range	Default	Access	Field Name and Description
31	0b	RO/V	**TPM Access Ongoing (TPM_ACC_ONG)**
30	0b	RO/V	**eSPI Access Ongoing (ESPI_ACC_ONG)** This bit is only defined if eSPI and SPI are sharing the SPI bus.
29:18	-	-	**Reserved**
17:15	000b	RO/V	**Master 5 Status (M5STATUS)** See description under M1STATUS.
14:12	000b	RO/V	**Master 6 Status (M6STATUS)** See description under M1STATUS.
11:9	000b	RO/V	**Master 4 Status (M4STATUS)** See description under M1STATUS.

Bit Range	Default	Access	Field Name and Description
8:6	000b	RO/V	**Master 3 Status (M3STATUS)** See description under M1STATUS.
5:3	000b	RO/V	**Master 2 Status (M2STATUS)** See description under M1STATUS.
2:0	000b	RO/V	**Master 1 Status (M1STATUS)** Indicates whether this master has an outstanding transaction enqueued or in flight and the transaction type. 0xx : no transaction 100 : flash read transaction 101 : flash write transaction 110 : flash erase transaction 111 : flash RPMC transaction

Thermal Reporting Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	Vendor Identification (VID)	8086h
2h	2	Device Identification (DID)	XXh
4h	2	Command (CMD)	0h
6h	2	Status (STS)	10h
8h	1	Revision Identification (RID)	0h
9h	1	Programming Interface (PI)	0h
ah	1	Sub Class Code (SCC)	80h
bh	1	Base Class Code (BCC)	11h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
ch	1	Cache Line Size (CLS)	0h
dh	1	Latency Timer (LT)	0h
eh	1	Header Type (HTYPE)	80h
10h	4	Thermal Base (TBAR)	4h
14h	4	Thermal Base High DWord (TBARH)	0h
2ch	2	Subsystem Vendor ID (SVID)	0h
2eh	2	Subsystem ID (SID)	0h
34h	4	Capabilities Pointer (CAP_PTR)	50h
3ch	1	Interrupt Line (INTLN)	0h
3dh	1	Interrupt Pin (INTPN)	0h
40h	4	BIOS Assigned Thermal Base Address (TBARB)	4h
44h	4	BIOS Assigned Thermal Base High DWord (TBARBH)	0h
48h	1	Control Bits (CB)	0h
50h	2	PCI Power Management Capability ID (PID)	8001h
52h	2	Power Management Capabilities (PC)	23h
54h	4	Power Management Control And Status (PCS)	8h
80h	2	Message Signaled Interrupt Identifiers (MID)	5h
82h	2	Message Signaled Interrupt Message Control (MC)	0h
84h	4	Message Signaled Interrupt Message Address (MA)	0h
88h	4	Message Signaled Interrupt Message Data (MD)	0h

Vendor Identification (VID) – Offset 0

Vendor Identification

Bit Range	Default	Access	Field Name and Description
15:0	8086h	RO	**Vendor ID (VID)** Indicates that Intel is the vendor.

Device Identification (DID) – Offset 2

Device Identification

Bit Range	Default	Access	Field Name and Description
15:0	See Description	RO/V	**Device ID (DID)** Indicates the device ID number for Thermal controller. Referto the Device and Revision ID Table in Volume 1 for default value.

Command (CMD) – Offset 4

Command

Bit Range	Default	Access	Field Name and Description
14:11	-	-	**Reserved**
10	0b	RW	**Interrupt Disable (ID)** Enables the device to assert an INTx#. When set, the Thermal logics INTx# signal will be de-asserted. When cleared AND MSI is not enabled, the INTx# signal may be asserted. NOTE: this bit has no affect on MSI generation.
9	0b	RO	**Fast Back to Back Enable (FBE)** Not implemented. Hardwired to 0.
8	0b	RW	**SERR Enable (SEN)** When set to 1 and an error occurs, SERR# is signaled to the system.
7	0b	RO	**Wait Cycle Control (WCC)** Not implemented. Hardwired to 0.

Bit Range	Default	Access	Field Name and Description
6	0b	RO	**Parity Error Response (PER)** Not implemented. Hardwired to 0.
5	0b	RO	**VGA Palette Snoop (VPS)** Not implemented. Hardwired to 0.
4	0b	RO	**Memory Write and Invalidate Enable (MWI)** Not implemented. Hardwired to 0.
3	0b	RO	**Special Cycle Enable (SCE)** Not implemented. Hardwired to 0.
2	0b	RW	**Bus Master Enable (BME)** When 1, enables
1	0b	RW	**Memory Space Enable (MSE)** When set, enables memory space accesses to the Thermal registers.
0	0b	RO	**I/O Space (IOS)** The Thermal logic does not implement IO Space, therefore this bit is hardwired to 0.

Status (STS) – Offset 6

Status

Bit Range	Default	Access	Field Name and Description
15	0b	RO	**Detected Parity Error (DPE)** This bit is set whenever a parity error is seen on the internal interface for this function, regardless of the setting of bit 6 in the command register. Software clears this bit by writing a '1' to this bit location. The thermal sensor unit never checks parity.
14	0b	RW/1C	**SERR# Status (SERRS)** Not implemented. Hardwired to 0.
13	0b	RO	**Received Master Abort (RMA)** Not implemented. Hardwired to 0.

Bit Range	Default	Access	Field Name and Description
12	0b	RO	**Received Target Abort (RTA)** Not implemented. Hardwired to 0.
11	0b	RW/1C	**Signaled Target-Abort (STA)** May be asserted on errors
10:9	00b	RO	**DEVSEL# Timing Status (DEVT)** Does not apply. Hardwired to 0.
8	0b	RO	**Master Data Parity Error (MDPE)** Not implemented. Hardwired to 0.
7	0b	RO	**Fast Back to Back Capable (FBC)** Does not apply. Hardwired to 0.
6	-	-	**Reserved**
5	0b	RO	**66 MHz Capable (C66)** Does not apply. Hardwired to 0.
4	1b	RO	**Capabilities List Exists (CLIST)** Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	0b	RO	**Interrupt Status (IS)** Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted. This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register). This bit is not set if MSI is enabled.
2:0	-	-	**Reserved**

Revision Identification (RID) – Offset 8

Revision Identification

Bit Range	Default	Access	Field Name and Description
7:0	00h	RO/V	**Revision ID (RID)** Indicates the device specific revision identifier.

Programming Interface (PI) – Offset 9

Programming Interface

Bit Range	Default	Access	Field Name and Description
7:0	00h	RO	**Programming Interface (PI)** PCH Thermal logic has no standard programming interface.

Sub Class Code (SCC) – Offset a

Sub Class Code

Bit Range	Default	Access	Field Name and Description
7:0	80h	RO	**Sub Class Code (SCC)** Value assigned to PCH Thermal logic.

Base Class Code (BCC) – Offset b

Base Class Code

Bit Range	Default	Access	Field Name and Description
7:0	11h	RO	**Base Class Code (BCC)** Value assigned to PCH Thermal logic.

Cache Line Size (CLS) – Offset c

Cache Line Size

Bit Range	Default	Access	Field Name and Description
7:0	00h	RO	**Cache Line Size (CLS)** Doesn't apply to PCI Bus Target-only devices.

Latency Timer (LT) – Offset d

Latency Timer

Bit Range	Default	Access	Field Name and Description
7:0	00h	RO	**Latency Timer (LT)** Doesn't apply to PCI Bus Target-only devices.

Header Type (HTYPE) – Offset e

Header Type

Bit Range	Default	Access	Field Name and Description
7	1b	RO/V	**Multi-Function Device (MFD)** This bit is '0' because a multi-function device only needs to be marked as such in Function 0, and the Thermal registers are not in Function 0.
6:0	0000000b	RO	**Header Type (HTYPE)** Implements Type 0 Configuration header.

Thermal Base (TBAR) – Offset 10

This BAR creates 4K bytes of memory space to signify the base address of Thermal memory mapped configuration registers. This memory space is active when the Command (CMD) register Memory Space Enable (MSE) bit is set and either TBAR[31:12] or TBARH are programmed to a non-zero address. This BAR is owned by the Operating System, and allows the OS to locate the Thermal registers in system memory space.

Note: It is illegal to program the TBAR/TBARH range to overlap the TBARB/TBARBH range. An address can decode to one and only one BAR.

Bit Range	Default	Access	Field Name and Description
31:12	00000h	RW	**Thermal Base Address (TBA)** Base address for the Thermal logic memory mapped configuration registers. 4KB bytes are requested by hardwiring bits 11:4 to 0's.
11:4	-	-	**Reserved**
3	0b	RO	**Prefetchable (PREF)** Indicates that this BAR is NOT pre-fetchable.
2:1	10b	RO	**Address Range (ADDRNG)** Indicates that this BAR can be located anywhere in 64 bit address space.
0	0b	RO	**Space Type (SPTYP)** Indicates that this BAR is located in memory space.

Thermal Base High DWord (TBARH) – Offset 14

This BAR extension holds the high 32 bits of the 64 bit TBAR. In conjunction with TBAR, it creates 4 KB of memory space to signify the base address of Thermal memory mapped configuration registers.

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Thermal Base Address High (TBAH)** TBAR bits 61:32.

Subsystem Vendor ID (SVID) – Offset 2c

This register should be implemented for any function that could be instantiated more than once in a given system,. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other(s).

Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SID to create one 32-bit write. This register is not affected by D3HOT to D0 reset.

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW/O	**SVID (SVID)** These RWO bits have no PCH functionality.

Subsystem ID (SID) – Offset 2e

This register should be implemented for any function that could be instantiated more than once in a given system,. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other(s).

Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SVID to create one 32-bit write. This register is not affected by D3HOT to D0 reset.

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW/O	**SID (SID)** These RWO bits have no PCH functionality.

Capabilities Pointer (CAP_PTR) – Offset 34

Capabilities Pointer

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	50h	RO	**Capability Pointer (CP)** Indicates that the first capability pointer offset is offset 50h (Power Management Capability).

Interrupt Line (INTLN) – Offset 3c

Interrupt Line

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**Interrupt Line (INTLN)** PCH hardware does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

Interrupt Pin (INTPN) – Offset 3d

Interrupt Pin

Bit Range	Default	Access	Field Name and Description
6:4	-	-	**Reserved**
3:0	0h	RW/O	**Interrupt Pin (INTPN)** This reflects the value of interrupt pin used by this device.

BIOS Assigned Thermal Base Address (TBARB) – Offset 40

This BAR creates 4K bytes of memory space to signify the base address of Thermal memory mapped configuration registers. This memory space is active when TBARB.SPTYPEN is asserted. This BAR is owned by the BIOS, and allows the BIOS to locate the Thermal registers in system memory space. It is up to the SW to manage having 2 independent code routines both accessing a single hardware resource (the TS).

NOTE: This register has its own enable, bit [0] below. TBARB and TBARBH decode must NOT be affected by MSE or D3 condition. BIOS and/or SMM use this register outside of official OS visibility. Therefore this BAR must not be affected by OS setting or clearing of MSE or the power state.

Bit Range	Default	Access	Field Name and Description
31:12	00000h	RW	**Thermal Base Address (TBA)** Base address for the Thermal logic memory mapped configuration registers. 4KB bytes are requested by hardwiring bits 11:4 to 0's.
11:4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3	0b	RO	**Prefetchable (PREF)** Indicates that this BAR is NOT pre-fetchable.
2:1	10b	RO	**Address Range (ADDRNG)** Indicates that this BAR can be located anywhere in 64 bit address space.
0	0b	RW	**Space Type Enable (SPTYPEN)** When set to 1b by software, enables the decode of this memory BAR.

BIOS Assigned Thermal Base High DWord (TBARBH) – Offset 44

This BAR extension holds the high 32 bits of the 64 bit TBARB.

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Thermal Base Address High (TBAH)** TBAR bits 61:32.

Control Bits (CB) – Offset 48

Control Bits

Bit Range	Default	Access	Field Name and Description
6:1	-	-	**Reserved**
0	0b	RW	**UR Reporting Enable (URRE)** When '1', the agent will set the URD bit. If SERR# enable (SEN) is set, then the agent will also send SERR# to the system. Note that both URRE and SEN must be set to generate an SERR#.

PCI Power Management Capability ID (PID) – Offset 50

PCI Power Management Capability ID

Bit Range	Default	Access	Field Name and Description
15:8	80h	RO	**Next Capability (NEXT)** Indicates that the next capability is MSI.
7:0	01h	RO	**Cap ID (CAP)** Indicates that this pointer is a PCI power management capability

Power Management Capabilities (PC) – Offset 52

Power Management Capabilities

Bit Range	Default	Access	Field Name and Description
15:11	00000b	RO	**PME_Support (PMES)** Indicates PME# is not supported
10	0b	RO	**D2_Support (D2S)** The D2 state is not supported.
9	0b	RO	**D1_Support (D1S)** The D1 state is not supported.
8:6	000b	RO	**Aux_Current (AUXC)** PME# from D3COLD state is not supported, therefore this field is 000b..
5	1b	RO	**Device Specific Initialization (DSI)** Indicates that device-specific initialization is required.
4	-	-	**Reserved**
3	0b	RO	**PME Clock (PMEC)** Does not apply. Hardwired to 0.
2:0	011b	RO	**Version (VS)** Indicates support for Revision 1.2 of the PCI Power Management Specification.

Power Management Control And Status (PCS) – Offset 54

Power Management Control And Status

Bit Range	Default	Access	Field Name and Description
30:23	-	-	**Reserved**
22	0b	RO	**B2/B3 Support (B23)** Does not apply. Hardwired to 0.
21:16	-	-	**Reserved**
15	0b	RO	**PME Status (PMES)** This bit is always zero, since this PCI Function does not generate PME#
14:9	-	-	**Reserved**
8	0b	RO	**PME Enable (PMEE)** This bit is always zero, since this PCI Function does not generate PME#
7:4	-	-	**Reserved**
3	1b	RO	**No Soft Reset (NOSOFTRST)**), this bit indicates that devices transitioning from D3HOT to D0 becuase of PowerState commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3HOT to D0 initialized state, no additional operating system intervention is required to preserve Configuration Context beyong writing the PowerState bits.
2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1:0	00b	RW	**Power State (PS)** This field is used both to determine the current power state of the Thermal controller and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3HOT states, the Thermal controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. When software changes this value from the D3 HOT state to the D0 state, no internal warm (soft) reset is generated.

Message Signaled Interrupt Identifiers (MID) – Offset 80

Message Signaled Interrupt Identifiers

Bit Range	Default	Access	Field Name and Description
15:8	00h	RO/V	**Next Pointer (NEXT)** Next Pointer (NEXT): Indicates this is the latst pointer. When configured as a PCI Express device by PCIe Mode Strap, this value is set to 90h, else it is 00h to hide the PCI Express capability structure when configured as a PCI device (default).
7:0	05h	RO	**Capability ID (CID)** Capabilities ID indicates MSI.

Message Signaled Interrupt Message Control (MC) – Offset 82

Message Signaled Interrupt Message Control

Bit Range	Default	Access	Field Name and Description
14:8	-	-	**Reserved**
7	0b	RO	**64 Bit Address Capable (C64)** Capable of generating a 32-bit message only.
6:4	000b	RW	**Multiple Message Enable (MME)** These bits are RW for software compatibility, but only one message is ever sent by the root port.
3:1	000b	RO	**Multiple Message Capable (MMC)** Only one message is required.
0	0b	RW	**MSI Enable (MSIE)** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.

Message Signaled Interrupt Message Address (MA) – Offset 84

Message Signaled Interrupt Message Address

Bit Range	Default	Access	Field Name and Description
31:2	00000000 00000000 00000000 00000000 00b	RW	**Address (ADDR)** Lower 32 bits of the system specified message address, always DW aligned.
1:0	-	-	**Reserved**

Message Signaled Interrupt Message Data (MD) – Offset 88

Message Signaled Interrupt Message Data

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0000h	RW	**Data (DATA)** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[15:0]) during the data phase of the MSI memory write transaction.

Thermal Reporting Memory Mapped Registers

The Thermal Reporting Registers are located in the Memory Space mapped by TBAR (OS) and/or TBARB (BIOS), in the offset range from 0h to 0FFh.

All registers are reset by PLTRST#.

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	Temperature (TEMP)	0h
4h	1	Thermal Sensor Control (TSC)	0h
6h	1	Thermal Sensor Status (TSS)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8h	1	Thermal Sensor Enable And Lock (TSEL)	0h
ah	1	Thermal Sensor Reporting Enable And Lock (TSREL)	0h
ch	1	Thermal Sensor SMI Control (TSMIC)	0h
10h	2	Catastrophic Trip Point (CTT)	1FFh
14h	2	Thermal Alert High Value (TAHV)	0h
18h	2	Thermal Alert Low Value (TALV)	0h
1ch	2	Thermal Sensor Power Management (TSPM)	800h
40h	4	Throttle Levels (TL)	0h
50h	4	Throttle Level 2 (TL2)	0h
60h	2	PCH Hot Level (PHL)	0h
62h	1	PHL Control (PHLC)	0h
80h	1	Thermal Alert Status (TAS)	0h
82h	1	PCI Interrupt Event Enables (TSPIEN)	0h
84h	1	General Purpose Event Enables (TSGPEN)	0h
f0h	1	Thernak Controller Function Disable (TCFD)	0h

Temperature (TEMP) – Offset 0

Temperature

Bit Range	Default	Access	Field Name and Description
14:9	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
8:0	000h	RO	**TS Reading (TSR)** The die temperature with resolution of 0.5 degree C and an offset of -50C. Thus a reading of 0x121 is 94.5C.

Thermal Sensor Control (TSC) – Offset 4

This register controls the operation of the thermal sensor.

Bit Range	Default	Access	Field Name and Description
7	0b	RW/1L	**Policy Lock-Down Bit (PLDB)** When written to 1, this bit prevents any more writes to this register (offset 04h) and to CTT (offset 0x10)
6:1	-	-	**Reserved**
0	0b	RW/L	**Catastrophic Power-Down Enable (CPDE)** When set to 1, the power management logic (PMC) transitions to the S5 state when a catastrophic temperature is detected by the sensor. The transition to the S5 state must be unconditional (like the Power Button Override Function). Note that the thermal sensor and response logic is in the core/main power well, therefore, detection of a catastrophic temperature is limited to times when this well is powered and out of reset.

Thermal Sensor Status (TSS) – Offset 6

This read only register provides trip point and other status of the thermal sensor.

Bit Range	Default	Access	Field Name and Description
6:5	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
4	0b	RO	**Thermal Sensor Dynamic Shutdown Status (TSDSS)** Thermal Sensor Dynamic Shutdown Status (TSDSS): This bit indicates the status of the thermal sensor circuit when TSEL.ETS=1. 1: thermal sensor is fully operational 0: thermal sensor is in a dynamic shutdown state
3	0b	RW/1C	**GPE Status (GPES)** Set when GPE is enabled for a trip event. SW must write a 1 to this bit to clear the GPE status. Note that GPE can be configured to cause an SMI or SCI. As long as this bit is set, the GPE indication to the global GPE logic is asserted..
2	0b	RW/1C	**SMI Status (SMIS)** Set when SMI is enabled for a trip event. SW must write a 1 to this bit to clear the SMI status. As long as this bit is set, the SMI indication to the global SMI logic is asserted.
1:0	-	-	**Reserved**

Thermal Sensor Enable And Lock (TSEL) – Offset 8

This register controls the operation of the thermal sensor.

Bit Range	Default	Access	Field Name and Description
7	0b	RW/1L	**Policy Lock-Down Bit (PLDB)** Policy Lock-Down Bit: When written to 1, this bit prevents any more writes to this register and to TTCB, Test1, Test2, Test3, Test4, Test5, Test6 and Test7 registers.
6:1	-	-	**Reserved**
0	0b	RW/L	**Enable TS (ETS)** 1: Enables the thermal sensor. Until this bit is set, no thermometer readings or trip events will occur. If SW reads the TEMP register before the sensor is enabled, it will read 0x0. The value of this bit is sent to the thermal sensor. NOTE: if the sensor is running and valid temperatures have been captured in TEMP and then ETS is cleared, TEMP will retain its old value. Clearing ETS does not force TEMP to 0x00. 0: Disables the sensor.

Thermal Sensor Reporting Enable And Lock (TSREL) – Offset a

Thermal Sensor Reporting Enable and Lock

Bit Range	Default	Access	Field Name and Description
7	0b	RW/1L	**Policy Lock-Down Bit (PLDB)** Policy Lock-Down Bit: When written to 1, this bit prevents any more writes to this register (offset 0Ah)
6:1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	0b	RW/L	**Enable SMBus Temperature Reporting (ESTR)** 1: Enables the reporting of the PCH temperature to the SMBus. Note that this must also be set if ME needs access to the PCH temperature. Once enabled this bit should not be cleared by SW. If it is cleared then the EC may get an undefined value. SW has no need to dynamically disable and then re-enable this bit. 0: Disables EC temperature reporting.

Thermal Sensor SMI Control (TSMIC) – Offset c

This register controls the operation of the thermal sensor.

Bit Range	Default	Access	Field Name and Description
7	0b	RW/1L	**Policy Lock-Down Bit (PLDB)** When written to 1, this bit prevents any more writes to this register (offset 0Ch)
6:1	-	-	**Reserved**
0	0b	RW/L	**SMI Enable on Alert Thermal Sensor Trip (ATST)** 1: Enables SMI# assertions on alert thermal sensor events for either low-to-high or high-to-low events. (Both edges are enabled by this one bit.) 0: Disables SMI# assertions for alert thermal events

Catastrophic Trip Point (CTT) – Offset 10

Catastrophic Trip Point

Bit Range	Default	Access	Field Name and Description
14:9	-	-	**Reserved**
8:0	111111111b	RW/L	**Catastrophic Temperature TRIP (CTRIP)** When the current temperature reading is = to the value in this register, a catastrophic trip event is signaled. The value of this register must not be changed while TSEL.ETS is set. The value in this register is sent to the thermal sensor. This register is locked by TSC[7]

Thermal Alert High Value (TAHV) – Offset 14

Thermal Alert High Value

Bit Range	Default	Access	Field Name and Description
14:9	-	-	**Reserved**
8:0	000h	RW	**Alert High (AH)** Sets the high value for the alert indication. The value of this register must not be changed while TSEL.ETS is set. The value in this register is sent to the thermal sensor. This register is not lockable, so that SW can change the values during runtime.

Thermal Alert Low Value (TALV) – Offset 18

Thermal Alert Low Value

Bit Range	Default	Access	Field Name and Description
14:9	-	-	**Reserved**
8:0	000h	RW	**Alert Low (AL)** Sets the low value for the alert indication. The value of this register must not be changed while TSEL.ETS is set. The value in this register is sent to the thermal sensor. This register is not lockable, so that SW can change the values during runtime.

Thermal Sensor Power Management (TSPM) – Offset 1c

Thermal Sensor Power Management

Bit Range	Default	Access	Field Name and Description
15	0b	RW/1L	**Thermal Sensor Power Management Lock (TSPMLOCK)** Thermal Sensor Power Management Lock (TSPMLOCK): Setting this bit to a 1 causes the rest of the bits in this register to be locked.
14	0b	RW/L	**Dynamic Thermal Sensor Shutdown in S0 Idle Enable (DTSSS0EN)** Dynamic Thermal Sensor Shutdown in S0 idle Enable (DTSSS0EN): 1: Dynamic thermal sensor shutdown in S0 idle is enabled. When set to 1, the power management logic shuts down the thermal sensor when the CPU is in a C-state and TEMP.TSR andlt;= LTT.LTT. 0: Dynamic thermal sensor shutdown in S0 idle is disabled

Bit Range	Default	Access	Field Name and Description
13	0b	RW/L	**Dynamic Thermal Sensor Shutdown in C0 Allowed (DTSSIC0)** Dynamic Thermal Sensor Shutdown in C0 Allowed (DTSSIC0) 0: CPU must be in a non-C0 state to allow PCH thermal sensor shutdown 1: CPU can be in a C0 or non-C0 state to allow PCH thermal sensor shutdown.
12	-	-	**Reserved**
11:9	100b	RW/L	**Maximum Thermal Sensor Shutdown Time (MAXTSST)** Maximum Thermal Sensor Shutdown Time (MAXTSST) - sets the maximum time that the thermal sensor will be held in a shutdown state assuming no other wake conditions. This register is used to set the expiration time of a timer that is used to wake up the thermal sensor on expiration. 000: 1 s 001: 2 s 010: 4 s 011: 8 s 100: 16 s 101-111: Reserved

Bit Range	Default	Access	Field Name and Description
8:0	0000000 00b	RW	**Low Temp Threshold (LTT)** Low Temp Threshold (LTT) - Sets the low maximum temp value used for dynamic thermal sensor shutdown consideration. See DTSSS0EN for details. This register field is not lockable, so that SW can change the values during runtime.

Throttle Levels (TL) – Offset 40

Throttle Levels

Bit Range	Default	Access	Field Name and Description
31	0b	RW/1L	**TT.Lock (TTL)** When set to 1, this entire register (TL) is locked and remains locked until the next platform reset.
30	0b	RW/L	**TT.State13 Enable (TT13EN)** When set to 1, then PMSync state 13 will force at least T2 state.
29	0b	RW/L	**TT Enable (TTEN)** When set the thermal throttling states are enabled. At reset, BIOS must set bits 28:0 and then do a separate write to set bit 29 to enable throttling. SW may set bit 31 at the same time it sets bit 29 if it wishes to lock the register. If SW wishes to change the values of 28:0, it must first clear the TTEN bit, then change the values in 28:0, and then re-enable TTEN. It is legal to set bits 31, 30 and 29 with the same write. This bit must not be set unless the thermal sensor is already enabled (set TSC[7]=1 and TSC[3:2] = 10).

Bit Range	Default	Access	Field Name and Description
28:20	0000000 00b	RW/L	**T2 Level (T2L)** When TTEN = 1 AND TSE = 1 AND (T2L = TSR[8:0] T1L), then the system is in T2 state. When TTEN = 1 AND TSE = 1 AND (TSR[8:0] T2L), then the system is in T3 state. NOTE: the T3 condition overrides PMSync[13] and forces the system to T3 if both cases are true. SW NOTE: T2L must be programmed to a value greater than T1L if TTEN=1
19	-	-	**Reserved**
18:10	0000000 00b	RW/L	**T1 Level (T1L)** When TTEN = 1 AND TSE = 1 AND (T1L = TSR[8:0] T0L), then the system is in T1 state. SW NOTE: T1L must be programmed to a value greater than T0L if TTEN=1
9	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
8:0	0000000 00b	RW/L	**T0 Level (T0L)** When TEMP.TSR[8:0] is less than or equal to T0L OR TT.Enable is 0 OR TSE = 0, then the system is in T0 state.

Throttle Level 2 (TL2) – Offset 50

Throttle Level 2

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15	0b	RW/1L	**TL2 lock (TL2LOCK)** TL2.Lock - When set to 1, this entire register (TL2) is locked and remains locked until the next platform reset.
14	0b	RW/L	**PMC Throttling Enable (PMCTEN)** PMC Throttling Enable (PMCTEN) - When set to 1 and the PMC is requesting throttling, force at least the T-state that PMC is requesting.
13:0	-	-	**Reserved**

PCH Hot Level (PHL) – Offset 60

PCH Hot Level

Bit Range	Default	Access	Field Name and Description
15	0b	RW/L	**PHL Enable (PHLE)** When set and the current temperature reading, TSR, is greater than or equal to PHLL, then the PCHHOT# pin will be asserted (active low).
14:9	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
8:0	0000000 00b	RW/L	**PHL Level (PHLL)** Temperature value used for PCHHOT# pin.

PHL Control (PHLC) – Offset 62

PHL Control

Bit Range	Default	Access	Field Name and Description
6:1	-	-	**Reserved**
0	0b	RW/1L	**PHL Lock (PHLL)** When written to a 1, then both PHL and PHLC are locked

Thermal Alert Status (TAS) – Offset 80

Thermal Alert Status

Bit Range	Default	Access	Field Name and Description
6:2	-	-	**Reserved**
1	0b	RW/1C	**Alerth High-to-Low Event (AHLE)** 1: Indicates that a Hot Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. 0: No trip for this event Software must write a 1 to clear this status bit.

Bit Range	Default	Access	Field Name and Description
0	0b	RW/1C	**Alert Low-to-High Event (ALHE)** 1: Indicates that an Aux Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. 0: No trip for this event Software must write a 1 to clear this status bit.

PCI Interrupt Event Enables (TSPIEN) – Offset 82

This register controls the conditions that result in the PCI Interrupt signal from the Thermal Sensor (TS) logic to assert. The interrupt may be either pin-based or MSI, based on how SW programmed the PCI header.

Bit Range	Default	Access	Field Name and Description
6:2	-	-	**Reserved**
1	0b	RW	**Alert High-to-Low Enable (AHLEN)** When set to 1, the thermal sensor logic asserts the Thermal logic PCI INTx signal when the corresponding status bit is set in the Thermal Error Status register. When cleared, the corresponding status bit does not result in PCI INTx.
0	0b	RW	**Alert Low-to-High Enable (ALHEN)** See the description for bit 1.

General Purpose Event Enables (TSGPEN) – Offset 84

This register controls the conditions that result in the General Purpose Event (GPE) flag (TSS[3]) being set. When the TS GPE signal asserts, the GPE block reports a 1 in the TCOSCI_STS bit.

Bit Range	Default	Access	Field Name and Description
6:2	-	-	**Reserved**
1	0b	RW	**Alert High-to-Low Enabble (AHLEN)** When set to 1, the thermal sensor logic asserts its General Purpose Event signal to the GPE block when the corresponding status bit is set in the Thermal Error Status register. When cleared, the corresponding status bit does not result in the GPE signal assertion.
0	0b	RW	**Alert Low-to-High Enable (ALHEN)** See the description for bit 1.

Thernak Controller Function Disable (TCFD) – Offset f0

Function Disable bit

Bit Range	Default	Access	Field Name and Description
6:1	-	-	**Reserved**
0	0b	RW	**Thermal Controller Disable (TCD)** Thermal Controller Disable (TCD): When set, the the Thermal Controller, is disabled.

UART Additional Memory Mapped Registers

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
200h	4	CLOCKS (CLOCKS)	0h
204h	4	RESETS (RESETS)	0h
210h	4	Active LTR (ACTIVELTR_VALUE)	800h
214h	4	IDLE LTR (IDLELTR_VALUE)	800h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
218h	4	reg_TX_BYTE_COUNT (TX_BYTE_COUNT)	0h
21ch	4	reg_RX_BYTE_COUNT (RX_BYTE_COUNT)	0h
228h	4	SW SCRATCH 0 (SW_SCRATCH_0)	0h
238h	4	reg_CLOCK_GATE (CLOCK_GATE)	0h
240h	4	reg_REMAP_ADDR_LO (REMAP_ADDR_LO)	0h
244h	4	reg_REMAP_ADDR_HI (REMAP_ADDR_HI)	0h
24ch	4	reg_DEVIDLE_CONTROL (DEVIDLE_ CONTROL)	8h
2fch	4	Capabilities (CAPABLITIES)	10h

CLOCKS (CLOCKS) – Offset 200

private clock configuraton

Bit Range	Default	Access	Field Name and Description
31	0h	RW	**clk_update (clk_update)** Update the clock divider after seeting new m and n values. 0 – No clock Update 1 – Clock gets updated.
30:16	0h	RW	**N_VAL (n_val)** This is the denominator value (N) for the M over N divider logic that creates CLK_ OUT. Used to generate the input clk to the UART.
15:1	0h	RW	**M_VAL (m_val)** The numerator value (M) for the M over N divider logic that creates the CLK_ OUT.Used to generate the input clk to the UART.

Bit Range	Default	Access	Field Name and Description
0	0h	RW	**clk_en (clk_en)** UART Serial Clock (output of M/N, input to UART) Clock Enable 0 – Clock disabled 1 – Clock Enabled.

RESETS (RESETS) – Offset 204

software reset

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**
2	0h	RW	**reset_dma (reset_dma)** reset the dma controller
1:0	-	-	**Reserved**

Active LTR (ACTIVELTR_VALUE) – Offset 210

Bit Range	Default	Access	Field Name and Description
31	0h	RO	**Non_Snoop_Requirment (non_snoop_requirment)** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
30:29	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
28:26	0h	RO	**Non_Snoop_latency_scale (non_snoop_latency_scale)** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale (1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
25:16	0h	RO	**Non_Snoop_value (non_snoop_value)** 10-bit latency value
15	0h	RW	**Snoop_Requirment (snoop_requirment)** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	-	-	**Reserved**
12:10	2h	RW	**Snoop_latency_scale (snoop_latency_scale)** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale (1us -> 32ms total span) only. Writes to this CSR which do not match those values will be dropped completely, next read will return previous value.
9:0	0h	RW	**Snoop_value (snoop_value)** 10-bit latency value

IDLE LTR (IDLELTR_VALUE) – Offset 214

Bit Range	Default	Access	Field Name and Description
31	0h	RO	**Non_Snoop_Requirment (non_snoop_requirment)** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
30:29	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
28:26	0h	RO	**Non_Snoop_latency_scale (non_snoop_latency_scale)** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale (1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
25:16	0h	RO	**Non_Snoop_value (non_snoop_value)** 10-bit latency value
15	0h	RW	**Snoop_Requirment (snoop_requirment)** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	-	-	**Reserved**
12:10	2h	RW	**Snoop_latency_scale (snoop_latency_scale)** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h	RW	**Snoop_value (snoop_value)** 10-bit latency value

reg_TX_BYTE_COUNT (TX_BYTE_COUNT) – Offset 218

Bit Range	Default	Access	Field Name and Description
31	0h	RO	**tx_count_overflow (tx_count_overflow)** 0= count valid 1= count overflow/invalid
30:24	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
23:0	0h	RO	**tx_byte_count (tx_byte_count)** 24-bit up-counter which counts the number of TX Bytes on the Serial bus. The Counter is forced to be cleared by software Read.

reg_RX_BYTE_COUNT (RX_BYTE_COUNT) – Offset 21c

Bit Range	Default	Access	Field Name and Description
31	0h	RO	**rx_count_overflow (rx_count_overflow)** 0= count valid 1= count overflow/invalid
30:24	-	-	**Reserved**
23:0	0h	RO	**rx_byte_count (rx_byte_count)** 24-bit up-counter which counts the number of RX Bytes on the Serial bus. The Counter is forced to be cleared by software Read.

SW SCRATCH 0 (SW_SCRATCH_0) – Offset 228

NOTE: The same registers are available at the following offsets:

SW SCRATCH 1: offset 22Ch

SW SCRATCH 2: offset 230h

SW SCRATCH 3: offset 234h

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**reg_SW_Scratch_0 (SW_Scratch_0)** Scratch Pad Register for SW to generated Local DATA for iDMA

reg_CLOCK_GATE (CLOCK_GATE) – Offset 238

Bit Range	Default	Access	Field Name and Description
30:4	-	-	**Reserved**
3:2	0h	RW	**sw_dma_clk_ctl (sw_dma_clk_ctl)** DMA Clock Control 00 = Dyanamic Clock Gate Enable 01 = Reserved 10 = Force iDMA Clock off 11 = Force iDMA Clock on
1:0	0h	RW	**sw_ip_clk_ctl (sw_ip_clk_ctl)** Clock Control 00 = Dyanamic Clock Gate Enable 01 = Reserved 10 = Force IP Clocks off 11 = Force IP Clocks on

reg_REMAP_ADDR_LO (REMAP_ADDR_LO) – Offset 240

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**uart_remap_addr_low (uart_remap_addr_low)** Low 32 bits of BAR address read by SW

reg_REMAP_ADDR_HI (REMAP_ADDR_HI) – Offset 244

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**uart_remap_addr_high (uart_remap_addr_high)** High 32 bits of BAR address read by SW

reg_DEVIDLE_CONTROL (DEVIDLE_CONTROL) – Offset 24c

dev idle control register

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4	0h	RO	**Interrupt Request Capable (intr_req_capable)** Set to '1' by HW if it is capable of generating an interrupt on command completion, else '0'.
3	1h	RW/1C	**Restore Require (restore_required)** When set (by HW), SW must restore state to the controller. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a '1'. This bit will be set on initial power up.
2	0h	RW	**Device Idle (devidle)** SW sets this bit to '1' to move the function into the DevIdle state. Writing this bit to '0' will return the function to the fully active D0 state (D0i0).
1	-	-	**Reserved**
0	0h	RO	**Command-In-Progress (cmd_in_progress)** HW sets this bit on a 1->0 or 0->1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is illegal for SW to write to any bit in this register. HW clears this bit upon completing the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit.If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW.SW writes to this bit have no effect.

Capabilities (CAPABLITIES) – Offset 2fc

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
8	0h	RO	**DMA Present (iDMA_present)** 0= DMA present 1= DMA not present
7:4	1h	RO	**Instant Type (instance_type)** 0000 = IC2 0001 = UART 0010 = SPI 0011 – 1111 = Reserved
3:0	0h	RO	**Instant Number (instance_number)**

UART DMA Controller Registers

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
800h	4	DMA Transfer Source Address Low (SAR_LO0)	0h
804h	4	DMA Transfer Source Address High (SAR_HI0)	0h
808h	4	DMA Transfer Destination Address Low (DAR_LO0)	0h
820h	4	Source Status (SSTAT0)	0h
828h	4	Destination Status (DSTAT0)	0h
80ch	4	DMA Transfer Destination Address High (DAR_HI0)	0h
810h	4	CH 0 Linked List Pointer Low (LLP_LO0)	0h
814h	4	CH0 Linked List Pointer High (LLP_HI0)	0h
830h	4	Source Status Address Low (SSTATAR_LO0)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
834h	4	Source Status Address High (SSTATAR_HI0)	0h
838h	4	Destination Status Address Low (DSTATAR_LO0)	0h
83ch	4	Destination Status Address High (DSTATAR_HI0)	0h
840h	4	DMA Transfer Configuration Low (CFG_LO0)	203h
844h	4	DMA Transfer Configuration High (CFG_HI0)	0h
848h	4	Source Gather (SGR0)	0h
850h	4	Destination Scatter (DSR0)	0h
868h	4	CH 1 Linked List Pointer Low (LLP_LO1)	0h
86ch	4	CH1 Linked List Pointer High (LLP_HI1)	0h
ac0h	4	Raw Interrupt Status (RawTfr)	0h
ac8h	4	Raw Status for Block Interrupts (RawBlock)	0h
ad0h	4	Raw Status for Source Transaction Interrupts (RawSrcTran)	0h
ad8h	4	Raw Status for Destination Transaction Interrupts (RawDstTran)	0h
ae0h	4	Raw Status for Error Interrupts (RawErr)	0h
ae8h	4	Interrupt Status (StatusTfr)	0h
af0h	4	Status for Block Interrupts (StatusBlock)	0h
af8h	4	Status for Source Transaction Interrupts (StatusSrcTran)	0h
b00h	4	Status for Destination Transaction Interrupts (StatusDstTran)	0h
b08h	4	Status for Error Interrupts (StatusErr)	0h
b10h	4	Mask for Transfer Interrupts (MaskTfr)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
b18h	4	Mask for Block Interrupts (MaskBlock)	0h
b20h	4	Mask for Source Transaction Interrupts (MaskSrcTran)	0h
b28h	4	Mask for Destination Transaction Interrupts (MaskDstTran)	0h
b30h	4	Mask for Error Interrupts (MaskErr)	0h
b38h	4	Clear for Transfer Interrupts (ClearTfr)	0h
b40h	4	Clear for Block Interrupts (ClearBlock)	0h
b48h	4	Clear for Source Transaction Interrupts (ClearSrcTran)	0h
b50h	4	Clear for Destination Transaction Interrupts (ClearDstTran)	0h
b58h	4	Clear for Error Interrupts (ClearErr)	0h
b60h	4	Combined Status register (StatusInt)	0h
b98h	4	DMA Configuration (DmaCfgReg)	0h
ba0h	4	DMA Channel Enable (ChEnReg)	0h
818h	4	Control Register Low (CTL_LO0)	0h
81ch	4	Control Register High (CTL_HI0)	0h

DMA Transfer Source Address Low (SAR_LO0) – Offset 800

NOTE: SAR_LO0 is for DMA Channel 0. The same register definition,SAR_LO1, is available for Channel 1 at address 858h.

SAR_LO0 (CH0): offset 800h

SAR_LO1 (CH1): offset 858h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**(SAR_LO)** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected). 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

DMA Transfer Source Address High (SAR_HI0) – Offset 804

NOTE: SAR_HI0 is for DMA Channel 0. The same register definition, SAR_HI1, is available for Channel 1 at address 85Ch.

SAR_HI0 (CH0): offset 804h

SAR_HI1 (CH1): offset 85Ch

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**(SAR_HI)** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

DMA Transfer Destination Address Low (DAR_LO0) – Offset 808

NOTE: DAR_LO0 is for DMA Channel 0. The same register definition, DAR_LO1, is available for Channel 1 at address 860h.

DAR_LO0 (CH0): offset 808h

DAR_LO1 (CH1): offset 860h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**(DAR_LO)** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

Source Status (SSTAT0) – Offset 820

NOTE: SSTAT0 is for DMA Channel 0. The same register definition, SSTAT1, is available for Channel 1 at address 878h.

SSTAT0 (CH0): offset 820h

SSTAT1 (CH1): offset 878h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.

Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**(SSTAT)** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

Destination Status (DSTAT0) – Offset 828

NOTE: DSTAT0 is for DMA Channel 0. The same register definition, DSTAT1, is available for Channel 1 at address 880h.

DSTAT0 (CH0): offset 828h

DSTAT1 (CH1): offset 880h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.

Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**(DSTAT)** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface.

DMA Transfer Destination Address High (DAR_HI0) – Offset 80c

NOTE: DAR_HI0 is for DMA Channel 0. The same register definition, DAR_HI1, is available for Channel 1 at address 864h.

DAR_HI0 (CH0): offset 80Ch

DAR_HI1 (CH1): offset 864h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	

Bit Range	Default	Access	(DAR_HI) Field Name and Description
			Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

CH 0 Linked List Pointer Low (LLP_LO0) – Offset 810

LLP_LO0 is for DMA Channel 0.

The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Bit Range	Default	Access	Field Name and Description
31:2	0000000 0h	RW	**LLP Address Low (LOC)** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit. Note: SW should avoid a LLP lower 32 bits equal to 0s assigned to 4GB boundary address.
1:0	-	-	**Reserved**

CH0 Linked List Pointer High (LLP_HI0) – Offset 814

LLP_HI0 is for DMA Channel 0.

The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Bit Range	Default	Access	Field Name and Description
31:2	0000000 0h	RW	**LLP Address High (LOC)** LLP Upper address.
1:0	-	-	**Reserved**

Source Status Address Low (SSTATAR_LO0) – Offset 830

NOTE: SSTATAR_LO0 is for DMA Channel 0. The same register definition, SSTATAR_LO1, is available for Channel 1 at address 888h.

SSTATAR_LO0(CH0): offset 830h

SSTATAR_LO1(CH1): offset 888h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**(SSTATAR_LO)** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

Source Status Address High (SSTATAR_HI0) – Offset 834

NOTE: SSTATAR_HI0 is for DMA Channel 0. The same register definition, SSTATAR_HI1, is available for Channel 1 at address 88Ch.

SSTATAR_HI0(CH0): offset 834h

SSTATAR_HI1(CH1): offset 88Ch

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**(SSTATAR_HI)** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block.

Destination Status Address Low (DSTATAR_LO0) – Offset 838

NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_LO1, is available for Channel 1 at address 890h.

DSTATAR_LO0(CH0): offset 838h

DSTATAR_LO1(CH1): offset 890h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**(DSTATAR_LO)** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

Destination Status Address High (DSTATAR_HI0) – Offset 83c

NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_HI1, is available for Channel 1 at address 894h.

DSTATAR_HI0(CH0): offset 83Ch

DSTATAR_HI1(CH1): offset 894h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Bit Range	Default	Access	Field Name and Description
31:0	0h	RW	**(DSTATAR_HI)** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

DMA Transfer Configuration Low (CFG_LO0) – Offset 840

NOTE: CFG_LO0 is for DMA Channel 0. The same register definition, CFG_LO1, is available for Channel 1 at address 898h.

CFG_LO0(CH0): offset 840h

CFG_LO1(CH1): offset 898h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Bit Range	Default	Access	Field Name and Description
31	0h	RW	**(RELOAD_DST)** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
30	0h	RW	**(RELOAD_SRC)** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	-	-	**Reserved**
21	0h	RW	**(SRC_OPT_BL)** Optimize Source Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ SRC_MSIZE)) *** This bit should be set to (0) if Source HW-Handshake is enabled
20	0h	RW	**(DST_OPT_BL)** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ DST_MSIZE)) *** This bit should be set to (0) if Destination HW-Handshake is enabled

Bit Range	Default	Access	Field Name and Description
19	0h	RW	**(SRC_HS_POL)** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h	RW	**(DST_HS_POL)** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17:11	-	-	**Reserved**
10	0b	RW	**(CH_DRAIN)** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND is asserted.
9	1b	RO	**(FIFO_EMPTY)** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default	Access	Field Name and Description
8	0h	RW	**(CH_SUSP)** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h	RW	**(SS_UPD_EN)** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
6	0h	RW	**(DS_UPD_EN)** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h	RW	**(CTL_HI_UPD_EN)** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3	0h	RW	**(HSHAKE_NP_WR)** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted) This bit must be set to 1 for proper operation
2	0h	RW	**(ALL_NP_WR)** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h	RW	**(SRC_BURST_ALIGN)** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h	RW	**(DST_BURST_ALIGN)** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

DMA Transfer Configuration High (CFG_HI0) – Offset 844

NOTE: CFG_HI0 is for DMA Channel 0. The same register definition, CFG_HI1, is available for Channel 1 at address 89Ch.

CFG_HI0(CH0): offset 844h

CFG_HI1(CH1): offset 89Ch

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Bit Range	Default	Access	Field Name and Description
30:28	-	-	**Reserved**
27:18	0h	RW	**(WR_ISSUE_THD)** Write Issue Threshold. Used to relax the issue criterion for Writes. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h	RW	**(RD_ISSUE_THD)** Read Issue Threshold. Used to relax the issue criterion for Reads. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_ MSIZE)*TW.
7:4	0h	RW	**(DST_PER)** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.
3:0	0h	RW	**(SRC_PER)** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

Source Gather (SGR0) – Offset 848

NOTE: SGR0 is for DMA Channel 0. The same register definition, SGR1, is available for Channel 1 at address 8A0h.

SGR0(CH0): offset 848h

SGR1(CH1): offset 8A0h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address

increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Bit Range	Default	Access	Field Name and Description
31:20	0h	RW	**(SGC)** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h	RW	**(SGI)** Source gather interval.

Destination Scatter (DSR0) – Offset 850

NOTE: DSR0 is for DMA Channel 0. The same register definition, DSR1, is available for Channel 1 at address 8A8h.

DSR0(CH0): offset 850h

DSR1(CH1): offset 8A8h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Bit Range	Default	Access	Field Name and Description
31:20	0h	RW	**(DSC)** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries.
19:0	0h	RW	**(DSI)** Destination scatter interval.

CH 1 Linked List Pointer Low (LLP_LO1) – Offset 868

LLP_LO1 is for DMA Channel 1.

The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Bit Range	Default	Access	Field Name and Description
31:2	0000000 0h	RW	**LLP Address Low (LOC)** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit. Note: SW should avoid a LLP lower 32 bits equal to 0s assigned to 4GB boundary address.
1:0	-	-	**Reserved**

CH1 Linked List Pointer High (LLP_HI1) – Offset 86c

LLP_LH1 is for DMA Channel 1.

The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Bit Range	Default	Access	Field Name and Description
31:2	0000000 0h	RW	**LLP Address High (LOC)** LLP upper address.
1:0	-	-	**Reserved**

Raw Interrupt Status (RawTfr) – Offset ac0

Interrupt events are stored in these Raw Interrupt Status registers before masking:

RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status

register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2

raw transfer complete interrupt.

Each bit in these registers is cleared by writing a 1 to the corresponding

location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers

The following RAW registers are available in the DMA

RawTfr - Raw Status for Transfer Interrupts

RawBlock - Raw Status for Block Interrupts Register

RawSrcTran - Raw Status for Source Transaction Interrupts Register

RawDstTran - Raw Status for Destination Transaction Interrupts Register

RawErr - Raw Status for Error Interrupts Register

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**(RAW)** Bit0 for channel 0 and bit 1 for channel 1.

Raw Status for Block Interrupts (RawBlock) – Offset ac8

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**(RAW)** Bit 0 for channel 0 and bit 1 for channel 1.

Raw Status for Source Transaction Interrupts (RawSrcTran) – Offset ad0

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**(RAW)** Bit 0 for channel 0 and bit 1 for channel 1.

Raw Status for Destination Transaction Interrupts (RawDstTran) – Offset ad8

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**(RAW)** Bit 0 for channel 0 and bit 1 for channel 1.

Raw Status for Error Interrupts (RawErr) – Offset ae0

Interrupt events are stored in these Raw Interrupt Status registers before masking:

RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status

register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2

raw transfer complete interrupt.

Each bit in these registers is cleared by writing a 1 to the corresponding

location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers

The following RAW registers are available in the DMA

RawTfr - Raw Status for Transfer Interrupts

RawBlock - Raw Status for Block Interrupts Register

RawSrcTran - Raw Status for Source Transaction Interrupts Register

RawDstTran - Raw Status for Destination Transaction Interrupts Register

RawErr - Raw Status for Error Interrupts Register

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**(RAW)** Bit 0 for channel 0 and bit 1 for channel 1.

Interrupt Status (StatusTfr) – Offset ae8

All interrupt events from all channels are stored in these Interrupt Status registers after masking: statusBlock, StatusDstTran, StatusErr, StatusSrcTran, and StatusTfr. Each Interrupt Status register has a bit allocated per channel, for example, StatusTfr(2) is the Channel 2 status transfer complete interrupt. The contents of these registers are used to generate the interrupt signals (int or int_n bus, depending on interrupt polarity) leaving the DMA.

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1:0	0h	RO	**(STATUS)** Bit 0 for channel 0 and bit 1 for channel 1.

Status for Block Interrupts (StatusBlock) – Offset af0

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**(STATUS)** Bit 0 for channel 0 and bit 1 for channel 1.

Status for Source Transaction Interrupts (StatusSrcTran) – Offset af8

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**(STATUS)** Bit 0 is for channel 0 and bit 1 is for channel 1.

Status for Destination Transaction Interrupts (StatusDstTran) – Offset b00

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1:0	0h	RO	**(STATUS)** Bit 0 is for channel 0 and bit 1 is for channel 1.

Status for Error Interrupts (StatusErr) – Offset b08

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RO	**(STATUS)** Bit 0 is for channel 0 and bit 1 is for channel 1.

Mask for Transfer Interrupts (MaskTfr) – Offset b10

The contents of the Raw Status registers are masked with the contents of the

Mask registers: MaskBlock, MaskDstTran, MaskErr, MaskSrcTran, and MaskTfr.

Each Interrupt Mask register has a bit allocated per channel, for example,

MaskTfr(2) is the mask bit for the Channel 2 transfer complete interrupt.

When the source peripheral of DMA channel i is memory, then the source transaction

complete interrupt, MaskSrcTran(i), must be masked to prevent an erroneous triggering

of an interrupt on the int_combined signal. Similarly, when the destination peripheral

of DMA channel i is memory, then the destination transaction complete interrupt,

MaskDstTran(i), must be masked to prevent an erroneous triggering of an interrupt

on the int_combined(_n) signal.

A channel INT_MASK bit will be written only if the corresponding mask write enable

bit in the INT_MASK_WE field is asserted on the same OCP write transfer. This allows

software to set a mask bit without performing a read-modified write operation.

For example, writing hex 01x1 to the MaskTfr register writes a 1 into MaskTfr(0),

while MaskTfr(7:1) remains unchanged. Writing hex 00xx leaves MaskTfr(7:0) unchanged.

Writing a 1 to any bit in these registers unmasks the corresponding interrupt, thus

allowing the DMA to set the appropriate bit in the Status registers and int_* port

signals.

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:8	0h	WO	**(INT_MASK_WE)** 0 = write disabled 1 = write enabled
7:2	-	-	**Reserved**
1:0	0h	RW	**(INT_MASK)** 0-mask 1-unmask

Mask for Block Interrupts (MaskBlock) – Offset b18

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:8	0h	WO	**(INT_MASK_WE)** 0 = write disabled 1 = write enabled

Bit Range	Default	Access	Field Name and Description
7:2	-	-	**Reserved**
1:0	0h	RW	**(INT_MASK)** 0-mask 1-unmask

Mask for Source Transaction Interrupts (MaskSrcTran) – Offset b20

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:8	0h	WO	**(INT_MASK_WE)** 0 = write disabled 1 = write enabled
7:2	-	-	**Reserved**
1:0	0h	RW	**(INT_MASK)** 0-mask 1-unmask

Mask for Destination Transaction Interrupts (MaskDstTran) – Offset b28

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
9:8	0h	WO	**(INT_MASK_WE)** 0 = write disabled 1 = write enabled
7:2	-	-	**Reserved**
1:0	0h	RW	**(INT_MASK)** 0-mask 1-unmask

Mask for Error Interrupts (MaskErr) – Offset b30

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:8	0h	WO	**(INT_MASK_WE)** 0 = write disabled 1 = write enabled
7:2	-	-	**Reserved**
1:0	0h	RW	**(INT_MASK)** 0-mask 1-unmask

Clear for Transfer Interrupts (ClearTfr) – Offset b38

Each bit in the Raw Status and Status registers is cleared on the same cycle

by writing a 1 to the corresponding location in the Clear registers: ClearBlock, ClearDstTran, ClearErr, ClearSrcTran, and ClearTfr. Each Interrupt Clear register has a bit allocated per channel, for example, ClearTfr(2) is the clear bit for the Channel 2 transfer complete interrupt. Writing a 0 has no effect. These registers are not readable.

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	WO	**(CLEAR)** 0 = no effect 1 = clear interrupt

Clear for Block Interrupts (ClearBlock) – Offset b40

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	WO	**(CLEAR)** 0 = no effect 1 = clear interrupt

Clear for Source Transaction Interrupts (ClearSrcTran) – Offset b48

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1:0	0h	WO	**(CLEAR)** 0 = no effect 1 = clear interrupt

Clear for Destination Transaction Interrupts (ClearDstTran) – Offset b50

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	WO	**(CLEAR)** 0 = no effect 1 = clear interrupt

Clear for Error Interrupts (ClearErr) – Offset b58

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	WO	**(CLEAR)** 0 = no effect 1 = clear interrupt

Combined Status register (StatusInt) – Offset b60

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is ORed to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only.

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4	0h	RO	**(ERR)** OR of the contents of StatusErr register.
3	0h	RO	**(DSTT)** OR of the contents of StatusDst register.
2	0h	RO	**(SRCT)** OR of the contents of StatusSrcTran register
1	0h	RO	**(BLOCK)** OR of the contents of StatusBlock register.
0	0h	RO	**(TFR)** OR of the contents of StatusTfr register.

DMA Configuration (DmaCfgReg) – Offset b98

This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RW	**(DMA_EN)** 0 = DMA Disabled 1 = DMA Enabled

DMA Channel Enable (ChEnReg) – Offset ba0

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority.

All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0.

The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer. For example, writing hex 01x1 writes a 1 into ChEnReg(0), while ChEnReg(7:1) remains unchanged. Writing hex 00xx leaves ChEnReg(7:0) unchanged.

Note that a read-modified write is not required.

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:8	0h	WO	**(CH_EN_WE)** Channel enable write enable.
7:2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1:0	0h	RW	**(CH_EN)** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

Control Register Low (CTL_LO0) – Offset 818

NOTE: CTL_LO0 is for DMA Channel 0. The same register definition, CTL_LO1, is available for Channel 1 at address 870h.

LLP_HI0 (CH0): offset 818h

LLP_LO1 (CH1): offset 870h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**
28	0h	RW	**(LLP_SRC_EN)** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h	RW	**(LLP_DST_EN)** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	-	-	**Reserved**
21:20	0h	RW	**(TT_FC)** The following transfer types are supported. Memory to Memory (00) Memory to Peripheral (01) Peripheral to Memory (10) Peripheral to Peripheral (11) Flow Control is always assigned to the DMA.
19	-	-	**Reserved**
18	0h	RW	**(DST_SCATTER_EN)** 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.

Bit Range	Default	Access	Field Name and Description
17	0h	RW	**(SRC_GATHER_EN)** 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h	RW	**(SRC_MSIZE)** Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source.
13:11	0h	RW	**(DEST_MSIZE)** Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h	RW	**(SINC)** Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	-	-	**Reserved**
8	0h	RW	**(DINC)** Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
6:4	0h	RW	**(SRC_TR_WIDTH)** BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
3:1	0h	RW	**(DST_TR_WIDTH)** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
0	0h	RW	**(INT_EN)** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

Control Register High (CTL_HI0) – Offset 81c

NOTE: CTL_HI0 is for DMA Channel 0. The same register definition, CTL_HI1, is available for Channel 1 at address 874h.

CTL_HI0 (CH0): offset 81Ch

CTL_HI1 (CH1): offset 874h

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:29	0h	RW	**(CH_CLASS)** A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.
28:18	0h	RW	**(CH_WEIGHT)** Channel Weight : Value of K assigns a weight of (K+1) in the round-robin arbitration between channels of the same class. A value of 0x7FF assigns an arbitration weight of 2048. Since K is from 0 to (2^11-1)=2047, Arbitration Weight ranges from 1 to 2048 **Restrictions : 1. CH_CLASS and CH_WEIGHT cannot be changed on the fly. Changes to either values for ANY channel require that ALL channels be quiescent in order to propagate those changes to the read and write arbiters without affecting their functionality. 2. Another possible way of achieving the quiescence requirement is to suspend ALL channels before changing the CH_CLASS and CH_WEIGHT. 3. Caution must be taken in descriptor-based (linked-list) multi-block transfers since the LLI.CTL_HI is one of the DW that needs to be read and loaded into the CTL_HI internal register. Hence, user needs to ensure that the CH_CLASS and CH_WEIGHT fields do not change from one descriptor to another nor do they disturb the aforementioned quiescence requirement.

Bit Range	Default	Access	Field Name and Description
17	0h	RW	**(DONE)** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h	RW	**(BLOCK_TS)** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It does not mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register. Theoretical Byte Size range is from 0 to (2^17 -1) = (128 KB - 1).

UART Memory Mapped Registers

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Receive Buffer Register (RBR)	0h
0h	4	Transmit Holding Register (THR)	0h
0h	4	Divisor Latch Low Register (DLL)	0h
4h	4	Interrupt Enable Register (IER)	0h
4h	4	Divisor Latch High (DLH)	0h
8h	4	Interrupt Identification (IIR)	1h
8h	4	FIFO Control (FCR)	1h
ch	4	Line Control Register (LCR)	0h
10h	4	MCR (MCR)	0h
14h	4	LSR (LSR)	60h
18h	4	MSR (MSR)	0h
1ch	4	SCR (SCR)	0h
30h	4	SRBR_STHR0 (SRBR_STHR0)	0h
70h	4	FAR (FAR)	0h
74h	4	TFR (TFR)	0h
78h	4	RFW (RFW)	0h
7ch	4	USR (USR)	6h
80h	4	TFL (TFL)	0h
84h	4	RFL (RFL)	0h
88h	4	SRR (SRR)	0h
8ch	4	SRTS (SRTS)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
90h	4	SBCR (SBCR)	0h
94h	4	SDMAM (SDMAM)	0h
98h	4	SFE (SFE)	0h
9ch	4	SRT (SRT)	0h
a0h	4	STET (STET)	0h
a4h	4	HTX (HTX)	0h
a8h	4	DMASA (DMASA)	0h
f4h	4	CPR (CPR)	43F32h

Receive Buffer Register (RBR) – Offset 0

RBR mode is only available when LCR register, DLAB bit = 0.

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	0h	RO	**Receive Buffer (RBR)** Data byte received on the serial input port in UART mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an over-run error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an over-run error occurs.

Transmit Holding Register (THR) – Offset 0

THR mode is only available when LCR register, DLAB bit = 0.

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	0h	WO	**Transmit Holding Register (thr)** Data to be transmitted on the serial output port in UART mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFOs are disabled (FCR[0] = 0) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFOs are enabled (FCR[0] = 1) and THRE is set, 64 characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.

Divisor Latch Low Register (DLL) – Offset 0

DLL mode is only available when LCR register, DLAB bit = 1.

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	0h	RW	**Devisor Latch Low (dll)** Lower 8 bits of a 16-bit, read/write Divisor Latch register that contains the baud rate divisor for the UART. This register may be accessed only when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur.

Interrupt Enable Register (IER) – Offset 4

IER mode is only available when LCR register [7] (DLAB bit) = 0.

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7	0h	RW	**PTIME (PTIME)** THRE Interrupt Mode Enable: This is used to enable/disable the generation of THRE Interrupt. 0 = disabled 1 = enabled
6:4	-	-	**Reserved**
3	0h	RW	**EDSSI (EDSSI)** Enable Modem Status Interrupt: This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0 = disabled 1 = enabled
2	0h	RW	**ELSI (ELSI)** Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0 = disabled 1 = enabled
1	0h	RW	**ETBEI (ETBEI)** Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0 = disabled 1 = enabled

Bit Range	Default	Access	Field Name and Description
0	0h	RW	**ERBFI (ERBFI)** Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0 = disabled 1 = enabled

Divisor Latch High (DLH) – Offset 4

DLH mode is only available when LCR register [7] (DLAB bit) = 1

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	0h	RW	**Devisor Latch High (dlh)** Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may be accessed only when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor).Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur.

Interrupt Identification (IIR) – Offset 8

Note that the register can also be used as FIFO Control Register (FCR) when it is written to.

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:6	0h	RO	**FIFOSE (FIFOSE)** FIFOs Enabled. This is used to indicate whether the FIFOs are enabled or disabled. 00 = disabled 11 = enabled
5:4	-	-	**Reserved**
3:0	1h	RO	**Interrupt ID. (IID)** This indicates the highest priority pending interrupt which can be oneof the following types: 0000 = modem status 0001 = no interrupt pending 0010 = THR empty 0100 = received data available 0110 = receiver line status 0111 = busy detect 1100 = character timeout Note: An interrupt of type 0111 (busy detect) is never indicated because the controller iscompatible with UART_16550 mode. Bit 3 indicates an interrupt can only occur when the FIFOs areenabled and used to distinguish a Character Timeout condition interrupt.

FIFO Control (FCR) – Offset 8

Note that the register can also be used as Interrupt Identification register (IIR)when it is read from.

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:6	0h	WO	**RCVR Trigger (RCVR)** This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO ¼ full 10 = FIFO ½ full 11 = FIFO 2 less than full
5:4	0h	WO	**TX Empty Trigger (TET)** This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO ¼ full 11 = FIFO ½ full
3	-	-	**Reserved**
2	0h	WO	**XMIT FIFO Reset (XFIFOR)** This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	0h	WO	**RCVR FIFO Reset (RFIFOR)** This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	1h	WO	**FIFOs Enabled (FIFOE)** This is used to indicate whether the FIFOs are enabled or disabled. 00 = disabled 11 = enabled

Line Control Register (LCR) – Offset c

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7	0h	RW	**Divisor Latch Access Bit (DLAB)** This bit is used to enable reading and writing of the Divisor Latch register(DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initialbaud rate setup in order to access other registers
6	0h	RW	**Break Control Bit (Break)** This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the serial out line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	-	-	**Reserved**
4	0h	RW	**Even Parity Select (EPS)** Even Parity Select. If UART_16550_COMPATIBLE == NO, then writeable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked. Reset Value: 0x0
3	0h	RW	**Parity Enable (PEN)** This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0 = parity disabled 1 = parity enabled

Bit Range	Default	Access	Field Name and Description
2	0h	RW	**Number of Stop Bits (STOP)** This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0 = 1 stop bit 1 = 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	0h	RW	**Data Length Select (DLS)** This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits

MCR (MCR) – Offset 10

Modem Control Register

Bit Range	Default	Access	Field Name and Description
30:6	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
5	0h	RW	**AFCE (AFCE)** Auto Flow Control Enable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set. The bit is used to help for flow control using external IO pins with the pairing device. 0 = Auto Flow Control Mode disabled 1 = Auto Flow Control Mode enabled
4	0h	RW	**LoopBack (LoopBack)** LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. Data on the serial out line is held high, while serial data output is looped back to the serial in line, internally. In this mode all the interrupts are fully functional. Also, in loop back mode, the modem control input (cts_n,) are disconnected and the modem control output (rts_n) are looped back to the inputs, internally.
3:2	-	-	**Reserved**
1	0h	RW	**RTS (RTS)** Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	-	-	**Reserved**

LSR (LSR) – Offset 14

Line Status Register

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7	0h	RW	**RFE (RFE)** Receiver FIFO Error bit. This bit is only relevant when FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 0 = no error in RX FIFO 1 = error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO
6	1h	RW	**TEMT (TEMT)** Transmitter Empty bit. If FIFOs enabled(FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	1h	RW	**THRE (THRE)** Transmit Holding Register Empty bit. If THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty.This bit is set whenever data is transferred from the THR or TX FIFO to thetransmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If both THRE Interrupt and FIFO modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting
4	0h	RW	**BI (BI)** Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. It is set whenever the serial input (sin) is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.

Bit Range	Default	Access	Field Name and Description
3	0h	RW	**FE (FE)** Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit(LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit(LSR[4]). 0 = no framing error 1 = framing error Reading the LSR clears the FE bit.
2	0h	RW	**PE (PE)** Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no parity error 1 = parity error Reading the LSR clears the PE bit.

Bit Range	Default	Access	Field Name and Description
1	0h	RW	**OE (OE)** Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and anew character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0 = no overrun error 1 = overrun error Reading the LSR clears the OE bit.
0	0h	RW	**DR (DR)** Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0 = no data ready 1 = data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

MSR (MSR) – Offset 18

Modem Status Register

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
4	0h	RO	**CTS (CTS)** Clear to Send. This is used to indicate the current state of the modem control line cts_n.This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it isan indication that the modem or data set is ready to exchange data with the UART. 0 = cts_n input is de-asserted (logic 1) 1 = cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3:1	-	-	**Reserved**
0	0h	RO	**DCTS (DCTS)** Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0 = no change on cts_n since last read of MSR 1 = change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS).Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs(software or otherwise), then the DCTS bit is set when the reset is removed if the cts_nsignal remains asserted.

SCR (SCR) – Offset 1c

Scratchpad Register

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	0h	RW	**scr (scr)** This register is for programmers to use as a temporary storage space.

SRBR_STHR0 (SRBR_STHR0) – Offset 30

NOTE: There are a total of 16 Shadow Receive Buffer Registers (SRBR_STHR[15:0]. The register description is the same for all of them. The other registers are at the following offsets:

SRBR_STHR1 at offset 34h

SRBR_STHR2 at offset 38h

SRBR_STHR3 at offset 3Ch

.....

SRBR_STHR14 at offset 68h

SRBR_STHR15 at offset 6Ch

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	0h	RW	**srbr_sthr0 (srbr_sthr0)** Used as SRBR: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Used as STHR: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as toaccommodate burst accesses from the master. This register contains data to be transmitted on theserial output port (sout) in UART mode. Data should only be written to the THR when the THR Empty(THRE) bit (LSR[5]) is set. If FIFOs are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THRclears the THRE. Any additional writes to the THR before the THRE is set again causes the THR datato be overwritten. If FIFOs are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may bewritten to the THR before the FIFO is full. The number x (default=16) is determined by the value ofFIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full resultsin the write data being lost.

FAR (FAR) – Offset 70

FIFO Access Register

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RW	**srbr_sthr (srbr_sthr)** Writes have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. 0 = FIFO access mode disabled 1 = FIFO access mode enabled Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty. Reset Value: 0x0

TFR (TFR) – Offset 74

Transmit FIFO Read

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	0h	RW	**tfr (tfr)** Transmit FIFO Read. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the THR. Reset Value: 0x0

RFW (RFW) – Offset 78

Receive FIFO Write

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9	0h	WO	**RFFE (RFFE)** Receive FIFO Framing Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR.

Bit Range	Default	Access	Field Name and Description
8	0h	WO	**RFPE (RFPE)** Receive FIFO Parity Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR.
7:0	0h	WO	**RFWD (RFWD)** Receive FIFO Write Data. These bits are only valid when FIFO access mode is enabled(FAR[0] is set to one). When FIFOs are enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR.

USR (USR) – Offset 7c

UART Status Register

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4	0h	RO	**RFF (RFF)** Receive FIFO Full. This is used to indicate that the receive FIFO is completely full. 0 = Receive FIFO not full 1 = Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	0h	RO	**RFNE (RFNE)** Receive FIFO Not Empty. This is used to indicate that the receive FIFO contains one or more entries. 0 = Receive FIFO is empty 1 = Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.

Bit Range	Default	Access	Field Name and Description
2	1h	RO	**TFE (TFE)** Transmit FIFO Empty. This is used to indicate that the transmit FIFO is completely empty. 0 = Transmit FIFO is not empty 1 = Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty
1	1h	RO	**TFNF (TFNF)** Transmit FIFO Not Full. This is used to indicate that the transmit FIFO in not full. 0 = Transmit FIFO is full 1 = Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	-	-	**Reserved**

TFL (TFL) – Offset 80

Transmit FIFO Level

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4:0	0h	RO	**tfl (tfl)** Transmit FIFO Level. This is indicates the number of data entries in the transmit FIFO. Reset Value: 0x0

RFL (RFL) – Offset 84

Receive FIFO Level

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4:0	0h	RO	**rfl (rfl)** Receive FIFO Level. This is indicates the number of data entries in the receive FIFO. Reset Value: 0x0

SRR (SRR) – Offset 88

Software Reset Register

Bit Range	Default	Access	Field Name and Description
30:3	-	-	**Reserved**
2	0h	RW	**XFR (XFR)** XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	0h	RW	**RFR (RFR)** RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	0h	RW	**UR (UR)** UART Reset. This asynchronously resets the UART controller and synchronously removes the reset assertion.

SRTS (SRTS) – Offset 8c

Shadow Request to Send

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RW	**srts (srts)** Shadow Request to Send. This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the DW_apb_uart is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input. Reset Value: 0x0

SBCR (SBCR) – Offset 90

Shadow Break Control Bit

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
0	0h	RW	**sbcb (sbcb)** Shadow Break Control Register. This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. When in Loopback Mode, the break condition is internally looped back to the receiver.

SDMAM (SDMAM) – Offset 94

Shadow DMA Mode

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RW	**sdmam (sdmam)** Shadow DMA Mode. This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. 0 = mode 0 1 = mode 1

SFE (SFE) – Offset 98

Shadow FIFO Enable

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RW	**sfe (sfe)** Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated.This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset. Reset Value: 0x0

SRT (SRT) – Offset 9c

Shadow RCVR Trigger

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RW	**srt (srt)** Shadow RCVR Trigger. This is a shadow register for the RCVR trigger bits(FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO ¼ full 10 = FIFO ½ full 11 = FIFO 2 less than full

STET (STET) – Offset a0

Shadow TX Empty Trigger. This is a shadow register for the TX empty trigger bits(FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TXempty trigger bit gets updated. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active.

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1:0	0h	RW	**stet (stet)** Shadow TX Empty Trigger: This is a shadow register for the TX empty trigger bits(FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated.165This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO ¼ full 11 = FIFO ½ full

HTX (HTX) – Offset a4

Halt TX

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RW	**htx (htx)** This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 = Halt TX disabled 1 = Halt TX enabled Note, if FIFOs are not enabled, the setting of the halt TX register has no effect on operation.

DMASA (DMASA) – Offset a8

DMA Software Acknowledge

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	WO	**dmasa (dmasa)** This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the UART should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.

CPR (CPR) – Offset f4

Component Parameter Register

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:16	4h	RO	**FIFO_MODE (FIFO_MODE)** 0x00 = 0 0x01 = 16 0x02 = 32 to 0x80 = 2048 0x81- 0xff = reserved
15:14	-	-	**Reserved**
13	1h	RO	**DMA_EXTRA (DMA_EXTRA)** 0 = FALSE, 1 = TRUE

Bit Range	Default	Access	Field Name and Description
12	1h	RO	**UART_ADD_ENCODED_PARAMS (UART_ADD_ENCODED_PARAMS)** 0 = FALSE, 1 = TRUE
11	1h	RO	**SHADOW (SHADOW)** 0 = FALSE, 1 = TRUE
10	1h	RO	**FIFO_STAT (FIFO_STAT)** 0 = FALSE, 1 = TRUE
9	1h	RO	**FIFO_ACCESS (FIFO_ACCESS)** 0 = FALSE, 1 = TRUE
8	1h	RO	**ADDITIONAL_FEAT (ADDITIONAL_FEAT)** 0 = FALSE, 1 = TRUE
7	0h	RO	**SIR_LP_MODE (SIR_LP_MODE)** 0 = FALSE, 1 = TRUE
6	0h	RO	**SIR_MODE (SIR_MODE)** 0 = FALSE, 1 = TRUE
5	1h	RO	**THRE_MODE (THRE_MODE)** 0 = FALSE, 1 = TRUE
4	1h	RO	**AFCE_MODE (AFCE_MODE)** 0 = FALSE, 1 = TRUE
3:2	-	-	**Reserved**
1:0	2h	RO	**APB_DATA_WIDTH (APB_DATA_WIDTH)** 00 = 8 bits 01 = 16 bits 10 = 32 bits 11 = reserved

UART PCI Configuration Registers

SAR1 PCI Configuration Registers

Summary of Bus:, Device:, Function: (MSG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID and Vendor ID (DEVVENDID)	XXXX8086h
4h	4	Status and Command (STATUSCOMMAND)	100000h
8h	4	Revision ID and Class Code (REVCLASSCODE)	78000XXh
ch	4	Cache Line Latency Header and BIST (CLLATHEADERBIST)	800000h
10h	4	Base Address (BAR)	4h
14h	4	Base Address High (BAR_HIGH)	0h
18h	4	Base Address 1 (BAR1)	4h
1ch	4	Base Address 1 High (BAR1_HIGH)	0h
2ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)	0h
34h	4	Capabilities Pointer (CAPABILITYPTR)	80h
3ch	4	Interrupt Register (INTERRUPTREG)	100h
80h	4	Power Management Capability ID (POWERCAPID)	39001h
84h	4	Power Management Control and Status (PMECTRLSTATUS)	8h
90h	4	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)	F0140009h
98h	4	SW LTR update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)	2101h
9ch	4	Device IDLE Pointer (DEVICE_IDLE_POINTER_REG)	24C1h
a0h	4	Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)	70800h
b0h	4	General Purpose Read Write 1 (GEN_REGRW1)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
b4h	4	General Purpose Read Write 2 (GEN_REGRW2)	0h
b8h	4	General Purpose Read Write 3 (GEN_REGRW3)	0h
bch	4	General Purpose Read Write 4 (GEN_REGRW4)	0h
c0h	4	General Purpose Input (GEN_INPUT_REG)	0h

Device ID and Vendor ID (DEVVENDID) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:16	See Description	RO	**Device Identification (DEVICEID)** This is a 16-bit value assigned to the controller. See the Device and Revision ID Table in Volume 1 for the default value.
15:0	8086h	RO	**Vendor ID (VENDORID)** Identifies the manufacturer of the device. 8086h = Intel.

Status and Command (STATUSCOMMAND) – Offset 4

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29	0h	RW/1C	**Received Master Abort (RMA)** S/W writes a '1' to this bit to clear it.

Bit Range	Default	Access	Field Name and Description
28	0h	RW/1C	**Received Target Abort (RTA)** S/W writes a '1' to this bit to clear it.
27:21	-	-	**Reserved**
20	1h	RO	**Capabilities List (CAPLIST)** Indicates that the controller contains a capabilities pointer list.
19	0h	RO	**Interrupt Status (INTR_STATUS)** This bit reflects state of interrupt in the device.
18:11	-	-	**Reserved**
10	0h	RW	**Interrupt Disable (INTR_DISABLE)** Setting this bit disables INTx assertion. The interrupt disabled is legacy INTx# interrupt.
9	-	-	**Reserved**
8	0h	RW	**SERR Enable (SERR_ENABLE)** Not implemented.
7:3	-	-	**Reserved**
2	0h	RW	**Bus Master Enable (BME)** If this bit is 0, the controller does not generate any new upstream transaction as a master.
1	0h	RW	**Memory Space Enable (MSE)** 0 = Disables memory mapped Configuration space. 1 = Enables memory mapped configuration space.
0	-	-	**Reserved**

Revision ID and Class Code (REVCLASSCODE) – Offset 8

Bit Range	Default	Access	Field Name and Description
31:8	See Description	RO	**Class Codes (CLASS_CODES)** Class Code register is read-only and is used to identify the generic function of the device, and in some cases, a specific register-level programming interface
7:0	See Description	RO	**Revision ID (RID)** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

Cache Line Latency Header and BIST (CLLATHEADERBIST) – Offset c

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	1b	RO	**Multi Function Device (MULFNDEV)** 0 = Single Function Device 1 = Multi Function device
22:16	00h	RO	**Header Type (HEADERTYPE)** Implements Type 0 Configuration header.
15:8	00h	RO	**Latency Timer (LATTIMER)** Hardwired to 0.
7:0	00h	RW	**Cache Line Size (CACHELINE_SIZE)**

Base Address (BAR) – Offset 10

Bit Range	Default	Access	Field Name and Description
31:12	00000h	RW	**Base Address (BASEADDR)** Provides system memory base address for the controller.

Bit Range	Default	Access	Field Name and Description
11:4	00h	RO	**Size Indicator (SIZEINDICATOR)** Always returns 0. The size of this register depends on the size of the memory space.
3	0h	RO	**Prefetchable (PREFETCHABLE)** 0 indicates that this BAR is not prefetchable.
2:1	10b	RO	**Type (TYPE)** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range, If BAR_64b_ EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h	RO	**Memory Space Indicator (MESSAGE_SPACE)** 0 indicates this BAR is present in the memory space.

Base Address High (BAR_HIGH) – Offset 14

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Base Address High (BASEADDR_HIGH)** Base address high - MSB

Base Address 1 (BAR1) – Offset 18

Bit Range	Default	Access	Field Name and Description
31:12	00000h	RW	**Base Address (BASEADDR1)** This field is present if BAR1 is enabled.
11:4	00h	RO	**Size Indicator (SIZEINDICATOR1)** Always is 0 as minimum size is 4K
3	0h	RO	**Prefetchable (PREFETCHABLE1)** 0 indicates that this BAR is not prefetchable.
2:1	2h	RO	**Type (TYPE1)** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_ EN is 1 then 10 Indicates BAR lies in 64 bit address range

Bit Range	Default	Access	Field Name and Description
0	0h	RO	**Memory Space Indicator (MESSAGE_SPACE1)** 0 indicates this BAR is present in the memory space.

Base Address 1 High (BAR1_HIGH) – Offset 1c

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Base Address High (BASEADDR1_HIGH)**

Subsystem Vendor and Subsystem ID (SUBSYSTEMID) – Offset 2c

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/O	**Subsystem ID (SUBSYSTEMID)** The register, in combinationwith the Subsystem Vendor ID register make it possible for theoperating environment to distinguish one subsystem from theother. This register is a Read Write Once type register.
15:0	0000h	RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID)** The register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from theother. This register is a Read Write Once register.

Capabilities Pointer (CAPABILITYPTR) – Offset 34

Capabilities Pointer register indicates what the next capability is

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
7:0	80h	RO	**Capabilities Pointer (CAPPTR_POWER)** Indicates what the next capability is.

Interrupt Register (INTERRUPTREG) – Offset 3c

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO	**Max Latency (MAX_LAT)** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h	RO	**Min Latency (MIN_GNT)** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	-	-	**Reserved**
11:8	1h	RO	**Interrupt Pin (INTPIN)**
7:0	00h	RW	**Interrupt Line (INTLINE)** It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

Power Management Capability ID (POWERCAPID) – Offset 80

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:27	00h	RO	**PME Support (PMESUPPORT)** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for for a bit indicates that the function is not capable of asserting the PME# signal while in that power state. Bit 27 = 1: PME# can be asserted from D0. Bit 30 = 1: PME# can be asserted from D3 hot. Other bits are not used.
26:19	-	-	**Reserved**
18:16	3h	RO	**Version (VERSION)** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h	RO	**Next Capability (NXTCAP)** Points to the next capability structure.
7:0	01h	RO	**Power Management Capability (POWER_CAP)** Indicates power management capability is supported.

Power Management Control and Status (PMECTRLSTATUS) – Offset 84

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
15	0h	RW/1C	**PME Status (PMESTATUS)**
14:9	-	-	**Reserved**
8	0h	RW	**PME Enable (PMEENABLE)** 0 = PME message is disabled 1 = PME message is enabled.
7:4	-	-	**Reserved**
3	1h	RO	**No Soft Reset (NO_SOFT_RESET)** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	-	-	**Reserved**
1:0	0h	RW	**Power State (POWERSTATE)** This field is used both todetermine the current power state and to set a new power state.The values are:00 = D0 state11 = D3HOT stateOthers = ReservedNotes: If software attempts to write a value of 01b or 10b in to this field,the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked.

PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD) – Offset 90

Bit Range	Default	Access	Field Name and Description
31:28	0Fh	RO	**Vendor Capability (VEND_CAP)** Vendor Specific Capability ID
27:24	0h	RO	**Revision ID (REVID)** Revision ID of capability structure
23:16	14h	RO	**Capability Length (CAP_LENGTH)** Vendor Specific Capability Length

Bit Range	Default	Access	Field Name and Description
15:8	00h	RO	**Next Capability (NEXT_CAP)** Points to the next capabilitystructure. This points to NULL.
7:0	09h	RO	**Capability ID (CAPID)**

SW LTR update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) – Offset 98

Software location pointer in MMIO space as an offset specified by BAR

Bit Range	Default	Access	Field Name and Description
31:4	0000210h	RO	**Location Pointer Offset (SW_LAT_DWORD_OFFSET)** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h	RO	**Bar Number (SW_LAT_BAR_NUM)** Indicates that the SW LTR update MMIO location is always at BAR0
0	1h	RO	**Valid (SW_LAT_VALID)**

Device IDLE Pointer (DEVICE_IDLE_POINTER_REG) – Offset 9c

Device IDLE pointer register giving details on Device MMIO offset location , BAR NUM and D0i3 Valid Strap

Bit Range	Default	Access	Field Name and Description
31:4	000024Ch	RO	**Device Idle Pointer (DWORD_OFFSET)** contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR
3:1	0h	RO	**Bar Number (BAR_NUM)** Indicates that the D0i3 MMIO location is always at BAR0.
0	1h	RO	**Valid (VALID)**

Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG) – Offset a0

Bit Range	Default	Access	Field Name and Description
30:19	-	-	**Reserved**
18	1b	RW	**Power Gate Enable (PGE)** If clear, the controller will never request a PG. If 1, then the function will power gate when idle and the DevIdle bit is set.
17	1b	RW	**D3-Hot Enable (I3_ENABLE)** If 1, then function will power gate when idle and the PMCSR[1:0] register in the function = 11 (D3).
16	1b	RW	**PMC Request Enable (PMCRE)** If this bit is set to '1', thefunction will power gate when idle.
15:13	-	-	**Reserved**
12:10	2h	RW/O	**Power On Latency Scale (POW_LAT_SCALE)** This value is written by BIOS to communicate to the Driver.
9:0	000h	RW/O	**Power On Latency Value (POW_LAT_VALUE)** This value is written by BIOS to communicate to the Driver.

General Purpose Read Write 1 (GEN_REGRW1) – Offset b0

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**General Purpose Read Write (GEN_REG_RW1)** General purpose read write PCI register.

General Purpose Read Write 2 (GEN_REGRW2) – Offset b4

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**General Purpose Read Write (GEN_REG_RW2)** General purpose read write PCI register.

General Purpose Read Write 3 (GEN_REGRW3) – Offset b8

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**General Purpose Read Write (GEN_REG_RW3)** General purpose read write PCI register.

General Purpose Read Write 4 (GEN_REGRW4) – Offset bc

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**General Purpose Read Write (GEN_REG_RW4)** General purpose read write PCI register.

General Purpose Input (GEN_INPUT_REG) – Offset c0

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RO	**General Purpose Input (GEN_REG_INPUT_RW)** General Purpose Input Register.

xDCI MMIO Device Registers

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
c700h	4	Device Configuration Register (DCFG)	80004h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
c704h	4	Device Control Register (DCTL)	F00000h
c708h	4	Device Event Enable Register (DEVTEN)	0h
c70ch	4	Device Status Register (DSTS)	520004h
c710h	4	Device Generic Command Parameter (DGCMDPAR)	0h
c714h	4	Device Generic Command (DGCMD)	0h
c720h	4	Device Active USB Endpoint Enable (DALEPENA)	0h
c800h	4	Device Physical Endpoint-n Command Parameter 2 (DEPCMDPAR2)	0h
c804h	4	Device Physical Endpoint-n Command Parameter 1 (DEPCMDPAR1)	0h
c808h	4	Device Physical Endpoint-n Command Parameter 0 (DEPCMDPAR0)	0h
c80ch	4	Device Physical Endpoint-n Command (DEPCMD)	0h

Device Configuration Register (DCFG) – Offset c700

Bit Range	Default	Access	Field Name and Description
30:23	-	-	**Reserved**
22	00h	RW	**LPM Capable (LPMCAP)** The application uses this bit to control the LPM capabilities: 1'b0: LPM capability is not enabled. 1'b1: LPM capability is enabled.

Bit Range	Default	Access	Field Name and Description
21:17	04h	RW	**Number of Receive Buffers (NUMP)** This bit indicates the number of receive buffers to be reported in the ACK TP.
16:12	00h	RW	**Interrupt Number (INTRNUM)** Indicates interrupt number on which non-endpoint-specific device-related interrupts are generated.
11:10	-	-	**Reserved**
9:3	00h	RW	**Device Address (DEVADDR)**
2:0	4h	RW	**Device Speed (DEVSPD)** Indicates the speed at which the application requires the core to connect, or the maximum speed the application can support: 3'b100: SuperSpeed 3'b000: High-speed 3'b001: Full-speed

Device Control Register (DCTL) – Offset c704

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31	00h	RW	**Run/Stop (RUN_STOP)** The software writes 1 to this bit to start the device controller operation.To stop the device controller operation, the software must remove any active transfers and write 0 to this bit. When the controller is stopped, it sets the DSTS.DevCtrlHlt bit when the core is idle and the lower layer finishes the disconnect process. The Run/Stop bit must be used in following cases as specified: 1.After power-on reset and CSR initialization, the software must write 1 to this bit to start the device controller. The controller does not signal connect to the host until this bit is set. 2.The software uses this bit to control the device controller to perform a soft disconnect. When the software writes 0 to this bit, the host does not see that the device is connected. The device controller stays in the disconnected state until the software writes 1 to this bit. The minimum duration of keeping this bit cleared: SS: 30ms HS/FS/LS: 10ms If the software attempts a connect after the soft disconnect or detects adisconnect event, it must set DCTL[8:5] to 5 before reasserting the Run/Stopbit. 3.When the USB or Link is in a lower power state and the Two Power Rails configuration is selected, software writes 0 to this bit to indicate that it is going to turn off the Core Power Rail. After the software turns on the Core Power Rail again and re-initializes the device controller, it must set this bit to start the device controller.
30	00h	RW	**Core Soft Reset (CSFTRST)** Resets the all clock domains

Bit Range	Default	Access	Field Name and Description
29	-	-	**Reserved**
28:24	00h	RW	**HIRD Threshold (HIRDTHRES)** The core asserts output signals utmi_l1_suspend_n and utmi_sleep_n on the basis of this signal: The core asserts utmi_l1_suspend_n to put the PHY into Deep Low-Power mode in L1 when both of the following are true: -HIRD value is greater than or equal to the value in DCTL.HIRD_Thres[3:0] -HIRD_Thres[4] is set to 1'b1. The core asserts utmi_sleep_n on L1 when one of the following is true: -If the HIRD value is less than HIRD_Thres[3:0] or -HIRD_Thres[4] is set to 1'b0. Note: This field must be set to '0' during SuperSpeed mode of operation.
23:20	fh	RW	**LPM NYET Response Threshold (LPM_NYET_thres)** Handshake response to LPM token specified by device application
19	0h	RW	**Keep Connect (KeepConnect)** When '1', this bit enables the save and restore programming model by preventing the core from disconnecting from the host when DCTL.RunStop is set to '0'. It also enables the Hibernation Request Event to be generated when the link goes to U3 or L2. The device core disconnects from the host when DCTL.RunStop is set to '0'. This bit indicates whether to preserve this behavior ('0'), or if the core should not disconnect when RunStop is set to 0 ('1').This bit also prevents the LTSSM from automatically going to U0/L0 when the host requests resume from U3/L2.
18	0h	RW	**L1 Hibernation Enable (L1HibernationEn)** When this bit is set along with KeepConnect, the device core generates a Hibernation Request Event if L1 is enabled and the HIRD value in the LPM token is larger than the threshold programmed in DCTL.HIRD_Thres. The core will not exit the LPM L1 state until software writes Recovery into the DCTL.ULStChngReq field. This prevents corner cases where the device is entering hibernation at the same time the host is attempting to exit L1.

Bit Range	Default	Access	Field Name and Description
17	0h	RW	**Controller Restore State (CRS)** This command initiates the restore process. When software sets this bit to '1', the controller immediately sets DSTS.RSS to '1'. When the controller has finished the restore process, it sets DSTS.RSS to '0'. Note: When read, this field always returns '0'.
16	0h	RW	**Controller Save State (CSS)** This command initiates the save process.When software sets this bit to '1', the controller immediately sets DSTS.SSS to '1'. When the controller has finished the save process, it sets DSTS.SSS to '0'. Note: When read, this field always returns '0'.
15:13	-	-	**Reserved**
12	0h	RW	**Initiate U2 Enable (INITU2ENA)** 1'b0: May not initiate U2 (default) 1'b1: May initiate U2 On USB reset, hardware clears this bit to ”0”. Software sets this bit after receiving SetFeature(U2_ENABLE), and clears this bit when ClearFeature(U2_ENABLE) is received.If DCTL[11] (AcceptU2Ena) is 0, the link immediately exits U2 state.
11	0h	RW	**Accept U2 Enable (ACCEPTU2ENA)** 1'b0: Reject U2 except when Force_LinkPM_Accept bit is set (default) 1'b1: Core accepts transition to U2 state if nothing is pending on the application side.On USB reset, hardware clears this bit to ”0”. Software sets this bit after receiving a SetConfiguration command
10	0h	RW	**Initiate U1 Enable (INITU1ENA)** 1'b0: May not initiate U1 1'b1: May initiate U1 On USB reset, hardware clears this bit to “0”. Software sets this bit after receiving SetFeature(U1_ENABLE), and clears this bit when ClearFeature(U1_ENABLE) is received. If DCTL[9] (AcceptU1Ena) is 0, the link immediately exits U1 state.

Bit Range	Default	Access	Field Name and Description
9	0h	RW	**Accept U1 Enable (ACCEPTU1ENA)** 1'b0: Core rejects U1 except when Force_LinkPM_Accept bit is set (default) 1'b1: Core accepts transition to U1 state if nothing is pending on the application side. On USB reset, hardware clears this bit to “0”. Software sets this bit after receiving a SetConfiguration command.
8:5	0h	WO	

Bit Range	Default	Access	Field Name and Description
			USB / Link State Change Request (ULSTCHNGREQ) Software writes this field to issue a USB/Link state change request. A change in this field indicates a new request to the core. If software wants to issue the same request back-to-back, it must write a 0 to this field between the two requests. The result of the state change request is reflected in the USB/Link State in DSTS. These bits are self-cleared on the MAC Layer exiting suspended state. If software is updating other fields of the DCTL register and not intending to force any link state change, then it must write a 0 to this field. SS Compliance mode is normally entered and controlled by the remote link partner. Alternatively, the local link can be forced directly into Compliance mode by resetting the SS link with the RUN/STOP bit set to zero. If then '10' is written to the USB/Link State Change field and '1' to RUN/STOP, the Link will go to Compliance. Once in Compliance, 'zero' and '10' may alternately be written to this field to advance the compliance pattern. In SS mode: ValueRequested Link State Transition: 0:No Action 4:SS.Disabled 5:Rx.Detect 6:SS.Inactive 8:Recovery 10:Compliance Others:Reserved In HS/FS/LS mode: ValueRequested USB state transition 8:Remote wakeup request Others:Reserved The Remote wakeup request should be issued 2µs after the device goes into suspend state. Note: After coming out of hibernation, software should write 8 (Recovery) into this field to confirm exit from the suspended state

Bit Range	Default	Access	Field Name and Description
4:0	-	-	**Reserved**

Device Event Enable Register (DEVTEN) – Offset c708

Bit Range	Default	Access	Field Name and Description
30:13	-	-	**Reserved**
12	00h	RW	**Vendor Device Test LMP Received Event (VENDEVTSTRCVDEN)**
11:10	-	-	**Reserved**
9	00h	RW	**Erratic Error Event Enable (ERRTICERREVTEN)**
8:7	-	-	**Reserved**
6	00h	RW	**U3/L2-L1 Suspend Event Enable (U3L2L1SuspEn)**
5	-	-	**Reserved**
4	00h	RW	**Resume/Remote Wakeup Detected Event Enable (WKUPEVTEN)**
3	00h	RW	**USB/Link State Change Event Enable (ULSTCNGEN)**

Bit Range	Default	Access	Field Name and Description
2	00h	RW	**Connection Done Enable (CONNECTDONEEVTEN)**
1	00h	RW	**USB Reset Enable (USBRSTEVTEN)**
0	00h	RW	**Disconnect Detected Event Enable (DISSCONNEVTEN)**

Device Status Register (DSTS) – Offset c70c

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29	0h	RO	**Device Controller Not Ready (DCNRD)** The bit indicates that the core is in the process of completing the state transitions after exiting from hibernation. To complete the state transitions, it takes 256 bus clock cycles from the time DCTL[31].Run/Stop is set. During hibernation, if the UTMI/ULPI PHY is in suspended state, then the 256-bus clock cycle delay starts after the PHY exited suspended state. Software must set DCTL[31].Run/Stop to '1' and wait for this bit to be de-asserted to zero before processing DSTS.USBLnkSt. This bit is valid only when DWC_USB3_EN_PWROPT is set to two and GCTL[1].GblHibernationEn =1.
28:26	-	-	**Reserved**
25	0h	RO	**Restore State Status (RSS)** When the controller has finished the restore process, it will complete the command by setting DSTS.RSS to '0'.
24	0h	RO	**Save State Status (SSS)** When the controller has finished the save process, it will complete the command by setting DSTS.SSS to '0'.
23	0h	RO	**Core Idle (COREIDLE)** The bit indicates that the core finished transferring all RxFIFO data to system memory, writing out all completed descriptors, and all Event Counts are zero.

Bit Range	Default	Access	Field Name and Description
22	1h	RO	**Device Controller Halted (DEVCTRLHLT)** This bit is set to 0 when the Run/Stop bit in the DCTL register is set to 1. The core sets this bit to 1 when, after SW sets Run/Stop to '0', the core is idle and the lower layer finishes the disconnect process. When Halted =1, the core does not generate Device events.

Bit Range	Default	Access	Field Name and Description
21:18	4h	RO	**USB/Link State (USBLNKST)** In SS mode: 4'h0: U0 4'h1: U1 4'h2: U2 4'h3: U3 4'h4: SS_DIS 4'h5: RX_DET 4'h6: SS_INACT 4'h7: POLL 4'h8: RECOV 4'h9: HRESET 4'ha: CMPLY 4'hb: LPBK 4'hf: Resume/Reset In HS/FS/LS mode: 4’h0: On state 4’h2: Sleep (L1) state 4’h3: Suspend (L2) state 4’h4: Disconnected state 4’h5: Early Suspend state 4'he: Reset 4'hf: Resume
17	0001h	RO	**RxFIFO Empty (RXFIFOEMPTY)**

Bit Range	Default	Access	Field Name and Description
16:3	0000h	RO	**Frame/Microframe Number of the Received SOF (SOFFN)** When the core is operating at high-speed: [16:6] indicates the frame number [5:3] indicates the microframe number When the core is operating at full-speed: [16:14] is not used. Software can ignore these 3 bits [13:3] indicates the frame number
2:0	4h	RO	**Connected Speed (CONNECTSPD)** Indicates the speed at which the core has come up after speed detection through a chirp sequence: 3'b100: SuperSpeed 3'b000: High-speed 3'b001: Full-speed 3'b010: Low-speed 3'b011: Full-speed

Device Generic Command Parameter (DGCMDPAR) – Offset c710

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Command Parameter (PARAMETER)** This register indicates the device command parameter. This must be programmed before or along with the device command (DGCMD).

Device Generic Command (DGCMD) – Offset c714

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:12	0h	RO	**Command Status (CMDSTATUS)** 1: CmdErr – Indicates that the device controller encountered an error while processing the command. 0: Indicates command success
11	-	-	**Reserved**
10	00h	NA	**Command Active (CMDACT)** The software sets this bit to 1 to enable the device controller to execute the generic command. The device controller sets this bit to 0 after executing the command.
9	-	-	**Reserved**
8	00h	RW	**Command Interrupt on Complete (CMDIOC)** When this bit is set, the device controller issues a Generic Command Completion event after executing the command. Note that this interrupt is mapped to DCFG.IntrNum. Note: This field must not set to '1' if the DCTL.RunStop field is '0'.
7:0	00h	RW	**Command Type (CMDTYP)** Specifies the type of command the software driver is requesting the core to perform: 02h: Set Periodic Parameters 04h: Set Scratchpad Buffer Array Address Lo 05h: Set Scratchpad Buffer Array Address Hi 07h:Transmit Device Notification 09h: Selected FIFO Flush 0Ah: All FIFO Flush 0Ch: Set Endpoint NRDY 10h: Run SoC Bus LoopBack Test

Device Active USB Endpoint Enable (DALEPENA) – Offset c720

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**USB Active Endpoints (USBACTEP)** This field indicates if a USB endpoint is active in the current configuration and interface. Bit[0]: USB EP0-OUT Bit[1]: USB EP0-IN Bit[2]: USB EP1-OUT Bit[3]: USB EP1-IN

Device Physical Endpoint-n Command Parameter 2 (DEPCMDPAR2) – Offset c800

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**PARAMETER (PARAMETER)** This register indicates the physical endpoint command Parameter 2. It must be programmed before issuing the command.

Device Physical Endpoint-n Command Parameter 1 (DEPCMDPAR1) – Offset c804

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**PARAMETER (PARAMETER)** This register indicates the physical endpoint command Parameter 1. It must be programmed before issuing the command

Device Physical Endpoint-n Command Parameter 0 (DEPCMDPAR0)

– Offset c808

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**PARAMETER (PARAMETER)** This register indicates the physical endpoint command parameter 0. This must be programmed before or along with the command. For commands needing only one 32-bit parameter, this register must be programmed with the command register.

Device Physical Endpoint-n Command (DEPCMD) – Offset c80c

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW	**Command Parameters (COMMANDPARAM)** When this register is written: For Start Transfer command: -[31:16]: StreamID. The USB StreamID assigned to this transfer For Start Transfer command applied to an isochronous endpoint: -[31:16]: StartMicroFramNum: Indicates the (micro)frame number to which the first TRB applies For Update Transfer, End Transfer, and Start New Configuration commands: -[22:16]: Transfer Resource Index (XferRscIdx). The hardware-assigned transfer resource index for the transfer, which was returned in response to the Start Transfer command. The application software-assigned transfer resource index for a Start New Configuration command
15:12	0h	RW	**Command Completion Status (CMDSTATUS)** Additional information about the completion of this command is available in this field.
11	0h	RW	**HighPriority/ForceRM (HIPRI_FORCERM)** HighPriority: Only valid for Start Transfer command ForceRM: Only valid for End Transfer command ClearPendIN: Only valid for Clear Stall command – Software sets this bit to clear any pending IN transaction (on that endpoint) stuck at the lower layers when a Clear Stall command is issued.

Bit Range	Default	Access	Field Name and Description
10	0h	RW	**Command Active (CMDACT)** Software sets this bit to 1 to enable the device endpoint controller to execute the generic command.The device controller sets this bit to 0 when the CmdStatus field is valid and the endpoint is ready to accept another command. This does not imply that all the effects of the previously-issued command have taken place.
9	-	-	**Reserved**
8	0h	RW	**Command Interrupt on Complete (CMDIOC)** When this bit is set, the device controller issues a generic Endpoint Command Complete event after executing the command. Note that this interrupt is mapped to DEPCFG.IntrNum. When the DEPCFG command is executed, the command interrupt on completion goes to the interrupt pointed by the DEPCFG.IntrNum in the current command. Note: This field must not set to '1' if the DCTL.RunStop field is '0'.
7:4	-	-	**Reserved**
3:0	0h	RW	**Command Type (CMDTYP)** Specifies the type of command the software driver is requesting the core to perform. 00h: Reserved 01h: Set Endpoint Configuration-64 or 96-bit Parameter 02h: Set Endpoint Transfer Resource Configuration-32-bit Parameter 03h: Get Endpoint State-No Parameter Needed 04h: Set Stall-No Parameter Needed 05h: Clear Stall (see Set Stall)-No Parameter Needed 06h: Start Transfer-64-bit Parameter 07h: Update Transfer-No Parameter Needed 08h: End Transfer-No Parameter Needed 09h: Start New Configuration-No Parameter Needed

xDCI MMIO Global Registers

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
c100h	4	Global SoC Bus Configuration 0 (GSBUSCFG0)	6h
c104h	4	Global SoC Bus Configuration 1 (GSBUSCFG1)	F00h
c108h	4	Global Tx Threshold Control (GTXTHRCFG)	0h
c10ch	4	Global Rx Threshold Control (GRXTHRCFG)	24400000h
c110h	4	Global Core Control (GCTL)	2000h
c114h	4	GPMSTS (GPMSTS)	0h
c118h	4	Global Status (GSTS)	0h
c130h	4	Bus Address Low (GBUSERRADDRLO)	0h
c134h	4	Bus Address High (GBUSERRADDRHI)	0h
c140h	4	GHWPARAMS0 (GHWPARAMS0)	40204008h
c144h	4	GHWPARAMS1 (GHWPARAMS1)	260C93Bh
c148h	4	GHWPARAMS2 (GHWPARAMS2)	8086A0h
c14ch	4	GHWPARAMS3 (GHWPARAMS3)	10420085h
c150h	4	GHWPARAMS4 (GHWPARAMS4)	222004h
c154h	4	GHWPARAMS5 (GHWPARAMS5)	4202088h
c158h	4	GHWPARAMS6 (GHWPARAMS6)	2F60020h
c15ch	4	GHWPARAMS7 (GHWPARAMS7)	38507E6h
c160h	4	GDBGFIFOSPACE (GDBGFIFOSPACE)	420000h
c164h	4	GDBGLTSSM (GDBGLTSSM)	41010440h
c168h	4	GDBGLNMCC (GDBGLNMCC)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
c16ch	4	GDBGBMU (GDBGBMU)	0h
c174h	4	GDBGLSP (GDBGLSP)	0h
c178h	4	GDBGEPINFO0 (GDBGEPINFO0)	0h
c17ch	4	GDBGEPINFO1 (GDBGEPINFO1)	800000h
c300h	4	Global Transmit FIFO Size Register N (GTXFIFOSIZ0_0)	42h
c380h	4	GRXFIFOSIZ0_0 (GRXFIFOSIZ0_0)	385h
c400h	4	GEVNTADRLO_0 (GEVNTADRLO_0)	0h
c404h	4	GEVNTADRHI_0 (GEVNTADRHI_0)	0h
c40ch	4	GEVNTCOUNT_0 (GEVNTCOUNT_0)	0h
c610h	4	GTXFIFOPRIDEV (GTXFIFOPRIDEV)	0h

Global SoC Bus Configuration 0 (GSBUSCFG0) – Offset c100

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**
11	0h	RW	**Data Access is Big-Endian (DATBIGEND)** This bit controls the endian modefor data accesses. 0: Little-endian (default) 1: Big-endian In big-endian mode, DMAaccess (both read and write) for packet data will utilize a Byte Invariant Big-Endianmode. Note: Since AXI requires byteinvariant endianness, settingDescBigend and DatBigEnd to one causes an address invariant transform to be applied,which is not appropriate. See section 9.3 and 9.4 of the AMBA AXI Specification. Hencefor an AXI master (DWC_USB3_MBUS_TYPE=1), this bit must be set to zero.

Bit Range	Default	Access	Field Name and Description
10:8	-	-	**Reserved**
7	0h	RW	**INCR256 Burst Type Enable (INCR256BRSTENA)** If software set this bit to “1”, the master uses INCR to do the 256-beat burst.
6	0h	RW	**INCR128 Burst Type Enable (INCR128BRSTENA)** If software set this bit to “1”, the master uses INCR to do the 128-beat burst.
5	0h	RW	**INCR64 Burst Type Enable (INCR64BRSTENA)** If software set this bit to “1”, the master uses INCR to do the 64-beat burst.
4	0h	RW	**INCR32 Burst Type Enable (INCR32BRSTENA)** If software set this bit to “1”, the master uses INCR to do the 32-beat burst.
3	0h	RW	**INCR16 Burst Type Enable (INCR16BRSTENA)** If software set this bit to "1", the master uses INCR to do the 16-beat burst.
2	1h	RW	**INCR8 Burst Type Enable (INCR8BRSTENA)** if software set this bit to "1", the master uses INCR to do the 8-beat burst
1	1h	RW	**INCR4 Burst Type Enable (INCR4BRSTENA)** When this bit is enabled the controller is allowed to do bursts of beat length 1, 2, 3, and 4
0	0h	RW	**Undefined Length INCR Burst Type Enable (INCRBrstEna) Input to BUS-GM (INCRBRSTENA)** When enabled, this has higher priority than other burst types. For the AHBconfiguration. if this bit is set to 1, AHB master tries to do only one INCR burst for eachtransfer unless it has to break it at a 1Kbyte boundary. If this bit is set to 0, the AHBmaster may still use INCR burst type at the beginning and end bursts of transfers toalign the address. The middle bursts are INCR4/8/16, depending when the type isenabled.

Global SoC Bus Configuration 1 (GSBUSCFG1) – Offset c104

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30:13	-	-	**Reserved**
12	0h	RW	**1k Page Boundary Enable (EN1KPAGE)** By default (this bit is disabled) the AXI breakstransfers at the 4k page boundary. When this bit is enabled, the AXI master (DMA data)breaks transfers at the 1k page boundary.
11:8	fh	RW	**AXI Pipelined Transfers Burst Request Limit (PipeTransLimit)** The fieldcontrols the number of outstanding pipelined transfers requests the AXI master willpush to the AXI slave. Once the AXI master reaches this limit, it will not make morerequests on the AXI ARADDR and AWADDR buses until the associated data phasescomplete. This field is encoded as follows: h0: 1 request h1: 2 requests h2: 3 requests h3: 4 requests ... hF: 16 requests
7:0	-	-	**Reserved**

Global Tx Threshold Control (GTXTHRCFG) – Offset c108

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
29	0h	RO	**USB Transmit Packet Count Enable (USBTxPktCntSel)** This fieldenables/disables the USB transmission multi-packet thresholding: 0: USB transmissionmulti-packet thresholding is disabled, the core can only start transmission on the USBafter the entire packet has been fetched into the corresponding TXFIFO. 1: USBtransmission multi-packet thresholding is enabled. The core can only start transmissionon the USB after USB Transmit Packet Count amount of packets for the USB transaction(burst) are already in the corresponding TXFIFO This mode is only valid in the hostmode. It is only used for SuperSpeed.
28	-	-	**Reserved**
27:24	0h	RO	**USB Transmit Packet Count (USBTxPktCnt)** This field specifies thenumber of packets that must be in the TXFIFO before the core can start transmission forthe corresponding USB transaction (burst). This field is only valid when the USBTransmit Packet Count Enable field is set to one. Valid values are from 1 to 15.
23:16	00h	RW	**USB Maximum TX Burst Size (USBMaxTxBurstSize)** When USBTxPktCntSel is one,this field specifies the Maximum Bulk OUT burst the core should do. When the systembus is slower than the USB, TX FIFO can underrun during a long burst. User canprogram a smaller value to this field to limit the TX burst size that the core can do. Itonly applies to SS Bulk, Isochronous, and Interrupt OUT endpoints in the host mode.Valid values are from 1 to 16
15:0	-	-	**Reserved**

Global Rx Threshold Control (GRXTHRCFG) – Offset c10c

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29	1h	RW	**USB ReceivePacket Count Enable (USBRxPktCntSel)** This field enables/disables theUSB reception multi-packet thresholding: n 0: The core can only start reception on theUSB when the RX FIFO has space for at least one packet. n 1: The core can only startreception on the USB when the RX FIFO has space for at least USBRxPktCnt amount ofpackets. This mode is only valid in the host mode. It is only used for SuperSpeed.
28	-	-	**Reserved**
27:24	4h	RW	**USB Receive Packet Count (USBRxPktCnt)** This field specifies space (in number ofpackets) that must be available in the RX FIFO before the core can start thecorresponding USB RX transaction (burst). This field is only valid when the USB ReceivePacket Count Enable field is set to one. The valid values are from 1 to 15.
23:19	08h	RW	**USB Maximum Rx Burst Size (USBMaxRxBurstSize)** This field is only validwhen USBRxPktCntSel is one. This field specifies the Maximum Bulk IN burst the coreshould do. When the system bus is slower than the USB, RX FIFO can overrun during along burst. User can program a smaller value to this field to limit the RX burst size thatthe core can do. It only applies to SS Bulk, Isochronous, and Interrupt IN endpoints inthe host mode. Valid values are from 1 to 16.
18:0	-	-	**Reserved**

Global Core Control (GCTL) – Offset c110

Bit Range	Default	Access	Field Name and Description
30:19	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
18	0h	RW	**Master Filter Bypass (MASTERFILTBYPASS)** When this bit is set to 1'b1, irrespective ofthe parameter DWC_USB3_EN_BUS_ FILTERS chosen, all the filters in theDWC_usb3_filter module will be bypassed. The double synchronizers to mac_clkpreceding the filters will also be bypassed. For enabling the filters, this bit should be1'b0.
17	-	-	**Reserved**
16	0h	RW	**U2RSTECN (U2RSTECN)** The super speed connection fails during POLL or LMP exchange, thedevice connects at non-SS mode. If this bit is set, then device attempts three moretimes to connect at SS, even if it previously failed to operate in SS mode.
15:14	0h	RW	**FRMSCLDWN (FRMSCLDWN)** This field scales down device view of a SOF/USOF/ITP duration. For SS/HS mode: 2'h3 implements interval to be 15. 625 us 2'h2 implementsinterval to be 31.25 us 2'h1 implements interval to be 62.5 us 2'h0implements interval to be125us For FS mode, the scale-down value is multiplied by 8.
13:12	2h	RW	**Port Capability Direction (PRTCAPDIR)** 2'b01: Reserved 2'b10: for Device configurations 2'b11: Reserved
11	0h	RW	**Core Soft Reset (CORESOFTRESET)** 1b0 - No soft reset 1b1 - Soft reset
10:4	-	-	**Reserved**
3	0h	RW	**Disable Scrambling (DISSCRAMBLE)** Transmit request to Link Partner on next transition to Recovery or Polling.

Bit Range	Default	Access	Field Name and Description
2	-	-	**Reserved**
1	0h	RW	**Global Hibernation Enable (GblHibernationEn)** This bit enables hibernation at the global level. If hibernation is not enabled via this bit, the PMU immediately accepts the D0->D3 and D3->D0 power state change requests, but does not save or restore any core state. In addition, the PMUs will never drive the PHY interfaces and let the core continue to drive the PHY interfaces.
0	0h	RW	**Disable Clock Gating (DSBLCLKGTNG)** When this bit is set to 1 and the core is in Low Power mode, internal clock gating is disabled.You can set this bit to 1'b1 after Power On Reset.

GPMSTS (GPMSTS) – Offset c114

Bit Range	Default	Access	Field Name and Description
31:28	0h	WO	**PortSel (PortSel)**
27:17	-	-	**Reserved**
16:12	00h	RO	**U3Wakeup (U3Wakeup)**
11:10	-	-	**Reserved**
9:0	000h	RO	**U2Wakeup (U2Wakeup)**

Global Status (GSTS) – Offset c118

Bit Range	Default	Access	Field Name and Description
30:7	-	-	**Reserved**
6	0h	RO	**Device Interrupt Pending (Device_IP)** This field indicates that there is a pendinginterrupt pertaining to peripheral (device) operation in the Device event queue
5	0h	RO	**CSR Timeout (CSRTimeout)** When this bit is 1'b1, it indicates that software performeda write or read to a core register that could not be completed withinbus clock cycles (default: 65535).
4	0h	RO	**Bus Error Address Valid (BUSERRADDRVLD)** Indicates that the GBUSERRADDR register is valid and reports the first bus address that encounters a bus error.
3:2	-	-	**Reserved**
1:0	0h	RO	**Current Mode of Operation (CURMOD)** Indicates the current mode of operation. 2'b00: Device mode 2'b01: Reserved

Bus Address Low (GBUSERRADDRLO) – Offset c130

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO	**Bus Address Low (BUSERRADDR)** This 64-bit register contains the lower 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1.It can only be cleared by resetting the core

GHWPARAMS0 (GHWPARAMS0) – Offset c140

Bit Range	Default	Access	Field Name and Description
31:24	40h	RO	DWC_USB3_ADWIDTH_31_24 (DWC_USB3_ADWIDTH_31_24)
23:16	20h	RO	DWC_USB3_SDWIDTH_23_16 (DWC_USB3_SDWIDTH_23_16)
15:8	40h	RO	DWC_USB3_MDWIDTH_15_8 (DWC_USB3_MDWIDTH_15_8)
7:6	0h	RO	DWC_USB3_SBUS_TYPE_7_6 (DWC_USB3_SBUS_TYPE_7_6)
5:3	1h	RO	DWC_USB3_MBUS_TYPE_5_3 (DWC_USB3_MBUS_TYPE_5_3)
2:0	0h	RO	DWC_USB3_MODE_2_0 (DWC_USB3_MODE_2_0)

GHWPARAMS1 (GHWPARAMS1) – Offset c144

Bit Range	Default	Access	Field Name and Description
30:27	-	-	Reserved
26	0h	RO	DWC_USB3_MAC_PHY_CLKS_SYNC_26 (DWC_USB3_MAC_PHY_CLKS_SYNC_26)
25:24	2h	RO	DWC_USB3_EN_PWROPT_25_24 (DWC_USB3_EN_PWROPT_25_24)
23	0h	RO	DWC_USB3_SPRAM_TYP_23 (DWC_USB3_SPRAM_TYP_23)
22:21	3h	RO	DWC_USB3_NUM_RAMS_22_21 (DWC_USB3_NUM_RAMS_22_21)

Bit Range	Default	Access	Field Name and Description
20:15	01h	RO	DWC_USB3_DEVICE_NUM_INT_20_15 (DWC_USB3_DEVICE_NUM_INT_20_15)
14:12	4h	RO	DWC_USB3_ASPACEWIDTH_14_12 (DWC_USB3_ASPACEWIDTH_14_12)
11:9	4h	RO	DWC_USB3_REQINFOWIDTH_11_9 (DWC_USB3_REQINFOWIDTH_11_9)
8:6	4h	RO	DWC_USB3_DATAINFOWIDTH_8_6 (DWC_USB3_DATAINFOWIDTH_8_6)
5:3	7h	RO	DWC_USB3_BURSTWIDTH_5_3 (DWC_USB3_BURSTWIDTH_5_3)
2:0	3h	RO	DWC_USB3_IDWIDTH_2_0 (DWC_USB3_IDWIDTH_2_0)

GHWPARAMS2 (GHWPARAMS2) – Offset c148

Bit Range	Default	Access	Field Name and Description
31:0	008086a0h	RO	DWC_USB3_USERID_31_0 (DWC_USB3_USERID_31_0)

GHWPARAMS3 (GHWPARAMS3) – Offset c14c

Bit Range	Default	Access	Field Name and Description
30:23	20h	RO	DWC_USB3_CACHE_TOTAL_XFER_RESOURCES_30_23 (DWC_USB3_CACHE_TOTAL_XFER_RESOURCES_30_23)
22:18	10h	RO	DWC_USB3_NUM_IN_EPS_22_18 (DWC_USB3_NUM_IN_EPS_22_18)

Bit Range	Default	Access	Field Name and Description
17:12	20h	RO	DWC_USB3_NUM_EPS_17_12 (DWC_USB3_NUM_EPS_17_12)
11	0h	RO	DWC_USB3_ULPI_CARKIT_11 (DWC_USB3_ULPI_CARKIT_11)
10	0h	RO	DWC_USB3_VENDOR_CTL_INTERFACE_10 (DWC_USB3_VENDOR_CTL_INTERFACE_10)
9:8	0h	RO	ghwparams3_9_8 (ghwparams3_9_8)
7:6	2h	RO	DWC_USB3_HSPHY_DWIDTH_7_6 (DWC_USB3_HSPHY_DWIDTH_7_6)
5:4	0h	RO	DWC_USB3_FSPHY_INTERFACE_5_4 (DWC_USB3_FSPHY_INTERFACE_5_4)
3:2	1h	RO	DWC_USB3_HSPHY_INTERFACE_3_2 (DWC_USB3_HSPHY_INTERFACE_3_2)
1:0	1h	RO	DWC_USB3_SSPHY_INTERFACE_1_0 (DWC_USB3_SSPHY_INTERFACE_1_0)

GHWPARAMS4 (GHWPARAMS4) – Offset c150

Bit Range	Default	Access	Field Name and Description
30:22	-	-	Reserved
21	1h	RO	DWC_USB3_EXT_BUFF_CONTROL_21 (DWC_USB3_EXT_BUFF_CONTROL_21)

Bit Range	Default	Access	Field Name and Description
20:17	1h	RO	**DWC_USB3_NUM_SS_USB_INSTANCES_20_17 (DWC_USB3_NUM_SS_USB_INSTANCES_20_17)**
16:13	1h	RO	**DWC_USB3_HIBER_SCRATCHBUFS_16_13 (DWC_USB3_HIBER_SCRATCHBUFS_16_13)** Number of external scratchpad buffers the core requires to save its internal state in the device mode. Each buffer is assumed to be 4KB
12	0h	RO	**ghwparams4_12 (ghwparams4_12)**
11	0h	RO	**ghwparams4_11 (ghwparams4_11)**
10:9	0h	RO	**ghwparams4_10_9 (ghwparams4_10_9)**
8:7	0h	RO	**ghwparams4_8_7 (ghwparams4_8_7)**
6	00h	RO	**ghwparams4_6 (ghwparams4_6)**
5:0	04h	RO	**DWC_USB3_CACHE_TRBS_PER_TRANSFER_5_0 (DWC_USB3_CACHE_TRBS_PER_TRANSFER_5_0)**

GHWPARAMS5 (GHWPARAMS5) – Offset c154

Bit Range	Default	Access	Field Name and Description
30:28	-	-	**Reserved**
27:22	10h	RO	**DWC_USB3_DFQ_FIFO_DEPTH_27_22 (DWC_USB3_DFQ_FIFO_DEPTH_27_22)**
21:16	20h	RO	**DWC_USB3_DWQ_FIFO_DEPTH_21_16 (DWC_USB3_DWQ_FIFO_DEPTH_21_16)**

Bit Range	Default	Access	Field Name and Description
15:10	08h	RO	**DWC_USB3_TXQ_FIFO_DEPTH_15_10 (DWC_USB3_TXQ_FIFO_DEPTH_15_10)**
9:4	08h	RO	**DWC_USB3_RXQ_FIFO_DEPTH_9_4 (DWC_USB3_RXQ_FIFO_DEPTH_9_4)**
3:0	8h	RO	**DWC_USB3_BMU_BUSGM_DEPTH_3_0 (DWC_USB3_BMU_BUSGM_DEPTH_3_0)**

GHWPARAMS6 (GHWPARAMS6) – Offset c158

Bit Range	Default	Access	Field Name and Description
31:16	02f6h	RO	**DWC_USB3_RAM0_DEPTH_31_16 (DWC_USB3_RAM0_DEPTH_31_16)**
15	0h	RO	**BusFltrsSupport (BusFltrsSupport)**
14	0h	RO	**BCSupport (BCSupport)**
13	0h	RO	**OTG_SS_Support (OTG_SS_Support)** 1’b0: No 3.0 support 1’b1: 3.0 support
12	0h	RO	**ADPSupport (ADPSupport)**
11	0h	RO	**HNPSupport (HNPSupport)**
10	0h	RO	**SRPSupport (SRPSupport)** The application uses this bit to determine the DWC_usb3 core’s SRP support. 1’b0: SRP support is not enabled 1’b1: SRP support is enabled
9:6	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
5:0	20h	RO	**DWC_USB3_PSQ_FIFO_DEPTH_5_0 (DWC_USB3_PSQ_FIFO_DEPTH_5_0)**

GHWPARAMS7 (GHWPARAMS7) – Offset c15c

Bit Range	Default	Access	Field Name and Description
31:16	0385h	RO	**DWC_USB3_RAM2_DEPTH_31_16 (DWC_USB3_RAM2_DEPTH_31_16)**
15:0	07e6h	RO	**DWC_USB3_RAM1_DEPTH_15_0 (DWC_USB3_RAM1_DEPTH_15_0)**

GDBGFIFOSPACE (GDBGFIFOSPACE) – Offset c160

Bit Range	Default	Access	Field Name and Description
31:16	0042h	RO	**SPACE_AVAILABLE (SPACE_AVAILABLE)**
15:9	-	-	**Reserved**
8:0	000h	RW	**FIFO_QUEUE_SELECT (FIFO_QUEUE_SELECT)** [8:5] indicates the FIFO/Queue Type [4:0] indicates the FIFO/Queue Number

GDBGLTSSM (GDBGLTSSM) – Offset c164

Bit Range	Default	Access	Field Name and Description
30	1h	RO	**RxElecidle (RxElecidle)**

Bit Range	Default	Access	Field Name and Description
29	0h	RO	**X3_XS_SWAPPING (X3_XS_SWAPPING)**
28	0h	RO	**X3_DS_HOST_SHUTDOWN (X3_DS_HOST_SHUTDOWN)**
27	0h	RO	**PRTDIRECTION (PRTDIRECTION)** 1'b0: Upstream 1'b1: Downstream
26	0h	RO	**LTDBTIMEOUT (LTDBTIMEOUT)**
25:22	4h	RO	**LTDBLINKSTATE (LTDBLINKSTATE)**
21:18	0h	RO	**LTDBSUBSTATE (LTDBSUBSTATE)**
17	0h	RO	**ELASTICBUFFERMODE (ELASTICBUFFERMODE)**
16	1h	RO	**TXELECLDLE (TXELECLDLE)**
15	0h	RO	**RXPOLARITY (RXPOLARITY)**
14	0h	RO	**TxDetRxLoopback (TxDetRxLoopback)**
13:11	0h	RO	**LTDBPhyCmdState (LTDBPhyCmdState)** 000: PHY_IDLE 001: PHY_DET 010: PHY_DET_3 011: PHY_PWR_DLY 100: PHY_PWR_A 101: PHY_PWR_B

Bit Range	Default	Access	Field Name and Description
10:9	2h	RO	**POWERDOWN (POWERDOWN)**
8	0h	RO	**RXEQTRAIN (RXEQTRAIN)**
7:6	1h	RO	**TXDEEMPHASIS (TXDEEMPHASIS)**
5:3	0h	RO	**LTDBClkState (LTDBClkState)** 000: CLK_NORM 001: CLK_TO_P3 010: CLK_WAIT1 011: CLK_P3 100: CLK_TO_P0 101: CLK_WAIT2
2	0000h	RO	**TXSWING (TXSWING)**
1	0000h	RO	**RXTERMINATION (RXTERMINATION)**
0	0000h	RO	**TXONESZEROS (TXONESZEROS)**

GDBGLNMCC (GDBGLNMCC) – Offset c168

Bit Range	Default	Access	Field Name and Description
30:9	-	-	**Reserved**
8:0	000h	RO	**LNMCC_BERC (LNMCC_BERC)**

GDBGBMU (GDBGBMU) – Offset c16c

Bit Range	Default	Access	Field Name and Description
31:8	000000h	RO	**BMU_BCU (BMU_BCU)**
7:4	0h	RO	**BMU_DCU (BMU_DCU)**
3:0	0h	RO	**BMU_CCU (BMU_CCU)**

GDBGLSP (GDBGLSP) – Offset c174

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO	**LSPDEBUG (LSPDEBUG)**

GDBGEPINFO0 (GDBGEPINFO0) – Offset c178

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RO	**EPDEBUG (EPDEBUG)**

GDBGEPINFO1 (GDBGEPINFO1) – Offset c17c

Bit Range	Default	Access	Field Name and Description
31:0	00800000h	RO	**EPDEBUG (EPDEBUG)**

Global Transmit FIFO Size Register N (GTXFIFOSIZ0_0) – Offset c300

FIFO_number: 0<= n <= 15

Offset: C300h + FIFO_number * 04h

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	0042h	RW	**TXFDEP_N (TXFDEP_N)**

GRXFIFOSIZ0_0 (GRXFIFOSIZ0_0) – Offset c380

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW	**RXFSTADDR_N (RXFSTADDR_N)**
15:0	0385h	RW	**RXFDEP_N (RXFDEP_N)**

GEVNTADRLO_0 (GEVNTADRLO_0) – Offset c400

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**EVNTADRLO (EVNTADRLO)**

GEVNTADRHI_0 (GEVNTADRHI_0) – Offset c404

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**EVNTADRHI (EVNTADRHI)**

GEVNTCOUNT_0 (GEVNTCOUNT_0) – Offset c40c

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0000h	NA	**EVNTCOUNT (EVNTCOUNT)**

GTXFIFOPRIDEV (GTXFIFOPRIDEV) – Offset c610

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0000h	RW	**gtxfifopridev (gtxfifopridev)**

xDCI PCI Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Device ID and Vendor ID (DEVVENDID)	AAA8086h
4h	4	Status and Command (STATUSCOMMAND)	100000h
10h	8	Base Address Register (BAR)	4h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
18h	8	Base Address Register1 (BAR1)	4h
2ch	4	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)	0h
34h	4	Capabilities Pointer (CAPABILITYPTR)	80h
3ch	4	Interrupt Register (INTERRUPTREG)	100h
80h	4	PowerManagement Capability ID (POWERCAPID)	48039001h
84h	4	Power Management Control and Status (PMECTRLSTATUS)	8h
90h	4	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)	F0140009h
94h	4	Device ID and Vendor Specific Register (DEVID_VEND_SPECIFIC_REG)	1400010h
98h	4	SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)	0h
9ch	4	Device IDLE pointer register (DEVICE_IDLE_ POINTER_REG)	10F8301h
a0h	4	(D0I3_MAX_POW_LAT_PG_CONFIG)	80800h

Device ID and Vendor ID (DEVVENDID) – Offset 0

Bit Range	Default	Access	Field Name and Description
31:16	See Description	RO	**(DEVICEID)** Device ID identifies the particular PCI device. Refer to the Device and Revision ID Table in Volume 1 for default value.
15:0	8086h	RO	**Vendor Identification (VENDORID)** Vendor ID is a unique ID identifying the manufacturer of the device. 8086h = Intel

Status and Command (STATUSCOMMAND) – Offset 4

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29	0h	RW/1C	**Received Master Abort (RMA)** If the completion status received from IOSF is UR, the Bridge sets this bit. Thesoftware writes a 1 to this bit to clear it.
28	0h	RW/1C	**Received Target Abort (RTA)** If the completion status received from IOSF is CA, the Bridge sets this bit. Thesoftware writes a 1 to this bit to clear it.
27:21	-	-	**Reserved**
20	1h	RO	**Capabilities List (CAPLIST)** Indicates that the controller contains a capabilities pointer list. The firstitem is pointed to by looking at the configuration offset 34h.
19	0h	RO	**Interrupt Status (INTR_STATUS)** This bit reflects state of interrupt in the device Only when theInterrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a1, is the device/function interrupt message sent. Setting the Interrupt Disable bit to a1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:11	-	-	**Reserved**
10	0h	RW	**Interrupt Disable (INTR_DISABLE)** Interrupt Disable: Setting this bit disables INTx assertion fromBridge. The interrupt disabled is legacy INTx# interrupt, which is the Bridge does notsend Interrupt Assert message through the IOSF Sideband Channel. Reset value ofthis bit is 0. This bit has no connection with the interrupt status bit.
9	-	-	**Reserved**
8	0h	RW	**SERR Enable (SERR_ENABLE)** Not implemented
7:3	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
2	0h	RW	**Bus Master Enable (BME)** Bus Master Enable: If this bit is 0,the Bridge does not generate any newupstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0h	RW	**Memory Space Enable (MSE)** Memory Space Enable: This bit controls Bridge response to downstreammemory accesses. When set, accesses to memory space of the device is enabled.Reset value of this bit is 0.
0	-	-	**Reserved**

Base Address Register (BAR) – Offset 10

Bit Range	Default	Access	Field Name and Description
63:21	0000000 0000h	RW	**Base Address Register Low (BASEADDR)**
20:12	-	-	**Reserved**
11:4	00h	RO	**Size Indicator (SIZEINDICATOR)** Always returns 0. The size of this register depends on the size of the memory space.
3	0h	RO	**Prefetchable (PREFETCHABLE)** Indicates that this BAR is not prefetchable
2:1	2h	RO	**Type (TYPE)** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range, If BAR_64b_ EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h	RO	**Memory Space Indicator (MESSAGE_SPACE)** 0 indicates this BAR is present in the memory space.

Base Address Register1 (BAR1) – Offset 18

Memory accesses to BAR1 region are aliased to the PCI configuration space. The BAR1region is always 4K. Software access through BAR1 can only access the regular PCIconfiguration space. BAR1 memory accesses, which do not access a defined PCIconfiguration register, are treated as access to reserved register. If this register isdisabled then this is RO and always returns 0.

Bit Range	Default	Access	Field Name and Description
63:32	00000000h	RW	**Base Address high (BASEADDR1_HIGH)**
31:12	00000h	RW	**(BASEADDR1)** This field is present if BAR1 is enabled through private configuration space.
11:4	00h	RO	**Size Indicator (SIZEINDICATOR1)** Always is 0 as minimum size is 4K
3	0h	RO	**Prefetchable (PREFETCHABLE1)** Indicates that this BAR is not prefetchable.
2:1	2h	RO	**Type (TYPE1)** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_ EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h	RO	**Memory Space Indicator (MESSAGE_SPACE1)** 0 Indicates this BAR is present in the memory space.

Subsystem Vendor and Subsystem ID (SUBSYSTEMID) – Offset 2c

SVID register along with SID register is to distinguish subsystem from another

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW/O	**Subsystem ID (SUBSYSTEMID)** This register is implemented for any function thatcan be instantiated more than once in a given system. The SID register, incombination with the Subsystem Vendor ID register make it possible for theoperating environment to distinguish one subsystem from the other. This register is aRead Write Once type register.
15:0	0000h	RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID)** This register must be implemented for any function thatcan be instantiated more than once in a given system. The SVID register, incombination with the Subsystem ID register, enables the operating environment todistinguish one subsystem from the other. This register is a Read Write Once register

Capabilities Pointer (CAPABILITYPTR) – Offset 34

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7:0	80h	RO	**Capabilities Pointer (CAPPTR_POWER)** Indicates what the next capability is.

Interrupt Register (INTERRUPTREG) – Offset 3c

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO	**Max Latency (MAX_LAT)** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	00h	RO	**Min Latency (MIN_GNT)** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	-	-	**Reserved**
11:8	1h	RO	**Interrupt Pin (INTPIN)** Interrupt Pin Value in this register is reflected from the IPIN value in theprivate configuration space. For a single function device, this ideally is INTA.
7:0	00h	RW	**Interrupt Line (INTLINE)** PCH does not use this field directly. It is used to communicate tosoftware, the interrupt line to which the interrupt pin is connected.

PowerManagement Capability ID (POWERCAPID) – Offset 80

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:27	09h	RO	**(PMESUPPORT)**
26:19	-	-	**Reserved**
18:16	3h	RO	**Version (VERSION)** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h	RO	**Next Capability (NXTCAP)** Points to the next capability structure.
7:0	01h	RO	**Power Management Capability (POWER_CAP)** Indicates this is power management capability.

Power Management Control and Status (PMECTRLSTATUS) – Offset 84

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15	0h	RW/1C	**PME Status (PMESTATUS)** 0 Software clears the bit by writing a 1 to it. 1 This bit is set when the PME# signal is asserted independent of the state of the PMEEnable bit (bit 8 in this register)
14:9	-	-	**Reserved**
8	0h	RW	**PME Enable (PMEENABLE)** 1 Enables the function to assert PME#. 0 PME# message on Sideband is disabled
7:4	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
3	1h	RO	**No Soft Reset (NO_SOFT_RESET)** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	-	-	**Reserved**
1:0	0h	RW	**Power State (POWERSTATE)** This field is used both to determine the current power state and toset a new power state.The values are: 00 D0 state 11 D3HOT state Others Reserved

PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD) – Offset 90

Bit Range	Default	Access	Field Name and Description
31:28	0Fh	RO	**(VEND_CAP)** Vendor Specific Capability ID
27:24	0h	RO	**(REVID)** Revision ID of capability structure
23:16	14h	RO	**(CAP_LENGTH)** Vendor Specific Capability Length
15:8	00h	RO	**(NEXT_CAP)** Next Capability
7:0	09h	RO	**(CAPID)** Capability ID

Device ID and Vendor Specific Register (DEVID_VEND_SPECIFIC_REG) – Offset 94

Bit Range	Default	Access	Field Name and Description
31:20	014h	RO	**(VSEC_LENGTH)** Vendor Specific Extended Capability Length
19:16	0h	RO	**(VSEC_REV)** Vendor specific Extended Capability revision
15:0	0010h	RO	**(VSECID)** Vendor Specific Extended Capability ID

SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG) – Offset 98

Bit Range	Default	Access	Field Name and Description
31:4	0000000h	RO	**(SW_LAT_DWORD_OFFSET)** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h	RO	**(SW_LAT_BAR_NUM)** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h	RO	**Valid (SW_LAT_VALID)**

Device IDLE pointer register (DEVICE_IDLE_POINTER_REG) – Offset 9c

Bit Range	Default	Access	Field Name and Description
31:4	010F830h	RO	**(DWORD_OFFSET)** Contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR

Bit Range	Default	Access	Field Name and Description
3:1	0h	RO	**BAR Number (BAR_NUM)** Indicates that the D0i3 MMIO location is always at BAR0
0	1h	RO	**Valid (VALID)**

(D0I3_MAX_POW_LAT_PG_CONFIG) – Offset a0

Bit Range	Default	Access	Field Name and Description
30:22	-	-	**Reserved**
21	0h	RW	**(HAE)** Hardware Autonomous Enable
20	-	-	**Reserved**
19	1h	RW	**(SLEEP_EN)** Sleep Enable
18	0h	RW	**(D3HEN)** D3-Hot Enable (D3HEN): If 1, then the function will power gate when idle and the PMCSR[1:0] register in the function D3.
17	0h	RW	**(DEVIDLEN)** If 1, then the function will power gate when idle and the DevIdle register (DevIdleC[2]=1) is set.
16	0h	RW	**(D3_ENABLE)** D3-Hot Enable (D3HEN): If set to 1, then function will power gate when idle and the PMCSR[1:0] register in the function = 11 (D3).
15:13	-	-	**Reserved**
12:10	2h	RW/O	**(POW_LAT_SCALE)** Power On Latency Scale

Bit Range	Default	Access	Field Name and Description
9:0	000h	RW/O	**(POW_LAT_VALUE)** Power On Latency value

xHCI Configuration Registers

Summary of Bus:, Device:, Function: (CFG)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	Vendor ID (VID)	8086h
2h	2	Device ID (DID)	XXXXh
4h	2	Command (CMD)	0h
6h	2	Device Status (STS)	290h
8h	1	Revision ID (RID)	XXh
9h	1	Programming Interface (PI)	30h
ah	1	Sub Class Code (SCC)	3h
bh	1	Base Class Code (BCC)	Ch
dh	1	Master Latency Timer (MLT)	0h
eh	1	Header Type (HT)	80h
10h	8	Memory Base Address (MBAR)	4h
2ch	2	USB Subsystem Vendor ID (SSVID)	0h
2eh	2	USB Subsystem ID (SSID)	0h
34h	1	Capabilities Pointer (CAP_PTR)	70h
3ch	1	Interrupt Line (ILINE)	0h
3dh	1	Interrupt Pin (IPIN)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
40h	4	XHC System Bus Configuration 1 (XHCC1)	1FDh
44h	4	XHC System Bus Configuration 2 (XHCC2)	3C000h
50h	4	Clock Gating (XHCLKGTEN)	0h
58h	4	Audio Time Synchronization (AUDSYNC)	0h
60h	1	Serial Bus Release Number (SBRN)	31h
61h	1	Frame Length Adjustment (FLADJ)	60h
62h	1	Best Effort Service Latency (BESL)	0h
70h	1	PCI Power Management Capability ID (PM_CID)	1h
71h	1	Next Item Pointer #1 (PM_NEXT)	80h
72h	2	Power Management Capabilities (PM_CAP)	C1C2h
74h	2	Power Management Control/Status (PM_CS)	8h
80h	1	Message Signaled Interrupt CID (MSI_CID)	5h
81h	1	Next item pointer (MSI_NEXT)	0h
82h	2	Message Signaled Interrupt Message Control (MSI_MCTL)	86h
84h	4	Message Signaled Interrupt Message Address (MSI_MAD)	0h
88h	4	Message Signaled Interrupt Upper Address (MSI_MUAD)	0h
8ch	2	Message Signaled Interrupt Message Data (MSI_MD)	0h
a2h	2	Power Control Enable (PCE_REG)	8h
a4h	4	High Speed Configuration 2 (HSCFG2)	2000h
a8h	4	Super Speed Configuration 1 (SSCFG1)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
d0h	4	XHCI USB3 Overcurrent Pin Mapping N (U3OCM)	0h
b0h	4	XHCI USB2 Overcurrent Pin Mapping N (U2OCM)	0h

Vendor ID (VID) – Offset 0

Bit Range	Default	Access	Field Name and Description
15:0	8086h	RO	**Vendor ID (VID)** 8086h indicates Intel.

Device ID (DID) – Offset 2

Bit Range	Default	Access	Field Name and Description
15:0	See Description	RO/V	**Device ID (DID)** See the Device and Revision ID Table in Volume 1 for the default value.

Command (CMD) – Offset 4

Bit Range	Default	Access	Field Name and Description
14:11	-	-	**Reserved**
10	0b	RW	**Interrupt Disable (ID)** When cleared to 0, the function is capable of generating interrupts. When 1, the function can not generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit is not affected by the interrupt enable.

Bit Range	Default	Access	Field Name and Description
9	0b	RO	**Fast Back to Back Enable (FBE)**
8	0b	RW	**SERR# Enable (SERR)** When set to 1, the XHC is capable of generating (internally) SERR#.
7	0b	RO	**Wait Cycle Control (WCC)**
6	0b	RW	**Parity Error Response (PER)** When set to 1, the XHCI Host Controller will check for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase as recommended by the XHCI specification. Note that this applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#.
5	0b	RO	**VGA Palette Snoop (VPS)**
4	0b	RO	**Memory Write Invalidate (MWI)**
3	0b	RO	**Special Cycle Enable (SCE)**
2	0b	RW	**Bus Master Enable (BME)** When set, it allows XHC to act as a bus master. When cleared, it disable XHC from initiating transactions on the system bus.
1	0b	RW	**Memory Space Enable (MSE)** This bit controls access to the XHC Memory Space registers. If this bit is set, accesses to the XHC registers are enabled. The Base Address register for the XHC should be programmed before this bit is set.
0	0b	RO	**I/O Space Enable (IOSE)** Reserved as 0. Read-Only.

Device Status (STS) – Offset 6

Bit Range	Default	Access	Field Name and Description
15	0b	RW/1C	**Detected Parity Error (DPE)** This bit is set by the Intel PCH whenever a parity error is seen on the internal interface to the XHC host controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions. Software clears this bit by writing a 1 to this bit location.
14	0b	RW/1C	**Signaled System Error (SSE)** This bit is set by the Intel PCH whenever it signals SERR# (internally). The SERR_EN bit (bit 8 in the Command Register) must be 1 for this bit to be set. Software clears this bit by writing a 1 to this bit location.
13	0b	RW/1C	**Received Master-Abort Status (RMA)** This bit is set when XHC, as a master, receives a master-abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.
12	0b	RW/1C	**Received Target Abort Status (RTA)** This bit is set when XHC, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.
11	0b	RW/1C	**Signaled Target-Abort Status (STA)** This bit is used to indicate when the XHC function responds to a cycle with a target abort.
10:9	01b	RO	**DEVSEL# Timing Status (DEVT)** This 2-bit field defines the timing for DEVSEL# assertion. Read-Only.
8	0b	RW/1C	**Master Data Parity Error Detected (MDPED)** This bit is set by the Intel PCH whenever a data parity error is detected on a XHC read completion packet on the internal interface to the XHC host controller and bit 6 of the Command register is set to 1. Software clears this bit by writing a 1 to this bit location.
7	1b	RO	**Fast Back-to-Back Capable (FBBC)** Reserved as 1 Read-Only.
6	0b	RO	**User Definable Features (UDF)** Reserved as 0. Read-Only.
5	0b	RO	**66 MHz Capable (MC)** Reserved as 0. Read-Only.

Bit Range	Default	Access	Field Name and Description
4	1b	RO	**Capabilities List (CL)** Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer.
3	0b	RO/V	**Interrupt Status (IS)** This read-only bit reflects the state of this function's interrupt at the input of the enable/disable logic. This bit is a 1 when the interrupt is asserted. This bit will be 0 when the interrupt is deasserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
2:0	-	-	**Reserved**

Revision ID (RID) – Offset 8

Bit Range	Default	Access	Field Name and Description
7:0	See Description	RO/V	**Revision ID (RID)** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 of the EDS for specific value.

Programming Interface (PI) – Offset 9

Bit Range	Default	Access	Field Name and Description
7:0	30h	RO	**Programming Interface (PI)** A value of 30h indicates that this USB Host Controller conforms to the XHCI specification.

Sub Class Code (SCC) – Offset a

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
7:0	03h	RO	**Sub Class Code (SCC)** A value of 03h indicates that this is a Universal Serial Bus Host Controller.

Base Class Code (BCC) – Offset b

Bit Range	Default	Access	Field Name and Description
7:0	0Ch	RO	**Base Class Code (BCC)** A value of 0Ch indicates that this is a Serial Bus controller.

Master Latency Timer (MLT) – Offset d

Bit Range	Default	Access	Field Name and Description
7:0	00h	RO	**Master Latency Timer (MLT)** Because the XHC controller is internally implemented with arbitration on an internal interface, it does not need a master latency timer. The bits will be fixed at 0.

Header Type (HT) – Offset e

Bit Range	Default	Access	Field Name and Description
7	1b	RO	**Multi-Function Bit (MFB)** Read only indicating single function device.
6:0	00h	RO	**Configuration layout (CL)** Hardwired to 0 to indicate a standard PCI configuration layout.

Memory Base Address (MBAR) – Offset 10

Value in this register will be different after the enumeration process.

Bit Range	Default	Access	Field Name and Description
63:16	0000000 00000h	RW	**Base Address (BA)** Bits (63:16) correspond to memory address signals (63:16), respectively. This gives 64 KB of relocatable memory space aligned to 64 KB boundaries.
15:4	-	-	**Reserved**
3	0b	RO	**Prefetchable (Prefetchable)** This bit is hardwired to 0 indicating that this range should not be prefetched.
2:1	10b	RO	**Type (Type)** If this field is hardwired to 00 it indicates that this range can be mapped anywhere within 32-bit address space. If this field is hardwired to 10 it indicates that this range can be mapped anywhere within 64-bit address space.
0	0b	RO	**Resource Type Indicator (RTE)** This bit is hardwired to 0 indicating that the base address field in this register maps to memory space

USB Subsystem Vendor ID (SSVID) – Offset 2c

This register is modified and maintained by BIOS

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW/L	**USB Subsystem Vendor ID (SSVID)** This register, in combination with the USB Subsystem ID register, enables the operating system to distinguish each subsystem from the others.

USB Subsystem ID (SSID) – Offset 2e

This register is modified and maintained by BIOS

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW/L	**USB Subsystem ID (SSID)** BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s).

Capabilities Pointer (CAP_PTR) – Offset 34

Bit Range	Default	Access	Field Name and Description
7:0	70h	RO	**Capabilities Pointer (CAP_PTR)** This register points to the starting offset of the capabilities ranges.

Interrupt Line (ILINE) – Offset 3c

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW	**Interrupt Line (ILINE)** This data is not used by the Intel PCH. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

Interrupt Pin (IPIN) – Offset 3d

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW/L	**Interrupt pin (IPIN)** Bits 7:0 reflect the Interrupt Pin assigned to the host controller by the platform (and are hardwired).

XHC System Bus Configuration 1 (XHCC1) – Offset 40

Bit Range	Default	Access	Field Name and Description
31	0b	RW/O	**Access Control (ACCTRL)** This bit is used by BIOS to lock/unlock lockable bits. When set to '1' the write access to bits locked by this bit is disabled (locked state). When set to '0', the write access to bit locked by this bit is enabled (unlocked state). Writable once after platform reset.
30:25	-	-	**Reserved**
24	0b	RW	**Master/Target Abort SERR (RMTASERR)** When set, it allows the out-of-band error reporting from the xHCI Controller to be reported as SERR# (if SERR# reporting is enabled) and thus set the STS.SSE bit.
23	0b	RW/1C	**Unsupported Request Detected (URD)** Set the HW when xHCI Controller received an unsupported request posted cycle. Cleared by SW when the bit is written with value of '1'.
22	0b	RW	**Unsupported Request Report Enable (URRE)** When set this bit allows the URD bit to be reported as SERR# (if SERR# reporting is enabled) and thus set the STS.SSE bit.
21:19	000b	RW	**Inactivity Initiated L1 Enable (IIL1E)** If programmed to non-zero, it allows L1 power managed to be enabled after the time-out period specified. 000: Disabled 001: 32 bb_cclk 010: 64 bb_cclk 011: 128 bb_cclk 100: 256 bb_cclk 101: 512 bb_cclk 110: 1024 bb_cclk 111: 131072 bb_cclk
18	0b	RW	**XHC Initiated L1 Enable (XHCIL1E)** If set, allow the XHC initiated L1 power mangement to be enabled.

Bit Range	Default	Access	Field Name and Description
17	0b	RW	**D3 Initiated L1 Enable (D3IL1E)** If set, allow PCI device state D3 initiated L1 power managment to be enables.
16:12	-	-	**Reserved**
11	0h	RW	**SW Assisted xHC Idle (SWAXHCI)** This bit being set will indicate xHC idleness (through SW means), which must be a '1' to allow L1 entry, and subsequently allow backbone clock to be gated. This bit is to be set by Intel xHCI driver after checking that the xHCI Controller will stay in idle state for a significant period of time, e.g. all ports disconnected. This bit can be cleared under the following conditions (see SWAXHCI Policy bits in xHC System Bus Configuration 2 register) SW: SW could write 0 to clear this bit.n HW: HW, under policy control, will clear this bit on an MMIO access to the Host Controller.n HW: HW, under policy control, will clear this bit when HW exits Idle state.
10:8	001b	RW	**L23 to Host Reset Acknowledge Wait Count (L23HRAWC)** If programmed to non zero, it allows a wait period after the L23 PHY has shutdown before returning host reset acknowledge to PMC. 000: Disabled 001: 128 bb_cclk 010: 256 bb_cclk 011: 512 bb_cclk 100: 1024 bb_cclk 101: 2048 bb_cclk 110: 4096 bb_cclk 111: 131072 bb_cclk
7:6	11b	RW	**Upstream Type Arbiter Grant Count Posted (UTAGCP)** Grant count for IOSF upstream L2 request type arbiter for posted type

Bit Range	Default	Access	Field Name and Description
5:4	11b	RW	**Upstream Type Arbiter Grant Count Non Posted (UDAGCNP)** Grant count for IOSF upstream L2 type arbiter for non-posted type
3:2	11b	RW	**Upstream Type Arbiter Grant Count Completion (UDAGCCP) (UDAGCCP)** Grant count for IOSF upstream L2 type arbiter for completion type
1:0	01b	RW	**Upstream Device Arbiter Grant Count (UDAGC) (UDAGC)** Grant count for IOSF upstream L1 device arbiter

XHC System Bus Configuration 2 (XHCC2) – Offset 44

Bit Range	Default	Access	Field Name and Description
31	0b	RW	**OC Configuration Done (OCCFGDONE)** This bit is used by BIOS to prevent spurious switching during OC configuration. It must be set by BIOS after configuration of the OC mapping bits is complete. Once this bit is set, OC mapping shall not be changed by SW.
30:26	-	-	**Reserved**
25	0b	RW	**DMA Request Boundary Crossing Control (DREQBCC)** This bit controls the boundary crossing limit of each Read/Write Request. 0: 4KB 1: 64B
24:22	0h	RW	**IDMA Read Request Size Control (IDMA_RDREQSZCTRL)** Read Request Size Control: This bit controls the maximum size of each Read Request. 000: 128B 001: 256B 011 - 110: Reserved 111: 64B

Bit Range	Default	Access	Field Name and Description
21	0b	RW	**XHC Upstream Read Relaxed Ordering Enable (XHCUPRDROE)** This policy controls the Relaxed Ordering attribute for upstream reads. 0 - xHC will clear RO for all upstream read requests. 1 - xHC will set RO for all upstream read requests.
20	0b	RW	**IOSF Sideband Register Access Disable (IOSFSRAD)** When set, it disables the IOSF sideband interface from accepting any host space register access.
19:14	0Fh	RW	**Upstream Non-Posted Pre-Allocation (UNPPA)** This field reserves data sizes, in 64 byte chunks, of the downstream completion resource. This value is zero based. 000000 - 111111: Pre-allocate 64 bytes - 4096 bytes If set greater than the default allows over-allocation If set less than default allows under-allocation Only allowed to be programmed when BME = 0 and no outstanding downstream completion
13:12	00b	RW	**SW Assisted xHC Idle Policy (SWAXHCIP)** Note: Irrespective of the setting of this field, SW write of 0 to SWAXHCI will clear the bit. 00b (default): xHC HW clears SWAXHCI bit upon MMIO access to Host Controller OR xHC HW exits Idle state 01b: xHC HW does not autonomously clear SWAXHCI bit. The bit could be cleared only by SW. 10b: xHC HW clears SWAXHCI upon MMIO acces to Host Controller. xHC HW exit from Idle state will not clear SWAXHCI. 11b: Reserved

Bit Range	Default	Access	Field Name and Description
11	0h	RW	**MMIO Read After MMIO Write Delay Disable (RAWDD)** This field controls delay on MMIO Read after MMIO Write. 0b (Default): Delay MMIO Read after MMIO Write 1b: Do not delay MMIO Read after MMIO Write Note that this delay applies after the second of the two DW writes in the case where the IOSF Gasket splits a QW write into two single DW writes to the IP.
10	0h	RW	**MMIO Write After MMIO Write Delay Enable (WAWDE)** This field controls delay on MMIO Write after previous MMIO Write. 0b (Default): Do not delay MMIO Write after previous MMIO Write 1b: Delay MMIO Write after previous MMIO Write Note that the delay count does not apply on the second of the two DW writes that are generated by IOSF Gasket when it splits a QW write into two. In other words, the second of the two DW writes could happen without any delay with respect to the first DW write. This choice is being made for ease of ECO. The delay count, in this case, will apply after the second of the two DW writes.

Bit Range	Default	Access	Field Name and Description
9:8	0h	RW	**SW Assisted Cx Inhibit (SWACXIHB)** This field controls how the DMI L1 inhibit signal from USB 3.1 to PMC will behave. 00: Never inhibit Cx 01: Inhibit Cx when Isochronous Endpoint is active (PPT Behavior) 10: Inhibit Cx when Periodic Active as defined in 40.4.3.2. 111: Always inhibit Cx
7:6	0h	RW	**SW Assisted DMI L1 Inhibit (SWADMIL1IHB)** This field controls how the DMI L1 inhibit signal from USB 3.1 to DMI will behave.00: Never inhibit DMI L1.01: Inhibit DMI L1 when Isochronous Endpoint is active (PPT Behavior).10: Inhibit DMI L1 when Priodic Active as defined in 40.4.3.2.1.11: Inhibit DMI L1 if XHCC1.SWAXHCI = 0.
5:3	0h	RW	**L1 Force P2 Clock Gating Wait Count (L1FP2CGWC)** If programmed to non zero, it allows L1 force P2 gating off the clock to be delayed after the time-out period specified. If wake up event is detected before the time-out, pclk remains alive and trigger L1 exit as though CPU host is causing the wake, 000: Disabled 001: 128 bb_cclk 010: 256 bb_cclk 011: 512 bb_cclk 100: 1024 bb_cclk 101: 2048 bb_cclk 110: 4096 bb_cclk 111: 131072 bb_cclk

Bit Range	Default	Access	Field Name and Description
2:0	000b	RW	**Read Request Size Control (RDREQSZCTRL)** Read Request Size Control: This bit controls the maximum size of each Read Request. 000: 128B 001: 256B 010: 512B 011 - 110: Reserved 111: 64B

Clock Gating (XHCLKGTEN) – Offset 50

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**
28	0b	RW	**Nak'ing USB2.0 EPs for Backbone Clock Gating and PLL Shutdown (NUEFBCGPS)** This field controls whether Naking USB2.0 EPs, once in Naking low priority schedule, should be considered as active for the considerations for backbone clock gating and PLL shutdown or not. 0: Naking USB2.0 EPs are not considered to be active for Backbone Clock Gating and PLL Shutdown evaluation. 1: Naking USB2.0 EPs are considered to be active for Backbone clock gating and PLL shutdown evaluation.

Bit Range	Default	Access	Field Name and Description
27	0b	RW	**SRAM Power Gate Enable (SRAMPGTEN)** This register enables the SRAM Power Gating when PLL shutdown conditions for all clock domains have been met 0 - Disallow SRAM Power Gating. 1 - Allow SRAM Power Gating
26	0h	RW	**SS Link PLL Shutdown Enable (SSLSE)** This register enables the SS P3 state to be exposed to PXP PLL Shutdown conditions on behalf of all USB SS Ports ontop of trunk clock gating. 0 - P3 state NOT allowed to result in PXP PLL shutdown. 1- P3 state allowed to result in PXP PLL shutdown
25	0h	RW	**USB2 PLL Shutdown Enable (USB2PLLSE)** When set, this bit allows USB2 PLL to be shutdown when HS Link trunk clock is gated, and xHC can tolerate PLL spin up time for subsequent clock request.
24	0h	RW	**IOSF Sideband Trunk Clock Gating Enable (IOSFSTCGE)** When set, this bit allows the IOSF sideband clock trunk to be gated when idle conditions are met.
23:20	0h	RW	**HS Backbone PXP Trunk Clock Gate Enable (HSTCGE)** This register determines the HS Ux state(s) which will be exposed to Backbone PXP trunk gating of core clock. Uy is a state allowed to result in trunk gating when ss_tcg_ux_en(x) is asserted. (0) ==) U0 or deeper (1) ==) NA (no support for U1) (2) ==) U2 (L1) or deeper (3) ==) U3 (L2) or deeper

Bit Range	Default	Access	Field Name and Description
19:16	0h	RW	**SS Backbone PXP Trunk Clock Gate Enable (SSTCGE)** This register determines the SS Ux state(s) which will be exposed to Backbone PXP trunk gating of core clock. Uy is a state allowed to result in trunk gating when ss_tcg_ux_en(x) is asserted. (0) ==> U0 or deeper (1) ==> U1 or deeper (2) ==> U2 or deeper (3) ==> U3 or deeper

Bit Range	Default	Access	Field Name and Description
15	0h	RW	**XHC Ignore_EU3S (XHCIGEU3S)** This register determines if the xHC will use the EU3S as a condition to allow for Frame timer gating. 0 - xHC may allow frame timer to be gated when EU3S is set and all ports are in the required state. 1 - xHC may allow frame timer to be gated regardless of EU3S.
14	0h	RW	**XHC Frame Timer Clock Shutdown Enable (XHCFTCLKSE)** This register determines if the xHC will allow the frame timer clock to be gated. 0 - xHC will not allow ICC PLL 96MHz output to be shutdown thus keeping the frame timer running. 1 - xHC will allow ICC PLL 96MHz output to be shutdown under specific conditions.
13	0h	RW	**XHC Backbone PXP Trunk Clock Gate In Presence of ISOCH EP (XHCBBTCGIPISO)** This register controls the policy on allowing Backbone PXP trunk clock gate in the presence of IDLE ISOCH EP s with active DB. Allows the periodic active to be used in enabling Backbone PXP trunk clock gating of core clock. 0 - Trunk gate of core clock is not allowed when ISOCH EP DB is set and ISOCH EP s are idle. 1 - Allow trunk gate of core clock when ISOCH EP DB is set and ISOCH EP s are idle.

Bit Range	Default	Access	Field Name and Description
12	0h	RW	**XHC HS Backbone PXP Trunk Clock Gate U2 non RWE (XHCHSTCGU2NRWE)** This register controls the policy on allowing Backbone PXP trunk gating of core clock when there is atleast 1 non Remote Wake Enabled HS Port in U2. 0 - Prevent trunk gate of core clock when a non RWE HS Port is in U2. 1 - Allow trunk gate of core clock when a non RWE HS Port is in U2.
11:10	0h	RW	**XHC USB2 PLL Shutdown Lx Enable (XHCUSB2PLLSDLE)** This register determines the HS Link state(s) which will be exposed to USB2 PLL Shutdown conditions on behalf of all USB2 HS Ports. Ly is a state allowed to result in USB2 PLL Shutdown when en(x) is asserted. (0) ==> L1 or deeper (1) ==> L2 or deeper

Bit Range	Default	Access	Field Name and Description
9:8	00b	RW	**HS Backbone PXP PLL Shutdown Ux Enable (HSUXDMIPLLSE)** This register determines the Ux state(s) which will be exposed to PXP PLL Shutdown conditions. PLL Shutdown is allowed in: 00b Disabled (Link states shall be disabled for DMI PLL shutdown) 01b U0 or conditions for 10b setting. 10b U2 or conditions for 11b setting. 10b U3, Disconnected, Disabled or Powered-Off.

Bit Range	Default	Access	Field Name and Description
7:5	000b	RW	**SS Backbone PXP PLL Shutdown Ux Enable (SSPLLSUE)** This register determines the Ux state(s) which will be exposed to DMI PLL Shutdown conditions. PLL Shutdown is allowed in: 000b Disabled (Link states shall be ignored for DMI PLL shutdown). 001b U0 or conditions for 010b setting. 010b U1 or conditions for 011b setting. 011b U2 or conditions for 100b setting. 100b U3, Disconnected, Disabled or Powered-Off
4	0b	RW	**XHC Backbone Local Clock Gating Enable (XHCBLCGE)** When set, this bit allows XHCI Controller IP backbone clock to be locally gated when idle conditions are met.
3	0b	RW	**HS Link Trunk Clock Gating Enable (HSLTCGE)** When set, this bit allows High Speed Link control's 480 MHz and its 48/60 MHz link clock trunk to be gated when idle conditions are met.
2	0b	RW	**SS Link Trunk Clock Gating Enable (SSLTCGE)** When set, this bit allows the SuperSpeed Link control's 250 MHz and its divided 125 MHz link clock trunk to ge gated when idle conditions are met.

Bit Range	Default	Access	Field Name and Description
1	0b	RW	**IOSF Backbone Trunk Clock Gating Enable (IOSFBTCGE)** When set, this bit allows the IOSF backbone clock trunk to be gated when idle conditions are met.
0	0b	RW	**IOSF Gasket Backbone Local Clock Gating Enable (IOSFBLCGE)** When set, this bit allows the IOSF Gasket backbone clock to be locally gated when idle conditions are met.

Audio Time Synchronization (AUDSYNC) – Offset 58

This 32 bit register is used for audio stream synchronization across different devices. Global signal sample_now captures a value in AUDSYNC register.

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29:16	0000h	RO/V	**Captured Frame List Current Index/Frame Number (CMFI)** The value in this register is updated in response to sample_now signal. Bits (29:16) reflect state of bits (13:0) of FRINDEX
15:13	-	-	**Reserved**
12:0	0000h	RO/V	**Captured Micro-frame BLIF (CMFB)** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done in FLA.

Serial Bus Release Number (SBRN) – Offset 60

Bit Range	Default	Access	Field Name and Description
7:0	31h	RO	**Serial Bus Release Number (SBRN)** A value of 30h indicates that this controller follows USB release 3.0.

Frame Length Adjustment (FLADJ) – Offset 61

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit in the USBSTS register is a one. Changing value of this register while the host controller is operating yields undefined results.

Bit Range	Default	Access	Field Name and Description
6	1b	RO	**No Frame Length Timing Capability (NO_FRAME_LENGTH_TIMING_CAP)** This flag is set to 1 to indicate that the host controller does not support a programmable Frame Length Timing Value field.
5:0	20h	RO	**Frame Length Timing Value (FLTV)** SOF (micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (number of High Speed bit times) FLADJ Value (decimal) (decimal) 59488 0 (00h) 59504 1 (01h) 59520 2 (02h) ... 59984 31 (1Fh) 60000 32 (20h) ... 60480 62 (3Eh) 60496 63 (3Fh) Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (# High Speed bit times) FLADJ Value

Best Effort Service Latency (BESL) – Offset 62

Bset Effort Service Latency.

Bit Range	Default	Access	Field Name and Description
7:4	0h	RW/L	**Default Best Effort Service Latency Deep (DBESLD)** If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESLD field. This is programmed by BIOS based on platform parameters.

Bit Range	Default	Access	Field Name and Description
3:0	0h	RW/L	**Default Best Effort Service Latency (DBESL)** If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESL field. This is programmed by BIOS based on platform parameters.

PCI Power Management Capability ID (PM_CID) – Offset 70

Bit Range	Default	Access	Field Name and Description
7:0	01h	RO	**PCI Power Management Capability ID (PM_CID)** A value of 01h indicates that this is a PCI Power Management capabilities field.

Next Item Pointer #1 (PM_NEXT) – Offset 71

This register is modified and maintained by BIOS

Bit Range	Default	Access	Field Name and Description
7:0	80h	RW/L	**Next Item Pointer #1 (PM_NEXT)** This register defaults to 80h, which indicates that the next capability registers begin at configuration offset 80h. This register is writable when the Access Control bit is set to '0'. This allows BIOS to effectively hide the next capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Values of: 80h implies next capability is MSI 00h implies that MSI capability is hidden. Note: This value is never expected to be programmed.

Power Management Capabilities (PM_CAP) – Offset 72

Normally, this register is read-only to report capabilities to the power management software. In order to report different power management capabilities depending on the system in which the Intel PCH is used, the write access to this register is controlled by the Access Control bit (ACCTRL). The value written to this register does not affect the hardware other than changing the value returned during a read.This register is modified and maintained by BIOS

Bit Range	Default	Access	Field Name and Description
15:11	11000b	RW/L	**PME_Support (PME_Support)** This 5-bit field indicates the power states in which the function may assert PME#. The Intel PCH XHC does not support the D1 or D2 states. For all other states, the Intel PCH XHC is capable of generating PME#. Software should never need to modify this field.
10	0b	RW/L	**D2_Support (D2_Support)** The D2 state is not supported.
9	0b	RW/L	**D1_Support (D1_Support)** The D1 state is not supported.
8:6	111b	RW/L	**Aux_Current (Aux_Current)** The Intel PCH XHC reports 375mA maximum Suspend well current required when in the D3cold state. This value can be written by BIOS when a more accurate value is known.
5	0b	RW/L	**DSI (DSI)** The Intel PCH reports 0, indicating that no device-specific initialization is required.
4	-	-	**Reserved**
3	0b	RW/L	**PME Clock (PMEClock)** The Intel PCH reports 0, indicating that no PCI clock is required to generate PME#.
2:0	010b	RW/L	**Version (Version)** The Intel PCH reports 010, indicating that it complies with Revision 1.1 of the PCI Power Management Specification.

Power Management Control/Status (PM_CS) – Offset 74

Bit Range	Default	Access	Field Name and Description
15	0b	RW/1C	**PME_Status (PME_Status)** This bit is set when the Intel PCH XHC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). Writing a 0 has no effect. This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14:13	00b	RO	**Data_Scale (Data_Scale)** The Intel PCH hardwires these bits to 00 because it does not support the associated Data register.
12:9	0h	RO	**Data_Select (Data_Select)** The Intel PCH hardwires these bits to 0000 because it does not support the associated Data register.
8	0b	RW	**PME_En (PME_En)** A 1 enables the Intel PCH XHC to generate an internal PME signal when PME_Status is 1. This bit must be explicitly cleared by the operating system each time it is initially loaded.
7:4	-	-	**Reserved**
3	1b	RO	**No Soft Reset (NSR)** this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.Transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
1:0	00b	RW	**PowerState (PowerState)** This 2-bit field is used both to determine the current power state of XHC function and to set a new power state. The definition of the field values are: 00b - D0 state 11b - D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3hot state, the Intel PCH must not accept accesses to the XHC memory range, but the configuration space must still be accessible.

Message Signaled Interrupt CID (MSI_CID) – Offset 80

Bit Range	Default	Access	Field Name and Description
7:0	05h	RO	**Capability ID (CID)** Indicates that this is an MSI capability

Next item pointer (MSI_NEXT) – Offset 81

Bit Range	Default	Access	Field Name and Description
7:0	00h	RW/L	**Next Pointer (NEXT)** Indicates that this is the last item on the capability list

Message Signaled Interrupt Message Control (MSI_MCTL) – Offset 82

Bit Range	Default	Access	Field Name and Description
14:9	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
8	0b	RO	**Per-Vector Masking Capable (PVM)** Specifies whether controller supports MSI per vector masking. Not supported
7	1b	RO	**64 Bit Address Capable (C64)** Specifies whether capable of generating 64-bit messages. This device is 64-bit capable.
6:4	0h	RW	**Multiple Message Enable (MME)** Indicates the number of messages the controller should assert. This device supports multiple message MSI.
3:1	011b	RO	**Multiple Message Capable (MMC)** Indicates the number of messages the controller wishes to assert.This field must be set by HW to reflect the number of Interrupters supported. Encoding number of Vectors requested (number of Interrupters) 000 1 001 2 010 4 011 8 100 16 101 32 110-111 Reserved

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**MSI Enable (MSIE)** If set to 1, MSI is enabled and the traditional interrupt pins are not used to generate interrupts. If cleared to 0, MSI operation is disabled and the traditional interrupt pins are used.

Message Signaled Interrupt Message Address (MSI_MAD) – Offset 84

Bit Range	Default	Access	Field Name and Description
31:2	0000000 0h	RW	**Addr (Addr)** Lower DW of system specified message address, always DWORD aligned
1:0	-	-	**Reserved**

Message Signaled Interrupt Upper Address (MSI_MUAD) – Offset 88

Bit Range	Default	Access	Field Name and Description
31:0	0000000 0h	RW	**Upper Addr (UpperAddr)** Upper DW of system specified message address.

Message Signaled Interrupt Message Data (MSI_MD) – Offset 8c

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW	**Data (Data)** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD(15:0)) during the data phase of the MSI memory write transaction. The Multiple Message Enable field (bits 6-4 of the Message Control register) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010 indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000, the function is not permitted to modify the message data.

Power Control Enable (PCE_REG) – Offset a2

Power Control Enable

Bit Range	Default	Access	Field Name and Description
14:4	-	-	**Reserved**
3	1h	RW	**Sleep Enable (SE)** 0: xHCI will never asset Sleep 1: xHCI may assert Sleep during PG'ing. Note that some platforms may default this bit to '0', others to '1'.
2	0h	RW	**D3 HOT ENABLE (D3_HOT_EN)** 0: xHCI will not power gate when idle 1: xHCI will power gate when idle
1:0	-	-	**Reserved**

High Speed Configuration 2 (HSCFG2) – Offset a4

Bit Range	Default	Access	Field Name and Description
30:19	-	-	**Reserved**
18	0h	RW	**PORT1_HOST_MODE_OVERRIDE (PORT1_HOST_MODE_OVERRIDE)** When set, this bit causes the Host_Device mux on port 1 to be forced into the Host mode.
17:16	0h	RW	**eUSB2SEL (eUSB2SEL)** The two bits are associate with USB2 ports 1 - bit 16 and 2 - bit 2 0: Port is mapped to USB2 1: Port is mapped to eUSB2
15	0h	RW	**HS ASYNC Active IN Mask (HSAAIM)** Determines if the Async Active will mask/ignore IN EP s. 0 HS ASYNC Active will include IN EP s. 1 HS ASYNC Active will mask/ignore IN EP s.
14	0h	RW	**HS OUT ASYNC Active Polling EP Mask (HSOAAPEPM)** Determines if the Async Active for OUT HS/FS/LS masks/ignores EP s that are polling/PINGing (HS) due to NAK. 0 HS OUT ASYNC Active will include EP s that are polling. 1 HS OUT ASYNC Active will mask/ignore EP s that are polling.
13	1h	RW	**HS IN ASYNC Active Polling EP Mask (HSIAAPEPM)** Determines if the Async Active for IN HS/FS/LS masks/ignores EP s that are polling due to NAK. 0 HS IN ASYNC Active will include EP s that are polling. 1 HS IN ASYNC Active will mask/ignore EP s that are polling.

Bit Range	Default	Access	Field Name and Description
12:11	0h	RW	**HS INTR IN Periodic Active Policy Control (HSIIPAPC)** Controls how the HS INTR IN periodic active is used to generate the global periodic active. This will determine how the smallest service interval among active EP s and number of active EP s are used. 0 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold OR Numb of EP Threshold values meet the requirement. 1 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold AND Numb of EP Threshold values meet the requirement. 2 Always allow HS INTR EP s to be used in the generation of the global Periodic Active indication. 3 Never allow HS INTR EP s to be used in the generation of the global Periodic Active indicaiton
10:4	00h	RW	**HS INTR IN Periodic Active Num of EP Threshold (HSIIPANEPT)** Defines the threshold used to determine if Periodic Acive may include HS/FS/LS INTR IN EP active indication. If there are more than NumEPThreshold active HS/FS/LS INTR EP s then they may be included as part of the periodic active generation.
3:0	0h	RW	**HS INTR IN Periodic Active Service Interval Threshold (HSIIPASIT)** Defines the Service Interval threshold used to determine if Periodic Acive will include HS/FS/LS INTR IN EP active indication. If there are any active HS/FS/LS INTR EP s with a service interval less than or equal to this threshold then they may be included as part of the periodic active generation.

Super Speed Configuration 1 (SSCFG1) – Offset a8

This register is modified and maintained by BIOS

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30:15	-	-	**Reserved**
14	0b	RW	**MODPHY Power Gate Enable for U2 (MPHYPGEU2)** This bit controls whether xHC will allow PHY power gating or not when a port is in U2 state. Note that this single bit controls all ports of xHC. 0b xHC shall not initiate Power Gate Request when in U2 1b xHC is enabled to initiate Power Gate Request when in U2 if power gating conditions are met.
13:0	-	-	**Reserved**

XHCI USB3 Overcurrent Pin Mapping N (U3OCM) – Offset d0

Address Offset: D0-D3h, ... (D0h+(NumOC-1)*4) to (D3h+(NumOC–1)*4)

The RW/L property of this register is controlled by OCCFGDONE bit.

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:0	00h	RW/L	**OC Mapping (OCM)** USB 3.1 Port assignment, when Set to 1 Bit 0 maps to USB 3.1 port 1 Bit 1 maps to USB 3.1 port 2 Bit N maps to USB 3.1 port N+1. The total number of USB 3.1 ports will depend on the SKU.

XHCI USB2 Overcurrent Pin Mapping N (U2OCM) – Offset b0

Address Offset: B0-B3h, ... (B0h+(NumOC-1)*4) to (B3h+(NumOC–1)*4)

The RW/L property of this register is controlled by OCCFDONE bit.

Each OC pin can be assigned to one or more of up to 32 Standard USB2 ports.

Each DWord maps one OC pin across upto 32 USB2 ports.

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0h	RW/L	**OC Mapping (OCM)** USB 2.0 Port assignment, set to 1 to map port, Bit 0 maps to USB 2.0 port 1 Bit 1 maps to USB 2.0 port 2 Bit N maps to USB 2.0 port N+1. The total number of USB 2.0 ports will depend on the SKU. Depending on the SKU, the upper bits may not apply. Note:The USB-R port which is the mostsignificant USB 2.0 port does not have an OC pin. Thus the OC assignmentfor the USB-R port is ignored.

xHCI Memory Mapped Registers

Summary of Bus:, Device:, Function: (MEM)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	1	Capability Registers Length (CAPLENGTH)	80h
2h	2	Host Controller Interface Version Number (HCIVERSION)	100h
4h	4	Structural Parameters 1 (HCSPARAMS1)	1A000840h
8h	4	Structural Parameters 2 (HCSPARAMS2)	14200054h
ch	4	Structural Parameters 3 (HCSPARAMS3)	40001h
10h	4	Capability Parameters (HCCPARAMS)	200077C1h
14h	4	Doorbell Offset (DBOFF)	3000h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
80ech	4	SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)	18000000h
80f0h	4	USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)	310803A0h
80fch	4	USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)	8003h
8140h	4	Power Scheduler Control-0 (PWR_SCHED_CTRL0)	A019132h
8144h	4	Power Scheduler Control-2 (PWR_SCHED_CTRL2)	33Fh
8154h	4	AUX Power Management Control (AUX_CTRL_REG2)	1390206h
8164h	4	USB2 PHY Power Management Control (USB2_PHY_PMC)	FCh
18h	4	Runtime Register Space Offset (RTSOFF)	2000h
80h	4	USB Command (USBCMD)	0h
84h	4	USB Status (USBSTS)	1h
88h	4	Page Size (PAGESIZE)	1h
94h	4	Device Notification Control (DNCTRL)	0h
98h	4	Command Ring Low (CRCR_LO)	0h
9ch	4	Command Ring High (CRCR_HI)	0h
816ch	4	xHCI Aux Clock Control Register (XHCI_AUX_CCR)	400h
8174h	4	xHC Latency Tolerance Parameters - LTV Control (XLTP_LTV1)	40047Dh
817ch	4	xHC Latency Tolerance Parameters - High Idle Time Control (XLTP_HITC)	0h
8180h	4	xHC Latency Tolerance Parameters - Medium Idle Time Control (XLTP_MITC)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8184h	4	xHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)	0h
8198h	4	PDDIS_REG (PDDIS - xHCI Pull Down Disable Control)	0h
81b8h	4	LFPSONCOUNT_REG (LFPSONCOUNT_REG)	20C8h
b0h	4	Device Context Base Address Array Pointer Low (DCBAAP_LO)	0h
b4h	4	Device Context Base Address Array Pointer High (DCBAAP_HI)	0h
480h	4	Port N Status and Control USB2 (PORTSCN)	2A0h
484h	4	Port Power Management Status and Control USB2 (PORTPMSCN)	0h
48ch	4	Port N Hardware LPM Control Register (PORTHLPMCN)	0h
81c4h	4	USB2 PM Control (USB2PMCTRL_REG)	0h
846ch	4	USB Legacy Support Capability (USBLEGSUP)	2201h
8470h	4	USB Legacy Support Control Status (USBLEGCTLSTS)	0h
84f4h	4	Port Disable Override capability register (PDO_CAPABILITY)	3C6h
84f8h	4	USB2 Port Disable Override (USB2PDO)	0h
84fch	4	USB3 Port Disable Override (USB3PDO)	0h
8700h	4	Debug Capability ID Register (DCID)	5100Ah
8704h	4	Debug Capability Doorbell Register (DCDB)	0h
8708h	4	Debug Capability Event Ring Segment Table Size Register (DCERSTSZ)	0h
8710h	8	Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8718h	8	Debug Capability Event Ring Dequeue Pointer Register (DCERDP)	0h
8720h	4	Debug Capability Control Register (DCCTRL)	0h
8724h	4	Debug Capability Status Register (DCST)	0h
8728h	4	Debug Capability Port Status and Control Register (DCPORTSC)	80h
8730h	8	Debug Capability Context Pointer Register (DCCP)	0h
8e10h	4	Global Time Sync Capability (GLOBAL_TIME_SYNC_CAP_REG)	12C9h
540h	4	Port Status and Control USB2 (PORTSCXUSB3)	2A0h
544h	4	Port Power Management Status and Control USB2 (PORTPMSCX)	0h
548h	4	USB3 Port X Link Info (PORTLIX)	0h
2000h	4	Microframe Index (RTMFINDEX)	0h
2020h	4	Interrupter x Management (IMANx)	0h
2024h	4	Interrupter x Moderation (IMODx)	FA0h
2028h	4	Event Ring Segment Table Size x (ERSTSZx)	0h
2030h	4	Event Ring Segment Table Base Address Low x (ERSTBA_LOx)	0h
2034h	4	Event Ring Segment Table Base Address High x (ERSTBA_HIx)	0h
2038h	4	Event Ring Dequeue Pointer Low x (ERDP_LOx)	0h
203ch	4	Event Ring Dequeue Pointer High x (ERDP_HIx)	0h
3000h	4	Door Bell x (DBx)	0h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
8000h	4	XECP_SUPP_USB2_0 (XECP_SUPP_USB2_0)	2000802h
8004h	4	XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1)	20425355h
8008h	4	XECP_SUPP_USB2_2 (XECP_SUPP_USB2_2)	30181001h
800ch	4	XECP_SUPP_USB3_3 (XECP_SUPP_USB2_3)	0h
8010h	4	XECP_SUPP_USB2_4 (Full Speed) (XECP_SUPP_USB2_4)	C0021h
8014h	4	XECP_SUPP_USB2_4 (Low Speed) (XECP_SUPP_USB2_5)	5DC0012h
8018h	4	XECP_SUPP_USB2_5 (High Speed) (XECP_SUPP_USB2_6)	1E00023h
8020h	4	XECP_SUPP_USB3_0 (XECP_SUPP_USB3_0)	3011402h
8024h	4	XECP_SUPP_USB3_1 (XECP_SUPP_USB3_1)	20425355h
8028h	4	XECP_SUPP_USB3_2 (XECP_SUPP_USB3_2)	80000A11h
802ch	4	XECP_SUPP_USB3_3 (XECP_SUPP_USB3_3)	0h
8030h	4	XECP_SUPP_USB3_4 (XECP_SUPP_USB3_4 Super Speed)	50134h
8034h	4	XECP_SUPP_USB3_5 (XECP_SUPP_USB3_5 Super Speed Plus)	A0135h
8038h	4	XECP_SUPP_USB3_6 (XECP_SUPP_USB3_6)	4E00126h
803ch	4	XECP_SUPP_USB3_7 (XECP_SUPP_USB3_7)	9C00127h
8040h	4	XECP_SUPP_USB3_8 (XECP_SUPP_USB3_8)	13800128h
8044h	4	XECP_SUPP_USB3_9 (XECP_SUPP_USB3_9)	5B10129h
8094h	4	Host Control Scheduler (HOST_CTRL_SCH_REG)	100h
80a4h	4	Power Management Control (PMCTRL_REG)	2DFF94h

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
80b0h	4	HOST_CTRL_MISC_REG (HOST_CTRL_MISC_REG)	1037Fh
80b4h	4	HOST_CTRL_MISC_REG2 (HOST_CTRL_MISC_REG2)	0h
80b8h	4	SSPE_REG (SSPE_REG)	0h
80e0h	4	AUX Power Management Control (AUX_CTRL_REG1)	8081BCA0h
8e14h	4	Global Time Sync Control (GLOBAL_TIME_SYNC_CTRL_REG)	0h
8e18h	4	Microframe Time (Local Time) (MICROFRAME_TIME_REG)	0h
8e20h	4	Always Running Time (ART) Low (ALWAYS_RUNNING_TIME_LOW)	0h
8e24h	4	Always Running Time (ART) High (ALWAYS_RUNNING_TIME_HIGH)	0h
8e7ch	4	Dublin LFPS Register 4 (HOST_CTRL_SSP_LFPS_REG4)	788000h
8ebch	4	Host Ctrl USB3 Soft Error Count Register 1 (HOST_CTRL_USB3_ERR_COUNT_REG1)	0h

Capability Registers Length (CAPLENGTH) – Offset 0

This register is modified and maintained by BIOS

Bit Range	Default	Access	Field Name and Description
7:0	80h	RW/L	**Capability Registers Length (CAPLENGTH)** This register is used as an offset to add to the Memory Base Register to find the beginning of the Operational Register Space.

Host Controller Interface Version Number (HCIVERSION) – Offset 2

This register is modified and maintained by BIOS

Bit Range	Default	Access	Field Name and Description
15:0	0100h	RW/L	**Host Controller Interface Version Number (HCIVERSION)** This is a two-byte register containing a BCD encoding of the version number of interface that this host controller interface conforms.

Structural Parameters 1 (HCSPARAMS1) – Offset 4

This register is modified and maintained by BIOS

Bit Range	Default	Access	Field Name and Description
31:24	26d	RW/L	**Number of Ports (MaxPorts)** This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Default value = 0Eh
23:19	-	-	**Reserved**
18:8	008h	RW/L	**Number of Interrupters (MaxIntrs)** This field specifies the number of interrupters implemented on this host controller. Each interrupter is allocated to a vector of MSI and controls its generation and moderation.
7:0	40h	RW/L	**Number of Device Slots (MaxSlots)** This field specifies the number of Device Context Structures and Doorbell Array entries this host controller can support. Valid values are in the range of 1 to 255.

Structural Parameters 2 (HCSPARAMS2) – Offset 8

This register is modified and maintained by BIOS

Bit Range	Default	Access	Field Name and Description
31:27	02h	RW/L	**Max Scratchpad Buffers LO (MaxScratchpadBufs)** Indicates the number of Scratchpad Buffers system software shall reserve for the xHC.

Bit Range	Default	Access	Field Name and Description
26	1b	RW/L	**Scratchpad Restore (SPR)** 0 = Indicates the Scratchpad buffer space may be freed and reallocated between power events. 1 = Indicates that the xHC requires the integrity of the Scratchpad buffer space to be maintained across power events.
25:21	01h	RW/L	**Max Scratchpad Buffers HI (MaxScratchpadBufs_HI)**
20:8	-	-	**Reserved**
7:4	5h	RW/L	**Event Ring Segment Table Max (ERSTMax)** This field determines the maximum value supported by the Event Ring Segment Table Base Size registers.
3:0	4h	RW/L	**Isochronous Scheduling Threshold (IST)** This field indicates to system software the minimum distance (in time) that it is required to stay ahead of the xHC while adding TRBs, in order to have the xHC process them at the correct time. The value is specified in the number if frames/ microframes. If bit [3] of IST is cleared to 0b, software can add a TRB no later than IST [2:0] microframes before that TRB is scheduled to be executed. If bit [3] of IST is set to 1b, software can add a TRB no later than IST[2:0] frames before that TRB is scheduled to be executed.

Structural Parameters 3 (HCSPARAMS3) – Offset c

This register is modified and maintained by BIOS

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:16	0004h	RW/L	**U2 Device Exit Latency (U2DEL)** Indicates the worst case latency to transition from U2 to U0. Applies to all root hub ports. The following are permissible values: Value Description 00h Zero 01h Less than 1 µs 02h Less than 2 µs ... 0800h-FFFFh Reserved
15:8	-	-	**Reserved**
7:0	01h	RW/L	**U1 Device Exit Latency (U1DEL)** Worst case latency to transition a root hub Port Link State (PLS) from U1 to U0. Applies to all root hub ports. The following are permissible values: Value Description 00h Zero 01h Less than 1 µs 02h Less than 2 µs ... 0Bh-FFh Reserved

Capability Parameters (HCCPARAMS) – Offset 10

This register is modified and maintained by BIOS

Bit Range	Default	Access	Field Name and Description
31:16	2000h	RW/L	**xHCI Extended Capabilities Pointer (xECP)** This field indicates the existence of a capabilities list. The value of this field indicates a relative offset, in 32-bit words, from Base to the beginning of the first extended capability.
15:12	7h	RW/L	**Maximum Primary Stream Array Size (MaxPSASize)** RW/L. This fields identifies the maximum size Primary Stream Array that the xHC supports. The Primary Stream Array size = 2MaxPSASize+1. Valid MaxPSASize values are 1 to 15.
11	0h	RW/L	**Contiguous Frame ID Capability (CFC)**
10	1h	RW/L	**Stopped EDLTA Capabilty (SEC)** This flag indicates that the host controller implementation Stream Context support a Stopped EDLTA field.
9	1h	RW/L	**Stopped - Short Packet Capability (SPC)** This flag indicates that the host controller implementation is capable of generating a Stopped-Short Packet Completion Code.
8	1b	RW/L	**Parst All Event Data (PAE)**
7	1b	RW/L	**No Secondary SID Support (NSS)** Hardwired to '0' indicating Secondary Stream ID decoding is supported.
6	1b	RW/L	**Latency Tolerance Messaging Capability (LTC)** 0 = Latency Tolerance Messaging is not supported. 1 = Latency Tolerance Messaging is supported
5	0b	RW/L	**Light HC Reset Capability (LHRC)** 0 = Light Host Controller Reset is not supported. 1 = Light Host Controller Reset is supported

Bit Range	Default	Access	Field Name and Description
4	0b	RW/L	**Port Indicators (PIND)** This bit indicates whether the xHC root hub ports support port indicator control. When this bit is a '1', the port status and control registers include a read/writeable field for controlling the state of the port indicator.
3	0b	RW/L	**Port Power Control (PPC)** This bit indicates whether the host controller implementation includes port power control. A '1' in this bit indicates the ports have port power switches. A '0' in this bit indicates the port do not have port power switches.
2	0b	RW/L	**Context Size (CSZ)** If this bit is set to '1', then the xHC uses 64 byte Context data structures. If this bit is cleared to '0', then the xHC uses 32 byte Context data structures.
1	0b	RW/L	**BW Negotiation Capability (BNC)** 0 = Not capable of BW Negotiation. 1 = Capable of BW Negotiation.
0	1b	RW/L	**64-bit Addressing Capability (AC64)** This bit documents the addressing range capability of the xHC. The value of this flag determines whether the xHC has implemented the high order 32- bits of 64-bit register and data structure pointer fields. Values for this flag have the following interpretation: 0 = Supports 32-bit address memory pointers 1 = Supports 64-bit address memory pointers If 32-bit address memory pointers are implemented, the xHC shall ignore the high order 32- bits of 64-bit data structure pointer fields, and system software shall ignore the high order 32- bits of 64- bit xHC registers.

Doorbell Offset (DBOFF) – Offset 14

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
31:2	00000C00h	RO	**Doorbell Array Offset (DBAO)** This field defines the DWord offset of the Doorbell Array base address from the Base (for example, the base address of the xHCI Capability register address space).
1:0	-	-	**Reserved**

SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG) – Offset 80ec

Bit Range	Default	Access	Field Name and Description
31:27	03h	RW	**Force LTSSM State (FORCE_LTSSM_ST)** LTSSM state to be forced This value is for test purpose only.
26	0b	RW	**Direct Link LTSSM State (DL_LTSSM_ST)** 0: Normal operation mode 1: Direct link to a specific state specified by bit 31:27 This bit is for test purpose only. It shall be written 0 in normal operation mode.
25	0b	RW	**Direct Link To U0 (DL_U0)** 0: Normal operation mode 1: Direct link to U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
24:21	0h	RW	**Forced Compliance Pattern (FORCED_CMP_PAT)** Compliance pattern to be forced to enter compliance mode This value is for test purpose only.
20:17	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
16:15	0h	RW	**PHY Low Power Latency (PHY_LP_LAT)** This field defines the latency to drive the PHY to enter low power mode 0: 4 cycles 1: 8 cycles 2: 16 cycles 3: 32 cycles
14:12	0h	RW	**Link Recovery Minimum Time (LR_MIN_TM)** This value defines the minimum time for the link to stay in Recovery.Active other than from U3. The granuity is 128us.
11:9	0h	RW	**Link Polling Minimum Time (LP_MIN_TM)** This value defines the minimum time for the link to stay in Polling.Active and Recovery.Active from U3. The granuity is 128us.
8	0b	RW	**Force Link Accept PM Command (FORCE_LA_PMC)** 0: Normal operation mode 1: Force link to accept power management command
7	0b	RW	**Direct Link Recovery U0 (DL_REC_U0)** 0: Normal operation mode 1: Direct link to Recovery from U0
6	0b	RW	**Link Fast Training Mode (LINK_FTM)** 0: Normal operation mode 1: Link fast training mode This bit should be written 0 in normal operation.
5	0b	RW	**Disable Link Scrambler (DIS_LINK_SCRAM)** 0: Enable link scrambler 1: Disable link scramber

Bit Range	Default	Access	Field Name and Description
4	0b	RW	**Direct Link U3 From U0 (DL_U3_U0)** 0: Normal operation mode 1: Direct link to U3 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
3	0b	RW	**Direct Link U3 From U0 (DL_U2_U0)** 0: Normal operation mode 1: Direct link to U2 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
2	0b	RW	**Direct Link U3 From U0 (DL_U1_U0)** 0: Normal operation mode 1: Direct link to U1 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
1	0b	RW	**Enable Link Loopback Master Mode (EN_LINK_LB_MAST)** 0: Disable link loopback master mode 1: Enable link loopback master mode
0	0b	RW	**Disable Link Compliance Mode (DIS_LINK_CM)** 0: Enable link compliance mode 1: Disable link compliance mode

USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1) – Offset 80f0

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Bit Range	Default	Access	Field Name and Description
31:24	31h	RW	**FS/LS Mode SE0 Disconnect Delay[7:0] (FSLS_SE0_DIS_DEL_7_0)** # of microseconds of SE0 in FS/LS mode to register disconnect had occurred.
23:21	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
20	0h	RW	**L1_EXIT_RECOVERY_MODE (L1_EXIT_RECOVERY_MODE)** Mode for extended L1 Exit recovery delay: 0: 12us 1: 50us
19	1h	RW	**L1_TO_INCR_MODE (L1_TO_INCR_MODE)** Mode select for L1 Timeout increments: 0: time out increments are in 125us 1: L1 Timeout increments are in 256us. Refer to USB2 PORTHLPMC.L1 Timeout in XHCI Spec for additional details
18	-	-	**Reserved**
17	0b	RW	**EN_DETECT_NOMINAL_PKT_EOP (EN_DETECT_NOMINAL_PKT_EOP)** 0: Detect minimal packet EOP. 1: Detect nominal packet EOP.
16	0b	RW	**Disable Chirp Response (DIS_CHIRP_RESPONSE)** 0: Normal 1: Force full speed on host ports (disable chirp response)
15	0b	RW	**Disable 192 Byte Limit Check (DIS_192B_LIM)** 0: Enforce 192 byte limit on complete-split INs. Treat any packet) 192 as babble case. 1: Disable 192 byte limit check.
14	0b	RW	**External Provided FS/LS Disconnect (EXT_FSLS_DIS)** 0: Internal FS/LS Disconnect from linestate(1:0) 1: External provided FS/LS Disconnect from hostdisconnect input

Bit Range	Default	Access	Field Name and Description
13:12	0h	RW	**UTMI Reset Source Select (UTMI_RST_SEL)** Select UTMI Reset Source (FRD UTMI Reset Only) 00: HCReset or Force PHY Reset or internal reset after disconnect/suspend for restart (default) 01,11: UTMI reset = ~UTMI suspendm 10: UTMI reset = ~UTMI suspendm and synchronization to port clk.
11	0b	RW	**Disable HS Disconnect Window (DIS_HS_DIS_WIN)** 0: Enable HS Disconnect Window Function 1: Disable HS Disconnect Window Function
10	0b	RW	**Disable Port Error Detection (DIS_PERR_DET)** 0: Enable Port Error Detection (default) 1: Disable Port Error Detection
9	1b	RW	**Disable Peek Function for ISO-OUT (DIS_PF_IOUT)** 0: Enable Peek function for ISO-OUT (default) 1: Disable Peek function for ISO-OUT
8	1b	RW	**Drive Resume-K FS/LS Serial Interface (DRV_RESK_FSLS_SER)** 0: Drive Resume-K on parallel Interface 1: Drive Resume-K directly on FS/LS Serial Interface (default)
7	1b	RW	**Enable USB2 Drop-Ping (EN_U2_DROP_PING)** 0: Disable Drop-Ping Function in USB2 Protocol (default) 1: Enable Drop-Ping Function in USB2 Protocol
6	0b	RW	**Enable USB2 Force-Ping (EN_U2_FORCE_PING)** 0: Disable Force-Ping Function in USB2 Protocol (default) 1: Enable Force-Ping Function in USB2 Protocol
5	1b	RW	**Enable USB2 Auto-Ping (EN_U2_AUTO_PING)** 0: Disable Auto-Ping Function 1: Enable Auto-Ping Function in USB2 Protocol (default)

Bit Range	Default	Access	Field Name and Description
4	0b	RW	**Disable PHY SuspendM (DIS_PHY_SUSM)** 0: PHY is suspend=U3,U2,disconnect (default) 1: Disable PHY SuspendM in All States
3	0b	RW	**UTMI Internal Clock Gate Disable (UTMI_INT_CG_DIS)** 0: Normal operation (internal clock gated in U2,U3,disconnect) 1: UTMI Internal Clock Gate Disable
2	0b	RW	**Disable PHY SuspendM in Disconnect State (DIS_PSUSM_DS)** 0: PHY is suspendM=0 in Disconnect State (default) 1: Disable PHY SuspendM in Disconnect State
1	0b	RW	**Force PHY Reset (FORCE_PHY_RST)** 0: Normal Operation (default) 1: Force PHY Reset
0	0b	RW	**USB2 Accelerated Simulation Timing (U2_ACC_SIM_TIM)** 0: Normal Operation (default - FPGA/ASIC) 1: USB2 Accelerated Simulation Timing (default - simulation)

USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4) – Offset 80fc

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Bit Range	Default	Access	Field Name and Description
30:22	-	-	**Reserved**
21:9	0040h	RW	**U2 Detect Remote Wake Delay (U2D_RWAKE_DEL)** #of microseconds after detecting U2 remote wake condition to reflect K
8:0	003h	RW	**U2 Entry Ignore Linestate Changes Duration[12:4] (U2_IGN_LS_DUR_12_4)** # of microseconds after entering U2, linestate changes are ignored as bus settles

Power Scheduler Control-0 (PWR_SCHED_CTRL0) – Offset 8140

Bit Range	Default	Access	Field Name and Description
31:24	0ah	RW	**Engine Idle Hysteresis (EIH)** This register controls the min. idle span that has to be observed from the engine idle indicators before the power state flags (xhc_*_idle) will indicate a 1.
23:12	019h	RW	**Backbone PLL Shutdown Advance Wake (BPSAW)** This register controls the time before the next scheduled transaction where the Backbone PLL request will assert. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124)
11:0	132h	RW	**Backbone PLL Shutdown Min. Idle Duration (BPSMID)** The sum of this register plus the Backbone PLL Shutdown Advance Wake form to a Total Idle time. When the next scheduled periodic transaction is after present time + Total Idle, the Backbone PLL request will de-assert, allowing the PLL to shutdwon. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124)

Power Scheduler Control-2 (PWR_SCHED_CTRL2) – Offset 8144

These bit enable by EP type those EPs classes that are considered for determining next periodic active interval for pre-wake of the periodic_active signal. EP classes that are disabled may never be observed in setting of the periodic_active signal.

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9	1b	RW	**HS Interrupt-OUT Alarm (HS_INT_OUT_ALRM)**
8	1b	RW	**HS Interrupt-IN Alarm (HS_INT_IN_ALRM)**

Bit Range	Default	Access	Field Name and Description
7	0b	RW	**SS Interrupt-OUT FC Alarm (SS_INT_OUT_FC_ALRM)**
6	0b	RW	**SS Interrupt-IN Alarm (SS_INT_IN_FC_ALRM)**
5	1b	RW	**SS Interrupt-OUT & not in FC Alarm (SS_INT_OUT_ALRM)**
4	1b	RW	**SS Interrupt-IN & not in FC Alarm (SS_INT_IN_ALRM)**
3	1b	RW	**HS ISO-OUT Alarm (HS_ISO_OUT_ALRM)**
2	1b	RW	**HS ISO-IN Alarm (HS_ISO_IN_ALRM)**
1	1b	RW	**SS ISO-OUT Alarm (SS_ISO_OUT_ALRM)**
0	1b	RW	**SS ISO-IN Alarm (SS_ISO_IN_ALRM)**

AUX Power Management Control (AUX_CTRL_REG2) – Offset 8154

Bit Range	Default	Access	Field Name and Description
30:25	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
24	1b	RW	**Enable L1 exit notification to SNPS PCIe core (EN_L1_EXIT_NOTIF_PCIE)** This bit enables a L1 exit notification to SNPS PCIe core. There is a case where USB ports have waked up and AUX PM module has started the wakeup process. The AUX PM control state got into a wait for P0 state because it needs to wait until PCIe core to signal powerdown state change. Due to the fact that the core is in D3Hot, there is no run_stop bit set such that no internal interrupt will be fired. This causes the LTSSM of PCIe stayed in L1 even though AUX PM has known that it needs an L1 exit. This bit works together with bit21 of this register. 1: enables this feature 0: disables this feature.
23	0b	RW	**DISABLE PLC ON DISCONNECT (DIS_PLC_ON_DISCONNECT)** 1: do not assert PLC for disconnection 0: assert PLC for disconnection
22	0b	RW	**TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2 (TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2)** This bit enables a feature in PCIe core LTSSM to treat IDLE received as TS2 when LTSSM is in wait for TS2 receive state. This is a function requested from PHY where it is possible to not able to receive TS2 without error. 1: treat Logic IDLE as TS2 received when in some PCIe LTSSM state. 0: disable this feature.
21	1b	RW	**Disable p2 overwrite due to the D3HOT where PCIe core enters the L1 (DIS_P2_OVERWRITE_DUE2_D3HOT)** We added a feature where if PCIe core LTSSM enters L1 due to the D3hot, the aux PM control will not start a P2 overwrite function in anticipating for the next L23 enter. 1: disables p2 overwrite due to the D3HOT where PCIe core enters the L1. 0: enables P2 overwrite even if we are in D3Hot.

Bit Range	Default	Access	Field Name and Description
20	1b	RW	**Enable the port to enter U3 automatically when in U1/U2 (ENABLE_AUTO_U3_ENTRY_FROM_U2_U3)** 1: enables the port to enter U3 automatically when in U1/U2 0: disables the port to enter U3 automatically when in U1/U2
19	1b	RW	**No linkdown reset is issue during low power state (DIS_LINKDOWN_RST_DURING_LOW_POWER)** No linkdown reset is issue during low power state
18	0b	RW	**EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0 (EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0)** This bit enables a feature in AUX PM module where if PCIe core LTSSM is in P0 for a duration of time, we will exit the deep sleep state. This is for failure control in case. 1: enables this feature 0: disable this feature
17	0b	RW	**U2_EXIT_LFPS_TIMER_VALUE (U2_EXIT_LFPS_TIMER_VALUE)** This bit selects U2 exit LFPS timer value 0: 320ns 400ns in 25MHz domain 1: 240ns 320ns in 25MHz domain
16	1b	RW	**EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP (EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP)** This bit enables a function that AUX PM module exits from the deep sleep state due to the USB ports wakeup level signal. We have added this feature where USB ports will generated a wakeup level signal to wakeup the AUX PM module if it is in deep sleep state and this level signal will be cleared if the change bits are updated by software. 1: enables this function 0: disables this function which means that a wakeup pulse generated from each USB PortSC event will wake up the AUX PM module from deep sleep if the D3 state is programmed.

Bit Range	Default	Access	Field Name and Description
15:14	0h	RW	**P3_ENTRY_TIMEOUT (P3_ENTRY_TIMEOUT)** This field defines the timeout value to enter P3 mode in U2. 00: 7us 8us 01: 511us 512us 10: disables the timer (0us) 11: disables the timer (0us)
13	0b	RW	**Enable U2 P3 Mode (EN_U2_P3)** 0: Disable U2 P3 mode 1: Enable U2 P3 mode
12:11	0h	RW	**Fine Debug Mode Select (FINE_DM_SEL)**
10	0b	RW	**Enable Low Power State Based Core Clock Gating (EN_LP_CORE_CG)** When set to '1' enable core clock gating based on low power state entered
9	1b	RW	**Disable USB3 Port Status Changed Event (DIS_U3_PORT_SCE)** 0: Enable USB3 port status change event generation if any change bit is not cleared 1: Disable USB3 port status change event generation if any change bit is not cleared Bit 12 default 0
8:4	00h	RW	**Debug Mode Select Register (DEB_MODE_SEL)**
3	0b	RW	**Enable Auto Wakeup Non-IDLE (EN_AWAK_NIDLE)** When set to 1 enables the auto wakeup function when engine has identified non IDLE condition.
2	1b	RW	**Enable PM Control P1 Exit P2 (EN_PMC_P1_EXIT_P2)** When set 1 enables the PM control module to transition to P1 instead of P0 when exit P2.
1	1b	RW	**Enable PCIe PIPE CLK Isolation (EN_PP_CLK_ISOL)** When set to 1 enables the PCIe PIPE CLK to be isolated when main power is removed.

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**Enable P2 Overwrite P1 Allowed Detect (EN_P2OVRP1_ADET)** When set to 1 enables a function that can detect whether or not enable P2 overwrite P1 function. The condition to get to P2 overwrite is when engine is in idle conditions. This means that there is no ISO EP pending.

USB2 PHY Power Management Control (USB2_PHY_PMC) – Offset 8164

Bit Range	Default	Access	Field Name and Description
30:8	-	-	**Reserved**
7	1b	RW	**EN_CMDM_TXRXB (EN_CMDM_TXRXB)** Enable Command Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy
6	1b	RW	**EN_TTE_TXRXB (EN_TTE_TXRXB)** Enable TTE Active indication for Tx/Rx Bias circuit HS Phy PM Policy
5	1b	RW	**EN_IDMA_TXRXB (EN_IDMA_TXRXB)** Enable IDMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
4	1b	RW	**EN_ODMA_TXRXB (EN_ODMA_TXRXB)** Enable ODMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
3	1b	RW	**EN_TRM_TXRXB (EN_TRM_TXRXB)** Enable Transfer Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy
2	1b	RW	**EN_SCH_TXRXB (EN_SCH_TXRXB)** Enable Scheduler Active indication for Tx/Rx Bias circuit HS Phy PM Policy
1	0b	RW	**Enable Rx Bias ckt disable (EN_RXB_CD)** When set enables the Rx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits)
0	0b	RW	**Enable Tx Bias ckt disable (EN_TXB_CD)** When set enables the Tx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits)

Runtime Register Space Offset (RTSOFF) – Offset 18

Bit Range	Default	Access	Field Name and Description
31:5	0000100h	RO	**Runtime Register Space Offset (RTRSO)** This field defines the 32-byte offset of the xHCI Runtime Registers from the Base. That is, Runtime Register Base Address = Base + Runtime Register Set Offset.
4:0	-	-	**Reserved**

USB Command (USBCMD) – Offset 80

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**
11	0b	RW	**Enable U3 MFINDEX Stop (EU3S)** When set to 1b, the xHC may stop the MFINDEX counting action if all Root Hub ports are in the U3, Disconnected, Disabled, or Powered-off state. When cleared to 0b, the xHC may stop the MFINDEX counting action if all Root Hub ports are in the Disconnected, Disabled, or Powered-off state.
10	0b	RW	**Enable Wrap Event (EWE)** When set to 1b, the xHC shall generate a MFINDEX Wrap Event every time the MFINDEX register transitions from 03FFFh to 0. When cleared to 0b, no MFINDEX Wrap Events are generated.
9	0b	RW	**Controller Restore State (CRS)** When set to 1b, MEM_BASE+80h:bit 0= 0b, and MEM_BASE+80h:bit 8 = 1b, the xHC shall perform a Restore State operation and restore its internal state. When set to 1b and MEM_BASE+80h:bit 0= 1b or MEM_BASE+80h:bit 8 = 0b, or when cleared to '0', no Restore State operation shall be performed.

Bit Range	Default	Access	Field Name and Description
8	0b	RW	**Controller Save State (CSS)** When written by software with 1b and MEM_BASE+80h:bit 0=0b, the xHC shall save any internal state that will be restored by a subsequent Restore State operation. When written by software with 1b and MEM_BASE+80h:bit 0= 1b, or written with '0', no Save State operation shall be performed.
7	0b	RW	**Light Host Controller Reset (LHCRST)** If the Light HC Reset Capability (LHRC) bit (MEM_BASE=10h:bit 5) is 1b, then setting this bit to 1b allows the driver to reset the xHC without affecting the state of the ports. A system software read of this bit as 0b indicates the Light Host Controller Reset has completed and it is safe for software to re-initialize the xHC. A software read of this bit as a 1b indicates the Light Host Controller Reset has not yet completed.
6:4	-	-	**Reserved**
3	0b	RW	**Host System Error Enable (HSEE)** When this bit is set to 1b, and the HSE bit (MEM_BASE+84h:bit 2) is set to 1b, the xHC shall assert out-of-band error signaling to the host. The signaling is acknowledged by software clearing the HSE bit.
2	0b	RW	**Interrupter Enable (INTE)** This control bit is used by software to reset the host controller. When software sets this bit to 1b, the Host Controller resets its internal pipelines, timers, counters, state machines, and so forth, to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values.
1	0b	RW	**Host Controller Reset (HCRST)** This control bit is used by software to reset the host controller. When software sets this bit to 1b, the Host Controller resets its internal pipelines, timers, counters, state machines, and so forth, to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values.

Bit Range	Default	Access	Field Name and Description
0	0b	RW	**Run/Stop (RS)** When set to 1b, the xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to 1b. When this bit is cleared to 0b, the xHC completes the current and any actively pipelined transactions on the USB and then halts. The xHC shall halt within 16 microframes after software clears the Run/ Stop bit. The HCHalted (HCH) bit (MEM_BASE+84h:bit 0) indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. Software shall not write a '1' to this flag unless the xHC is in the Halted state (that is, HCH in the USBSTS register is '1'); doing so will yield undefined results. Note: Software shall halt all of the EndPoints before clearing this bit. Note: Software shall halt all of the EndPoints before clearing this bit.

USB Status (USBSTS) – Offset 84

This register indicates pending interrupts and various states of the Host controller. The status resulting from a transaction on the serial bus is not indicated in this register. See the Interrupts description in section 4 of the xHCI specification for additional information concerning interrupt conditions.

Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 has no effect.

Bit Range	Default	Access	Field Name and Description
30:13	-	-	**Reserved**
12	0b	RO	**Host Controller Error (HCE)** This flag shall be set to indicate that an internal error condition has been detected which requires software to reset and re-initialize the xHC. 0 = No internal xHC error conditions exist. 1 = Internal xHC error condition exists.
11	0b	RO	**Controller Not Ready (CNR)** 0 = Ready 1 = Not Ready Software shall not write any Doorbell or Operational register of the xHC, other than the USBSTS register, until CNR = 0b. This flag is set by the xHC after a Hardware Reset and cleared when the xHC is ready to begin accepting register writes. This flag shall remain cleared (0b) until the next Chip Hardware Reset.

Bit Range	Default	Access	Field Name and Description
10	0b	RW/1C	**Save/Restore Error (SRE)** If an error occurs during a Save or Restore operation this bit shall be set to 1b. This bit shall be cleared to 0b when a Save or Restore operation is initiated or when written with 1b.
9	0b	RO	**Restore State Status (RSS)** When the Controller Restore State (CRS) flag in the USB_CMDregister is written with 1b this bit shall be set to 1b and remain set while the xHC restores its internalstate. Note: When the Restore State operation is complete, this bit shall be cleared to 0b.
8	0b	RO	**Save State Status (SSS)**
7:5	-	-	**Reserved**
4	0b	RW/1C	**Port Change Detect (PCD)** This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the xHC, this bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, overcurrent change, enable/ disable change and connect status change). Regardless of the implementation, when this bit is readable (that is, in the D0 state), it must provide a valid view of the Port Status registers. 0 = No change bit transition from a 0 to 1 or No Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port. 1 = The Host controller sets this bit to 1 when any port for which the Port Owner bit is set to 0 has a change bit transition from a 0 to 1 or a Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port.
3	0b	RW/1C	**Event Interrupt (EINT)** The xHC sets this bit to 1b when the Interrupt Pending (IP) bit of any Interrupter is transitions from 0b to 1b. Software that uses EINT shall clear it prior to clearing any IP flags. A race condition will occur if software clears the IP flags then clears the EINT flag, and between the operations another IP ‘0’ to '1' transition occurs. In this case the new IP transition will be lost.

Bit Range	Default	Access	Field Name and Description
2	0b	RW/1C	**Host System Error (HSE)** The xHC sets this bit to 1b when a serious error is detected, either internal to the xHC or during a host system access involving the xHC module. Conditions that set this bit to '1' include PCI Parity error, PCI Master Abort, and PCI Target Abort. When this error occurs, the xHC clears the Run/Stop (R/S) bit in the USB_CMD register to prevent further execution of the scheduled TDs. If the HSEE bit in the USB_CMD register is 1b, the xHC shall also assert out-ofband error signaling to the host.
1	-	-	**Reserved**
0	1b	RO	**HCHalted (HCH)** This bit is a '0' whenever the Run/Stop (R/S) bit is set to 1b. The xHC sets this bit to 1b after it has stopped executing as a result of the Run/Stop (R/S) bit being cleared to 0b, either by software or by the xHC hardware (for example, internal error). If this bit is set to1b, then SOFs, microSOFs, or Isochronous Timestamp Packets (ITP) shall not be generated by the xHC.

Page Size (PAGESIZE) – Offset 88

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0001h	RO	**Page Size (PAGESIZE)** Hardwired to 1h to indicate support for 4 Kbyte page sizes.

Device Notification Control (DNCTRL) – Offset 94

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
15:0	0000h	RW	**Notification Enable (N0_N15)** When a Notification Enable bit is set, a Device Notification Event will be generated when a Device Notification Transaction Packet is received with the matching value in the Notification Type field. For example, setting N1 to '1' enables Device Notification Event generation if a Device Notification TP is received with its Notification Type field set to '1' (FUNCTION_WAKE), and so on

Command Ring Low (CRCR_LO) – Offset 98

Bit Range	Default	Access	Field Name and Description
31:6	0000000h	WO	**Command Ring Pointer (CRP)** This field defines low order bits of the initial value of the 64-bitCommand Ring Dequeue Pointer. Notes: 1. Writes to this field are ignored when Command Ring Running bit (CRR) = 1b. 2. If the CRCR register is written while the Command Ring is stopped (CRR = 0b), the value ofthis field shall be used to fetch the first Command TRB the next time the Host ControllerDoorbell register is written with the DB Reason field set to Host Controller Command. 3. If the CRCR register is not written while the Command Ring is stopped (CRR = 0b), then theCommand Ring shall begin fetching Command TRBs at the current value of the internal xHCCommand Ring Dequeue Pointer. 4. Reading this field always returns 0b.
5:4	-	-	**Reserved**
3	0b	RO	**Command Ring Running (CRR)** This bit is set to 1b if the Run/Stop (R/S) bit is 1b and theHost Controller Doorbell register is written with the DB Reason field set to Host ControllerCommand. It is cleared to 0b when the Command Ring is stopped after writing a 1b to theCommand Stop (CS) or Command Abort (CA) bits, or if the R/S bit is cleared to 0b.

Bit Range	Default	Access	Field Name and Description
2	0b	WO	**Command Abort (CA)** Writing a 1b to this bit shall immediately terminate the currentlyexecuting command, stop the Command Ring, and generate a Command Completion Event with theCompletion Code set to Command Ring Stopped. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Commandshall restart the Command Ring operation. Notes: 1. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = 0b. 2. Reading this bit always returns 0b.
1	0b	WO	**Command Stop (CS)** Writing a 1b to this bit shall stop the operation of the Command Ringafter the completion of the currently executing command, and generate a Command CompletionEvent with the Completion Code set to Command Ring Stopped and the Command TRB Pointer setto the current value of the Command Ring Dequeue Pointer. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Commandshall restart the Command Ring operation. Notes: 1. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) bit = 0b. 2. Reading this bit always returns 0b.
0	0b	WO	**Ring Cycle State (RCS)** This bit identifies the value of the xHC Consumer Cycle State (CCS)flag for the TRB referenced by the Command Ring Pointer. Notes: 1. Writes to this bit are ignored when the Command Ring Running (CRR) bit = 1b. 2. If the CRCR register is written while the Command Ring is stopped (CCR = 0b), then the valueof this flag shall be used to fetch the first Command TRB the next time the Host ControllerDoorbell register is written with the DB Reason field set to Host Controller Command. 3. If the CRCR register is not written while the Command Ring is stopped (CCR = 0b), then theCommand Ring will begin fetching Command TRBs using the current value of the internalCommand Ring CCS flag. 4. Reading this flag always returns 0b.

Command Ring High (CRCR_HI) – Offset 9c

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	WO	**Command Ring Pointer (CRP)** Command Ring Pointer—R/W. This field defines high order bits of the initial value of the 64-bitCommand Ring Dequeue Pointer. Notes: 1. Writes to this field are ignored when Command Ring Running bit (CRR) = 1b. 2. If the CRCR register is written while the Command Ring is stopped (CRR = 0b), the value ofthis field shall be used to fetch the first Command TRB the next time the Host ControllerDoorbell register is written with the DB Reason field set to Host Controller Command. 3. If the CRCR register is not written while the Command Ring is stopped (CRR = 0b), then theCommand Ring shall begin fetching Command TRBs at the current value of the internal xHCCommand Ring Dequeue Pointer. 4. Reading this field always returns 0b.

xHCI Aux Clock Control Register (XHCI_AUX_CCR) – Offset 816c

Bit Range	Default	Access	Field Name and Description
30:20	-	-	**Reserved**
19	0b	RW	**USB3 Partition Engine/Link trunk gating Enable (PARUSB3_ENG_GEN)** When set to 1 enables gating of the SOSC trunk to the XHCI engine and link in the PARUSB3 partition.
18	0b	RW	**USB3 Partition Frame Timer trunk gating Enable (PARUSB3_LINK_GEN)** When set to 1 enables gating of the SOSC trunk to the Frame timer in the PARUSB3 partition.
17	0b	RW	**USB2 link partition clock gating enable (PARUSB2_CLK_GEN)** When set to 1 enables gating of the SOSC trunk to the USB2 link and Phy logic in the PARUSB2 partition.

Bit Range	Default	Access	Field Name and Description
16	0b	RW	**USB2/USHIP 12.5 MHz partition clock gating enable (USHIP_PCGEN)** When set to 1 enables gating of the 12.5 MHz SOSC trunk to the USB2 and USHIP logic in the PARUSB2 partition.
15	-	-	**Reserved**
14	0b	RW	**USB3 Port Aux/Core clock gating enable (USB3_AC_CGE)** When set, allows the aux_cclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating being enabled.
13:12	0h	RW	**Rx Detect Timer when port Aux Clock is Gated (RX_DT_ACG)** This field defines the value of the timer used to perform Rx Detect when port Aux Clock has been gated. 0x0: 100ms 0x1: 12ms Others: Reserved Note: This timer shall use the Fast Training Timer Tick (about 1us tick) for simulation purposes. For Fast Training mode, the above timeouts will become about 11us and about 100us, +/- implementation uncertainty, respectively.

Bit Range	Default	Access	Field Name and Description
11:8	4h	RW	**U2 Residency Before ModPHY Clock Gating (U2R_BM_CG)** Before gating ModPHY Aux clock, Host Controller shall wait for this time in U2. This time is meant to ensure that the attached device has entered U2 as well. 0x0: 1us 0x1: 128us 0x2: 256us 0x3: 512us 0x4: 640us 0x5: 768us 0x6: 896us 0x7: 1024us Others: Reserved Note: This counter shall start counting once pipe has entered PS3 state in response to link in U2.
7	0h	RW	**Frame Timer Clock Gating Ports in U2 Enable (FTCGPU2E)** This bit, when set, allows Host Controller to gate the clock to the Frame Timer when ports are in U2.
6	0b	RW	**USB2 port clock throttle enable (USB2_PC_TE)** When set, allows the Aux clock into the USB2 ports to be throttled when conditions allow.
5	0b	RW	**XHCI Engine Aux clock gating enable (XHCI_AC_GE)** When set, allows the aux clock into the XHCI engine to be gated when idle.Usage of this bit is further qualified with xHC Dynamic Clock Gating being enabled.
4	0b	RW	**XHCI Aux PM block clock gating enable (XHCI_APMB_CGE)** When set, allows the aux clock into the Aux PM block to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating being enabled.
3	0b	RW	**USB3 Aux Clock Trunk Gating Enable (USB3_AC_TGE)** When set, allows Aux Clock Trunk feeding to USB3.0 ports to be gated when port Aux clock is gated at all USB3.0 ports and all USB3.0 modPHY instances.Usage of this bit is further qualified with xHC Dynamic Clock Gating being enabled.

Bit Range	Default	Access	Field Name and Description
2	-	-	**Reserved**
1	0b	RW	**ModPHY port Aux clock gating enable in U2 (MPP_AC_GEU2)** When set, allows the aux clock into the ModPhy to be gated when Link is in U2 and pipe has been in PS3 for at least the time defined by U2 Residency Before ModPHY Clock Gating field.Usage of this bit is further qualified with xHC Dynamic Clock Gating being enabled.
0	0b	RW	**ModPHY port Aux clock gating enable in Disconnected, U3 or Disabled (MPP_AC_GE_DDU3)** When set, allows the aux clock into the ModPHY to be gated when Link is in Disconnected, U3 or Disabled state.Usage of this bit is further qualified with xHC Dynamic Clock Gating being enabled.

xHC Latency Tolerance Parameters - LTV Control (XLTP_LTV1) – Offset 8174

Bit Range	Default	Access	Field Name and Description
31	0b	RW	**Disable scheduler direct transition from IDLE to NO requirement (DIS_SDT_IDL_NR)** 0: (default) allow scheduler direct transition from IDLE to NO requirement 1: Disable scheduler direct transition from IDLE to NO requirement
30:26	-	-	**Reserved**
25	0b	RW	**XHCI LTR Transition Policy (XLTRTP)** When '0', LTR messaging state machine transitions from High, Medium, or Low LTR states to Active state upon the Alarm Timer timeout and stays in Active until the next service boundary. When '1', the LTR messaging state machine transitions through High-Med-Low to Active states assuming enough latency is available for each transition.
24	0b	RW	**XHCI LTR Enable (XLTRE)** This bit must be set to enable LTV messaging from XHCI to the PMC.

Bit Range	Default	Access	Field Name and Description
23:12	400h	RW	**Periodic Active LTV (PA_LTV)** Bits[23:22] Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 Bits[21:12] Latency Value (ns). Defaults to 0 micro seconds
11:0	47Dh	RW	**USB2 Port L0 LTV (USB2_PL0_LTV)** Bits[11:10] Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 Bits[9:0] Latency Value (ns). Defaults to 128 Micro Seconds

xHC Latency Tolerance Parameters - High Idle Time Control (XLTP_HITC) – Offset 817c

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
28:16	0000h	RW	**Minimum High Idle Time (MHIT)** LTR value can be indicated. This value must be larger than HIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	-	-	**Reserved**
12:0	0000h	RW	**High Idle Wake Latency (HIWL)** This is the latency to access memory from the High Idle Latency state. This value must be larger than MIWL and LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

xHC Latency Tolerance Parameters - Medium Idle Time Control (XLTP_MITC) – Offset 8180

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
28:16	0000h	RW	**Minimum Medium Idle Time (MMIT)** LTR value can be indicated. This value must be larger than MIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	-	-	**Reserved**
12:0	0000h	RW	**Medium Idle Wake Latency (MIWL)** This is the latency to access memory from the Medium Idle Latency state. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

xHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC) – Offset 8184

Bit Range	Default	Access	Field Name and Description
30:29	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
28:16	0000h	RW	**Minimum Low Idle Time (MLIT)** LTR value can be indicated. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	-	-	**Reserved**
12:0	0000h	RW	**Low Idle Wake Latency (LIWL)** This is the latency to access memory from the Medium Idle Latency state. 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

PDDIS_REG (PDDIS - xHCI Pull Down Disable Control) – Offset 8198

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
15:0	0h	RW	**PDDISEN (PDDISEN)** Allow the USB Pulldown to be disabled Each bit corresponds to a USB2 port indexed by the bit number (zero based). Bit 0 = USB2 port 1 Bit 1 = USB2 port 2 Etc. When set, allow the pulldown on D+ or D- (as appropriate) to be disabled when the port is connected and in L2.

LFPSONCOUNT_REG (LFPSONCOUNT_REG) – Offset 81b8

Bit Range	Default	Access	Field Name and Description
30:18	-	-	**Reserved**
17:16	0h	RW	**U2P3 LFPS Periodic Sampling Control (XU2P3LPSC)** This field controls the OFF time for the LFPS periodic sampling for SS and SSIC ports in U2P3. If LFPSPM for a port is 1, it will override the OFF time and LFPS receiver will remain OFF permanently. For Fast Sim mode, 500us will be equivalent to 5us. 0x0 Polling Disable. (RXDET Polling will become 100ms.) 0x1 500us OFF Time 0x2 1ms OFF Time 0x3 1.5ms OFF Time
15:10	08h	RW	**XLFPSONCNTSSIC (XLFPSONCNTSSIC)** This time would describe the number of clocks SSIC LFPS will remain ON. SSIC LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 8.
9:0	0C8h	RW	**XLFPSONCNTSS (XLFPSONCNTSS)** This time would describe the number of clocks LFPS will remain ON. LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 200.

Device Context Base Address Array Pointer Low (DCBAAP_LO) – Offset b0

Bit Range	Default	Access	Field Name and Description
31:6	0000000h	RW	**Device Context Base Address Array Pointer (DCBAAP)** This field defines low order bits of the 64-bitbase address of the Device Context Pointer Array table (a table of address pointers that referenceDevice Context structures for the devices attached to the host.
5:0	-	-	**Reserved**

Device Context Base Address Array Pointer High (DCBAAP_HI) – Offset b4

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Device Context Base Address Array Pointer (DCBAAP)** This field defines high order bits of the 64-bitbase address of the Device Context Pointer Array table (a table of address pointers that referenceDevice Context structures for the devices attached to the host.)

Port N Status and Control USB2 (PORTSCN) – Offset 480

Note that this USB2 Port Status and Control register is available at the following offsets for all applicable USB2 ports:

USB2 Port 1: 480h

USB2 Port 2: 490h

USB2 Port 3: 4A0h

.....

USB2 Port 9: 500h

USB2 Port 10: 510h

Bit Range	Default	Access	Field Name and Description
31	0b	RW/1S	**Warm Port Reset (WPR)** When software sets this bit to 1b, the Warm Reset sequence is enabled
30	0b	RW/L	**Device Removable (DR)** This bit indicates if this port has a removable device. 0 = Device is removable. 1 = Device is non-removable.
29:28	-	-	**Reserved**
27	0b	RW/P	**Wake on Over-current Enable (WOE)** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to overcurrent conditions as system wake-up events.
26	0b	RW/P	**Wake on Disconnect Enable (WDE)** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device disconnects as system wake-up events.
25	0b	RW/P	**Wake on Connect Enable (WCE)** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device connects as system wake-up events.
24	0b	RO	**Cold Attach Status (CAS)** This bit indicates that far-end terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable to advance to the Enabled state. Software shall clear this bit by writing a 1b to the WPR bit or the xHC shall clear this bit if the CSS bit transitions to 1.
23	0b	RW/1C	**Port Config Error Change (CEC)** Note: This register is sticky.

Bit Range	Default	Access	Field Name and Description
22	0b	RW/1C	**Port Link State Change (PLC)** 0 = No change 1 = Link Status Change This flag is set to '1' due to the following Port Link State (PLS) transitions:
21	0b	RW/1C	**Port Reset Change (PRC)** This flag is set to '1' due a '1' to '0' transition of Port Reset (PR), for example, when any reset processing on this port is complete. 0 = No change 1 = Reset Complete
20	0b	RW/1C	**Over-current Change (OCC)** The functionality of this bit is not dependent upon the port owner. Software clears this bit by writing a 1 to it. 0 = No change. (Default) 1 = There is a change to Overcurrent Active.
19	0b	RW/1C	**Warm Port Reset Change (WRC)** This bit is set when Warm Reset processing on this port completes. 0 = No change. (Default) 1 = Warm reset complete
18	0b	RW/1C	**Port Enabled Disabled Change (PEC)** 0 = No change. (Default) 1 = There is a change to PED bit.

Bit Range	Default	Access	Field Name and Description
17	0b	RW/1C	**Connect Status Change (CSC)** R/WC. This flag indicates a change has occurred in the port's Current Connect Status (CCS) or Cold Attach Status (CAS) bits. 0 = No change. (Default) 1 = There is a change to the CCS or CAS bit. The xHC sets this bit to 1b for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (that is, the bit will remain 1b).
16	0b	RW	**Port Link State Write Strobe (LWS)** 0 = When 0b, write data in PLS field is ignored. (Default) 1 = When this bit is set to 1b on a write reference to this register, this flag enables writes to the PLS field. Reads to this bit return '0'.
15:14	0h	RW/P	**Port Indicator Control (PIC)** Note: This register is sticky.
13:10	0h	RO	**Port Speed (PortSpeed)** A device attached to this port operates at a speed defined by the following codes: Value Speed 0001b Full-speed 0010b Low speed 0011b Highspeed All other values reserved. Refer to the eXtensible Host Controller Interface for Universal Serial Bus Specification for additional details.
9	1b	RW/P	**Port Power (PP)** Default value of 1. 0 = This port is in the powered-off state 1 = This port is in the powered-on state. This indicates that the port does have power.
8:5	5h	RW/P	**Port Link State (PLS)**

Bit Range	Default	Access	Field Name and Description
			This field is used to power manage the port and reflects its currentlink state.When the port is in the Enabled state, system software may set the link U-state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write Value and Description 0: The link shall transition to a U0 state from any of the U-states. 2: USB 2.0 ports only. The link should transition to the U2 State. 3: The link shall transition to a U3 state from any of the U-states. This action selectively suspends the device connected to this port. While the Port LinkState = U3, the hub does not propagate downstream-directed traffic to this port, but the hub will respond to resume signaling from the port. 5: USB 3.0 ports only. If the port is in the Disabled state (PLS = Disabled, PP= 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 15: USB 2.0 ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3Exit substate, else ignored. All other values are ignored Read Value and Definition 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspended) 4: Link is in the Disabled State 5:Link is in the RxDetect State 6:Link is in the Inactive State 7: Link is in the Polling State 8:Link is in the Recovery State 9: Link is in the Hot Reset State 10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12–14: Reserved

Bit Range	Default	Access	Field Name and Description
			15: Link is in the Resume State
4	0b	RW/1S	**Port Reset (PR)** When software writes a 1 to this bit (from a 0), the bus reset sequence as 1=port in reset 0=port not in reset
3	0b	RW	**Over-current Active (OCA)** 0 = This port does not have an overcurrent condition. (Default) 1 = This port currently has an overcurrent condition. This bit will automatically transition from 1 to 0 when the overcurrent condition is removed. The PCH automatically disables the port when the overcurrent active bit is 1.
2	-	-	**Reserved**
1	0b	RW/1C	**Port Enabled Disabled (PED)** Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a 1 to this bit. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. The bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. 0=disable 1=enable(default)
0	0b	RW	**Current Connect Status (CCS)** This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 0=no device is present 1=device is present on port.

Port Power Management Status and Control USB2 (PORTPMSCN) – Offset 484

Note that this USB2 Port Power Management Status and Control register is available at the following offsets for all applicable USB2 ports:

USB2 Port 1: 484h

USB2 Port 2: 494h

USB2 Port 3: 4A4h

.....

USB2 Port 9: 504h

USB2 Port 10: 514h

Bit Range	Default	Access	Field Name and Description
31:28	0h	RW/P	**Port Test Control (PTC)** When this field is '0', the port is not operating in a test mode. (Default) A non-zero value indicates that the port is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the Disabled state. If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error. The encoding of the Test Mode bits for a USB 2.0 port are: Value Test Mode 0h Test mode not enabled 1h Test J_STATE 2h Test K_STATE 3h Test SE0_NAK 4h Test Packet 5h Test FORCE_ENABLE 6h–14h Reserved. 15 Port Test Control Error

Bit Range	Default	Access	Field Name and Description
27:17	-	-	**Reserved**
16	0b	RW	**Hardware LPM Enable (HLE)** 0=disable 1=Enable. When this bit is a 1, hardware controlled LPM shall be enabled for this port. Refer to section 4 of the USB 2.0 LPM Specification for more information.
15:8	-	-	**Reserved**
7:4	0h	RW/P	**Host Initiated Resume Duration (HIRD)** Note: This register is sticky.
3	0b	RW/P	**Remote Wake Enable (RWE)** The host system sets this flag to enable or disable the device for remote wake from L1. 0=disable 1=enable The value of this flag will temporarily (while in L1) override the current setting of the Remote Wake feature set by the standard Set/ClearFeature() commands defined in Universal Serial Bus Specification, revision 2.0, Chapter 9.
2:0	0h	RW	**L1 Status (L1S)** Note: This register is sticky.

Port N Hardware LPM Control Register (PORTHLPMCN) – Offset 48c

Note that this Port Hardware Control register is available at the following offsets for all applicable USB ports:

USB2 Port 1: 48Ch

USB2 Port 2: 49Ch

USB2 Port 3: 4ACh

.....

USB2 Port 9: 50Ch

USB2 Port 10: 51Ch

This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST).The definition for the fields depend on the protocol supported.

For USB3 this register is reserved and shall be treated by software as RsvdP.

For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**
13:10	0h	RW	**Host Initiated Resume Duration-Deep (HIRDD)** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us...Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9:2	00h	RW/P	**L1 Timeout (L1_TO)** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us....FFh: 65,280us
1:0	0h	RW/P	**Host Initiated Resume Duration Mode (HIRDM)** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

USB2 PM Control (USB2PMCTRL_REG) – Offset 81c4

Bit Range	Default	Access	Field Name and Description
30:12	-	-	**Reserved**
11	0h	RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2PSPGPSCBP)** This controls the policy for blocking PORTSC Updates while the USB2 PHY SUS Well is power gated. When set, the controller will block any updates to the PORTSC caused by port status change if the USB2 PHY SUS is power gated.
10:8	0h	RW	**USB2 PHY SUS Well Power Gate Entry Hysteresis Count (U2PSPGEHC)** This controls the amount of hysteresis time the controller will enforce after detecting the USB2 PHY SUS Power Gate entry condition. 0h 0 clocks 1h 32 clocks 2h 64 clocks 3h 128 clocks 4h 256 clocks 5h 512 clocks 6h 1024 clocks 7h 2048 clocks
7:4	0h	RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2CLPGLAT)** This field represents the worst case latency for the USB2 Common Lane to enter and exit its power gate state. This fields is required to be compared to a ports HIRD/HIRD value for the ports that have allowed L1 to L2 mapping to determine if the Common Lane can be allowed to power off. If the power gate entry/exit latency is greater than the HIRD/HIRDD then the common lane should not be allowed to power gate as this will result in a L1 exit violation. 0h 100 us 1h 200 us 2h 300 us Eh 1500us Fh 1600 us

Bit Range	Default	Access	Field Name and Description
3:2	0h	RW	**USB2 PHY SUS Well Power Gate Policy (U2PSUSPGP)** This field controls when to enable the USB2 PHY SUS Well Power Gating when the proper conditions are met. 00 USB2 PHY SUS Power Gating is Disabled. 01 USB2 PHY SUS Power Gating is Enabled in Only D0 and D0i2 (Excludes D0i3 and D3) 10 USB2 PHY SUS Power Gating is Eanabled in only in D0, D0i2 and D0i3 (Excludes D3) 11 USB2 PHY SUS Power Gating is Eanabled in D0/D0i2/D0i3/D3
1	0h	RW	**USB2 Common Lane Power Gating Enable During L1 to L2 Mapping for USB2 PHY Power Gating (U2CLPGEL1L2)** This field when set enables the controller to allow for the common lane power gating to be enabled when all ports are exposed as in L2 to the USB2 PHY while at least 1 port has been mapped to L2 from L1. This field alone does not guarantee power gating since the L1 HIRD/HIRDD Value must be compared with the PHYs power gate exit latency (U2CLPGLAT) held in this register to ensure that L1 exit is not violated. 0 USB2 Common Lane Power Gating is disabled when any port has been mapped from L1 to L2. 1 USB2 Common Lane Power Gating is allowed when any port has been mapped to L2 from L1 with the additional condition that the HIRD/HIRDD is greater than the PHYs Power Gate exit latency.
0	0h	RW	**USB2 Data Lane L1 to L2 Mapping Enable for USB2 PHY Power Gating (U2DLL1L2ME)** This field when set enables the controller to map an L1 entry directly to L2 to allow the USB2 PHY to trigger its Autonomous Power Gating. The USB2 PHY will trigger PG only when in L2 since it does not fully understand the requirements for L1. 0 USB2 L1 to L2 mapping is disabled for all ports 1 USB2 L1 to L2 mapping is enabled for all ports

USB Legacy Support Capability (USBLEGSUP) – Offset 846c

This register is modified and maintained by BIOS

Bit Range	Default	Access	Field Name and Description
30:25	-	-	**Reserved**
24	0b	RW	**HC OS Owned Semaphore (HCOSOS)** Default = '0'. System software sets this bit to request ownership of the xHC. Ownership is obtained when this bit reads as '1' and the HC BIOS Owned Semaphore bit reads as '0'.
23:17	-	-	**Reserved**
16	0b	RW	**HC BIOS Owned Semaphore (HCBIOSOS)** Default = '0'. The BIOS sets this bit to establish ownership of the xHC. System BIOS will set this bit to a '0' in response to a request for ownership of the xHC by system software.
15:8	22h	RW/L	**Next Capability Pointer (NextCP)** This field indicates the location of the next capability with respect to the effective address of this capability. Refer to Table 145 for more information on this field.
7:0	01h	RW/L	**Capability ID (CID)** This field identifies the extended capability. Refer to Table 146 for the value that identifies the capability as Legacy Support.This extended capability requires one additional 32-bit register for control/status information (USBLEGCTLSTS), and this register is located at offset xECP+04h.

USB Legacy Support Control Status (USBLEGCTLSTS) – Offset 8470

Bit Range	Default	Access	Field Name and Description
31	0b	RW/1C	**SMI on BAR (SMIBAR)** Default = '0'. This bit is set to '1' whenever the Base Address Register (BAR) is written.
30	0b	RW/1C	**SMI on PCI Command (SMIPCIC)** . Default = '0'. This bit is set to '1' whenever the PCI Command Register is written.
29	0b	RW/1C	**SMI on OS Ownership Change (SMIOSOC)** Default = '0'. This bit is set to '1' whenever the HC OS Owned Semaphore bit in the USBLEGSUP register transitions from '1' to a '0' or '0' to a '1'.

Bit Range	Default	Access	Field Name and Description
28:21	-	-	**Reserved**
20	0b	RO	**SMI on Host System Error (SMIHSE)** Default = '0'. Shadow bit of Host System Error (HSE) bit in the USBSTS register.To clear this bit to a '0', system software shall write a '1' to the Host System Error (HSE) bit in the USBSTS register.
19:17	-	-	**Reserved**
16	0b	RO	**SMI on Event Interrupt (SMIEI)** Default = '0'. Shadow bit of Event Interrupt (EINT) bit in the USBSTS register. This bit follows the state the Event Interrupt (EINT) bit in the USBSTS register, e.g. it automatically clears when EINT clears or set when EINT is set.
15	0b	RW	**SMI on BAR Enable (SMIBARE)** Default = '0'. When this bit is '1' and SMI on BAR is '1', then the host controller will issue an SMI.
14	0b	RW	**SMI on PCI Command Enable (SMIPCICE)** . Default = '0'. When this bit is '1' and SMI on PCI Command is '1', then the host controller will issue an SMI.
13	0b	RW	**SMI on OS Ownership Enable (SMIOSOE)** Default = '0'. When this bit is a '1' AND the OS Ownership Change bit is '1', the host controller will issue an SMI.
12:5	-	-	**Reserved**
4	0b	RW	**SMI on Host System Error Enable (SMIHSEE)** Default = '0'. When this bit is a '1', and the SMI on Host System Error bit (below) in this register is a '1', the host controller will issue an SMI immediately.
3:1	-	-	**Reserved**
0	0b	RW	**USB SMI Enable (USBSMIE)** . Default = '0'. When this bit is a '1', and the SMI on Event Interrupt bit (below) in this register is a '1', the host controller will issue an SMI immediately.

Port Disable Override capability register (PDO_CAPABILITY) – Offset 84f4

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:8	03h	RO	**Next Capability Pointer (NCP)**
7:0	C6h	RO	**Capability ID (CID)**

USB2 Port Disable Override (USB2PDO) – Offset 84f8

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0h	RW/O	**USB2PDO (USB2PDO)** A '1' in a bit position prevents the corresponding USB2 port from reporting a Device Connection to the XHC.This applies across all USB2 protocol ports 0 = Allows corresponding USB port to report a device connection to the xHC. 1 = Prevents the corresponding USB port from reporting a device Connection to the xHC. Port to bit mapping is in one-hot encoding, that is bit 0 controls port 1 and so on. Bit 0 = USB 2.0 port 1 ... Bit N-1 = USB 2.0 port N

USB3 Port Disable Override (USB3PDO) – Offset 84fc

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:0	0h	RW/O	**USB3 Port Disable Override (USB3PDO)** 0 = Allows corresponding USB port to report a Device Connection to the xHC. 1 = Prevents the corresponding USB port from reporting a Device Connection to the xHC. Bit 0 = USB 3.1 Port 1 ... Bit N-1 = USB 3.1 Port N

Debug Capability ID Register (DCID) – Offset 8700

This register is modified and maintained by BIOS

Bit Range	Default	Access	Field Name and Description
30:21	-	-	**Reserved**
20:16	05h	RW/L	**Debug Capability Event Ring Segment Table Max (DCERSTM)** Note: This register is sticky.
15:8	10h	RW/L	**Next Capability Pointer (NCP)** Note: This register is sticky.
7:0	0Ah	RW/L	**Capability ID (CID)** Note: This register is sticky.

Debug Capability Doorbell Register (DCDB) – Offset 8704

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:8	00h	RW	**Doorbell Target (DBTGT)** Doorbell Target (DB Target) – RW. This field defines the target of the doorbell reference. Thetable below defines the Debug Capability notification that is generated by ringing the doorbell. Value Definition 0 Data EP 1 OUT Enqueue Pointer Update 1 Data EP 1 IN Enqueue Pointer Update 2:255 Reserved This field returns '0' when read and the value should be treated as undefined by software.
7:0	-	-	**Reserved**

Debug Capability Event Ring Segment Table Size Register (DCERSTSZ) – Offset 8708

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0000h	RW	**Event Ring Segment Table Size (ERSTS)** Event Ring Segment Table Size – RW. Default = '0'. This field identifies the number of validEvent Ring Segment Table entries in the Event Ring Segment Table pointed to by the DebugCapability Event Ring Segment Table Base Address register. The maximum value supported byan xHC implementation for this register is defined by the DCERST Max field in the DCID register. Software shall initialize this register before setting the Debug Capability Enable field in theDCCTRL register to '1'.

Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA) – Offset 8710

Bit Range	Default	Access	Field Name and Description

Bit Range	Default	Access	Field Name and Description
63:4	0000000 0000000 0h	RW	**Event Ring Segment Table Base Address Register (ERSTBAR)** 4 Event Ring Segment Table Base Address Register – RW. Default = '0'. This field defines thehigh order bits of the start address of the Debug Capability Event Ring Segment Table.Software shall initialize this register before setting the Debug Capability Enable field in theDCCTRL register to '1'.
3:0	-	-	**Reserved**

Debug Capability Event Ring Dequeue Pointer Register (DCERDP) – Offset 8718

Bit Range	Default	Access	Field Name and Description
63:4	0000000 0000000 0h	RW	**Dequeue Pointer (DQP)** Dequeue Pointer - RW. Default = '0'. This field defines the high order bits of the 64-bit addressof the current Debug Capability Event Ring Dequeue Pointer.Software shall initialize this register before setting the Debug Capability Enable field in theDCCTRL register to '1'.
3	-	-	**Reserved**
2:0	0h	RW	**Dequeue ERST Segment Index (DESI)** Dequeue ERST Segment Index (DESI) - RW. Default = '0'. This field may be used by the xHCto accelerate checking the Event Ring full condition. This field is written with the low order 3 bitsof the offset of the ERST entry which defines the Event Ring segment that the Event RingDequeue Pointer resides in.

Debug Capability Control Register (DCCTRL) – Offset 8720

Bit Range	Default	Access	Field Name and Description
31	0b	RW	**Debug Capability Enable (DCE)** Default = 0. Setting this bit to a '1' enables xHCI USB Debug Capability operation. This bit is a '0' if the USB Debug Capability is disabled. Clearing this bit releases the Root Hub port assigned to the Debug Capability, and terminates any Debug Capability Transfer or Event Ring activity. Note that DCE may be cleared to '0' by the assertion of a reset condition.

Bit Range	Default	Access	Field Name and Description
30:24	00h	RO	**Device Address (DADDR)** Default = 0. This field reports the USB device address assigned to the Debug Device during the enumeration process. This field is valid when the DbC Run bit is '1'.
23:16	00h	RO	**Debug Max Burst Size (DMBS)** Default = xHC Vendor defined. This field identifies the maximum burst size supported by the bulk endpoints of this DbC implementation.
15:5	-	-	**Reserved**
4	0b	RW/1C	**DbC Run Change (DRC)** Default = 0. This bit shall be set to '1' when DCR bit is cleared to '0', i.e. by any DbC Port State transition that exits the DbC-Configured state. While this bit is '1' the Debug Capability Doorbell Register (DCDB) is disabled. Software shall clear this bit to re-enable the DCDB.
3	0b	RW/1S	**Halt IN TR (HIT)** Default = 0. While this bit is '1' the Debug Capability shall generate STALL TPs for all OUT DPs received for the IN TR. The Debug Capability shall clear this bit when a ClearFeature(ENDPOINT_HALT) request is received for the endpoint. This field is valid only when the Debug Capability is in Run Mode (DCR = '1'). When not in Run Mode, this field shall return '0' when read, and writes will have no effect.
2	0b	RW/1S	**Halt OUT TR (HOT)** Default = 0. While this bit is '1' the Debug Capability shall generate STALL TPs for all IN TPs received for the OUT TR. The Debug Capability shall clear this bit when a ClearFeature(ENDPOINT_HALT) request is received for the endpoint. This field is valid only when the Debug Capability is in Run Mode (DCR = '1'). When not in Run Mode, this field shall return '0' when read, and writes will have no effect.
1	0b	RW	**Link Status Event Enable (LSE)** Default = '0'. Setting this bit to a '1' enables the Debug Capability to generate Port Status Change Events due the Port Link Status Change bit transitioning from a '0' to a '1'.
0	0b	RO	**DbC Run (DCR)** . Default = 0. When '0', Debug Device is not in the Configured state. When '1', Debug Device is in the Configured state and bulk Data pipe transactions are accepted by Debug Capability and routed to the IN and OUT Transfer Rings. A '0' to '1' transition of the Port Reset (DCPORTSC:PR) bit will clear this bit to '0'.

Debug Capability Status Register (DCST) – Offset 8724

Bit Range	Default	Access	Field Name and Description
31:24	00h	RO	**Debug Port Number (DPNUM)** Debug Port Number – RO. Default = 0. This field provides the ID of the Root Hub port that theDebug Capability has been automatically attached to. The value is '0' when the DebugCapability is not attached to a Root Hub port.
23:1	-	-	**Reserved**
0	0b	RO	**Event Ring Not Empty (ERNE)** Event Ring Not Empty (ER) – RO. Default = '0'. When '1', this field indicates that the DebugCapability Event Ring has a Transfer Event on it. It is automatically cleared to '0' by the xHCwhen the Debug Capability Event Ring is empty, i.e. the Debug Capability Enqueue Pointer isequal to the Debug Capability Event Ring Dequeue Pointer register.

Debug Capability Port Status and Control Register (DCPORTSC) – Offset 8728

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23	0b	RW/1C	**Port Config Error Change (CEC)** This flag indicates that the port failed to configure its link partner. 0 = No change. 1 = Port Config Error detected. Software shall clear this bit by writing a '1' to it.
22	0b	RW/1C	**Port Link Status Change (PLC)** Port Link Status Change (PLC) = RW1C. Default = '0'. This flag is set to '1' due to thefollowing PLS transitions: Transition Condition U0 -> U3 Suspend signaling detected from Debug Host U3 -> U0 Resume completePolling -> Disabled Training Error Ux or Recovery -> Inactive Error Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'.

Bit Range	Default	Access	Field Name and Description
21	0b	RW/1C	**Port Reset Change (PRC)** This bit is set when reset processing on this port is complete (i.e. a '1' to '0' transition of PR). '0' = No change. '1' = Reset complete.Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'.
20:18	-	-	**Reserved**
17	0b	RW/1C	**Connect Status Change (CSC)** an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'.
16:14	-	-	**Reserved**
13:10	0h	RO	**Port Speed (PSPD)** Port Speed (Port Speed) – RO. Default = ‘0’. This field identifies the speed of the port. Thisfield is only relevant when a Debug Host is attached (CCS = ‘1’) in all other cases this field shallindicate Undefined Speed. Value Speed 0100b SuperSpeed (5Gb/s) All other values reserved.
9	-	-	**Reserved**
8:5	4h	RO	**Port Link State (PLS)** Port Link State (PLS) – RO. Default = undefined. This field reflects its current link state. Thisfield is only relevant when a Debug Host is attached (Debug Port Number > ‘0’). 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspended) 4: Link is in the Disabled State 5: Link is in the RxDetect State 6: Link is in the Inactive State 7: Link is in the Polling State 8: Link is in the Recovery State 9: Link is in the Hot Reset State 15-10: Reserved Note: Transitions between different states are not reflected until the transition is complete
4	0b	RO	**Port Reset (PR)** '1' = Port is in Reset. '0' = Port is not in Reset. This bit is set to '1' when the bus reset sequence as defined in the USB Specification is detected on the Root Hub port assigned to the Debug capability. It is cleared when the bus reset sequence is completed by the Debug Host, and the DbC shall transition to the USB Default state. A '0' to '1' transition of this bit shall clear DCPORTSC PED ('0'). This field is '0' if DCE or CCS are '0'.

Bit Range	Default	Access	Field Name and Description
3:2	-	-	**Reserved**
1	0b	RW	**Port Enabled/Disabled (PED)** Port Enabled/Disabled (PED) – RW. Default = ‘0’. ‘1’ = Enabled. ‘0’ = Disabled. This flag shallbe set to '1' by a '0' to '1' transition of CCS or a '1' to '0' transition of the PR. When PEDtransitions from '1' to '0' due to the assertion of PR, the port's link shall transition to theRx.Detect state. This flag may be used by software to enable or disable the operation of theRoot Hub port assigned to the Debug Capability. The Debug Capability Root Hub portoperation may be disabled by a fault condition (disconnect event or other fault condition, e.g. aLTSSM Polling substate timeout, tPortConfiguration timeout error, etc.), the assertion ofDCPORTSC PR, or by software. 0 = Debug Capability Root Hub port is disabled. 1 = Debug Capability Root Hub port is enabled. When the port is disabled (PED = ‘0’) the port’s link shall enter the SS.Disabled state andremain there until PED is reasserted ('1') or DCE is negated ('0'). Note that the Root Hub port isremains mapped to Debug Capability while PED = '0'. While PED = '0' the Debug Capability willappear to be disconnected to the Debug Host. This field is ‘0’ if DCE or CCS are ‘0’.
0	0b	RO	**Current Connect Status (CCS)** '1' = A Root Hub port is connected to a Debug Host and assigned to the Debug Capability. '0' = No Debug Host is present. This value reflects the current state of the port, and may not correspond to the value reported by the Connect Status Change (CSC) field in the Port Status Change Event that was generated by a '0' to '1' transition of this bit. This flag is '0' if Debug Capability Enable (DCE) is '0'.

Debug Capability Context Pointer Register (DCCP) – Offset 8730

Bit Range	Default	Access	Field Name and Description
63:4	0000000 0000000 0h	RW	**Debug Capability Context Pointer Register (DCCPR)** This field defines the high order bits of the start address of the Debug Capability Context data structure associated with the Debug Capability. Software shall initialize this register before setting the Debug Capability Enable bit in the Debug Capability Control Register to '1'.

Bit Range	Default	Access	Field Name and Description
3:0	-	-	**Reserved**

Global Time Sync Capability (GLOBAL_TIME_SYNC_CAP_REG) – Offset 8e10

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:8	12h	RO	**Next Capability pointer (NCP)**
7:0	C9h	RO	**Capability ID (CID)**

Port Status and Control USB2 (PORTSCXUSB3) – Offset 540

The USB3 Port Status and Control registers are available at the following offsets forapplicable USB3 ports:

USB3 Port 1: 540h

USB3 port 2: 550h

USB3 port 3: 560h

USB3 port 4: 570h

USB3 port 5: 580h

USB3 port 6: 590h

Bit Range	Default	Access	Field Name and Description
31	0b	RW/1S	**Warm Port Reset (WPR)** When software sets this bit to 1b, the Warm Reset sequence is enabled

Bit Range	Default	Access	Field Name and Description
30	0b	RW/L	**Device Removable (DR)** This bit indicates if this port has a removable device. 0 = Device is removable. 1 = Device is non-removable.
29:28	-	-	**Reserved**
27	0b	RW/P	**Wake on Over-current Enable (WOE)** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to overcurrent conditions as system wake-up events.
26	0b	RW/P	**Wake on Disconnect Enable (WDE)** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device disconnects as system wake-up events.
25	0b	RW/P	**Wake on Connect Enable (WCE)** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device connects as system wake-up events.
24	0b	RO	**Cold Attach Status (CAS)** This bit indicates that far-end terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable to advance to the Enabled state. Software shall clear this bit by writing a 1b to the WPR bit or the xHC shall clear this bit if the CSS bit transitions to 1.
23	0b	RW/1C	**Port Config Error Change (CEC)** Note: This register is sticky.

Bit Range	Default	Access	Field Name and Description
22	0b	RW/1C	**Port Link State Change (PLC)** 0 = No change 1 = Link Status Change This flag is set to '1' due to the following Port Link State (PLS) transitions:
21	0b	RW/1C	**Port Reset Change (PRC)** This flag is set to '1' due a '1' to '0' transition of Port Reset (PR), for example, when any reset processing on this port is complete. 0 = No change 1 = Reset Complete
20	0b	RW/1C	**Over-current Change (OCC)** The functionality of this bit is not dependent upon the port owner. Software clears this bit by writing a 1 to it. 0 = No change. (Default) 1 = There is a change to Overcurrent Active.
19	0b	RW/1C	**Warm Port Reset Change (WRC)** This bit is set when Warm Reset processing on this port completes. 0 = No change. (Default) 1 = Warm reset complete
18	0b	RW/1C	**Port Enabled Disabled Change (PEC)** 0 = No change. (Default) 1 = There is a change to PED bit.

Bit Range	Default	Access	Field Name and Description
17	0b	RW/1C	**Connect Status Change (CSC)** R/WC. This flag indicates a change has occurred in the port's Current Connect Status (CCS) or Cold Attach Status (CAS) bits. 0 = No change. (Default) 1 = There is a change to the CCS or CAS bit. The xHC sets this bit to 1b for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (that is, the bit will remain 1b).
16	0b	RW	**Port Link State Write Strobe (LWS)** 0 = When 0b, write data in PLS field is ignored. (Default) 1 = When this bit is set to 1b on a write reference to this register, this flag enables writes to the PLS field. Reads to this bit return '0'.
15:14	0h	RW/P	**Port Indicator Control (PIC)** Note: This register is sticky.
13:10	0h	RO	**Port Speed (PortSpeed)** A device attached to this portoperates at a speed defined by the following codes: Value Speed 0100b SuperSpeed (5Gb/s) 0101b SuperSpeedPlus (10Gb/s) All other values reserved.
9	1b	RW/P	**Port Power (PP)** Default value of 1. 0 = This port is in the powered-off state 1 = This port is in the powered-on state. This indicates that the port does have power.
8:5	5h	RW/P	

Bit Range	Default	Access	Port Link State (PLS) Field Name and Description
			This field is used to power manage the port and reflects its current link state.When the port is in the Enabled state, system software may setthe link U-state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write Value and Description: 0: The link shall transition to a U0 state from any of the U-states. 2: USB 2.0 ports only. The link should transition to the U2 State. 3: The link shall transition to a U3 state from any of the U-states.This action selectively suspends the device connected to this port.While the Port Link State = U3, the hub does not propagatedownstream-directed traffic to this port, but the hub will respondto resume signaling from the port. 5: USB 3.0 ports only. If the port is in the Disabled state (PLS =Disabled, PP = 1), then the link shall transition to a RxDetect stateand the port shall transition to the Disconnected state, elseignored. 15: USB 2.0 ports only. If the port is in the U3 state (PLS = U3),then the link shall remain in the U3 state and the port shalltransition to the U3Exit substate, else ignored.All other values IgnoredNote: The Port Link State Write Strobe (LWS) shall be set to 1b towrite this field. Read Value and Definition: 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspended) 4: Link is in the Disabled State 5: Link is in the RxDetect State 6: Link is in the Inactive State 7: Link is in the Polling State 8: Link is in the Recovery State 9: Link is in the Hot Reset State 10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12–14: Reserved 15: Link is in the Resume State

Bit Range	Default	Access	Field Name and Description
4	0b	RW/1S	**Port Reset (PR)** When software writes a1 to this bit (from a 0), the bus reset sequence as defined in the USB Specification, Revision 2.0 is started. Software writes a 0 tothis bit to terminate the bus reset sequence. Software must keep this bit at a 1 long enough to ensure the reset sequence completes as specified in the USB Specification, Revision 2.0. USB 3.0 portsshall execute the Hot Reset sequence as defined in the USB 3.0 Specification. PR remains set until reset signaling is completed by the root hub. 1 = Port is in Reset. 0 = Port is not in Reset.

Bit Range	Default	Access	Field Name and Description
3	0b	RW	**Over-current Active (OCA)** 0 = This port does not have an overcurrent condition. (Default) 1 = This port currently has an overcurrent condition. This bit will automatically transition from 1 to 0 when the overcurrent condition is removed. The PCH automatically disables the port when the overcurrent active bit is 1.
2	-	-	**Reserved**
1	0b	RW/1C	**Port Enabled Disabled (PED)** Note: This register is sticky.
0	0b	RW	**Current Connect Status (CCS)** This value reflects the currentstate of the port, and may not correspond directly to the eventthat caused the Connect Status Change bit (Bit 1) to be set. 0 = No device is present. (Default) 1 = Device is present on port.

Port Power Management Status and Control USB2 (PORTPMSCX) – Offset 544

The USB3 Port Status and Control registers are available at the following offsets forapplicable USB3 ports:

USB3 Port 1: 544h

USB3 port 2: 554h

USB3 port 3: 564h

USB3 port 4: 574h

USB3 port 5: 584h

USB3 port 6: 594h

Bit Range	Default	Access	Field Name and Description
30:17	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
16	0h	RW	**Force Link PM Accept (FLA)**
15:8	0h	RW/P	**U2 Timeout (U2T)**
7:0	0h	RW/P	**U1 Timeout (U1T)**

USB3 Port X Link Info (PORTLIX) – Offset 548

Note that this USB3 Port Link Info register is available at the following offsets for allapplicable USB3 ports:

USB3 Port 1: 548h

USB3 port 2: 558h

USB3 port 3: 568h

USB3 port 4: 578h

USB3 port 5: 588h

USB3 port 6: 598h

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0000h	RO	**Link Error Count (LEC)** Displays the Link Error Count for the USB 3 port.

Microframe Index (RTMFINDEX) – Offset 2000

Bit Range	Default	Access	Field Name and Description
30:14	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
13:0	0000h	RO	**Microframe Index (MI)** The value in this register increments at the end of each microframe (for example, 125 µs.). Bits [13:3] may be used to determine the current 1ms. Frame Index.

Interrupter x Management (IMANx) – Offset 2020

Note that there are a total of 8 IMAN registers at the following offsets:

IMAN0: at offset 2020h

IMAN1: at offset 2040h

IMAN2: at offset 2060h

.....

IMAN6: at offset 20E0h

IMAN7; at offset 2100h

Bit Range	Default	Access	Field Name and Description
30:2	-	-	**Reserved**
1	0b	RW	**Interrupt Enable (IE)** This flag specifies whether the Interrupter is capable of generating an interrupt.0 = The Interrupter is prohibited from generating interrupts.1 = When this bit and the IP bit are set (1b), the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches '0'.
0	0b	RW/1C	**Interrupt Pending (IP)** 0 = No interrupt is pending for the Interrupter.1 = An interrupt is pending for this Interrupter.This bit is set to 1b when IE = 1, the IMODI Interrupt Moderation Counter field = 0b, the Event Ring associated with the Interrupter is not empty (or for the Primary Interrupter when the HCE flag is set to 1b), and EHB = 0. If MSI interrupts are enabled, this flag shall be cleared automatically when the PCI DWord write generated by the Interrupt assertion is complete. If PCI Pin Interrupts are enabled, this flag shall be cleared by software.

Interrupter x Moderation (IMODx) – Offset 2024

Note that there are a total of 8 IMOD registers at the following offsets:

IMOD0 : at offset 2024h

IMOD1: at offset 2044h

IMOD2: at offset 2064h

.....

IMOD6: at offset 20E4h

IMOD7; at offset 2104h

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW	**Interrupt Moderation Counter (IMODC)** Down counter. Loaded with Interval Moderation value—value of bits 15:0, whenever the IP bit is cleared to 0b, counts down to '0', and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP bits = 1, and EHB = 0.This counter may be directly written by software at any time to alter the interrupt rate
15:0	0FA0h	RW	**Interrupt Moderation Interval (IMODI)** Minimum inter-interrupt interval. The interval is specified in 250 ns increments. A value of '0' disables interrupt throttling logic and interrupts shall be generated immediately if IP = 0, EHB = 0, and the Event Ring is not empty.

Event Ring Segment Table Size x (ERSTSZx) – Offset 2028

There are 8 ERSTSZ registers available at the following address offsets:

ERSTSZ0: at offset 2028h

ERSTSZ1: at offset 2048h

ERSTSZ2: at offset 2068h

ERSTSZ3: at offset 2088h

ERSTSZ4: at offset 20A8h

ERSTSZ5: at offset 20C8h

ERSTSZ6: at offset 20E8h

ERSTSZ7: at offset 2108h

Address Offset: 2028-202Bh, 2048-204Bh, ..., 2028+(MaxInts-1)*20h-202B+(MaxInts-1)*20h

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0000h	RW	**Event Ring Segment Table Size (ERSTS)** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register.

Event Ring Segment Table Base Address Low x (ERSTBA_LOx) – Offset 2030

There are 8 ERSTBA_LO registers available at the following address offsets:

ERSTBA_LO0: at offset 2030h

ERSTBA_LO1: at offset 2050h

ERSTBA_LO2: at offset 2070h

ERSTBA_LO3: at offset 2090h

ERSTBA_LO4: at offset 20B0h

ERSTBA_LO5: at offset 20D0h

ERSTBA_LO6: at offset 20F0h

ERSTBA_LO7: at offset 2110h

Bit Range	Default	Access	Field Name and Description
31:6	0000000h	RW	**Event Ring Segment Table Base Address Register (ERSTBA)** This field defines the low order bits of the start address of the Event Ring Segment Table. This field shall not be modified if HCHalted (HCH) = 0.
5:0	-	-	**Reserved**

Event Ring Segment Table Base Address High x (ERSTBA_HIx) – Offset 2034

There are 8 ERSTBA_HI registers available at the following address offsets:

ERSTBA_HI0: at offset 2034h

ERSTBA_HI1: at offset 2054h

ERSTBA_HI2: at offset 2074h

ERSTBA_HI3: at offset 2094h

ERSTBA_HI4: at offset 20B4h

ERSTBA_HI5: at offset 20D4h

ERSTBA_HI6: at offset 20F4h

ERSTBA_HI7: at offset 2114h

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Event Ring Segment Table Base Address (ERSTBA)** This field defines the low order bits of the start address of the Event Ring Segment Table. This field shall not be modified if HCHalted (HCH) = 0.

Event Ring Dequeue Pointer Low x (ERDP_LOx) – Offset 2038

There are 8 ERDP_LO registers available at the following address offsets:

ERDP_LO0: at offset 2038h

ERDP_LO1: at offset 2058h

ERDP_LO2: at offset 2078h

ERDP_LO3: at offset 2098h

ERDP_LO4: at offset 20B8h

ERDP_LO5: at offset 20D8h

ERDP_LO6: at offset 20F8h

ERDP_LO7: at offset 2118h

Bit Range	Default	Access	Field Name and Description
31:4	0000000h	RW	**Event Ring Dequeue Pointer (ERDP)** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that Event Ring Dequeue Pointer resides in.
3	0b	RW/1C	**Event Handler Busy (EHB)** This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written.
2:0	0h	RW	**Dequeue ERST Segment Index (DESI)** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that Event Ring Dequeue Pointer resides in.

Event Ring Dequeue Pointer High x (ERDP_HIx) – Offset 203c

There are 8 ERDP_LO registers available at the following address offsets:

ERDP_HI0: at offset 203Ch

ERDP_HI1: at offset 205Ch

ERDP_HI2: at offset 207Ch

ERDP_HI3: at offset 209Ch

ERDP_HI4: at offset 20BCh

ERDP_HI5: at offset 20DCh

ERDP_HI6: at offset 20FCh

ERDP_HI7: at offset 211Ch

Bit Range	Default	Access	Field Name and Description
31:0	00000000h	RW	**Event Ring Dequeue Pointer (ERDP)** This field defines the low order bits of the 64- bit address of the current Event Ring Dequeue Pointer.

Door Bell x (DBx) – Offset 3000

Door Bell registers are an array of 32 registers.

The door bell registers are at the following offset:

Door Bell 0: 3000-3003h

Door Bell 1: 3004-3007h

.....

Door Bell 30: 3078-307Bh

Door Bell 31: 307C-307Fh

Bit Range	Default	Access	Field Name and Description
31:16	0000h	RW	**DB Stream ID (DSID)** If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.
15:8	-	-	**Reserved**
7:0	00h	RW	**DB Target (DT)** This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Refer to the xHCI Specification for definitions of the values.

XECP_SUPP_USB2_0 (XECP_SUPP_USB2_0) – Offset 8000

Bit Range	Default	Access	Field Name and Description
31:24	02h	RO	**USB Major Revision: 2.0 (USB2_MAJ_REV)** Major Specification Release Number in Binary-Coded Decimal (i.e., version 3.x is 03h). This field identifies the major release number component of the specification with which the xHC is compliant.
23:16	00h	RO	**USB Minor Revision (USB_MIN_REV)** Minor Specification Release Number in Binary-Coded Decimal (i.e., version x.10 is 10h). This field identifies the minor release number component of the specification with which the xHC is compliant.
15:8	08h	RO	**Next Capability Pointer (NCP)** This field indicates the location of the next capability with respect to the effective address of this capability.
7:0	02h	RO	**Supported Protocol ID (SPID)** This field identifies the xHCI Extended capability. Refer to Table 146 for a list of the valid xHCI extended capabilities.

XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1) – Offset 8004

Bit Range	Default	Access	Field Name and Description
31:0	20425355h	RO	**XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1)** This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters may be defined. Allowed characters are: alphanumeric, space, and underscore. Alpha characters are case sensitive.

XECP_SUPP_USB2_2 (XECP_SUPP_USB2_2) – Offset 8008

Bit Range	Default	Access	Field Name and Description
31:28	3h	RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT)** 3 USB 2.0 Speed (High, Full, Low)
27:21	-	-	**Reserved**

Bit Range	Default	Access	Field Name and Description
20	1b	RW/L	**BESL LPM Capability (BLC)** Bit is set to 1 to indicate that the the ports described by this xHCI Supported Protocol Capability will apply BESL timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMCC registers.
19	1b	RW/L	**Protocol Defined - Hardware LMP Capability (HLC)**
18	0b	RO	**Protocol Defined - Integrated Hub Implementation (IHI)**
17	0b	RO	**Protocol Defined - High SPeed Only (HSO)** This field indicates the number of Protocol Speed ID (PSI) Dwords that the xHCI Supported Protocol Capability data structure contains.If this field is non-zero, then all speeds supported by the protocol shall be defined using PSI Dwords, i.e. no implied Speed ID mappings apply.
16	-	-	**Reserved**
15:8	16d	RO	**Compatible Port Count (CPC)** This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are 1 to MaxPorts.
7:0	1h	RO	**Compatible Port Offset (CPO)** This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are '1' to MaxPorts.

XECP_SUPP_USB3_3 (XECP_SUPP_USB2_3) – Offset 800c

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4:0	00h	RO	**XECP_SUPP_USB3_3 (PROTOCOL_SLOT_TYPE)** Protocol Slot Type

XECP_SUPP_USB2_4 (Full Speed) (XECP_SUPP_USB2_4) – Offset 8010

Bit Range	Default	Access	Field Name and Description
31:16	000Ch	RO	**Protocol Speed ID Mantissa (PSIM)** This field defines the mantissa that shall be applied to the PSIE when calculating the maximum bit rate represented by this PSI Dword
15:14	00h	RO	**Link Protocol (LP)** Link Protocol (LP): 0: SuperSpeed 1: SuperSpeedPlus 3-2: Reserved
13:9	-	-	**Reserved**
8	0b	RO	**PSI Full Duplex (PFD)** If this bit is '1' the link is full-duplex (dual-simplex), and if '0' the link is half-duplex (simplex).
7:6	0h	RO	**PSI Type (PLT)** This field identifies whether the PSI Dword defines a symmetric or asymmetric bit rate, and if asymmetric, then this field also indicates if this Dword defines the receive or transmit bit rate. Note that the Asymmetric PSI Dwords shall be paired, i.e. an Rx immediately followed by a Tx, and both Dwords shall define the same value for the PSIV.PLT Value Bit Rate Note 0 Symmetric Single PSI Dword 1 Reserved 2 Asymmetric Rx Paired with Asymmetric Tx PSI Dword 3 Asymmetric Tx Immediately follows Rx Asymmetric PSI Dword
5:4	2h	RO	**Protocol Speed ID Exponent (PSIE)** This field defines the base 10 exponent times 3, that shall be applied to the Protocol Speed ID Mantissa when calculating the maximum bit rate represented by this PSI Dword.PSIE Value Bit Rate 0 Bits per second 1 Kb/s 2 Mb/s 3 Gb/s

Bit Range	Default	Access	Field Name and Description
3:0	1h	RO	**Protocol Speed ID Value (PSIV)** If a device is attached that operates at the bit rate defined by this PSI Dword, then the value of this field shall be reported in the Port Speed field of PORTSC register (5.4.8) of a compatible port. Note, the PSIV value of '0' is reserved and shall not be defined by a PSI.

XECP_SUPP_USB2_4 (Low Speed) (XECP_SUPP_USB2_5) – Offset 8014

Bit Range	Default	Access	Field Name and Description
31:16	05DCh	RO	**Protocol Speed ID Mantissa (PSIM)**
15:14	0h	RO	**Link Protocol (LP)** Link Protocol (LP): 0: SuperSpeed 1: SuperSpeedPlus 3-2: Reserved
13:9	-	-	**Reserved**
8	0b	RO	**PSI Full Duplex (PFD)**
7:6	0h	RO	**PSI Type (PLT)**
5:4	1h	RO	**Protocol Speed ID Exponent (PSIE)**
3:0	2h	RO	**Protocol Speed ID Value (PSIV)**

XECP_SUPP_USB2_5 (High Speed) (XECP_SUPP_USB2_6) – Offset 8018

Bit Range	Default	Access	Field Name and Description
31:16	01E0h	RO	**Protocol Speed ID Mantissa (PSIM)**
15:14	0h	RO	**Link Protocol (LP)** Link Protocol (LP): 0: SuperSpeed 1: SuperSpeedPlus 3-2: Reserved
13:9	-	-	**Reserved**
8	0b	RO	**PSI Full Duplex (PFD)**
7:6	0h	RO	**PSI Type (PLT)**
5:4	2h	RO	**Protocol Speed ID Exponent (PSIE)**
3:0	3h	RO	**Protocol Speed ID Value (PSIV)**

XECP_SUPP_USB3_0 (XECP_SUPP_USB3_0) – Offset 8020

Bit Range	Default	Access	Field Name and Description
31:24	03h	RO	**USB Major Revision: 3.0 (USB3_MAJ_REV)**
23:16	01h	RO	**USB Minor Revision (USB3_MIN_REV)**
15:8	14h	RO	**Next Capability Pointer (NCP)**
7:0	02h	RO	**Supported Protocol ID (SPID)**

XECP_SUPP_USB3_1 (XECP_SUPP_USB3_1) – Offset 8024

Bit Range	Default	Access	Field Name and Description
31:0	20425355h	RO	**XECP_SUPP_USB3_1 (XECP_SUPP_USB3_1)** Namestring USB

XECP_SUPP_USB3_2 (XECP_SUPP_USB3_2) – Offset 8028

Bit Range	Default	Access	Field Name and Description
31:28	8h	RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT)** 1 USB 3.0 Speed (Supper Speed)
27:16	-	-	**Reserved**
15:8	10d	RO	**Compatible Port Count (CPC)**
7:0	17d	RO	**Compatible Port Offset (CPO)**

XECP_SUPP_USB3_3 (XECP_SUPP_USB3_3) – Offset 802c

Bit Range	Default	Access	Field Name and Description
30:5	-	-	**Reserved**
4:0	00h	RO	**XECP_SUPP_USB3_3 (PROTOCOL_SLOT_TYPE)** Protocol Slot Type

XECP_SUPP_USB3_4 (XECP_SUPP_USB3_4 Super Speed) – Offset 8030

Bit Range	Default	Access	Field Name and Description
31:16	0005h	RO	**Protocol Speed ID Mantissa (PSIM)**
15:14	0h	RO	**Link Protocol (LP)** Link Protocol (LP): 0: SuperSpeed 1: SuperSpeedPlus 3-2: Reserved
13:9	-	-	**Reserved**
8	1b	RO	**PSI Full Duplex (PFD)**
7:6	0h	RO	**PSI Type (PLT)**
5:4	3h	RO	**Protocol Speed ID Exponent (PSIE)**
3:0	4h	RO	**Protocol Speed ID Value (PSIV)**

XECP_SUPP_USB3_5 (XECP_SUPP_USB3_5 Super Speed Plus) – Offset 8034

Bit Range	Default	Access	Field Name and Description
31:16	Ah	RO	**Protocol Speed ID Mantissa (PSIM)**
15:14	0h	RO	**Link Protocol (LP)** Link Protocol (LP): 0: SuperSpeed 1: SuperSpeedPlus 3-2: Reserved

Bit Range	Default	Access	Field Name and Description
13:9	-	-	**Reserved**
8	1b	RO	**PSI Full Duplex (PFD)**
7:6	0h	RO	**PSI Type (PLT)**
5:4	3h	RO	**Protocol Speed ID Exponent (PSIE)**
3:0	5h	RO	**Protocol Speed ID Value (PSIV)**

XECP_SUPP_USB3_6 (XECP_SUPP_USB3_6) – Offset 8038

Bit Range	Default	Access	Field Name and Description
31:16	4E0h	RO	**Protocol Speed ID Mantissa (PSIM)**
15:14	0h	RO	**Link Protocol (LP)** Link Protocol (LP): 0: SuperSpeed 1: SuperSpeedPlus 3-2: Reserved
13:9	-	-	**Reserved**
8	1b	RO	**PSI Full Duplex (PFD)**
7:6	0h	RO	**PSI Type (PLT)**
5:4	2h	RO	**Protocol Speed ID Exponent (PSIE)**

Bit Range	Default	Access	Field Name and Description
3:0	6h	RO	**Protocol Speed ID Value (PSIV)**

XECP_SUPP_USB3_7 (XECP_SUPP_USB3_7) – Offset 803c

Bit Range	Default	Access	Field Name and Description
31:16	9C0h	RO	**Protocol Speed ID Mantissa (PSIM)**
15:14	0h	RO	**Link Protocol (LP)** Link Protocol (LP): 0: SuperSpeed 1: SuperSpeedPlus 3-2: Reserved
13:9	-	-	**Reserved**
8	1b	RO	**PSI Full Duplex (PFD)**
7:6	0h	RO	**PSI Type (PLT)**
5:4	2h	RO	**Protocol Speed ID Exponent (PSIE)**
3:0	7h	RO	**Protocol Speed ID Value (PSIV)**

XECP_SUPP_USB3_8 (XECP_SUPP_USB3_8) – Offset 8040

Bit Range	Default	Access	Field Name and Description
31:16	1380h	RO	**Protocol Speed ID Mantissa (PSIM)**

Bit Range	Default	Access	Field Name and Description
15:14	0h	RO	**Link Protocol (LP)** Link Protocol (LP): 0: SuperSpeed 1: SuperSpeedPlus 3-2: Reserved
13:9	-	-	**Reserved**
8	1b	RO	**PSI Full Duplex (PFD)**
7:6	0h	RO	**PSI Type (PLT)**
5:4	2h	RO	**Protocol Speed ID Exponent (PSIE)**
3:0	8h	RO	**Protocol Speed ID Value (PSIV)**

XECP_SUPP_USB3_9 (XECP_SUPP_USB3_9) – Offset 8044

Bit Range	Default	Access	Field Name and Description
31:16	05B1h	RO	**Protocol Speed ID Mantissa (PSIM)**
15:14	0h	RO	**Link Protocol (LP)** Link Protocol (LP): 0: SuperSpeed 1: SuperSpeedPlus 3-2: Reserved
13:9	-	-	**Reserved**
8	1b	RO	**PSI Full Duplex (PFD)**

Bit Range	Default	Access	Field Name and Description
7:6	0h	RO	**PSI Type (PLT)**
5:4	2h	RO	**Protocol Speed ID Exponent (PSIE)**
3:0	9h	RO	**Protocol Speed ID Value (PSIV)**

Host Control Scheduler (HOST_CTRL_SCH_REG) – Offset 8094

Bit Range	Default	Access	Field Name and Description
30:13	-	-	**Reserved**
12:11	0h	RW	**Cache Size Control Reg (CACHE_SZ_CTRL)** 0: 64 1: 32 2,3: 16
10:9	-	-	**Reserved**
8	1b	RW	**Turn on scratch_pad_en (TO_SCRATCH_PAD_EN)**
7	00h	RW	**Scheduler Host Control Reg (STOP_SCH_UNCON)** enable check to stop scheduling on port that are not connected
6	0b	RW	**disable 1 pack scheduling limit when ISO pending in present microframe (DIS_SCH_LIMIT)** disable 1 pack scheduling limit when ISO pending in present microframe

Bit Range	Default	Access	Field Name and Description
5:4	0h	RW	**scheduler sort pattern (SCH_SORT_PATTERN)** 00 (default) search ISO ahead of interrupt within each service interval 01 - search USB2-ISO, USB3-ISO, USB2-Interrupt, USB3-Interrupt within each service interval 10 - search strictly by interval 11 - search all ISO intervals ahead interrupt intervals and within each interval, USB2 ahead of USB3
3	0b	RW	**enable TTE overlap prevention on interrupt OUT EPs (at cost of possible service interval slip (EN_TTE_OVERLAP_PREV_OUT)** enable TTE overlap prevention on interrupt OUT EPs (at cost of possible service interval slip
2	0b	RW	**enable TTE overlap prevention on interrupt IN EPs (at cost of possible service interval slip (EN_TTE_OVERLAP_PREV_IN)** enable TTE overlap prevention on interrupt IN EPs (at cost of possible service interval slip
1	0b	RW	**Disable TRM active IN EP valid check function (DIS_TRM_ACT_IN_VALID)** Disable TRM active IN EP valid check function
0	0b	RW	**Disable poll delay function (DIS_POLL_DELAY)**

Power Management Control (PMCTRL_REG) – Offset 80a4

Bit Range	Default	Access	Field Name and Description
31	0h	RW	**Async PME Source Enable (ASYNC_PME_SRC_EN)** This field allows the async PME source to be allowed to generate PME. This is specifically required for SOCs that do not allow for any clock other than RTC to be available during RTD3.

Bit Range	Default	Access	Field Name and Description
30	0h	RW	**Legacy PME Source Enable (LEGACY_PME_SRC_EN)** This field allows the legacy PME source to be used in PME generation. The legacy source in in reference to the source prior to the RTD3 changes.
29	0h	RW	**Reset Warn Power Gate Trigger Disable (RESET_WARN_PWR_GATE_TRIGGER_DISABLE)** This field controls the actions taken for due to reset warn. 0 - Reset Warn will trigger a HW autonomous Power Gate 1 - Reset Warn will not trigger a HW autonomous Power Gate
28	0h	RW	**CLR_PME_FLAG_PULSE_AUX_CCLK (CLR_PME_FLAG_PULSE_AUX_CCLK)** Internal PME flag Clear This Write-Only bit can be used to clear the internal PME flag. SW write to '1' will clear the PME flag. SW write to '0' will have no effect and be ignored by the controller.
27	0h	RW	**Disable RTD3 power gating when in D3 (DIS_D3_PG)** Disable RTD3 power gating when in D3 and context save operation is not performed
26	0h	RW	**XLFPSCOUNTSRC (XLFPSCOUNTSRC)** XLFPSCOUNTSRC (Source for LFPS OFF Counter) 0: Central RTC Counter for LFPS detection 1: Local Counter for LFPS detection
25	0h	RW	**XELFPSRTC (XELFPSRTC)** XELFPSRTC (Enable LFPS Filtering on RTC) 0: Use Oscillator clock for LFPS Filtering during P3 1: Use RTC Clock for LFPS Filtering during P3

Bit Range	Default	Access	Field Name and Description
24	0h	RW	**XMPHYSPGDD0I2 (XMPHYSPGDD0I2)** XMPHYSPGDD0I2 (ModPhy Sus Well Power Gate Disable for D0I2) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
23	0h	RW	**XMPHYSPGDD0I3 (XMPHYSPGDD0I3)** XMPHYSPGDD0I3 (ModPhy Sus Well Power Gate Disable for D0I3) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
22	0h	RW	**XMPHYSPGDRTD3 (XMPHYSPGDRTD3)** XMPHYSPGDRTD3 (ModPhy Sus Well Power Gate Disable for RTD3) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
21:18	Bh	RW	**XD3RTCPTTM (XD3RTCPTTM)** XD3RTCPTTM (D3 RTC Port Timer Tick Multiplier) This register will be the multiplication factor for determining SSIC Wake Detection Frequency and RXDET based on the XD3RTCPTTC value. If XD3RTCPTTC is 9h and this register is Bh, frequency for RXDET and SSIC H8EXIT detection while MODPHY SUS Power gating is enabled would be 99ms.
17	0h	RW	**U3 LFPS Periodic Sampling ON Time Control (U3_LFPS_PRDC_SAMPLING_ON_TIME_CTRL)** This field controls the ON time for the LFPS periodic sampling for USB3/SSIC ports. 0 ON time is 2 rtc clocks 1 ON time is 3 rtc clocks Note: This field is ignored if USB3/SSIC PHY SUS Well Power Gating is enabled.
16	1h	RW	**AON LFPS Detector Enable Mode (AON_LFPS_DETECTOR_EN_MODE)** 1 - Allow the LFSP Detector in AON to own LFPS detection when the port is in PS3 for U2/U3 - not RxD regardless of port ownership. 0 - Allow the LFPS Detector in AON to own the LFPS detection only when the AON owns the port and in U2/U3 - not RxD

Bit Range	Default	Access	Field Name and Description
15:8	FFh	RW	**SS U3 LFPS Detection Threshold (SS_U3_LFPS_DETECTION_THRESHOLD)** This field controls the threshold used to determine when a valid U3 Wake is detected through when using the unfiltered LFPS source. The value on this field will reflect the binary count required to have been detected on the counter being clocked by the unfiltered lfps source to result in a valid U3 wake detection.
7:4	9h	RW	**SS_U3_LFPS_PRDC_SAMPLING_OFFTIME_CTRL (SS_U3_LFPS_PRDC_ SAMPLING_OFFTIME_CTRL)** This field controls the OFF time for the LFPS periodic sampling for USB3 Ports 0x0 periodic sampling is disabled. 0x1 OFF time is 1ms 0x2 OFF time is 2ms 0xF OFF time is 15ms The ON Time is determined by the amount of time required to reliably determine if there is a valid LFPS and is HW implementation specific. A speed up mode shall be implemented where this field is in units of us. i.e. 0x1 = 1 us OFF time, 0x2 = 2 us OFF time, etc.
3	0h	RW	**PS3 LFPS Source Select (PS3_LFPS_SRC_SEL)** 0 LFPS Source is unfiltered 1 LFPS Source is filtered (Rx-Elec-Idle) LFPS Source is Rx-Elec-Idle for any non PS3 state.

Bit Range	Default	Access	Field Name and Description
2	1h	RW	**XHCI Engine Autonomous Power Gate Exit Reset Policy (XHC_AUTO_PWRGATE_EXITRST_POLICY)** Controls when the xHCI engine is brought out of reset due to a power ungate. 0 Engine is brought out of reset when D3 to D0 is triggered. This allows for a quick power up sequence while leaving the virtual PCIe LTSSM in L23 is power ungate is not due to D3 to D0. 1 Engine is brought out of reset along with the rest of the IP. This is required for PMC save/restore flow.
1	0h	RW	**USB2 Port Wake Unit Coupling Policy (USB2_PORT_WAKE_COUPLING_POLICY)** Controls the trigger for USB2 Port Wake Units to initiate Port Level Power Off Preparation. 0 RTD3 triggered 1 - Port Triggered when in L1, L2 or Disabled, Disconnected
0	0h	RW	**USB3 Port Wake Unit Coupling Policy (USB3_PORT_WAKE_COUPLING_POLICY)** Controls the trigger for USB3 Port Wake Units to initiate Port Level Power Off Preparation. 0 - RTD3 Triggered 1 - Port Triggered when in PS3 due to RxDetect, U3, U2 or Disabled

HOST_CTRL_MISC_REG (HOST_CTRL_MISC_REG) – Offset 80b0

Bit Range	Default	Access	Field Name and Description
31	0b	RW	**USB2_LTRUPDT_DIS (USB2_LTRUPDT_DIS)**

Bit Range	Default	Access	Field Name and Description
30	0b	RW	**USB2 Line State Debounce During Port Reset Policy (USB2_LINE_STATE_DEBOUNCE_DURING_PORT_RESET_POLICY)** This register controls how the debounce is enforced during the Port Reset phase. 0 do not enable the line state debounce during port reset. 1 enable the line state debounce during port reset.
29	0b	RW	**TTE PEXE Credit Fix Disable (TTE_PEXE_CREDIT_FIX_DISABLE)** When set, it disables a fix implemented to re-deem PEXE credits when a port is disconnected
28	0b	RW	**TTE Scheduling policy (TTE_SCHEDULING_POLICY)** This register controls a fix made to prevent over-scheduling by not account for 188B in each uFrame. Setting this bit will disable the fix and allow for over-scheduling.
27	0b	RW	**USB3 ITP Delta Timer Source Select (USB3_ITP_DELTA_TIMER_SOURCE_SELECT)** This register selects the source for the delta timer tracking used for ITP generation. 0 the source is a 16.666 ns tick generated from a crystal reference clock 1 - the source is a 16.666 ns tick generated from the aux_cclk. This field needs to remain in sync with Frame Timer Source Select to ensure the are both set or both cleared. There is no support for any other combination.
26	0b	RW	**Frame Timer Source Select (FRAME_TIMER_SOURCE_SELECT)** This register controls the source for the frame timer. 0 the source for the frame timer is a crystal reference clock 1 the source for the frame timer is the aux_cclk.

Bit Range	Default	Access	Field Name and Description
25	0b	RW	**uFrame Masking Enable (UFRAME_MASKING_ENABLE)** If set, enables the uFrame tick to be masked due to ports being in U3/NC. This controls a fix made to disable the auto masking of uFrame tick due to port state w/o any pipeline idle condition. When cleared, we rely on gating of frame timer due to proper port state and idleness tracking from the pipeline.
24	0b	RW	**Late FID Check Disable (LATE_FID_CHECK_DISABLE)** This register disables the Late FID Check performed when starting an ISOCH stream.
23:20	-	-	**Reserved**
19	0h	RW	**USB2 Resume Cx Inhibit Disable (USB2_RESUME_CX_INHIBIT_DISABLE)** Controls if USB2 L1 Resume is allowed to contribute to DMA Active which will inhibit Cx state. 0 USB2 L1 Resume is allowed to inhibit Cx via DMA Active 1 USB2 L1 Resume is NOT allowed to inhibit Cx via DMA Active When cleared, Cx will only be inhibited when the DMA traffic for the port begins.
18	0h	RW	**(LATE_FID_TTE_DIS)** Late FID TTE Disable 0: Late Frame ID Check is enabled for TTE Endpoints 1: Late Frame ID Check is disabled for TTE Endpoints
17	0h	RW	**Late FID uframe Check Disable (LATE_FID_UFRAME_CHK_DIS)** 0 Frame ID Match only asserts in uframe 7 for non-TTE Endpoints Frame before match 1 Frame ID Match can assert in any uframe
16	1h	RW	**Late FID Extra Interval (LATE_FID_EXTRA_INTER)** This register controls the extra number of intervals added onto the advancing of late FID check escentially a bias used to correct for possible errors in implementation

Bit Range	Default	Access	Field Name and Description
15:0	037Fh	RW	**Valid Isoch Scheduling Range (VALID_ISOCH_SCHEDULING_RANGE)** This register defines the window in miliseconds from the current Frame that will be considered for scheduling in an upcoming Frame. Anything scheduled outside of this window will be considered as late and will trigger the Missed Service Error.

SSPE_REG (SSPE_REG) – Offset 80b8

Bit Range	Default	Access	Field Name and Description
30:10	-	-	**Reserved**
9:0	0h	RW	**SSPE_REG (SSPE_REG)**

AUX Power Management Control (AUX_CTRL_REG1) – Offset 80e0

Bit Range	Default	Access	Field Name and Description
31	1b	RW	**D3 Hot function enable register (D3_HOT_FXN_EN)** This bit is from pin input which is set 1. But we allow software to alter it if it is needed. 1: D3 hot enabled 0: D3 hot not abled.
30	0b	RW	**Allow L1 Core Clock Gating (ALL_L1_CORE_CG)** When set to 1 allows core clock being gated during L1 state.
29	0b	RW	**Allow Engine PHY Status Extension (AL_EP_SEXT)** When set to 1 allows the engine to extend PHY status of PCIe PIPE for one more cycle. This is due to the fact that our rate change function has a potential of not being able to sample the phystatus signal.

Bit Range	Default	Access	Field Name and Description
28	0b	RW	**Allow Engine PCIe Rate Change Passing (ALL_EP_RCP)** When set to 1 allows the engine to pass PCIe rate change signal as it is from PCIe core to PCIe PHY.
27	0b	RW	**Allow Engine PERST Fundamental Reset (AL_PERST_FRST)** When set to 1 allow engine to treat PERST# as a foundamental reset
26	0b	RW	**Overwrite PCIe P2 to P1 (OVR_PCIE_P2_P1)** When set to 1 will overwrite a PCIe powerdown state of P2 to P1.
25	0b	RW	**Set Internal SSV 1 (SET_ISSV_1)** When set to 1 set the internal SSV to 1.
24	0b	RW	**Clear Internal SSV 0 (CLR_ISSV_0)** When set to 1 clear the internal SSV to 0.
23	1b	RW	**Enable save_restore_enable SW Loading (EN_SRE_SW_LD)** This is a bit that enables the save_restore_enable signal being loaded when a software command has set Save bit. This is a debug function.
22	-	-	**Reserved**
21	0b	RW	**Force save_restore 1 (FORCE_SR1)** When set to 1, it will force the save_restore flag to 1. This flag is an bit to ensure that we have masked the update during low power state. If software write this bit to 1, it must write it to 0 in order to resume the normal save and restore function.
20	-	-	**Reserved**
19	0b	RW	**cfg iob drivestrength[1] (CIDS1)**
18	0b	RW	**cfg iob drivestrength[0] (CIDS0)**
17	0b	RW	**cfg_dis_arc_RXDP3 (cfg_dis_arc_RXDP3)** When set to '1' DIsables arc to RXDET_p3 on disc from U2P3/U3

Bit Range	Default	Access	Field Name and Description
16	1b	RW	**cfg clk gate dis (CCGD)**
15	1b	RW	**Enable CFG RXDET P3 (EN_CFG_RDP3)** When set to '1' enable cfg rxdet p3
14	0b	RW	**Enable CFG PIPE Reset (EN_CFG_PIPE_RST)** When set to '1' enable cfg pipe rst
13	1b	RW	**Enable Filter TX Idle (EN_FILT_TX_IDLE)** When set to 1 enables a filter function to TX electrical idle signal at PCie PIPE. We have a filter that will set TXelecidle signal of PCIe PIPE to 1 whenever we are in isolation state or power down transition states.
12	1b	RW	**Enable Host Engine Generate PME (EN_HE_GEN_PME)** This is a global switch to whether or not eable this host engine to generate PME message.
11	1b	RW	**Enable Isolation (EN_ISOL)** When set to '1' enable isolation
10	1b	RW	**Enable L1 Caused P2 Overwrite (EN_L1_P2_OVR)** Set 1 to enable a new feature. This new feature is designed to use L1 as a state to identify whether we should do P2 Overwrite or not. We used to use P1 state to identify whether or not to invoke P2 overwrite function.
9	0b	RW	**Enable Core Clock Gating (EN_CORE_CG)** When set to '1' disable core clock gating based on low power state entered
8	0b	RW	**Enable PHY Status Timeout (EN_PHY_STS_TO)** When set to '1' enable PHY status timeout function which is designed to cover the PCIePHY issue that we may have not able to detect the PHY status toggle.
7	1b	RW	**Ignore aux_pm_en PCIe Core (IGN_APE_PC)** When set to '1' ignore the aux_pm_en reg from PCIe core to continue the remote wake/clock switching support
6	0b	RW	**Enable P2 Overwrite P1 (EN_P2_OVR_P1)** When set to '1' enable P2 overwrite P1 when PCIe core has indicated the transition from P0 to P1. This is to enable entering the even lower power state.

Bit Range	Default	Access	Field Name and Description
5	1b	RW	**Enable P2 Remote Wake (EN_P2_REM_WAKE)** When set 1 '1' enable the remote wake function by allowing P2 clock/switching and P2 entering
4:1	0h	RW	**Forced PM State (FORCED_PM_STATE)**
0	0b	RW	**Initiate Force PM State (INIT_FPMS)** When set to '1' force PM state to go to the state indicated in bit 4:1

Global Time Sync Control (GLOBAL_TIME_SYNC_CTRL_REG) – Offset 8e14

Bit Range	Default	Access	Field Name and Description
30:1	-	-	**Reserved**
0	0h	RW/1S	**Always Running Time (ART) Capture Initiate (TIME_STAMP_CNTR_CAPTURE_INITIATE)** SW sets this bit to initiate a time capture. Once the time capture is complete and the time values are valid in the Local and Global time capture registers, HW clears the bit.

Microframe Time (Local Time) (MICROFRAME_TIME_REG) – Offset 8e18

Bit Range	Default	Access	Field Name and Description
30	-	-	**Reserved**
29:16	0h	RO	**Captured Frame List Current Index/Frame Number (CMFI)** The value in this register is updated in response to sample_now signal. Bits [29:16] reflect state of bits [13:0] of FRINDEX

Bit Range	Default	Access	Field Name and Description
15:13	-	-	**Reserved**
12:0	0000h	RO	**Captured Micro-frame BLIF (CMFB)** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done via Bus Interval Adjust (BIA).

Always Running Time (ART) Low (ALWAYS_RUNNING_TIME_LOW) – Offset 8e20

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO	**Global Time Value (Low) (GLOBAL_TIME_LOW)**

Always Running Time (ART) High (ALWAYS_RUNNING_TIME_HIGH) – Offset 8e24

Bit Range	Default	Access	Field Name and Description
31:0	0h	RO	**Global Time Value (High) (GLOBAL_TIME_HI)**

Dublin LFPS Register 4 (HOST_CTRL_SSP_LFPS_REG4) – Offset 8e7c

Bit Range	Default	Access	Field Name and Description
30:24	-	-	**Reserved**
23:17	3ch	RW	**SCD_LFPS_TIMEOUT (SCD_LFPS_TIMEOUT)**
16:14	2h	RW	**TX_SCD_COUNT (SCD_TX_COUNT)**
13:0	-	-	**Reserved**

Host Ctrl USB3 Soft Error Count Register 1 (HOST_CTRL_USB3_ERR_COUNT_REG1) – Offset 8ebc

This register is updated by hardware and cleared by software
Port 1...N: (8EBCh + (USB3_NPORT - 1)*4h)

Bit Range	Default	Access	Field Name and Description
30:16	-	-	**Reserved**
15:0	0000h	RW	**USB Soft Error Count (cfg_usb3_soft_error_cnt)** This register will keep count of soft errors on SS and SSP ports for a particular port. This register is read/write by software and it can be cleared by software by writing to it. Once reached to maximum value, it will stop incrementing.