Intel® 400 Series Chipset Family Platform Controller Hub

GPIO Implementation Summary

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Signal Name	GPIO	Power Well	Voltage Tolerance	Native Function 1	Native Dir 1	Native Function 2	Native Dir 2	Native Function 3	Native Dir 3	Native Function 4	Native Dir 4	Default	Strap	Pin Strap Termination	NMI/SMI Capable	Input Deglitch	Output Power Sequence Deglitch	Pin State During Reset	Pin State Immediately After Reset	Notes
Primary Well Group A (Per-Group 1.8 V or 3.3 V)																				
GPP_A0 / RCIN# / ESPI_ALERT1#	GPP_A0	VCCPGPPA	1.8 V or 3.3 V	RCIN#	in			ESPI_ALERT1#	in			Native F1 / Native F3 / GP-In			no	no	yes(1)	Native F1: Z / Native F3: PU / GPIO: Z	Native F1: Z / Native F3: PU / GPIO: Z	Native F1 if eSPI or LPC pin strap = 0 (LPC Mode). Else GPI in SKU supporting 1 eSPI chip select (CS) signal and Native F3 in SKU supporting 2 eSPI CS signals.
GPP_A1 / LAD0 / ESPI_IO0	GPP_A1	VCCPGPPA	1.8 V or 3.3 V	LAD0	inout			ESPI_IO0	inout			Native F1 / Native F3			no	no	yes(1)	Native F1: PU / Native F3: PU	Native F1: PU / Native F3: PU	Native F1 if if eSPI or LPC pin strap = 0 (LPC Mode), else Native F3
GPP_A2 / LAD1 / ESPI_IO1	GPP_A2	VCCPGPPA	1.8 V or 3.3 V	LAD1	inout			ESPI_IO1	inout			Native F1 / Native F3			no	no	yes(1)	Native F1: PU / Native F3: PU	Native F1: PU / Native F3: PU	Native F1 if if eSPI or LPC pin strap = 0 (LPC Mode), else Native F3
GPP_A3 / LAD2 / ESPI_IO2	GPP_A3	VCCPGPPA	1.8 V or 3.3 V	LAD2	inout			ESPI_IO2	inout			Native F1 / Native F3			no	no	yes(1)	Native F1: PU / Native F3: PU	Native F1: PU / Native F3: PU	Native F1 if if eSPI or LPC pin strap = 0 (LPC Mode), else Native F3
GPP_A4 / LAD3 / ESPI_IO3	GPP_A4	VCCPGPPA	1.8 V or 3.3 V	LAD3	inout			ESPI_IO3	inout			Native F1 / Native F3			no	no	yes(1)	Native F1: PU / Native F3: PU	Native F1: PU / Native F3: PU	Native F1 if if eSPI or LPC pin strap = 0 (LPC Mode), else Native F3
GPP_A5 / LFRAME# / ESPI_CS0#	GPP_A5	VCCPGPPA	1.8 V or 3.3 V	LFRAME#	out			ESPI_CS0#	out			Native F1 / Native F3			no	no	yes(2)	Native F1: H / Native F3: PU	Native F1: H / Native F3: H	Native F1 if if eSPI or LPC pin strap = 0 (LPC Mode), else Native F3
GPP_A6 / SERIRQ / ESPI_CS1#	GPP_A6	VCCPGPPA	1.8 V or 3.3 V	SERIRQ	inout			ESPI_CS1#	out			Native F1 / Native F3 / GP-In			no	no	yes(1)	Native F1: Z / Native F3: PU / GPIO: Z	Native F1: Z / Native F3: H / GPIO: Z	Native F1 if eSPI or LPC pin strap = 0 (LPC Mode). Else GPI in SKU supporting 1 eSPI chip select (CS) signal and Native F3 in SKU supporting 2 eSPI CS signals.
GPP_A7 / PIRQA# / ESPI_ALERT0#	GPP_A7	VCCPGPPA	1.8 V or 3.3 V	PIRQA#	iod			ESPI_ALERT0#	in			Native F1 / Native F3 / GP-In			no	no	yes(1)	Native F1: Z / Native F3: PU / GPIO: Z	Native F1: Z / Native F3: PU / GPIO: Z	Native F1 if eSPI or LPC pin strap = 0 (LPC Mode). Else GPI in SKU supporting 1 eSPI chip select (CS) signal and Native F3 in SKU supporting 2 eSPI CS signals.
GPP_A8 / CLKRUN#	GPP_A8	VCCPGPPA	1.8 V or 3.3 V	CLKRUN#	iod							Native F1 / GP-In			no	no	yes(1)	Native F1: Z / GPIO: Z	Native F1: Z / GPIO: Z	Native F1 if if eSPI or LPC pin strap = 0 (LPC Mode), else GP-In
GPP_A9 / CLKOUT_LPC0 / ESPI_CLK	GPP_A9	VCCPGPPA	1.8 V or 3.3 V	CLKOUT_LPC0	out			ESPI_CLK	out			Native F1 / Native F3			no	no	yes(1)	Native F1: T / Native F3: PD	Native F1: T / Native F3: L	Native F1 if if eSPI or LPC pin strap = 0 (LPC Mode), else Native F3
GPP_A10 / CLKOUT_LPC1	GPP_A10	VCCPGPPA	1.8 V or 3.3 V	CLKOUT_LPC1	out							Native F1/GP-In			no	no	yes(1)	Native F1: T / GPIO: Z	Native F1: T / GPIO: Z	Native F1 if eSPI or LPC pin strap = 0 (LPC Mode), else GP-In.
GPP_A11 / PME# / SD_VDD2_PWR_EN#	GPP_A11	VCCPGPPA	1.8 V or 3.3 V	PME#	iod	SD_VDD2_PWR_EN#	out					Native F1/GP-In			no	no	yes(1)	Native F1: PU / GPIO: Z	Native F1: PU / GPIO: Z	Native F1 if eSPI or LPC pin strap = 0 (LPC Mode), else GP-In.
GPP_A12 / BM_BUSY# / ISH_GP6 / SX_EXIT_	GPP_A12	VCCPGPPA	1.8 V or 3.3 V	BM_BUSY#	in	ISH_GP6	inout	SX_EXIT_HOLDOFF#	in			GP-In			no	no	yes(1)	Z	Z	
GPP_A13 / SUSWARN# / SUSPWRDNACK	GPP_A13	VCCPGPPA	1.8 V or 3.3 V	SUSWARN# / SUSPWRDNACK	out							Native F1/GP-In			no	no	yes(2)	Native F1: L / GPIO: Z	Native F1: L / GPIO: Z	Native F1 if eSPI or LPC pin strap = 0 (LPC Mode), else GP-In.
GPP_A14 / SUS_STAT# / ESPI_RESET#	GPP_A14	VCCPGPPA	1.8 V or 3.3 V	SUS_STAT#	out			ESPI_RESET#	out			Native F1 / Native F3			no	no	yes(2)	Native F1: L / Native F3: L	Native F1: note / Native F3: H	Native F1 if eSPI or LPC pin strap = 0 (LPC Mode), else Native F3. SUS_STAT# state After Reset: L, and then H after PCH_PWROK asserts
GPP_A15 / SUSACK#	GPP_A15	VCCPGPPA	1.8 V or 3.3 V	SUSACK#	in							Native F1/GP-In			no	no	yes(1)	Native F1: PU / GPIO: Z	Native F1: PU / GPIO: Z	Native F1 if eSPI or LPC pin strap = 0 (LPC Mode), else GP-In.
GPP_A16 / CLKOUT_48	GPP_A16	VCCPGPPA	1.8 V or 3.3 V	CLKOUT_48	out							Native F1/GP-In			no	no	yes(1)	Native F1: T / GPIO: Z	Native F1: T / GPIO: Z	Native F1 if CLKOUT_48 Mode Configuration soft strap = 0 , else GP-In
GPP_A17 / SD_VDD1_PWR_EN# / ISH_GP7	GPP_A17	VCCPGPPA	1.8 V or 3.3 V	SD_VDD1_PWR_EN#	out	ISH_GP7	inout					GP-In			no	no	yes(1)	Z	Z	
GPP_A18 / ISH_GP0	GPP_A18	VCCPGPPA	1.8 V or 3.3 V	ISH_GP0	inout							GP-In			no	no	yes(1)	Z	Z	
GPP_A19 / ISH_GP1	GPP_A19	VCCPGPPA	1.8 V or 3.3 V	ISH_GP1	inout							GP-In			no	no	yes(1)	Z	Z	
GPP_A20 / ISH_GP2	GPP_A20	VCCPGPPA	1.8 V or 3.3 V	ISH_GP2	inout							GP-In			no	no	yes(1)	Z	Z	
GPP_A21 / ISH_GP3	GPP_A21	VCCPGPPA	1.8 V or 3.3 V	ISH_GP3	inout							GP-In			no	no	yes(1)	Z	Z	
GPP_A22 / ISH_GP4	GPP_A22	VCCPGPPA	1.8 V or 3.3 V	ISH_GP4	inout							GP-In			no	no	yes(1)	Z	Z	
GPP_A23 / ISH_GP5	GPP_A23	VCCPGPPA	1.8 V or 3.3 V	ISH_GP5	inout							GP-In			no	no	yes(1)	Z	Z	
Primary Well Group B (Per-Group 1.8 V or 3.3 V)																				
GPP_B0 / GSPI0_CS1#	GPP_B0	VCCPGPPBC	1.8 V or 3.3 V	GSPI0_CS1#	out							GP-In			no	no	yes(1)	Z	Z	
GPP_B1 / GSPI1_CS1# / TIME_SYNC1	GPP_B1	VCCPGPPBC	1.8 V or 3.3 V	GSPI1_CS1#	out	TIME_SYNC1	inout					GP-In			no	no	yes(1)	Z	Z	
GPP_B2 / VRALERT#	GPP_B2	VCCPGPPBC	1.8 V or 3.3 V	VRALERT#	in							GP-In			no	no	yes(1)	Z	Z	
GPP_B3 / CPU_GP2	GPP_B3	VCCPGPPBC	1.8 V or 3.3 V	CPU_GP2	in							GP-In			no	no	yes(1)	Z	Z	
GPP_B4 / CPU_GP3	GPP_B4	VCCPGPPBC	1.8 V or 3.3 V	CPU_GP3	in							GP-In			no	no	yes(1)	Z	Z	
GPP_B5 / SRCCLKREQ0#	GPP_B5	VCCPGPPBC	1.8 V or 3.3 V	SRCCLKREQ0#	iod							GP-In			no	no	yes(1)	Z	Z	

Signal Name	GPIO	Power Well	Voltage Tolerance	Native Function 1	Native Dir 1	Native Function 2	Native Dir 2	Native Function 3	Native Dir 3	Native Function 4	Native Dir 4	Default	Strap	Pin Strap Termination	NMI/SMI Capable	Input Deglitch	Output Power Sequence Deglitch	Pin State During Reset	Pin State Immediately After Reset	Notes
GPP_B6 / SRCCLKREQ1#	GPP_B6	VCCPGPPBC	1.8 V or 3.3 V	SRCCLKREQ1#	iod							GP-In			no	no	yes(1)	Z	Z	
GPP_B7 / SRCCLKREQ2#	GPP_B7	VCCPGPPBC	1.8 V or 3.3 V	SRCCLKREQ2#	iod							GP-In			no	no	yes(1)	Z	Z	
GPP_B8 / SRCCLKREQ3#	GPP_B8	VCCPGPPBC	1.8 V or 3.3 V	SRCCLKREQ3#	iod							GP-In			no	no	yes(1)	Z	Z	
GPP_B9 / SRCCLKREQ4#	GPP_B9	VCCPGPPBC	1.8 V or 3.3 V	SRCCLKREQ4#	iod							GP-In			no	no	yes(1)	Z	Z	
GPP_B10 / SRCCLKREQ5#	GPP_B10	VCCPGPPBC	1.8 V or 3.3 V	SRCCLKREQ5#	iod							GP-In			no	no	yes(1)	Z	Z	
GPP_B11 / I2S_MCLK	GPP_B11	VCCPGPPBC	1.8 V or 3.3 V	I2S_MCLK	out							GP-In			no	no	yes(1)	Z	Z	
GPP_B12 / SLP_S0#	GPP_B12	VCCPGPPBC	1.8 V or 3.3 V	SLP_S0#	out							Native F1			no	no	yes(1)	H (Refer note)	H	The During Reset Pin State of this GPIO is H via a ~20 k pull-up to 3.3 V independent of soft strap assigned pad voltage. A 1.8 V device connected to this GPIO must be capable of taking ~20 kohm pull-up to 3.3V.
GPP_B13 / PLTRST#	GPP_B13	VCCPGPPBC	1.8 V or 3.3 V	PLTRST#	out							Native F1			no	no	yes(2)	L	H	
GPP_B14 / SPKR	GPP_B14	VCCPGPPBC	1.8 V or 3.3 V	SPKR	out							GP-Out	Top Swap Override	20K PD	NMI / SMI	no	no	PD	L	Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% Pull-down is disabled after PCH_PWROK is high.
GPP_B15 / GSPI0_CS0#	GPP_B15	VCCPGPPBC	1.8 V or 3.3 V	GSPI0_CS0#	out							GP-In			no	no	yes(1)	Z	Z	
GPP_B16 / GSPI0_CLK	GPP_B16	VCCPGPPBC	1.8 V or 3.3 V	GSPI0_CLK	out							GP-In			no	no	yes(1)	Z	Z	
GPP_B17 / GSPI0_MISO	GPP_B17	VCCPGPPBC	1.8 V or 3.3 V	GSPI0_MISO	in							GP-In			no	no	yes(1)	Z	Z	
GPP_B18 / GSPI0_MOSI	GPP_B18	VCCPGPPBC	1.8 V or 3.3 V	GSPI0_MOSI	out							GP-Out	No Reboot	20K PD	no	no	no	PD	L	Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% Pull-down is disabled after PCH_PWROK is high.
GPP_B19 / GSPI1_CS0#	GPP_B19	VCCPGPPBC	1.8 V or 3.3 V	GSPI1_CS0#	out							GP-In			no	no	yes(1)	Z	Z	
GPP_B20 / GSPI1_CLK	GPP_B20	VCCPGPPBC	1.8 V or 3.3 V	GSPI1_CLK	out							GP-In			NMI / SMI	no	yes(1)	Z	Z	
GPP_B21 / GSPI1_MISO	GPP_B21	VCCPGPPBC	1.8 V or 3.3 V	GSPI1_MISO	in							GP-In			no	no	yes(1)	Z	Z	
GPP_B22 / GSPI1_MOSI	GPP_B22	VCCPGPPBC	1.8 V or 3.3 V	GSPI1_MOSI	out							GP-Out	Boot BIOS Strap Bit	20K PD	no	no	no	PD	L	Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% Pull-down is disabled after PCH_PWROK is high.
GPP_B23 / SML1ALERT# / PCHHOT#	GPP_B23	VCCPGPPBC	1.8 V or 3.3 V	SML1ALERT#	iod	PCHHOT#	od					GP-Out	Intel® DCIOOB Enable	20K PD	NMI / SMI	yes	no	PD	L	Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts. Note: When used as PCHHOT# and strap low, a 150 kohm weak board pull-up is recommended to ensure it does not override the internal pull-down strap sampling.
Primary Well Group C (Per-Group 1.8 V or 3.3 V)																				
GPP_C0 / SMBCLK	GPP_C0	VCCPGPPBC	1.8 V or 3.3 V	SMBCLK	iod							Native F1			no	yes	yes(1)	Z	Z	
GPP_C1 / SMBDATA	GPP_C1	VCCPGPPBC	1.8 V or 3.3 V	SMBDATA	iod							Native F1			no	yes	yes(1)	Z	Z	
GPP_C2 / SMBALERT#	GPP_C2	VCCPGPPBC	1.8 V or 3.3 V	SMBALERT#	iod							Native F1/GP-Out	TLS Confidentiality	20K PD	no	yes	no	Native F1: PD / GPIO: PD	Native F1: L / GPIO: L	Native F1 if intel® SMBus ASD Mode Configuration soft strap = 1, else GP-Out; Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts.
GPP_C3 / SML0CLK	GPP_C3	VCCPGPPBC	1.8 V or 3.3 V	SML0CLK	iod							Native F1			no	yes	yes(1)	Z	Z	
GPP_C4 / SML0DATA	GPP_C4	VCCPGPPBC	1.8 V or 3.3 V	SML0DATA	iod							Native F1			no	yes	yes(1)	Z	Z	
GPP_C5 / SML0ALERT#	GPP_C5	VCCPGPPBC	1.8 V or 3.3 V	SML0ALERT#	iod							GP-Out	eSPI or LPC	20K PD	no	yes	no	PD	L	Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts.
GPP_C6 / SML1CLK	GPP_C6	VCCPGPPBC	1.8 V or 3.3 V	SML1CLK	iod							GP-In			no	yes	yes(1)	Z	Z	
GPP_C7 / SML1DATA	GPP_C7	VCCPGPPBC	1.8 V or 3.3 V	SML1DATA	iod							GP-In			no	yes	yes(1)	Z	Z	
GPP_C8 / UART0A_RXD	GPP_C8	VCCPGPPBC	1.8 V or 3.3 V	UART0_RXD	in							GP-In			no	no	yes(1)	Z	Z	
GPP_C9 / UART0A_TXD	GPP_C9	VCCPGPPBC	1.8 V or 3.3 V	UART0_TXD	out							GP-In			no	no	yes(1)	Z	Z	
GPP_C10 / UART0A_RTS#	GPP_C10	VCCPGPPBC	1.8 V or 3.3 V	UART0_RTS#	out							GP-In			no	no	yes(1)	Z	Z	

Signal Name	GPIO	Power Well	Voltage Tolerance	Native Function 1	Native Dir 1	Native Function 2	Native Dir 2	Native Function 3	Native Dir 3	Native Function 4	Native Dir 4	Default	Strap	Pin Strap Termination	NMI/SMI Capable	Input Deglitch	Output Power Sequence Deglitch	Pin State During Reset	Pin State Immediately After Reset	Notes
GPP_C11 / UART0A_CTS#	GPP_C11	VCCPGPPBC	1.8 V or 3.3 V	UART0_CTS#	in							GP-In			no	no	yes(1)	Z	Z	
GPP_C12 / UART1_RXD / ISH_UART1_RXD	GPP_C12	VCCPGPPBC	1.8 V or 3.3 V	UART1_RXD	in	ISH_UART1_RXD	in					GP-In			no	no	yes(1)	Z	Z	
GPP_C13 / UART1_TXD / ISH_UART1_TXD	GPP_C13	VCCPGPPBC	1.8 V or 3.3 V	UART1_TXD	out	ISH_UART1_TXD	out					GP-In			no	no	yes(1)	Z	Z	
GPP_C14 / UART1_RTS# / ISH_UART1_RTS#	GPP_C14	VCCPGPPBC	1.8 V or 3.3 V	UART1_RTS#	out	ISH_UART1_RTS#	out					GP-In			no	no	yes(1)	Z	Z	
GPP_C15 / UART1_CTS# / ISH_UART1_CTS#	GPP_C15	VCCPGPPBC	1.8 V or 3.3 V	UART1_CTS#	in	ISH_UART1_CTS#	in					GP-In			no	no	yes(1)	Z	Z	
GPP_C16 / I2C0_SDA	GPP_C16	VCCPGPPBC	1.8 V or 3.3 V	I2C0_SDA	od							GP-In			no	yes	yes(1)	Z	Z	
GPP_C17 / I2C0_SCL	GPP_C17	VCCPGPPBC	1.8 V or 3.3 V	I2C0_SCL	od							GP-In			no	yes	yes(1)	Z	Z	
GPP_C18 / I2C1_SDA	GPP_C18	VCCPGPPBC	1.8 V or 3.3 V	I2C1_SDA	od							GP-In			no	yes	yes(1)	Z	Z	
GPP_C19 / I2C1_SCL	GPP_C19	VCCPGPPBC	1.8 V or 3.3 V	I2C1_SCL	od							GP-In			no	yes	yes(1)	Z	Z	
GPP_C20 / UART2_RXD	GPP_C20	VCCPGPPBC	1.8 V or 3.3 V	UART2_RXD	in							GP-In			no	no	yes(1)	Z	Z	
GPP_C21 / UART2_TXD	GPP_C21	VCCPGPPBC	1.8 V or 3.3 V	UART2_TXD	out							GP-In			no	no	yes(1)	Z	Z	
GPP_C22 / UART2_RTS#	GPP_C22	VCCPGPPBC	1.8 V or 3.3 V	UART2_RTS#	out							GP-In			NMI / SMI	no	yes(1)	Z	Z	
GPP_C23 / UART2_CTS#	GPP_C23	VCCPGPPBC	1.8 V or 3.3 V	UART2_CTS#	in							GP-In			NMI / SMI	no	yes(1)	Z	Z	
Primary Well Group D (Per-Group 1.8 V or 3.3 V)																				
GPP_D0 / SPI1_CS# / SBK0 / BK0	GPP_D0	VCCPGPPD	1.8 V or 3.3 V	SPI1_CS#	out			SBK0	out	BK0	out	GP-In			NMI / SMI	no	yes(1)	Z	Z	
GPP_D1 / SPI1_CLK / SBK1 / BK1	GPP_D1	VCCPGPPD	1.8 V or 3.3 V	SPI1_CLK	out			SBK1	out	BK1	out	GP-In			NMI / SMI	no	yes(1)	Z	Z	
GPP_D2 / SPI1_MISO / SBK2 / BK2	GPP_D2	VCCPGPPD	1.8 V or 3.3 V	SPI1_MISO	inout			SBK2	out	BK2	out	GP-In			NMI / SMI	no	yes(1)	Z	Z	
GPP_D3 / SPI1_MOSI / SBK3 / BK3	GPP_D3	VCCPGPPD	1.8 V or 3.3 V	SPI1_MOSI	inout			SBK3	out	BK3	out	GP-In			NMI / SMI	no	yes(1)	Z	Z	
GPP_D4 / ISH_I2C2_SDA / I2C3_SDA / SBK4	GPP_D4	VCCPGPPD	1.8 V or 3.3 V	ISH_I2C2_SDA	iod	I2C3_SDA	iod	SBK4	out	BK4	out	GP-In			NMI / SMI	Yes	yes(1)	Z	Z	
GPP_D5 / I2S2_SFRM / CNV_RF_RESET#	GPP_D5	VCCPGPPD	1.8 V or 3.3 V	I2S2_SFRM	inout			CNV_RF_RESET#	out			Native F3			no	no	yes(2)	L	H	
GPP_D6 / I2S2_TXD / MODEM_CLKREQ	GPP_D6	VCCPGPPD	1.8 V or 3.3 V	I2S2_TXD	out			MODEM_CLKREQ	out			Native F3			no	no	yes(1)	Z	H	
GPP_D7 / I2S2_RXD	GPP_D7	VCCPGPPD	1.8 V or 3.3 V	I2S2_RXD	in							GP-In			no	no	yes(1)	Z	Z	
GPP_D8 / I2S2_SCLK	GPP_D8	VCCPGPPD	1.8 V or 3.3 V	I2S2_SCLK	inout							GP-In			no	no	yes(1)	Z	Z	
GPP_D9 / ISH_SPI_CS# / GSPI2_CS0#	GPP_D9	VCCPGPPD	1.8 V or 3.3 V	ISH_SPI_CS#	out			GSPI2_CS0#	out			GP-In			no	no	yes(1)	Z	Z	
GPP_D10 / ISH_SPI_CLK / GSPI2_CLK	GPP_D10	VCCPGPPD	1.8 V or 3.3 V	ISH_SPI_CLK	out			GSPI2_CLK	out			GP-In			no	no	yes(1)	Z	Z	
GPP_D11 / ISH_SPI_MISO / GP_BSSB_CLK /	GPP_D11	VCCPGPPD	1.8 V or 3.3 V	ISH_SPI_MISO	in	GP_BSSB_CLK	in	GSPI2_MISO	in			Native F2			no	no	yes(1)	Z	Z	
GPP_D12 / ISH_SPI_MOSI / GP_BSSB_DI / G	GPP_D12	VCCPGPPD	1.8 V or 3.3 V	ISH_SPI_MOSI	out	GP_BSSB_DI	in	GSPI2_MOSI	out			Native F2			no	no	yes(1)	Z	Z	
GPP_D13 / ISH_UART0_RXD / I2C2_SDA	GPP_D13	VCCPGPPD	1.8 V or 3.3 V	ISH_UART0_RXD	in			I2C2_SDA	iod			GP-In			no	no	yes(1)	Z	Z	
GPP_D14 / ISH_UART0_TXD / I2C2_SCL	GPP_D14	VCCPGPPD	1.8 V or 3.3 V	ISH_UART0_TXD	out			I2C2_SCL	iod			GP-In			no	no	yes(1)	Z	Z	
GPP_D15 / ISH_UART0_RTS# / GSPI2_CS1#	GPP_D15	VCCPGPPD	1.8 V or 3.3 V	ISH_UART0_RTS#	out	GSPI2_CS1#	out			CNV_WFEN	in	GP-In			no	no	yes(1)	Z	Z	
GPP_D16 / ISH_UART0_CTS# / CNV_WCEN	GPP_D16	VCCPGPPD	1.8 V or 3.3 V	ISH_UART0_CTS#	in					CNV_WCEN	in	GP-In			no	no	yes(1)	Z	Z	
GPP_D17 / DMIC_CLK1 / SNDW3_CLK	GPP_D17	VCCPGPPD	1.8 V or 3.3 V	DMIC_CLK1	out	SNDW3_CLK	inout					GP-In			no	no	yes(1)	Z	Z	
GPP_D18 / DMIC_DATA1 / SNDW3_DATA	GPP_D18	VCCPGPPD	1.8 V or 3.3 V	DMIC_DATA1	in	SNDW3_DATA	inout					GP-In			no	no	yes(1)	Z	Z	
GPP_D19 / DMIC_CLK0 / SNDW4_CLK	GPP_D19	VCCPGPPD	1.8 V or 3.3 V	DMIC_CLK0	out	SNDW4_CLK	inout					GP-In			no	no	yes(1)	Z	Z	
GPP_D20 / DMIC_DATA0 / SNDW4_DATA	GPP_D20	VCCPGPPD	1.8 V or 3.3 V	DMIC_DATA0	in	SNDW4_DATA	inout					GP-In			no	no	yes(1)	Z	Z	
GPP_D21 / SPI1_IO2	GPP_D21	VCCPGPPD	1.8 V or 3.3 V	SPI1_IO2	inout							GP-In			no	no	yes(1)	Z	Z	
GPP_D22 / SPI1_IO3	GPP_D22	VCCPGPPD	1.8 V or 3.3 V	SPI1_IO3	inout							GP-In			no	no	yes(1)	Z	Z	
GPP_D23 / ISH_I2C2_SCL / I2C3_SCL	GPP_D23	VCCPGPPD	1.8 V or 3.3 V	ISH_I2C2_SCL	iod	I2C3_SCL	iod					GP-In			no	yes	yes(1)	Z	Z	
Primary Well Group E (Per-Group 1.8 V or 3.3 V)																				
GPP_E0 / SATAXPCIE0 / SATAGP0	GPP_E0	VCCPGPPEF	1.8 V or 3.3 V	SATAXPCIE0	in	SATAGP0	in					Native F1/GP-In			NMI / SMI	no	yes(1)	Native F1: PU / GPIO: Z	Native F1: PU / GPIO: Z	Native F1 if SATA / PCIe GP Select for Port 0 soft strap = 00b or 01b; GP-In if soft strap = 11b. Note: Different Connectors have different polarity for the SATAxPCIe select. Note: Default state is GP-In before soft straps are loaded or in the case the soft straps are invalid

Signal Name	GPIO	Power Well	Voltage Tolerance	Native Function 1	Native Dir 1	Native Function 2	Native Dir 2	Native Function 3	Native Dir 3	Native Function 4	Native Dir 4	Default	Strap	Pin Strap Termination	NMI/SMI Capable	Input Deglitch	Output Power Sequence Deglitch	Pin State During Reset	Pin State Immediately After Reset	Notes
GPP_E1 / SATAXPCIE1 / SATAGP1	GPP_E1	VCCPGPPEF	1.8 V or 3.3 V	SATAXPCIE1	in	SATAGP1	in					Native F1/GP-In			NMI / SMI	no	yes(1)	Native F1: PU / GPIO: Z	Native F1: PU / GPIO: Z	Native F1 if SATA / PCIe GP Select for Port 1 soft strap = 00b or 01b; GP-In if soft strap = 11b. Note: Different Connectors have different polarity for the SATAxPCIe select. Note: Default state is GP-In before soft straps are loaded or in the case the soft straps are invalid
GPP_E2 / SATAXPCIE2 / SATAGP2	GPP_E2	VCCPGPPEF	1.8 V or 3.3 V	SATAXPCIE2	in	SATAGP2	in					Native F1/GP-In			NMI / SMI	no	yes(1)	Native F1: PU / GPIO: Z	Native F1: PU / GPIO: Z	Native F1 if SATA / PCIe GP Select for Port 2 soft strap = 00b or 01b; GP-In if soft strap = 11b. Note: Different Connectors have different polarity for the SATAxPCIe select. Note: Default state is GP-In before soft straps are loaded or in the case the soft straps are invalid
GPP_E3 / CPU_GP0	GPP_E3	VCCPGPPEF	1.8 V or 3.3 V	CPU_GP0	in							GP-In			NMI / SMI	no	yes(1)	Z	Z	
GPP_E4 / SATA_DEVSLP0	GPP_E4	VCCPGPPEF	1.8 V or 3.3 V	SATA_DEVSLP0	od							GP-In			NMI / SMI	no	yes(1)	Z	Z	
GPP_E5 / SATA_DEVSLP1	GPP_E5	VCCPGPPEF	1.8 V or 3.3 V	SATA_DEVSLP1	od							GP-In			NMI / SMI	no	yes(1)	Z	Z	
GPP_E6 / SATA_DEVSLP2	GPP_E6	VCCPGPPEF	1.8 V or 3.3 V	SATA_DEVSLP2	od							GP-In			NMI / SMI	no	yes(1)	Z	Z	
GPP_E7 / CPU_GP1	GPP_E7	VCCPGPPEF	1.8 V or 3.3 V	CPU_GP1	in							GP-In			NMI / SMI	no	yes(1)	Z	Z	
GPP_E8 / SATA_LED#	GPP_E8	VCCPGPPEF	1.8 V or 3.3 V	SATA_LED#	od							GP-In			NMI / SMI	no	yes(1)	Z	Z	
GPP_E9 / USB_OC0#	GPP_E9	VCCPGPPEF	1.8 V or 3.3 V	USB_OC0#	in							GP-In			no	no	yes(1)	Z	Z	
GPP_E10 / USB_OC1#	GPP_E10	VCCPGPPEF	1.8 V or 3.3 V	USB_OC1#	in							GP-In			no	no	yes(1)	Z	Z	
GPP_E11 / USB_OC2#	GPP_E11	VCCPGPPEF	1.8 V or 3.3 V	USB_OC2#	in							GP-In			no	no	yes(1)	Z	Z	
GPP_E12 / USB_OC3#	GPP_E12	VCCPGPPEF	1.8 V or 3.3 V	USB_OC3#	in							GP-In			no	no	yes(1)	Z	Z	
Primary Well Group F (Per-Group 1.8 V or 3.3 V)																				
GPP_F0 / SATAXPCIE3 / SATAGP3	GPP_F0	VCCPGPPEF	1.8 V or 3.3 V	SATAXPCIE3	in	SATAGP3	in					Native F1/GP-In			NMI / SMI	no	yes(1)	Native F1: PU / GPIO: Z	Native F1: PU / GPIO: Z	Native F1 if SATA / PCIe GP Select for Port 3 soft strap = 00b or 01b; GP-In if soft strap = 11b. Note: Different Connectors have different polarity for the SATAxPCIe select. Note: Default state is GP-In before soft straps are loaded or in the case the soft straps are invalid
GPP_F1 / SATAXPCIE4 / SATAGP4	GPP_F1	VCCPGPPEF	1.8 V or 3.3 V	SATAXPCIE4	in	SATAGP4	in					Native F1/GP-In			NMI / SMI	no	yes(1)	Native F1: PU / GPIO: Z	Native F1: PU / GPIO: Z	Native F1 if SATA / PCIe GP Select for Port 4 soft strap = 00b or 01b; GP-In if soft strap = 11b. Note: Different Connectors have different polarity for the SATAxPCIe select. Note: Default state is GP-In before soft straps are loaded or in the case the soft straps are invalid
GPP_F2 / SATAXPCIE5 / SATAGP5	GPP_F2	VCCPGPPEF	1.8 V or 3.3 V	SATAXPCIE5	in	SATAGP5	in					Native F1/GP-In			NMI / SMI	no	yes(1)	Native F1: PU / GPIO: Z	Native F1: PU / GPIO: Z	Native F1 if SATA / PCIe GP Select for Port 5 soft strap = 00b or 01b; GP-In if soft strap = 11b. Note: Different Connectors have different polarity for the SATAxPCIe select. Note: Default state is GP-In before soft straps are loaded or in the case the soft straps are invalid
GPP_F3 / SATAXPCIE6 / SATAGP6	GPP_F3	VCCPGPPEF	1.8 V or 3.3 V	SATAXPCIE6	in	SATAGP6	in					Native F1/GP-In			NMI / SMI	no	yes(1)	Native F1: PU / GPIO: Z	Native F1: PU / GPIO: Z	Native F1 if SATA / PCIe GP Select for Port 6 soft strap = 00b or 01b; GP-In if soft strap = 11b. Note: Different Connectors have different polarity for the SATAxPCIe select. Note: Default state is GP-In before soft straps are loaded or in the case the soft straps are invalid

Signal Name	GPIO	Power Well	Voltage Tolerance	Native Function 1	Native Dir 1	Native Function 2	Native Dir 2	Native Function 3	Native Dir 3	Native Function 4	Native Dir 4	Default	Strap	Pin Strap Termination	NMI/SMI Capable	Input Deglitch	Output Power Sequence Deglitch	Pin State During Reset	Pin State Immediately After Reset	Notes
GPP_F4 / SATAXPCIE7 / SATAGP7	GPP_F4	VCCPGPPEF	1.8 V or 3.3 V	SATAXPCIE7	in	SATAGP7	in					Native F1/GP-In			NMI / SMI	no	yes(1)	Native F1: PU / GPIO: Z	Native F1: PU / GPIO: Z	Native F1 if SATA / PCIe GP Select for Port 7 soft strap = 00b or 01b; GP-In if soft strap = 11b. Note: Different Connectors have different polarity for the SATAxPCIe select. Note: Default state is GP-In before soft straps are loaded or in the case the soft straps are invalid
GPP_F5 / SATA_DEVSLP3	GPP_F5	VCCPGPPEF	1.8 V or 3.3 V	SATA_DEVSLP3	od							GP-In			no	no	yes(1)	Z	Z	
GPP_F6 / SATA_DEVSLP4	GPP_F6	VCCPGPPEF	1.8 V or 3.3 V	SATA_DEVSLP4	od							GP-In			no	no	yes(1)	Z	Z	
GPP_F7 / SATA_DEVSLP5	GPP_F7	VCCPGPPEF	1.8 V or 3.3 V	SATA_DEVSLP5	od							GP-In			no	no	yes(1)	Z	Z	
GPP_F8 / SATA_DEVSLP6	GPP_F8	VCCPGPPEF	1.8 V or 3.3 V	SATA_DEVSLP6	od							GP-In			no	no	yes(1)	Z	Z	
GPP_F9 / SATA_DEVSLP7	GPP_F9	VCCPGPPEF	1.8 V or 3.3 V	SATA_DEVSLP7	od							GP-In			no	no	yes(2)	Z	Z	
GPP_F10 / SATA_SCLOCK	GPP_F10	VCCPGPPEF	1.8 V or 3.3 V	SATA_SCLOCK	od							GP-In			no	no	yes(1)	PD	Z	
GPP_F11 / SATA_SLOAD	GPP_F11	VCCPGPPEF	1.8 V or 3.3 V	SATA_SLOAD	od							GP-In			no	no	yes(1)	Z	Z	
GPP_F12 / SATA_SDATAOUT1	GPP_F12	VCCPGPPEF	1.8 V or 3.3 V	SATA_SDATAOUT1	od							GP-In			no	no	yes(1)	Z	Z	
GPP_F13 / SATA_SDATAOUT0	GPP_F13	VCCPGPPEF	1.8 V or 3.3 V	SATA_SDATAOUT0	od							GP-In			no	no	yes(1)	Z	Z	
GPP_F14 / PS_ON#	GPP_F14	VCCPGPPEF	1.8 V or 3.3 V			PS_ON#	out					Native F2			no	no	yes(2)	L	L	
GPP_F15 / USB2_OC4#	GPP_F15	VCCPGPPEF	1.8 V or 3.3 V	USB_OC4#	in							GP-In			no	no	yes(1)	Z	Z	
GPP_F16 / USB2_OC5#	GPP_F16	VCCPGPPEF	1.8 V or 3.3 V	USB_OC5#	in							GP-In			no	no	yes(1)	Z	Z	
GPP_F17 / USB2_OC6#	GPP_F17	VCCPGPPEF	1.8 V or 3.3 V	USB_OC6#	in							GP-In			no	no	yes(1)	Z	Z	
GPP_F18 / USB2_OC7#	GPP_F18	VCCPGPPEF	1.8 V or 3.3 V	USB_OC7#	in							GP-In			no	no	yes(1)	Z	Z	
GPP_F19 / eDP_VDDEN	GPP_F19	VCCPGPPEF	1.8 V or 3.3 V	eDP_VDDEN	out							GP-In			no	no	yes(1)	Z	Z	
GPP_F20 / eDP_BKLTEN	GPP_F20	VCCPGPPEF	1.8 V or 3.3 V	eDP_BKLTEN	out							GP-In			no			Z	Z	
GPP_F21 / eDP_BKLTCTL	GPP_F21	VCCPGPPEF	1.8 V or 3.3 V	eDP_BKLTCTL	out							GP-In			no			Z	Z	
GPP_F22 / DDPF_CTRLCLK	GPP_F22	VCCPGPPEF	1.8 V or 3.3 V	DDPF_CTRLCLK	iod							GP-In			no	no	yes(1)	Z	Z	
GPP_F23 / DDPF_CTRLDATA	GPP_F23	VCCPGPPEF	1.8 V or 3.3 V	DDPF_CTRLDATA	iod							GP-Out	Display Port F Detected	20K PD	no	no	no	PD	L	Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% Pull-down is disabled after PCH_PWROK is high.
Primary Well Group G (Per-Group 1.8 V or 3.3 V)																				
GPP_G0 / SD_CMD	GPP_G0	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V	SD_CMD	inout							GP-In			SMI	no	yes(1)	Z	Z	
GPP_G1 / SD_DATA0	GPP_G1	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V	SD_DATA0	inout							GP-In			SMI	no	yes(1)	Z	Z	
GPP_G2 / SD_DATA1	GPP_G2	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V	SD_DATA1	inout							GP-In			SMI	no	yes(1)	Z	Z	
GPP_G3 / SD_DATA2	GPP_G3	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V	SD_DATA2	inout							GP-In			SMI	no	yes(1)	Z	Z	
GPP_G4 / SD_DATA3	GPP_G4	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V	SD_DATA3	inout							GP-In			SMI	no	yes(1)	Z	Z	
GPP_G5 / SD_CD#	GPP_G5	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V	SD_CD#	in							GP-In			SMI	no	yes(1)	Z	Z	
GPP_G6 / SD_CLK	GPP_G6	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V	SD_CLK	out							GP-In			SMI	no	yes(1)	Z	Z	
GPP_G7 / SD_WP	GPP_G7	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8 V or 3.3 V	SD_WP	in							GP-In			SMI	no	yes(1)	Z	Z	
Primary Well Group H (Per-Group 1.8 V or 3.3 V)																				
GPP_H0 / SRCCLKREQ6#	GPP_H0	VCCPGPPHK	1.8 V or 3.3 V	SRCCLKREQ6#	iod							GP-In			no	no	yes(1)	Z	Z	
GPP_H1 / SRCCLKREQ7#	GPP_H1	VCCPGPPHK	1.8 V or 3.3 V	SRCCLKREQ7#	iod							GP-In			no	no	yes(1)	Z	Z	
GPP_H2 / SRCCLKREQ8#	GPP_H2	VCCPGPPHK	1.8 V or 3.3 V	SRCCLKREQ8#	iod							GP-In			no	no	yes(1)	Z	Z	
GPP_H3 / SRCCLKREQ9#	GPP_H3	VCCPGPPHK	1.8 V or 3.3 V	SRCCLKREQ9#	iod							GP-In			no	no	yes(1)	Z	Z	
GPP_H4 / SRCCLKREQ10#	GPP_H4	VCCPGPPHK	1.8 V or 3.3 V	SRCCLKREQ10#	iod							GP-In			no	no	yes(1)	Z	Z	

Signal Name	GPIO	Power Well	Voltage Tolerance	Native Function 1	Native Dir 1	Native Function 2	Native Dir 2	Native Function 3	Native Dir 3	Native Function 4	Native Dir 4	Default	Strap	Pin Strap Termination	NMI/SMI Capable	Input Deglitch	Output Power Sequence Deglitch	Pin State During Reset	Pin State Immediately After Reset	Notes
GPP_H5 / SRCCLKREQ11#	GPP_H5	VCCPGPPHK	1.8 V or 3.3 V	SRCCLKREQ11#	iod							GP-In			no	no	yes(1)	Z	Z	
GPP_H6 / SRCCLKREQ12#	GPP_H6	VCCPGPPHK	1.8 V or 3.3 V	SRCCLKREQ12#	iod							GP-In			no	no	yes(1)	Z	Z	
GPP_H7 / SRCCLKREQ13#	GPP_H7	VCCPGPPHK	1.8 V or 3.3 V	SRCCLKREQ13#	iod							GP-In			no	no	yes(1)	Z	Z	
GPP_H8 / SRCCLKREQ14#	GPP_H8	VCCPGPPHK	1.8 V or 3.3 V	SRCCLKREQ14#	iod							GP-In			no	no	yes(1)	Z	Z	
GPP_H9 / SRCCLKREQ15#	GPP_H9	VCCPGPPHK	1.8 V or 3.3 V	SRCCLKREQ15#	iod							GP-In			no	no	yes(1)	Z	Z	
GPP_H10 / SML2CLK	GPP_H10	VCCPGPPHK	1.8 V or 3.3 V	SML2CLK	iod							GP-In			no	yes	yes(1)	Z	Z	
GPP_H11 / SML2DATA	GPP_H11	VCCPGPPHK	1.8 V or 3.3 V	SML2DATA	iod							GP-In			no	yes	yes(1)	Z	Z	
GPP_H12 / SML2ALERT#	GPP_H12	VCCPGPPHK	1.8 V or 3.3 V	SML2ALERT#	iod							GP-Out	eSPI Flash Sharing Mode	20K PD	no	yes	no	PD	L	Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts.
GPP_H13 / SML3CLK	GPP_H13	VCCPGPPHK	1.8 V or 3.3 V	SML3CLK	iod							GP-In			no	yes	yes(1)	Z	Z	
GPP_H14 / SML3DATA	GPP_H14	VCCPGPPHK	1.8 V or 3.3 V	SML3DATA	iod							GP-In			no	yes	yes(1)	Z	Z	
GPP_H15 / SML3ALERT#	GPP_H15	VCCPGPPHK	1.8 V or 3.3 V	SML3ALERT#	iod							GP-In	Reserved		no	yes	yes(1)	Z	Z	Strap read at rising edge of RSMRST#. External pull-up is required. Recommend 100 kohm if pulled up to 3.3 V or 75 kohm if pulled up to 1.8 V. This strap should sample HIGH. There should NOT be any on-board device driving it toopposite direction during strap sampling.
GPP_H16 / SML4CLK	GPP_H16	VCCPGPPHK	1.8 V or 3.3 V	SML4CLK	iod							GP-In			no	yes	yes(1)	Z	Z	
GPP_H17 / SML4DATA	GPP_H17	VCCPGPPHK	1.8 V or 3.3 V	SML4DATA	iod							GP-In			no	yes	Yes (1)	Z	Z	
GPP_H18 / SML4ALERT#	GPP_H18	VCCPGPPHK	1.8 V or 3.3 V	SML4ALERT#	iod							GP-In			no	yes	yes(1)	Z	Z	
GPP_H19 / ISH_I2C0_SDA	GPP_H19	VCCPGPPHK	1.8 V or 3.3 V	ISH_I2C0_SDA	iod							GP-In			no	yes	yes(1)	Z	Z	
GPP_H20 / ISH_I2C0_SCL	GPP_H20	VCCPGPPHK	1.8 V or 3.3 V	ISH_I2C0_SCL	iod							GP-In			no	yes	yes(1)	Z	Z	
GPP_H21 / ISH_I2C1_SDA	GPP_H21	VCCPGPPHK	1.8 V or 3.3 V	ISH_I2C1_SDA	iod							GP-In			no	yes	yes(1)	Z	Z	
GPP_H22 / ISH_I2C1_SCL	GPP_H22	VCCPGPPHK	1.8 V or 3.3 V	ISH_I2C1_SCL	iod							GP-In			no	yes	yes(1)	Z	Z	
GPP_H23 / TIME_SYNC0	GPP_H23	VCCPGPPHK	1.8 V or 3.3 V	TIME_SYCN0	inout							GP-In			no	no	yes(1)	Z	Z	
Primary Well Group I (3.3 V Only)																				
GPP_I0 / DDPB_HPD0 / DISP_MISC0	GPP_I0	VCCPRIM_3P3	3.3 V	DDPB_HPD0	in	DISP_MISC0	inout					GP-In			NMI /SMI	no	yes(1)	Z	Z	
GPP_I1 / DDPC_HPD1 / DISP_MISC1	GPP_I1	VCCPRIM_3P3	3.3 V	DDPB_HPD1	in	DISP_MISC1	inout					GP-In			NMI /SMI	no	yes(1)	Z	Z	
GPP_I2 / DDPD_HPD2 / DISP_MISC2	GPP_I2	VCCPRIM_3P3	3.3 V	DDPB_HPD2	in	DISP_MISC2	inout					GP-In			NMI /SMI	no	yes(1)	Z	Z	
GPP_I3 / DDPF_HPD3 / DISP_MISC3	GPP_I3	VCCPRIM_3P3	3.3 V	DDPB_HPD3	in	DISP_MISC3	inout					GP-In			NMI /SMI	no	yes(1)	Z	Z	
GPP_I4 / EDP_HPD / DISP_MISC4	GPP_I4	VCCPRIM_3P3	3.3 V	EDP_HPD	in	DISP_MISC4	inout					GP-In			no	no	yes(1)	Z	Z	
GPP_I5 / DDPB_CTRLCLK	GPP_I5	VCCPRIM_3P3	3.3 V	DDPB_CTRLCLK	iod							GP-In			no	Yes	yes(1)	Z	Z	
GPP_I6 / DDPB_CTRLDATA	GPP_I6	VCCPRIM_3P3	3.3 V	DDPB_CTRLDATA	iod							GP-Out	Display Port B Detected	20K PD	no	Yes	no	PD	L	Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% pull-down is disabled after PCH_PWROK is high.
GPP_I7 / DDPC_CTRLCLK	GPP_I7	VCCPRIM_3P3	3.3 V	DDPC_CTRLCLK	iod							GP-In			no	Yes	yes(1)	Z	Z	
GPP_I8 / DDPC_CTRLDATA	GPP_I8	VCCPRIM_3P3	3.3 V	DDPC_CTRLDATA	iod							GP_Out	Display Port C Detected	20K PD	no	Yes	no	PD	L	Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% pull-down is disabled after PCH_PWROK is high.
GPP_I9 / DDPD_CTRLCLK	GPP_I9	VCCPRIM_3P3	3.3 V	DDPD_CTRLCLK	iod							GP-In			no	Yes	yes(1)	Z	Z	
GPP_I10 / DDPD_CTRLDATA	GPP_I10	VCCPRIM_3P3	3.3 V	DDPD_CTRLDATA	iod							GP-Out	Display Port D Detected	20K PD	no	Yes	no	PD	L	Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% pull-down is disabled after PCH_PWROK is high.
GPP_I11 / M2_SKT2_CFG0	Strap read at rising edge of	VCCPRIM_3P3	3.3 V	M2_SKT2_CFG0	in							GP-In			no	No	yes(1)	Z	Z	
GPP_I12 / M2_SKT2_CFG1	GPP_I12	VCCPRIM_3P3	3.3 V	M2_SKT2_CFG1	in							GP-In			no	No	yes(1)	Z	Z	
GPP_I13 / M2_SKT2_CFG2	GPP_I13	VCCPRIM_3P3	3.3 V	M2_SKT2_CFG2	in							GP-In			no	No	yes(1)	Z	Z	

Signal Name	GPIO	Power Well	Voltage Tolerance	Native Function 1	Native Dir 1	Native Function 2	Native Dir 2	Native Function 3	Native Dir 3	Native Function 4	Native Dir 4	Default	Strap	Pin Strap Termination	NMI/SMI Capable	Input Deglitch	Output Power Sequence Deglitch	Pin State During Reset	Pin State Immediately After Reset	Notes
GPP_I14 / M2_SKT2_CFG3	GPP_I14	VCCPRIM_3P3	3.3 V	M2_SKT2_CFG3	in							GP-In			no	No	yes(1)	Z	Z	
Primary Well Group J (1.8 V Only)																				
GPP_J0 / CNV_PA_BLANKING	GPP_J0	VCCPRIM_1P8	1.8 V	CNV_PA_BLANKING	in							GP-In			no	no	yes(1)	Z	Z	
GPP_J1 / CPU_C10_GATE#	GPP_J1	VCCPRIM_1P8	1.8 V			CPU_C10_GATE#	out					Native F2			no	no	yes(1)	H (Refer note)	H	The During Reset Pin State of this GPIO is H via a ~20 kohm pull-up to 3.3 V independent of soft strap assigned pad voltage. A 1.8 V device connected to this GPIO must be capable of taking ~20 kohm pull-up to 3.3V.
GPP_J2	GPP_J2	VCCPRIM_1P8	1.8 V									GP-In			no	no	yes(1)	Z	Z	
GPP_J3	GPP_J3	VCCPRIM_1P8	1.8 V									GP-In			no	no	yes(1)	Z	Z	
GPP_J4 / CNV_BRI_DT / UART0B_RTS#	GPP_J4	VCCPRIM_1P8	1.8 V	CNV_BRI_DT	out	UART0B_RTS#	out					Natiive F1	XTAL Frequency Select	20K PD	no	no	no	PD	H	Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% Pull-down is disabled after RSMRST# de-asserts.
GPP_J5 / CNV_BRI_RSP / UART0B_RXD	GPP_J5	VCCPRIM_1P8	1.8 V	CNV_BRI_RSP	in	UART0B_RXD	in					Natiive F1			no	no	yes(1)	Z	H	
GPP_J6 / CNV_RGI_DT / UART0B_TXD	GPP_J6	VCCPRIM_1P8	1.8 V	CNV_RGI_DT	out	UART0B_TXD	out					Natiive F1	M.2 CNV Mode		no	no	no	Z	H	Strap read at rising edge of RSMRST#. An external pull-up or pull-down resistor is required.
GPP_J7 / CNV_RGI_RSP / UART0B_CTS#	GPP_J7	VCCPRIM_1P8	1.8 V	CNV_RGI_RSP	in	UART0B_CTS#	in					Natiive F1			no	no	yes(1)	Z	H	
GPP_J8 / CNV_MFUART2_RXD	GPP_J8	VCCPRIM_1P8	1.8 V	CNV_MFUART2_RXD	in							GP-In			no	no	yes(1)	Z	Z	
GPP_J9 / CNV_MFUART2_TXD	GPP_J9	VCCPRIM_1P8	1.8 V	CNV_MFUART2_TXD	out							GP-Out	1.8 V VCCSPI	20K PD	no	no	no	PD	L	Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% Pull-down is disabled after RSMRST# de-asserts.
GPP_J10	GPP_J10	VCCPRIM_1P8	1.8 V									GP-In			no	no	yes(1)	Z	Z	
GPP_J11 / A4WP_PRESENT	GPP_J11	VCCPRIM_1P8	1.8 V	A4WP_PRESENT	in							Native F1			no	no	yes(1)	Z	Z	
Primary Well Group K (Per-Group 1.8 V or 3.3 V)																				
GPP_K0	GPP_K0	VCCPGPPHK	1.8 V or 3.3 V									GP-In			no	yes	yes(1)	Z	Z	
GPP_K1	GPP_K1	VCCPGPPHK	1.8 V or 3.3 V									GP-In			no	yes	yes(1)	Z	Z	
GPP_K2	GPP_K2	VCCPGPPHK	1.8 V or 3.3 V									GP-In			no	yes	yes(1)	Z	Z	
GPP_K3	GPP_K3	VCCPGPPHK	1.8 V or 3.3 V									GP-In			no	yes	yes(1)	Z	Z	
GPP_K4	GPP_K4	VCCPGPPHK	1.8 V or 3.3 V									GP-In			no	yes	yes(1)	Z	Z	
GPP_K5	GPP_K5	VCCPGPPHK	1.8 V or 3.3 V									GP-In			no	yes	yes(1)	Z	Z	
GPP_K6	GPP_K6	VCCPGPPHK	1.8 V or 3.3 V									GP-In			no	yes	yes(1)	Z	Z	
GPP_K7	GPP_K7	VCCPGPPHK	1.8 V or 3.3 V									GP-In			no	yes	yes(1)	Z	Z	
GPP_K8	GPP_K8	VCCPGPPHK	1.8 V or 3.3 V	Reserved	od							Native F1			no	no	yes(1)	Z	Z	
GPP_K9	GPP_K9	VCCPGPPHK	1.8 V or 3.3 V	Reserved	od							Native F1			no	no	yes(1)	Z	Z	
GPP_K10	GPP_K10	VCCPGPPHK	1.8 V or 3.3 V	Reserved	od							Native F1			no	no	yes(1)	Z	Z	
GPP_K11	GPP_K11	VCCPGPPHK	1.8 V or 3.3 V	Reserved	od							Native F1			no	no	yes(1)	Z	Z	
GPP_K12 / GSXDOUT	GPP_K12	VCCPGPPHK	1.8 V or 3.3 V	GSXDOUT	out							GP-In			no	no	yes(1)	Z	Z	
GPP_K13 / GSXSLOAD	GPP_K13	VCCPGPPHK	1.8 V or 3.3 V	GSXSLOAD	out							GP-In			no	no	yes(1)	Z	Z	
GPP_K14 / GSXDIN	GPP_K14	VCCPGPPHK	1.8 V or 3.3 V	GSXDIN	in							GP-In			no	no	yes(1)	Z	Z	
GPP_K15 / GSXSRESET#	GPP_K15	VCCPGPPHK	1.8 V or 3.3 V	GSXSRESET#	out							GP-In			no	no	yes(1)	Z	Z	
GPP_K16 / GSXCLK	GPP_K16	VCCPGPPHK	1.8 V or 3.3 V	GSXCLK	out							GP-In			no	no	yes(1)	Z	Z	
GPP_K17 / ADR_COMPLETE	GPP_K17	VCCPGPPHK	1.8 V or 3.3 V	ADR_COMPLETE	out							GP-In			no	no	yes(1)	Z	Z	
GPP_K18 / NMI#	GPP_K18	VCCPGPPHK	1.8 V or 3.3 V	NMI#	od							GP-In			no	no	yes(1)	Z	Z	
GPP_K19 / SMI#	GPP_K19	VCCPGPPHK	1.8 V or 3.3 V	SMI#	od							GP-In			no	no	yes(1)	Z	Z	
GPP_K20	GPP_K20	VCCPGPPHK	1.8 V or 3.3 V	Reserved	out							Native F1			no	no	yes(1)	H (Refer note)	H	The During Reset Pin State of this GPIO is H via a ~20 kohm pull-up to 3.3 V independent of soft strap assigned pad voltage. A 1.8 V device connected to this GPIO must be capable of taking ~20 kohm pull-up to 3.3V.

Signal Name	GPIO	Power Well	Voltage Tolerance	Native Function 1	Native Dir 1	Native Function 2	Native Dir 2	Native Function 3	Native Dir 3	Native Function 4	Native Dir 4	Default	Strap	Pin Strap Termination	NMI/SMI Capable	Input Deglitch	Output Power Sequence Deglitch	Pin State During Reset	Pin State Immediately After Reset	Notes
GPP_K21	GPP_K21	VCCPGPPHK	1.8 V or 3.3 V	Reserved	out							Native F1			no	no	yes(1)	H (Refer note)	H	The During Reset Pin State of this GPIO is H via a ~20 kohm pull-up to 3.3 V independent of soft strap assigned pad voltage. A 1.8 V device connected to this GPIO must be capable of taking ~20 kohm pull-up to 3.3V.
GPP_K22 / IMGCLKOUT0	GPP_K22	VCCPGPPHK	1.8 V or 3.3 V	IMGCLKOUT0	out							GP-In			no	no	yes(1)	Z	Z	
GPP_K23 / IMGCLKOUT1	GPP_K23	VCCPGPPHK	1.8 V or 3.3 V	IMGCLKOUT1	out							GP-In			no	no	yes(1)	Z	Z	
Deep Sleep Well Group (3.3 V Only)																				
GPD0 / BATLOW#	GPD0	VCCDSW_3P3	3.3 V	BATLOW#	in							Native F1			no	no	yes(1)	Z	Z	
GPD1 / ACPRESENT	GPD1	VCCDSW_3P3	3.3 V	ACPRESENT	in							Native F1			no	no	yes(1)	See note	Z	Pin state during reset: In Deep Sx enabled configurations, pin is PD when PD is enabled (see ACPRES_PD_DSX_DIS bit); else Z
GPD2 / LAN_WAKE#	GPD2	VCCDSW_3P3	3.3 V	LAN_WAKE#	in							Native F1			no	no	yes(1)	Z	Z	
GPD3 / PWRBTN#	GPD3	VCCDSW_3P3	3.3 V	PWRBTN#	in							Native F1			no	yes	yes(1)	PU	PU	
GPD4 / SLP_S3#	GPD4	VCCDSW_3P3	3.3 V	SLP_S3#	out							Native F1/GP-In			no	no	yes(2)	Native F1: L / GPIO: L	Native F1: H / GPIO: L	Native if SLP_S3# / GPD4 Signal Configuration soft strap = 0, else GPI
GPD5 / SLP_S4#	GPD5	VCCDSW_3P3	3.3 V	SLP_S4#	out							Native F1/GP-In			no	no	yes(2)	Native F1: L / GPIO: L	Native F1: H / GPIO: L	Native if SLP_S4# / GPD5 Signal Configuration soft strap = 0, else GPI
GPD6 / SLP_A#	GPD6	VCCDSW_3P3	3.3 V	SLP_A#	out							Native F1/GP-In			no	no	yes(2)	Native F1: L / GPIO: L	Native F1: H / GPIO: L	Native if SLP_A# / GPD6 Signal Configuration soft strap = 0, else GP-In
GPD7	GPD7	VCCDSW_3P3	3.3 V									GP-Out	Reserved		no	no	no	Z	L	Strap read at rising edge of DSW_PWROK. External pull-up is required. Recommend 100 kohm. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPD8 / SUSCLK	GPD8	VCCDSW_3P3	3.3 V	SUSCLK	out							Native F1			no	no	yes(2)	L	T	
GPD9 / SLP_WLAN#	GPD9	VCCDSW_3P3	3.3 V	SLP_WLAN#	out							Native F1/GP-In			no	no	yes(2)	Native F1: L / GPIO: L	Native F1: L / GPIO: L	Native if SLP_WLAN# / GPD9 Signal Configuration soft strap = 0, else GPI
GPD10 / SLP_S5#	GPD10	VCCDSW_3P3	3.3 V	SLP_S5#	out							Native F1/GP-In			no	no	yes(2)	Native F1: L / GPIO: L	Native F1: H / GPIO: L	Native if SLP_S5# / GDP10 Signal Configuration soft strap = 0, else GPI
GPD11 / LANPHYPC	GPD11	VCCDSW_3P3	3.3 V	LANPHYPC	out							Native F1/GP-In			no	no	yes(2)	Native F1: L / GPIO: L	Native F1: L / GPIO: Z	Native if LAN PHY Power Control GPD11 Signal Configuration soft strap = 0, else GPI

Deglitch Legend
yes(1) - o/p Hi-Z, no internal weak pull during respective pin power sequencing
yes(2) - o/p Hi-Z, with integrated 20 kohm ± 30% pull-down during respective pin power sequencing

Pin State Legend
H- Driven High
L - Driven Low
Z - Hi-Z
PU - Integrated 20 kohm ± 30% pull-up pulls pin high
PD - Integrated 20 kohm ± 30% pull-down pulls pin low
T - Toggling