Intel® 400 Series Chipset Family Platform Controller Hub (PCH)

Specification Update

July 2022

Revision 009

Document Number: 620856-009

Contents

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Revision History

Revision Number	Description	Release Date
001	• Initial Release	April 2020
002	• Added the following errata: — Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment — System May Hang with USB-C* Power Adapter	May 2020
003	• Added the following Specification Clarification — PCIe Precision Time Measurement (PTM) Byte Order	June 2020
004	• Added the following erratum: — Audio Global Time Synchronization Register Access	July 2020
005	• Added the following erratum: — Phase Lock Loop (PLL) Feedback Circuit	September 2020
006	• Added the following Specification Clarification —	November 2020
007	• Added the following erratum: — xHCI D3 Exit Timing	July 2021
008	• Added the following erratum: — Leakage Current from VCCPRIM_1P8 Power Rail	January 2022
009	• Added the following erratum: — G3 Current Specification on VCCRTC Rail — Timed GPIO Event May Have a Mismatched Time Stamp — USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst	July 2022

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Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation errata, specification changes and Specification clarifications. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents

Title	Document Number
Intel® 400 Series Chipset Family Platform Controller Hub Datasheet	620854 (Vol1) 620855 (Vol2)

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

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Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed in Intel® hardware, firmware, or software.
No Fix:	There are no plans to fix this erratum.

Errata Summary Table

Erratum ID	Stepping	Errata
	A0	
1	No Fix	USB DbC or Device Mode Port When Resuming from S3, S4, S5, or G3 State
2	No Fix	xHCI Minor Revision Value
3	No Fix	xHCI Link Error Count Field
4	No Fix	xHCI U1 Exit LFPS Duration
5	No Fix	xHCI Power Management Link Timer
6	No Fix	DbC (Debug Capability) Device Fails To Enumerate When Connected To USB 3.2 Gen 2x1 Port
7	No Fix	SDXC CRC Detection
8	No Fix	Intel® Trace Hub Pipe Line Empty
9	No Fix	SPI SFDP Program Suspend and Program Resume Instruction Fields Not Used
10	No Fix	PCIe* Root Port CLKREQ# Asserted Low to Clock Active Timing
11	No Fix	xHCI USB 2.0 ISOCH Device Missed Service Interval
12	No Fix	xHCI Link Protocol Field Value
13	No Fix	xHCI Short Packet Event Using Non-Event Data TRB
14	No Fix	eSPI SBLCL Register Bit Not Cleared by PLTRST#
15	No Fix	xHCI Host Controller Reset May Cause a System Hang
16	No Fix	xHCI Protocol Speed ID Count Field
17	No Fix	SATA Enclosure Management LED Messaging
18	No Fix	Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment
19	No Fix	System May Hang with USB-C* Power Adapter

Erratum ID	Stepping	Errata
	A0	
20	No Fix	Audio Global Time Synchronization Register Access
21	No Fix	Phase Lock Loop (PLL) Feedback Circuit
22	No Fix	Leakage Current from VCCPRIM_1P8 Power Rail
23	No Fix	G3 Current Specification on VCCRTC Rail
24	No Fix	Timed GPIO Event May Have a Mismatched Time Stamp
25	No Fix	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst

Specification Change

Number	Stepping	Specification Change
	A0	
		No specification changes in this revision of the Specification Update

Specification Clarification

Number	Specification Clarification
1	PCIe Precision Time Measurement (PTM) Byte Order
2	SX_EXIT_HOLDOFF# Not Functional with eSPI Enabled
3	xHCI D3 Exit Timing

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Errata

1. USB DbC or Device Mode Port When Resuming from S3, S4, S5, or G3 State

Problem: If a PCH USB Type-C* port is configured in Device Mode (or in DbC mode) and connected to an external USB 3.2 host controller, it may cause the USB port to go into a non-functional state in the following scenarios:

1. The PCH resumes from S3, S4, or S5 state, the port may remain in U2.
2. The port is connected to a USB 3.2 Gen 1x1 host controller when resuming from S3, S4, S5 or G3, the port may enter into Compliance Mode or an inactive state if Compliance mode is disabled.
3. The port is connected to a USB 3.2 Gen 2x1 host controller when resuming from S3, S4, S5 or G3, the port may enter an inactive state.

Implication: PCH USB Type-C port configured in Device Mode (or in DbC mode) may fail to enumerate or become unavailable.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

2. xHCI Minor Revision Value

Problem: The PCH reports USB Minor Revision in the XECP_SUPP_USB3_0 register (offset 8020h) as 01h. The USB-IF released a ECN to update the minor revision to 10h.

Implication: USB-IF xHCI CV TD 1.5 may report a failure. Intel has obtained a waiver for TD 1.5.

Note: No functional impact is expected.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

3. xHCI Link Error Count Field

Problem: The xHCI Link Error Count Field in the USB 3.0 Port X Link Info – (PORTLI) register is implemented as Read/Write instead of Read Only as defined by the xHCI specification.

Implication: USB-IF xHCI CV TD 3.17 may report a failure. Intel has obtained a waiver for TD 3.17.

Note: No functional impact is expected.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

4. xHCI U1 Exit LFPS Duration

Problem: The xHCI U1 Exit LFPS (t13-t11) duration timing is implemented as 0.6 us to 0.9 us. The USB-IF released a ECN updating this timing value to 0.9 us to 1.2 us.

Implication: USB-IF xHCI CV TD 7.18 may report a failure. Intel has obtained a waiver for TD 7.18.

Note: No functional issues are expected.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

5. xHCI Power Management Link Timer

Problem: The xHCI implements the Power Management Link Timer (PM LC Timer) Timeout value as 10 us instead of 4 us as defined by the USB 3.2 specification.

Implication: USB-IF xHCI CV TD 7.21 may report a failure. Intel has obtained a waiver for TD 7.21.

Note: No functional issues are expected.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

6. DbC (Debug Capability) Device Fails To Enumerate When Connected To USB 3.2 Gen 2x1 Port

Problem: The PCH DbC (Debug Capability) Device may fail to enumerate if connected to a USB host controller's USB 3.2 Gen 2x1 port.

Implication: The PCH DbC may not function.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

7. SDXC CRC Detection

Problem: The SDXC controllers may fail to detect a CRC error if a bit error occurs on the DATA3 signal during read operations when in SDXC DDR50 mode. CRC detection on other DATA signals is not impacted.

Implication: The controller will not flag the CRC error to the driver or application, which could result in data integrity issues. Bit errors on SDXC DATA signals are not expected on platforms that follow Intel recommended design guidelines and tuning processes.

Workaround: None identified. To mitigate the issue, SDXC SDR50 modes can be used instead of DDR50.

Status: For the steppings affected, refer to the Summary Tables of Changes.

8. Intel® Trace Hub Pipe Line Empty

Problem: The Intel® Trace Hub Pipe Line Empty bit (CSR_MTB_BAR, Offset D4h) for a given output port may be set while the Input Buffer Empty for the associated output port is not set. This will only happen when the captureDone signal is de-asserted by clearing the ForceCaptureDone bit (CSR_MTB_BAR, Offset D8h) is cleared or the StoreQual[0] signal is de-asserted by the Trigger Unit before the pipe line is empty, and the destination is either system memory or USB (DCI).

Implication: There may be valid trace data in the trace source input buffer which did not get sent to the destination (output port).

Workaround: None identified. CaptureDone should be cleared or de-asserted after the pipe line is empty.

Status: For the steppings affected, refer to the Summary Tables of Changes.

9. SPI SFDP Program Suspend and Program Resume Instruction Fields Not Used

Problem: For flash device suspend / resume opcodes, the SPI controller does not use JEDEC SFDPs 13th DWORD bits [15:0], Program Suspend Instruction and Program Resume Instruction fields. The controller only uses bits [31:16], Suspend Instruction and Resume Instruction fields, to obtain the suspend / resume opcodes.

Implication: If the SPI flash requires bits [15:0] to be different than bits [31:16], then the suspend / resume feature is not functional. In this case, system behavior varies depending on what the suspend / resume instruction is and when it is generated.

Note: Major flash vendors have been using the same value for bits [31:16] and bits [15:0].

Workaround: None identified.
If a device requires bits [15:0] to be different than bits [31:16], then disable the device suspend / resume via the SPI Suspend / Resume Enable soft strap.

Status: For the steppings affected, refer to the Summary Tables of Changes.

10. PCIe* Root Port CLKREQ# Asserted Low to Clock Active Timing

Problem: During L1 exit, the PCH PCIe* Root Ports may exceed the CLKREQ# asserted low to clock active maximum specification due to PCH PCIe clock un-gate path delays.

Implication: PCIe end point device L1 exit instabilities may be observed.

Note: PCIe end point devices that message LTR latency greater than or equal to 1 µs are not affected by this.

Workaround: None identified.

- Platforms not supporting S0ix with PCIe end point devices that do not support LTR may disable the associated PCH SRCCLKREQ# signal to keep the PCIe clock active during L1.
- Platforms supporting S0ix with PCIe end point devices that have LTR latencies less than 1 µs may disable the associated PCH SRCCLKREQ# signal to keep the PCIe clock active during L1.

Status: For the steppings affected, refer to the Summary Tables of Changes.

11. xHCI USB 2.0 ISOCH Device Missed Service Interval

Problem: When the xHCI controller is stressed with concurrent traffic across multiple USB ports, the xHCI controller may fail to service USB 2.0 Isochronous IN endpoints within the required service interval.

Implication: USB 2.0 isochronous devices connected to the xHCI controller may experience dropped packets.

Note: This issue has only been observed in a synthetic environment.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

12. xHCI Link Protocol Field Value

Problem: The xHCI Host Controller reports the Link Protocol (LP) bits [15:14] as 0x0h in the XECP_SUPP_USB3_5 Super Speed Plus register (xHCI MMIO offset 8034h). The xHCI spec rev 1.1 (published in Nov. 2017) defines this bit should be set to 0x1h for SuperSpeed USB 10 Gbps port.

Implication: USB-IF xHCI CV TD 1.9 may report a failure. The failure was not observed during the USB certification for the xHCI USB host controller and thus a waiver was not required.

Note: No functional impact is expected.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

13. xHCI Short Packet Event Using Non-Event Data TRB

Problem: The xHCI may generate an unexpected short packet event for the last transfer's Transfer Request Block (TRB) when using Non-Event Data TRB with multiples TRBs.

Implication: Transfer may fail due to the packet size error.

Note: This issue has only been observed in an synthetic environment. No known implication has been identified with commercial software.

Workaround: None identified.

Intel recommends software to use Data Event TRBs for short packet completion.

Status: For the steppings affected, refer to the Summary Tables of Changes.

14. eSPI SBLCL Register Bit Not Cleared by PLTRST#

Problem: The IOSF-SB eSPI Link Configuration Lock (SBLCL) bit (offset 4000h, bit 27 in eSPI PCR space) is reset by RSMRST# assertion instead of PLTRST# assertion.

Implication: If the SBLCL bit is set to 1, software will not be able to access the eSPI device Capabilities and Configuration register in the reserved address range (0h - 7FFh) until RSMRST# asserts.

Workaround: None identified.

If software needs to access the eSPI device reserved range 0h - 7FFh while SBLCL bit is set to 1, a RSMRST# assertion should be performed.

Status: For the steppings affected, refer to the Summary Tables of Changes.

15. xHCI Host Controller Reset May Cause a System Hang

Problem: The xHCI host controller may fail to response if either of the two actions are performed:

1. Accessing xHCI configuration space within 1 ms of setting the xHCI HCRST (Host Controller Reset) bit of the USB Command Register (xHC IBAR, offset 80h,Bit[1]), or
2. Setting the HCRST bit two times within 120 ms.

Implication: The system may hang.

Workaround: None identified.

Note: Software must not make any accesses to the xHCI Host Controller registers for 1 ms after setting the HCRST bit 1 of the USB Command Register (xHCI BAR + 80h) and must add a 120 ms delay in between consecutive xHCI host controller resets.

Status: For the steppings affected, refer to the Summary Tables of Changes.

16. xHCI Protocol Speed ID Count Field

Problem: The xHCI Host Controller reports an incorrect protocol Speed ID Count value for the USB 3.2 Supported Protocol Capability register -xHCI MMIO offset 8028 bits [31:28].

Implication: USB-IF xHCI CV TD 1.9 may report a failure.

Note: No Functional impact is expected.

Workaround: None Identified

Status: For the steppings affected, refer to the Summary Tables of Changes.

17. SATA Enclosure Management LED Messaging

Problem: When sending a SATA enclosure LED message and all SATA ports are either idle or disabled, the PCH may not transmit the LED message due to an internal clock gating issue.

Implication: The LED status for SATA enclosure may be incorrect.

Workaround: None identified.

Note: Enclosure Management SW can poll the Enclosure Management (EM_CTL) - Offset 20h bit 8 register for a 0 value immediately before writing LED messages.

Status: For the steppings affected, refer to the .

18. Intel® Serial I/O Controller DMA LLP 4 GB Boundary Alignment

Problem: If software assigns a 4 GB-aligned address to the Linked List Pointer (LLP_LOn = 0h) for Intel® Serial I/O Controller DMA engine, then the DMA engine interprets this as an empty link list and will not perform DMA transfers.

Implication: An Intel® Serial IO controller (i.e. I^2C, GSPI, or UART) may stop operating which may cause the system to hang.

Workaround: Driver software should not assign LLP to a 4 GB-aligned address.

Note: This issue has been addressed in the Intel Serial IO drivers in the following versions or later: For Microsoft* Windows* 10, I^2C device driver rev 30.100.1724.2, SPI device driver rev 30.100.1725.1, and UART device driver rev 30.100.1725.1.

Status: For the steppings affected, refer to the Summary Tables of Changes.

19. System May Hang with USB-C* Power Adapter

Problem: Connecting a USB-C* power adapter to a PCH USB port may cause a race condition that can result in a xHCI controller hang. This issue only occurs on designs where the USB-C Power Delivery (PD) implements OOB messaging to communicate with the PCH for port mapping.

Implication: The system may hang.

Note: This issue does not occur when the system is in Sx state and has only been observed when repeatedly connecting a USB-C power adapter.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

20. Audio Global Time Synchronization Register Access

Problem: Disabling the audio DSP through the Intel High Definition Audio Function Configuration Register Offset 530h in the PCH Private Configuration Space by setting bit 2 to '1' will block accesses to Audio Global Time Synchronization registers in MMIO space (Offset 500h - 55Fh).

Implication: Audio Global Time Synchronization registers may not be accessible and any attempted accesses may result in a system hang.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

21. Phase Lock Loop (PLL) Feedback Circuit

Problem: The Main PLL and USBPCIe PLL have independent feedback circuits. A feedback circuit timing marginality may result in a momentary jitter excursion in the corresponding PLL and downstream circuitry.

Implication: If the Main PLL loses lock, then the system may hang. If the USBPCIe PLL loses lock, USB 3.1 / SATA / PCIe / integrated GbE / DMI / CLKOUT_PCIE interfaces may experience errors, including correctable errors, interface downtrains, or hangs.

Workaround: A fix has been identified for this erratum and may be available in a software update.

Status: For the steppings affected, refer to the Summary Tables of Changes.

22. Leakage Current from VCCPRIM_1P8 Power Rail

Problem: When the VCCPRIM_1P8 is off and the VCCPRIM_3P3 is powered on during G3 to S5, there may be a leakage current from the VCCPRIM_3P3 power rail to VCCPRIM_1P8 power rail.

Implication: The leakage voltage may be observed on VCCPRIM_1P8 power rail. There is no known functional or reliability impact.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

23. G3 Current Specification on VCCRTC Rail

Problem: The PCH VCCRTC current draw during the G3 state may exceed the maximum current specification of 6 µA, as documented in the Intel 500 Series Chipset Family On-Package Platform Controller Hub Electrical and Thermal Specification (Document ID: 620854).

Implication: PCH units may experience VCCRTC rail current draw during the G3 state up to 8 uA. Platform implications are platform design specific.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

24. Timed GPIO Event May Have a Mismatched Time Stamp

Problem: When a Timed GPIO event is counted in the Event Counter Capture (TGPIOECCV) register (offset 1238h, bits 31 to 0 in PWRMBASE space), the Time Capture (TGPIOTCV) register (offset 1230h, bits 31 to 0 in PWRMBASE space) value is not immediately updated after that event is counted.

Implication: A Timed GPIO event may have a mismatched time stamp.

Workaround: None identified. A Timed GPIO driver can partially mitigate for this erratum by detecting that a TGPIOECCV register change has occurred without a TGPIOTCV register change and then repeatedly re-read the TGPIOTCV register until a change does occur.

Status: For the steppings affected, refer to the Summary Tables of Changes.

25. USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst

Problem: On USB 3.2 Gen 1x1 capable ports, including ports configured as USB 3.2 Gen 1x1 by soft strap, the xHCI controller may send only 15 LFPS signals instead of a burst of 16 LFPS signals as specified by the USB 3.2 specification.

Implication: There are no known functional implications due to this erratum. LFPS handshake requires the receiver link partner to only detect 2 LFPS signals. This issue may impact the SuperSpeed compliance test case which checks for the 16 LFPS burst requirements: TD6.4, TD6.5, and TD7.31.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

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Specification Change

There are no Specification Changes in this revision of the Specification Update.

Specification Clarification

1. PCIe Precision Time Measurement (PTM) Byte Order

Added the following note to the Intel® 400 Series Chipset Family Platform Controller Hub (PCH) Datasheet Volume 1 of 2 (#620854) in the section Precision Time Measurement (PTM):

> PCIe Root Ports transmit the lower byte [7:0] of the Propagation Delay Field first instead of the upper byte [31:24] within their PTM DelayResponseD (Response with Data) messages.

2. SX_EXIT_HOLDOFF# Not Functional with eSPI Enabled

Added the following note to the Intel® 400 Series Chipset Family Platform Controller Hub (PCH) Datasheet Volume 1 of 2 (#620854) in the Power Management chapter Signal Description section:

> When eSPI is enabled, SX_EXIT_HOLDOFF# functionality is not available, and assertion of the signal will not impact Sx exit flows.

3. xHCI D3 Exit Timing

Added the following text to the Intel® 400 Series Chipset Family Platform Controller Hub (PCH) External Design Specification (EDS) Volume 2 of 2 (#610272) in the Power Management Control/Status (PM_CS) register summary, bits 1:0, 'PowerState (POWERSTATE)' field description section:

> Software should wait for 100 ms before requesting the xHCI controller to re-enter D3 after a D3 exit.

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