Intel® B460 and H410 Chipset Platform Controller Hub

GPIO Implementation Summary

April 2020

Revision 001

Document Number: 621884-001

Signal Name	GPIO	Power Well	Voltage Tolerance	Native Function 1	Native Dir 1	Native Function 2	Native Dir 2	Native Function 3	Native Dir 3	Default	Strap	Pin Strap Termination	NMI/SMI Capable	Input Deglitch	Output Power Sequence Deglitch	Notes
Primary Well Group A (Per-Group 1.8 V or 3.3 V)																
GPP_A0 / RCIN#	GPP_A0	VCCPGPPA	1.8 V or 3.3 V	RCIN#	in					Native F1 /GP-In			no	no	yes(1)	Native F1 if eSPI or LPC pin strap = 0 (LPC Mode). Else GPI.
GPP_A1 / LAD0 / ESPI_IO0	GPP_A1	VCCPGPPA	1.8 V or 3.3 V	LAD0	inout			ESPI_IO0	inout	Native F1/Native F3			no	no	yes(1)	Native F1 if if eSPI or LPC pin strap = 0 (LPC Mode), else Native F3
GPP_A2 / LAD1 / ESPI_IO1	GPP_A2	VCCPGPPA	1.8 V or 3.3 V	LAD1	inout			ESPI_IO1	inout	Native F1/Native F3			no	no	yes(1)	Native F1 if if eSPI or LPC pin strap = 0 (LPC Mode), else Native F3
GPP_A3 / LAD2 / ESPI_IO2	GPP_A3	VCCPGPPA	1.8 V or 3.3 V	LAD2	inout			ESPI_IO2	inout	Native F1/Native F3			no	no	yes(1)	Native F1 if if eSPI or LPC pin strap = 0 (LPC Mode), else Native F3
GPP_A4 / LAD3 / ESPI_IO3	GPP_A4	VCCPGPPA	1.8 V or 3.3 V	LAD3	inout			ESPI_IO3	inout	Native F1/Native F3			no	no	yes(1)	Native F1 if if eSPI or LPC pin strap = 0 (LPC Mode), else Native F3
GPP_A5 / LFRAME# / ESPI_CS#	GPP_A5	VCCPGPPA	1.8 V or 3.3 V	LFRAME#	out			ESPI_CS#	out	Native F1/Native F3			no	no	yes(2)	Native F1 if if eSPI or LPC pin strap = 0 (LPC Mode), else Native F3
GPP_A6 / SERIRQ	GPP_A6	VCCPGPPA	1.8 V or 3.3 V	SERIRQ	inout					Native F1/GP-In			no	no	yes(1)	Native F1 if eSPI or LPC pin strap = 0 (LPC Mode). Else GPI.
GPP_A7 / PIRQA#	GPP_A7	VCCPGPPA	1.8 V or 3.3 V	PIRQA#	iod					Native F1/GP-In			no	no	yes(1)	Native F1 if eSPI or LPC pin strap = 0 (LPC Mode). Else GPI in.
GPP_A8 / CLKRUN#	GPP_A8	VCCPGPPA	1.8 V or 3.3 V	CLKRUN#	iod					Native F1/GP-In			no	no	yes(1)	Native F1 if if eSPI or LPC pin strap = 0 (LPC Mode), else GP-In
GPP_A9 / CLKOUT_LPC0 / ESPI_CLK	GPP_A9	VCCPGPPA	1.8 V or 3.3 V	CLKOUT_LPC0	out			ESPI_CLK	out	Native F1/Native F3			no	no	yes(1)	Native F1 if if eSPI or LPC pin strap = 0 (LPC Mode), else Native F3
GPP_A10 / CLKOUT_LPC1	GPP_A10	VCCPGPPA	1.8 V or 3.3 V	CLKOUT_LPC1	out					Native F1/GP-In			no	no	yes(1)	Native F1 if eSPI or LPC pin strap = 0 (LPC Mode), else GP-In.
GPP_A11 / PME#	GPP_A11	VCCPGPPA	1.8 V or 3.3 V	PME#	iod					Native F1/GP-In			no	no	yes(1)	Native F1 if eSPI or LPC pin strap = 0 (LPC Mode), else GP-In.
GPP_A12 / BM_BUSY# / ISH_GP6 / SX_EXIT_HOLDOFF#	GPP_A12	VCCPGPPA	1.8 V or 3.3 V	BM_BUSY#	in	ISH_GP6	inout	SX_EXIT_HOLDOFF#	in	GP-In			no	no	yes(1)	
GPP_A13 / SUSWARN# / SUSPWRDNACK	GPP_A13	VCCPGPPA	1.8 V or 3.3 V	SUSWARN# / SUSPWRDNACK	out					Native F1/GP-In			no	no	yes(2)	Native F1 if eSPI or LPC pin strap = 0 (LPC Mode), else GP-In.
GPP_A14 / SUS_STAT# / ESPI_RESET#	GPP_A14	VCCPGPPA	1.8 V or 3.3 V	SUS_STAT#	out			ESPI_RESET#	out	Native F1 / Native F3			no	no	yes(2)	Native F1 if eSPI or LPC pin strap = 0 (LPC Mode), else Native F3.
GPP_A15 / SUSACK#	GPP_A15	VCCPGPPA	1.8 V or 3.3 V	SUSACK#	in					Native F1/GP-In			no	no	yes(1)	Native F1 if eSPI or LPC pin strap = 0 (LPC Mode), else GP-In.
GPP_A16	GPP_A16	VCCPGPPA	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_A17 / ISH_GP7	GPP_A17	VCCPGPPA	1.8 V or 3.3 V	ISH_GP7	inout					GP-In			no	no	yes(1)	
GPP_A18 / ISH_GP0	GPP_A18	VCCPGPPA	1.8 V or 3.3 V	ISH_GP0	inout					GP-In			no	no	yes(1)	
GPP_A19 / ISH_GP1	GPP_A19	VCCPGPPA	1.8 V or 3.3 V	ISH_GP1	inout					GP-In			no	no	yes(1)	
GPP_A20 / ISH_GP2	GPP_A20	VCCPGPPA	1.8 V or 3.3 V	ISH_GP2	inout					GP-In			no	no	yes(1)	
GPP_A21 / ISH_GP3	GPP_A21	VCCPGPPA	1.8 V or 3.3 V	ISH_GP3	inout					GP-In			no	no	yes(1)	
GPP_A22 / ISH_GP4	GPP_A22	VCCPGPPA	1.8 V or 3.3 V	ISH_GP4	inout					GP-In			no	no	yes(1)	
GPP_A23 / ISH_GP5	GPP_A23	VCCPGPPA	1.8 V or 3.3 V	ISH_GP5	inout					GP-In			no	no	yes(1)	
Primary Well Group B (Per-Group 1.8 V or 3.3 V)																
GPP_B0	GPP_B0	VCCPGPPBCH	1.8 V or 3.3 V							GP-Out			no	no	yes(2)	As GPO, the signal defaults to '0'
GPP_B1	GPP_B1	VCCPGPPBCH	1.8 V or 3.3 V							GP-Out			no	no	yes(2)	As GPO, the signal defaults to '0'
GPP_B2 / VRALERT#	GPP_B2	VCCPGPPBCH	1.8 V or 3.3 V	VRALERT#	in					GP-In			no	no	yes(1)	
GPP_B3 / CPU_GP2	GPP_B3	VCCPGPPBCH	1.8 V or 3.3 V	CPU_GP2	in					GP-In			no	no	yes(1)	
GPP_B4 / CPU_GP3	GPP_B4	VCCPGPPBCH	1.8 V or 3.3 V	CPU_GP3	in					GP-In			no	no	yes(1)	
GPP_B5 / SRCCLKREQ0#	GPP_B5	VCCPGPPBCH	1.8 V or 3.3 V	SRCCLKREQ0#	iod					GP-In			no	no	yes(1)	
GPP_B6 / SRCCLKREQ1#	GPP_B6	VCCPGPPBCH	1.8 V or 3.3 V	SRCCLKREQ1#	iod					GP-In			no	no	yes(1)	
GPP_B7 / SRCCLKREQ2#	GPP_B7	VCCPGPPBCH	1.8 V or 3.3 V	SRCCLKREQ2#	iod					GP-In			no	no	yes(1)	
GPP_B8 / SRCCLKREQ3#	GPP_B8	VCCPGPPBCH	1.8 V or 3.3 V	SRCCLKREQ3#	iod					GP-In			no	no	yes(1)	
GPP_B9 / SRCCLKREQ4#	GPP_B9	VCCPGPPBCH	1.8 V or 3.3 V	SRCCLKREQ4#	iod					GP-In			no	no	yes(1)	

Signal Name	GPIO	Power Well	Voltage Tolerance	Native Function 1	Native Dir 1	Native Function 2	Native Dir 2	Native Function 3	Native Dir 3	Default	Strap	Pin Strap Termination	NMI/SMI Capable	Input Deglitch	Output Power Sequence Deglitch	Notes
GPP_B10 / SRCCLKREQ5#	GPP_B10	VCCPGPPBCH	1.8 V or 3.3 V	SRCCLKREQ5#	iod					GP-In			no	no	yes(1)	
GPP_B11	GPP_B11	VCCPGPPBCH	1.8 V or 3.3 V							GP-Out			no	no	yes(2)	As GPO, the signal defaults to '0'
GPP_B12 / SLP_S0#	GPP_B12	VCCPGPPBCH	1.8 V or 3.3 V	SLP_S0#	out					Native F1			no	no	yes(3)	
GPP_B13 / PLTRST#	GPP_B13	VCCPGPPBCH	1.8 V or 3.3 V	PLTRST#	out					Native F1			no	no	yes(2)	
GPP_B14 / SPKR	GPP_B14	VCCPGPPBCH	1.8 V or 3.3 V	SPKR	out					GP-Out	Top Swap Override	20K PD	NMI / SMI	no	no	Strap read at rising edge of PCH_PWROK. The internal 20 kohm pull-down is disabled after PCH_PWROK is high. As GPO, the signal defaults to '0'
GPP_B15 / GSPI0_CS#	GPP_B15	VCCPGPPBCH	1.8 V or 3.3 V	GSPI0_CS#	out					GP-In			no	no	yes(1)	
GPP_B16 / GSPI0_CLK	GPP_B16	VCCPGPPBCH	1.8 V or 3.3 V	GSPI0_CLK	out					GP-In			no	no	yes(1)	
GPP_B17 / GSPI0_MISO	GPP_B17	VCCPGPPBCH	1.8 V or 3.3 V	GSPI0_MISO	in					GP-In			no	no	yes(1)	
GPP_B18 / GSPI0_MOSI	GPP_B18	VCCPGPPBCH	1.8 V or 3.3 V	GSPI0_MOSI	out					GP-Out	No Reboot	20K PD	no	no	no	Strap read at rising edge of PCH_PWROK. The internal 20 kohm pull-down is disabled after PCH_PWROK is high. As GPO, the signal defaults to '0'
GPP_B19 / GSPI1_CS#	GPP_B19	VCCPGPPBCH	1.8 V or 3.3 V	GSPI1_CS#	out					GP-In			no	no	yes(1)	
GPP_B20 / GSPI1_CLK	GPP_B20	VCCPGPPBCH	1.8 V or 3.3 V	GSPI1_CLK	out					GP-In			NMI / SMI	no	yes(1)	
GPP_B21 / GSPI1_MISO	GPP_B21	VCCPGPPBCH	1.8 V or 3.3 V	GSPI1_MISO	in					GP-In			no	no	yes(1)	
GPP_B22 / GSPI1_MOSI	GPP_B22	VCCPGPPBCH	1.8 V or 3.3 V	GSPI1_MOSI	out					GP-Out	Boot BIOS Strap Bit	20K PD	no	no	no	Strap read at rising edge of PCH_PWROK. The internal 20 kohm Pull-down is disabled after PCH_PWROK is high. As GPO, the signal defaults to '0'
GPP_B23 / SML1ALERT# / PCHHOT#	GPP_B23	VCCPGPPBCH	1.8 V or 3.3 V	SML1ALERT#	iod	PCHHOT#	od			GP-Out	Reserved	20K PD	NMI / SMI	yes	no	This strap should sample LOW at the rising edge of RSMRST#. There should NOT be any on-board device driving it to opposite direction during strap sampling. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts. Note: When used as PCHHOT# and strap low, a 150 kohm weak board pull-up is recommended to ensure it does not override the internal pull-down strap sampling. As GPO, the signal defaults to '0'
Primary Well Group C (Per-Group 1.8 V or 3.3 V)																
GPP_C0 / SMBCLK	GPP_C0	VCCPGPPBCH	1.8 V or 3.3 V	SMBCLK	iod					Native F1			no	yes	yes(1)	
GPP_C1 / SMBDATA	GPP_C1	VCCPGPPBCH	1.8 V or 3.3 V	SMBDATA	iod					Native F1			no	yes	yes(1)	
GPP_C2 / SMBALERT#	GPP_C2	VCCPGPPBCH	1.8 V or 3.3 V	SMBALERT#	iod					GP-Out	TLS Confidentiality	20K PD	no	yes	no	Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts. As GPO, the signal defaults to '0'
GPP_C3 / SML0CLK	GPP_C3	VCCPGPPBCH	1.8 V or 3.3 V	SML0CLK	iod					Native F1			no	yes	yes(1)	
GPP_C4 / SML0DATA	GPP_C4	VCCPGPPBCH	1.8 V or 3.3 V	SML0DATA	iod					Native F1			no	yes	yes(1)	
GPP_C5 / SML0ALERT#	GPP_C5	VCCPGPPBCH	1.8 V or 3.3 V	SML0ALERT#	iod					GP-Out	eSPI or LPC	20K PD	no	yes	no	Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts. As GPO, the signal defaults to '0'
GPP_C6 / SML1CLK	GPP_C6	VCCPGPPBCH	1.8 V or 3.3 V	SML1CLK	iod					GP-In			no	yes	yes(1)	
GPP_C7 / SML1DATA	GPP_C7	VCCPGPPBCH	1.8 V or 3.3 V	SML1DATA	iod					GP-In			no	yes	yes(1)	
GPP_C8 / UART0A_RXD	GPP_C8	VCCPGPPBCH	1.8 V or 3.3 V	UART0_RXD	in					GP-In			no	no	yes(1)	
GPP_C9 / UART0_TXD	GPP_C9	VCCPGPPBCH	1.8 V or 3.3 V	UART0_TXD	out					GP-In			no	no	yes(1)	
GPP_C10 / UART0_RTS#	GPP_C10	VCCPGPPBCH	1.8 V or 3.3 V	UART0_RTS#	out					GP-In			no	no	yes(1)	
GPP_C11 / UART0_CTS#	GPP_C11	VCCPGPPBCH	1.8 V or 3.3 V	UART0_CTS#	in					GP-In			no	no	yes(1)	
GPP_C12 / UART1_RXD / ISH_UART1_RXD	GPP_C12	VCCPGPPBCH	1.8 V or 3.3 V	UART1_RXD	in	ISH_UART1_RXD	in			GP-In			no	no	yes(1)	
GPP_C13 / UART1_TXD / ISH_UART1_TXD	GPP_C13	VCCPGPPBCH	1.8 V or 3.3 V	UART1_TXD	out	ISH_UART1_TXD	out			GP-In			no	no	yes(1)	
GPP_C14 / UART1_RTS# / ISH_UART1_RTS#	GPP_C14	VCCPGPPBCH	1.8 V or 3.3 V	UART1_RTS#	out	ISH_UART1_RTS#	out			GP-In			no	no	yes(1)	
GPP_C15 / UART1_CTS# / ISH_UART1_CTS#	GPP_C15	VCCPGPPBCH	1.8 V or 3.3 V	UART1_CTS#	in	ISH_UART1_CTS#	in			GP-In			no	no	yes(1)	
GPP_C16 / I2C0_SDA	GPP_C16	VCCPGPPBCH	1.8 V or 3.3 V	I2C0_SDA	od					GP-In			no	yes	yes(1)	
GPP_C17 / I2C0_SCL	GPP_C17	VCCPGPPBCH	1.8 V or 3.3 V	I2C0_SCL	od					GP-In			no	yes	yes(1)	
GPP_C18 / I2C1_SDA	GPP_C18	VCCPGPPBCH	1.8 V or 3.3 V	I2C1_SDA	od					GP-In			no	yes	yes(1)	

Signal Name	GPIO	Power Well	Voltage Tolerance	Native Function 1	Native Dir 1	Native Function 2	Native Dir 2	Native Function 3	Native Dir 3	Default	Strap	Pin Strap Termination	NMI/SMI Capable	Input Deglitch	Output Power Sequence Deglitch	Notes
GPP_C19 / I2C1_SCL	GPP_C19	VCCPGPPBCH	1.8 V or 3.3 V	I2C1_SCL	od					GP-In			no	yes	yes(1)	
GPP_C20 / UART2_RXD	GPP_C20	VCCPGPPBCH	1.8 V or 3.3 V	UART2_RXD	in					GP-In			no	no	yes(1)	
GPP_C21 / UART2_TXD	GPP_C21	VCCPGPPBCH	1.8 V or 3.3 V	UART2_TXD	out					GP-In			no	no	yes(1)	
GPP_C22 / UART2_RTS#	GPP_C22	VCCPGPPBCH	1.8 V or 3.3 V	UART2_RTS#	out					GP-In			NMI / SMI	no	yes(1)	
GPP_C23 / UART2_CTS#	GPP_C23	VCCPGPPBCH	1.8 V or 3.3 V	UART2_CTS#	in					GP-In			NMI / SMI	no	yes(1)	
Primary Well Group D (Per-Group 1.8 V or 3.3 V)																
GPP_D0	GPP_D0	VCCPGPPD	1.8 V or 3.3 V							GP-In			NMI / SMI	no	yes(1)	This GPIO is blink capable
GPP_D1	GPP_D1	VCCPGPPD	1.8 V or 3.3 V							GP-In			NMI / SMI	no	yes(1)	This GPIO is blink capable
GPP_D2	GPP_D2	VCCPGPPD	1.8 V or 3.3 V							GP-In			NMI / SMI	no	yes(1)	This GPIO is blink capable
GPP_D3	GPP_D3	VCCPGPPD	1.8 V or 3.3 V							GP-In			NMI / SMI	no	yes(1)	This GPIO is blink capable
GPP_D4 / ISH_I2C2_SDA / I2C3_SDA	GPP_D4	VCCPGPPD	1.8 V or 3.3 V	ISH_I2C2_SDA	iod	I2C3_SDA	iod			GP-In			NMI / SMI	yes	yes(1)	This GPIO is blink capable
GPP_D5 / I2S0_SFRM	GPP_D5	VCCPGPPD	1.8 V or 3.3 V	I2S0_SFRM	inout					GP-In			no	no	yes(2)	
GPP_D6 / I2S0_TXD	GPP_D6	VCCPGPPD	1.8 V or 3.3 V	I2S0_TXD	out					GP-In			no	no	yes(1)	
GPP_D7 / I2S0_RXD	GPP_D7	VCCPGPPD	1.8 V or 3.3 V	I2S0_RXD	in					GP-In			no	no	yes(1)	
GPP_D8 / I2S0_SCLK	GPP_D8	VCCPGPPD	1.8 V or 3.3 V	I2S0_SCLK	inout					GP-In			no	no	yes(1)	
GPP_D9	GPP_D9	VCCPGPPD	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_D10	GPP_D10	VCCPGPPD	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_D11	GPP_D11	VCCPGPPD	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_D12	GPP_D12	VCCPGPPD	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_D13 / ISH_UART0_RXD / I2C2_SDA	GPP_D13	VCCPGPPD	1.8 V or 3.3 V	ISH_UART0_RXD	in			I2C2_SDA	iod	GP-In			no	no	yes(1)	
GPP_D14 / ISH_UART0_TXD / I2C2_SCL	GPP_D14	VCCPGPPD	1.8 V or 3.3 V	ISH_UART0_TXD	out			I2C2_SCL	iod	GP-In			no	no	yes(1)	
GPP_D15 / ISH_UART0_RTS#	GPP_D15	VCCPGPPD	1.8 V or 3.3 V	ISH_UART0_RTS#	out					GP-In			no	no	yes(1)	
GPP_D16 / ISH_UART0_CTS#	GPP_D16	VCCPGPPD	1.8 V or 3.3 V	ISH_UART0_CTS#	in					GP-In			no	no	yes(1)	
GPP_D17 / DMIC_CLK1	GPP_D17	VCCPGPPD	1.8 V or 3.3 V	DMIC_CLK1	out					GP-In			no	no	yes(1)	
GPP_D18 / DMIC_DATA1	GPP_D18	VCCPGPPD	1.8 V or 3.3 V	DMIC_DATA1	in					GP-In			no	no	yes(1)	
GPP_D19 / DMIC_CLK0	GPP_D19	VCCPGPPD	1.8 V or 3.3 V	DMIC_CLK0	out					GP-In			no	no	yes(1)	
GPP_D20 / DMIC_DATA0	GPP_D20	VCCPGPPD	1.8 V or 3.3 V	DMIC_DATA0	in					GP-In			no	no	yes(1)	
GPP_D21	GPP_D21	VCCPGPPD	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_D22	GPP_D22	VCCPGPPD	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_D23 / ISH_I2C2_SCL / I2C3_SCL	GPP_D23	VCCPGPPD	1.8 V or 3.3 V	ISH_I2C2_SCL	iod	I2C3_SCL	iod			GP-In			no	yes	yes(1)	
Primary Well Group E (Per-Group 1.8 V or 3.3 V)																
GPP_E0 / SATAXPCIE0 / SATAGP0	GPP_E0	VCCPGPPEF	1.8 V or 3.3 V	SATAXPCIE0	in	SATAGP0	in			Native F1/GP-In			NMI / SMI	no	yes(1)	Native F1 if SATA / PCIe GP Select for Port 0 soft strap = 00b or 01b; GP-In if soft strap = 11b. Note: Different Connectors have different polarity for the SATAxPCIe select. Note: Default state is GP-In before soft straps are loaded or in the case the soft straps are invalid
GPP_E1 / SATAXPCIE1 / SATAGP1	GPP_E1	VCCPGPPEF	1.8 V or 3.3 V	SATAXPCIE1	in	SATAGP1	in			Native F1/GP-In			NMI / SMI	no	yes(1)	Native F1 if SATA / PCIe GP Select for Port 1 soft strap = 00b or 01b; GP-In if soft strap = 11b. Note: Different Connectors have different polarity for the SATAxPCIe select. Note: Default state is GP-In before soft straps are loaded or in the case the soft straps are invalid
GPP_E2 / SATAXPCIE2 / SATAGP2	GPP_E2	VCCPGPPEF	1.8 V or 3.3 V	SATAXPCIE2	in	SATAGP2	in			Native F1/GP-In			NMI / SMI	no	yes(1)	Native F1 if SATA / PCIe GP Select for Port 2 soft strap = 00b or 01b; GP-In if soft strap = 11b. Note: Different Connectors have different polarity for the SATAxPCIe select. Note: Default state is GP-In before soft straps are loaded or in the case the soft straps are invalid
GPP_E3 / CPU_GP0	GPP_E3	VCCPGPPEF	1.8 V or 3.3 V	CPU_GP0	in					GP-In			NMI / SMI	no	yes(1)	
GPP_E4 / DEVSLP0	GPP_E4	VCCPGPPEF	1.8 V or 3.3 V	DEVSLP0	od					GP-In			NMI / SMI	no	yes(1)	
GPP_E5 / DEVSLP1	GPP_E5	VCCPGPPEF	1.8 V or 3.3 V	DEVSLP1	od					GP-In			NMI / SMI	no	yes(1)	

Signal Name	GPIO	Power Well	Voltage Tolerance	Native Function 1	Native Dir 1	Native Function 2	Native Dir 2	Native Function 3	Native Dir 3	Default	Strap	Pin Strap Termination	NMI/SMI Capable	Input Deglitch	Output Power Sequence Deglitch	Notes
GPP_E6 / DEVSLP2	GPP_E6	VCCPGPPEF	1.8 V or 3.3 V	DEVSLP2	od					GP-In			NMI / SMI	no	yes(1)	
GPP_E7 / CPU_GP1	GPP_E7	VCCPGPPEF	1.8 V or 3.3 V	CPU_GP1	in					GP-In			NMI / SMI	no	yes(1)	
GPP_E8 / SATALED#	GPP_E8	VCCPGPPEF	1.8 V or 3.3 V	SATALED#	od					GP-In			NMI / SMI	no	yes(1)	
GPP_E9 / USB_OC0#	GPP_E9	VCCPGPPEF	1.8 V or 3.3 V	USB_OC0#	in					GP-In			no	no	yes(1)	The signal has a 20K pull-down which is disabled after RSMRST# de-asserts
GPP_E10 / USB_OC1#	GPP_E10	VCCPGPPEF	1.8 V or 3.3 V	USB_OC1#	in					GP-In			no	no	yes(1)	The signal has a 20K pull-down which is disabled after RSMRST# de-asserts
GPP_E11 / USB_OC2#	GPP_E11	VCCPGPPEF	1.8 V or 3.3 V	USB_OC2#	in					GP-In			no	no	yes(1)	The signal has a 20K pull-down which is disabled after RSMRST# de-asserts
GPP_E12 / USB_OC3#	GPP_E12	VCCPGPPEF	1.8 V or 3.3 V	USB_OC3#	in					GP-In			no	no	yes(1)	The signal has a 20K pull-down which is disabled after RSMRST# de-asserts
Primary Well Group F (Per-Group 1.8 V or 3.3 V)																
GPP_F0 / SATAXPCIE3 / SATAGP3	GPP_F0	VCCPGPPEF	1.8 V or 3.3 V	SATAXPCIE3	in	SATAGP3	in			Native F1/GP-In			NMI / SMI	no	yes(1)	Native F1 if SATA / PCIe GP Select for Port 3 soft strap = 00b or 01b; GP-In if soft strap = 11b. Note: Different Connectors have different polarity for the SATAxPCIe select. Note: Default state is GP-In before soft straps are loaded or in the case the soft straps are invalid
GPP_F1 / SATAXPCIE4 / SATAGP4	GPP_F1	VCCPGPPEF	1.8 V or 3.3 V	SATAXPCIE4	in	SATAGP4	in			Native F1/GP-In			NMI / SMI	no	yes(1)	Native F1 if SATA / PCIe GP Select for Port 4 soft strap = 00b or 01b; GP-In if soft strap = 11b. Note: Different Connectors have different polarity for the SATAxPCIe select. Note: Default state is GP-In before soft straps are loaded or in the case the soft straps are invalid
GPP_F2 / SATAXPCIE5 / SATAGP5	GPP_F2	VCCPGPPEF	1.8 V or 3.3 V	SATAXPCIE5	in	SATAGP5	in			Native F1/GP-In			NMI / SMI	no	yes(1)	Native F1 if SATA / PCIe GP Select for Port 5 soft strap = 00b or 01b; GP-In if soft strap = 11b. Note: Different Connectors have different polarity for the SATAxPCIe select. Note: Default state is GP-In before soft straps are loaded or in the case the soft straps are invalid
GPP_F3	GPP_F3	VCCPGPPEF	1.8 V or 3.3 V							GP-In			NMI / SMI	no	yes(1)	
GPP_F4	GPP_F4	VCCPGPPEF	1.8 V or 3.3 V							GP-In			NMI / SMI	no	yes(1)	
GPP_F5 / DEVSLP3	GPP_F5	VCCPGPPEF	1.8 V or 3.3 V	DEVSLP3	od					GP-In			no	no	yes(1)	
GPP_F6 / DEVSLP4	GPP_F6	VCCPGPPEF	1.8 V or 3.3 V	DEVSLP4	od					GP-In			no	no	yes(1)	
GPP_F7 / DEVSLP5	GPP_F7	VCCPGPPEF	1.8 V or 3.3 V	DEVSLP5	od					GP-In			no	no	yes(1)	
GPP_F8	GPP_F8	VCCPGPPEF	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_F9	GPP_F9	VCCPGPPEF	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_F10 / SCLOCK	GPP_F10	VCCPGPPEF	1.8 V or 3.3 V	SCLOCK	od					GP-In			no	no	yes(1)	
GPP_F11 / SLOAD	GPP_F11	VCCPGPPEF	1.8 V or 3.3 V	SLOAD	od					GP-In			no	no	yes(1)	
GPP_F12 / SDATAOUT1	GPP_F12	VCCPGPPEF	1.8 V or 3.3 V	SDATAOUT1	od					GP-In			no	no	yes(1)	
GPP_F13 / SDATAOUT0	GPP_F13	VCCPGPPEF	1.8 V or 3.3 V	SDATAOUT0	od					GP-In			no	no	yes(1)	
GPP_F14	GPP_F14	VCCPGPPEF	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_F15 / USB2_OC4#	GPP_F15	VCCPGPPEF	1.8 V or 3.3 V	USB_OC4#	in					GP-In			no	no	yes(1)	
GPP_F16 / USB2_OC5#	GPP_F16	VCCPGPPEF	1.8 V or 3.3 V	USB_OC5#	in					GP-In			no	no	yes(1)	
GPP_F17 / USB2_OC6#	GPP_F17	VCCPGPPEF	1.8 V or 3.3 V	USB_OC6#	in					GP-In			no	no	yes(1)	
GPP_F18 / USB2_OC7#	GPP_F18	VCCPGPPEF	1.8 V or 3.3 V	USB_OC7#	in					GP-In			no	no	yes(1)	
GPP_F19 / eDP_VDDEN	GPP_F19	VCCPGPPEF	1.8 V or 3.3 V	eDP_VDDEN	out					GP-In			no	no	yes(1)	

Signal Name	GPIO	Power Well	Voltage Tolerance	Native Function 1	Native Dir 1	Native Function 2	Native Dir 2	Native Function 3	Native Dir 3	Default	Strap	Pin Strap Termination	NMI/SMI Capable	Input Deglitch	Output Power Sequence Deglitch	Notes
GPP_F20 / eDP_BKLTEN	GPP_F20	VCCPGPPEF	1.8 V or 3.3 V	eDP_BKLTEN	out					GP-In			no	no	yes(1)	
GPP_F21 / eDP_BKLTCTL	GPP_F21	VCCPGPPEF	1.8 V or 3.3 V	eDP_BKLTCTL	out					GP-In			no	no	yes(1)	
GPP_F22	GPP_F22	VCCPGPPEF	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_F23	GPP_F23	VCCPGPPEF	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
Primary Well Group G (Per-Group 1.8 V or 3.3 V)																
GPP_G0	GPP_G0	VCCPGPPG	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_G1	GPP_G1	VCCPGPPG	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_G2	GPP_G2	VCCPGPPG	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_G3	GPP_G3	VCCPGPPG	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_G4	GPP_G4	VCCPGPPG	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_G5	GPP_G5	VCCPGPPG	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_G6	GPP_G6	VCCPGPPG	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_G7	GPP_G7	VCCPGPPG	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
GPP_G8	GPP_G8	VCCPGPPG	1.8 V or 3.3 V							GP-In			no		yes(1)	
GPP_G9	GPP_G9	VCCPGPPG	1.8 V or 3.3 V							GP-In			no		yes(1)	
GPP_G10	GPP_G10	VCCPGPPG	1.8 V or 3.3 V							GP-In			no		yes(1)	
GPP_G11	GPP_G11	VCCPGPPG	1.8 V or 3.3 V							GP-In			no		yes(1)	
GPP_G12 / GSXDOUT	GPP_G12	VCCPGPPG	1.8 V or 3.3 V	GSXDOUT	out					GP-In			no		yes(1)	
GPP_G13 / GSXSLOAD	GPP_G13	VCCPGPPG	1.8 V or 3.3 V	GSXSLOAD	out					GP-In			no		yes(1)	
GPP_G14 / GSXDIN	GPP_G14	VCCPGPPG	1.8 V or 3.3 V	GSXDIN	in					GP-In			no		yes(1)	
GPP_G15 / GSXRESET#	GPP_G15	VCCPGPPG	1.8 V or 3.3 V	GSXRESET#	out					GP-In			no		yes(1)	
GPP_G16 / GSXCLK	GPP_G16	VCCPGPPG	1.8 V or 3.3 V	GSXCLK	out					GP-In			no		yes(1)	
GPP_G17	GPP_G17	VCCPGPPG	1.8 V or 3.3 V							GP-In			no		yes(1)	
GPP_G18	GPP_G18	VCCPGPPG	1.8 V or 3.3 V							GP-In			no		yes(1)	
GPP_G19	GPP_G19	VCCPGPPG	1.8 V or 3.3 V							GP-In			no		yes(1)	
GPP_G20	GPP_G20	VCCPGPPG	1.8 V or 3.3 V							GP-In			no		yes(1)	
GPP_G21	GPP_G21	VCCPGPPG	1.8 V or 3.3 V							GP-In			no		yes(1)	
GPP_G22	GPP_G22	VCCPGPPG	1.8 V or 3.3 V							GP-In			no		yes(1)	
GPP_G23	GPP_G23	VCCPGPPG	1.8 V or 3.3 V							GP-In			no		yes(1)	
Primary Well Group H (Per-Group 1.8 V or 3.3 V)																
GPP_H0 / SRCCLKREQ6#	GPP_H0	VCCPGPPBCH	1.8 V or 3.3 V	SRCCLKREQ6#	iod					GP-In			no	no	yes(1)	
GPP_H1 / SRCCLKREQ7#	GPP_H1	VCCPGPPBCH	1.8 V or 3.3 V	SRCCLKREQ7#	iod					GP-In			no	no	yes(1)	
GPP_H2 / SRCCLKREQ8#	GPP_H2	VCCPGPPBCH	1.8 V or 3.3 V	SRCCLKREQ8#	iod					GP-In			no	no	yes(1)	
GPP_H3 / SRCCLKREQ9#	GPP_H3	VCCPGPPBCH	1.8 V or 3.3 V	SRCCLKREQ9#	iod					GP-In			no	no	yes(1)	
GPP_H4 / SRCCLKREQ10#	GPP_H4	VCCPGPPBCH	1.8 V or 3.3 V	SRCCLKREQ10#	iod					GP-In			no	no	yes(1)	
GPP_H5 / SRCCLKREQ11#	GPP_H5	VCCPGPPBCH	1.8 V or 3.3 V	SRCCLKREQ11#	iod					GP-In			no	no	yes(1)	
GPP_H6 / SRCCLKREQ12#	GPP_H6	VCCPGPPBCH	1.8 V or 3.3 V	SRCCLKREQ12#	iod					GP-In			no	no	yes(1)	
GPP_H7 / SRCCLKREQ13#	GPP_H7	VCCPGPPBCH	1.8 V or 3.3 V	SRCCLKREQ13#	iod					GP-In			no	no	yes(1)	
GPP_H8 / SRCCLKREQ14#	GPP_H8	VCCPGPPBCH	1.8 V or 3.3 V	SRCCLKREQ14#	iod					GP-In			no	no	yes(1)	
GPP_H9 / SRCCLKREQ15#	GPP_H9	VCCPGPPBCH	1.8 V or 3.3 V	SRCCLKREQ15#	iod					GP-In			no	no	yes(1)	
GPP_H10	GPP_H10	VCCPGPPBCH	1.8 V or 3.3 V							GP-In			no	yes	yes(1)	

Signal Name	GPIO	Power Well	Voltage Tolerance	Native Function 1	Native Dir 1	Native Function 2	Native Dir 2	Native Function 3	Native Dir 3	Default	Strap	Pin Strap Termination	NMI/SMI Capable	Input Deglitch	Output Power Sequence Deglitch	Notes
GPP_H11	GPP_H11	VCCPGPPBCH	1.8 V or 3.3 V							GP-In			no	yes	yes(1)	
GPP_H12	GPP_H12	VCCPGPPBCH	1.8 V or 3.3 V							GP-Out	Reserved	20K PD	no	yes	no	Strap read at rising edge of RSMRST#. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. The internal 20 kohm ± 30% pull-down is disabled after RSMRST# de-asserts. As GPO, the signal defaults to '0'
GPP_H13	GPP_H13	VCCPGPPBCH	1.8 V or 3.3 V							GP-In			no	yes	yes(1)	
GPP_H14	GPP_H14	VCCPGPPBCH	1.8 V or 3.3 V							GP-In			no	yes	yes(1)	
GPP_H15	GPP_H15	VCCPGPPBCH	1.8 V or 3.3 V							GP-In			no	yes	yes(1)	
GPP_H16	GPP_H16	VCCPGPPBCH	1.8 V or 3.3 V							GP-In			no	yes	yes(1)	
GPP_H17	GPP_H17	VCCPGPPBCH	1.8 V or 3.3 V							GP-In			no	yes	Yes (1)	
GPP_H18	GPP_H18	VCCPGPPBCH	1.8 V or 3.3 V							GP-In			no	yes	yes(1)	
GPP_H19 / ISH_I2C0_SDA	GPP_H19	VCCPGPPBCH	1.8 V or 3.3 V	ISH_I2C0_SDA	iod					GP-In			no	yes	yes(1)	
GPP_H20 / ISH_I2C0_SCL	GPP_H20	VCCPGPPBCH	1.8 V or 3.3 V	ISH_I2C0_SCL	iod					GP-In			no	yes	yes(1)	
GPP_H21 / ISH_I2C1_SDA	GPP_H21	VCCPGPPBCH	1.8 V or 3.3 V	ISH_I2C1_SDA	iod					GP-In			no	yes	yes(1)	
GPP_H22 / ISH_I2C1_SCL	GPP_H22	VCCPGPPBCH	1.8 V or 3.3 V	ISH_I2C1_SCL	iod					GP-In			no	yes	yes(1)	
GPP_H23	GPP_H23	VCCPGPPBCH	1.8 V or 3.3 V							GP-In			no	no	yes(1)	
Primary Well Group I (3.3 V Only)																
GPP_I0 / DDPB_HPD0	GPP_I0	VCCPRIM_3P3	3.3 V	DDPB_HPD0	in					GP-In			NMI /SMI	no	yes(1)	
GPP_I1 / DDPC_HPD1	GPP_I1	VCCPRIM_3P3	3.3 V	DDPC_HPD1	in					GP-In			NMI /SMI	no	yes(1)	
GPP_I2 / DDPD_HPD2	GPP_I2	VCCPRIM_3P3	3.3 V	DDPD_HPD2	in					GP-In			NMI /SMI	no	yes(1)	
GPP_I3 / DDPE_HPD3	GPP_I3	VCCPRIM_3P3	3.3 V	DDPE_HPD3	in					GP-In			NMI /SMI	no	yes(1)	
GPP_I4 / EDP_HPD	GPP_I4	VCCPRIM_3P3	3.3 V	EDP_HPD	in					GP-In			no	no	yes(1)	
GPP_I5 / DDPB_CTRLCLK	GPP_I5	VCCPRIM_3P3	3.3 V	DDPB_CTRLCLK	iod					GP-In			no	Yes	yes(1)	
GPP_I6 / DDPB_CTRLDATA	GPP_I6	VCCPRIM_3P3	3.3 V	DDPB_CTRLDATA	iod					GP-Out	Display Port B Detected	20K PD	no	Yes	no	Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% pull-down is disabled after PCH_PWROK is high. As GPO, the signal defaults to '0'
GPP_I7 / DDPC_CTRLCLK	GPP_I7	VCCPRIM_3P3	3.3 V	DDPC_CTRLCLK	iod					GP-In			no	Yes	yes(1)	
GPP_I8 / DDPC_CTRLDATA	GPP_I8	VCCPRIM_3P3	3.3 V	DDPC_CTRLDATA	iod					GP_Out	Display Port C Detected	20K PD	no	Yes	no	Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% pull-down is disabled after PCH_PWROK is high. As GPO, the signal defaults to '0'
GPP_I9 / DDPD_CTRLCLK	GPP_I9	VCCPRIM_3P3	3.3 V	DDPD_CTRLCLK	iod					GP-In			no	Yes	yes(1)	
GPP_I10 / DDPD_CTRLDATA	GPP_I10	VCCPRIM_3P3	3.3 V	DDPD_CTRLDATA	iod					GP-Out	Display Port D Detected	20K PD	no	Yes	no	Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% pull-down is disabled after PCH_PWROK is high. As GPO, the signal defaults to '0'
Deep Sleep Well Group (3.3 V Only)																
GPD0 / BATLOW#	GPD0	VCCDSW_3P3	3.3 V	BATLOW#	in					Native F1			no	no	yes(1)	
GPD1 / ACPRESENT	GPD1	VCCDSW_3P3	3.3 V	ACPRESENT	in					Native F1			no	no	yes(1)	
GPD2 / LAN_WAKE#	GPD2	VCCDSW_3P3	3.3 V	LAN_WAKE#	in					Native F1			no	no	yes(1)	
GPD3 / PWRBTN#	GPD3	VCCDSW_3P3	3.3 V	PWRBTN#	in					Native F1			no	yes	yes(1)	
GPD4 / SLP_S3#	GPD4	VCCDSW_3P3	3.3 V	SLP_S3#	out					Native F1			no	no	yes(2)	
GPD5 / SLP_S4#	GPD5	VCCDSW_3P3	3.3 V	SLP_S4#	out					Native F1			no	no	yes(2)	
GPD6 / SLP_A#	GPD6	VCCDSW_3P3	3.3 V	SLP_A#	out					Native F1			no	no	yes(2)	

Signal Name	GPIO	Power Well	Voltage Tolerance	Native Function 1	Native Dir 1	Native Function 2	Native Dir 2	Native Function 3	Native Dir 3	Default	Strap	Pin Strap Termination	NMI/SMI Capable	Input Deglitch	Output Power Sequence Deglitch	Notes
GPD7 / RSVD	GPD7	VCCDSW_3P3	3.3 V	Reserved Functionality						Reserved Functionality (Needs to be programmed for GPIO)			no	no	yes(2)	The reserved functionality defaults to an output. During reset, the signal is low and right after reset it’s high by default.
GPD8 / SUSCLK	GPD8	VCCDSW_3P3	3.3 V	SUSCLK	out					Native F1			no	no	yes(2)	
GPD9 / SLP_WLAN#	GPD9	VCCDSW_3P3	3.3 V	SLP_WLAN#	out					Native F1			no	no	yes(2)	
GPD10 / SLP_S5#	GPD10	VCCDSW_3P3	3.3 V	SLP_S5#	out					Native F1			no	no	yes(2)	
GPD11 / LANPHYPC	GPD11	VCCDSW_3P3	3.3 V	LANPHYPC	out					Native F1/GP-In			no	no	yes(2)	

Deglitch Legend

yes(1) - Output Hi-Z with no internal glitch-free resistortor during resecctive pin power sequencing

yes(2) - output Hi-Z with integrated 20 kohm ± 30% pull-down during respective pin power sequencing

yes(3) - output Hi-Z with integrated 20 kohm ± 30% pull-up during respective pin power sequencing