Intel® 500 Series Chipset Family On-Package Platform Controller Hub (PCH)

Specification Update

July 2021

Revision 008

Document Number: 630747-008

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Revision History

Document Number	Revision Number	Description	Revision Date
630747	008	• Updated – xHCI D3 Exit Timing Spec Clarification	July 2021
630747	007	• Added – FIVR Transitions During Deep Sx Entry with Integrated GbE Enabled – Ring Oscillator Calibration – xHCI D3 Exit Timing Spec Clarification • Updated – PCIe* Clock and PCIe Reference Clock to Processor Maximum Rising/Falling Edge Rate and V_{CROSS}	July 2021
630747	006	• Added – USB VTIO Device Capabilities Field Length	June 2020
630747	005	• Added – Integrated GbE Controller Reset on D3 Exit – PCIe Clock Maximum Rising/Falling Edge Rate and V_{CROSS} – SATA Controller Support for Automatic Partial to Slumber Transition (APST) Feature	January 2021
630747	004	• Added – PCH and Processor Sync Error During C8 Entry	December 2020
630747	003	• Added – SX_EXIT_HOLDOFF# Not Functional with eSPI Enabled	November 2020
630747	002	• Added – Unexpected Shutdown with VCCIN_AUX Retention Mode Enabled – Time-Sensitive Networking Incorrectly Advertised RX FIFO Size (for IoT Platforms only) – xHCI Serial Bus Release Number Version	October 2020
630747	001	• Initial Release	August 2020

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1 Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents table. This document is a compilation of device and document errata, and specification clarifications, and changes. It is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the nomenclature section of this document are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that has not been previously published.

1.1 Affected Documents

Document Title	Document Number
Intel® 500 Series Chipset Family On-Package Platform Controller Hub (PCH) Datasheet, Volume 1 of 2	631119
Intel® 500 Series Chipset Family On-Package Platform Controller Hub (PCH) Datasheet, Volume 2 of 2	631120
11th Generation Intel® Core™ Processor Family for IoT Platforms Datasheet Addendum	632133

1.2 Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

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2 Summary Tables of Changes

The following tables indicate the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

2.1 Codes Used in Summary Table

Stepping	Description
X	Erratum exists in the stepping indicated. Specification Change that applies to the stepping indicated.
(No mark) or (Blank Box)	This erratum is fixed or not applicable in listed stepping or Specification Change does not apply to listed stepping.

Status	Description
Doc	Document change or update that is implemented.
Planned Fix	This erratum may be fixed in a future stepping of the product.
Fixed	This erratum has been previously fixed in Intel® hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

2.2 Errata Summary Table

Erratum ID / Internal Reference#	Stepping / B0	Errata
1	No Fix	USB DbC Or Device Mode Port When Resuming From S3, S4, S5, or G3 State
2	No Fix	xHCI Power Management Link Timer
3	No Fix	xHCI USB 2.0 ISOCH Device Missed Service Interval
4	No Fix	SPI SFDP Program Suspend And Program Resume Instruction Fields Not Used
5	No Fix	Intel® Trace Hub Pipe Line Empty
6	No Fix	xHCI Short Packet Event Using Non-Event Data TRB
7	No Fix	eSPI SBLCL Register Bit Not Cleared By PLTRST#
8	No Fix	xHCI Protocol Speed ID Count Field
9	No Fix	S0ix Entry When Connecting a USB-C* Power Adapter
10	No Fix	Unexpected Shutdown with VCCIN_AUX Retention Mode Enabled
11	No Fix	Time-Sensitive Networking Incorrectly Advertised RX FIFO Size (for IoT Platforms only)
12	No Fix	xHCI Serial Bus Release Number Version
13	Fixed	PCH and Processor Sync Error During C8 Entry
14	No Fix	Integrated GbE Controller Reset on D3 Exit
15	No Fix	PCIe Clock and PCIe Reference Clock to Processor Maximum Rising/Falling Edge Rate and V_{CROSS}
16	No Fix	USB VTIO Device Capabilities Field Length
17	Fixed	FIVR Transitions During Deep Sx Entry with Integrated GbE Enabled
18	Fixed	Ring Oscillator Calibration

2.3 Specification Changes

No.	Specification Changes
	No specification changes for this revision of the specification update.

2.4 Specification Clarifications

No.	Specification Clarifications
1	SX_EXIT_HOLDOFF# Not Functional with eSPI Enabled
2	SATA Controller Support for Automatic Partial to Slumber Transition (APST) Feature
3	xHCI D3 Exit Timing

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3 Errata Details

1	**USB DbC Or Device Mode Port When Resuming From S3, S4, S5, or G3 State**
Problem	If a PCH USB 3.2 Type-C port is configured in Device Mode (or in DbC mode) and connected to an external USB 3.2 host controller, it may cause the USB port to go into a non-functional state in the following scenarios: 1. The PCH resumes from S3, S4, or S5 state, the port may remain in U2. 2. The port is connected to a USB 3.2 Gen 1x1 host controller when resuming from S3, S4, S5, or G3, the port may enter into Compliance Mode or an inactive state if Compliance mode is disabled. 3. The port is connected to a USB 3.2 Gen 2x1 host controller when resuming from S3, S4, S5, or G3, the port may enter an inactive state.
Implication	PCH USB Type-C port configured in Device Mode (or in DbC mode) may fail to enumerate or become unavailable.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

2	**xHCI Power Management Link Timer**
Problem	The xHCI implements the Power Management Link Timer (PM LC Timer) Timeout value as 10 us instead of 4 us as defined by the USB 3.2 specification.
Implication	USB-IF xHCI CV TD 7.21 may report a failure. Intel has obtained a waiver for TD 7.21. **Note:** No functional issues are expected.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

3	**xHCI USB 2.0 ISOCH Device Missed Service Interval**
Problem	When the xHCI controller is stressed with concurrent traffic across multiple USB ports, the xHCI controller may fail to service USB 2.0 Isochronous IN endpoints within the required service interval.
Implication	USB 2.0 isochronous devices connected to the xHCI controller may experience dropped packets. **Note**: This issue has only been observed in a synthetic environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

4	**SPI SFDP Program Suspend And Program Resume Instruction Fields Not Used**
Problem	For flash device suspend/resume opcodes, the SPI controller does not use JEDEC SFDPs 13th DWORD bits [15:0], Program Suspend Instruction and Program Resume Instruction fields. The controller only uses bits [31:16], Suspend Instruction and Resume Instruction fields, to obtain the suspend/resume opcodes.
Implication	If the SPI flash requires bits [15:0] to be different than bits [31:16], then the suspend/resume feature is not functional. In this case, system behavior varies depending on what the suspend/resume instruction is and when it is generated. **Note**: Major flash vendors have been using the same value for bits [31:16] and bits [15:0].
Workaround	None identified. If a device requires bits [15:0] to be different than bits [31:16], then disable the device suspend / resume via the SPI Suspend / Resume Enable soft strap.
Status	For the steppings affected, refer to the Summary Table of Changes.

5	**Intel® Trace Hub Pipe Line Empty**
Problem	The Intel® Trace Hub Pipe Line Empty bit (CSR_MTB_BAR, Offset D4h) for a given output port may be set while the Input Buffer Empty for the associated output port is not set. This will only happen when the captureDone signal is de-asserted by clearing the ForceCaptureDone bit (CSR_MTB_BAR, Offset D8h) is cleared or the StoreQual[0] signal is de-asserted by the Trigger Unit before the pipe line is empty, and the destination is either system memory or USB (DCI).
Implication	There may be valid trace data in the trace source input buffer which did not get sent to the destination (output port).
Workaround	None identified. CaptureDone should be cleared or de-asserted after the pipe line is empty.
Status	For the steppings affected, refer to the Summary Table of Changes.

6	**xHCI Short Packet Event Using Non-Event Data TRB**
Problem	The xHCI may generate an unexpected short packet event for the last transfer's Transfer Request Block (TRB) when using Non-Event Data TRB with multiples TRBs.
Implication	Transfer may fail due to the packet size error. **Note**: This issue has only been observed in a synthetic environment. No known implication has been identified with commercial software.
Workaround	None identified. Intel recommends software to use Data Event TRBs for short packet completion.
Status	For the steppings affected, refer to the Summary Table of Changes.

7	eSPI SBLCL Register Bit Not Cleared By PLTRST#
Problem	The IOSF-SB eSPI Link Configuration Lock (SBLCL) bit (offset 4000h, bit 27 in eSPI PCRspace) is reset by RSMRST# assertion instead of PLTRST# assertion.
Implication	If the SBLCL bit is set to 1, software will not be able to access the eSPI device Capabilities and Configuration register in the reserved address range (0h - 7FFh) until RSMRST# asserts.
Workaround	None identified. If software needs to access the eSPI device reserved range 0h - 7FFh while SBLCL bit is set to 1, a RSMRST# assertion should be performed.
Status	For the steppings affected, refer to the Summary Table of Changes.

8	xHCI Protocol Speed ID Count Field
Problem	The xHCI Host Controller reports an incorrect Protocol Speed ID Count value for the USB 3.2 Supported Protocol Capability register - xHCI MMIO offset 8028 bits [31:28].
Implication	USB-IF xHCI CV TD 1.9 may report a failure. **Note**: No functional impact is expected.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

9	S0ix Entry When Connecting a USB-C* Power Adapter
Problem	Connecting a USB-C* power adapter to a PCH USB port may cause a race condition that can prevent the system from entering S0ix. This issue only occurs on designs where the USB-C Power Delivery (PD) implements Out Of Band (OOB) messaging to communicate with the PCH for port mapping.
Implication	The system may fail to enter S0ix.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

10	Unexpected Shutdown with VCCIN_AUX Retention Mode Enabled
Problem	Due to a PMC logic bug, the FIVR may unexpectedly shutdown during C10 exit when retention mode is enabled for VCCIN_AUX.
Implication	The system may unexpectedly shut down and requires a global reset cycle to recover.
Workaround	None identified. Due to this erratum, VCCIN_AUX retention mode is not supported and should be disabled. BIOS Reference Code Revision 3357.02 or later disables VCCIN_AUX retention mode by default.
Status	For the steppings affected, refer to the Summary Table of Changes.

11	Time-Sensitive Networking Incorrectly Advertised RX FIFO Size (for IoT Platforms only)
Problem	The Time-Sensitive Networking (TSN) controller MTL Receive FIFO Size (RXFIFOSIZE) bits [4:0] in register MAC_HW_FEATURE1 (MMIO offset 120h) advertises 32 KB as the allowable RX FIFO size, while the implemented size is 24 KB.
Implication	The maximum aggregate size for MTL RX queues is 24 KB. If software allocation of RX queues exceeds this amount, then data attempted to be queued greater than 24 KB will be lost.
Workaround	None identified. Software should not allocate an aggregate size of more than 24 KB for MTL RX queues.
Status	For the steppings affected, refer to the Summary Table of Changes.

12	xHCI Serial Bus Release Number Version
Problem	The xHCI Host Controller reports the value of 31h for the Serial Bus Release Number (SBRN) register (offset 60h), which does not meet the xHCI specification revision 1.2.
Implication	USB-IF xHCI CV TD 1.1 may report a failure. Intel has obtained a waiver for TD 1.1. **Note**: There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

13	PCH and Processor Sync Error During C8 Entry
Problem	Due to an Internal PMC logic issue, the PCH and processor may become out of sync during C8 entry flow.
Implication	The system may hang.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

14	Integrated GbE Controller Reset on D3 Exit
Problem	Upon GbE controller D3 exit, the GbE host driver performs a controller reset. During this reset, software accesses to the GbE MMIO registers may not complete.
Implication	The system may hang. **Note**: This erratum has only been observed in a synthetic environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

15	PCIe Clock and PCIe Reference Clock to Processor Maximum Rising/Falling Edge Rate and V_{CROSS}
Problem	The PCIe Clock Output signals (CLKOUT_PCIE_P/N) and PCIe reference clock signals to processor (CLKOUT_CPUPCIBCLK_P/N) may not meet the maximum Rising/Falling Edge Rate and V_{CROSS} specifications as defined in the PCI Express Card Electromechanical Specification Revision 3.0, section 2.1.3, REFCLK AC Specifications.
Implication	There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

16	USB VTIO Device Capabilities Field Length
Problem	The xHCI spec version 1.2 defines the PCI Express Capability structure offset 04h Device Capabilities (DVSEC) field to be 8 bytes. The USB Virtualization Based Trusted IO (VTIO) Management controller implements the DVSEC field as 12 bytes.
Implication	A USB controller driver may not be able to enable the USB VTIO controller.
Workaround	None identified. To mitigate this erratum, an Independent Software Vendor could account for the field length in the USB controller driver.
Status	For the steppings affected, refer to the Summary Table of Changes.

17	FIVR Transitions During Deep Sx Entry with Integrated GbE Enabled
Problem	During Deep Sx entry, if ACPRESENT is asserted during the SUSWARN# / SUSACK# handshake, PMC FW may prematurely transition FIVR to a deeper power state before determining Integrated GbE presence. This issue occurs only on platforms with Integrated GbE.
Implication	The system may hang during Deep Sx entry.
Workaround	A BIOS code change has been identified and may be implemented as a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

18	Ring Oscillator Calibration
Problem	The PCH contains a ring oscillator calibration circuit to stabilize internal clocks across voltage and temperature changes. During operation, noise from the calibration circuit may cause the PCH internal clocks to deviate from expected frequency.
Implication	If the PCH internal clocks deviate from expected frequency, several unexpected behaviors may occur including system shutdown, system hang, or device detection issues.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

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4 Specification Changes

There are no specification changes in this revision of the Specification Update.

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5 Specification Clarification

1	**SX_EXIT_HOLDOFF# Not Functional with eSPI Enabled**
	Add the following note to the Intel® 500 Series Chipset Family On-Package Platform Controller Hub (PCH) Datasheet, Volume 1 of 2 (#631119) inthe SX_EXIT_HOLDOFF# Signal Description in the Power Management chapter Signal Description section: "When eSPI is enabled, SX_EXIT_HOLDOFF# functionality is not available, and assertion of the signal will not impact Sx exit flows."

2	**SATA Controller Support for Automatic Partial to Slumber Transition (APST) Feature**
	Add the following note to the Intel® 500 Series Chipset Family On-Package Platform Controller Hub Datasheet, Volume 2 of 2 (#631120) in the HBA Capabilities Extended (GHC_CAP2) register summary, bit 2, 'Automatic Partial to Slumber Transitions (APST)' field description section: "BIOS should set this bit to 0 as APST is not supported."

3	**xHCI D3 Exit Timing**
	Add the following text to the Intel® 500 Series Chipset Family On-Package Platform Controller Hub (PCH) Datasheet Volume 2 of 2 (#631120) in the Power Management Control/Status (PM_CS) register summary, bits 1:0, 'PowerState (POWERSTATE)' field description section: "Software should wait for 100 ms before requesting the xHCI controller to re-enter D3 after a D3 exit."

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