Intel® 500 Series Chipset Family On-Package Platform Controller Hub

Datasheet, Volume 2 of 2

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Revision 002

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Contents

Tables

Revision History

Revision Number	Description	Date
002	• Added Bit 6 in Section 4.3.73, "Global Reset Causes (GBLRST_CAUSE0)—Offset 1924h"	February 2023
001	• Initial Release	September 2020

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1 Introduction

This document (Volume 2) describes the PCH's registers that are located in the PCI configuration space, memory space, or IO space. The following notations and definitions are used in the register description.

Table 1-1. Register Attributes and Terminology

Item	Description
RO	**Read Only:** Writes to this register bit have no effect. When writing to RO bits, software must preserve the value. When software updates a register that has RO fields, it must read the register value first so that the appropriate merge between the reserved and updated fields will occur.
RW	**Read / Write:** These bits can be read and written by software.
RW1C	**Read / Write 1 to Clear:** These bits can be read and cleared by software. Writing a '1' to a bit will clear it, while writing a '0' to a bit has no effect. Hardware sets these bits.
RW0C	**Read / Write 0 to Clear:** These bits can be read and cleared by software. Writing a '0' to a bit will clear it, while writing a '1' to a bit has no effect. Hardware sets these bits.
RW1S	**Read / Write 1 to Set:** These bits can be read and set by software. Writing a '1' to a bit will set it, while writing a '0' to a bit has no effect. Hardware clears these bits.
RW/O	**Read / Write Once**: A register bit with this attribute can be written only once after power up. After the first write, the bit becomes read only.
WO	**Write Only:** These bits can only be written by software, reads return zero.
RC	**Read Clear:** These bits can only be read by software, but a read causes the bits to be cleared. Hardware sets these bits.
RW/1C	**Read/Write Clear.** The register bit is set to 1 by hardware and cleared by software writing a 1 to it.
RW/1S	**Read/Write Set**. The register bit is set to 1 by software and cleared by hardware.
RW/L	**Read/Write Locked**. A register bit with this attribute can be read and write, but cannot be written after the lock bit is set.
/V	**Volatile or variable.** This attribute indicates that the register bit can be updated by hardware (aside from resetting it). For example, RO/V means hardware controls the value; RW/V means that generally the bit is written by SW/FW but can be also updated by hardware.
/P	This attribute indicates that the register is reset only on loss of power.
/S	This attribute indicates that the initial value of the register bit is taken from software.

The PCH contains registers and bits that are reserved. These are designated by being defined as Reserved or RSVD. In addition, registers or register bits not defined in this document are also reserved. Software must not attempt to access a reserved register, use the value read from a reserved register or bit, or modify the value in a reserved register or bit. Doing so is unsupported and may cause unexpected behavior on the platform. When writing to reserved bits, software must preserve the value. When software updates a register that has reserved fields, it must read the register value first so that the appropriate merge between the reserved and updated fields will occur.

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2 Enhanced SPI Interface (D31:F0)

2.1 eSPI PCI Configuration Registers Summary

Table 1. Summary of eSPI PCI Configuration Registers

Table 2.

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device and Vendor Identifiers (ESPI_DID_VID)—Offset 0h	XXXX8086h
4h	7h	Device Status and Command (ESPI_STS_CMD)—Offset 4h	3h
8h	Bh	Class Code and Revision ID (ESPI_CC_RID)—Offset 8h	60100XXh
2Ch	2Fh	Sub System Identifiers (ESPI_SS)—Offset 2Ch	0h
34h	37h	Capability List Pointer (ESPI_CAPP)—Offset 34h	0h
80h	83h	I/O Decode Ranges and I/O Enables (ESPI_IOD_IOE)—Offset 80h	0h
84h	87h	eSPI Generic IO Range 1 (ESPI_LGIR1)—Offset 84h	0h
88h	8Bh	eSPI Generic IO Range 2 (ESPI_LGIR2)—Offset 88h	0h
8Ch	8Fh	eSPI Generic IO Range 3 (ESPI_LGIR3)—Offset 8Ch	0h
90h	93h	eSPI Generic IO Range 4 (ESPI_LGIR4)—Offset 90h	0h
94h	97h	USB Legacy Keyboard/Mouse Control (ESPI_ULKMC)—Offset 94h	0h
98h	9Bh	eSPI Generic Memory Range (ESPI_LGMR)—Offset 98h	0h
D8h	DBh	BIOS Decode Enable (ESPI_BDE)—Offset D8h	FFCFh
DCh	DFh	BIOS Control (ESPI_BC)—Offset DCh	20h

2.1.1 Device and Vendor Identifiers (ESPI_DID_VID)—Offset 0h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 31
Function: 0

Default: XXXX8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO/V	**Device Identification (DID):** Indicates the Device ID of thecontroller. Refer to the Device and Revision ID Table in Volume 1for the default value.
15:0	8086h RO	**Vendor Identification (VID):** Indicates Intel

2.1.2 Device Status and Command (ESPI_STS_CMD)—Offset 4h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 31
Function: 0

Default: 3h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the bridge detects a parity error. This bit gets set even if CMD.PERE is not set.
30	0h RW/1C/V	**Signaled System Error (SSE):** Set when the bridge signals a system error to the internal SERR# logic.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the bridge receives a completion with unsupported request.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the bridge receives a completion with completer abort status.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the bridge generates a completion packet with target abort status.
26:25	0h RO	**DEVSEL# Timing Status (DTS):** Indicates medium timing, although this has no meaning on the HW.
24	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the bridge receives a completion packet from a previous request, and detects a parity error, and CMD.PERE is set.
23:21	0h RO	Reserved.
20	0h RO	**Capabilities List (CLIST):** There is a capabilities list in the eSPI bridge.
19:9	0h RO	Reserved.
8	0h RW	**SERR# Enable (SEE):** Enable SERR# to be generated if this bit is set.
7	0h RO	Reserved.
6	0h RW	**Parity Error Response Enable (PERE):** When this bit is set to 1, it enables the HW to response to parity errors detected on the interface.
5:3	0h RO	Reserved.
2	0h RW	**Bus Master Enable (BME):** Controls a device's ability to act as a master on the bus. A value of 0 disables the device from generating traffic. A value of 1 allows the device to behave as a bus master. State after RST# is 0.
1	1h RO	**Memory Space Enable (MSE):** Memory space cannot be disabled.
0	1h RO	**I/O Space Enable (IOSE):** I/O space cannot be disabled.

2.1.3 Class Code and Revision ID (ESPI_CC_RID)—Offset 8h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 31
Function: 0

Default: 60100XXh

Bit Range	Default & Access	Field Name (ID): Description
31:24	6h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	1h RO	**Sub-Class Code (SCC):** Indicates the device a PCI to ISA bridge.
15:8	0h RO	**Programming Interface (PI):** Hardwired to 0. The bridge has no programming interface.
7:0	-- RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

2.1.4 Sub System Identifiers (ESPI_SS)—Offset 2Ch

This register is initialized to logic 0 by the assertion of PLTRST#. This register can be written only once after PLTRST# de-assertion.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value.

2.1.5 Capability List Pointer (ESPI_CAPP)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RO	**Capability Pointer (CP):** Indicates the offset of the first Capability Item.

2.1.6 I/O Decode Ranges and I/O Enables (ESPI_IOD_IOE)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW	**Microcontroller Enable #2 (ME2):** Enables decoding of I/O locations 4Eh and 4Fh.
28	0h RW	**SuperI/O Enable (SE):** Enables decoding of I/O locations 2Eh and 2Fh.
27	0h RW	**Microcontroller Enable #1 (ME1):** Enables decoding of I/O locations 62h and 66h.
26	0h RW	**Keyboard Enable (KE):** Enables decoding of the keyboard I/O locations 60h and 64h.
25	0h RW	**High Gameport Enable (HGE):** Enables decoding of the I/O locations 208h to 20Fh.
24	0h RW	**Low Gameport Enable (LGE):** Enables decoding of the I/O locations 200h to 207h.
23:20	0h RO	Reserved.
19	0h RW	**Floppy Drive Enable (FDE):** Enables decoding of the FDD range. Range is selected by LIOD.FDE
18	0h RW	**Parallel Port Enable (PPE):** Enables decoding of the LPT range. Range is selected by LIOD.LPT.
17	0h RW	**Com Port B Enable (CBE):** Enables decoding of the COMB range. Range is selected LIOD.CB.
16	0h RW	**Com Port A Enable (CAE):** Enables decoding of the COMA range. Range is selected LIOD.CA.
15:13	0h RO	Reserved.
12	0h RW	**FDD Range (FDD):** The following table describes which range to decode for the FDD Port Bits Decode Range 0 3F0h - 3F5h, 3F7h (Primary) 1 370h - 375h, 377h (Secondary)
11:10	0h RO	Reserved.
9:8	0h RW	**LPT Range (LPT):** The following table describes which range to decode for the LPT Port: Bits Decode Range 00 378h - 37Fh and 778h - 77Fh 01 278h - 27Fh (port 279h is read only) and 678h - 67Fh 10 3BCh - 3BEh and 7BCh - 7BEh 11 Reserved

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6:4	0h RW	**ComB Range (CB):** The following table describes which range to decode for the COMB Port Bits Decode Range 000 3F8h - 3FFh (COM 1) 001 2F8h - 2FFh (COM 2) 010 220h - 227h 011 228h - 22Fh 100 238h - 23Fh 101 2E8h - 2EFh (COM 4) 110 338h - 33Fh 111 3E8h - 3EFh (COM 3)
3	0h RO	Reserved.
2:0	0h RW	**ComA Range (CA):** The following table describes which range to decode for the COMA Port Bits Decode Range 000 3F8h - 3FFh (COM 1) 001 2F8h - 2FFh (COM 2) 010 220h - 227h 011 228h - 22Fh 100 238h - 23Fh 101 2E8h - 2EFh (COM 4) 110 338h - 33Fh 111 3E8h - 3EFh (COM 3)

2.1.7 eSPI Generic IO Range 1 (ESPI_LGIR1)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address[15:2] (ADDR):** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	Reserved.
0	0h RW	**eSPI Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

2.1.8 eSPI Generic IO Range 2 (ESPI_LGIR2)—Offset 88h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address[15:2] (ADDR):** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	Reserved.
0	0h RW	**eSPI Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

2.1.9 eSPI Generic IO Range 3 (ESPI_LGIR3)—Offset 8Ch

Access Method

Type: CFG Register (Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address[15:2] (ADDR):** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	Reserved.
0	0h RW	**eSPI Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

2.1.10 eSPI Generic IO Range 4 (ESPI_LGIR4)—Offset 90h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address[7:2] Mask (ADDR_MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address[15:2] (ADDR):** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
1	0h RO	Reserved.
0	0h RW	**eSPI Decode Enable (LDE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

2.1.11 USB Legacy Keyboard/Mouse Control (ESPI_ULKMC)—Offset 94h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C/V	**SMI Caused by End of Pass-through (SMIBYENDPS):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 7, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
14:12	0h RO	Reserved.
11	0h RW/1C/V	**SMI Caused by Port 64 Write (TRAPBY64W):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 3, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch. Note that the A20Gate Pass-Through Logic allows specific port 64h Writes to complete without setting this bit.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/1C/V	**SMI Caused by Port 64 Read (TRAPBY64R):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 2, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
9	0h RW/1C/V	**SMI Caused by Port 60 Write (TRAPBY60W):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 1, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch. Note that the A20Gate Pass-Through Logic allows specific port 60h Writes to complete without setting this bit.
8	0h RW/1C/V	**SMI Caused by Port 60 Read (TRAPBY60R):** Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 0, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
7	0h RW	**SMI at End of Pass-through Enable (SMIATENDPS):** May need to cause SMI at the end of a pass-through. Can occur if an SMI is generated in the middle of a pass through, and needs to be serviced later.
6	0h RO/V	**Pass Through State (PSTATE):** This read-only bit indicates that the state machine is in the middle of an A20GATE pass-through sequence. If software needs to reset this bit, it should set Bit 5 0.
5	0h RW	**A20Gate Pass-Through Enable (A20PASSEN):** When enabled, allows A20GATE sequence Pass-Through function. When enabled, a specific cycle sequence involving writes to port 60h and port 64h does not result in the setting of the SMI status bits. SMI# will not be generated, even if the various enable bits are set.
4	0h RO	Reserved.
3	0h RW	**SMI on Port 64 Writes Enable (S64WEN):** When set, a 1 in bit 11 will cause an SMI event.
2	0h RW	**SMI on Port 64 Reads Enable (S64REN):** When set, a 1 in bit 10 will cause an SMI event.
1	0h RW	**SMI on Port 60 Writes Enable (S60WEN):** When set, a 1 in bit 9 will cause an SMI event.
0	0h RW	**SMI on Port 60 Reads Enable (S60REN):** When set, a 1 in bit 8 will cause an SMI event.

2.1.12 eSPI Generic Memory Range (ESPI_LGMR)—Offset 98h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Memory Address[31:16] (MADDR):** This field specifies a 64KB memory block anywhere in the 4GB memory space that will be decoded to eSPI if enabled.
15:1	0h RO	Reserved.
0	0h RW	**eSPI Memory Range Decode Enable (LGMRD_EN):** When this bit is set to 1, then the range specified in this register is enabled for decoding to eSPI.

2.1.13 BIOS Decode Enable (ESPI_BDE)—Offset D8h

The concept of Feature Space does not apply to SPI-based flash. PCH simply decodes these ranges as memory accesses when enabled for the SPI flash interface.

Access Method

Type: CFG Register (Size: 32 bits)

Device: 31
Function: 0

Default: FFCFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**BDE Lock Enable (BLE):** When this bit is set, the RW bits of this BDE register are locked down. Once set, this bit can only be cleared by PLTRST#.
30:16	0h RO	Reserved.
15	1h RO	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS range: Data space: FFF80000h - FFFFFFFFh Feature space: FFB80000h - FFBFFFFFh
14	1h RW/L	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS range: Data space: FFF00000h - FFF7FFFFh{br]Feature space: FFB00000h - FFB7FFFFh
13	1h RW/L	**E8-EF Enable (EE8):** Enables decoding of 512K of the followingBIOS range: Data space: FFE80000h - FFEFFFFFh Feature space: FFA80000h - FFAFFFFFh
12	1h RW/L	**E0-E8 Enable (EE0):** Enables decoding of 512K of the followingBIOS range: Data space: FFE00000h - FFE7FFFFh Feature Space: FFA00000h - FFA7FFFFh
11	1h RW/L	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS range: Data space: FFD80000h - FFDFFFFFh Feature space: FF980000h - FF9FFFFFh
10	1h RW/L	**D0-D7 Enable (ED0):** Enables decoding of 512K of the followingBIOS range: Data space: FFD00000h - FFD7FFFFh Feature space: FF900000h - FF97FFFFh
9	1h RW/L	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS range: Data space: FFC80000h - FFCFFFFFh Feature space: FF880000h - FF8FFFFFh
8	1h RW/L	**C0-C7 Enable (EC0):** Enables decoding of 512K of the following BIOS range: Data space: FFC00000h - FFC7FFFFh Feature space: FF800000h - FF87FFFFh
7	1h RW/L	**Legacy F Segment Enable (LFE):** This enables the decoding of thelegacy 64KB range at F0000h - FFFFFh Note that decode for the BIOS legacy F segment is enabled by theLFE bit only, it is not affected by the GEN_PMCON_1.iA64_EN bit.
6	1h RW/L	**Legacy E Segment Enable (LEE):** This enables the decoding of thelegacy 64KB range at E0000h - EFFFFh Note that decode for the BIOS legacy E segment is enabled by the LEE bit only, it is not affected by the GEN_PMCON_1.iA64_EN bit.
5:4	0h RO	Reserved.
3	1h RW/L	**70-7F Enable (E70):** Enables decoding of 1MB of the followingBIOS range: Data space: FF700000h - FF7FFFFFh Feature space: FF300000h - FF3FFFFFh

Bit Range	Default & Access	Field Name (ID): Description
2	1h RW/L	**60-6F Enable (E60):** Enables decoding of 1MB of the followingBIOS range: Data space: FF600000h - FF6FFFFFh Feature Space: FF200000h - FF2FFFFFh
1	1h RW/L	**50-5F Enable (E50):** Enables decoding of 1MB of the followingBIOS range: Data space: FF500000h - FF5FFFFFh Feature space: FF100000h - FF1FFFFFh
0	1h RW/L	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS range: Data space: FF400000h - FF4FFFFFh Feature space: FF000000h - FF0FFFFFh

2.1.14 BIOS Control (ESPI_BC)—Offset DCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 0

Default: 20h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW/L	**BIOS Write Reporting (Async-SMI) Enable (BWRE):** 1'b0: Disable reporting of BIOS Write event. 1'b1: Enable reporting of BIOS Write event (BWRS bit = 1) using Async-SMI.
10	0h RW/1C/V	**BIOS Write Status (BWRS):** HW sets this bit if a memory write access is detected to a protected BIOS range. 1'b0: Memory write to BIOS region not attempted or attempted with WPD bit = 1. 1'b1: A memory write transaction to BIOS region has been received with WPD bit = 0. Note: An Async-SMI message is generated to report this event if BWRE bit is set. Note: SW must write a 1 to this bit to clear it, which will also deassert the Async-SMI, if BWRE is set.
9	0h RO	Reserved.
8	0h RW/1C/V	**BIOS Write Protect Disable Status (BWPDS):** HW sets this bit if configuration write access is detected to protected WPD bit. 1'b0: No attempt has been made to set WPD bit with LE bit = 1. 1'b1: A configuration write request has been received to set WPD bit (0 or 1) with LE bit = 1. Note: An SB Sync-SMI (Assert_SSMI) message is generated to report this event if HW sets this bit. The unsuccessful completion for the configuration write is returned upon receiving the SMI_Ack message response. Note: SW must write a 1 to this bit to clear it, which will also deassert the Sync-SMI Note: The Sync-SMI sets the PMC SMI_STS.TCO_STS register.
7	0h RW/L	**BIOS Interface Lock-Down (BILD):** When set, prevents TS and BBS bits from being changed. This bit can only be written from 0 to 1 once. BIOS Note: This bit is not backed up in the RTC well. This bit should also be set in the BUC register in the RTC device to record the last state of this value following a cold reset.
6	0h RW/V/L	**Boot BIOS Strap (BBS):** This field determines the destination of accesses to the BIOS memory range. For the default see the strap section in Vol1 for details. 0: SPI 1: eSPI When SPI or eSPI is selected, the range that is decoded is further qualified by other configuration bits described in the respective sections. The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down is not set.

Bit Range	Default & Access	Field Name (ID): Description
5	1h RW/L	**Enable InSMM.STS (EISS):** When this bit is set, the BIOS region is not writable until SMM sets the InSMM.STS bit. Today BIOS Flash is writable if WPD is a 1. If this bit is set, then WPD must be a 1 and InSMM.STS (0xFED3_0880(0)) must be 1 also. If this bit is clear, then BIOS is writable based only on WPD = 1 and the InSMM.STS is a dont care.
4	0h RO/V	**Top Swap (TS):** When set, PCH will invert either A16, A17, or A18 for cycles going to the BIOS space (but not the Feature space). When cleared, PCH will not invert A16. If booting from eSPI, then the Boot Block Size is fixed at 64KB and A16 is inverted if Top Swap is enabled. If booting from SPI, then the BOOT_BLOCK_SIZE soft strap determines if A16, A17, orA18 should be inverted if Top Swap is enabled. Note: If the Top-Swap strap is asserted, then this bit cannot be cleared by software. The strap jumper should be removed and the system rebooted. BIOS Note: This bit provides a read-only path to view the state of the Top Swap strap. It is backed up and driven from the RTC well. BIOS will need to program the corresponding register in the RTC well, which will be reflected in this register.
3	0h RO	Reserved.
2	0h RO/V	**eSPI Enable Pin Strap (ESPI):** This field determines the destination of accesses to the D31:F0 and related Fixed and Variable IO and Memory decode ranges, including BIOS memory range. 1'b0: Reserved 1'b1: eSPI is the D31:F0 target. Notes: 1. This field, along with the BBS field setting, determines PCH configuration. 2. This field cannot be overwritten by software (unlike the BBS field). 3. This bit is also reflected in the SPI Flash PCI Configuration register Offset DCh.
1	0h RW/L	**Lock Enable (LE):** When set, setting the WP bit will cause SMI. When cleared, setting the WP bit will not cause SMI. Once set, this bit can only be cleared by a PLTRST#. When this bit is set, EISS - bit (5) of this register is locked down.
0	0h RW	**Write Protect Disable (WPD):** When set, access to the BIOS space is enabled for both read and write cycles to BIOS. When cleared, only read cycles are permitted to the FWH or SPI flash. When this bit is written from a 0 to a 1 and the LE bit is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

2.2 eSPI PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 3. Summary of eSPI PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4000h	4003h	eSPI Slave Configuration And Link Control (SLV_CFG_REG_CTL)—Offset 4000h	0h
4004h	4007h	eSPI Slave Configuration Register Data (SLV_CFG_REG_DATA)—Offset 4004h	0h
4020h	4023h	Peripheral Channel Error for Slave 0 (PCERR_SLV0)—Offset 4020h	80h
4030h	4033h	Virtual Wire Channel Error for Slave 0 (VWERR_SLV0)—Offset 4030h	0h
4040h	4043h	Flash Access Channel Error for Slave 0 (FCERR_SLV0)—Offset 4040h	40080h
4050h	4053h	Link Error for Slave 0 (LNKERR_SLV0)—Offset 4050h	FF00h

2.2.1 eSPI Slave Configuration And Link Control (SLV_CFG_REG_CTL)—Offset 4000h

Along with SLV_CFG_REG_DATA, this register controls Rd/Wr access to Slave Configuration registers using eSPI Get/Set_Configuration, Get_Status and In-Band Reset cycles. It allows Tunneled Access to Slave Configuration (TASC) registers from Host SW /CSME firmware.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Slave Configuration Register Access Enable (SCRE):** Writing a 1 to this field triggers an access (SCRT) to a Slave Config Register ('Go'). Note: Hardware clears this bit to 0 (& sets the SCRS field) when the transaction has completed on the eSPI bus. In the case of a configuration/status register read, the data is valid only after this bit has been cleared by HW. Note: The SCRE is effective only if SCRS is clear.
30:28	0h RW/1C/V	**Slave Configuration Register Access Status (SCRS):** This field is set by upon the completion of a configuration register access (SCRE). Software must clear this field by writing all 1s before initiating another Slave configuration register access (SCRE). 0h: Status not valid 1h: Slave No_Response 2h: Slave Response CRC Error 3h: Slave Response Fatal Error 4h: Slave Response Non-Fatal Error 5h – 6h: Reserved 7h: No errors (transaction completed successfully)
27	0h RW/1S	**SB eSPI Link Configuration Lock (SBLCL):** When set, eSPI controller prevents writes (i.e.,SET_CONFIGURATION) to any eSPI Specification defined Slave Capabilities and Configuration registers in the reserved register address range (0h – 7FFh). Access to Slave implementation specific configuration registers outside this range are not impacted by this lock bit and are always available – access protections to such registers are Slave implementation dependent. Notes: 1. This bit cannot be written to 0 once it has been set to 1. It can only be cleared by PLTRST# assertion. The lock is automatically disabled if and while the LNKERR_SLV0.SLCRR register bit is asserted (upon an eSPI link Fatal Error condition) to allow BIOS (or another SW agent) to attempt to recover the link. 2. This bit has no effect when PLTRST# is asserted. BIOS Note: BIOS must ensure that this bit is set to 1 after initial eSPI link configuration is over to prevent any further (unintentional or malicious) changes to the eSPI link configuration.
26:21	0h RO	Reserved.
20:19	0h RW	**Slave ID (SID):** eSPI Slave ID (CS#) to which the Slave Configuration Register Access (SCRT) is directed. 00: eSPI Slave 0 (EC/BMC) 01: eSPI Slave 1 (only support when a second eSPI Slave device is present) 10 – 2'b11: Reserved
18	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
17:16	0h RW	**Slave Configuration Register Access Type (SCRT):** 00: Slave Configuration register read from address SCRA[11:0] (GET_CONFIG) 01: Slave Configuration register write to address SCRA[11:0] (SET_CONFIG) 10: Slave Status register read (GET_STATUS) 11: In-Band Reset Notes: 1. Writes to Slave Configuration registers in the reserved address range (0h – 7FFh) are gated by the SBLCL bit. 2. Setting this field to 10 triggers a Get_Status command to the Slave. In this case, the SCRA field is ignored and only the lower 16-bits of the returned data(SLV_CFG_REG_DATA[15:0]) are valid. 3. Setting this field to 11 triggers an In-Band Reset command to the Slave. In this case, the SCRA field is ignored and no data is returned. This command resets the link for the targeted Slave to a default configuration. Software is responsible for reinitializing the link to optimized (higher performance) settings using these registers.
15:12	0h RO	Reserved.
11:0	0h RW	**Slave Configuration Register Address (SCRA):** Per eSPI Spec / eSPI Compatibility Spec.

2.2.2 eSPI Slave Configuration Register Data (SLV_CFG_REG_DATA)—Offset 4004h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Slave Configuration Register for Read and Write data (SCRD):** Configuration register Write data from software or read data from the Slave. For writes, this register must be programmed before the CTL register. For reads, data in this register is valid after the CTL.SCRE bit has been cleared by HW and the CTL.SCRS field indicates a successful transaction.

2.2.3 Peripheral Channel Error for Slave 0 (PCERR_SLV0)—Offset 4020h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RW	**Slave Host Reset Ack Override (SLV_HOST_RST_ACK_OVRD):** A 1 in this bit will cause the eSPI-MC to not wait for theSlave HOST_RESET_ACK Virtual Wire before (immediately) asserting the ResetPrepAck(Host space, GenPrep). The Host_Reset_Warn VW will be transmitted to the Slaveindependent of the setting for this bit.
27:26	0h RW	**Peripheral Channel Received Master or Target Abort Reporting Enable (PCRMTARE):** 00: Disable RMA or RTA Reporting 01: Reserved 10: Enable RMA or RTA Reporting as SERR 11: Enable RMA or RTA Reporting as SMI Notes: 1. SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# isdeasserted. 2. SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted.
25	0h RW	**Peripheral Channel Unsupported Request Reporting Enable (PCURRE):** If set to 1 by software, it allows reporting of an Unsupported Request (UR) as a System Error (SERR). If eSPI controller decodes a Posted transaction that is not supported, it sets the PCURD bit. If PCCMD.SEE (SERR enable) is also set to 1, then eSPIMCsets the PCSTS.SSE (Signaled System Error) bit and sends a Do_SErr message. Note: If the transaction was a Non-Posted request, then the agent handles thetransaction as an Advisory Non-Fatal error, and no error logging or signaling is done. The Completion with UR Completion Status serves the purpose of error reporting.
24	0h RW/1C/V	**Peripheral Channel Unsupported Request Detected (PCURD):** Set to 1 by hardwareupon detecting an Unspported Request (UR) that is not considered an Advisory Non-Fatal error and PCERR.PCURRE is set. Cleared to 0 when software writes a 1 to thisregister.
23:15	0h RO	Reserved.
14:13	0h RW	**Peripheral Channel Non-Fatal Error Reporting Enable (PCNFEE):** 00: Disable Non-Fatal Error Reporting 01: Reserved 10: Enable Non-Fatal Error Reporting as SERR 11: Enable Non-Fatal Error Reporting as SMI Note: SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# isdeasserted. Notes: 1. SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. 2. SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
12	0h RW/1C/V	**Peripheral Channel Non-Fatal Status (PCNFES):** This field is set by hardware if a Non-Fatal Error condition is detected on the Peripheral Channel. Software must clearthis bit. 0: No Non-Fatal Error detected 1: Non-Fatal Error detected (PCNFEC has a non-zero value) Notes: 1. Clearing this unlocks the PCNFEC field and triggers a SB Deassert_SMImessage if PCNFEE is set to SMI. 2. Setting of this bit is independent of the enable to generate a SMI/SERR (PCNFEE)
11:8	0h RO/V	**Peripheral Channel Non-Fatal Cause (PCNFEC):** 0h: No error 1h: Slave Response Code: NONFATAL_ERROR 2h: Slave Response Code: Unsuccessful Completion 3h: Unexpected completion received from Slave (i.e. completion without non-postedrequest or completion with invalid tag or completion with invalid length) 4h: Unsupported Cycle Type (w.r.t. Command) 5h: Unsupported Message Code 6h: Unsupported Address/Length alignment (upstream only): Memory: Address +Length > 64 B (aligned) [for both Posted and Non-Posted transactions] 7h: Unsupported Address/Length alignment (upstream only): Memory: 64-bit Addresswith Addr[63:32] = 0h [for both Posted and Non-Posted transactions] 8h – Fh: Reserved Note: This field is updated after a Peripheral channel transaction is completed if the PCNFES bit is not set.

Bit Range	Default & Access	Field Name (ID): Description
7	1h RW	**PLCC Misaligned Memory Access (PMMA):** Applies to only posted and non-posted memory transactions directed towards D31:f0 to be sent over the eSPI Peripheral Channel to an eSPI Slave. 1'b0: Requests with a length of 3 bytes or requests with a length of 1/2/4 bytes whose Address+Length is not DWord aligned will be rejected. 1'b1: Requests with a length of 3 bytes or requests with a length of 1/2/4 bytes whose Address+Length is not DWord aligned will be sent to the slave using the memory write/read format.
6:5	0h RW	**Peripheral Channel Fatal Error Reporting (PCFEE):** 00: Disable Fatal Error Reporting 01: Reserved 10: Enable Fatal Error Reporting as SERR (IOSF-SB Do_SErr message) 11: Enable Fatal Error Reporting as SMI (IOSF-SB Assert_SMI message) Notes: 1. SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# isdeasserted. 2. SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. 3. SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
4	0h RW/1C/V	**Peripheral Channel Fatal Error Reporting (PCFES):** This field is set by hardware if a FatalError condition is detected on the Peripheral Channel. Software must clear this bit by writing a 1 to it. 0: No Fatal Error detected 1: Fatal Error Type 2 detected (PCFEC has a non-zero value) Notes: 1. Clearing this unlocks the PCFEC field and triggers an SB Deassert_SMI message if PCFEE is set to SMI. 2. Setting of this bit is independent of the enable to generate a SMI/SERR (PCFEE).
3:0	0h RO/V	**Peripheral Channel Fatal Error Cause (PCFEC):** 0h: No error 1h – 7h: Reserved 8h: Malformed Slave Response Payload: Payload length > Max Payload Size (aligned) [Type 2] 9h: Malformed Slave Response Payload: Read request size > Max Read Request Size(aligned) [Type 2] Ah: Malformed Slave Response Payload: Address + Length > 4KB (aligned) [Type 2] Bh – Fh: Reserved Note: This field is updated after a Peripheral channel transaction is completed if the PCFES bit is not set.

2.2.4 Virtual Wire Channel Error for Slave 0 (VWERR_SLV0)—Offset 4030h

This register is used to control error reporting for the eSPI Virtual Wire Channel

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:13	0h RW	**Virtual Wire Channel Non-Fatal Error Reporting Enable (VWNFEE):** 00: Disable Non-Fatal Error Reporting 01: Reserved 10: Enable Non-Fatal Error Reporting as SERR (SB Do_SErr message) 11: Enable Non-Fatal Error Reporting as SMI (SB Assert_SMI message) Notes: 1. SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. 2. SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. 3. SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
12	0h RW/1C/V	**Virtual Wire Channel Non-Fatal Error Status (VWNFES):** This field is set by hardware if a Non-Fatal Error condition is detected on the Virtual Wire Channel. Software must clear this bit. 0: No Non-Fatal Error detected 1: Non-Fatal Error detected (VWNFEC has a non-zero value) Notes: 1. Clearing this unlocks the VWNFEC field and triggers an SB Deassert_SMImessage if VWNFEE is set to SMI. 2. Setting of this bit is independent of the enable to generate a SMI/SERR(VWNFEE).
11:8	0h RO/V	**Virtual Wire Channel Non-Fatal Error Cause (VWNFEC):** 0h: No error 1h: Slave Response Code: NONFATAL_ERROR 2h – Dh: Reserved Eh: Slave Virtual Wire: NON_FATAL_ERROR: 0 to 1 transition (1 to 0 transition on this VW is ignored) Fh: Reserved Note: This field is updated after a Virtual Wire Channel transaction is completed if the VWNFES bit is not set.
7	0h RO	Reserved.
6:5	0h RW	**Virtual Wire Channel Fatal Error Reporting Enable (VWFEE):** 00: Disable Fatal Error Reporting 01: Reserved 10: Enable Fatal Error Reporting as SERR (IOSF-SB Do_SErr message) 11: Enable Fatal Error Reporting as SMI (SB Assert_SMI message) Notes: 1. SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. 2. SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted.3. SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
4	0h RW/1C/V	**Virtual Wire Channel Fatal Error Status (VWFES):** This field is set by hardware if a Fatal Error condition is detected on the Virtual Wire Channel. Software must clear this bit by writing all 1s to it. 0: No Fatal Error detected 1: Fatal Error Type 2 detected (VWFEC has a non-zero value) Notes: 1. Clearing this unlocks the VWFEC field and triggers an SB Deassert_SMImessage if VWFEE is set to SMI. 2. Setting of this bit is independent of the enable to generate a SMI/SERR (VWFEE).
3:0	0h RO/V	**Virtual Wire Channel Fatal Error Cause (VWFEC):** 0h: No error 1h – 7h: Reserved 8h: Malformed Slave Response Payload: VW Count > Max. VW Count [Type 2] 9h – 4'hD: Reserved Eh: Slave Virtual Wire: FATAL_ERROR 0 to 1 transition (1 to 0 transition on this VW is ignored) [Type 2] Fh: Reserved Note: This field is updated after a Virtual Wire Channel transaction is completed if the VWFES bit is not set.

2.2.5 Flash Access Channel Error for Slave 0 (FCERR_SLV0)—Offset 4040h

This register is used to determine how to log and report errors on the Flash Access channel, for both Master and Slave Attached Flash configurations.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 40080h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	1h RO/V	**SAF CAM Empty (SAFCAMEMPTY):** Only valid in slave-attached flash mode. Will always read 1 otherwise. 0: SAF CAM is not empty - there are outstanding NP flash transactions to the eSPI slave. 1: SAF CAM is empty - there are no outstanding NP flash transactions to the eSPI slave.
17	0h RO	Reserved.
16	0h RW	**SAF NF Error Blocking Enable (SAFNFEBLKEN):** Only valid in slave-attached flash mode. Has no impact otherwise. 1: the flash channel will be blocked when a NON_FATAL_ERROR response is received in response to a GET_FLASH_C. 0: the flash channel will NOT be blocked when a NON_FATAL_ERROR response is received in response to a GET_FLASH_C.
15	0h RO	Reserved.
14:13	0h RW	**Flash Access Channel Non-Fatal Error Reporting Enable (FCNFEE):** 00: Disable Non-Fatal Error Reporting 01: Reserved 10: Enable Non-Fatal Error Reporting as SERR (SB Do_SErr message) 11: Enable Non-Fatal Error Reporting as SMI (SB Assert_SMI message) Notes: 1. SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. 2. SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. 3. SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
12	0h RW/1C/V	**Flash Access Channel Non-Fatal Error Status (FCNFES):** This field is set by hardware if aNon-Fatal Error condition is detected on the Flash Access Channel. Software must clearthis bit. 0: No Non-Fatal Error detected 1: Non-Fatal Error detected (FCNFEC has a non-zero value) Notes: 1. Clearing this unlocks the FCNFEC field and triggers an SB Deassert_SMI message if FCNFEE is set to SMI. 2. Setting of this bit is independent of the enable to generate a SMI/SERR (FCNFEE).
11:8	0h RO/V	**Flash Access Channel Non-Fatal Error Cause (FCNFEC):** 0h: No error 1h: Slave Response Code: NONFATAL_ERROR received in response to GET_FLASH_NP, PUT_FLASH_C [for Master-Attached Flash accesses only] or GET_FLASH_C [for Slave-Attached Flash accesses only]. 2h: Slave Response Code: Unsuccessful Completion [for Slave-Attached Flash accesses only] 3h: Unexpected completion received from Slave (i.e. completion without non-posted request or completion with invalid tag or completion with invalid length) [for Slave-Attached Flash accesses only] 4h: Unsupported Cycle Type (w.r.t. Command) 5h: Slave Response Code: NONFATAL_ERROR received in response to PUT_FLASH_NP [for Slave-Attached Flash accesses only]. 6h: Unsupported Address (i.e., address > Flash linear address range) [for Master-Attached Flash accesses only] set to Flash Access Error 7h: Reserved 8h-Fh: Reserved Note: This field is updated after a Flash Access Channel transaction is completed if the FCNFES bit is not set
7	1h RW	**Master Attached Flash Request Priority (MAFRP):** 1'b0: MAF Completion Requests are highest priority 1'b1: MAF Non-posted Requests are highest priority

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RW	**Flash Access Channel Fatal Error Reporting Enable (FCFEE):** 00: Disable Fatal Error Reporting 01: Reserved 10: Enable Fatal Error Reporting as SERR (SB Do_SErr message) 11: Enable Fatal Error Reporting as SMI (SB Assert_SMI message) Notes: 1. SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# isdeasserted. 2. SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. 3. SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted).
4	0h RW/1C/V	**Flash Access Channel Fatal Error Status (FCFES):** This field is set by hardware if a Fatal Error condition is detected on the Flash Access Channel. Software must clear this bit by writing a 1 to it. 0: No Fatal Error detected 1: Fatal Error Type 2 detected (FCFEC has a non-zero value) Notes: 1. Clearing this unlocks the FCFEC field and triggers an IOSF-SB Deassert_SMI message if FCFEE is set to SMI. 2. Setting of this bit is independent of the enable to generate a SMI/SERR (FCFEE).
3:0	0h RO/V	**Flash Access Channel Fatal Error Cause (FCFEC):** 0h: No error 1h – 7h: Reserved 8h: Malformed Slave Response Payload: Payload length > Max Payload Size [Type 2] 9h: Malformed Slave Response Payload: Read request size > Max Read Request Size [for Master-Attached Flash accesses only] [Type 2] Ah – Fh: Reserved Note: This field is updated after a Flash Access Channel transaction is completed if the FCFES bit is not set.

2.2.6 Link Error for Slave 0 (LNKERR_SLV0)—Offset 4050h

This register is used to control link error reporting for the eSPI Slave 0.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: FF00h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**eSPI Link and Slave Channel Recovery Required (SLCRR):** HW sets this bit when it has detected a Type 1 Fatal Error condition, for any channel (LFET1C is non-zero). Setting of this bit will trigger an error handling sequence by the eSPI-MC, followed by the suspension of all HW initiated transactions on the eSPI link with the Slave. SW must clear this bit (by writing a 1 to it) after it has taken all necessary actions to recover the link. This indicates the eSPI-MC to resume HW initiated transactions with the Slave.
30:23	0h RO	Reserved.
22:21	0h RW	**Fatal Error Type 1 Reporting Enable (LFET1E):** 00: Disable Fatal Error Type 1 Reporting 01: Reserved 10: Enable Fatal Error Type 1 Reporting as SERR (IOSF-SB Do_SErr message) 11: Enable Fatal Error Type 1 Reporting as SMI (IOSF-SB Assert_SMI message) Notes: 1. SERR enable is also qualified by PCCMD.SEE (Offset 04h) when PLTRST# is deasserted. 2. SERR also sets PCSTS.SSE (Offset 06h) when PLTRST# is deasserted. 3. SMI/SERR messages are not generated if the Host is in reset (PLTRST# asserted). 4. When this error is reported, SW must also inspect and handle the SLCRR field.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW/1C/V	**Fatal Error Type 1 Reporting Status (LFET1S):** This field is set by hardware if a Link Fatal Error Type 1 condition is detected on the eSPI link (any transaction). Software must clear this bit by writing a 1 to it. 0: No Link Fatal Error Type 1 detected 1: Fatal Error Type 1 detected (LFET1C has a non-zero value) Note: 1. Clearing this unlocks the LFET1C field and triggers an IOSF-SB Deassert_SMI message if LFET1E is set to SMI. 2. Setting of this bit is independent of the enable to generate a SMI/SERR (LFET1E).
19:16	0h RO/V	**Link Fatal Type 1 cause (LFET1C):** 4'h0: No error 4'h1: Slave Response Code: NO_RESPONSE [Type 1] 4'h2: Slave Response Code: FATAL_ERROR [Type 1] 4'h3: Slave Response Code: CRC_ERROR [Type 1] 4'h4: Invalid Slave Response Code (w.r.t. to Command) [Type 1] 4'h5: Invalid Slave Cycle Type (w.r.t. to Command) [Type 1] 4'h6 - 4'hF: Reserved Note: 1. This field is updated after a transaction (any channel) is completed if the LFET1S bit is clear. 2. A non-zero value in this field also causes the SLCRR bit to be set.
15:8	FFh RO/V	**Link Fatal Error Type 1 Cycle Type (LFET1CTYP):** When LFET1C is set, this field reflects the Cycle Type for the transaction that encountered the Fatal Error Type 1. If no valid Cycle Type exists w.r.t. the Command (LFET1CMD), this field is set to 8hFF to indicate that it should be ignored. **Note:** This field is updated after a transaction (any channel) is completed if the LFET1S bit is clear.
7:0	0h RO/V	**Link Fatal Error Type 1 Command (LFET1CMD):** When LFET1C is set, this field reflects the Command for the transaction that encountered the Fatal Error Type 1. **Note:** This field is updated after a transaction (any channel) is completed if the LFET1S bit is clear.

3 P2SB Bridge (D31:F1)

3.1 P2SB PCI Configuration Registers Summary

Table 3-1. Summary of P2SB PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	PCI Identifier (PCIID)—Offset 0h	XXXX8086h
4h	5h	PCI Command (PCICMD)—Offset 4h	4h
8h	Bh	Revision ID (PCIRID_CC)—Offset 8h	XXh
Eh	Eh	PCI Header Type (PCIHTYPE)—Offset Eh	0h
10h	13h	Sideband Register Access BAR (SBREG_BAR)—Offset 10h	4h
14h	17h	Sideband Register BAR High DWORD (SBREG_BARH)—Offset 14h	0h
2Ch	2Fh	PCI Subsystem Identifiers (PCIHSS)—Offset 2Ch	0h
34h	34h	PCI Capabilities Pointer (CAPPTR)—Offset 34h	0h
52h	53h	ERROR Bus:Device:Function (EBDF)—Offset 52h	F8h
54h	57h	Routing Configuration (RCFG)—Offset 54h	C700h
60h	60h	High Performance Event Timer Configuration (HPTC)—Offset 60h	0h
64h	65h	IOxAPIC Configuration (IOAC)—Offset 64h	0h
6Ch	6Dh	IOxAPIC Bus:Device:Function (IBDF)—Offset 6Ch	F8h
70h	71h	HPET Bus:Device:Function (HBDF)—Offset 70h	F8h
C0h	C3h	Display Bus:Device:Function (DISPBDF)—Offset C0h	60010h
C4h	C5h	ICC Register Offsets (ICCOS)—Offset C4h	0h
D0h	D3h	SBI Address (SBIADDR)—Offset D0h	0h
D4h	D7h	SBI Data (SBIDATA)—Offset D4h	0h
D8h	D9h	SBI Status (SBISTAT)—Offset D8h	0h
DAh	DBh	SBI Routing Identification (SBIRID)—Offset DAh	0h
DCh	DFh	SBI Extended Address (SBIEXTADDR)—Offset DCh	0h
E0h	E3h	P2SB Control (P2SBC)—Offset E0h	0h
E4h	E4h	Power Control Enable (PCE)—Offset E4h	1h
200h	203h	Sideband Register Posted 0 (SBREGPOSTED0)—Offset 200h	0h
204h	207h	Sideband Register Posted 1 (SBREGPOSTED1)—Offset 204h	0h
208h	20Bh	Sideband Register Posted 2 (SBREGPOSTED2)—Offset 208h	0h
20Ch	20Fh	Sideband Register Posted 3 (SBREGPOSTED3)—Offset 20Ch	0h
210h	213h	Sideband Register Posted 4 (SBREGPOSTED4)—Offset 210h	0h
214h	217h	Sideband Register Posted 5 (SBREGPOSTED5)—Offset 214h	0h
218h	21Bh	Sideband Register Posted 6 (SBREGPOSTED6)—Offset 218h	0h
21Ch	21Fh	Sideband Register Posted 7 (SBREGPOSTED7)—Offset 21Ch	0h
220h	223h	Endpoint Mask 0 (EPMASK0)—Offset 220h	0h
224h	227h	Endpoint Mask 1 (EPMASK1)—Offset 224h	0h
228h	22Bh	Endpoint Mask 2 (EPMASK2)—Offset 228h	0h

Table 3-1. Summary of P2SB PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
22Ch	22Fh	Endpoint Mask 3 (EPMASK3)—Offset 22Ch	0h
230h	233h	Endpoint Mask 4 (EPMASK4)—Offset 230h	0h
234h	237h	Endpoint Mask 5 (EPMASK5)—Offset 234h	0h
238h	23Bh	Endpoint Mask 6 (EPMASK6)—Offset 238h	0h
23Ch	23Fh	Endpoint Mask 7 (EPMASK7)—Offset 23Ch	0h

3.1.1 PCI Identifier (PCIID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: XXXX8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO/V	**Device Identification (DID):** Indicates the device identification. Refer the Device and Revision ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor Identification (VID):** Indicates Intel

3.1.2 PCI Command (PCICMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RO	**Interrupt Disable (INTD):** P2SB does not issue any interrupts on its own behalf
9	0h RO	**Fast Back to Back Enable (FB2BE):** Not applicable
8:6	0h RO	Reserved.
5	0h RO	**VGA Palette Snoop (VGA):** Not applicable.
4	0h RO	**Memory Write & Invalidate Enable (MWIE):** Not applicable.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Special Cycle Enable (SCE):** Not applicable.
2	1h RO	**Bus Master Enable (BME):** Bus mastering cannot be disabled as this device acts as a proxy for non-PCI devices.
1	0h RW	**Memory Space Enable (MSE):** Will control the P2SB acceptance of PCI MMIO BARs only. Other legacy regions are unaffected by this bit.
0	0h RW	**I/O Space Enable (IOSE):** Legacy regions are unaffected by this bit.

3.1.3 Revision ID (PCIRID_CC)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: XXh

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	-- RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

3.1.4 PCI Header Type (PCIHTYPE)—Offset Eh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Multi-Function Device (MFD):** Indicates that this is part of a multi-function device.
6:0	0h RO	**Header Type (HTYPE):** Indicates a generic device header.

3.1.5 Sideband Register Access BAR (SBREG_BAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Register Base Address (RBA):** Lower DWORD of the base address for the sideband register access BAR.
23:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PREF):** Indicates this is not prefetchable.
2:1	2h RO	**Address Type (ATYPE):** Indicates that this can be placed anywhere in 64b space.
0	0h RO	**Space Type (STYPE):** Indicates memory space

3.1.6 Sideband Register BAR High DWORD (SBREG_BARH)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Register Base Address (RBAH):** Upper DWORD of the base address for the sideband register access BAR.

3.1.7 PCI Subsystem Identifiers (PCIHSS)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** Written by BIOS. Not used by hardware.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** Written by BIOS. Not used by hardware.

3.1.8 PCI Capabilities Pointer (CAPPTR)—Offset 34h

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW/O	**Capabilities Pointer (CPTR):** Indicates the offset of the first Capability Item.

3.1.9 ERROR Bus:Device:Function (EBDF)—Offset 52h

This register specifies the bus:device:function ID that the Error Signalling messages will use for its Requester ID. This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: F8h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Bus Number (BUS):** ERROR Bus Number
7:3	1Fh RW	**Device Number (DEV):** ERROR Device Number
2:0	0h RW	**Function Number (FUNC):** ERROR Function Number

3.1.10 Routing Configuration (RCFG)—Offset 54h

This register contains information used for routing transactions between primary and sideband interfaces.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: C700h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	C7h RW	**Reserved Page Register Destination ID (RPRID):** Specifies the sideband destination ID for sending Reserved Page Register cycles (e.g. Port 80h). By default this will load to the ID of eSPI device if it's enabled by pin strap.
7:1	0h RO	Reserved.
0	0h RW	**RTC Shadow Enable (RSE):** When set, all IO writes to the RTC will be also sent to the PMC. This allows cases where the battery backed storage is in an external PMIC.

3.1.11 High Performance Event Timer Configuration (HPTC)—Offset 60h

HPET configuration register

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**Address Enable (AE):** When set, the P2SB will decode the High Performance Timer memory address range selected by bits 1:0 below.
6:2	0h RO	Reserved.
1:0	0h RW	**Address Select (AS):** This 2-bit field selects 1 of 4 possible memory address ranges for the High Performance Timer functionality. The encodings are: 00 : FED0_0000h - FED0_03FFFh 01 : FED0_1000h - FED0_13FFFh 10 : FED0_2000h - FED0_23FFFh 11 : FED0_3000h - FED0_33FFFh

3.1.12 IOxAPIC Configuration (IOAC)—Offset 64h

IOAPIC configuration register

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	Reserved.
8	0h RW	**Address Enable (AE):** When set, the P2SB will decode the IOxAPIC memory address range selected by bits 7:0 below.
7:0	0h RW	**APIC Range Select (ASEL):** These bits define address bits 19:12 for the IOxAPIC range. The default value of 00h enables compatibility with prior products as an initial value. This value must not be changed unless the IOxAPIC Enable bit is cleared.

3.1.13 IOxAPIC Bus:Device:Function (IBDF)—Offset 6Ch

This register specifies the bus:device:function ID that the IOxAPIC will use in the following cases: - As the Requester ID when initiating Interrupt Messages to the processor.
- As the Completer ID when responding to the reads targeting the IOxAPICs Memory-Mapped I/O registers.
This field is default to Bus 0:Device 31:Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required for the internal IOxAPIC.

Access Method

Type: CFG Register (Size: 16 bits)

Device: 31
Function: 1

Default: F8h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Bus Number (BUS):** IOxAPIC Bus Number
7:3	1Fh RW	**Device Number (DEV):** IOxAPIC Device Number
2:0	0h RW	**Function Number (FUNC):** IOxAPIC Function Number

3.1.14 HPET Bus:Device:Function (HBDF)—Offset 70h

This register specifies the bus:device:function ID that the HPET device will use in the following cases:
- As the Requester ID when initiating Interrupt Messages to the processor
- As the Completer ID when responding to the reads targeting the corresponding HPETs Memory-Mapped I/O registers.
This field is default to Bus 0:Device 31:Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required for the corresponding HPET.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: F8h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Bus Number (BUS):** HPET Bus Number
7:3	1Fh RW	**Device Number (DEV):** HPET Device Number
2:0	0h RW	**Function Number (FUNC):** HPET Function Number

3.1.15 Display Bus:Device:Function (DISPBDF)—Offset C0h

This register specifies the bus:device:function ID that the Display initiated upstream RAVDMs will use for its Requester ID. This will also be used for the claiming these Route-by-ID RAVDMs downstream.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 60010h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18:16	6h RW	**Display Target Block (DTBLK):** This register contains the Target BLK field that will be used when sending RAVDM messages to the CPU Complex North Display.
15:8	0h RW	**Bus Number (BUS):** The bus number of the Display in the CPU Complex.
7:3	2h RW	**Device Number (DEV):** The bus number of the Display in the CPU Complex.
2:0	0h RW	**Function Number (FUNC):** The function number of the Display in the CPU Complex

3.1.16 ICC Register Offsets (ICCOS)—Offset C4h

This register contains the offsets to be used when sending RAVDMs to the Integrated Clock Controller. Each of the two spaces decoded for the ICC have a separate base address that will be used when sending those transactions on IOSF-SB to the ICC.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Modulator Control Address Offset (MODBASE):** This specifies the upper 8b for the 16b address that will be used for sending RAVDM access that target the Modulator Control range of the ICC (FFF00h - FFFFFh).
7:0	0h RW	**Buffer Address Offset (BUFBASE):** This specifies the upper 8b for the 16b address that will be used for sending RAVDM access that target the Buffer range of the ICC (FFE00h - FFEFFh).

3.1.17 SBI Address (SBIADDR)—Offset D0h

Provides mechanism to send message on sideband interface.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**Destination Port ID (DESTID):** The content of this register field is sent in the Sideband Message Register Access dest field.
23:16	0h RO	Reserved.
15:0	0h RW	**Address Offset (OFFSET):** Register address offset. The content of this register field is sent in the Sideband Message Register Access address(15:0) field.

3.1.18 SBI Data (SBIDATA)—Offset D4h

Provides mechanism to send message on sideband interface.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Data (DATA):** The content of this register field is sent on the sideband Message Register Access data(31:0) field.

3.1.19 SBI Status (SBISTAT)—Offset D8h

Provides mechanism to send message on sideband interface.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**Opcode (OPCODE):** This is the Opcode sent in the sideband message.
7	0h RW	**Posted (POSTED):** When set to 1, the message will be sent as a posted message instead of non-posted. This should only be used if the receiver is known to support posted operations for the specified operation.
6:3	0h RO	Reserved.
2:1	0h RW/V	**Response Status (RESPONSE):** 00 - Successful 01 - Unsuccessful / Not Supported 10 - Powered Down 11 - Multi-cast Mixed This register reflects the response status for the previously completed transaction. The value of this register is only meaningful if SBISTAT.INITRDY is zero.
0	0h RW/1S	**Initiate/ Ready# (INITRDY):** 0: The sideband interface is ready for a new transaction 1: The sideband interface is busy with the previous transaction. A write to set this register bit to 1 will trigger a sideband message on the private sideband interface. The message will be formed based on the values programmed in the Sideband Message Interface Register Access registers. Software needs to ensure that the interface is not busy (SBISTAT.INITRDY is clear) before writing to this register.

3.1.20 SBI Routing Identification (SBIRID)—Offset DAh

Provides mechanism to send message on sideband interface.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RW	**First Byte Enable (FBE):** The content of this field is sent in the Sideband Register Access FBE field.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	Reserved.
10:8	0h RW	**Base Address Register (BAR):** The contents of this field are sent in the Sideband Register Access BAR field. This should be zero performing a Memory Mapped operation to a PCI compliant device.
7:0	0h RW	**Function ID (FID):** The contents of this field are sent in the Sideband Register access FID field.This field should generally remain at zero unless specifically required by a particular application.

3.1.21 SBI Extended Address (SBIEXTADDR)—Offset DCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Extended Address (ADDR):** The content of this register field is sent on the sideband Message Register Access address(48:32) field.This must be set to all 0 if 16b addressing is desired.

3.1.22 P2SB Control (P2SBC)—Offset E0h

P2SB general configuration register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/O	**SBI register Lock (SBILOCK):** Once written, it will not be writeable until reset. When 1, the bit will lock down access to the P2SB SB interface registers (P2SB PCI offsets D0h - DFh)
30:18	0h RO	Reserved.
17	0h RW/O	**Endpoint Mask Lock (MASKLOCK):** Locks the value of the EPMASK[0-7] registers. Once this value is written to a one it may only be cleared by a reset.

Bit Range	Default & Access	Field Name (ID): Description
16:9	0h RO	Reserved.
8	0h RW	**Hide Device (HIDE):** When this bit is set, the P2SB will return 1s on any PCI Configuration Read on sideband interface. All other transactions including PCI Configuration Writes are unaffected by this. This does not affect reads performed on the SB interface.
7:0	0h RO	Reserved.

3.1.23 Power Control Enable (PCE)—Offset E4h

Power Control Enable register

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 1

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	Reserved.
5	0h RW	**Hardware Autonomous Enable (HAE):** When set, the P2SB will automatically engage power gating when it has reached its idle condition.
4:3	0h RO	Reserved.
2	0h RO	**D3-Hot Enable (D3HE):** No support for D3 Hot power gating.
1	0h RO	**I3 Enable (I3E):** No support for S0i3 power gating.
0	1h RW	**PMC Power Gating Enable (PMCPG_EN):** When set to 1, the P2SB will engage power gating if it is idle (and an internal PMC power gating signal is asserted.)

3.1.24 Sideband Register Posted 0 (SBREGPOSTED0)—Offset 200h

Provides a mechanism to send MMIO writes as posted writes on the sideband space.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 0 (SBREGPOSTED0):** One hot masks for setting SBREG to posted posted for SB endpoint IDs 31-0.

3.1.25 Sideband Register Posted 1 (SBREGPOSTED1)—Offset 204h

Provides an mechanism to send MMIO writes as posted writes on the sideband space.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 1 (SBREGPOSTED1):** One hot masks for setting SBREG to posted for SB endpoint IDs 63-32.

3.1.26 Sideband Register Posted 2 (SBREGPOSTED2)—Offset 208h

Provides an mechanism to send MMIO writes as posted writes on the sideband space.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 0 (SBREGPOSTED2):** One hot masks for setting SBREG to posted for SB endpoint IDs 95-64.

3.1.27 Sideband Register Posted 3 (SBREGPOSTED3)—Offset 20Ch

Provides a mechanism to send MMIO writes as posted writes on the sideband space.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 3 (SBREGPOSTED3):** One hot masks for setting SBREG to posted for SB endpoint IDs 127-96.

3.1.28 Sideband Register Posted 4 (SBREGPOSTED4)—Offset 210h

Provides a mechanism to send MMIO writes as posted writes on the sideband space.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 4 (SBREGPOSTED4):** One hot masks for setting SBREG to posted for SB endpoint IDs 159-128.

3.1.29 Sideband Register Posted 5 (SBREGPOSTED5)—Offset 214h

Provides a mechanism to send MMIO writes as posted writes on the sideband space.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 5 (SBREGPOSTED5):** One hot masks for setting SBREG to posted for SB endpoint IDs 191-160.

3.1.30 Sideband Register Posted 6 (SBREGPOSTED6)—Offset 218h

Provides a mechanism to send MMIO writes as posted writes on the sideband space.

Access Method

Type: CFG Register (Size: 32 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 6 (SBREGPOSTED6):** One hot masks for setting SBREG to posted for IOSF-SB endpoint IDs 223-192.

3.1.31 Sideband Register Posted 7 (SBREGPOSTED7)—Offset 21Ch

Provides a mechanism to send MMIO writes as posted writes on the sideband space.

Access Method

Type: CFG Register (Size: 32 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Sideband Register Posted 7 (SBREGPOSTED7):** One hot masks for setting SBREG to posted for SB endpoint IDs 255-224.

3.1.32 Endpoint Mask 0 (EPMASK0)—Offset 220h

Provides a mechanism for disabling particular SB endpoints from being allowed to targeted by transactions from the P2SB.

Access Method

Type: CFG Register (Size: 32 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 0 (EPMASK0):** One hot masks for disabling SB endpoint IDs 31-0.

3.1.33 Endpoint Mask 1 (EPMASK1)—Offset 224h

Provides a mechanism for disabling particular SB endpoints from being allowed to targeted by transactions from the P2SB.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 31 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 1 (EPMASK1):** One hot masks for disabling SB endpoint IDs 63-32.

3.1.34 Endpoint Mask 2 (EPMASK2)—Offset 228h

Provide a mechanism for disabling particular SB endpoints from being allowed to targeted by transactions from the P2SB.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 31 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 2 (EPMASK2):** One hot masks for disabling SB endpoint IDs 95-64

3.1.35 Endpoint Mask 3 (EPMASK3)—Offset 22Ch

Provides a mechanism for disabling particular SB endpoints from being allowed to targeted by transactions from the P2SB.

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 31 **Function:** 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 3 (EPMASK3):** One hot masks for disabling SB endpoint IDs 127-96

3.1.36 Endpoint Mask 4 (EPMASK4)—Offset 230h

Provides a mechanism for disabling particular SB endpoints from being allowed to targeted by transactions from the P2SB.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 4 (EPMASK4):** One hot masks for disabling SB endpoint IDs 128-159

3.1.37 Endpoint Mask 5 (EPMASK5)—Offset 234h

Provides a mechanism for disabling particular SB endpoints from being allowed to targeted by transactions from the P2SB.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 5 (EPMASK5):** One hot masks for disabling SB endpoint IDs 191-160

3.1.38 Endpoint Mask 6 (EPMASK6)—Offset 238h

Provides a mechanism for disabling particular SB endpoints from being allowed to targeted by transactions from the P2SB.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 6 (EPMASK6):** One hot masks for disabling SB endpoint IDs 223-192

3.1.39 Endpoint Mask 7 (EPMASK7)—Offset 23Ch

Provides a mechanism for disabling particular SB endpoints from being allowed to targeted by transactions from the P2SB.

Access Method

Type: CFG Register (Size: 32 bits)

Device: 31
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**Endpoint Mask 7 (EPMASK7):** One hot masks for disabling SB endpoint IDs 255-224

4 PMC Controller (D31:F2)

4.1 Power Management Configuration Registers Summary

The power management registers are distributed within the PCI Device 31: Function 2 space, with dedicated I/O and memory-mapped spaces.
Bits not explicitly defined in each register are assumed to be reserved. Writes to reserved bits must retain their previous values. Other than a read/modify/write, software should not attempt to use the value read from a reserved bit, as it may not be consistently 1 or 0.

Table 4-1. Summary of Power Management Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device Vendor ID (DEVVENDID)—Offset 0h	XXXX8086h
4h	7h	Status and Command (STATUSCOMMAND)—Offset 4h	0h
8h	Bh	Class Code and Revision ID (REVCLASSCODE)—Offset 8h	000000XXh
Ch	Fh	Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	0h
10h	13h	PWRMBASE (BAR)—Offset 10h	4h
14h	17h	Base Address High (BAR_HIGH)—Offset 14h	0h
20h	23h	Base Address 2 (BAR2)—Offset 20h	0h
2Ch	2Fh	Subsystem Identifiers (SUBSYSTEMID)—Offset 2Ch	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	Interrupt Register (INTERRUPTREG)—Offset 3Ch	100h
80h	83h	Power Management Capability ID (POWERCAPID)—Offset 80h	48000001h
84h	87h	PME Control Status (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
98h	9Bh	D0I3 Control SW LTR MMIO (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	Device Idle Pointer (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	0h
A0h	A3h	D0I3 MAX POW LAT PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	800h
B0h	B3h	General Purpose Read Write 1 (GEN_REGRW1)—Offset B0h	0h
B4h	B7h	General Purpose Read Write 2 (GEN_REGRW2)—Offset B4h	0h
B8h	BBh	General Purpose Read Write 3 (GEN_REGRW3)—Offset B8h	0h
BCh	BFh	General Purpose Read Write 4 (GEN_REGRW4)—Offset BCh	0h
C0h	C3h	General Purpose Input (GEN_INPUT_REG)—Offset C0h	0h

4.1.1 Device Vendor ID (DEVVENDID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: XXXX8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	-- RO	**Device Identification (DEVICEID):** Refer to the Revision and Device ID Table in Volume 1 for default value.
15:0	8086h RO	**Vendor Identification (VENDORID):** This is a 16-bit value assigned to Intel. Intel VID=8086h.

4.1.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** Set when the bridge receives a completion with unsupported request status. This bit is reset by PLTRST# assertion.
28	0h RW/1C	**Received Target Abort (RTA):** Set when the bridge receives a completion with completer abort status. This bit is reset by PLTRST# assertion.
27:20	0h RO	Reserved.
19	0h RO	**Interrupt Status (INTR_STATUS)**
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE)**
9	0h RO	Reserved.
8	0h RW	**System Error Enable (SERR_ENABLE)**
7:3	0h RO	Reserved.
2	0h RW	**Bus Master Enable (BME):** Bus master Enable does not apply to messages sent out by PMC. This bit is reset by PLTRST# assertion.
1	0h RW	**Memory Space Enable (MSE):** Controls a device's response to Memory Space accesses. This bit controls whether the host to PMC MMIO BAR is enabled or not. This bit is reset by PLTRST# assertion.
0	0h RO	Reserved.

4.1.3 Class Code and Revision ID (REVCLASSCODE)—Offset 8h

Revision Class Codes

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 000000XXh

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	**Class Codes (CLASS_CODES)**
7:0	-- RO	**Revision ID (RID):** Indicates stepping of the host controller. Refer to the Device and Revision ID Table in Volume 1 for specific value. This field is reset by PLTRST# assertion.

4.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Cache Line Latency Header And BIST

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RO	**Multi Function Device (MULFNDEV):** Indicates that this is part of a multi-function device.
22:16	0h RO	**Header Type (HEADERTYPE):** Indicates a generic device header.
15:8	0h RO	**Latency Timer (LATTIMER):** Latency Timer
7:0	0h RW	**Cache Line Size (CACHELINE_SIZE):** Cache line Size

4.1.5 PWRMBASE (BAR)—Offset 10h

Base Address for MMIO Registers.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:13	0h RW	**BAR (BASEADDR):** Software programs this register with the base address of the device's memory region
12:4	0h RO	**Size Indicator (SIZEINDICATOR):** Hardwired to 0 to indicate 8KB of memory space
3	0h RO	**Prefetchable (PREFETCHABLE):** A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables. Hardwired to 0 to indicate the device's memory space as notprefetchable.
2:1	2h RO	**Type (TYPE):** Hardwired to 10 to indicate that Base register is 64 bits wide and mapping can be done anywhere in the 64-bit Memory Space.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** Hardwired to 0 to identify a Memory BAR.

4.1.6 Base Address High (BAR_HIGH)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address HIGH (BASEADDR_HIGH):** Base Address

4.1.7 Base Address 2 (BAR2)—Offset 20h

Base Address for ACPI Power Management IO (ACPI base).

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:7	0h RW	**Base Address (BASEADDR):** Base Address
6:1	0h RO	Reserved.
0	0h RO	**Message Space (MESSAGE_SPACE):** Message Space

4.1.8 Subsystem Identifiers (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SUBSYSTEMID):** Written by BIOS. Not used by hardware.
15:0	0h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** Written by BIOS. Not used by hardware.

4.1.9 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**Capabilities Pointer (CAPPTR_POWER):** Capabilities Pointer

4.1.10 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 100h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Interrupt Pin
7:0	0h RW	**Interrupt Line (INTLINE):** Interrupt Line

4.1.11 Power Management Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 48000001h

Bit Range	Default and Access	Field Name (ID): Description
31:27	9h RO	**PME Support (PMESUPPORT):** PME Support
26:16	0h RO	Reserved.
15:8	0h RO	**Next Capability (NXTCAP):** Next Capability
7:0	1h RO	**Power Management Capability (POWER_CAP):** Power Management Capability

4.1.12 PME Control Status (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** PME Status
14:9	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
8	0h RW	**PME Enable (PMEENABLE):** No HW impact.
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NO_SOFT_RESET)**
2	0h RO	Reserved.
1:0	0h RW	**Power State (POWERSTATE):** Power State

4.1.13 PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: F0140009h

Bit Range	Default and Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Capability (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision (REVID):** Vendor Specific Capability Revision
23:16	14h RO	**Capability Length (CAP_LENGTH):** Vendor Specific Capability Length
15:8	0h RO	**Next Capability (NEXT_CAP):** NEXT Capability
7:0	9h RO	**Capability ID (CAPID):** Capability ID

4.1.14 D0I3 Control SW LTR MMIO (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

SW LTR Update MMIO Location Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	**SW_LAT_DWORD_OFFSET (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location
3:1	0h RO	**SW_LAT_BAR_NUM (SW_LAT_BAR_NUM):** SW LTR Bar Num
0	0h RO	**SW_LAT_VALID (SW_LAT_VALID):** SW LTR Valid Strap

4.1.15 Device Idle Pointer (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	**DWORD_OFFSET (DWORD_OFFSET):** Device MMIO Offset Location
3:1	0h RO	**BAR_NUM (BAR_NUM):** D0i3 MMIO Location
0	0h RO	**VALID (VALID):** D0i3 Valid Strap

4.1.16 D0I3 MAX POW LAT PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 800h

Bit Range	Default and Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW	**HAE (HAE):** Hardware Autonomous Enable
20	0h RO	Reserved.
19	0h RW	**SLEEP_EN (SLEEP_EN):** Sleep Enable

Bit Range	Default and Access	Field Name (ID): Description
18	0h RW	**PGE (PGE):** Power Gate Enable
17	0h RW	**I3_ENABLE (I3_ENABLE):** I3 Enable
16	0h RW	**PMCRE (PMCRE):** PMC Request Enable
15:13	0h RO	Reserved.
12:10	2h RW/O	**POW_LAT_SCALE (POW_LAT_SCALE):** Power On Latency Scale
9:0	0h RW/O	**POW_LAT_VALUE (POW_LAT_VALUE):** Power On Latency Value

4.1.17 General Purpose Read Write 1 (GEN_REGRW1)—Offset B0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW1 (GEN_REG_RW1):** General Purpose PCI Register

4.1.18 General Purpose Read Write 2 (GEN_REGRW2)—Offset B4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW2 (GEN_REG_RW2):** General Purpose PCI Register

4.1.19 General Purpose Read Write 3 (GEN_REGRW3)—Offset B8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW3 (GEN_REG_RW3):** General Purpose PCI Register

4.1.20 General Purpose Read Write 4 (GEN_REGRW4)—Offset BCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW4 (GEN_REG_RW4):** General Purpose PCI Register

4.1.21 General Purpose Input (GEN_INPUT_REG)—Offset C0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**GEN REG INPUT_RW (GEN_REG_INPUT_RW):** General Purpose Input Register

4.2 PMC I/O Based Registers Summary

The ACPI power management I/O registers are accessed based upon offsets from PM Base Address, BAR2, defined in PCI Device 31: Function 2.

Table 4-2. Summary of PMC I/O Based Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Power Management 1 Enables and Status (PM1_EN_STS)—Offset 0h	0h
4h	7h	Power Management 1 Control (PM1_CNT)—Offset 4h	0h
8h	Bh	Power Management 1 Timer (PM1_TMR)—Offset 8h	0h
20h	23h	Thermal Timer Delay (THERM_TIMER_DELAY)—Offset 20h	0h
30h	33h	SMI Control and Enable (SMI_EN)—Offset 30h	2h
34h	37h	SMI Status Register (SMI_STS)—Offset 34h	0h
40h	43h	General Purpose Event Control (GPE_CTRL)—Offset 40h	0h
50h	53h	PM2a Control Block (PM2A_CNT_BLK)—Offset 50h	0h
54h	57h	Over-Clocking WDT Control (OC_WDT_CTL)—Offset 54h	2000h
60h	63h	General Purpose Event 0 Status [31:0] (GPE0_STS_31_0)—Offset 60h	0h
64h	67h	General Purpose Event 0 Status [63:32] (GPE0_STS_63_32)—Offset 64h	0h
68h	6Bh	General Purpose Event 0 Status [95:64] (GPE0_STS_95_64)—Offset 68h	0h
6Ch	6Fh	General Purpose Event 0 Status [127:96] (GPE0_STS[127:96])—Offset 6Ch	0h
70h	73h	General Purpose Event 0 Enable [31:0] (GPE0_EN_31_0)—Offset 70h	0h
74h	77h	General Purpose Event 0 Enable [63:32] (GPE0_EN_63_32)—Offset 74h	0h
78h	7Bh	General Purpose Event 0 Enable [95:64] (GPE0_EN_95_64)—Offset 78h	0h
7Ch	7Fh	General Purpose Event 0 Enable [127:96] (GPE0_EN[127:96])—Offset 7Ch	0h

4.2.1 Power Management 1 Enables and Status (PM1_EN_STS)—Offset 0h

Power Management 1 Enables and Status

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	0h RW	**PCI Express Wake Disable (PCIEXP_WAKE_DIS):** This bit disables the inputs to the PCIEXP_WAKE_STS bit in the PM1 Status register from waking the system. Modification of this bit has no impact on the value of the PCIEXP_WAKE_STS bit. This bit is reset by DSW_PWROK de-assertion.
29:27	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
26	0h RW/V	**RTC Alarm Enable (RTC_EN):** This is the RTC alarm enable bit. It works in conjunction with the SCI_EN bit as described below. RTC_EN: SCI_EN: Effect when RTC_STS is set 0: X: No SMI# or SCI. If system was in S3-S5, no wake even occurs. 1: 0: SMI#. If system was in S3-S5, then a wake event occurs before the SMI#. 1: 1: SCI. If system was in S3-S5, then a wake event occurs before the SCI. Note: This bit is in the RTC well and is reset by RTCRST# assertion, to allow an RTC event to wake after a power failure.
25	0h RO	Reserved.
24	0h RW/V	**Power Button Enable (PWRBTN_EN):** This bit is the power button enable. It works in conjunction with the SCI_EN bit as described below: PWRBTN_EN: SCI_EN: Effect when PWRBTN_STS is set 0: X: No SMI# or SCI 1: 0: SMI#. 1: 1: SCI. NOTE: PWRBTN_EN has no effect on the PWRBTN_STS bit being set by the assertion of the power button. The Power Button is always enabled as a Wake event.
23:22	0h RO	Reserved.
21	0h RW	**Global Enable (GBL_EN):** Global enable bit. When both the GBL_EN and the GBL_STS are set, PCH generates an SCI. This bit is reset by PLTRST# assertion.
20:17	0h RO	Reserved.
16	0h RW	**Timer Overflow Interrupt Enable (TMROF_EN):** This is the timer overflow interrupt enable bit. It works in conjunction with the SCI_EN bit as described below: TMROF_EN: SCI_EN: Effect when TMROF_STS is set 0: X: No SMI# or SCI. 1: 0: SMI#. 1: 1: SCI. This bit is reset by PLTRST# assertion.
15	0h RW/1C/V	**Wake Status (WAK_STS):** This bit is set when the system is in one of the Sleep states (via the SLP_EN bit) and an enabled Intel PCH Wake event occurs. Upon setting this bit, the Intel PCH will transition the system to the ON state. This bit can only be set by hardware and can only be cleared by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST#. If a power failure occurs (such as removed batteries) without the SLP_EN bit set, the WAK_STS bit will not be set when the power returns if the AFTER_G3 bit is 0. If the AFTER_G3 bit is 1, then the WAK_STS bit will be set after waking from a power failure. If necessary, the BIOS can clear the WAK_STS bit in this case.
14	0h RW/1C/V	**PCI Express Wake Status (PCIEXP_WAKE_STS):** This bit is set by hardware to indicate that the system woke due to a PCI Express wakeup event. This event can be caused by the PCI Express WAKE# pin being active, or one or more of the PCI Express ports being in beacon state, or receipt of a PCI Express PME message at root port. This bit should only be set when one of these events causes the system to transition from a non-S0 system power state to the S0 system power state. This bit is set independant of the PCIEXP_WAKE_DIS bit. Software writes a 1 to clear this bit. If WAKE# pin is still active during the write or one or more PCI Express ports is in the beacon state or PME message received indication is not cleared in the root port, then the bit will remain active (i.e. all inputs to this bit are level sensitive) Note: This bit does not itself cause a wake event or prevent entry to a sleeping state. Thus if the bit is 1 and the system is put into a sleeping state, the system will not automatically wake.
13:12	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RW/1C/V	**Power Button Override (PWRBTNOR_STS):** This bit is set any time a Power Button Override Event occurs (i.e. the power button is pressed for at least 4 consecutive seconds), the corresponding bit is received in the SMBus slave message, the Intel(R)CSME-Initiated Power Button Override bit is set, the Intel(R)CSME-Initiated Host Reset with Power Down is set, or due to an internal thermal sensor catastrophic condition. These events cause an unconditional transition to the S5 state. The BIOS or SCI handler clears this bit by writing a 1 to it. This bit is not affected by hard resets via CF9h writes, and is not reset by RSMRST#. Thus, this bit is on RTC well and is preserved through power failures (reset by RTCRST#). Note that this bit is still asserted when the global SCI_EN is set to '1' then an SCI will be generated.
10	0h RW/1C/V	**RTC Status (RTC_STS):** This bit is set when the RTC generates an alarm (assertion of the IRQ8# signal), and is not affected by any other enable bit. See RTC_EN for the effect when RTC_STS goes active. This bit is only set by hardware and can only be reset by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by DSW_PWROK de-assertion.
9	0h RO	Reserved.
8	0h RW/1C/V	**Power Button Status (PWRBTN_STS):** This bit is set when the PWRBTN# signal is asserted (low), independent of any other enable bit. See PWRBTN_EN for the effect when PWRBTN_STS goes active. PWRBTN_STS is always a wake event. This bit is only set by hardware and can be cleared by software writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by DSW_PWROK de-assertion. If the PWRBTN# signal is held low for more than 4 seconds, the Intel PCH clears the PWRBTN_STS bit, sets the PWRBTNOR_STS bit, the system transitions to the S5 state, and only PWRBTN# is enabled as a wake event. If PWRBTN_STS bit is cleared by software while the PWRBTN# pin is still held low, this will not cause the PWRBTN_STS bit to be set. The PWRBTN# signal must go inactive and active again to set the PWRBTN_STS bit. Note that the SMBus Unconditional Powerdown message, the CPU Thermal Trip and the Internal Thermal Sensors' Catastrophic Condition result in behavior matching the Powerbutton Override, which includes clearing this bit.
7:6	0h RO	Reserved.
5	0h RW/1C/V	**GBL Status (GBL_STS):** This bit is set when an SCI is generated due to the BIOS wanting the attention of the SCI handler. BIOS has a corresponding bit, BIOS_RLS, which will cause an SCI and set this bit. The SCI handler should then clear this bit by writing a 1 to it. This bit will not cause wake events or SMI#. This bit is not effected by SCI_EN. Note: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place. This bit is reset by PLTRST# assertion.
4	0h RW/1C/V	**Bus Master Status (BM_STS):** This bit is set to 1 by the Intel PCH when a PCH-visible bus master requests access to memory or the BM_BUSY# signal is active. This bit is cleared by the Processor writing a 1 to this bit position. This bit will not cause a wake event, SCI, or SMI. This bit is reset by PLTRST# assertion.
3:1	0h RO	Reserved.
0	0h RW/1C/V	**Timer Overflow Status (TMROF_STS):** This is the timer overflow status bit. This bit gets set anytime bit 22 of the 24 bit timer goes low (bits are counted from 0 to 23). This will occur every 2.3435 seconds. See TMROF_EN for the effect when TMROF_STS goes active. Software clears this bit by writing a 1 to it. This bit is reset by PLTRST# assertion.

4.2.2 Power Management 1 Control (PM1_CNT)—Offset 4h

Lockable: No Usage: ACPI or Legacy Power Well: Bits 0-9, 13-31: Primary, Bits 10-12: RTC

Access Method

Type: IO Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h WO	**Sleep Enable (SLP_EN):** This is a write-only bit and reads to it always return a zero. Setting this bit causes the system to sequence into the Sleep state defined by the SLP_TYP field. This bit is reset by PLTRST# assertion.
12:10	0h RW	**Sleep Type (SLP_TYP):** This 3-bit field defines the type of Sleep the system should enter when the SLP_EN bit is set to 1. Bits Mode Typical Mapping 000 ON S0 001 Reserved 010 Reserved 011 Reserved 100 Reserved 101 Suspend-To-RAM S3 110 Suspend-To-Disk S4 111 Soft Off S5 These bits are reset by RTCRST# only.
9:3	0h RO	Reserved.
2	0h WO	**GBL_RLS (GBL_RLS):** This bit always reads as 0. ACPI software writes a '1' to this bit to raise an event to the BIOS. BIOS software has corresponding enable and status bits to control its ability to receive ACPI events.
1	0h RO	Reserved.
0	0h RW	**SCI Enable (SCI_EN):** Selects the SCI interrupt or the SMI# for various events. 0 = These events will generate an SMI#. 1 = These events will generate an SCI. This bit is reset by PLTRST# assertion.

4.2.3 Power Management 1 Timer (PM1_TMR)—Offset 8h

Lockable: No
Usage: ACPI
Power Well: Primary

Access Method

Type: IO Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RO/V	**Timer Value (TMR_VAL):** This read-only field returns the running count of the PM timer. This counter runs off a 3.579545 MHz clock (derived from 14.31818 MHz divided by 4). It is reset (to 0) during a PCI reset, and then continues counting as long as the system is in the S0 state. Anytime bit 22 of the timer goes HIGH to LOW (bits referenced from 0 to 23), the TMROF_STS bit is set. The High-to-Low transition will occur every 2.3435 seconds. Writes to this register have no effect.

4.2.4 Thermal Timer Delay (THERM_TIMER_DELAY)—Offset 20h

Thermal timer delay register

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW	**Thermal Timer Delay (THERM_TIMER_DELAY_VALUE):** Thermal Timer Delay

4.2.5 SMI Control and Enable (SMI_EN)—Offset 30h

Lockable: No
Usage: ACPI or Legacy
Power Well: Primary
Note: This register is symmetrical to the SMI Status Register.

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 2h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**xHCI SMI Enable (xHCI_SMI_EN):** Software sets this bit to enable xHCI SMI events. This bit is reset by PLTRST# assertion.
30	0h RW	**Intel(R) CSME SMI Enable (ME_SMI_EN):** Software sets this bit to enable Intel(R)CSME SMI# events. This bit is reset by PLTRST# assertion.
29	0h RO	Reserved.
28	0h RW/L	**eSPI SMI Enable (ESPI_SMI_EN):** Software sets this bit to enable eSPI SMI events. This bit is reset by PLTRST# assertion.
27	0h RW/1S	**GPIO Unlock SMI Enable (GPIO_UNLOCK_SMI_EN):** Setting this bit will cause the Intel PCH to generate an SMI# when the GPIO_UNLOCK_SMI_STS bit is set in the SMI_STS register. Once written to '1', this bit can only be cleared by PLTRST# assertion.
26:18	0h RO	Reserved.
17	0h RW	**Legacy USB 2 Enable (LEGACY_USB2_EN):** Enables legacy USB2 logic to cause SMI#.
16:15	0h RO	Reserved.
14	0h RW	**Periodic Enable (PERIODIC_EN):** Setting this bit will cause the Intel PCH to generate an SMI# when the PERIODIC_STS bit is set in the SMI_STS register. This bit is reset by PLTRST# assertion.
13	0h RW/L	**TCO Enable (TCO_EN):** 1 = Enables the TCO logic to generate SMI#. 0 = Disables TCO logic from generating an SMI#. If the NMI2SMI_EN bit is set, then SMI's that are caused by NMI's (i.e. rerouted) will not be gated by the TCO_EN bit. Even if the TCO_EN bit is 0, the NMI's will still be routed to cause the SMI#. NOTE: This bit can not be written once the TCO_LOCK bit (at offset 08h of TCO I/O Space) is set. This prevents unauthorized software from disabling the generation of TCO-based SMI's. This bit is reset by PLTRST# assertion.
12	0h RO	Reserved.
11	0h RW	**Microcontroller SMI Enable (MCSMI_EN):** Software sets this bit to 1 to enables Intel PCH to trap access to the microcontroller range (62h or 66h). A 'trapped' cycles will be claimed by Intel PCH, but not forwarded to eSPI. An SMI# will also be generated. This bit is reset by PLTRST# assertion.
10:8	0h RO	Reserved.
7	0h WO	**BIOS Release (BIOS_RLS):** Enables the generation of an SCI interrupt for ACPI software when a '1' is written to this bit position by BIOS software. This bit always reads a '0'. NOTE: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place. This bit is reset by PLTRST# assertion.
6	0h RW	**Software SMI Timer Enable (SWSMI_TMR_EN):** Software sets this bit to a '1' to start the Software SMI# Timer. When the timer expires (depending on the SWSMI_RATE_SEL bits), it will generate an SMI# and set the SWSMI_TMR_STS bit. The SWSMI_TMR_EN bit will remain at 1 until software sets it back to 0. Clearing the SWSMI_TMR_EN bit before the timer expires will reset the timer and the SMI# will not be generated. The default for this bit is 0. This bit is reset by PLTRST# assertion.
5	0h RW	**APMC Enable (APMC_EN):** If set, this enables writes to the APM_CNT register to cause an SMI#. This bit is reset by PLTRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**SMI On Sleep Enable (SMI_ON_SLP_EN):** If this bit is set, the Intel PCH will generate an SMI# when a write access attempts to set the SLP_EN bit (in the PM1_CNT register). Furthermore, the Intel PCH will not put the system to a sleep state. It is expected that the SMI# handler will turn off the SMI_ON_SLP_EN bit before actually setting the SLP_EN bit. This bit is reset by PLTRST# assertion.
3	0h RW	**Legacy USB Enable (LEGACY_USB_EN):** Enables legacy USB circuit to cause SMI#. This bit is reset by PLTRST# assertion.
2	0h RW	**BIOS Enable (BIOS_EN):** Enables the generation of SMI# when ACPI software writes a 1 to the GBL_RLS bit. Note that if the BIOS_STS bit, which gets set when software writes a 1 to GBL_RLS bit, is already a 1 at the time that BIOS_EN becomes 1, an SMI# will be generated when BIOS_EN gets set. This bit is reset by PLTRST# assertion.
1	1h RW/1S/V	**End of SMI (EOS):** This bit controls the arbitration of the SMI signal to the processor. This bit must be set in order for Intel PCH to assert SMI# low to the processor after SMI# has been asserted previously. Once Intel ICH asserts SMI# low, the EOS bit is automatically cleared. In the SMI handler, the CPU should clear all pending SMIs (by servicing them and then clearing their respective status bits), set the EOS bit, and exit SMM. This will allow the SMI arbiter to reassert SMI upon detection of an SMI event and the setting of a SMI status bit. The SMI# signal will go inactive for 4 PCI clocks. This bit is reset by PLTRST# assertion.
0	0h RW/L	**Global SMI Enable (GBL_SMI_EN):** 0 = No SMI# will be generated by PCH. 1 = Enables the generation of SMI# in the system upon any enabled SMI event. NOTE: When the SMI_LOCK bit is set, this bit cannot be changed. This bit is reset by PLTRST# assertion.

4.2.6 SMI Status Register (SMI_STS)—Offset 34h

Lockable: No
Usage: ACPI or Legacy
Power Well: Primary
Note: If the corresponding _EN bit is set when the _STS bit is set, the Intel PCH will cause an SMI# (except bits 8-10, which don't cause SMI#)

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**xHCI SMI Status (xHCI_SMI_STS):** This bit will be set when any USB3 (xHCI) Host Controller is requesting an SMI.
30	0h RO/V	**Intel(R) CSME SMI Status (ME_SMI_STS):** This bit will be set when Intel(R)CSME is requesting an SMI#.
29	0h RO	Reserved.
28	0h RO/V	**eSPI SMI Status (ESPI_SMI_STS):** This bit is set if an eSPI agent is requesting an SMI#. This bit is set by hardware and cleared when the PCH receives an eSPI SMI deassertion from an eSPI device.

Bit Range	Default & Access	Field Name (ID): Description
27	0h RW/1C/V	**GPIO Unlock SMI Status (GPIO_UNLOCK_SMI_STS):** This bit will be set of the GPIO registers lockdown logic is requesting an SMI#. Writing a '1' to this bit position clears this bit to '0'. This bit is reset by PLTRST# assertion.
26	0h RO/V	**SPI_SMI Status (SPI_SMI_STS):** This bit will be set when the SPI logic is requesting an SMI#. This bit is read only because the sticky status and enable bits associated with this function are located in the SPI registers.
25:22	0h RO	Reserved.
21	0h RO/V	**Monitor Status (MONITOR_STS):** This bit will be set if the Trap/SMI logic has caused the SMI. This will occur when the CPU or a bus master accesses an assigned register (or a sequence of accesses).
20	0h RO/V	**PCI_EXP_SMI Status (PCI_EXP_SMI_STS):** 1- PCI Express SMI event occurred. This could be due to a PCI Express PME event or Hot Plug Event.
19:17	0h RO	Reserved.
16	0h RW/1C/V	**SMBUS_SMI Status (SMBUS_SMI_STS):** 0 = This bit is set from the 64 KHz clock domain used by the SMBus. Software must wait at least 15.63 microseconds after initial assertion of this bit before clearing it. This bit is sticky and is cleared by writing a 1 to this bit position. 1 = Indicates that the SMI# was caused by: 1.The SMBus Slave receiving a message that an SMI# should be caused, or 2. The SMBALERT# signal goes active and the SMB_SMI_EN bit is set and the SMBALERT_DIS bit is cleared, or 3. The SMBus Slave receiving a HOST_NOTIFY message and the HOST_NOTIFY_INTREN and the SMB_SMI_EN bits are set, or 4. The SMBus Slave receiving a “SMI in S0“msage. This bit is reset by PLTRST# assertion.
15	0h RO/V	**SERIRQ_SMI Status (SERIRQ_SMI_STS):** 1 = Indicates the SMI# was caused by the SERIRQ decoder. 0 = SMI# not caused by SERIRQ decoder. NOTE: this bit is not sticky. Writes to this bit will have no effect.
14	0h RW/1C/V	**Periodic Status (PERIODIC_STS):** This bit will be set at the rate determined by the PER_SMI_SEL bits. If the PERIODIC_EN bit is also set, the Intel PCH will generate an SMI#. This bit is cleared by writing a 1 to this bit position. This bit is reset by PLTRST# assertion.
13	0h RW/1C/V	**TCO Status (TCO_STS):** 0 = SMI not caused by TCO logic. 1 = Indicates SMI was caused by the TCO logic. NOTE: Will not cause wake event. This bit is cleared by writing a 1 to this bit position. This bit is reset by PLTRST# assertion.
12	0h RO/V	**DEVMON Status (DEVMON_STS):** This read-only bit is set when bit 0 in the DEVTRAP_STS register is set. It is not sticky, so writes to this bit will have no effect.
11	0h RW/1C/V	**MCSMI Status (MCSMI_STS):** This bit is set if there is an access to the power management microcontroller range (62h or 66h). If this bit is set, and the MCSMI_EN bit is also set, the Intel PCH will generate an SMI#. This bit is set by hardware and cleared by software writing a 1 to its bit position. This bit is reset by PLTRST# assertion.
10	0h RO/V	**GPIO SMI Status (GPIO_SMI_STS):** This bit will be a 1 if any GPIO that is enabled to trigger SMI is asserted. GPIOs that are not routed to cause an SMI will have no effect on this bit. This bit is NOT sticky. Writes to this bit will have no effect. Note: See the GPIO chapter for the individual GPIO SMI status, enable, and routing bit definitions.
9	0h RO/V	**GPE0 Status (GPE0_STS):** There are several status/enable bit pairs in GPE0_STS/EN_127_96 that are capable of triggering SMI#s. This bit is a logical OR of all of those pairs (i.e. this bit is asserted whenever at least one of those pairs has both the status and enable bit asserted). This bit is NOT sticky. Writes to this bit will have no effect. Note: The setting of this bit does not cause the SMI#. The following bit pairs are included in this logical OR: - GPE0_STS/EN_127_96 [18, 17, 16, 13, 11, 10, 8, 2]
8	0h RO/V	**PM1 Status Register (PM1_STS_REG):** This is an OR of the bits (except for bits 5 and 4) in the ACPI PM1 Status Reg. Not sticky. Writes to this bit have no effect. Note: The setting of this bit does not cause the SMI#.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6	0h RW/1C/V	**Software SMI Timer Status (SWSMI_TMR_STS):** This bit will be set to 1 by the hardware when the Software SMI# Timer expires. This bit will remain 1 until the software writes a 1 to this bit. This bit is reset by PLTRST# assertion.
5	0h RW/1C/V	**APM Status (APM_STS):** SMI# was generated by a write access to the APM control register and if the APMC_EN bit is set. This bit is cleared by writing a one to its bit position. This bit is reset by PLTRST# assertion.
4	0h RW/1C/V	**SMI_ON_SLP_EN Status (SMI_ON_SLP_EN_STS):** This bit will be set by the Intel PCH when a write access attempts to set the SLP_EN bit. This bit is cleared by writing a 1 to this bit position. This bit is reset by PLTRST# assertion.
3	0h RO/V	**Legacy USB Status (LEGACY_USB_STS):** This non-sticky read-only bit is a logical OR of each of the SMI status bits in the USB Legacy Keybd Register ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect.
2	0h RW/1C/V	**BIOS Status (BIOS_STS):** This bit gets set by hardware when a 1 is written by software to the GBL_RLS bit. When both BIOS_EN and the BIOS_STS bit are set, an SMI# will be generated. The BIOS_STS bit is cleared when software writes a 1 to this bit position. This bit is reset by PLTRST# assertion.
1:0	0h RO	Reserved.

4.2.7 General Purpose Event Control (GPE_CTRL)—Offset 40h

Lockable: No
Usage: ACPI or Legacy
Power Well: Primary

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW/V	**Software GPE Control (SWGPE_CTRL):** This bit allows software to control the assertion of SWGPE_STS bit. This bit is used by hardware as the level input signal for the SWGPE_STS bit in the GPE0_STS register. When SWGPE_CTRL is 1, SWGPE_STS will be set to 1, and writes to SWGPE_STS with a value of 1 to clear SWGPE_STS will result in SWGPE_STS being set back to 1 by hardware. When SWGPE_CTRL is 0, writes to SWGPE_STS with a value of 1 will clear SWGPE_STS to 0. This bit is reset by RSMRST# assertion.
16:0	0h RO	Reserved.

4.2.8 PM2a Control Block (PM2A_CNT_BLK)—Offset 50h

Lockable: No Usage
Usage: ACPI or Legacy
Power Well: Primary
Note: BIOS must describe this register as 1 byte wide to the OS

Access Method

Type: IO Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**Arbiter Disable (ARB_DIS):** This bit is a scratchpad bit for legacy software compatibility. This bit is reset by PLTRST# assertion.

4.2.9 Over-Clocking WDT Control (OC_WDT_CTL)—Offset 54h

This register controls the operation of the PCH Over-Clocking Watchdog Timer.

Access Method

Type: IO Register (Size: 32 bits)
Device:
Function:

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h WO	**Over-Clocking WDT Reload (OC_WDT_RLD):** Software can write a '1' to this bit to reload ("ping") the PCH over-clocking watchdog timer while it is running. A write of '0' to this bit has no effect. A write of '1' to this bit while OC_WDT_EN=0, or with the clearing of OC_WDT_EN, does not start or reload the WDT (i.e. OC_WDT_EN takes precedence). The value in OC_WDT_TOV may be changed by software along with its setting of this bit. On a WDT reload, the current (potentially new) value in OC_WDT_TOV is loaded into the WDT as the new timeout value.
30:26	0h RO	Reserved.
25	0h RW/1C/V	**Over-Clocking WDT ICC Survivability Mode Timeout Status (OC_WDT_ICCSURV_STS):** This bit is set to '1' if the over-clocking WDT has timed out and triggered a global reset while running in a mode that has ICC survivability impact (OC_WDT_ICCSURV=1). It is cleared by a software write of '1' or by RSMRST# assertion.
24	0h RW/1C/V	**Over-Clocking WDT Non-ICC Survivability Mode Timeout Status (OC_WDT_NO_ICCSURV_STS):** This bit is set to '1' if the over-clocking WDT has timed out and triggered a global reset while running in a mode that does not have ICC survivability impact (OC_WDT_ICCSURV=0). It is cleared by a software write of '1' or by RSMRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0h RW	**Over-Clocking WDT Scratchpad (OC_WDT_SCRATCH):** This field is available as scratchpad space for software and has no effect on PCH HW operation. This bit is reset by RSMRST# assertion.
15	0h RW/L	**Over-Clocking WDT Force All (OC_WDT_FORCE_ALL):** GATE_BIT:OC_WDT_CTL.OC_WDT_CTL_LCK.HIGH When this bit is set to '1' and the OC_WDT is running, any included global reset source will behave as though the OC_WDT expired. This bit is reset by RSMRST# assertion or CF9 reset.
14	0h RW/V/L	**Over-Clocking WDT Enable (OC_WDT_EN):** Software sets this bit to '1' to enable the PCH over-clocking watchdog timer. While the counter is running, if it expires before being reloaded by software via the OC_WDT_RLD bit or halted by software clearing this bit, then one of the status bits will be set (which one depends on the WDT operating mode at the time - see the OC_WDT_ICCSURV bit description), and a global reset will be triggered. This bit is also set by the hardware when conditions allow the OC_WDT to self-start at power cycle reboot (effectively changes the default of this bit as seen by software).
13	1h RW/L	**Over-Clocking WDT ICC Survivability Impact (OC_WDT_ICCSURV):** This bit determines whether OC_WDT expiration will have an impact on ICC (Integrated Clock Controller) bootstrap survivability. OC_WDT_ICCSURV=1 (default) An OC_WDT timeout while operating in this mode causes certain ICC hardware auto-recovery actions to take place. A timeout in this mode will set OC_WDT_ICCSURV_STS.OC_WDT_ICCSURV=0 Software should configure the OC_WDT to this mode if no ICC hardware auto-recovery actions are desired in the event of a timeout. A timeout in this mode will set OC_WDT_NO_ICCSURV_STS
12	0h RW/L	**OC_WDT_CTL Register Lock (OC_WDT_CTL_LCK):** This bit controls write-ability to this register. Encodings: 0: All fields of register OC_WDT_CTL operate as normal and can be updated by software. Reads to the register operate as normal. 1: All RW/L fields of register OC_WDT_CTL, including this lock control bit, are locked. Writes to these register fields have no effect and the register fields retain their current states. Reads to the register operate as normal. Once this bit is set, it can only be cleared by Primary well power loss (via RSMRST# assertion).
11:10	0h RO	Reserved.
9:0	0h RW/V/L	**Over-Clocking WDT Timeout Value (OC_WDT_TOV):** Software programs the desired over-clocking WDT timeout value into this register. This timer is zero-based and has a granularity of 1 second. Example timeout values: 000h: 1 second 001h: 2 seconds ... 3FFh: ~17 minutes (1024 seconds) The value of OC_WDT_TOV may be changed by software along with its setting of the OC_WDT_RLD bit. On a WDT reload, the current (potentially new) value in OC_WDT_TOV is loaded into the WDT as the new timeout value. This field is also updated by the hardware when conditions allow the OC_WDT to self-start at power cycle reboot (effectively changes the default of this field as seen by software).

4.2.10 General Purpose Event 0 Status [31:0] (GPE0_STS_31_0)—Offset 60h

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/1C/V	**General Purpose Event 0 Status [31:0] (GPE0_STS_31_0):** These bits are set any time the corresponding GPIO is setup as an input and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPE0_EN_31_0 register, then when the GPE0_STS_31_0 bit is set: - If system is in an S3-S5 state, the event will also wake the system. - If system is in an S0 state (or upon waking back to S0), an SCI will be caused, depending on the GPIROUTSCI bit for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position. Note: The GPP/GPD group mapped to this GPE0_STS_31_0 is configured via GPIO_CFG.DW0 and MISCCFG.DW0. Both GPIO_CFG.DW0 and MISCCFG.DW0 must be programmed to the same GPIO group.

4.2.11 General Purpose Event 0 Status [63:32] (GPE0_STS_63_32)—Offset 64h

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/1C/V	**General Purpose Event 0 Status [63:32] (GPE0_STS_63_32):** These bits are set any time the corresponding GPIO is setup as an input and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPE0_EN_63_32 register, then when the GPE0_STS_63_32 bit is set: - If system is in an S3-S5 state, the event will also wake the system. - If system is in an S0 state (or upon waking back to S0), an SCI will be caused, depending on the GPIROUTSCI bit for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position. Note: The GPP/GPD group mapped to this GPE0_STS_63_32 is configured via GPIO_CFG.DW1 and MISCCFG.DW1. Both GPIO_CFG.DW1 and MISCCFG.DW1 must be programmed to the same GPIO group.

4.2.12 General Purpose Event 0 Status [95:64] (GPE0_STS_95_64)—Offset 68h

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/1C/V	**General Purpose Event 0 Status [95:64] (GPE0_STS_95_64):** These bits are set any time the corresponding GPIO is setup as an input and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPE0_EN_95_64 register, then when the GPE0_STS_95_64 bit is set: - If system is in an S3-S5 state, the event will also wake the system. - If system is in an S0 state (or upon waking back to S0), an SCI will be caused, depending on the GPIROUTSCI bit for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position. Note: The GPP/GPD group mapped to this GPE0_STS_95_64 is configured via GPIO_CFG.DW2 and MISCCFG.DW2. Both GPIO_CFG.DW2 and MISCCFG.DW2 must be programmed to the same GPIO group.

4.2.13 General Purpose Event 0 Status [127:96] (GPE0_STS[127:96])—Offset 6Ch

Note: This register is symmetrical to the General Purpose Event 0 Enable [127:96] Register. Unless indicated otherwise below, if the corresponding _EN bit is set, then when the STS bit get set, the Intel PCH will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the Intel PCH will also generate an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit is not set and GBL_SMI_EN is set.
Note that GPE0_STS bits 95:0 are claimed by the GPIO register block.

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW/1C/V	**Wake Alarm Device Timer Status (WADT_STS):** This bit is set whenever the any of the wake alarm device timers signal a timer expiration. This bit is reset by RSMRST# assertion.
17:16	0h RO	Reserved.
15	0h RW/1C/V	**GPIO Tier2 SCI Status (GPIO_TIER2_SCI_STS):** This bit is a logical OR of sci_wake from tier 2 GPIO's.
14	0h RW/1C/V	**eSPI SCI Status (ESPI_SCI_STS):** This bit will be set when an agent attached to eSPI is requesting an SCI. Note: This source is not able to cause a wake event. This bit is reset by RSMRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW/1C/V	**Power Management Event Bus 0 Status (PME_B0_STS):** This bit will be set to 1 by the Intel PCH when any internal device with PCI Power Management capabilities on bus 0 asserts the equivalent of the PME# signal. Additionally, if the PME_B0_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the PME_B0_STS bit will generate an SCI (or SMI# if SCI_EN is not set). If the PME_B0_EN bit is set, and the system is in an S3-S4 state (or S5 state due to SLP_TYP and SLP_EN), then the setting of the PME_B0_STS bit will generate a wake event. If the system is in an S5 state due to power button override, then the PME_B0_STS bit will not cause a wake event or SCI. This bit is cleared by a software write of '1'. Internal devices which can set this bit: - Integrated LAN - HD Audio/Audio DSP - SATA - xHCI - CNVi - Intel (R)CSME Maskable Host Wake This bit is reset by RSMRST# assertion.
12	0h RW/1C/V	**Intel(R)CSME SCI Status (ME_SCI_STS):** This bit will be set when Intel(R)CSME is requesting an SCI. Software must clear the Intel(R)CSME source of the SCI before clearing this bit. Note: This source is not able to cause a wake event. This bit is reset by RSMRST# assertion.
11	0h RW/1C/V	**Power Management Event Status (PME_STS):** This bit will be set to 1 by hardware when the PME# signal goes active. Additionally, if the PME_EN and SCI_EN bits are set, and system is in an S0 state, then the setting of the PME_STS bit will generate an SCI (or SMI# if SCI_EN is not set). If the PME_EN bit is set, and the system is in an S3-S4 state (or S5 state due to SLP_TYP and SLP_EN), then the setting of the PME_STS bit will generate a wake event. If the system is in an S5 state due to power button override, then PME_STS will not cause a wake event or SCI. This bit is cleared by writing a 1 to this bit position or RSMRST# assertion.
10	0h RW/1C/V	**Battery Low Status (BATLOW_STS):** In Mobile Mode this bit will be set to 1 by hardware when the BATLOW# signal goes low. Software clears the bit by writing a 1 to the bit position. In Desktop Mode, this bit will be treated as Reserved. This bit is reset by RSMRST# assertion.
9	0h RW/1C/V	**PCI Express Status (PCI_EXP_STS):** This bit will be set to 1 by hardware to indicate that: - The PME event message was received on one or more of the PCI-Express Ports - An Assert PMEGPE message received from the MCH via DMI Note: The PCI WAKE# pin and the PCI-Express Beacons have no impact on this bit. Software attempts to clear this bit by writing a 1 to this bit position. If the PCI_EXP_STS bit went active due to an Assert PMEGPE message, then a Deassert PMEGPE message must be received prior to the software write in order for the bit to be cleared. If the bit is not cleared and the corresponding PCI_EXP_EN bit is set, the leveltriggered SCI will remain active. Note that a race condition exists where the PCI Express device sends another PME message because the PCI Express device was not serviced within the time when it must resend the message. This may result in a spurious interrupt, and this is comprehended and approved by the PCI Express specification. The window for this race condition is approximately 95-105 milliseconds. This bit is reset by RSMRST# assertion.
8	0h RO	Reserved.
7	0h RW/1C/V	**SMBus Wake Status (SMB_WAK_STS):** This bit is set to 1 by the hardware to indicate that the wake event was caused by the PCH's SMBus logic. This could be due to either the SM Bus slave unit receiving a message or the SMBALERT# signal going active. NOTES: 1. The SMBus controller will independently cause an SMI# so this bit does not need to do so (unlike the other bits in this register). 2. This bit is set by the SMBus slave command 01h (Wake/SMI#) even when the system is in the S0 state. Therefore, to avoid an instant wake on subsequent transitions to sleep states, software must clear this bit after each reception of the Wake/SMI# command or just prior to entering the sleep state. 3. The SMBALERT_STS bit (D31:F3:I/O Offset 00h:bit 5) should be cleared by software before clearing this bit. This bit is reset by RSMRST# assertion.
6	0h RW/1C/V	**TCOSCI Status (TCOSCI_STS):** This bit will be set to 1 by hardware when the TCO logic or Thermal Sensor logic causes an SCI. This bit can be reset by writing a one to this bit position or by RSMRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	Reserved.
4	0h RW/1C/V	**Thermal SCI Status (THERM_SCI_STS):** This bit will be set to 1 by hardware when the firmware sets the DRV_THERM_SMI_SCI_STS.DRV_SCI_STS. This bit can be cleared by writing a one to this bit position.
3	0h RO	Reserved.
2	0h RW/1C/V	**Software GPE Status (SWGPE_STS):** The SWGPE_CTRL bit(bit 1 of GPE_CTRL reg) acts as a level input to this bit. This bit is reset by RSMRST# assertion.
1	0h RW/1C/V	**Hot Plug Status (HOT_PLUG_STS):** Enables PCH to cause an SCI when the HOT_PLUG_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to hot-plug events. The following events cause HOT_PLUG_STS bit to set - Assert GPE message received from any of the PCIE ports in PCH - Assert HPGPE message received from any of the PCIE ports in PCH - Assert GPE message received downstream from processor - Assert HPGPE message received downstream from processor. This bit is reset by RSMRST# assertion.
0	0h RO	Reserved.

4.2.14 General Purpose Event 0 Enable [31:0] (GPE0_EN_31_0)—Offset 70h

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Event 0 Enable [31:0] (GPE0_EN_31_0):** These bits enable the corresponding GPE0_STS[31:0] bits being set to cause an SCI and/or wake event. Note: The GPP/GPD group mapped to this GPE0_EN_31_0 is configured via GPIO_CFG.DW0 and MISCCFG.DW0. Both GPIO_CFG.DW0 and MISCCFG.DW0 must be programmed to the same value.

4.2.15 General Purpose Event 0 Enable [63:32] (GPE0_EN_63_32)—Offset 74h

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Event 0 Enable [63:32] (GPE0_EN_63_32):** These bits enable the corresponding GPE0_STS[63:32] bits being set to cause an SCI and/or wake event. Note: The GPP/GPD group mapped to this GPE0_EN_63_32 is configured via GPIO_CFG.DW1 and MISCCFG.DW1. Both GPIO_CFG.DW1 and MISCCFG.DW1 must be programmed to the same value.

4.2.16 General Purpose Event 0 Enable [95:64] (GPE0_EN_95_64)—Offset 78h

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Event 0 Enable [95:64] (GPE0_EN_95_64):** These bits enable the corresponding GPE0_STS[95:64] bits being set to cause an SCI and/or wake event. Note: The GPP/GPD group mapped to this GPE0_EN_95_64 is configured via GPIO_CFG.DW2 and MISCCFG.DW2. Both GPIO_CFG.DW2 and MISCCFG.DW2 must be programmed to the same value.

4.2.17 General Purpose Event 0 Enable [127:96] (GPE0_EN[127:96])—Offset 7Ch

Note: This register is symmetrical to the General Purpose Event 0 Status [127:96] Register.
Note that GPE0_STS bits 95:0 are claimed by the GPIO register block.

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW	**Wake Alarm Device Timer Enable (WADT_EN):** Used to enable the setting of the WADT_STS bit to generate Wake/SMI#/SCI. This bit is reset by DSW_PWROK de-assertion.
17	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**LAN WAKE Enable (LAN_WAKE_EN):** Used to enable the setting of the LANWAKE_STS bit to generate wake/SMI#/SCI. Host wake events from the PHY through LANWAKE cannot be disabled by clearing this bit. Note that GPIO[27] is a valid host wake event from Deep-Sx. But the wake enable configuration must persist even after a G3. So this bit is in the RTC well.
15	0h RW/V	**GPIO Tier2 SCI EN (GPIO_TIER2_SCI_EN):** Used to enable the setting of GPIO_TIER2_SCI_STS to generate wake/SCI#.
14	0h RW/V	**eSPI SCI Enable (ESPI_SCI_EN):** Used to enable the setting of the ESPI_SCI_STS bit to generate a SCI.
13	0h RW/V	**PME_B0 Enable (PME_B0_EN):** Enables the setting of the PME_B0_STS bit to generate a wake event and/or an SCI or SMI#. This bit is reset by RTCRST# assertion.
12	0h RW/V	**Intel (R) CSME SCI Enable (ME_SCI_EN):** Used to enable the setting of the ME_SCI_STS bit to generate a SCI.
11	0h RW/V	**Power Management Event Enable (PME_EN):** Enables the setting of the PME_STS to generate a wake event and/or an SCI. This bit is reset by RTCRST# assertion.
10	0h RW/V	**Low Battery Enable (BATLOW_EN):** In Mobile Mode, this bit enables the BATLOW# signal to cause an SMI# or SCI (depending on the SCI_EN bit) when it goes low.This bit does not prevent the BATLOW# signal from inhibiting the wake event. In Desktop Mode this bit will be treated as Reserved. This bit is reset by RTCRST# assertion.
9	0h RW/V	**PCI Express Enable (PCI_EXP_EN):** Enables PCH to cause an SCI when PCI_EXP_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to wake/PME events.
8:7	0h RO	Reserved.
6	0h RW/V	**TCOSCI Enable (TCOSCI_EN):** When TCOSCI_EN and TCOSCI_STS are both set, an SCI will be generated. This bit is reset by RSMRST# assetion.
5	0h RO	Reserved.
4	0h RW	**Thermal SCI Enable (THERM_EN):** When THERM_EN and THERM_SCI_STS are both set, an SCI will be generated.
3	0h RO	Reserved.
2	0h RW/V	**Software GPE Enable (SWGPE_EN):** This bit, when set to 1, enables the SW GPE function. If SWGPE_CTRL is written to a 1, hardware will set SWGPE_STS (acts as a level input) If SWGPE_STS, SWGPE_EN, and SCI_EN are all 1's, an SCI will be generated If SWGPE_STS = 1, SWGPE_EN = 1, SCI_EN = 0, and GBL_SMI_EN = 1 then an SMI# will be generated
1	0h RW/V	**Hot Plug Enable (HOT_PLUG_EN):** Enables PCH to cause an SCI when the HOT_PLUG_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to hot-plug events. The following events cause HOT_PLUG_STS bit to set - Assert GPE message received from any of the PCIE ports in PCH - Assert HPGPE message received from any of the PCIE ports in PCH - Assert GPE message received downstream from MCH - Assert HPGPE message received downstream from MCH
0	0h RO	Reserved.

4.3 PMC Memory Mapped Registers Summary

The PMC memory mapped registers are accessed based upon offsets from PM Base Address (PWRMBASE) defined in PCI Device 31: Function 2.

Table 4-3. Summary of PMC Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1020h	1023h	General PM Configuration A (GEN_PMCON_A)—Offset 1020h	20014000h
1024h	1027h	General PM Configuration B (GEN_PMCON_B)—Offset 1024h	4h
1030h	1033h	Configured Revision ID (CRID)—Offset 1030h	0h
1048h	104Bh	Extended Test Mode Register 3 (ETR3)—Offset 1048h	0h
104Ch	104Fh	SET STRAP MSG LOCK (SSML)—Offset 104Ch	0h
1050h	1053h	SET STRAP MSG CONTROL (SSMC)—Offset 1050h	0h
1054h	1057h	SET STRAP MSG DATA (SSMD)—Offset 1054h	0h
10B0h	10B3h	Configured Revision ID (CRID_UIP)—Offset 10B0h	0h
10C0h	10C3h	HSIO Power Management Configuration 1 (MODPHY_PM_CFG1)—Offset 10C0h	0h
10C4h	10C7h	HSIO Power Management Configuration 2 (MODPHY_PM_CFG2)—Offset 10C4h	FFFh
10C8h	10CBh	HSIO Power Management Configuration 3 (MODPHY_PM_CFG3)—Offset 10C8h	5000000h
10CCh	10CFh	HSIO Power Management Configuration 4 (MODPHY_PM_CFG4)—Offset 10CCh	0h
10D0h	10D3h	HSIO Power Management Configuration 5 (MODPHY_PM_CFG5)—Offset 10D0h	0h
10D4h	10D7h	HSIO Power Management Configuration 6 (MODPHY_PM_CFG6)—Offset 10D4h	0h
11B8h	11BBh	External Rail Config (EXT_RAIL_CONFIG)—Offset 11B8h	0h
11C0h	11C3h	External Rail Config (EXT_V1P05_VR_CONFIG)—Offset 11C0h	0h
11C4h	11C7h	External Rail Config (EXT_VNN_VR_CONFIG0)—Offset 11C4h	0h
11C8h	11CBh	VNN V1p05 Control Hold Off (VNN_V1P05_CTRL_HOLD_OFF)—Offset 11C8h	101h
11CCh	11CFh	EXT FET RAMP CFG (EXT_FET_RAMP_CFG)—Offset 11CCh	40004h
11D0h	11D3h	VCCIN AUX CONFIG Register1 (VCCIN_AUX_CFG1)—Offset 11D0h	0h
11D4h	11D7h	VCCIN AUX CONFIG Register2 (VCCIN_AUX_CFG2)—Offset 11D4h	0h
1200h	1203h	Always Running Timer Value 31:0 (ARTV_31_0)—Offset 1200h	0h
1204h	1207h	Always Running Timer Value 31:0 (ARTV_63_32)—Offset 1204h	0h
1210h	1213h	Timed GPIO Control 0 (TGPIOCTL0)—Offset 1210h	0h
1220h	1223h	Timed GPIO 0 Comparator Value 31:0 (TGPIOCOMPV0_31_0)—Offset 1220h	0h
1224h	1227h	Timed GPIO Comparator Value 63:32 (TGPIOCOMPV0_63_32)—Offset 1224h	0h
1228h	122Bh	Timed GPIO0 Periodic Interval Value 31_0 (TGPIOPIV0_31_0)—Offset 1228h	0h
122Ch	122Fh	Timed GPIO 0 Periodic Interval Value 63_32 (TGPIOPIV0_63_32)—Offset 122Ch	0h
1230h	1233h	Timed GPIO Time Capture Register 31_0 (TGPIOTCV0_31_0)—Offset 1230h	0h
1234h	1237h	Timed GPIO0 Time Capture Register 63_32 (TGPIOTCV0_63_32)—Offset 1234h	0h
1238h	123Bh	Timed GPIO0 Event Counter Capture Register 31_0 (TGPIOECCV0_31_0)—Offset 1238h	0h

Table 4-3. Summary of PMC Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
123Ch	123Fh	Timed GPIO0 Event Counter Capture Register 63_32 (TGPIOECCV0_63_32)—Offset 123Ch	0h
1240h	1243h	Timed GPIO0 Event Counter Register 31_0 (TGPIOEC0_31_0)—Offset 1240h	0h
1244h	1247h	Timed GPIO0 Event Counter Register 63_32 (TGPIOEC0_63_32)—Offset 1244h	0h
1310h	1313h	Timed GPIO Control 1 (TGPIOCTL1)—Offset 1310h	0h
1320h	1323h	Timed GPIO 1 Comparator Value 31:0 (TGPIOCOMPV1_31_0)—Offset 1320h	0h
1324h	1327h	Timed GPIO Comparator Value 63:32 (TGPIOCOMPV1_63_32)—Offset 1324h	0h
1328h	132Bh	Timed GPIO1 Periodic Interval Value 31_0 (TGPIOPIV1_31_0)—Offset 1328h	0h
132Ch	132Fh	Timed GPIO 1 Periodic Interval Value 63_32 (TGPIOPIV1_63_32)—Offset 132Ch	0h
1330h	1333h	Timed GPIO Time Capture Register 31_0 (TGPIOTCV1_31_0)—Offset 1330h	0h
1334h	1337h	Timed GPIO Time Capture Register 63_32 (TGPIOTCV1_63_32)—Offset 1334h	0h
1338h	133Bh	Timed GPIO0 Event Counter Capture Register 31_0 (TGPIOECCV1_31_0)—Offset 1338h	0h
133Ch	133Fh	Timed GPIO0 Event Counter Capture Register 63_32 (TGPIOECCV1_63_32)—Offset 133Ch	0h
1340h	1343h	Timed GPIO1 Event Counter Register 31_0 (TGPIOEC1_31_0)—Offset 1340h	0h
1344h	1347h	Timed GPIO Event Counter Register 63_32 (TGPIOEC1_63_32)—Offset 1344h	0h
150Ch	150Fh	Catastrophic Trip Point Enable (CTEN)—Offset 150Ch	1h
1510h	1513h	EC Thermal Sensor Reporting Enable (ECRPTEN)—Offset 1510h	0h
1520h	1523h	Throttle Level (TL)—Offset 1520h	FF3FCFFh
1528h	152Bh	Throttle Levels Enable (TLEN)—Offset 1528h	0h
1530h	1533h	Thermal Sensor Alert High Value (TSAHV)—Offset 1530h	FFh
1534h	1537h	Thermal Sensor Alert Low Value (TSALV)—Offset 1534h	0h
1538h	153Bh	Thermal Alert Trip Status (TAS)—Offset 1538h	0h
1540h	1543h	PCH Hot Level Control (PHLC)—Offset 1540h	0h
1560h	1563h	Temperature Sensor Control and Status (TSS0)—Offset 1560h	0h
1800h	1803h	Wake Alarm Device Timer: AC (WADT_AC)—Offset 1800h	FFFFFFFFh
1804h	1807h	Wake Alarm Device Timer: DC (WADT_DC)—Offset 1804h	FFFFFFFFh
1808h	180Bh	Wake Alarm Device Expired Timer: AC (WADT_EXP_AC)—Offset 1808h	FFFFFFFFh
180Ch	180Fh	Wake Alarm Device Expired Timer: DC (WADT_EXP_DC)—Offset 180Ch	FFFFFFFFh
1810h	1813h	Power and Reset Status (PRSTS)—Offset 1810h	0h
1818h	181Bh	Power Management Configuration Reg 1 (PM_CFG)—Offset 1818h	20h
1828h	182Bh	S3 Power Gating Policies (S3_PWRGATE_POL)—Offset 1828h	0h
182Ch	182Fh	S4 Power Gating Policies (S4_PWRGATE_POL)—Offset 182Ch	0h
1830h	1833h	S5 Power Gating Policies (S5_PWRGATE_POL)—Offset 1830h	0h

Table 4-3. Summary of PMC Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1834h	1837h	DeepSx Configuration (DSX_CFG)—Offset 1834h	0h
183Ch	183Fh	Power Management Configuration Reg 2 (PM_CFG2)—Offset 183Ch	0h
18C8h	18CBh	PM_SYNC Miscellaneous Configuration (PM_SYNC_MISC_CFG)—Offset 18C8h	0h
18E0h	18E3h	Chipset Initialization Register E0 (CIRE0)—Offset 18E0h	0h
18ECh	18EFh	CPU Early Power-on Configuration (CPU_EPOC)—Offset 18ECh	0h
18FCh	18FFh	ACPI Timer Control (ACPI_TMR_CTL)—Offset 18FCh	0h
1910h	1913h	Last TSC Alarm Value[31:0] (TSC_ALARM_LO)—Offset 1910h	0h
1914h	1917h	Last TSC Alarm Value[63:32] (TSC_ALARM_HI)—Offset 1914h	0h
1920h	1923h	GPIO Configuration (GPIO_CFG)—Offset 1920h	432h
1924h	1927h	Global Reset Causes (GBLRST_CAUSE0)—Offset 1924h	0h
1928h	192Bh	Global Reset Causes Register 1 (GBLRST_CAUSE1)—Offset 1928h	0h
192Ch	192Fh	Host Partition Reset Causes (HPR_CAUSE0)—Offset 192Ch	0h
1930h	1933h	LATENCY_LIMIT_RESIDENCY_0 (LAT_LIM_RES_0)—Offset 1930h	0h
1934h	1937h	LATENCY_LIMIT_RESIDENCY_1 (LAT_LIM_RES_1)—Offset 1934h	0h
1938h	193Bh	LATENCY_LIMIT_RESIDENCY_2 (LAT_LIM_RES_2)—Offset 1938h	0h
193Ch	193Fh	SLP S0 RESIDENCY (SLP_S0_RES)—Offset 193Ch	0h
1940h	1943h	Latency Limit Control (LLC)—Offset 1940h	0h
1B1Ch	1B1Fh	Chipset Initialization Register B1C (CPPMVRIC)—Offset 1B1Ch	0h
1B24h	1B27h	Chipset Initialization Register B24 (CIRB24)—Offset 1B24h	0h
1B40h	1B43h	Chipset Initialization Register 340 (CIRB40)—Offset 1B40h	0h
1B44h	1B47h	Chipset Initialization Register B44 (CIRB44)—Offset 1B44h	0h
1B4Ch	1B4Fh	Chipset Initialization Register 34C (CIR34C)—Offset 1B4Ch	2000000h
1BD4h	1BD7h	CWB MDID Status Register (CWBMDIDSTATUS)—Offset 1BD4h	0h
1BD8h	1BDBh	ACPI Control (ACTL)—Offset 1BD8h	0h
1D80h	1D83h	Power Gated ACK Status Register 0 (PPASR0)—Offset 1D80h	0h
1D84h	1D87h	Power Gated ACK Status Register 1 (PPASR1)—Offset 1D84h	0h
1D90h	1D93h	PFET Enable Ack Register 0 (PPFEAR0)—Offset 1D90h	0h
1D94h	1D97h	PFET Enable Ack Register 1 (PPFEAR1)—Offset 1D94h	0h
1DE0h	1DE3h	Chipset Initialization Register 5E0 (CIR5E0)—Offset 1DE0h	0h
1DE4h	1DE7h	Chipset Initialization Register 5E4 (CIR5E4)—Offset 1DE4h	0h
1E20h	1E23h	Static PG Function Disable 1 (ST_PG_FDIS1)—Offset 1E20h	0h
1E24h	1E27h	Static Function Disable Control 2 (ST_PG_FDIS2)—Offset 1E24h	0h
1E28h	1E2Bh	Chipset Initialization Register (NST_PG_FDIS_1)—Offset 1E28h	0h
1E40h	1E43h	PCIe Controller Disable Read (N_STPG_FUSE_SS_DIS_RD_1)—Offset 1E40h	0h
1E44h	1E47h	Capability Disable Read Register (STPG_FUSE_SS_DIS_RD_2)—Offset 1E44h	0h

4.3.1 General PM Configuration A (GEN_PMCON_A)—Offset 1020h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 20014000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	0h RW	**DC PHY Power Disable (DC_PP_DIS):** This bit determines the Host software contribution to whether the LAN PHY remains powered in Sx/MOFF or DeepSx while on battery.
29	1h RW	**Deep-Sx PHY Power Disable (DSX_PP_DIS):** This bit determines the Host software contribution to whether the LAN PHY remains powered in DeepSx. If this bit is cleared, for the PHY to be powered in deep-Sx state, SX_PP_EN must be set to 1.
28	0h RW	**After G3 PHY Power Enable (AG3_PP_EN):** This bit determines the Host software contribution to whether the LAN PHY is powered up after exiting G3 (to either Sx/MOFF or DeepSx).
27	0h RW	**Sx PHY Power Enable (SX_PP_EN):** This bit determines the Host software contribution to whether the LAN PHY remains powered in an Sx/MOFF state that was entered from S0 (rather than from G3).
26:25	0h RO	Reserved.
24	0h RW/1C/V	**Global Reset Status (GBL_RST_STS):** This bit is set after a global reset (not G3 or DeepSx) occurs. See the GEN_PMCON_B.HOST_RST_STS bit for potential usage models.
23	0h RW	**DRAM Initialization Scratchpad Bit (DISB):** This bit does not effect hardware functionality in any way. It is provided as a scratchpad bit that is maintained through main power well resets and CF9h-initiated resets. BIOS is expected to set this bit prior to starting the DRAM initialization sequence and to clear this bit after completing the DRAM initialization sequence. BIOS can detect that a DRAM initialization sequence was interrupted by a reset by reading this bit during the boot sequence. If the bit is 1, then the DRAM initialization was interrupted. This bit is reset by the assertion of the RSMRST# pin.
22	0h RO	Reserved.
21	0h RO/V	**Memory Placed in Self-Refresh (MEM_SR):** This bit will be set to 1 if DRAM should have remained powered and held in Self-Refresh through the last power state transition (i.e. the last time the system left S0). The scenarios where this should be the case are: - successful S3 entry & exit - successful Host partition reset without power cycle These scenarios both involve a handshake between the PCH and the CPU/MCH. The acknowledge from the CPU/MCH back to the PCH is assumed to imply that memory was successfully placed into Self-Refresh (the PCH has no way to verify whether that actually occurred). This bit will be cleared whenever the PCH begins a transition out of S0. Note: This bit should not be consulted upon wake from S1, as that state does not involve the same type of handshake or placing memory into Self-Refresh. It is assumed that software is already aware that memory context is not impacted by S1 and therefore does not need to check this bit.
20:19	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW/1C/V	**Minimum SLP_S4# Assertion Width Violation Status (MS4V):** Hardware sets this bit when the SLP_S4# assertion width is less than the time programmed in the SLP_S4# Minimum Assertion Width field (D31.F0.A4h.5:4). The PCH begins the timer when SLP_S4# pin (including Intel (R) CSME override logic) is asserted during S4/S5 entry, or when the RSMRST# input is deasserted during SUS well power-up. The status bit is cleared by software writing a 1 to the bit. Note that this bit is functional regardless of the value in the SLP_S4# Assertion Stretch Enable and the Disable SLP_X Stretching After SUS Power Failure bits. This bit is reset by the assertion of the RSMRST# pin, but can be set in some cases before the default value is readable.
17	0h RO	Reserved.
16	1h RW/1C	**SUS Well Power Failure (SUS_PWR_FLR):** This bit is set to '1' whenever SUS well power is lost, as indicated by RSMRST# assertion. Software writes a 1 to this bit to clear it.
15	0h RW	**PME B0 S5 Disable (PME_B0_S5_DIS):** When set to '1', this bit blocks wake events from PME_B0_STS in S5, regardless of the state of PME_B0_EN. When cleared (default), wake events from PME_B0_STS are allowed in S5 if PME_B0_EN = '1'. Wakes from power states other than S5 are not affected by this policy bit. The net effect of setting PME_B0_S5_DIS = '1' is described by the truth table below: Y = Wake N = Don't wake B0 = PME_B0_EN OV = WOL Enable Override B0/OV | S1/S3/S4 | S5 00 | N | N 01 | N | Y (LAN only) 11 | Y (all PME B0 sources) | Y (LAN only) 10 | Y (all PME B0 sources) | N This bit is cleared by the RTCRST# pin.
14	1h RW/1C	**PWR_FLR (PF):** 1 = Indicates that the trickle current (from the main battery or trickle supply) was removed or failed. 0 = Indicates that the trickle current has not failed since the last time the bit was cleared. Software writes a 1 to this bit to clear it. This bit is in the DSW well, and defaults to '1' based on DSW_PWROK deassertion (not cleared by any type of reset).
13	0h RO	Reserved.
12	0h RW/L	**Disable SLP_X Stretching After SUS Well Power Up (DIS_SLP_X_STRCH_SUS_UP):** When this bit is set to 1, all SLP_* pin stretching is disabled when powering up after a SUS well power loss. When this bit is left at 0, SLP_* stretching will be performed after SUS power failure as enabled in various other fields. Note that if this bit is a 0, SLP_* stretch timers start on SUS well power up (the PCH has no ability to count stretch time while the SUS well is powered down). Setting this bit can therefore prevent long delays after SUS power loss which may be common in mobile platforms and in manufacturing flow testing, while still allowing for the full power cycling during S3, S4 and S5 states. If the platform guarantees minimum SUS power down residence in other ways, an additional PCH-induced delay is not needed or wanted. Note: This policy bit has a different effect on SLP_SUS# stretching than on the other SLP_* pins, since SLP_SUS# is the control signal for one of the scenarios where SUS well power is lost (DeepSx). The effect of setting this bit to '1' on: - SLP_S3#, SLP_S4#, SLP_A# and SLP_LAN# stretching: disabled after any SUS power loss - SLP_SUS# stretching: disabled after G3, but no impact on DeepSx This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by the RTCRST# pin.

Bit Range	Default & Access	Field Name (ID): Description
11:10	0h RW/L	**SLP_S3# Minimum Assertion Width (SLP_S3_MIN_ASST_WDTH):** This 2-bit value indicates the minimum assertion width of the SLP_S3# signal to guarantee that the Main power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00: 60 usec 01: 1 ms 10: 50 ms 11: 2 sec This field is not writable when the SLP_Sx# Stretching Policy Lock- Down bit is set. This bit is cleared by the RSMRST# pin.
9	0h RW/1C/V	**Host Reset Status (HOST_RST_STS):** This bit is set by hardware when a host partition reset (not a global reset, DeepSx, or G3) occurs. This bit is an optional tool to help BIOS determine when a host partition reset might have collided with a wake from a valid sleep state. A possible usage model would be to consult and then write a '1' to clear this bit during the boot flow before determining what action to take based on reading PM1_STS.WAK_STS = '1'. If HOST_RST_STS = '1' and/or GEN_PMCON_A.GBL_RST_STS = '1', the cold reset boot path could be followed rather than the resume path, regardless of the setting of WAK_STS. This bit does not affect PCH operation in any way, and can therefore be left set if BIOS chooses not to use it.
8	0h RW/L	**ESPI SMI Lock (ESPI_SMI_LOCK):** When this bit is set, writes to the ESPI_SMI_EN bit will have no effect. Once the ESPI_SMI_LOCK bit is set, writes of 0 to ESPI_SMI_LOCK bit will have no effect (i.e. once set, this bit can only be cleared by RSMRST#).
7:6	0h RO	Reserved.
5:4	0h RW/L	**SLP_S4# Minimum Assertion Width (S4MAW):** This 2-bit value indicates the minimum assertion width of the SLP_S4# signal to guarantee that the DRAMs have been safely power-cycled. This value may be modified per platform depending on DRAM types, power supply capacitance, etc. Valid values are: 11: 1 second 10: 2 seconds 01: 3 seconds 00: 4 seconds This value is used in two ways: 1. If the SLP_S4# assertion width is ever shorter than this time, a status bit (D31.F0.A2h.2) is set for BIOS to read when S0 is entered 2. If enabled by bit 3 in this register, the hardware will prevent the SLP_S4# signal from deasserting within this minimum time period after asserting. Note that the logic that measures this time is in the suspend power well. Therefore, when leaving a G3 or DeepSx state, the minimum time is measured from the deassertion of the internal suspend well reset (unless the Disable SLP_X Stretching After SUS Power Failure bit is set). This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. RTCRST# forces this field to the conservative default state (00b).

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/L	**SLP_S4# Assertion Stretch Enable (S4ASE):** When set to 1, the SLP_S4# pin will minimally assert for the time specified in bits 5:4 of this register. When 0, the minimum assertion time for SLP_S4# is the same as the timing defined in the Platform Design Guide. This bit is provided so that all DIMMs in the system can deterministically detect a power-cycle event for proper initialization. Note that there are behavioral changes that may be noticeable when this bit is set. Resume times from S4 and S5 and power-up times from G3 or DeepSx may be delayed by several seconds. This bit is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by RTCRST#.
2:1	0h RW	**Period SMI Select (PER_SMI_SEL):** Software sets these bits to control the rate at which the periodic SMI# is generated: 00 = 64 seconds (default), 01 = 32 seconds, 10 = 16 seconds, 11 = 8 seconds Tolerance for the timer is +/- 1 second.
0	0h RW	**AFTERG3_EN (AG3E):** Determines what state to go to when power is reapplied after a power failure (G3 state). 0 = System will return to an S0 state (boot) after power is re-applied. 1 = System will return to the S5 state (except if it was in S4, in which case it will return to S4-like state). In the S5 state, the only enabled wake-up event is the Power Button or any enabled wake event that was preserved through the power failure. This bit is in the RTC well and is only cleared by RTCRST#.

4.3.2 General PM Configuration B (GEN_PMCON_B)—Offset 1024h

General PM configuration B

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW/L	**SLP_Sx# Stretching Policy Lock-Down (SLPSX_STR_POL_LOCK):** When set to 1, this bit locks down the following fields: - GEN_PMCON_3.DIS_SLP_X_STRCH_SUSPF - GEN_PMCON_3.SLP_S3_MIN_ASST_WDTH - GEN_PMCON_3.S4MAW - GEN_PMCON_3.S4ASE - PM_CFG.SLP_A_MIN_ASST_WDTH - PM_CFG.SLP_LAN_MIN_ASST_WDTH - PM_CFG.PWR_CYC_DUR Those bits become read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset. This lockdown bit is available in both desktop and mobile.
17	0h RW/L	**VR Config Lock (VR_CONFIG_LOCK):** When set to 1, this bit locks down the enable bits in the EXT_RAIL_CONFIG register such that the enable becomes read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset. This lockdown bit is available in both desktop and mobile.
16:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RW	**WOL Enable Override (WOL_EN_OVRD):** When this bit is set to 1, the integrated LAN is enabled to wake the system from S5 regardless of the value in the PME_B0_EN bit in the GPE0_EN register. This allows the system BIOS to enable Wake-On-LAN regardless of the policies selected through the operating system. This bit is maintained in the RTC power well, therefore permitting WOL following a surprise power failure even in cases in which the system may have been running in S0 without the PME Enables set. (Note that the LAN NVRAM configuration must support WOL after SUS power loss.) When this bit is cleared to 0, the wake-on-LAN policies are determined by OS-visible bits. This bit has no effect on wakes from S1, S3, or S4. This bit is cleared by RSMRST# pin
12:11	0h RO	Reserved.
10	0h RW	**BIOS PCI Express Enable (BIOS_PCI_EXP_EN):** This bit acts as a global enable for the SCI associated with the PCI express ports. If this bit is not set, then the various PCI Express ports and MCH cannot cause the PCI_EXP_STS bit to go active.
9	0h RO/V	**Power Button Level (PWRBTN_LVL):** This read-only bit indicates the current state of the PWRBTN# signal. 1= High, 0 = Low. The value reflected in this bit is dependent upon PM_CFG1.PB_DB_MODE. The PB_DB_MODE bit's value causes the following behavior: - '0': PWRBTN_LVL is taken from the debounced PWRBTN# pin value that is seen at the output of a 16ms debouncer. - '1': PWRBTN_LVL is taken from the raw PWRBTN# pin (before the debouncer).
8:5	0h RO	Reserved.
4	0h RW/L	**SMI Lock (SMI_LOCK):** When this bit is set, writes to the GLB_SMI_EN bit will have no effect. Once the SMI_LOCK bit is set, writes of 0 to SMI_LOCK bit will have no effect (i.e. once set, this bit can only be cleared by RSMRST#).
3	0h RO	Reserved.
2	1h RW	**RTC_PWR_STS (RPS):** The PCH will set this bit to 1 when rtc_pwrgood_rst indicates a weak or missing battery. The bit will remain set until the software clears it by writing a 0 back to this bit position. This bit is not cleared by any type of reset.
1:0	0h RO	Reserved.

4.3.3 Configured Revision ID (CRID)—Offset 1030h

Configured revision ID Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**CRID Lock (CRID_LK):** BIOS writes to this bit to lock this register (a specific lock bit is preferable over a write-based self-lock for the RID_SEL field). When this bit is written to 1, the entire register becomes RO (writes have no effect, reads return actual value) until the next assertion of RMSRST#.
30:2	0h RO	Reserved.
1:0	0h RW/L	**RID Select(RID_SEL) (rid_sel):** Software writes this field to select Revision ID reflected in PCI Config space. The decoding is: 00 - Revision ID 01 - CRID 0 10 - CRID 1 11 - CRID 2 Once written, this field can only be cleared by RSMRST#. BIOS should write to this bit on all boots, (HOST_RST/platform.)

4.3.4 Extended Test Mode Register 3 (ETR3)—Offset 1048h

This register resides in the primary well.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V/L	**CF9h Lockdown (CF9LOCK):** When set, this bit will lock the CF9h Global Reset bit and this register. This register is reset by a CF9h reset.
30:21	0h RO	Reserved.
20	0h RW/L	**CF9h Global Reset (CF9GR):** 1 = a CF9h write of 6h or Eh will cause a Global Reset of both the Host and the Intel (R) ME partitions. 0 = a CF9h write of 6h or Eh will only reset the Host partition. It is recommended that BIOS should set this bit early on in the boot sequence, and then clear it and set the CF9LOCK bit prior to loading the OS in both an Intel CSME Enabled and a Intel CSME Disabled system. This register is locked by the CF9 Lockdown (CF9LOCK) bit. This register is not reset by a CF9h reset.
19:0	0h RO	Reserved.

4.3.5 SET STRAP MSG LOCK (SSML)—Offset 104Ch

SET STRAP MSG LOCK

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/L	**Set_Strap Lock (SSL):** When set to 1, all of SSML, SSMC and SSMD is locked, including this Lock bit. Note that this bit is reset on host partition reset

4.3.6 SET STRAP MSG CONTROL (SSMC)—Offset 1050h

SET STRAP Message Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/L	**Set_Strap Mux Select (SSMS):** When set to 1, the Set strap message bits [47:32] come from the Set_Strap Msg Data register. This bit is reset by the RSMRST# pin only. When 0, the Set-Strap data continues to come from the soft straps themselves.This register field is locked by the Set Strap Lock (SSML.SSL) bit.

4.3.7 SET STRAP MSG DATA (SSMD)—Offset 1054h

This register is used to provide a BIOS programmable sticky register which contains data that will be used in the Set-Strap type 1 msg on subsequent resets. The bits in the message control certain CPU features, for which see the CPU spec. These bits are in the resume well, so only reset on G3. The usage model is that on each reset BIOS will check the state of the CPU. If the state is correct, then BIOS continues. If not, then BIOS writes the SSMD and SSMC registers and does a CF9 reset. On the reset the value of what was written to SSMD takes effect. Note that some mobile platforms force G3 on S5 requests. For those platforms, if the user/BIOS wants to have these bits set, there will be 2 resets on every power-on. If the platform accepts the default of 0 for these controls, then there is only one reset. The bits are in DSW and not RTC well because this allows a user upgrade, assuming the user unplugged the system before doing the upgrade, to revert to a setting of 0. This should reduce any interoperability concerns regarding user upgrades. The DSW bits are all cleared by DSW_PWROK, and must not be cleared by CF9h resets.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW/L	**Set_Strap DATA (SSD):** When SSMS is 1, then this data is sent in the Set-Strap msg Type 1 upon reset. This data is sent i//n the 2nd DW of data, bits 15:0. This register field is locked by the Set Strap Lock SSML.SSL bit.

4.3.8 Configured Revision ID (CRID_UIP)—Offset 10B0h

Configured revision ID Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/V	**CRID Update in Progress (CRID_UIP):** PMC HW sets this bit to indicate that SetID broadcast flow has been requested by BIOS. This bit is cleared by PMC FW only when the completion/s for the multicast non-posted SetIDVal message is received by PMC. BIOS is required to read this bit as cleared before writing to the CRID register (to request a CRID update). BIOS is also required to poll on reads to this bit until it sees the bit as cleared after BIOS has written to the CRID register. 0 Any previously requested CRID Update is complete. 1 the most recently requested CRID update is still in progress.

4.3.9 HSIO Power Management Configuration 1 (MODPHY_PM_CFG1)—Offset 10C0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11:0	0h RW	**HSIO Lane S0 SUS Well Power Gating Policy (MLS0SWPGP):** This is a bit per lane that controls SUS Well Power Gating for a HSIO lane to be used for S0 and S0ix. Bit 0: Corresponds to HSIO Lane 0 Bit 1: Corresponds to HSIO Lane 1 Bit 2: Corresponds to HSIO Lane 2 : : Bit 11: Corresponds to HSIO Lane 11 For each lane: 0: Lane power gating not permitted in S0. 1: Lane power gating is permitted in S0. Note that strap information/PCIe Lane reversal information will be factored by BIOS when programming these bits in the configuration registers. Note that it is not allowed for SW programming to have a bit location to be 1 in this field and the corresponding bit position to be 0 in MLSXSWPGP

4.3.10 HSIO Power Management Configuration 2 (MODPHY_PM_CFG2)—Offset 10C4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FFFh

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11:0	FFFh RW	**HSIO Lane Sx SUS Well Power Gating Policy [11:0] (MLSXSWPGP):** This is a bit per lane that controls SUS Well Power Gating for a HSIO lane when system is in Sx. Bit 0: Corresponds to HSIO Lane 0 Bit 1: Corresponds to HSIO Lane 1 Bit 2: Corresponds to HSIO Lane 2 : : Bit 11: Corresponds to HSIO Lane 11 For each lane: 0: Lane power gating not permitted in Sx. 1: Lane power gating is permitted in Sx. Note that strap information/PCIe Lane reversal information will be factored by BIOS when programming these bits in the configuration registers. This field will be used to manage Sx policies even in S0. In other words, the earlier restriction that BIOS does not have to program this field if MLSPDDGE is 1 does not apply any more. BIOS shall set this field appropriately for all cases.

4.3.11 HSIO Power Management Configuration 3 (MODPHY_PM_CFG3)—Offset 10C8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 5000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	0h RW	**HSIO Lane SUS Power Domain Dynamic Gating Enable (MLSPDDGE):** When this bit is set to 1, HSIO Lane SUS Well Dynamic Gating is enabled. When this bit is 0, HSIO Lane SUS Well Gating can still be done at a more coarse level using MLSXSWPGP and MLS0SWPGP fields.
29	0h RW	**Enable HSIO FET Control (EMFC):** This bit enables PMC dynamic control of HSIO lane external FET. When this bit is 0 and MLSPDDGE is 1, PMC goes through all of the HSIO lane power gating flows except that the external FET is not turned off. This bit is being provided primarily to prevent External FET gating during EXI debug
28:24	5h RW/L	**External FET Ramp Time (EFRT):** This field defines the ramp time of HSIO FET. 00000b: 00us 00001b: 20us 00010b: 40us ... 00101b: 100us ... 11111b: 620us This bit is locked while PM_SYNC_MISC_CFG.PM_SYNC_LOCK = '1'
23:2	0h RO	Reserved.
1	0h RW	**HSIO Per-Lane SUS Power Domain Dynamic Gating Enable (MPLSPDDGE):** When this bit is set to 1, HSIO Per-Lane SUS Well Dynamic Gating is enabled. When this bit is 0, if HSIO lane SUS power domain dynamic gating is enabled, all lanes are gated/ungated together. This bit has no impact if HSIO lane SUS power domain dynamic gating is disabled.
0	0h RO	Reserved.

4.3.12 HSIO Power Management Configuration 4 (MODPHY_PM_CFG4)—Offset 10CCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**ASL Over-rides [26:0] (ASLOR):** This field provides BIOS code to take over SPD power gating control. If BIOS code sets a bit corresponding to a controller, it implies that PMC shall ignore any other inputs from that controller and assume that the controller is ready for SPD power gating. 0 in a bit position: Use HW interfaces for the controller to manage SPD gating/wake-up. 1 in a bit position: Ignore HW interfaces for the controller, rely only on MSPDRTReq field thats managed by BIOS code. Bit 0: Corresponds to PCIe Controller A, Function 0 Bit 1: Corresponds to PCIe Controller A, Function 1 Bit 2: Corresponds to PCIe Controller A, Function 2 Bit 3: Corresponds to PCIe Controller A, Function 3 Bit 4: Corresponds to PCIe Controller B, Function 0 Bit 5: Corresponds to PCIe Controller B, Function 1 Bit 6: Corresponds to PCIe Controller B, Function 2 Bit 7: Corresponds to PCIe Controller B, Function 3 Bit 8: Corresponds to PCIe Controller C, Function 0 Bit 9: Corresponds to PCIe Controller C, Function 1 Bit 10: Corresponds to PCIe Controller C, Function 2 Bit 11: Corresponds to PCIe Controller C, Function 3 Bit 12: Corresponds to SATA Controller Bit 13: Corresponds to Gbe Controller Bit 14: Corresponds to xHCI Controller Bit 15: Corresponds to xDCI Controller Bit 16-24: Reserved Bit 25: Corresponds to DMI Controller Bit 26: Reserved This field is going to be used in conjunction with MSPDRTReq and MSPDRTRAck fields above. If BIOS code intends to over-ride HW decisions, it will set the corresponding bit for a controller/function to 1 in ASLOR and use MSPDRTReq bits to power-up/power-down SPD.

4.3.13 HSIO Power Management Configuration 5 (MODPHY_PM_CFG5)—Offset 10D0h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Controller SPD RTD3 Request [26:0] (MSPDRTREQ):** This field provides BIOS code to take over SPD power gating control. If BIOS code sets a bit corresponding to a controller, it implies that PMC shall ignore any other inputs from that controller and assume that the controller is ready for SPD power gating. 0 in a bit position: Use HW interfaces for the controller to manage SPD gating/wake-up. 1 in a bit position: Ignore HW interfaces for the controller, rely only on MSPDRTReq field thats managed by BIOS code. Bit 0: Corresponds to PCIe Controller A, Function 0 Bit 1: Corresponds to PCIe Controller A, Function 1 Bit 2: Corresponds to PCIe Controller A, Function 2 Bit 3: Corresponds to PCIe Controller A, Function 3 Bit 4: Corresponds to PCIe Controller B, Function 0 Bit 5: Corresponds to PCIe Controller B, Function 1 Bit 6: Corresponds to PCIe Controller B, Function 2 Bit 7: Corresponds to PCIe Controller B, Function 3 Bit 8: Corresponds to PCIe Controller C, Function 0 Bit 9: Corresponds to PCIe Controller C, Function 1 Bit 10: Corresponds to PCIe Controller C, Function 2 Bit 11: Corresponds to PCIe Controller C, Function 3 Bit 12: Corresponds to SATA Controller Bit 13: Corresponds to Gbe Controller Bit 14: Corresponds to xHCI Controller Bit 15: Corresponds to xDCI Controller Bit 16-24: Reserved Bit 25: Corresponds to DMI Controller Bit 26: Reserved

4.3.14 HSIO Power Management Configuration 6 (MODPHY_PM_CFG6)—Offset 10D4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Controller SPD RTD3 Request Acknowledge [19:0] (MSPDRTRACK):** This field provides BIOS code to take over SPD power gating control. If BIOS code sets a bit corresponding to a controller, it implies that PMC shall ignore any other inputs from that controller and assume that the controller is ready for SPD power gating. 0 in a bit position: Use HW interfaces for the controller to manage SPD gating/wake-up. 1 in a bit position: Ignore HW interfaces for the controller, rely only on MSPDRTReq field thats managed by BIOS code. Bit 0: Corresponds to PCIe Controller A, Function 0 Bit 1: Corresponds to PCIe Controller A, Function 1 Bit 2: Corresponds to PCIe Controller A, Function 2 Bit 3: Corresponds to PCIe Controller A, Function 3 Bit 4: Corresponds to PCIe Controller B, Function 0 Bit 5: Corresponds to PCIe Controller B, Function 1 Bit 6: Corresponds to PCIe Controller B, Function 2 Bit 7: Corresponds to PCIe Controller B, Function 3 Bit 8: Corresponds to PCIe Controller C, Function 0 Bit 9: Corresponds to PCIe Controller C, Function 1 Bit 10: Corresponds to PCIe Controller C, Function 2 Bit 11: Corresponds to PCIe Controller C, Function 3 Bit 12: Corresponds to SATA Controller Bit 13: Corresponds to Gbe Controller Bit 14: Corresponds to xHCI Controller Bit 15: Corresponds to xDCI Controller Bit 16-24: Reserved Bit 25: Corresponds to DMI Controller Bit 26: Reserved

4.3.15 External Rail Config (EXT_RAIL_CONFIG)—Offset 11B8h

External Rail Configuration

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RW/L	**Enable External V1P05 Rail in S5 (ENABLE_EXT_V1P05_RAIL_S5):** Enable External V1P05 Rail in S5
11	0h RW/L	**Enable External V1P05 Rail in S4 (ENABLE_EXT_V1P05_RAIL_S4):** Enable External V1P05 Rail in S4
10	0h RW/L	**Enable External V1P05 Rail in S3 (ENABLE_EXT_V1P05_RAIL_S3):** Enable External V1P05 Rail in S3
9	0h RW/L	**Enable External V1P05 Rail in S0i3 (ENABLE_EXT_V1P05_RAIL_S0I3):** Enable External V1P05 Rail in S0i3
8	0h RW/L	**Enable External V1P05 Rail in S0i1/S0i2 (ENABLE_EXT_V1P05_RAIL_S0I1_I2):** Enable External V1P05 Rail in S0i1/S0i2
7:5	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/L	**Enable External VNN Rail in S5 (ENABLE_EXT_VNN_RAIL_S5):** Enable External Vnn Rail in S5
3	0h RW/L	**Enable External VNN Rail in S4 (ENABLE_EXT_VNN_RAIL_S4):** Enable External Vnn Rail in S4
2	0h RW/L	**Enable External VNN Rail in S3 (ENABLE_EXT_VNN_RAIL_S3):** Enable External Vnn Rail in S3
1	0h RW/L	**Enable External VNN Rail in S0i3 (ENABLE_EXT_VNN_RAIL_S0I3):** Enable External Vnn Rail in S0i3
0	0h RW/L	**Enable External VNN Rail in S0i1/S0i2 (ENABLE_EXT_VNN_RAIL_S0I1_I2):** Enable External Rail in S0i1/S0i2

4.3.16 External Rail Config (EXT_V1P05_VR_CONFIG)—Offset 11C0h

External Rail Configuration

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:24	0h RW/L	**External V1P05 Voltage Value - Upper (EXT_V1P05_VOLTAGE1):** This register houses the voltage for the external V1p05 rail that will be used in S0i2/S0i3 states. Expectation is that SW will update this based on if we are i S0i2 or S0i3. This value is given in 2.5mV increments. PMC will need to write this value to the WORKPOINT FIVR sleep entrance register. When this register is updated, the value in this field gets translated into a write to the SSBFEXITWP1 regsiter in the associated FIVR , in the format expected in SSBEXITWP1. OEM cannot change the value of the PMIC voltage during idle windows in which this supply is being used.
23:16	0h RW/L	**External V1P05 Voltage Value - Lower (EXT_V1P05_VOLTAGE0):** This register houses the voltage for the external V1p05 rail that will be used in S0i2/S0i3 states. Expectation is that SW will update this based on if we are i S0i2 or S0i3. This value is given in 2.5mV increments. PMC will need to write this value to the WORKPOINT FIVR sleep entrance register. When this register is updated, the value in this field gets translated into a write to the SSBFEXITWP1 regsiter in the associated FIVR , in the format expected in SSBEXITWP1. OEM cannot change the value of the PMIC voltage during idle windows in which this supply is being used.
15:8	0h RW/L	**External V1P05 Icc Max Value - Upper (EXT_V1P05_ICC_MAX_VAL1):** This register houses the Icc max for the external V1p05 rail in granularity of ma in U2.14 format.
7:0	0h RW/L	**External V1P05 Icc Max Value - Lower (EXT_V1P05_ICC_MAX_VAL0):** This register houses the Icc max for the external V1p05 rail in granularity of ma in U2.14 format.of this register can be programmed to 200mA

4.3.17 External Rail Config (EXT_VNN_VR_CONFIG0)—Offset 11C4h

External Rail Configuration

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:24	0h RW/L	**External VNN Voltage Value - Upper (EXT_VNN_VOLTAGE1):** This register houses the voltage for the external VNN rail that will be used in S0i2/S0i3 states. Expectation is that SW will update this based on if we are in S0i2 or S0i3. This value is given in 2.5mV increments. The value of the PMIC voltage cannot be changed during idle windows in which this supply is being used.
23:16	0h RW/L	**External VNN Voltage Value - Lower (EXT_VNN_VOLTAGE0):** This register houses the voltage for the external VNN rail that will be used in S0i2/S0i3 states. Expectation is that SW will update this based on if we are in S0i2 or S0i3. This value is given in 2.5mV increments. The value of the PMIC voltage cannot be changed during idle windows in which this supply is being used.
15:8	0h RW/L	**External VNN Icc Max Value - Upper (EXT_VNN_ICC_MAX_VAL1):** This register houses the Icc max for the external VNN rail in granularity of ma in U2.14 format.
7:0	0h RW/L	**External VNN Icc Max Value - Lower (EXT_VNN_ICC_MAX_VAL0):** This register houses the Icc max for the external VNN rail in granularity of ma in U2.14 format.

4.3.18 VNN V1p05 Control Hold Off (VNN_V1P05_CTRL_HOLD_OFF)—Offset 11C8h

Hold Off Control for V1p05

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 101h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	1h RW/L	**V1p05 Control Ramp Timer (V1P05_CTRL_RAMP_TMR):** This register holds the V1P05 control hold off values to be used when changing the v1p05_ctrl for external bypass value in us
7:0	1h RW/L	**VNN Control Ramp Timer (VNN_CTRL_RAMP_TMR):** This register holds the VNN control hold off values to be used when changing the vnn_ctrl for external bypass value in us

4.3.19 EXT FET RAMP CFG (EXT_FET_RAMP_CFG)—Offset 11CCh

External FET Ramp Time Configuration

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 40004h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**V1p05-IS FET Ramp Time Lock (V1P05_IS_FRT_LOCK):** The bit is used to lock V1P05_IS_FET_RAMP_TIME. This bit is self-locking (i.e. once written to '1', it can only be cleared by RSMRST#).
30:24	0h RO	Reserved.
23:16	4h RW/L	**V1p05-IS FET Ramp Time (V1P05_IS_FET_RAMP_TIME):** This field defines the ramp time of the external V1p05-IS FET. Each increment is 10us (ie. 0x4=40us). This field is locked by V1P05_IS_FRT_LOCK.
15	0h RW/L	**V1P05-PHY FET Ramp Time Lock (V1P05_PHY_FRT_LOCK):** The bit is used to lock V1P05_PHY_FET_RAMP_TIME. This bit is self-locking (i.e. once written to '1', it can only be cleared by RSMRST#).
14:8	0h RO	Reserved.
7:0	4h RW/L	**V1p05-PHY FET Ramp Time (V1P05_PHY_FET_RAMP_TIME):** This field defines the ramp time of the external V1p05-PHY FET. Each increment is 31us (ie. 0x4=124us). This field is locked by V1P05_PHY_FRT_LOCK.

4.3.20 VCCIN AUX CONFIG Register1 (VCCIN_AUX_CFG1)—Offset 11D0h

This register defines the characteristics of the VCCIN_AUX voltage rail

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	0h RW/L	**Low Current Mode Voltage to High Current Mode Voltage Transition Time (LCM_HCM_VOLT_TRANS_TIME):** Voltage transition time required by motherboard voltage regulator when PCH changes the VCCIN_AUX regulator set point from the low current mode voltage and high current mode voltage. This field has 1us resolution. 8'h00 = Transition from low current mode voltage retention mode VID disabled. (default) 8'h01 = 1us 8'h02 = 2us ... 8'hFF = 255us Note: When [23:16]=8'h00 PCH will not transition VCCIN_AUX to low current mode voltage.
15:8	0h RW/L	**Retention Mode Voltage to High Current Mode Voltage Transition Mode (RMV_HCM_VOLT_TRANS_TIME):** Voltage transition time required by motherboard voltage regulator when PCH changes the VCCIN_AUX regulator set point from the retention mode voltage and low current mode voltage. This field has 1us resolution. 8'h00 = Transition from retention mode voltage to high current mode voltage is disabled (default) 8'h01 = 1us 8'h02 = 2us ... 8'hFF = 255us Note: When [7:0]=8'h00 and [15:8]=8'h00 PCH will not transition VCCIN_AUX to retention voltage.
7:0	0h RW/L	**Retention Mode Voltage to Low Current Mode Voltage Transition Mode (RMV_LCM_VOLT_TRANS_TIME):** Voltage transition time required by motherboard voltage regulator when PCH changes the VCCIN_AUX regulator set point from the retention mode voltage and low current mode voltage.This field has 1us resolution. 8'h00 = Transition from retention mode voltage to low current mode voltage is disabled (default) 8'h01 = 1us 8'h02 = 2us ... 8'hFF = 255us Note: When [7:0]=8'h00 and [15:8]=8'h00 PCH will not transition VCCIN_AUX to retention voltage.

4.3.21 VCCIN AUX CONFIG Register2 (VCCIN_AUX_CFG2)—Offset 11D4h

This register defines the characteristics of the VCCIN_AUX voltage rail

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10:8	0h RW/L	**Off To High Current Mode Voltage Transition Time Bits [10:8] (OFF_HCM_VOLT_TRANS_TIME_10_8):** Voltage transition time required by motherboard voltage regulator when PCH changes the VCCIN_AUX regulator set point from 0V to the high current mode voltage. 11'h000 = Transition to 0V in S0 & Sx states is disabled (default) 11'h001 = 1us 11'h002 = 2us ... 11'hFFF = 2048us Note: Setting this field to 11'h000 sets VCCIN_AUX as a fixed rail that stays on in all S0 & Sx power states after initial start up on G3 exit
7:0	0h RW/L	**Off To High Current Mode Voltage Transition Time Bits[7:0] (OFF_HCM_VOLT_TRANS_TIME_7_0):** Voltage transition time required by motherboard voltage regulator when PCH changes the VCCIN_AUX regulator set point from 0V to the high current mode voltage. 11'h000 = Transition to 0V in S0 & Sx states is disabled (default) 11'h001 = 1us 11'h002 = 2us ... 11'hFFF = 2048us Note: Setting this field to 11'h000 sets VCCIN_AUX as a fixed rail that stays on in all S0 & Sx power states after initial start up on G3 exit

4.3.22 Always Running Timer Value 31:0 (ARTV_31_0)—Offset 1200h

Note: This register is intended for debug purposes. To obtain the most accurate timer reading, customers are recommended to read the PCH ART through the CPU TSC register and apply CPUID conversion.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**ART Value (ARTV):** Reads return current value of the ART timer [31:0]. Writes to this register has no effect Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.3.23 Always Running Timer Value 31:0 (ARTV_63_32)—Offset 1204h

Note: This register is intended for debug purposes. To obtain the most accurate timer reading, customers are recommended to read the PCH ART through the CPU TSC register and apply CPUID conversion.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**ART Value (ARTV):** Reads return current value of the ART timer [63:32]. Writes to this register has no effect Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.3.24 Timed GPIO Control 0 (TGPIOCTL0)—Offset 1210h

Timed GPIO COntrol 0

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW	**Periodic Mode (PM):** 0:Periodic mode is disabled 1:periodic mode is enabled This bit is only applicable when Timed GPIO is configured as an output
3:2	0h RW	**Event Polarity (EP):** 00:Rising Edge 01:Falling Edge 10:Toggle Edge 11:Reserved
1	0h RW	**Direction (DIR):** 0: Output 1: Input
0	0h RW	**Enable (EN):** 0: Timed GPIO is disabled 1: Timed GPIO is enabled Note: a. When Enabled, xtal clock turnoff is disabled. This may also disable SLP_S0 assertion b. All other Timed GPIO configuration bits must be programmed before enable bit is set and must not change while the enable is 1

4.3.25 Timed GPIO 0 Comparator Value 31:0 (TGPIOCOMPV0_31_0)—Offset 1220h

Timed GPIO 0 comparator Value 31:0

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Comparator Value (COMPV):** This register is only applicable when Timed GPIO is configured as an output. If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. For example, in periodic mode if the value written to this register is 00000100h, and Periodic Interval register has the value of 200h. 1. A Timed GPIO event will be generated when ART reaches 00000100h. 2. The value in this register will then be adjusted by the hardware to 00000300h. 3. Another Timed GPIO event will be generated when the ART reaches 00000300h. 4. The value in this register will then be adjusted by the hardware to 00000500h As such when periodic Timed GPIO event occurs, the value in this register will increment. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.3.26 Timed GPIO Comparator Value 63:32 (TGPIOCOMPV0_63_32)—Offset 1224h

Timed GPIO Comparator Value

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Comparator Value (COMPV):** Refer to Comparator Value [31:0] for description.

4.3.27 Timed GPIO0 Periodic Interval Value 31_0 (TGPIOPIV0_31_0)—Offset 1228h

Timed GPIO0 Periodic Interval Value 31_0

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Periodic Interval Value [31:0] (PIV):** This register is only applicable when Timed GPIO is configured as an output, and Periodic Mode is enabled. The value in this register is written by SW to set the interval for the periodic Timed GPIO event

4.3.28 Timed GPIO 0 Periodic Interval Value 63_32 (TGPIOPIV0_63_32)—Offset 122Ch

Timed GPIO 0 Periodic Interval Value 63_32

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Periodic Interval Value [63:32] (PIV):** Refer to Periodic Interval Value [31:0] for description.

4.3.29 Timed GPIO Time Capture Register 31_0 (TGPIOTCV0_31_0)—Offset 1230h

Timed GPIO Time Cpature Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Time Capture Value [31:0] (TCV):** When Timed GPIO event triggers, HW captures the current ART time into this register. This register is applicable to both when Timed GPIO is configured as an input or an output. When Timed GPIO is configured as an output, the Time Capture Value in this register is the Comparator Value (COMPV) when a match with ART time happens and a Timed GPIO output event generated. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.3.30 Timed GPIO0 Time Capture Register 63_32 (TGPIOTCV0_63_32)—Offset 1234h

Timed GPIO Time Capture Register 63_32

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Time Capture Value [63:32] (TCV):** Refer to Time Capture Value [31:0] for description.

4.3.31 Timed GPIO0 Event Counter Capture Register 31_0 (TGPIOECCV0_31_0)—Offset 1238h

Timed GPIO0 Event Counter Capture Register 31_0

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Event Counter Capture Value [31:0] (ECCV):** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register. A read to the Time Capture Value (TGPIOTCV0_31_0) register triggers HW to load the Event Counter value into this register. Note: The 'load' signal is the same register read signal that returns the Time Capture Value to the SW. SW must first perform a read to the Time Capture Value (TGPIOTCV0_31_0) register, followed by a read to this Event Counter Capture Value (ECCV) register such that these two values are associated with each others, despite they are obtained thru 2 separate register read operations one after another. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.3.32 Timed GPIO0 Event Counter Capture Register 63_32 (TGPIOECCV0_63_32)—Offset 123Ch

Timed GPIO0 Event Counter Capture Register 63_32

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Event Counter Capture Value [63:32] (ECCV):** Refer to Event Counter Capture Value [31:0] for description.

4.3.33 Timed GPIO0 Event Counter Register 31_0 (TGPIOEC0_31_0)—Offset 1240h

Timed GPIO0 Event Counter Register 31_0

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Event Counter Register [31:0] (EC):** Event Counter (EC): After Timed GPIO is enabled, event counter operates as follow: ' When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. ' When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. Note: The signal to increment the count is the same signal that captures the ART time into the TCV register. For Timed GPIO configured as output with Periodic Mode enabled, it is also the same signal that updates the Comparator Value for the subsequent match. When Timed GPIO is disabled, event counter is reset to 0x0. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.3.34 Timed GPIO0 Event Counter Register 63_32 (TGPIOEC0_63_32)—Offset 1244h

Timed GPIO0 Event Counter Register 63_32

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Event Counter Register [31:0] (EC):** Refer to Event Counter Register [31:0] for description.

4.3.35 Timed GPIO Control 1 (TGPIOCTL1)—Offset 1310h

Timed GPIO Control 1

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW	**Periodic Mode (PM):** 0:Periodic mode is disabled 1:periodic mode is enabled This bit is only applicable when Timed GPIO is configured as an output
3:2	0h RW	**Event Polarity (EP):** 00:Rising Edge 01:Falling Edge 10:Toggle Edge 11:Reserved
1	0h RW	**Direction (DIR):** 0: Output 1: Input
0	0h RW	**Enable (EN):** 0: Timed GPIO is disabled 1: Timed GPIO is enabled Note: a. When Enabled, xtal clock turnoff is disabled. This may also disable SLP_S0 assertion b. All other Timed GPIO configuration bits must be programmed before enable bit is set and must not change while the enable is 1

4.3.36 Timed GPIO 1 Comparator Value 31:0 (TGPIOCOMPV1_31_0)—Offset 1320h

Timed GPIO 1 comparator Value 31:0

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Comparator Value (COMPV):** This register is only applicable when Timed GPIO is configured as an output. If periodic mode is not enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. The value in this register does not change. If periodic mode is enabled, when ART equals the value last written to this register, the Timed GPIO event is generated. When this occurs, the value in this register is increased by the value in the Periodic Interval register. For example, in periodic mode if the value written to this register is 00000100h, and Periodic Interval register has the value of 200h. 1. A Timed GPIO event will be generated when ART reaches 00000100h. 2. The value in this register will then be adjusted by the hardware to 00000300h. 3. Another Timed GPIO event will be generated when the ART reaches 00000300h. 4. The value in this register will then be adjusted by the hardware to 00000500h As such when periodic Timed GPIO event occurs, the value in this register will increment. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.3.37 Timed GPIO Comparator Value 63:32 (TGPIOCOMPV1_63_32)—Offset 1324h

Timed GPIO Comparator Value 63:32

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Comparator Value (COMPV):** Refer to Comparator Value [31:0] for description.

4.3.38 Timed GPIO1 Periodic Interval Value 31_0 (TGPIOPIV1_31_0)—Offset 1328h

Timed gPIO Periodic Interval Value 31_0

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Periodic Interval Value [31:0] (PIV):** This register is only applicable when Timed GPIO is configured as an output, and Periodic Mode is enabled. The value in this register is written by SW to set the interval for the periodic Timed GPIO event

4.3.39 Timed GPIO 1 Periodic Interval Value 63_32 (TGPIOPIV1_63_32)—Offset 132Ch

Timed GPIO 1 Periodic Interval Value 63_32

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Periodic Interval Value [63:32] (PIV):** Refer to Periodic Interval Value [31:0] for description.

4.3.40 Timed GPIO Time Capture Register 31_0 (TGPIOTCV1_31_0)—Offset 1330h

Timed GPIO Time Capture Register 31_0

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Time Capture Value [31:0] (TCV):** When Timed GPIO event triggers, HW captures the current ART time into this register. This register is applicable to both when Timed GPIO is configured as an input or an output. When Timed GPIO is configured as an output, the Time Capture Value in this register is the Comparator Value (COMPV) when a match with ART time happens and a Timed GPIO output event generated. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.3.41 Timed GPIO Time Capture Register 63_32 (TGPIOTCV1_63_32)—Offset 1334h

Timed GPIO Time Capture Register 63_32

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Time Capture Value [63:32] (TCV):** Refer to Time Capture Value [31:0] for description.

4.3.42 Timed GPIO0 Event Counter Capture Register 31_0 (TGPIOECCV1_31_0)—Offset 1338h

Timed GPIO0 Event Counter Capture Register 31_0

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Event Counter Capture Value [31:0] (ECCV):** The value in this register must be the Timed GPIO event count associated with the time captured in the Time Capture Value register. A read to the Time Capture Value (TCV1_31_0) register triggers HW to load the Event Counter value into this register. Note: The 'load' signal is the same register read signal that returns the Time Capture Value to the SW. SW must first perform a read to the Time Capture Value (TCV1_31_0) register, followed by a read to this Event Counter Capture Value (ECCV) register such that these two values are associated with each others, despite they are obtained thru 2 separate register read operations one after another. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.3.43 Timed GPIO0 Event Counter Capture Register 63_32 (TGPIOECCV1_63_32)—Offset 133Ch

Timed GPIO0 Event Counter Capture Register 63_32

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Event Counter Capture Value [63:32] (ECCV):** Refer to Event Counter Capture Value [31:0] for description.

4.3.44 Timed GPIO1 Event Counter Register 31_0 (TGPIOEC1_31_0)—Offset 1340h

Timed GPIO1 Event Counter Register 31_0

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Event Counter Register [31:0] (EC):** Event Counter (EC): After Timed GPIO is enabled, event counter operates as follow: ' When Timed GPIO is configured as input, event counter will increment by 1 for every input event triggered. ' When Timed GPIO is configured as output, event counter will increment by 1 for every output event generated. Note: The signal to increment the count is the same signal that captures the ART time into the TCV register. For Timed GPIO configured as output with Periodic Mode enabled, it is also the same signal that updates the Comparator Value for the subsequent match. When Timed GPIO is disabled, event counter is reset to 0x0. Note: Given that 64 bit values are in two registers, SW needs to account for roll over possibility

4.3.45 Timed GPIO Event Counter Register 63_32 (TGPIOEC1_63_32)—Offset 1344h

Timed GPIO Event Counter Register 63_32

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Event Counter Register [31:0] (EC):** Refer to Event Counter Register [31:0] for description.

4.3.46 Catastrophic Trip Point Enable (CTEN)—Offset 150Ch

This register is used to enable Catastrophic Trip point assertion into S5 state on a Cattrip event. This bit should always be set in all functional cases.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Policy Lock-Down Bit (CTENLOCK):** When written to 1, this bit prevents any more writes to this register.
30:1	0h RO	Reserved.
0	1h RW/L	**Catastrophic Power-Down Enable (CPDEN):** 1 = the power management logic (PMC) transitions to the S5 state when a catastrophic temperature is detected by any of the sensor. The transition to the S5 state is unconditional (like the Power Button Override Function). 0 = Disable going into S5 state on a CatTrip detection. This bit should only be set to 0 for debug purposes. Note: Thermal sensor and response logic are in the core/main power well; therefore, detection of a catastrophic temperature is limited to times when this well is powered and out of reset.

4.3.47 EC Thermal Sensor Reporting Enable (ECRPTEN)—Offset 1510h

This is a BIOS programmable register used to enable reporting of temperature by PMC to EC over eSPI. Setting bit 0 will cause a GCR interrupt to PMC FW through generic GCR mechanism. FW needs to enable the periodic reporting task accordingly. Bit 31 is uses as a lock bit to prevent any further writes to bit 0.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Lock-Down Bit (ECRPTENLOCK):** When written to 1, this bit prevents any more writes to this register.
30:1	0h RO	Reserved.
0	0h RW/L	**Enable PMC to EC Temperature Reporting (EN_PMC_TO_EC_TEMP_RPT):** 0x1 : Enables the reporting of the PCH temperature to the EC (via SMBUS or eSPI). Note that this must also be set if Intel (R) CSME needs access to the PCH temperature. Once enabled this bit should not be cleared by SW. If it is cleared then the EC may get an undefined value. SW has no need to dynamically disable and then re-enable this bit. 0x0 (Default) : Disables temperature reporting (default)

4.3.48 Throttle Level (TL)—Offset 1520h

Throttle Level.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: FF3FCFFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**TLLOCK (TLLOCK):** When set to 1, this entire register (TL) is locked and remains locked until the next platform reset
30	0h RW/L	**TT State 13 Enable (TT13EN):** When set to 1 and the programmed GPIO pin is a 1, then PMSync state 13 (now called GPIO_A) will force at least T2 state.
29	0h RW/L	**TT Enable (TTEN):** This is the enable bit associated with the FW control of the throttle state. This bit needs to be set in order for the FW to be able to update the throttle state based on the comparison of the T2L/T1L/T0L with the temperature. At reset, BIOS must set bits 28:0 and then do a separate write to set bit 29 to enable throttling. SW may set bit 31 at the same time it sets bit 29 if it wishes to lock the register. If SW wishes to change the values of 28:0, it must first clear the TTEN bit, then change the values in 28:0; and then re-enable TTEN. It is legal to set bits 31, 30 and 29 with the same write This bit must not be set by SW until SW has already enabled atleast one of the thermal sensor(setting TSENx.ETS bits to 1) If TTEN is written to 0, after having been enabled, then the PCH may stay in the throttling state it was in at the moment TTEN is disabled. There is no intent that the sensor be enabled for a while and then disabled and left off. It may be disabled temporarily while changing the register values, but it should not be left in the disabled state
28:20	FFh RW/L	**T2 Level (T2L):** Determines the temp level for T2 state. If TTEN = 1 AND TSEN = 1 AND T2L >= TEMP.MAXTEMP[8:0] > T1L, then the system is in T2 state. If TTEN = 1 AND TSE = 1 AND TEMP.MAXTEMP [8:0] > T2L, then the system is in T3 state.SW Note: When TTEN =1 condition to satisfy is T2L > T1L > T0L NOTE: the T3 condition overrides PMSync[13] and forces the system to T3 if both cases are true

Bit Range	Default & Access	Field Name (ID): Description
19	0h RO	Reserved.
18:10	FFh RW/L	**T1 Level (T1L):** Determines the temp level for T1 state. If TTEN = 1 AND (|TSEN) = 1 AND T1L >= TEMP.MAXTEMP[8:0] > T0L, then the system is in T1 state. SW Note: When TTEN =1 condition to satisfy is T2L > T1L > T0L
9	0h RO	Reserved.
8:0	FFh RW/L	**T0 Level (T0L):** Determines the temp level for T0 state. If TEMP.MAXTEMP[8:0] <= T0L or TTEN = 0 OR (|TSEN) = 0, then the system is in T0 state SW Note: When TTEN =1 condition to satisfy is T2L> T1L > T0L

4.3.49 Throttle Levels Enable (TLEN)—Offset 1528h

Throttle Levels Enable

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**TLENLOCK (TLENLOCK):** When set to 1, this entire register (TLEN) is locked and remains locked until the next platform reset
30:0	0h RO	Reserved.

4.3.50 Thermal Sensor Alert High Value (TSAHV)—Offset 1530h

This register is used to set the Thermal Alert High Value for all Thermal Sensors on the chip. PMC HW should compare the aggregated MAXTEMP against these values to cause an SMI or SCI Interrupt

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: FFh

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8:0	FFh RW	**Alert High Value (AHV):** Sets the high value for the alert indication. Temperature programmed in S9.8.0 2s complement format This register is not lockable, so that SW can change the values during runtime. NOTE: it is unsupported for SW to program TSAHV.AHV to a value lower than TSAL.ALV

4.3.51 Thermal Sensor Alert Low Value (TSALV)—Offset 1534h

This register is used to set the Thermal Alert Low Value for all Thermal Sensors on the chip. PMC HW should compare the aggregated MINTEMP against these values to cause an SMI or SCI Interrupt

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8:0	0h RW	**Alert Low Value (ALV):** Sets the low value for the alert indication. Temperature programmed in S9.8.0 2s complement format This register is not lockable, so that SW can change the values during runtime. NOTE: it is unsupported for SW to program TSALV.ALV to a value higher than TSAH.AHV

4.3.52 Thermal Alert Trip Status (TAS)—Offset 1538h

SW uses this register to determine the Thermal Alert Trip event (Low-to-High or High-to-Low) along with the Thermal Sensor ID that caused this event.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C/V	**TS Alert High-to-Low Event (AHLE):** 0x1: Indicates that an Thermal Sensor trip event occurred based on a higher to lower temperature transition thru the trip point 0x0: No trip for this event Software must write a 1 to clear this status bit Note: AHLE will not be set until there has been one occurrence of a Low to High event (ALHE must have been set once). This prevents the case where the system power up at a reasonably high temperature and starts to cool off while booting and causing an interrupt before there is SW loaded to handle it
14:12	0h RO	Reserved.
11:8	0h RO/V	**High-to-Low trip TS (HLTTS):** 0xF 0x3 : Reserved 0x2 : TS2 0x1 : TS1 0x0 : TS0
7	0h RW/1C/V	**TS Alert Low-to-High Event (ALHE):** 0x1: Indicates that an Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point 0x0: No trip for this event Software must write a 1 to clear this status bit Note: AHLE will not be set until there has been one occurrence of a Low to High event (ALHE must have been set once). This prevents the case where the system power up at a reasonably high temperature and starts to cool off while booting and causing an interrupt before there is SW loaded to handle it
6:4	0h RO	Reserved.
3:0	0h RO/V	**Low-to-High trip TS (LHTTS):** 0xF 0x3 : Reserved 0x2 : TS2 0x1 : TS1 0x0 : TS0

4.3.53 PCH Hot Level Control (PHLC)—Offset 1540h

PCH Hot Level Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**PHL Lock (PHLCLOCK):** When written to a 1, this entire register is locked and remains locked until next platform reset
30:16	0h RO	Reserved.
15	0h RW/L	**PHL Enable (PHLE):** When set and the current temperature reading, MaxTSR is greater than PHLL, then the PCHHOT# pin will be asserted (active low)
14:9	0h RO	Reserved.
8:0	0h RW/L	**PHL Level (PHLL):** Temperature value used for PCHHOT# pin assertion based on 2s complement format 0x001 positive 1oC 0x000 0oC 0x1FF negative 1oC 0x1D8 negative 40oC and so on

4.3.54 Temperature Sensor Control and Status (TSS0)—Offset 1560h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Policy Lock-Down Bit (TSS0LOCK):** When set to 1, this bit locks down the following fields: - TSS0.TSMASKEN The other bits in TSSx are anyway RO and hence do not need a lock bit set for them.Those bits become read-only . This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a global reset.
30:17	0h RO	Reserved.
16	0h RW/L	**TS MASK for MAXTEMP calculation (TSMASKEN):** 0 (Default) = Temperature reported from TS is used for temperature comparison with PMC. 1 = Temperature reported from the TS is masked for TEMP comparison within PMC. This in turn will also enable/disable SMI/SCI assertions for alert thermal events from this TS.
15:10	0h RO	Reserved.
9	0h RO/V	**TS Reading Valid (TSRV):** This bit indicates if the TS die temperature reported in valid or not.
8:0	0h RO/V	**TS Reading (TSR):** The TS die temperature with resolution of 1oC in S9.8.0 2s complement format 0x001 positive 1oC 0x000 0oC 0x1FF negative 1oC 0x1D8 negative 40oC and so on

4.3.55 Wake Alarm Device Timer: AC (WADT_AC)—Offset 1800h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**Wake Alarm Device Timer Value for AC Mode (WADT_AC_VAL):** This field contains the 32-bit wake alarm device timer value (granularity 1s) for AC power. The timer begins decrementing when written to a value other than FFFFFFFFh (regardless of the power source when the write occurs). Upon counting down to 0: - If on AC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. - If the power source is DC at this time, the status bit is not set. However, if AC power subsequently returns to the platform, the AC Expired Timer begins running. See the WADT_EXP_AC register for details. - The timer returns to its default value of FFFFFFFFh. This bit is reset by DSW_PWROK de-assertion.

4.3.56 Wake Alarm Device Timer: DC (WADT_DC)—Offset 1804h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**Wake Alarm Device Timer Value for DC Mode (WADT_DC_VAL):** This field contains the 32-bit wake alarm device timer value (granularity 1s) for DC power. The timer begins decrementing when written to a value other than FFFFFFFFh (regardless of the power source when the write occurs). Upon counting down to 0: - If on DC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. - If the power source is AC at this time, the status bit is not set. However, if DC power subsequently returns to the platform, the DC Expired Timer begins running. See the WADT_EXP_DC register for details. - The timer returns to its default value of FFFFFFFFh. This bit is reset by DSW_PWROK de-assertion.

4.3.57 Wake Alarm Device Expired Timer: AC (WADT_EXP_AC)—Offset 1808h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**Wake Alarm Device Expired Timer Value for AC Mode (WADT_EXP_AC_VAL):** This field contains the 32-bit wake alarm device "Expired Timer" value (granularity 1s) for AC power. The timer begins decrementing after switching from DC to AC power. In the case where the WADT_AC timer has already expired while the platform was on DC power, this timer only decrements while operating on AC power. So if the power source switches back to DC power, the timer will stop (but not reset). When AC power returns, the timer will again begin decrementing. Note: This timer will only begin decrementing under the conditions described above if this field has been configured for something other than its default value of FFFFFFFFh (i.e. FFFFFFFFh = disabled). Upon expiration of this timer: - If on AC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. - BOTH the AC and DC Expired Timers return to their defaults value of FFFFFFFFh. This bit is reset by DSW_PWROK de-assertion.

4.3.58 Wake Alarm Device Expired Timer: DC (WADT_EXP_DC)—Offset 180Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FFFFFFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:0	FFFFFFFFh RW/V	**Wake Alarm Device Expired Timer Value for DC Mode (WADT_EXP_DC_VAL):** This field contains the 32-bit wake alarm device "Expired Timer" value (granularity 1s) for DC power.The timer begins decrementing after switching from AC to DC power. In the case where the WADT_DC timer has already expired while the platform was on AC power, this timer only decrements while operating on DC power. So if the power source switches back to AC power, the timer will stop (but not reset). When DC power returns, the timer will again begin decrementing. Note: This timer will only begin decrementing under the conditions described above if this field has been configured for something other than its default value of FFFFFFFFh (i.e. FFFFFFFFh = disabled). Upon expiration of this timer: - If on DC power, GPE0b_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0b_EN.WADT_EN is 1. - BOTH the AC and DC Expired Timers return to their defaults value of FFFFFFFFh. This bit is reset by DSW_PWROK de-assertion.

4.3.59 Power and Reset Status (PRSTS)—Offset 1810h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	0h RW/1C/V	**Wake On LAN Override Wake Status (WOL_OVR_WK_STS):** This bit gets set when integrated LAN Signals a Power Management Event AND the system is in S5. BIOS can read this status bit to determine this wake source. Software clears this bit by writing a 1 to it.
4:1	0h RO	Reserved.
0	0h RW/1C/V	**ME_HOST_WAKE_STS (ME_HOST_WAKE_STS):** This bit is set when the ME generates a non-maskable wake event and is not affected by any other enable bit. When this bit is set, the host power management logic wakes to S0.

4.3.60 Power Management Configuration Reg 1 (PM_CFG)—Offset 1818h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 20h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	Reserved.
25	0h RW	**Allow USB2 PHY Core Power Gating (ALLOW_USB2_CORE_PG):** When this bit is '0' (default), USB2 PHY power gating is disabled. When this bit is '1', USB2 PHY power gating can occur if all other required conditions are met.
24	0h RW/L	**Energy Reporting Lock (ER_LOCK):** When this bit is written to 1, it will remain 1 until the next host_prim_rst_b assertion. While this bit is 1, GEN_PMCON_A.ER_EN value cannot be changed. BIOS should write 1b1 to this bit only AFTER writing to GEN_PMCON_A.ER_EN.
23:22	0h RO	Reserved.
21	0h RW	**RTC Wake from DeepSx Disable (RTC_DSX_WAKE_DIS):** When set, this bit disables RTC wakes from waking the system from DeepSx. This bit is reset by RTCRST# assertion.
20	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
19:18	0h RW/L	**SLP_SUS# Minimum Assertion Width (SLP_SUS_MIN_ASST_WDTH):** This 2-bit value indicates the minimum assertion width of the SLP_SUS# signal to guarantee that the SUS well power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00 = 0 ms (i.e. stretching disabled - default) 01 = 500ms 10 = 1s 11 = 4s This field is not writable when the SLP_Sx# Stretching Policy Lock- Down bit is set. This field is ignored when exiting a G3 state if the "Disable SLP_X Stretching After SUS Power Failure" bit is set. Note that unlike with all other SLP_* pin stretching, this disable bit only impacts SLP_SUS# stretching during G3 exit rather than both G3 and DeepSx exit. SLP_SUS# stretching always applies to DeepSx regardless of the disable bit. Programming Note: For platforms that enable DeepSx, BIOS must program SLP_SUS# stretching to be greater than or equal to the largest stretching value on any other SLP_* pin (SLP_S3#, SLP_S4#, SLP_LAN#, or SLP_A#). This bit is cleared by the RTCRST# pin.
17:16	0h RW/L	**SLP_A# Minimum Assertion Width (SLP_A_MIN_ASST_WDTH):** This 2-bit value indicates the minimum assertion width of the SLP_A# signal to guarantee that the ASW power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00 = 0 ms (i.e. stretching disabled - default) 01 = 4 s 10 = 98 ms 11 = 2 s This field is not writable when the SLP_Sx# Stretching Policy Lock- Down bit is set. This field is ignored when exiting a G3 or Deep Sx state if the "Disable SLP_X Stretching After SUS Power Failure" bit is set. This bit is cleared by the RTCRST# pin.
15:14	0h RW/L	**SLP_LAN# Minimum Assertion Width (SLP_LAN_MIN_ASST_WDTH):** This 2-bit value indicates the minimum assertion width of the SLP_LAN# signal to guarantee that the power to the PHY has been fully power-cycled. This value may be modified per platform depending on power supply, capacitance, board capacitance, power failure detection circuits, etc. This field is not writable when the SLP_Sx# Stretching Policy Lock Down bit is set to 1. This bit is reset by RTCRST# assertion.
13	0h RW	**After G3 Last State Enable (AG3_LS_EN):** When PM_CFG.AG3E is '0', AG3_LS_EN determines whether the PCH will consider the platform's previous state when determining whether to power-up after G3. Encodings: 0: PCH power-up policies after G3 do not depend on the platform's state when the G3 occurred. (default) 1: PCH power-up policies after G3 depend on the platform's state when the G3 occurred. - If the power failure occurred while the platform was in S0 or while in the process of going to S0, the platform will power-up to S0 upon exiting G3. - If the power failure occurred while the platform was in Sx or while in the process of going to Sx, the platform will stay in S4/S5 upon exiting G3. Note: This bit applies only when GEN_PMCON_3.AG3E is '0'. If AG3E is '1', the platform will always stay in S4/S5 after G3 regardless of the value of AG3_LS_EN.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**After Type 8 Global Reset Last State Enable (A8GR_LS_EN):** AGR_LS_EN determines whether the PCH will consider the platform's previous state when determining whether to power-up after non-thermal and non-explicitly requested type 8 global resets. Encodings: 0 (default): PCH power-up policies after a global reset do not depend on the platform's state when the reset occurred. 1: PCH power-up policies after a global reset depend on the platform's state when the reset occurred. If the global reset occurred while the platform was in S0 or while in the process of going to S0, the platform will power-up to S0 after the reset. If the global reset occurred while the platform was in Sx or while in the process of going to Sx, the platform will stay in S5 upon exiting G3.
11	0h RO	Reserved.
10	0h RW	**Power Button Debounce Mode (PB_DB_MODE):** This bit controls when interrupts (SMI#, SCI) are generated in response to assertion of the PWRBTN# pin. This bit's values cause the following behavior: - '0': The 16ms debounce period applies to all usages of the PWRBTN# pin (legacy behavior). - '1': When a falling edge occurs on the PWRBTN# pin, an interrupt is generated and the 16ms debounce timer starts. Subsequent interrupts are masked while the debounce timer is running. Note: Power button override logic always samples the post-debounce version of the pin. This bit is reset by RTCRST# assertion.
9:8	0h RW/L	**Reset Power Cycle Duration (PWR_CYC_DUR):** The value in this register determines the minimum time a platform will stay in reset (SLP_S3#, SLP_S4#, SLP_S5# asserted and also SLP_A# and SLP_LAN# asserted if applicable) during a host partition reset with power cycle or a global reset. The duration programmed in this register takes precedence over the applicable SLP_# stretch timers in these reset scenarios. This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. Note that the duration programmed in this register should never be smaller than the stretch duration programmed in the following registers - - GEN_PMCON_3.SLP_S3_MIN_ASST_WDTH - GEN_PMCON_3.S4MAW - PM_CFG.SLP_A_MIN_ASST_WDTH - PM_CFG.SLP_LAN_MIN_ASST_WDTH This bit is reset by RTCRST# assertion. 00 = 4 - 5 seconds 01 = 3 - 4 seconds 10 = 2 - 3 seconds 11 = 1 - 2 seconds
7:6	0h RO	Reserved.
5	1h RW/V	**CPU OC Strap (COCS):** SW programs this pin with the value that should be reflected to the GPIO8_OCS pin, when the pin is in native mode. Hardware also sets this bit when the over-clocking watchdog timer expires. This bit is reset by RSMRST# assertion.

Bit Range	Default & Access	Field Name (ID): Description
4:3	0h RO	Reserved.
2	0h RW/L	**Energy Reporting Enable (ER_EN):** When this bit is 1, the PCH will periodically calculate and report its energy consumption to the CPU via PM_SYNC. When this bit is 0, the PCH will neither calculate nor report its energy consumption.
1:0	0h RW/V	**Timing t581 (TIMING_T581):** This field configures the t581 timing involved in the power down flow (CPUPWRGD inactive to ICC_ICLK_INIT inactive). Encodings (all min timings): 00: 10 us (default) 01: 100 us 10: 1 ms 11: 10 ms reset_type=host_deep_rst_b

4.3.61 S3 Power Gating Policies (S3_PWRGATE_POL)—Offset 1828h

This register contains policy bits to configure various power gating options while the system is in S3. Note that setting any of these policies to "enabled" may not directly result in power gating - in some cases other HW qualifications may be dynamically applied.
This register is in the RTC power well and is reset by RTCRST# assertion.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**S3 Power Gate Enable in DC Mode: SUS Well (S3DC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S3 while operating on DC power (based on the AC_PRESENT pin value).
0	0h RW	**S3 Power Gate Enable in AC Mode: SUS Well (S3AC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S3 while operating on AC power (based on the AC_PRESENT pin value).

4.3.62 S4 Power Gating Policies (S4_PWRGATE_POL)—Offset 182Ch

This register contains policy bits to configure various power gating options while the system is in S4. Note that setting any of these policies to "enabled" may not directly result in power gating - in some cases other HW qualifications may be dynamically applied.
This register is in the RTC power well and is reset by RTCRST# assertion.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**S4 Power Gate Enable in DC Mode: SUS Well (S4DC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S4 while operating on DC power (based on the AC_PRESENT pin value).
0	0h RW	**S4 Power Gate Enable in AC Mode: SUS Well (S4AC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S4 while operating on AC power (based on the AC_PRESENT pin value).

4.3.63 S5 Power Gating Policies (S5_PWRGATE_POL)—Offset 1830h

This register contains policy bits to configure various power gating options while the system is in S5. Note that setting any of these policies to "enabled" may not directly result in power gating - in some cases other HW qualifications may be dynamically applied.
This register is in the RTC power well and is reset by RTCRST# assertion.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**S5 Power Gate Enable in DC Mode: SUS Well (S5DC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S5 while operating on DC power (based on the AC_PRESENT pin value).
14	0h RW	**S5 Power Gate Enable in AC Mode: SUS Well (S5AC_GATE_SUS):** A '1' in this bit enables power gating of the SUS well in S5 while operating on AC power (based on the AC_PRESENT pin value).
13:0	0h RO	Reserved.

4.3.64 DeepSx Configuration (DSX_CFG)—Offset 1834h

This register contains misc. fields used to configure the PCH's power management behavior.
This register is in the RTC power well and is reset by RTCRST# assertion.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW	**Require CNV Wake Disabled for DeepSx Entry/SUSPWRDNACK (REQ_CNV_NOWAKE_DSX):** If this bit is 0, the state of connectivity wake enable is not considered when making DeepSx entry decisions. If this bit is 1, connectivity wake must be disabled to allow DeepSx entry or SUSPWRDNACK assertion, and even then all other conditions must be satisfied.
3	0h RW	**Require BATLOW# Assertion for DeepSx Entry/SUSPWRDNACK (REQ_BATLOW_DSX):** If this bit is 0, the state of the BATLOW# pin is not considered when making DeepSx entry and SUSPWRDNACK decisions. If this bit is 1, BATLOW# must be asserted to allow DeepSx entry or SUSPWRDNACK assertion, and even then all other entry conditions must be satisfied.
2	0h RW	**WAKE# Pin DeepSx Enable (WAKE_PIN_DSX_EN):** When this bit is 1, the PCI Express WAKE# pin is monitored while in Deep Sx, supporting waking from Deep Sx due to assertion of this pin. In this case, the platform must externally pull up the pin to the DSW (instead of pulling up to the SUS as has historically been the case). When this bit is 0: - DeepSx enabled configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. -Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled Note: Deep Sx disabled configurations must leave this bit at 0.
1	0h RW	**AC_PRESENT Pin Pulldown in DeepSx Disable (ACPRES_PD_DSX_DIS):** When this bit is 1, the internal pull-down on the ACPRESENT pin is disabled. However, the pulldown is not necessarily enabled if the bit is '0'. This bit must be left at '0' for Deep Sx disabled configurations, and the pulldown is disabled for those configurations even though the bit is '0'. To support Intel (R) CSME wakes from Deep Sx, the pin is always monitored regardless of the value of this host policy bit. When this bit is '0': DeepSx enabled configurations: The PCH internal pull-down on ACPRESENT is enabled in Deep Sx and during G3 exit. Deep Sx disabled configurations: The PCH internal pull-down on ACPRESENT is always disabled.
0	0h RW	**LANWAKE Pin DeepSx Enable (LANWAKE_PIN_DSX_EN):** When this bit is 1, the LANWAKE pin is monitored while in DeepSx, supporting waking from DeepSx due to assertion of this pin. In this case, the platform must drive the pin to the correct value while in DeepSx. DeepSx disabled configurations must leave this bit at 0. When this bit is 0: DeepSx enabled configurations: The PCH internal pull-down on LANWAKE pin is enabled in deep-Sx and during G3 exit and the pin is not monitored during this time. DeepSx disabled configurations: The PCH internal pull-down is never enabled

4.3.65 Power Management Configuration Reg 2 (PM_CFG2)—Offset 183Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**Power Button Override Period (PBOP):** This field determines, while the power button remains asserted, how long the PMC will wait before initiating a global reset. Encoding: 000b - 4 seconds 001b - 6 seconds 010b - 8 seconds 011b - 10 seconds 100b - 12 seconds 101b - 14 seconds Others - Reserved This bit is reset by DSW_PWROK de-assertion.
28	0h RW/L	**Power Button Native Mode Disable (PB_DIS):** When this bit is '0' (default), the PMC's power button logic will act upon the input value from the GPIO unit, as normal. When this bit is set to '1', the PMC must force its internal version of the power button pin to '1'. This will result in the PMC logic constantly seeing the pin as de-asserted. This bit is reset by RTCRST# assertion.
27	0h RO	Reserved.
26	0h RW/V	**DRAM_RESET# Control (DRAM_RESET_CTL):** BIOS uses this bit to control the DRAM_RESET# pin from the PCH, which is routed to the reset pin on the DRAM. Encoding: 0 = DRAM_RESET# output is asserted (driven low) 1 = DRAM_RESET# output is tri-stated. Note: This bit is cleared to '0' by HW when SLP_S4# goes low. This bit is reset by DSW_PWROK de-assertion.
25:0	0h RO	Reserved.

4.3.66 PM_SYNC Miscellaneous Configuration (PM_SYNC_MISC_CFG)—Offset 18C8h

This register is used to configure miscellaneous aspects of the PM_SYNC pin.
This register is in the CORE power well and is reset by PLTRST#.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW/L	**GPIO_D Pin Selection (GPIO_D_SEL):** There are two possible GPIOs that can be routed to the GPIO_D PM_SYNC state. This bit selects between them: 0: CPU_GP_3 (default) 1: CPU_GP_2 This field is not writeable when PM_SYNC_LOCK=1.
10	0h RW/L	**GPIO_C Pin Selection (GPIO_C_SEL):** There are two possible GPIOs that can be routed to the GPIO_C PM_SYNC state. This bit selects between them: 0: CPU_GP_0 (default) 1: CPU_GP_1 This field is not writeable when PM_SYNC_LOCK=1.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/L	**GPIO_B Pin Selection (GPIO_B_SEL):** There are two possible GPIOs that can be routed to the GPIO_B PM_SYNC state. This bit selects between them: 0: CPU_GP_2 (default) 1: CPU_GP_0 This field is not writeable when PM_SYNC_LOCK=1.
8	0h RW/L	**GPIO_A Pin Selection (GPIO_A_SEL):** There are two possible GPIOs that can be routed to the GPIO_A PM_SYNC state. This bit selects between them: 0: CPU_GP_1 (default) 1: CPU_GP_3 This field is not writeable when PM_SYNC_LOCK=1.
7:0	0h RO	Reserved.

4.3.67 Chipset Initialization Register E0 (CIRE0)—Offset 18E0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Host Wireless LAN Phy Power Enable (HOST_WLAN_PP_EN):** This policy bit is set by Host software when it desires the wireless LAN PHY to be powered in Sx power states for wakes over wireless LAN (WoWLAN). This bit is reset by DSW_PWROK de-assertion.
16	0h RW	**Deep-Sx WLAN Phy Power Enable (DSX_WLAN_PP_EN):** When set to '1, PMC will keep SLP_WLAN# high in deep-Sx to enable WoWLAN. Note: 1. This policy bit will be applied for Deep Sx entry from S3, S4 and S5. 2. This bit does not affect SLP_WLAN# behaviour in Sx after G3 or after a global reset 3. HOST_WLAN_PP_EN must be set when this bit is set. This bit is reset by DSW_PWROK de-assertion.
15:0	0h RO	Reserved.

4.3.68 CPU Early Power-on Configuration (CPU_EPOC)—Offset 18ECh

CPU Early Power on Configuration

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21:20	0h RO/V	**Crystal Frequency[2:1] (XTAL_FREQ_MSB):** Along with XTAL_FREQ_LSB the 3 bit field reflects the frequency of the crystal (aka NSSC) clock used by the CPU and PCH Encoding: 000b -24MHz 001b -19.Mhz 010b -38.4 Mhz Others - Reserved
19:18	0h RO	Reserved.
17	0h RO/V	**Crystal Frequency [0] (XTAL_FREQ_LSB):** See XTAL_FREQ_MSB
16:8	0h RO	Reserved.
7:3	0h RW/L	**EPOC Data [7:3] (EPOC_DATA_7_3):** EPOC Data [7:3]
2	0h RO	Reserved.
1:0	0h RW/L	**EPOC Data [1:0] (EPOC_DATA_1_0):** EPOC Data [1:0]

4.3.69 ACPI Timer Control (ACPI_TMR_CTL)—Offset 18FCh

This register allows software to disable the ACPI Timer, which could result in power savings for the PCH.
This register is in the CORE power well and is reset by PLTRST#

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**ACPI Timer Disable (ACPI_TIM_DIS):** This bit determines whether the ACPI Timer is enabled to run. - 0: ACPI Timer is enabled (default) - 1: ACPI Timer is disabled (halted at the current value) Even when enabled, the timer only runs during S0. This bit must only be set to "1" if the operating system can tolerate disabling the 14.31818 MHz ACPI PM Timer. Note: 1.Some operating systems may only tolerate disabling the timer during entry into deep idle states. In such cases, the bit must be set to "1" during entry into those states and cleared to "0" during exit. This bit is reset by PLTRST# assertion.
0	0h RW/1S/V	**ACPI Timer Clear (ACPI_TIM_CLR):** Writing a 1 to this bit will clear the ACPI Timer to all 0s. Hardware will automatically clear the bit back to 0 once the timer clear operation has completed. Writing a 0 to this bit has no effect. The PCH is capable of honoring this bit even while ACPI_TIM_DIS=1. This bit is reset by PLTRST# assertion.

4.3.70 Last TSC Alarm Value[31:0] (TSC_ALARM_LO)—Offset 1910h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Last TSC Alarm Value [31:0] (TSC_ALARM_VAL_LO):** This field contains bits 31:0 of the last TSC alarm value received from the CPU. This field is reset by PLTRST# assertion.

4.3.71 Last TSC Alarm Value[63:32] (TSC_ALARM_HI)—Offset 1914h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Last TSC Alarm Value [63:32] (TSC_ALARM_VAL_HI):** This field contains bits 63:32 of the last TSC alarm value received from the CPU. This field is reset by PLTRST# assertion.

4.3.72 GPIO Configuration (GPIO_CFG)—Offset 1920h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 432h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
11:8	4h RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[87:64]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[67:66]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[87:64]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[71:64]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[75:64]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[71:64]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[87:64]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[83:64]; other GPE bits not used. 8h = GPP_U[5:4] mapped to GPE[69:68]; other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[87:64]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[87:64]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[87:64]; other GPE bits not used. Dh - Fh = Reserved
7:4	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[55:32]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[35:34]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[55:32]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[39:32]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[43:32]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[39:32]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[55:32]; other GPE bis not used. 7h = GPP_D[19:0] mapped to GPE[41:32]; other GPE bits not used. 8h = GPP_U[5:4]mapped to GPE[36:35]; other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[55:32]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[55:32]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[55:32]; other GPE bits not used. Dh - Fh = Reserved
3:0	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[23:0]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[3:2]; other GPE bits not used 2h = GPP_A[23:0] mapped to GPE[23:0]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[7:0]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[11:0]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[7:0]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[23:0]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[19:0]; other GPE bits not used. 8h = GPP_U[5:4] mapped to GPE[5:4]; other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[23:0]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[23:0]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[23:0]; other GPE bits not used. Dh - Fh = Reserved

4.3.73 Global Reset Causes (GBLRST_CAUSE0)—Offset 1924h

This register logs causes of host partition resets.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW/1C/V	**PMC RF FUSA Error Global Reset (PMC_RF_FUSA_ERROR):** This bit is set to 1 by hardware if an MBIST error is detected from any RFs during FUSA Power-On Self Test.
23:17	0h RO	Reserved.
16	0h RW/1C/V	**CPU Thermal Runaway Watchdog Timer (CPU_THRM_WDT):** This bit is set to '1' by hardware when a global reset is triggered by the expiration of the CPU Thermal Runaway Watchdog Timer.
15:13	0h RO	Reserved.
12	0h RW/1C/V	**SYS_PWROK Failure (SYSPWR_FLR):** This bit is set to '1' by hardware when a global reset is triggered by an unexpected loss of SYS_PWROK. This bit is reset by DSW_PWROK de-assertion.
11	0h RW/1C/V	**PCH_PWROK Failure (PCHPWR_FLR):** This bit is set to '1' by hardware when a global reset is triggered by an unexpected loss of PCH_PWROK. This bit is reset by DSW_PWROK de-assertion.
10	0h RW/1C/V	**PMC Firmware Global Reset (PMC_FW):** This bit is set to '1' by hardware when a global reset is triggered by a request from PMC firmware (i.e. a write of '1' to the GBLRST_CTL.TRIG_GBL bit).
9:6	0h RO	Reserved.
6	0h RW/1C/V	**ME-Initiated Global Reset (ME_GBL):** This bit is set to'1' by hardware when a global rest is triggered by Intel ME FW. This bit is reset DSW_PWROK de-assertion.
5	0h RW/1C/V	**CPU Thermal Trip (CPU_TRIP):** This bit is set to '1' by hardware when a global reset is triggered by a CPU thermal trip event (i.e. an assertion of the THRMTRIP# pin).
4	0h RO	Reserved.
3	0h RW/1C/V	**PCH Catastrophic Temperature Event (ICH_CAT_TMP):** This bit is set to '1 by hardware when a global reset is triggered by a catastrophic temperature event from the ICH internal thermal sensor.
2	0h RO	Reserved.
1	0h RW/1C/V	**Power Button Override (PB_OVR):** This bit is set to '1' by hardware when a global reset is triggered by a power button override (i.e. an assertion of the PWRBTN# pin for 5 seconds). This bit is reset by DSW_PWROK de-assertion.
0	0h RO	Reserved.

4.3.74 Global Reset Causes Register 1 (GBLRST_CAUSE1)—Offset 1928h

This register logs causes of host partition resets.

Access Method

Type: MEM Register (Size: 32 bits)

Device:

Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9	0h RW/1C/V	**eSPI Initiated Type 8 Global Reset (ESPI_TYPE8):** This bit is set to '1' by hardware when a shutdown is requested via eSPI
8	0h RW/1C/V	**eSPI Initiated Type 7 Global Reset (ESPI_TYPE7):** This bit is set to '1' by hardware when a global reset is requested via eSPI
7:6	0h RO	Reserved.
5	0h RW/1C/V	**Intel (R) CSME Set Power Button Status (ME_SET_PBO_STS):** If this bit is set, the cause of the previous global reset was Intel (R) CSME FW setting the power button override status. This bit is reset by DSW_PWROK de-assertion.
4	0h RO	Reserved.
3	0h RW/1C/V	**Host SMBus Message (HSMB_MSG):** If this bit is set, the cause of the previous global reset was a global reset request received over the host SMBus interface.
2	0h RW/1C/V	**Host Partition Reset Promotion (HOST_RST_PROM):** If this bit is set, the cause of the previous global reset was a host partition reset that was promoted to a global reset either due to Intel CSME or host policy. This bit is reset by DSW_PWROK de-assertion.
1	0h RO	Reserved.
0	0h RW/1C/V	**Host Partition Reset Timeout (HOST_RESET_TIMEOUT):** If this bit is set, the cause of the previous global reset was an expiration of the timer that runs during host partition resets. This bit is reset by DSW_PWROK de-assertion.

4.3.75 Host Partition Reset Causes (HPR_CAUSE0)—Offset 192Ch

This register logs causes of host partition resets.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RO/V	**eSPI Host Reset With Power Cycle (ESPI_HRWPC):** eSPI requested host partition reset with power cycle.
16	0h RO/V	**eSPI Host Reset Without Power Cycle (ESPI_HRWOPC):** eSPI requested host partition reset without power cycle
15:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO/V	**Host SMBUS Host Reset With Power Cycle (HSMB_HRPC):** SMBus initiated host partition reset with power cycle.
12	0h RO/V	**Host SMBUS Host Reset Without Power Cycle (HSMB_HR):** SMBus initiated host partition reset without power cycle.
11	0h RO	Reserved.
10	0h RO/V	**Intel CSME-Initiated Host Reset With Power Down (MI_HRPD):** Intel CSME initiated host reset with power down.
9	0h RO/V	**Intel (R) CSME-Initiated Host Reset With Power Cycle (MI_HRPC):** Intel CSME initiated host reset with power cycle.
8	0h RO/V	**Intel CSME-Initiated Host Reset Without Power Cycle (MI_HR):** Intel CSME initiated host reset without power cycle.
7	0h RO	Reserved.
6	0h RO/V	**Host TCO Watchdog Timer Second Expiration (TCO_WDT):** Host TCO watchdog timer reached zero for the second time.
5:3	0h RO	Reserved.
2	0h RO/V	**SYS_RESET# (SYSRST_ES):** Assertion of the SYS_RESET# pin after the 16 ms HW debounce.
1	0h RO/V	**Write to CF9 (CF9_ES):** This bit will be set when Host software writes a value of 6h or Eh to the CF9 register. Note: The shutdown special cycle from the CPU will also set this bit.
0	0h RO	Reserved.

4.3.76 LATENCY_LIMIT_RESIDENCY_0 (LAT_LIM_RES_0)—Offset 1930h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**LATENCY_LIMIT_RESIDENCY (LLR0):** This field contains the amount of time (in 100us granularity) for the corresponding 0/1/2 counter in the LATENCY_LIMIT_CONTROL register that the appropriate counter is limiting the memory LTR request to the CPU. Note that this counter can wrap and that should not be of any concern. This register will reset to 0 anytime the corresponding enable for the register transitions from a 0->1. Note that on a 1->0 transition, the counter should hold its previous value

4.3.77 LATENCY_LIMIT_RESIDENCY_1 (LAT_LIM_RES_1)—Offset 1934h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**LATENCY_LIMIT_RESIDENCY (LLR1):** This field contains the amount of time (in 100us granularity) for the corresponding 0/1/2 counter in the LATENCY_LIMIT_CONTROL register that the appropriate counter is limiting the memory LTR request to the CPU. Note that this counter can wrap and that should not be of any concern. This register will reset to 0 anytime the corresponding enable for the register transitions from a 0->1. Note that on a 1->0 transition, the counter should hold its previous value

4.3.78 LATENCY_LIMIT_RESIDENCY_2 (LAT_LIM_RES_2)—Offset 1938h

LATENCY_LIMIT_RESIDENCY_2

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**LATENCY_LIMIT_RESIDENCY (LLR2):** This field contains the amount of time (in 100us granularity) for the corresponding 0/1/2 counter in the LATENCY_LIMIT_CONTROL register that the appropriate counter is limiting the memory LTR request to the CPU. Note that this counter can wrap and that should not be of any concern. This register will reset to 0 anytime the corresponding enable for the register transitions from a 0->1. Note that on a 1->0 transition, the counter should hold its previous value

4.3.79 SLP S0 RESIDENCY (SLP_S0_RES)—Offset 193Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**Residency In S0 (RESIDENCY_IN_S0):** This field contains the amount of time that the SLP_S0# has been asserted. Note that this counter can wrap. The timer counts with 122 us granularity.

4.3.80 Latency Limit Control (LLC)—Offset 1940h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22	0h RW	**CTR2_ENABLE (CTR2_ENABLE):** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0
21	0h RW	**CTR2_EA_CTL (CTR2_EA_CTL):** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0
20:16	0h RW	**CTR2_DEVICE (CTR2_DEVICE):** Encoding of the LTR device to be monitored 0 - PCIe SPA 1 - PCIe SPB 2 - PCIe SPC 3 - SATA 4 - GbE 5 - xHCI 6 - Intel CSME 7 - Reserved 8 - Intel HD Audio 9 - eSPI 10 - I2C, UART, GSPI 11 - PCIe SPD 12:13 - Reserved 14 - SDXC 15 - ISH 16 - CNVi 17 - eMMC
15	0h RO	Reserved.
14	0h RW	**CTR1_ENABLE (CTR1_ENABLE):** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0
13	0h RW	**CTR1_EA_CTL (CTR1_EA_CTL):** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0

Bit Range	Default & Access	Field Name (ID): Description
12:8	0h RW	**CTR1_DEVICE (CTR1_DEVICE):** Encoding of the LTR device to be monitored 0 - PCIe SPA 1 - PCIe SPB 2 - PCIe SPC 3 - SATA 4 - GbE 5 - xHCI 6 - Intel CSME 7 - Reserved 8 - Intel HD Audio 9 - eSPI 10 - I2C, UART, GSPI 11 - PCIe SPD 12:13 - Reserved 14 - SDXC 15 - ISH 16 - CNVi 17 - eMMC
7	0h RO	Reserved.
6	0h RW	**CTR0_ENABLE (CTR0_ENABLE):** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0
5	0h RW	**CTR0_EA_CTL (CTR0_EA_CTL):** Control for counting only if EA=0 0 Count always (EA=0 or 1) 1 Count only if in a state where EA=0
4:0	0h RW	**CTR0_DEVICE (CTR0_DEVICE):** Encoding of the LTR device to be monitored 0 - PCIe SPA 1 - PCIe SPB 2 - PCIe SPC 3 - SATA 4 - GbE 5 - xHCI 6 - Intel CSME 7 - Reserved 8 - Intel HD Audio 9 - eSPI 10 - I2C, UART, GSPI 11 - PCIe SPD 12:13 - Reserved 14 - SDXC 15 - ISH 16 - CNVi 17 - eMMC

4.3.81 Chipset Initialization Register B1C (CPPMVRIC)—Offset 1B1Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**CSME Power Gated Qualification Disable (MEPGQDIS):** 0 = SLP_S0# assertion requires CSME to be power gated 1 = SLP_S0# assertion does not require CSME to be power gated
30	0h RW	**GbE Disconnected Qualification Disable (GBEDISCQDIS):** 0 = SLP_S0# assertion requires GbE LAN to be disconnected 1 = SLP_S0# assertion does not require GbE LAN to be disconnected
29	0h RW	**Audio DSP is in D3 Qualification Disable (ADSPD3QDIS):** 0 = SLP_S0# assertion requires the Audio DSP controller to be in D3 1 = SLP_S0# assertion does not require the Audio DSP controller to be in D3
28	0h RW	**XHCI is in D3 Qualification Disable (XHCID3QDIS):** 0 = SLP_S0# assertion requires the XHCI controller to be in D3 1 = SLP_S0# assertion does not require the XHCI controller to be in D3
27	0h RW	**LPIO is in D3 Qualification Disable (LPIOD3QDIS):** 0 = SLP_S0# assertion requires LPIO controllers to be in D3 1 = SLP_S0# assertion does not require LPIO controllers to be in D3
26	0h RW	**Thermal Sensor Disable Qualification Disable (TSDQDIS):** 0 = SLP_S0# assertion requires the thermal sensor to be disabled 1 = SLP_S0# assertion does not require the thermal sensor to be disabled
25	0h RW	**ICC PLL Wake Block Enable (ICCPLLWBE):** 0 = PMC HW never blocks ICLK PLL from being re-enabled during a dynamic ICC PLL shutdown event. 1 = PMC HW blocks ICLK PLL from being re-enabled for any reason following a dynamic ICC PLL shutdown event while SLP_S0# assertion conditions are met and until VR idle mode exit timer expires after SLP_S0# de-assertion.
24	0h RO	Reserved.
23	0h RW	**Power Ungate Block Enable (PUGBEN):** 0 = PMC HW does not block Intel(R)CSME and HSIO Power from being restored upon being requested to do so while SLP_S0# assertion conditions are met and until VR idle mode exit timer expires after SLP_S0# de-assertion. 1 = PMC HW blocks Intel(R)CSME and HSIO Power from being restored upon being requested to do so while SLP_S0# assertion conditions are met and until VR idle mode exit timer expires after SLP_S0# de-assertion.
22	0h RW	**24MHz Crystal Shutdown Qualification Disable (XTALSDQDIS):** 0 = SLP_S0# assertion requires the 24MHz Crystal Oscillator to be shutdown. Once SLP_S0# is asserted, the Crystal oscillator should be kept off until PMC notifies it is allowed to be re-enabled. 1 = SLP_S0# assertion does not require the 24MHz Crystal to be shutdown.
21:16	0h RW	**SRC[5:0]CLKRQ# VR Idle Enable (CLKRQ_VRI_EN):** Each bit in this register deterimes whether the corresponding PCIe clock request pin (SRC[bit #]CLKRQ#) is enabled as a VR Idle break event / entry inhibitor. For example, if CLKRQ_VRI_EN[0] = '1' then SRC0CLKRQ# must be a '1' in order for SLP_S0# to be asserted and if SRC0CLKRQ# goes to '0' then it will cause SLP_S0# to be deasserted. On the other hand, if CLKRQ_VRI_EN[0] = '0' then the state of SRC0CLKRQ# has no impact on SLP_S0#.
15	0h RW/V	**Global SLP_S0# (VR Idle) Enable (GSLPS0EN):** 0 = CPPMVRIC-based SLP_S0# HW functionality is disabled (controlled by the LPM*_ACT_*.ASSERT_SLPS0 bits). 1 = CPPMVRIC-based SLP_S0# HW functionality is enabled (the LPM*_ACT_*.ASSERT_SLPS0 bits have no impact on the SLP_S0# pin). When GSLPS0EN = 0, SLP_S0# is always driven based on the 'Low power mode actions' registers, except if being overridden by PMC FW.
14	0h RO	Reserved.
13	0h RW	**SLP_S0# Low Voltage Mode Enable (SLPS0LVEN):** 0 = high speed ring oscillator (>24 MHz) clocks are allowed to run when SLP_S0#=0 1 = high speed ring oscillator (>24 MHz) clocks are not allowed to run when SLP_S0#=0. The PMC prevent ungating of these clock domains while SLP_S0#=0.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**Intel (R) Trace Hub AON Active Request Qualification Disable (NPKAONACTREQQDIS):** 0 = SLP_S0# assertion requires Intel(R) Trace Hub not to be requesting AON active 1 =SLP_S0# assertion does not require Intel(R) Trace Hub not to be requesting AON active.
11:9	0h RW	**SLP_S0# Minimum Assertion Width (SLP_S0_MIN_ASST_WDTH):** 000 = 30.5us 001 = 61us 010 = 91.5us 011 = 122us 100 = 152.5us 101 = 183us 110 = 500us 111 = 1ms
8:0	0h RW	**SLP_S0# De-assertion Exit Latency (SLP_S0_EXIT_LAT):** This value is used in the SLP_S0# exit timer and has an RTC clk period (30.5us) granularity. 000h = 0us (reserved) 001h = 30.5us 002h = 61us 003h = 91.5us 1FFh = 15.6ms

4.3.82 Chipset Initialization Register B24 (CIRB24)—Offset 1B24h

BIOS may program this register.

4.3.83 Chipset Initialization Register 340 (CIRB40)—Offset 1B40h

BIOS may program this register.

4.3.84 Chipset Initialization Register B44 (CIRB44)—Offset 1B44h

BIOS may program this register.

4.3.85 Chipset Initialization Register 34C (CIR34C)—Offset 1B4Ch

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 2000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**PCIe Root Ports Low Voltage Qualification Disable (PCIELVQDIS):** 0 = SLP_S0# assertion requires all PCIe ports and their controllers to allow for Low Voltage mode entry. 1 = SLP_S0# assertion does not require all PCIe ports and their controllers to allow for Low Voltage mode entry
30	0h RW	**SATA Controller in D3 Qualification Disable (SATAD3QDIS):** 0 = SLP_S0# assertion requires the SATA controller to be in D3 1 = SLP_S0# assertion does not require the SATA controller to be in D3
29	0h RW	**USB Device in D3 Qualification Disable (USBDEVD3QDIS):** 0 = SLP_S0# assertion requires the USB Device controller to be in D3 1 = SLP_S0# assertion does not require the USB Device controller to be in D3
28:26	0h RO	Reserved.
25	1h RW	**Connectivity Vnn Request Qualification Disable (CNVIVNNREQQDIS):** 0 = SLP_S0# assertion requires CNVi not to be requesting Vnn active 1 = SLP_S0# assertion does not require CNVi not to be requesting Vnn active
24	0h RO	Reserved.
23	0h RW	**HPET 24MHz Clk Request Qualification Disable (HPET24CLKREQQDIS):** 0 = SLP_S0# assertion requires the HPET 24MHz clkreq to be low 1 = SLP_S0# assertion does not require the HPET 24MHz clkreq to be low
22	0h RW	**Audio DSP ROSC Off Qualification Disable (ADSPROSCOFFQDIS):** 0 = SLP_S0# assertion requires the Audio DSP ROSC to be off 1 = SLP_S0# assertion does not require the Audio DSP ROSC to be off
21	0h RW	**HSIO Core Power Gated Qualification Disable (HSIOCPGQDIS):** 0 = SLP_S0# assertion requires all lanes of the HSIO Core Power Domain to be gated. 1 = SLP_S0# assertion does not require all lanes of the HSIO Core Power Domain to be gated.
20	0h RW	**USB2 PLL is off Qualification Disable (USB2PLLSDQDIS):** 0 = SLP_S0# assertion requires the USB2 PLL to be shut down. 1 = SLP_S0# assertion does not require the USB2 PLL to be shut down.
19	0h RW	**Audio PLL is off Qualification Disable (APLLSDQDIS):** 0 = SLP_S0# assertion requires the Audio PLL to be shut down. 1 = SLP_S0# assertion does not require the Audio PLL to be shut down.
18	0h RW	**IsCLK PLL Shutdown Qualification Disable (ICCPLLSDQDIS):** 0 = SLP_S0# assertion requires the IsCLK PLL to be shut down. 1 = SLP_S0# assertion does not require the IsCLK PLL to be shut down.
17	0h RW	**CPU in C10 Qualification Disable (CPUC10QDIS):** 0 = SLP_S0# assertion requires the CPU to be in a C10 state. 1 = SLP_S0# assertion does not require the CPU to be in a C10 state.
16:0	0h RO	Reserved.

4.3.86 CWB MDID Status Register (CWBMDIDSTATUS)—Offset 1BD4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**CWB Status (CWB_STS):** When set , DMI Central Write Buffer is enabled. 1: CWB on 0: CWB off
30:18	0h RO	Reserved.
17:9	0h RW/V	**DMI MDID Value (DMI_MDID):** DMI sent MDID value.
8:0	0h RW/V	**CNVi MDID Value (CNVI_MDID):** CNVi sent MDID value. Note: this is used for CNVi WIFI

4.3.87 ACPI Control (ACTL)—Offset 1BD8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**ACPI Enable (EN):** When set, decode of the I/O range pointed to by the ACPI base register is enabled and the ACPI power management function is enabled.
6:3	0h RO	Reserved.
2:0	0h RW	**SCI IRQ Select (SCIS):** Specifies on which IRQ the SCI will internally appear. If not using the APIC, the SCI must be routed to IRQ[9-11], and that interrupt is not sharable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the SCI can also be mapped to IRQ20-23, and can be shared with other interrupts. Bits - SCI Map ---- - ------- 000 - IRQ9 001 - IRQ10 010 - IRQ11 011 - Reserved 100 - IRQ20 (only if APIC is enabled) 101 - IRQ21 (only if APIC is enabled) 110 - IRQ22 (only if APIC is enabled) 111 - IRQ23 (only if APIC is enabled) When the interrupt is mapped to APIC interrupts 9, 10 or 11, the APIC should be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, the APIC should be programmed for active-low reception.

4.3.88 Power Gated ACK Status Register 0 (PPASR0)—Offset 1D80h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**CSME Power Gate Ack Status (AGT31_PG_ACK_STS):** Same description as bit 2.
30	0h RO/V	**Controller Link Power Gate Ack Status (AGT30_PG_ACK_STS):** Same description as bit 2.
29	0h RO/V	**CSME Power Gate Ack Status (AGT29_PG_ACK_STS):** Same description as bit 2.
28	0h RO/V	**CSME_KVM Power Gate Ack Status (AGT28_PG_ACK_STS):** Same description as bit 2.
27	0h RO/V	**CSME Power Gate Ack Status (AGT27_PG_ACK_STS):** Same description as bit 2.
26	0h RO/V	**DCI Power Gate Ack Status (AGT26_PG_ACK_STS):** Same description as bit 2.
25	0h RO/V	**XDCI Power Gate Ack Status (AGT25_PG_ACK_STS):** Same description as bit 2.
24:21	0h RO	Reserved.
20	0h RO/V	**SDXC Power Gate Ack Status (AGT20_PG_ACK_STS):** Same description as bit 2.
19	0h RO/V	**Intel Trace Hub Power Gate Ack Status (AGT19_PG_ACK_STS):** Same description as bit 2.
18	0h RO	Reserved.
17	0h RO/V	**ISH Power Gate Ack Status (AGT17_PG_ACK_STS):** Same description as bit 2.
16	0h RO/V	**SMBus Power Gate Ack Status (AGT16_PG_ACK_STS):** Same description as bit 2.
15	0h RO	Reserved.
14	0h RO/V	**Intel Serial I/O Power Gate Ack Status (AGT14_PG_ACK_STS):** Same description as bit 2.
13	0h RO/V	**PCIe Controller D Power Gate Ack Status (AGT13_PG_ACK_STS):** Same description as bit 2.
12	0h RO/V	**HDA Power Gate Ack Status (AGT12_PG_ACK_STS):** Same description as bit 2.
11	0h RO/V	**HDA Power Gate Ack Status (AGT11_PG_ACK_STS):** Same description as bit 2.
10	0h RO/V	**HDA Power Gate Ack Status (AGT10_PG_ACK_STS):** Same description as bit 2.
9	0h RO/V	**HDA_PGD0 Power Gate Ack Status (AGT9_PG_ACK_STS):** Same description as bit 2.
8	0h RO/V	**SATA Power Gate Ack Status (AGT8_PG_ACK_STS):** Same description as bit 2.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO/V	**GbE Power Gate Ack Status (AGT7_PG_ACK_STS):** Same description as bit 2.
6	0h RO/V	**PCIe Controller C Power Gate Ack Status (AGT6_PG_ACK_STS):** Same description as bit 2.
5	0h RO/V	**PCIe Controller B Power Gate Ack Status (AGT5_PG_ACK_STS):** Same description as bit 2.
4	0h RO/V	**PCIe Controller A Power Gate Ack Status (AGT4_PG_ACK_STS):** Same description as bit 2.
3	0h RO/V	**xHCI Power Gate Ack Status (AGT3_PG_ACK_STS):** Same description as bit 2.
2	0h RO/V	**SPI Power Gate Ack Status (AGT2_PG_ACK_STS):** This indicates the current status of the controller. 0: Controller may be power gated 1: Controller may not be power gated
1:0	0h RO	Reserved.

4.3.89 Power Gated ACK Status Register 1 (PPASR1)—Offset 1D84h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RO/V	**HDA Power Gate Ack Status (AGT60_PG_ACK_STS):** Same description as bit 0.
27	0h RO/V	**HDA Power Gate Ack Status (AGT59_PG_ACK_STS):** Same description as bit 0.
26	0h RO/V	**HDA Power Gate Ack Status (AGT58_PG_ACK_STS):** Same description as bit 0.
25:20	0h RO	Reserved.
19	0h RO/V	**CNVI_WIFI Power Gate Ack Status (AGT51_PG_ACK_STS):** Same description as bit 0.
18:8	0h RO	Reserved.
7	0h RO/V	**CSME Power Gate Ack Status (AGT39_PG_ACK_STS):** Same description as bit 0.
6	0h RO/V	**CSME Power Gate Ack Status (AGT38_PG_ACK_STS):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO/V	**CSME Power Gate Ack Status (AGT37_PG_ACK_STS):** Same description as bit 0.
4	0h RO/V	**CSME Power Gate Ack Status (AGT36_PG_ACK_STS):** Same description as bit 0.
3	0h RO	Reserved.
2	0h RO/V	**CSME Power Gate Ack Status (AGT34_PG_ACK_STS):** Same description as bit 0.
1	0h RO/V	**CSME Power Gate Ack Status (AGT33_PG_ACK_STS):** Same description as bit 0.
0	0h RO/V	**CSME_USBR Power Gate Ack Status (AGT32_PG_ACK_STS):** This indicates the current status of the controller. 0: Controller may be power gated 1: Controller may not be power gated

4.3.90 PFET Enable Ack Register 0 (PPFEAR0)—Offset 1D90h

Intel(R) IP is power gated when the corresponding bit in PPFEAR0 or PPFEAR1 is set to 1

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**CSME PFET Enable Ack Status (AGT31_PFET_EN_ACK_STS):** Same definition as bit 2.
30	0h RO/V	**CSME_CLINK PFET Enable Ack Status (AGT30_PFET_EN_ACK_STS):** Same definition as bit 2.
29	0h RO/V	**CSME PFET Enable Ack Status (AGT29_PFET_EN_ACK_STS):** Same definition as bit 2.
28	0h RO/V	**CSME_KVM PFET Enable Ack Status (AGT28_PFET_EN_ACK_STS):** Same definition as bit 2.
27	0h RO/V	**CSME PFET Enable Ack Status (AGT27_PFET_EN_ACK_STS):** Same definition as bit 2.
26	0h RO/V	**DCI PFET Enable Ack Status (AGT26_PFET_EN_ACK_STS):** Same definition as bit 2.
25	0h RO/V	**XDCI PFET Enable Ack Status (AGT25_PFET_EN_ACK_STS):** Same definition as bit 2.
24:20	0h RO	Reserved.
19	0h RO/V	**Intel Trace Hub PFET Enable Ack Status (AGT19_PFET_EN_ACK_STS):** Same definition as bit 2.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	Reserved.
17	0h RO/V	**ISH PFET Enable Ack Status (AGT17_PFET_EN_ACK_STS):** Same definition as bit 2.
16	0h RO/V	**SMBus PFET Enable Ack Status (AGT16_PFET_EN_ACK_STS):** Same definition as bit 2.
15	0h RO	Reserved.
14	0h RO/V	**Intel Serial I/O PFET Enable Ack Status (AGT14_PFET_EN_ACK_STS):** Same definition as bit 2.
13	0h RO/V	**PCIe Controller D PFET Enable Ack Status (AGT13_PFET_EN_ACK_STS):** Same definition as bit 2.
12	0h RO/V	**HDA PFET Enable Ack Status (AGT12_PFET_EN_ACK_STS):** Same definition as bit 2.
11	0h RO/V	**HDA PFET Enable Ack Status (AGT11_PFET_EN_ACK_STS):** Same definition as bit 2.
10	0h RO/V	**HDA PFET Enable Ack Status (AGT10_PFET_EN_ACK_STS):** Same definition as bit 2.
9	0h RO/V	**HDA PFET Enable Ack Status (AGT9_PFET_EN_ACK_STS):** Same definition as bit 2.
8	0h RO/V	**SATA PFET Enable Ack Status (AGT8_PFET_EN_ACK_STS):** Same definition as bit 2.
7	0h RO/V	**GbE PFET Enable Ack Status (AGT7_PFET_EN_ACK_STS):** Same definition as bit 2.
6	0h RO/V	**PCIe Controller C PFET Enable Ack Status (AGT6_PFET_EN_ACK_STS):** Same definition as bit 2.
5	0h RO/V	**PCIe Controller B PFET Enable Ack Status (AGT5_PFET_EN_ACK_STS):** Same definition as bit 2.
4	0h RO/V	**PCIe Controller A PFET Enable Ack Status (AGT4_PFET_EN_ACK_STS):** Same definition as bit 2.
3	0h RO/V	**xHCI PFET Enable Ack Status (AGT3_PFET_EN_ACK_STS):** Same definition as bit 2.
2	0h RO/V	**SPI PFET Enable Ack Status (AGT2_PFET_EN_ACK_STS):** 0: PFET is turned on 1: PFET is turned off
1:0	0h RO	Reserved.

4.3.91 PFET Enable Ack Register 1 (PPFEAR1)—Offset 1D94h

Intel(R) CSME is power gated when PPFEAR0[31..24]=0xF9 and PPFEAR1[7..0]=0xFF

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RO/V	**HDA PFET Enable Ack Status (AGT60_PFET_EN_ACK_STS):** Same definition as bit 0.
27	0h RO/V	**HDA PFET Enable Ack Status (AGT59_PFET_EN_ACK_STS):** Same definition as bit 0.
26	0h RO/V	**HDA PFET Enable Ack Status (AGT58_PFET_EN_ACK_STS):** Same definition as bit 0.
25:20	0h RO	Reserved.
19	0h RO/V	**CNVI_WIFI PFET Enable Ack Status (AGT51_PFET_EN_ACK_STS):** Same definition as bit 0.
18:8	0h RO	Reserved.
7	0h RO/V	**CSME PFET Enable Ack Status (AGT39_PFET_EN_ACK_STS):** Same definition as bit 0.
6	0h RO/V	**CSME PFET Enable Ack Status (AGT38_PFET_EN_ACK_STS):** Same definition as bit 0.
5	0h RO/V	**CSME PFET Enable Ack Status (AGT37_PFET_EN_ACK_STS):** Same definition as bit 0.
4	0h RO/V	**CSME PFET Enable Ack Status (AGT36_PFET_EN_ACK_STS):** Same definition as bit 0.
3	0h RO	Reserved.
2	0h RO/V	**CSME PFET Enable Ack Status (AGT34_PFET_EN_ACK_STS):** Same definition as bit 0.
1	0h RO/V	**CSME PFET Enable Ack Status (AGT33_PFET_EN_ACK_STS):** Same definition as bit 0.
0	0h RO/V	**CSME__USBR PFET Enable Ack Status (AGT32_PFET_EN_ACK_STS):** 0: PFET is turned on 1: PFET is turned off

4.3.92 Chipset Initialization Register 5E0 (CIR5E0)—Offset 1DE0h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**CSME Power Gate Req Status (AGT31_PG_REQ_STS):** Same definition as bit 2.
30	0h RO/V	**CSME_CLINK Power Gate Req Status (AGT30_PG_REQ_STS):** Same definition as bit 2.
29	0h RO/V	**CSME Power Gate Req Status (AGT29_PG_REQ_STS):** Same definition as bit 2.
28	0h RO/V	**CSME_KVM Power Gate Req Status (AGT28_PG_REQ_STS):** Same definition as bit 2.
27	0h RO/V	**CSME Power Gate Req Status (AGT27_PG_REQ_STS):** Same definition as bit 2.
26	0h RO/V	**DCI Power Gate Req Status (AGT26_PG_REQ_STS):** Same definition as bit 2.
25	0h RO/V	**XDCI Power Gate Req Status (AGT25_PG_REQ_STS):** Same definition as bit 2.
24:21	0h RO	Reserved.
20	0h RO/V	**SDXC Power Gate Req Status (AGT20_PG_REQ_STS):** Same definition as bit 2.
19	0h RO/V	**Intel Trace Hub Power Gate Req Status (AGT19_PG_REQ_STS):** Same definition as bit 2.
18	0h RO	Reserved.
17	0h RO/V	**ISH Power Gate Req Status (AGT17_PG_REQ_STS):** Same definition as bit 2.
16	0h RO/V	**SMBus Power Gate Req Status (AGT16_PG_REQ_STS):** Same definition as bit 2.
15	0h RO	Reserved.
14	0h RO/V	**Intel Serial I/O Power Gate Req Status (AGT14_PG_REQ_STS):** Same definition as bit 2.
13	0h RO	Reserved.
12	0h RO/V	**HDA Power Gate Req Status (AGT12_PG_REQ_STS):** Same definition as bit 2.
11	0h RO/V	**HDA Power Gate Req Status (AGT11_PG_REQ_STS):** Same definition as bit 2.
10	0h RO/V	**HDA Power Gate Req Status (AGT10_PG_REQ_STS):** Same definition as bit 2.
9	0h RO/V	**HDA Power Gate Req Status (AGT9_PG_REQ_STS):** Same definition as bit 2.
8	0h RO/V	**SATA Power Gate Req Status (AGT8_PG_REQ_STS):** Same definition as bit 2.
7	0h RO/V	**GbE Power Gate Req Status (AGT7_PG_REQ_STS):** Same definition as bit 2.
6	0h RO/V	**PCIe Controller C Power Gate Req Status (AGT6_PG_REQ_STS):** Same definition as bit 2.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO/V	**PCIe Controller B Power Gate Req Status (AGT5_PG_REQ_STS):** Same definition as bit 2.
4	0h RO/V	**PCIe Controller A Power Gate Req Status (AGT4_PG_REQ_STS):** Same definition as bit 2.
3	0h RO/V	**xHCI Power Gate Req Status (AGT3_PG_REQ_STS):** Same definition as bit 2.
2	0h RO/V	**SPI Power Gate Req Status (AGT2_PG_REQ_STS):** This indicates the current power gating request status of the controller. 0: Controller is requesting to be power-gated 1: Controller is requesting to be powered-on.
1:0	0h RO	Reserved.

4.3.93 Chipset Initialization Register 5E4 (CIR5E4)—Offset 1DE4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RO/V	**HDA Power Gate Req Status (AGT60_PG_REQ_STS):** Same definition as bit 0.
27	0h RO/V	**HDA Power Gate Req Status (AGT59_PG_REQ_STS):** Same definition as bit 0.
26	0h RO/V	**HDA Power Gate Req Status (AGT58_PG_REQ_STS):** Same definition as bit 0.
25:23	0h RO	Reserved.
22	0h RO/V	**SPF Power Gate Req Status (AGT54_PG_REQ_STS):** Same definition as bit 0.
21	0h RO/V	**eMMC Power Gate Req Status (AGT53_PG_REQ_STS):** Same definition as bit 0.
20	0h RO/V	**UFS Power Gate Req Status (AGT52_PG_REQ_STS):** Same definition as bit 0.
19	0h RO/V	**CNVI_WIFI Power Gate Req Status (AGT51_PG_REQ_STS):** Same definition as bit 0.
18:8	0h RO	Reserved.
7	0h RO/V	**CSME Power Gate Req Status (AGT39_PG_REQ_STS):** Same definition as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RO/V	**CSME Power Gate Req Status (AGT38_PG_REQ_STS):** Same definition as bit 0.
5	0h RO/V	**CSME Power Gate Req Status (AGT37_PG_REQ_STS):** Same definition as bit 0.
4	0h RO/V	**CSME_SMS2 Power Gate Req Status (AGT36_PG_REQ_STS):** Same definition as bit 0.
3	0h RO	Reserved.
2	0h RO/V	**CSME Power Gate Req Status (AGT34_PG_REQ_STS):** Same definition as bit 0.
1	0h RO/V	**CSME Power Gate Req Status (AGT33_PG_REQ_STS):** Same definition as bit 0.
0	0h RO/V	**CSME_USBR Power Gate Req Status (AGT32_PG_REQ_STS):** 0: IP may be power gated 1: IP may not be power gated

4.3.94 Static PG Function Disable 1 (ST_PG_FDIS1)—Offset 1E20h

Static PG Related Function Disable Register 1

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Static Function Disable Lock (ST_FDIS_LK):** Lock control for all ST_PG_FDIS* and NST_PG_FDIS_* registers. Also self-locks when written to 1. This bit is reset by RSMRST# assertion.
30:6	0h RO	Reserved.
5	0h RW/L	**ISH Function Disable (PMC Version) (ISH_FDIS_PMC):** BIOS is required to set this bit when ISH function is configured to be function disabled. This bit is reset by RTCRST# assertion.
4:2	0h RO	Reserved.
1	0h RW/L	**CNVI Function Disable (PMC Version) (CNVI_FDIS_PMC):** BIOS is required to set this bit when GBE function is configured to be function disabled.
0	0h RW/L	**GBE Function Disable (PMC Version) (GBE_FDIS_PMC):** BIOS is required to set this bit when GBE function is configured to be function disabled. This bit is reset by RTCRST#

4.3.95 Static Function Disable Control 2 (ST_PG_FDIS2)—Offset 1E24h

Static Function Disable Control 2 Register

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW/L	**GSPI Controller Device Device 2 Function Disable (PMC Version) (LPSS_GSPI2_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
10	0h RW/L	**GSPI Controller Device Device 1 Function Disable (PMC Version) (LPSS_GSPI1_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
9	0h RW/L	**GSPI Controller Device Device 0 Function Disable (PMC Version) (LPSS_GSPI0_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
8	0h RW/L	**UART Controller Device Device 2 Function Disable (PMC Version) (LPSS_UART2_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
7	0h RW/L	**UART Controller Device Device 1 Function Disable (PMC Version) (LPSS_UART1_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
6	0h RW/L	**UART Controller Device Device 0 Function Disable (PMC Version) (LPSS_UART0_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
5	0h RW/L	**I2C Controller Device 5 Function Disable (PMC Version) (LPSS_I2C5_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
4	0h RW/L	**I2C Controller Device 4 Function Disable (PMC Version) (LPSS_I2C4_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
3	0h RW/L	**I2C Controller Device 3 Function Disable (PMC Version) (LPSS_I2C3_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
2	0h RW/L	**I2C Controller Device 2 Function Disable (PMC Version) (LPSS_I2C2_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
1	0h RW/L	**I2C Controller Device 1 Function Disable (PMC Version) (LPSS_I2C1_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.
0	0h RW/L	**I2C Controller Device 0 Function Disable (PMC Version) (LPSS_I2C0_FDIS_PMC):** BIOS is required to set this bit when this Device (single function) is configured to be function disabled.

4.3.96 Chipset Initialization Register (NST_PG_FDIS_1)—Offset 1E28h

BIOS may need to program this register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27	0h RW/L	**UFSX2 Function Disable (PMC Version) (UFSX2_FDIS_PMC):** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled.
26	0h RW/L	**XDCI Function Disable (PMC Version) (XDCI_FDIS_PMC):** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled.
25	0h RW/L	**SMB Function Disable (PMC Version) (SMB_FDIS_PMC):** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled.
24	0h RO	Reserved.
23	0h RW/L	**ADSP Function Disable (PMC Version) (ADSP_FDIS_PMC):** BIOS is required to set this bit when this IP block (single function) is configured to be function disabled.
22	0h RW/L	**SATA Controller Function Disable (PMC Version) (ST_FDIS_PMC):** BIOS is required to set this bit when the SATA controller (single function) is configured to be function disabled.
21:18	0h RO	Reserved.
17	0h RW/L	**PCIe Controller D Port 3 Function Disable [PMC Version] (PCIE_D3_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
16	0h RW/L	**PCIe Controller D Port 2 Function Disable [PMC Version] (PCIE_D2_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
15	0h RW/L	**PCIe Controller D Port 1 Function Disable [PMC Version] (PCIE_D1_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
14	0h RW/L	**PCIe Controller D Port 0 Function Disable [PMC Version] (PCIE_D0_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
13	0h RW/L	**PCIe Controller C Port 3 Function Disable (PMC Version) (PCIE_C3_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
12	0h RW/L	**PCIe Controller C Port 2 Function Disable (PMC Version) (PCIE_C2_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
11	0h RW/L	**PCIe Controller C Port 1 Function Disable (PMC Version) (PCIE_C1_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
10	0h RW/L	**PCIe Controller C Port 0 Function Disable (PMC Version) (PCIE_C0_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
9	0h RW/L	**PCIe Controller B Port 3 Function Disable (PMC Version) (PCIE_B3_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
8	0h RW/L	**PCIe Controller B Port 2 Function Disable (PMC Version) (PCIE_B2_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW/L	**PCIe Controller B Port 1 Function Disable (PMC Version) (PCIE_B1_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
6	0h RW/L	**PCIe Controller B Port 0 Function Disable (PMC Version) (PCIE_B0_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
5	0h RW/L	**PCIe Controller A Port 3 Function Disable (PMC Version) (PCIE_A3_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
4	0h RW/L	**PCIe Controller A Port 2 Function Disable (PMC Version) (PCIE_A2_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
3	0h RW/L	**PCIe Controller A Port 1 Function Disable (PMC Version) (PCIE_A1_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
2	0h RW/L	**PCIe Controller A Port 0 Function Disable (PMC Version) (PCIE_A0_FDIS_PMC):** BIOS is required to set this bit when this PCIE port (single function) is configured to be function disabled.
1	0h RO	Reserved.
0	0h RW/L	**xHCI Function Disable (PMC Version) (xHCI_FDIS_PMC):** BIOS is required to set this bit when this IP block (single logical function) is configured to be function disabled.

4.3.97 PCIe Controller Disable Read (N_STPG_FUSE_SS_DIS_RD_1)—Offset 1E40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RO/V	**PCIe Controller D Port 3 Disable (PCIE_D3_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
16	0h RO/V	**PCIe Controller D Port 2 Disable (PCIE_D2_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
15	0h RO/V	**PCIe Controller D Port 1 Disable (PCIE_D1_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
14	0h RO/V	**PCIe Controller D Port 0 Disable (PCIE_D0_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
13	0h RO/V	**PCIe Controller C Port 3 Disable (PCIE_C3_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
12	0h RO/V	**PCIe Controller C Port 2 Disable (PCIE_C2_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO/V	**PCIe Controller C Port 1 Disable (PCIE_C1_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
10	0h RO/V	**PCIe Controller C Port 0 Disable (PCIE_C0_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
9	0h RO/V	**PCIe Controller B Port 3 Disable (PCIE_B3_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
8	0h RO/V	**PCIe Controller B Port 2 Disable (PCIE_B2_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
7	0h RO/V	**PCIe Controller B Port 1 Disable (PCIE_B1_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
6	0h RO/V	**PCIe Controller B Port 0 Disable (PCIE_B0_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
5	0h RO/V	**PCIe Controller A Port 3 Disable (PCIE_A3_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
4	0h RO/V	**PCIe Controller A Port 2 Disable (PCIE_A2_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
3	0h RO/V	**PCIe Controller A Port 1 Disable (PCIE_A1_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
2	0h RO/V	**PCIe Controller A Port 0 Disable (PCIE_A0_FUSE_DIS):** RO bit indicating if this PCIE port (single function) is disabled.
1:0	0h RO	Reserved.

4.3.98 Capability Disable Read Register (STPG_FUSE_SS_DIS_RD_2)—Offset 1E44h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RO/V	**TBT LSX Disable (TBTLSX_FUSE_SS_DIS):** This bit indicates if TBTLSX function is disabled.
28:20	0h RO	Reserved.
19	0h RO/V	**xDCI Disable (XDCI_FUSE_SS_DIS):** RO bit indicating if xDCI function is disabled.
18:17	0h RO	Reserved.
16	0h RO/V	**DSP Disable (DSP_FUSE_SS_DIS):** RO bit indicating if DSP function is disabled.

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	Reserved.
9	0h RO/V	**SMBus Disable (SMB_FUSE_SS_DIS):** RO bit indicating if SMBus function is disabled.
8:7	0h RO	Reserved.
6	0h RO/V	**Intel Serial I/O Disable (LPSS_FUSE_SS_DIS):** RO bit indicating if Serial IO (I2C, UART, GSPI) function is disabled.
5	0h RO/V	**eMMC Disable (EMMC_FUSE_SS_DIS):** RO bit indicating if eMMC function is disabled.
4	0h RO/V	**CNVi Disable (CNVI_FUSE_SS_DIS):** RO bit indicating if CNVi function is disabled.
3	0h RO	Reserved.
2	0h RO/V	**SD Controller Disable (SDX_FUSE_SS_DIS):** RO bit indicating if SDXC function is disabled.
1	0h RO/V	**ISH Disable (ISH_FUSE_SS_DIS):** RO bit indicating if ISH function is disabled.
0	0h RO/V	**GBE Disable (GBE_FUSE_SS_DIS):** RO bit indicating if GBE function is disabled.

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5 High Definition Audio Interface (D31:F3)

5.1 High Definition Audio PCI Configuration Registers Summary

Table 5-1. Summary of High Definition Audio PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Vendor Identification (VID)—Offset 0h	8086h
2h	3h	Device ID (DID)—Offset 2h	XXXXh
4h	5h	Command (CMD)—Offset 4h	0h
6h	7h	Status (STS)—Offset 6h	10h
8h	8h	Revision Identification (RID)—Offset 8h	XXh
9h	9h	Programming Interface (PI)—Offset 9h	0h
Ah	Ah	Sub Class Code (SCC)—Offset Ah	3h
Bh	Bh	Base Class Code (BCC)—Offset Bh	4h
Ch	Ch	Cache Line Size (CLS)—Offset Ch	0h
Dh	Dh	Latency Timer (LT)—Offset Dh	0h
Eh	Eh	Header Type (HTYPE)—Offset Eh	0h
10h	13h	Intel HD Audio Base Lower Address (HDALBA)—Offset 10h	4h
14h	17h	Intel HD Audio Base Upper Address (HDAUBA)—Offset 14h	0h
18h	1Bh	Shadowed PCI Configuration Lower Base Address (SPCLBA)—Offset 18h	0h
1Ch	1Fh	Shadowed PCI Configuration Upper Base Address (SPCUBA)—Offset 1Ch	0h
20h	23h	Audio DSP Lower Base Address (ADSPLBA)—Offset 20h	4h
24h	27h	Audio DSP Upper Base Address (ADSPUBA)—Offset 24h	0h
2Ch	2Dh	Subsystem Vendor ID (SVID)—Offset 2Ch	0h
2Eh	2Fh	Subsystem ID (SID)—Offset 2Eh	0h
34h	34h	Capability Pointer (CAPPTR)—Offset 34h	50h
3Ch	3Ch	Interrupt Line (INTLN)—Offset 3Ch	0h
3Dh	3Dh	Interrupt Pin (INTPN)—Offset 3Dh	1h
50h	51h	PCI Power Management Capability ID (PID)—Offset 50h	6001h
52h	53h	Power Management Capabilities (PC)—Offset 52h	C043h
54h	57h	Power Management Control And Status (PCS)—Offset 54h	8h
60h	61h	MSI Capability ID (MID)—Offset 60h	7005h
62h	63h	MSI Message Control (MMC)—Offset 62h	80h
64h	67h	MSI Message Lower Address (MMLA)—Offset 64h	0h
68h	6Bh	MSI Message Upper Address (MMUA)—Offset 68h	0h
6Ch	6Dh	MSI Message Data (MMD)—Offset 6Ch	0h
70h	71h	PCI Express Capability ID (PXID)—Offset 70h	10h

Table 5-1. Summary of High Definition Audio PCI Configuration Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
72h	73h	PCI Express Capabilities (PXC)—Offset 72h	91h
74h	77h	Device Capabilities (DEVCAP)—Offset 74h	10000000h
78h	79h	Device Control (DEVC)—Offset 78h	2800h
7Ah	7Bh	Device Status (DEVS)—Offset 7Ah	10h

5.1.1 Vendor Identification (VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 8086h

Bit Range	Default and Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID):** Indicates that Intel is the vendor.

5.1.2 Device ID (DID)—Offset 2h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: XXXXh

Bit Range	Default and Access	Field Name (ID): Description
15:0	8C20h RO/V	**Device ID (DID):** Indicates the Device ID of the controller. Refer to the Device and Revision ID Table in Volume 1 for default value.

5.1.3 Command (CMD)—Offset 4h

This register provides coarse control over a device's ability to generate and respond to PCI cycles.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (ID):** Enables the device to assert an INTx#. When set, the Intel(r) HD Audio controller's INTx# signal will be de-asserted. When cleared, the INTx# signal may be asserted. Note that this bit does not affect the generation of MSI's.
9	0h RO	**Fast Back to Back Enable (FBE):** Not implemented. Hardwired to 0.
8	0h RW	**SERR Enable (SEN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
7	0h RO	**Wait Cycle Control (WCC):** Not implemented. Hardwired to 0.
6	0h RW	**Parity Error Response (PER):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
5	0h RO	**VGA Palette Snoop (VPS):** Not implemented. Hardwired to 0.
4	0h RO	**Memory Write and Invalidate Enable (MWI):** Not implemented. Hardwired to 0.
3	0h RO	**Special Cycle Enable (SCE):** Not implemented. Hardwired to 0.
2	0h RW	**Bus Master Enable (BME):** 1 = Enable, 0 = Disable. Controls standard PCI Express bus mastering capabilities for Memory and IO, reads and writes. Note that this also controls MSI generation since MSI are essentially Memory writes.
1	0h RW	**Memory Space Enable (MSE):** When set, enables memory space accesses to the Intel HD Audio controller.
0	0h RO	**I/O Space (IOS):** The Intel HD Audio controller does not implement IO Space, therefore this bit is hardwired to 0.

5.1.4 Status (STS)—Offset 6h

This register is used to record status information for PCI bus related events.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 10h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RO	**Detected Parity Error (DPE):** Not implemented. Hardwired to 0.
14	0h RO	**SERR# Status (SERRS):** Not implemented. Hardwired to 0.
13	0h RW/1C/V	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, this bit is set. SW writes a 1 to this bit to clear it.
12	0h RW/1C/V	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, this bit is set. SW writes a 1 to this bit to clear it.

Bit Range	Default and Access	Field Name (ID): Description
11	0h RO	**Signaled Target-Abort (STA):** Not implemented. Hardwired to 0.
10:9	0h RO	**DEVSEL# Timing Status (DEVT):** Does not apply. Hardwired to 0.
8	0h RO	**Master Data Parity Error (MDPE):** Not implemented. Hardwired to 0.
7	0h RO	**Fast Back to Back Capable (FBC):** Does not apply. Hardwired to 0.
6	0h RO	Reserved.
5	0h RO	**66 MHz Capable (C66):** Does not apply. Hardwired to 0.
4	1h RO	**Capabilities List Exists (CLIST):** Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	0h RO/V	**Interrupt Status (IS):** Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted. This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register). Note that this bit is not set by an MSI.
2:0	0h RO	Reserved.

5.1.5 Revision Identification (RID)—Offset 8h

This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: XXh

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Volume 1 for specific value.

5.1.6 Programming Interface (PI)—Offset 9h

This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW/L	**Programming Interface (PI):** Value assigned to the Intel HD Audio subsystem. Locked when FNCFG.BCLD = 1.

5.1.7 Sub Class Code (SCC)—Offset Ah

This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 3h

Bit Range	Default and Access	Field Name (ID): Description
7:0	3h RW/L	**Sub Class Code (SCC):** This indicates the device is an Intel HD Audio audio device, in the context of a multimedia device. Locked when FNCFG.BCLD = 1.

5.1.8 Base Class Code (BCC)—Offset Bh

This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
7:0	4h RW/L	**Base Class Code (BCC):** This register indicates that the function implements a multimedia device. Locked when FNCFG.BCLD = 1.

5.1.9 Cache Line Size (CLS)—Offset Ch

This register specifies the system cache line size in units of DWORDs.

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Cache Line Size (CLS):** Does not apply to PCI Express. PCI Express spec requires this to be implemented as a R/W register but has no functional impact on the PCH.

5.1.10 Latency Timer (LT)—Offset Dh

This register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master.

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW/L	**Latency Timer (LT):** Doesn t apply to PCI Express. RO as 00h if PCI Express. If configured to appear as PCI device, maintain RW for Legacy PCI SW compliancy. Locked when FNCFG.HDASPCID = 0

5.1.11 Header Type (HTYPE)—Offset Eh

This register identifies the layout of the second part of the predefined header and also whether or not the device contains multiple functions.

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RW/L	**Multi Function Device (MFD):** Value of 0 indicates a single function device. Value of 1 indicates a multi function device. Locked when FNCFG.BCLD = 1.
6:0	0h RO	**Header Type (HTYPE):** Implements Type 0 Configuration header.

5.1.12 Intel HD Audio Base Lower Address (HDALBA)—Offset 10h

This BAR creates a selected size of memory space to signify the base address of the Intel HD Audio memory mapped configuration registers depending on implementation.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:14	0h RW	**Lower Base Address (LBA):** Base address for the Intel HD Audio subsystem s memory mapped configuration registers. 16 Kbytes are requested by hardwiring bits 13:4 to 0 s.
13:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

5.1.13 Intel HD Audio Base Upper Address (HDAUBA)—Offset 14h

This BAR creates a selected size of memory space to signify the base address (upper 32 bits) of the Intel HD Audio memory mapped configuration registers, depending on implementation.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Intel HD Audio Upper Base Address (UBA):** Upper 32 bits of the Base address for the Intel(r) HD Audio controller's memory mapped configuration registers.

5.1.14 Shadowed PCI Configuration Lower Base Address (SPCLBA)—Offset 18h

This BAR creates 4 Kbytes of memory space to signify the base address (lower 32 bits) of the shadowed PCI configuration when used as an ACPI device.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW/L	**Lower Base Address (LBA):** Base address for the PCI Configuration register shadowed to memory mapped. 4 KB is requested by hardwiring bits 11:4 to 0 s. Locked when PCICFGCTL0.SPCBAD = 1.
11:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	0h RO/V	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

5.1.15 Shadowed PCI Configuration Upper Base Address (SPCUBA)—Offset 1Ch

This BAR creates 4 Kbytes of memory space to signify the base address (upper 32 bits) of the shadowed PCI configuration when used as an ACPI device.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**Upper Base Address (UBA):** Upper 32 bits of the Base address for the PCI Configuration register shadowed to memory mapped. Locked when PCICFGCTL0.SPCBAD = 1.

5.1.16 Audio DSP Lower Base Address (ADSPLBA)—Offset 20h

This BAR creates a selected size of memory space to signify the base address of the Audio DSP memory mapped configuration registers depending on implementation. The number of LBA bits in this register is depending on the size of the memory window implemented.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RW	**Lower Base Address (LBA):** Base address for the Audio DSP memory mapped configuration registers.
19:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in 64-bit address space.
0	0h RO	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

5.1.17 Audio DSP Upper Base Address (ADSPUBA)—Offset 24h

This BAR creates a selected size of memory space to signify the base address (upper 32 bits) of the Audio DSP memory-mapped configuration registers, depending on implementation.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Upper Base Address (UBA):** Upper 32 bits of the Base address for the Audio DSP memory mapped configuration registers.

5.1.18 Subsystem Vendor ID (SVID)—Offset 2Ch

This register should be implemented for any function that could be instantiated more than once in a given system, for example, a system with 2 audio subsystems, one down on the motherboard and the other plugged into a PCI expansion slot, should have the SVID register implemented. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one audio subsystem from the other(s).
Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SID to create one 32-bit write. This register is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW/L	**SVID (SVID):** These RW bits have no functionality. Locked when FNCFG.BCLD = 1.

5.1.19 Subsystem ID (SID)—Offset 2Eh

This register should be implemented for any function that could be instantiated more than once in a given system, for example, a system with 2 audio subsystems, one down on the motherboard and the other plugged into a PCI expansion slot. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one audio subsystem from the other(s). Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SVID to create one 32-bit write. This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW/L	**SID (SID):** These RW bits have no functionality. Locked when FNCFG.BCLD = 1.

5.1.20 Capability Pointer (CAPPTR)—Offset 34h

This optional register is used to point to a linked list of new capabilities implemented by this device.

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 50h

Bit Range	Default and Access	Field Name (ID): Description
7:0	50h RO	**Capability Pointer (CAPPTR):** Indicates that the first capability pointer offset is offset 50h (Power Management Capability).

5.1.21 Interrupt Line (INTLN)—Offset 3Ch

This register is not affected by FLR.

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Line (INTLN):** Hardware does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

5.1.22 Interrupt Pin (INTPN)—Offset 3Dh

This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 3

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3:0	1h RW/L	**Interrupt Pin (INTPN):** Identifies the interrupt pin the function uses. 0h: No interrupt pin 1h: INTA 2h: INTB 3h: INTC 4h: INTD 5h - Fh: reserved Locked when FNCFG.BCLD = 1.

5.1.23 PCI Power Management Capability ID (PID)—Offset 50h

This register declares the power management capability structure.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 6001h

Bit Range	Default and Access	Field Name (ID): Description
15:8	60h RW/L	**Next Capability (NEXT):** Points to the next capability structure (MSI). Locked when FNCFG.BCLD = 1.
7:0	1h RO	**Cap ID (CAP):** Indicates that this pointer is a PCI power management capability

5.1.24 Power Management Capabilities (PC)—Offset 52h

This register provides information on the capabilities of the function related to power management.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: C043h

Bit Range	Default and Access	Field Name (ID): Description
15:11	18h RW/L	**PME_Support (PMES):** Indicates PME# can be generated from D3 and D0 states. Programmable by BIOS for the option to declare SUS well wake is supported or not: 19h (SUS well wake supported) or 09h (SUS well wake not supported). Locked when FNCFG.BCLD = 1
10	0h RO	**D2_Support (D2S):** The D2 state is not supported.
9	0h RO	**D1_Support (D1S):** The D1 state is not supported.
8:6	1h RW/L	**Aux_Current (AC):** Reports 55 mA maximum Suspend well current required when in the D3cold state. Programmable by BIOS for the option to declare SUS well wake is supported or not: 001b (SUS well wake supported) or 000b (SUS well wake not supported). Locked when FNCFG.BCLD = 1.
5	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	0h RO	Reserved.
3	0h RO	**PME Clock (PMEC):** Does not apply. Hardwired to 0.
2:0	3h RW/L	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification. Programmable by BIOS to older revision if compatibility issue is found. Locked when FNCFG.BCLD = 1.

5.1.25 Power Management Control And Status (PCS)—Offset 54h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	**Data (DT):** Does not apply. Hardwired to 0's.
23	0h RO	**Bus Power/Clock Control Enable (BPCCE):** Does not apply. Hardwired to0.
22	0h RO	**B2/B3 Support (B23):** Does not apply. Hardwired to 0.
21:16	0h RO	Reserved.
15	0h RW/1C/V	**PME Status (PMES):** This bit is set when the Intel HD Audio controller would normally assert the PME# signal independent of the state of the PME bit. This bit is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
14:9	0h RO	Reserved.
8	0h RW	**PME Enable (PMEE):** When set, and if corresponding PMES is also set, the Intel HD Audio subsystem send PME to PMC. This bit is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
7:4	0h RO	Reserved.
3	1h RW/L	**No Soft Reset (NSR):** When set (1), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. When clear (0), devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled. Locked when FNCFG.BCLD = 1.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the Intel HD Audio subsystem and to set a new power state. The values are: 00 D0 state 11 D3HOT state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3HOT states, the Intel HD Audio subsystem s configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. When software changes this value from the D3HOT state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.

5.1.26 MSI Capability ID (MID)—Offset 60h

NEXT field is not affected by D3HOT to D0 reset or FLR

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 7005h

Bit Range	Default and Access	Field Name (ID): Description
15:8	70h RO/V	**Next Capability (NEXT):** Points to the PCI Express* capability structure. The value of this field depends on the FNCFG.HDASPCID bit. When FNCFG.HDASPCID is 0 , this field has a value of 70h where it points to the PCI Express capability structure. When FNCFG.HDASPCID bit is 1 , this field has a value of 00h to indicate that this is the last capability structure in the list.
7:0	5h RO	**Cap ID (CAP):** Indicates that this pointer is a MSI capability

5.1.27 MSI Message Control (MMC)—Offset 62h

This register provides system software control over MSI.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	1h RO	**64b Address Capability (ADD64):** Indicates the ability to generate a 64-bitmessage address
6:4	0h RO	**Multiple Message Enable (MME):** Normally this is a R/W register. However since only 1 message is supported, these bits are hardwired to 000 = 1 message.
3:1	0h RO	**Multiple Message Capable (MMC):** Hardwired to 0 indicating request for 1message
0	0h RW	**MSI Enable (ME):** If set to 1 an MSI will be generated instead of an INTx#signal. If set to 0, an MSI may not be generated.

5.1.28 MSI Message Lower Address (MMLA)—Offset 64h

This register specifies the MSI message address (lower 32 bits).

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI Message Lower Address (MMLA):** Lower Address used for MSI Message.
1:0	0h RO	Reserved.

5.1.29 MSI Message Upper Address (MMUA)—Offset 68h

This register specifies the MSI message address (upper 32 bits).

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI Message Upper Address (MMUA):** Upper 32 bits of address used for MSIMessage.

5.1.30 MSI Message Data (MMD)—Offset 6Ch

This register specifies the MSI message data.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW	**MSI Message Data (MMD):** Data used for MSI Message.

5.1.31 PCI Express Capability ID (PXID)—Offset 70h

This register declares the PCI Express capability structure.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 10h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RO	**Next Capability (NEXT):** Indicates that this is the last capability structure in the list.
7:0	10h RO	**Cap ID (CAP):** Indicates that this pointer is a PCI Express capability structure.

5.1.32 PCI Express Capabilities (PXC)—Offset 72h

This register identifies PCI Express device Function type and associated capabilities.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 91h

Bit Range	Default and Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13:9	0h RO	**Interrupt Message Number (IMN):** Hardwired to 0.
8	0h RO	**Slot Implemented (SI):** Hardwired to 0.
7:4	9h RO	**Device/Port Type (DPT):** Indicates that this is a Root Complex IntegratedEndpoint Device.
3:0	1h RO	**Capability Version (CV):** Indicates version #1 PCI Express capability

5.1.33 Device Capabilities (DEVCAP)—Offset 74h

This register is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 3

Default: 10000000h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	1h RW/L	**Functional Level Reset (FLR):** A 1 indicates that the Intel HD Audio subsystem supports the Function Level Reset capability. Locked when FNCFG.BCLD = 1.
27:26	0h RO	**Captured Slot Power Limit Scale (SPLS):** Hardwired to 0.
25:18	0h RO	**Captured Slot Power Limit Value (SPLV):** Hardwired to 0.
17:15	0h RO	Reserved.
14	0h RO	**Power Indicator Present (PIP):** Hardwired to 0.

Bit Range	Default and Access	Field Name (ID): Description
13	0h RO	**Attention Indicator Present (AIP):** Hardwired to 0.
12	0h RO	**Attention Button Present (ABP):** Hardwired to 0.
11:9	0h RW/L	**Endpoint L1 Acceptable Latency (L1CAP):** This bit field is defined in the PCI Express spec as RO. At this time it is risky to assign a hardwired value to this bit field. Making it RW would cause a WHQL failure. By making it RW/L it will appear as RO to WHQL testing while allowing BIOS to write a value at boot that is determined by post silicon system testing. Locked when FNCFG.BCLD = 1.
8:6	0h RW/L	**Endpoint L0s Acceptable Latency (L0SCAP):** This bit field is defined in the PCI Express spec as RO. At this time it is risky to assign a hardwired value to this bit field. Making it RW would cause a WHQL failure. By making it RW/L it will appear as RO to WHQL testing while allowing BIOS to write a value at boot that is determined by post silicon system testing. Locked when FNCFG.BCLD = 1.
5	0h RO	**Extended Tag Field Support (ETCAP):** Indicates 5 bit tag supported.
4:3	0h RO	**Phantom Functions Supported (PFCAP):** Indicates phantom functions notsupported.
2:0	0h RO	**Max Payload Size Supported (MPCAP):** Indicates 128B maximum payloadsize capability.

5.1.34 Device Control (DEVC)—Offset 78h

NSNPEN bit is not affected by D3HOT to D0 reset or FLR.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 2800h

Bit Range	Default and Access	Field Name (ID): Description
15	0h WO	**Initiate FLR (IF):** Used to initiate FLR transition. A write of 1 initiates FLR transition. Since hardware must not respond to any cycles until FLR completion, the read value by software from this bit is 0 .
14:12	2h RW	**Max Read Request Size (MRRS):** This field sets the maximum Read Request size for the Function as a Requester. The Function must not generate Read Requests with size exceeding the set value. Defined encodings for this field are: 000: 128 B 001: 256 B 010: 512 B 011: 1024 B 100: 2048 B 101: 4096 B 110 111: Reserved
11	1h RW	**Enable No Snoop (NSNPEN):** When set to 1 the Intel HD Audio controller is permitted to set the No Snoop bit in the Requester Attributes of a bus master transaction. In this case VC0, VCp, or VC1 may be used for isochronous transfers. When set to 0 the Intel HD Audio controller will not set the No Snoop bit. In the case isochronous transfers will not use VC1(VCi) even if it is enabled since VC1 is never snooped. Isochronous transfers will use either VCp or VC0. This bit is not affected by D3HOT to D0 reset or FLR.
10	0h RO	**Auxiliary (AUX) Power PM Enable (AUXPEN):** Hardwired to 0 indicating Intel HD Audio device does not draw AUX power.

Bit Range	Default and Access	Field Name (ID): Description
9	0h RO	**Phantom Functions Enable (PFEN):** Hardwired to 0 disabling phantom functions.
8	0h RO	**Extended Tag Field Enable (ETEN):** Hardwired to 0 enabling 5-bit tag.
7:5	0h RO	**Max Payload Size (MAXPAY):** Hardwired to 000 indicating 128 B.
4	0h RO	**Enable Relaxed Ordering (ROEN):** Hardwired to 0 disabling relaxed ordering.
3	0h RW	**Unsupported Request Reporting Enable (URREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
2	0h RW	**Fatal Error Reporting Enable (FEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
1	0h RW	**Non-Fatal Error Reporting Enable (NFEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.
0	0h RW	**Correctable Error Reporting Enable (CEREN):** Functionality not implemented. This bit is R/W to pass PCIe compliance testing.

5.1.35 Device Status (DEVS)—Offset 7Ah

This register provides information about PCI Express device (Function) specific parameters.

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 3

Default: 10h

Bit Range	Default and Access	Field Name (ID): Description
15:6	0h RO	Reserved.
5	0h RO/V	**Transactions Pending (TXP):** A 1 indicates that the Intel HD Audio controller has issued Non-Posted requests which have not been completed. A 0 indicates that Completions for all Non-Posted Requests have been received.
4	1h RW/L	**AUX Power Detected (AUXDET):** Hardwired to 1 indicating the device is connected to Suspend power. Programmable by BIOS for the option to declare SUS well wake is supported or not: 1b (SUS well wake supported) or 0b (SUS well wake not supported). Locked when FNCFG.BCLD = 1.
3	0h RO	**Unsupported Request Detected (URDET):** Not implemented. Hardwired to 0.
2	0h RO	**Fatal Error Detected (FEDET):** Not implemented. Hardwired to 0.
1	0h RO	**Non-Fatal Error Detected (NFEDET):** Not implemented. Hardwired to 0.
0	0h RO	**Correctable Error Detected (CEDET):** Not implemented. Hardwired to 0.

5.2 High Definition Audio Memory Mapped I/O Registers Summary

Table 5-2. Summary of High Definition Audio Memory Mapped I/O Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Global Capabilities (GCAP)—Offset 0h	9701h
2h	2h	Minor Version (VMIN)—Offset 2h	0h
3h	3h	Major Version (VMAJ)—Offset 3h	1h
4h	5h	Output Payload Capability (OUTPAY)—Offset 4h	3Ch
6h	7h	Input Payload Capability (INPAY)—Offset 6h	1Dh
8h	Bh	Global Control (GCTL)—Offset 8h	0h
Ch	Dh	Wake Enable (WAKEEN)—Offset Ch	0h
Eh	Fh	Wake Status (WAKESTS)—Offset Eh	0h
10h	11h	Global Status (GSTS)—Offset 10h	0h
12h	13h	Global Capabilities 2 (GCAP2)—Offset 12h	1h
14h	15h	Linked List Capabilities Header (LLCH)—Offset 14h	C00h
18h	19h	Output Stream Payload Capability (OUTSTRMPAY)—Offset 18h	30h
1Ah	1Bh	Input Stream Payload Capability (INSTRMPAY)—Offset 1Ah	18h
20h	23h	Interrupt Control (INTCTL)—Offset 20h	0h
24h	27h	Interrupt Status (INTSTS)—Offset 24h	0h
30h	33h	Wall Clock Counter (WALCLK)—Offset 30h	0h
38h	3Bh	Stream Synchronization (SSYNC)—Offset 38h	0h
40h	43h	CORB Lower Base Address (CORBLBASE)—Offset 40h	0h
44h	47h	CORB Upper Base Address (CORBUBASE)—Offset 44h	0h
48h	49h	CORB Write Pointer (CORBWP)—Offset 48h	0h
4Ah	4Bh	CORB Read Pointer (CORBRP)—Offset 4Ah	0h
4Ch	4Ch	CORB Control (CORBCTL)—Offset 4Ch	0h
4Dh	4Dh	CORB Status (CORBSTS)—Offset 4Dh	0h
4Eh	4Eh	CORB Size (CORBSIZE)—Offset 4Eh	42h
50h	53h	RIRB Lower Base Address (RIRBLBASE)—Offset 50h	0h
54h	57h	RIRB Upper Base Address (RIRBUBASE)—Offset 54h	0h
58h	59h	RIRB Write Pointer (RIRBWP)—Offset 58h	0h
5Ah	5Bh	Response Interrupt Count (RINTCNT)—Offset 5Ah	0h
5Ch	5Ch	RIRB Control (RIRBCTL)—Offset 5Ch	0h
5Dh	5Dh	RIRB Status (RIRBSTS)—Offset 5Dh	0h
5Eh	5Eh	RIRB Size (RIRBSIZE)—Offset 5Eh	42h
60h	63h	Immediate Command (IC)—Offset 60h	0h
64h	67h	Immediate Response (IR)—Offset 64h	0h
68h	69h	Immediate Command Status (ICS)—Offset 68h	0h
70h	73h	DMA Position Lower Base Address (DPLBASE)—Offset 70h	0h
74h	77h	DMA Position Upper Base Address (DPUBASE)—Offset 74h	0h
80h	83h	Input/Output Stream Descriptor x Control (ISD0CTL)—Offset 80h	40000h

Table 5-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
83h	83h	Input/Output Stream Descriptor x Status (ISD0STS)—Offset 83h	0h
84h	87h	Input/Output Stream Descriptor x Link Position in Buffer (ISD0LPIB)—Offset 84h	0h
88h	8Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD0CBL)—Offset 88h	0h
8Ch	8Dh	Input/Output Stream Descriptor x Last Valid Index (ISD0LVI)—Offset 8Ch	0h
8Eh	8Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD0FIFOW)—Offset 8Eh	4h
90h	91h	Input/Output Stream Descriptor x FIFO Size (ISD0FIFOS)—Offset 90h	0h
92h	93h	Input/Output Stream Descriptor x Format (ISD0FMT)—Offset 92h	0h
94h	95h	Input/Output Stream Descriptor x FIFO Limit (ISD0FIFOL)—Offset 94h	0h
98h	9Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD0BDLPLBA)—Offset 98h	0h
9Ch	9Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD0BDLPUBA)—Offset 9Ch	0h
A0h	A0h	Input/Output Stream Descriptor x Control (ISD1CTLB0)—Offset A0h	0h
A0h	A3h	Input/Output Stream Descriptor x Control (ISD1CTL)—Offset A0h	0h
A2h	A2h	Input/Output Stream Descriptor x Control (ISD1CTLB2)—Offset A2h	0h
A3h	A3h	Input/Output Stream Descriptor x Status (ISD1STS)—Offset A3h	0h
A4h	A7h	Input/Output Stream Descriptor x Link Position in Buffer (ISD1LPIB)—Offset A4h	0h
A8h	ABh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD1CBL)—Offset A8h	0h
ACh	ADh	Input/Output Stream Descriptor x Last Valid Index (ISD1LVI)—Offset ACh	0h
AEh	AFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD1FIFOW)—Offset AEh	0h
B0h	B1h	Input/Output Stream Descriptor x FIFO Size (ISD1FIFOS)—Offset B0h	0h
B2h	B3h	Input/Output Stream Descriptor x Format (ISD1FMT)—Offset B2h	0h
B4h	B5h	Input/Output Stream Descriptor x FIFO Limit (ISD1FIFOL)—Offset B4h	0h
B8h	BBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD1BDLPLBA)—Offset B8h	0h
BCh	BFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD1BDLPUBA)—Offset BCh	0h
C0h	C3h	Input/Output Stream Descriptor x Control (ISD2CTL)—Offset C0h	0h
C3h	C3h	Input/Output Stream Descriptor x Status (ISD2STS)—Offset C3h	0h
C4h	C7h	Input/Output Stream Descriptor x Link Position in Buffer (ISD2LPIB)—Offset C4h	0h
C8h	CBh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD2CBL)—Offset C8h	0h
CCh	CDh	Input/Output Stream Descriptor x Last Valid Index (ISD2LVI)—Offset CCh	0h
CEh	CFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD2FIFOW)—Offset CEh	0h
D0h	D1h	Input/Output Stream Descriptor x FIFO Size (ISD2FIFOS)—Offset D0h	0h
D2h	D3h	Input/Output Stream Descriptor x Format (ISD2FMT)—Offset D2h	0h
D4h	D5h	Input/Output Stream Descriptor x FIFO Limit (ISD2FIFOL)—Offset D4h	0h
D8h	DBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD2BDLPLBA)—Offset D8h	0h
DCh	DFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD2BDLPUBA)—Offset DCh	0h
E0h	E3h	Input/Output Stream Descriptor x Control (ISD3CTL)—Offset E0h	0h

Table 5-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
E0h	E0h	Input/Output Stream Descriptor x Control (ISD3CTLB0)—Offset E0h	0h
E3h	E3h	Input/Output Stream Descriptor x Status (ISD3STS)—Offset E3h	0h
E4h	E7h	Input/Output Stream Descriptor x Link Position in Buffer (ISD3LPIB)—Offset E4h	0h
E8h	EBh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD3CBL)—Offset E8h	0h
ECh	EDh	Input/Output Stream Descriptor x Last Valid Index (ISD3LVI)—Offset ECh	0h
EEh	EFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD3FIFOW)—Offset EEh	0h
F0h	F1h	Input/Output Stream Descriptor x FIFO Size (ISD3FIFOS)—Offset F0h	0h
F2h	F3h	Input/Output Stream Descriptor x Format (ISD3FMT)—Offset F2h	0h
F4h	F5h	Input/Output Stream Descriptor x FIFO Limit (ISD3FIFOL)—Offset F4h	0h
F8h	FBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD3BDLPLBA)—Offset F8h	0h
FCh	FFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD3BDLPUBA)—Offset FCh	0h
100h	103h	Input/Output Stream Descriptor x Control (ISD4CTL)—Offset 100h	0h
103h	103h	Input/Output Stream Descriptor x Status (ISD4STS)—Offset 103h	0h
104h	107h	Input/Output Stream Descriptor x Link Position in Buffer (ISD4LPIB)—Offset 104h	0h
108h	10Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD4CBL)—Offset 108h	0h
10Ch	10Dh	Input/Output Stream Descriptor x Last Valid Index (ISD4LVI)—Offset 10Ch	0h
10Eh	10Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD4FIFOW)—Offset 10Eh	0h
110h	111h	Input/Output Stream Descriptor x FIFO Size (ISD4FIFOS)—Offset 110h	0h
112h	113h	Input/Output Stream Descriptor x Format (ISD4FMT)—Offset 112h	0h
114h	115h	Input/Output Stream Descriptor x FIFO Limit (ISD4FIFOL)—Offset 114h	0h
118h	11Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD4BDLPLBA)—Offset 118h	0h
11Ch	11Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD4BDLPUBA)—Offset 11Ch	0h
120h	123h	Input/Output Stream Descriptor x Control (ISD5CTL)—Offset 120h	0h
123h	123h	Input/Output Stream Descriptor x Status (ISD5STS)—Offset 123h	0h
124h	127h	Input/Output Stream Descriptor x Link Position in Buffer (ISD5LPIB)—Offset 124h	0h
128h	12Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD5CBL)—Offset 128h	0h
12Ch	12Dh	Input/Output Stream Descriptor x Last Valid Index (ISD5LVI)—Offset 12Ch	0h
12Eh	12Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD5FIFOW)—Offset 12Eh	0h
130h	131h	Input/Output Stream Descriptor x FIFO Size (ISD5FIFOS)—Offset 130h	0h
132h	133h	Input/Output Stream Descriptor x Format (ISD5FMT)—Offset 132h	0h
134h	135h	Input/Output Stream Descriptor x FIFO Limit (ISD5FIFOL)—Offset 134h	0h
138h	13Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD5BDLPLBA)—Offset 138h	0h
13Ch	13Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD5BDLPUBA)—Offset 13Ch	0h
140h	143h	Input/Output Stream Descriptor x Control (ISD6CTL)—Offset 140h	0h
143h	143h	Input/Output Stream Descriptor x Status (ISD6STS)—Offset 143h	0h

Table 5-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
144h	147h	Input/Output Stream Descriptor x Link Position in Buffer (ISD6LPIB)—Offset 144h	0h
148h	14Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD6CBL)—Offset 148h	0h
14Ch	14Dh	Input/Output Stream Descriptor x Last Valid Index (ISD6LVI)—Offset 14Ch	0h
14Eh	14Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD6FIFOW)—Offset 14Eh	0h
150h	151h	Input/Output Stream Descriptor x FIFO Size (ISD6FIFOS)—Offset 150h	0h
152h	153h	Input/Output Stream Descriptor x Format (ISD6FMT)—Offset 152h	0h
154h	155h	Input/Output Stream Descriptor x FIFO Limit (ISD6FIFOL)—Offset 154h	0h
158h	15Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD6BDLPLBA)—Offset 158h	0h
15Ch	15Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD6BDLPUBA)—Offset 15Ch	0h
180h	183h	Input/Output Stream Descriptor x Control (OSD1CTL)—Offset 180h	0h
183h	183h	Input/Output Stream Descriptor x Status (OSD1STS)—Offset 183h	0h
184h	187h	Input/Output Stream Descriptor x Link Position in Buffer (OSD1LPIB)—Offset 184h	0h
188h	18Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD1CBL)—Offset 188h	0h
18Ch	18Dh	Input/Output Stream Descriptor x Last Valid Index (OSD1LVI)—Offset 18Ch	0h
18Eh	18Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD1FIFOW)—Offset 18Eh	0h
190h	191h	Input/Output Stream Descriptor x FIFO Size (OSD1FIFOS)—Offset 190h	0h
192h	193h	Input/Output Stream Descriptor x Format (OSD1FMT)—Offset 192h	0h
194h	195h	Input/Output Stream Descriptor x FIFO Limit (OSD1FIFOL)—Offset 194h	0h
198h	19Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD1BDLPLBA)—Offset 198h	0h
19Ch	19Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD1BDLPUBA)—Offset 19Ch	0h
1A0h	1A3h	Input/Output Stream Descriptor x Control (OSD2CTL)—Offset 1A0h	0h
1A3h	1A3h	Input/Output Stream Descriptor x Status (OSD2STS)—Offset 1A3h	0h
1A4h	1A7h	Input/Output Stream Descriptor x Link Position in Buffer (OSD2LPIB)—Offset 1A4h	0h
1A8h	1ABh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD2CBL)—Offset 1A8h	0h
1ACh	1ADh	Input/Output Stream Descriptor x Last Valid Index (OSD2LVI)—Offset 1ACh	0h
1AEh	1AFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD2FIFOW)—Offset 1AEh	0h
1B0h	1B1h	Input/Output Stream Descriptor x FIFO Size (OSD2FIFOS)—Offset 1B0h	0h
1B2h	1B3h	Input/Output Stream Descriptor x Format (OSD2FMT)—Offset 1B2h	0h
1B4h	1B5h	Input/Output Stream Descriptor x FIFO Limit (OSD2FIFOL)—Offset 1B4h	0h
1B8h	1BBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD2BDLPLBA)—Offset 1B8h	0h
1BCh	1BFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD2BDLPUBA)—Offset 1BCh	0h
1C0h	1C0h	Input/Output Stream Descriptor x Control (OSD3CTLB0)—Offset 1C0h	0h
1C0h	1C3h	Input/Output Stream Descriptor x Control (OSD3CTL)—Offset 1C0h	0h
1C2h	1C2h	Input/Output Stream Descriptor x Control (OSD3CTLB2)—Offset 1C2h	0h
1C3h	1C3h	Input/Output Stream Descriptor x Status (OSD3STS)—Offset 1C3h	0h

Table 5-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1C4h	1C7h	Input/Output Stream Descriptor x Link Position in Buffer (OSD3LPIB)—Offset 1C4h	0h
1C8h	1CBh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD3CBL)—Offset 1C8h	0h
1CCh	1CDh	Input/Output Stream Descriptor x Last Valid Index (OSD3LVI)—Offset 1CCh	0h
1CEh	1CFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD3FIFOW)—Offset 1CEh	0h
1D0h	1D1h	Input/Output Stream Descriptor x FIFO Size (OSD3FIFOS)—Offset 1D0h	0h
1D2h	1D3h	Input/Output Stream Descriptor x Format (OSD3FMT)—Offset 1D2h	0h
1D4h	1D5h	Input/Output Stream Descriptor x FIFO Limit (OSD3FIFOL)—Offset 1D4h	0h
1D8h	1DBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD3BDLPLBA)—Offset 1D8h	0h
1DCh	1DFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD3BDLPUBA)—Offset 1DCh	0h
1E0h	1E3h	Input/Output Stream Descriptor x Control (OSD4CTL)—Offset 1E0h	0h
1E3h	1E3h	Input/Output Stream Descriptor x Status (OSD4STS)—Offset 1E3h	0h
1E4h	1E7h	Input/Output Stream Descriptor x Link Position in Buffer (OSD4LPIB)—Offset 1E4h	0h
1E8h	1EBh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD4CBL)—Offset 1E8h	0h
1ECh	1EDh	Input/Output Stream Descriptor x Last Valid Index (OSD4LVI)—Offset 1ECh	0h
1EEh	1EFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD4FIFOW)—Offset 1EEh	0h
1F0h	1F1h	Input/Output Stream Descriptor x FIFO Size (OSD4FIFOS)—Offset 1F0h	0h
1F2h	1F3h	Input/Output Stream Descriptor x Format (OSD4FMT)—Offset 1F2h	0h
1F4h	1F5h	Input/Output Stream Descriptor x FIFO Limit (OSD4FIFOL)—Offset 1F4h	0h
1F8h	1FBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD4BDLPLBA)—Offset 1F8h	0h
1FCh	1FFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD4BDLPUBA)—Offset 1FCh	0h
200h	203h	Input/Output Stream Descriptor x Control (OSD5CTL)—Offset 200h	0h
203h	203h	Input/Output Stream Descriptor x Status (OSD5STS)—Offset 203h	0h
204h	207h	Input/Output Stream Descriptor x Link Position in Buffer (OSD5LPIB)—Offset 204h	0h
208h	20Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD5CBL)—Offset 208h	0h
20Ch	20Dh	Input/Output Stream Descriptor x Last Valid Index (OSD5LVI)—Offset 20Ch	0h
20Eh	20Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD5FIFOW)—Offset 20Eh	0h
210h	211h	Input/Output Stream Descriptor x FIFO Size (OSD5FIFOS)—Offset 210h	0h
212h	213h	Input/Output Stream Descriptor x Format (OSD5FMT)—Offset 212h	0h
214h	215h	Input/Output Stream Descriptor x FIFO Limit (OSD5FIFOL)—Offset 214h	0h
218h	21Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD5BDLPLBA)—Offset 218h	0h
21Ch	21Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD5BDLPUBA)—Offset 21Ch	0h
220h	223h	Input/Output Stream Descriptor x Control (OSD6CTL)—Offset 220h	0h
223h	223h	Input/Output Stream Descriptor x Status (OSD6STS)—Offset 223h	0h
224h	227h	Input/Output Stream Descriptor x Link Position in Buffer (OSD6LPIB)—Offset 224h	0h
228h	22Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD6CBL)—Offset 228h	0h

Table 5-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
22Ch	22Dh	Input/Output Stream Descriptor x Last Valid Index (OSD6LVI)—Offset 22Ch	0h
22Eh	22Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD6FIFOW)—Offset 22Eh	0h
230h	231h	Input/Output Stream Descriptor x FIFO Size (OSD6FIFOS)—Offset 230h	0h
232h	233h	Input/Output Stream Descriptor x Format (OSD6FMT)—Offset 232h	0h
234h	235h	Input/Output Stream Descriptor x FIFO Limit (OSD6FIFOL)—Offset 234h	0h
238h	23Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD6BDLPLBA)—Offset 238h	0h
23Ch	23Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD6BDLPUBA)—Offset 23Ch	0h
240h	240h	Input/Output Stream Descriptor x Control (OSD7CTLB0)—Offset 240h	0h
240h	243h	Input/Output Stream Descriptor x Control (OSD7CTL)—Offset 240h	0h
242h	242h	Input/Output Stream Descriptor x Control (OSD7CTLB2)—Offset 242h	0h
243h	243h	Input/Output Stream Descriptor x Status (OSD7STS)—Offset 243h	0h
244h	247h	Input/Output Stream Descriptor x Link Position in Buffer (OSD7LPIB)—Offset 244h	0h
248h	24Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD7CBL)—Offset 248h	0h
24Ch	24Dh	Input/Output Stream Descriptor x Last Valid Index (OSD7LVI)—Offset 24Ch	0h
24Eh	24Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD7FIFOW)—Offset 24Eh	0h
250h	251h	Input/Output Stream Descriptor x FIFO Size (OSD7FIFOS)—Offset 250h	0h
252h	253h	Input/Output Stream Descriptor x Format (OSD7FMT)—Offset 252h	0h
254h	255h	Input/Output Stream Descriptor x FIFO Limit (OSD7FIFOL)—Offset 254h	0h
258h	25Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD7BDLPLBA)—Offset 258h	0h
25Ch	25Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD7BDLPUBA)—Offset 25Ch	0h
260h	263h	Input/Output Stream Descriptor x Control (OSD8CTL)—Offset 260h	0h
263h	263h	Input/Output Stream Descriptor x Status (OSD8STS)—Offset 263h	0h
264h	267h	Input/Output Stream Descriptor x Link Position in Buffer (OSD8LPIB)—Offset 264h	0h
268h	26Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD8CBL)—Offset 268h	0h
26Ch	26Dh	Input/Output Stream Descriptor x Last Valid Index (OSD8LVI)—Offset 26Ch	0h
26Eh	26Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD8FIFOW)—Offset 26Eh	0h
270h	271h	Input/Output Stream Descriptor x FIFO Size (OSD8FIFOS)—Offset 270h	0h
272h	273h	Input/Output Stream Descriptor x Format (OSD8FMT)—Offset 272h	0h
274h	275h	Input/Output Stream Descriptor x FIFO Limit (OSD8FIFOL)—Offset 274h	0h
278h	27Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD8BDLPLBA)—Offset 278h	0h
27Ch	27Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD8BDLPUBA)—Offset 27Ch	0h
280h	283h	Input/Output Stream Descriptor x Control (ISD7CTL)—Offset 280h	0h
283h	283h	Input/Output Stream Descriptor x Status (ISD7STS)—Offset 283h	0h
284h	287h	Input/Output Stream Descriptor x Link Position in Buffer (ISD7LPIB)—Offset 284h	0h
288h	28Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD7CBL)—Offset 288h	0h

Table 5-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
28Ch	28Dh	Input/Output Stream Descriptor x Last Valid Index (ISD7LVI)—Offset 28Ch	0h
28Eh	28Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD7FIFOW)—Offset 28Eh	0h
290h	291h	Input/Output Stream Descriptor x FIFO Size (ISD7FIFOS)—Offset 290h	0h
292h	293h	Input/Output Stream Descriptor x Format (ISD7FMT)—Offset 292h	0h
294h	295h	Input/Output Stream Descriptor x FIFO Limit (ISD7FIFOL)—Offset 294h	0h
298h	29Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD7BDLPLBA)—Offset 298h	0h
29Ch	29Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD7BDLPUBA)—Offset 29Ch	0h
2A0h	2A3h	Input/Output Stream Descriptor x Control (ISD8CTL)—Offset 2A0h	0h
2A3h	2A3h	Input/Output Stream Descriptor x Status (ISD8STS)—Offset 2A3h	0h
2A4h	2A7h	Input/Output Stream Descriptor x Link Position in Buffer (ISD8LPIB)—Offset 2A4h	0h
2A8h	2ABh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD8CBL)—Offset 2A8h	0h
2ACh	2ADh	Input/Output Stream Descriptor x Last Valid Index (ISD8LVI)—Offset 2ACh	0h
2AEh	2AFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD8FIFOW)—Offset 2AEh	0h
2B0h	2B1h	Input/Output Stream Descriptor x FIFO Size (ISD8FIFOS)—Offset 2B0h	0h
2B2h	2B3h	Input/Output Stream Descriptor x Format (ISD8FMT)—Offset 2B2h	0h
2B4h	2B5h	Input/Output Stream Descriptor x FIFO Limit (ISD8FIFOL)—Offset 2B4h	0h
2B8h	2BBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD8BDLPLBA)—Offset 2B8h	0h
2BCh	2BFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD8BDLPUBA)—Offset 2BCh	0h
2C0h	2C3h	Input/Output Stream Descriptor x Control (ISD9CTL)—Offset 2C0h	0h
2C3h	2C3h	Input/Output Stream Descriptor x Status (ISD9STS)—Offset 2C3h	0h
2C4h	2C7h	Input/Output Stream Descriptor x Link Position in Buffer (ISD9LPIB)—Offset 2C4h	0h
2C8h	2CBh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD9CBL)—Offset 2C8h	0h
2CCh	2CDh	Input/Output Stream Descriptor x Last Valid Index (ISD9LVI)—Offset 2CCh	0h
2CEh	2CFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD9FIFOW)—Offset 2CEh	0h
2D0h	2D1h	Input/Output Stream Descriptor x FIFO Size (ISD9FIFOS)—Offset 2D0h	0h
2D2h	2D3h	Input/Output Stream Descriptor x Format (ISD9FMT)—Offset 2D2h	0h
2D4h	2D5h	Input/Output Stream Descriptor x FIFO Limit (ISD9FIFOL)—Offset 2D4h	0h
2D8h	2DBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD9BDLPLBA)—Offset 2D8h	0h
2DCh	2DFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD9BDLPUBA)—Offset 2DCh	0h
2E0h	2E3h	Input/Output Stream Descriptor x Control (ISD10CTL)—Offset 2E0h	0h
2E3h	2E3h	Input/Output Stream Descriptor x Status (ISD10STS)—Offset 2E3h	0h
2E4h	2E7h	Input/Output Stream Descriptor x Link Position in Buffer (ISD10LPIB)—Offset 2E4h	0h
2E8h	2EBh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD10CBL)—Offset 2E8h	0h
2ECh	2EDh	Input/Output Stream Descriptor x Last Valid Index (ISD10LVI)—Offset 2ECh	0h

Table 5-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
2EEh	2EFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD10FIFOW)—Offset 2EEh	0h
2F0h	2F1h	Input/Output Stream Descriptor x FIFO Size (ISD10FIFOS)—Offset 2F0h	0h
2F2h	2F3h	Input/Output Stream Descriptor x Format (ISD10FMT)—Offset 2F2h	0h
2F4h	2F5h	Input/Output Stream Descriptor x FIFO Limit (ISD10FIFOL)—Offset 2F4h	0h
2F8h	2FBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD10BDLPLBA)—Offset 2F8h	0h
2FCh	2FFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD10BDLPUBA)—Offset 2FCh	0h
300h	303h	Input/Output Stream Descriptor x Control (ISD11CTL)—Offset 300h	0h
303h	303h	Input/Output Stream Descriptor x Status (ISD11STS)—Offset 303h	0h
304h	307h	Input/Output Stream Descriptor x Link Position in Buffer (ISD11LPIB)—Offset 304h	0h
308h	30Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD11CBL)—Offset 308h	0h
30Ch	30Dh	Input/Output Stream Descriptor x Last Valid Index (ISD11LVI)—Offset 30Ch	0h
30Eh	30Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD11FIFOW)—Offset 30Eh	0h
310h	311h	Input/Output Stream Descriptor x FIFO Size (ISD11FIFOS)—Offset 310h	0h
312h	313h	Input/Output Stream Descriptor x Format (ISD11FMT)—Offset 312h	0h
314h	315h	Input/Output Stream Descriptor x FIFO Limit (ISD11FIFOL)—Offset 314h	0h
318h	31Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD11BDLPLBA)—Offset 318h	0h
31Ch	31Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD11BDLPUBA)—Offset 31Ch	0h
320h	323h	Input/Output Stream Descriptor x Control (ISD12CTL)—Offset 320h	0h
323h	323h	Input/Output Stream Descriptor x Status (ISD12STS)—Offset 323h	0h
324h	327h	Input/Output Stream Descriptor x Link Position in Buffer (ISD12LPIB)—Offset 324h	0h
328h	32Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD12CBL)—Offset 328h	0h
32Ch	32Dh	Input/Output Stream Descriptor x Last Valid Index (ISD12LVI)—Offset 32Ch	0h
32Eh	32Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD12FIFOW)—Offset 32Eh	0h
330h	331h	Input/Output Stream Descriptor x FIFO Size (ISD12FIFOS)—Offset 330h	0h
332h	333h	Input/Output Stream Descriptor x Format (ISD12FMT)—Offset 332h	0h
334h	335h	Input/Output Stream Descriptor x FIFO Limit (ISD12FIFOL)—Offset 334h	0h
338h	33Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD12BDLPLBA)—Offset 338h	0h
33Ch	33Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD12BDLPUBA)—Offset 33Ch	0h
340h	343h	Input/Output Stream Descriptor x Control (ISD13CTL)—Offset 340h	0h
343h	343h	Input/Output Stream Descriptor x Status (ISD13STS)—Offset 343h	0h
344h	347h	Input/Output Stream Descriptor x Link Position in Buffer (ISD13LPIB)—Offset 344h	0h
348h	34Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD13CBL)—Offset 348h	0h
34Ch	34Dh	Input/Output Stream Descriptor x Last Valid Index (ISD13LVI)—Offset 34Ch	0h
34Eh	34Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD13FIFOW)—Offset 34Eh	0h

Table 5-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
350h	351h	Input/Output Stream Descriptor x FIFO Size (ISD13FIFOS)—Offset 350h	0h
352h	353h	Input/Output Stream Descriptor x Format (ISD13FMT)—Offset 352h	0h
354h	355h	Input/Output Stream Descriptor x FIFO Limit (ISD13FIFOL)—Offset 354h	0h
358h	35Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD13BDLPLBA)—Offset 358h	0h
35Ch	35Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD13BDLPUBA)—Offset 35Ch	0h
360h	363h	Input/Output Stream Descriptor x Control (ISD14CTL)—Offset 360h	0h
363h	363h	Input/Output Stream Descriptor x Status (ISD14STS)—Offset 363h	0h
364h	367h	Input/Output Stream Descriptor x Link Position in Buffer (ISD14LPIB)—Offset 364h	0h
368h	36Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (ISD14CBL)—Offset 368h	0h
36Ch	36Dh	Input/Output Stream Descriptor x Last Valid Index (ISD14LVI)—Offset 36Ch	0h
36Eh	36Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD14FIFOW)—Offset 36Eh	0h
370h	371h	Input/Output Stream Descriptor x FIFO Size (ISD14FIFOS)—Offset 370h	0h
372h	373h	Input/Output Stream Descriptor x Format (ISD14FMT)—Offset 372h	0h
374h	375h	Input/Output Stream Descriptor x FIFO Limit (ISD14FIFOL)—Offset 374h	0h
378h	37Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD14BDLPLBA)—Offset 378h	0h
37Ch	37Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD14BDLPUBA)—Offset 37Ch	0h
380h	383h	Input/Output Stream Descriptor x Control (OSD9CTL)—Offset 380h	0h
383h	383h	Input/Output Stream Descriptor x Status (OSD9STS)—Offset 383h	0h
384h	387h	Input/Output Stream Descriptor x Link Position in Buffer (OSD9LPIB)—Offset 384h	0h
388h	38Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD9CBL)—Offset 388h	0h
38Ch	38Dh	Input/Output Stream Descriptor x Last Valid Index (OSD9LVI)—Offset 38Ch	0h
38Eh	38Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD9FIFOW)—Offset 38Eh	0h
390h	391h	Input/Output Stream Descriptor x FIFO Size (OSD9FIFOS)—Offset 390h	0h
392h	393h	Input/Output Stream Descriptor x Format (OSD9FMT)—Offset 392h	0h
394h	395h	Input/Output Stream Descriptor x FIFO Limit (OSD9FIFOL)—Offset 394h	0h
398h	39Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD9BDLPLBA)—Offset 398h	0h
39Ch	39Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD9BDLPUBA)—Offset 39Ch	0h
3A0h	3A3h	Input/Output Stream Descriptor x Control (OSD10CTL)—Offset 3A0h	0h
3A3h	3A3h	Input/Output Stream Descriptor x Status (OSD10STS)—Offset 3A3h	0h
3A4h	3A7h	Input/Output Stream Descriptor x Link Position in Buffer (OSD10LPIB)—Offset 3A4h	0h
3A8h	3ABh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD10CBL)—Offset 3A8h	0h
3ACh	3ADh	Input/Output Stream Descriptor x Last Valid Index (OSD10LVI)—Offset 3ACh	0h
3AEh	3AFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD10FIFOW)—Offset 3AEh	0h
3B0h	3B1h	Input/Output Stream Descriptor x FIFO Size (OSD10FIFOS)—Offset 3B0h	0h
3B2h	3B3h	Input/Output Stream Descriptor x Format (OSD10FMT)—Offset 3B2h	0h

Table 5-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3B4h	3B5h	Input/Output Stream Descriptor x FIFO Limit (OSD10FIFOL)—Offset 3B4h	0h
3B8h	3BBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD10BDLPLBA)—Offset 3B8h	0h
3BCh	3BFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD10BDLPUBA)—Offset 3BCh	0h
3C0h	3C3h	Input/Output Stream Descriptor x Control (OSD11CTL)—Offset 3C0h	0h
3C3h	3C3h	Input/Output Stream Descriptor x Status (OSD11STS)—Offset 3C3h	0h
3C4h	3C7h	Input/Output Stream Descriptor x Link Position in Buffer (OSD11LPIB)—Offset 3C4h	0h
3C8h	3CBh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD11CBL)—Offset 3C8h	0h
3CCh	3CDh	Input/Output Stream Descriptor x Last Valid Index (OSD11LVI)—Offset 3CCh	0h
3CEh	3CFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD11FIFOW)—Offset 3CEh	0h
3D0h	3D1h	Input/Output Stream Descriptor x FIFO Size (OSD11FIFOS)—Offset 3D0h	0h
3D2h	3D3h	Input/Output Stream Descriptor x Format (OSD11FMT)—Offset 3D2h	0h
3D4h	3D5h	Input/Output Stream Descriptor x FIFO Limit (OSD11FIFOL)—Offset 3D4h	0h
3D8h	3DBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD11BDLPLBA)—Offset 3D8h	0h
3DCh	3DFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD11BDLPUBA)—Offset 3DCh	0h
3E0h	3E3h	Input/Output Stream Descriptor x Control (OSD12CTL)—Offset 3E0h	0h
3E3h	3E3h	Input/Output Stream Descriptor x Status (OSD12STS)—Offset 3E3h	0h
3E4h	3E7h	Input/Output Stream Descriptor x Link Position in Buffer (OSD12LPIB)—Offset 3E4h	0h
3E8h	3EBh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD12CBL)—Offset 3E8h	0h
3ECh	3EDh	Input/Output Stream Descriptor x Last Valid Index (OSD12LVI)—Offset 3ECh	0h
3EEh	3EFh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD12FIFOW)—Offset 3EEh	0h
3F0h	3F1h	Input/Output Stream Descriptor x FIFO Size (OSD12FIFOS)—Offset 3F0h	0h
3F2h	3F3h	Input/Output Stream Descriptor x Format (OSD12FMT)—Offset 3F2h	0h
3F4h	3F5h	Input/Output Stream Descriptor x FIFO Limit (OSD12FIFOL)—Offset 3F4h	0h
3F8h	3FBh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD12BDLPLBA)—Offset 3F8h	0h
3FCh	3FFh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD12BDLPUBA)—Offset 3FCh	0h
400h	403h	Input/Output Stream Descriptor x Control (OSD13CTL)—Offset 400h	0h
403h	403h	Input/Output Stream Descriptor x Status (OSD13STS)—Offset 403h	0h
404h	407h	Input/Output Stream Descriptor x Link Position in Buffer (OSD13LPIB)—Offset 404h	0h
408h	40Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD13CBL)—Offset 408h	0h
40Ch	40Dh	Input/Output Stream Descriptor x Last Valid Index (OSD13LVI)—Offset 40Ch	0h
40Eh	40Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD13FIFOW)—Offset 40Eh	0h
410h	411h	Input/Output Stream Descriptor x FIFO Size (OSD13FIFOS)—Offset 410h	0h
412h	413h	Input/Output Stream Descriptor x Format (OSD13FMT)—Offset 412h	0h
414h	415h	Input/Output Stream Descriptor x FIFO Limit (OSD13FIFOL)—Offset 414h	0h

Table 5-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
418h	41Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD13BDLPLBA)—Offset 418h	0h
41Ch	41Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD13BDLPUBA)—Offset 41Ch	0h
420h	423h	Input/Output Stream Descriptor x Control (OSD14CTL)—Offset 420h	0h
423h	423h	Input/Output Stream Descriptor x Status (OSD14STS)—Offset 423h	0h
424h	427h	Input/Output Stream Descriptor x Link Position in Buffer (OSD14LPIB)—Offset 424h	0h
428h	42Bh	Input/Output Stream Descriptor x Cyclic Buffer Length (OSD14CBL)—Offset 428h	0h
42Ch	42Dh	Input/Output Stream Descriptor x Last Valid Index (OSD14LVI)—Offset 42Ch	0h
42Eh	42Fh	Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD14FIFOW)—Offset 42Eh	0h
430h	431h	Input/Output Stream Descriptor x FIFO Size (OSD14FIFOS)—Offset 430h	0h
432h	433h	Input/Output Stream Descriptor x Format (OSD14FMT)—Offset 432h	0h
434h	435h	Input/Output Stream Descriptor x FIFO Limit (OSD14FIFOL)—Offset 434h	0h
438h	43Bh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD14BDLPLBA)—Offset 438h	0h
43Ch	43Fh	Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD14BDLPUBA)—Offset 43Ch	0h
500h	503h	Global Time Synchronization Capability Header (GTSCH)—Offset 500h	11F00h
504h	507h	Global Time Synchronization Capability Declaration (GTSCD)—Offset 504h	0h
520h	523h	Global Time Synchronization Capture Control (GTSCC0)—Offset 520h	0h
524h	527h	Wall Frame Counter Captured (WALFCC0)—Offset 524h	0h
528h	52Bh	Time Stamp Counter Captured Lower (TSCCL0)—Offset 528h	0h
52Ch	52Fh	Time Stamp Counter Captured Upper (TSCCU0)—Offset 52Ch	0h
534h	537h	Linear Link Position Frame Offset Captured (LLPFOC0)—Offset 534h	0h
538h	53Bh	Linear Link Position Captured Lower (LLPCL0)—Offset 538h	0h
53Ch	53Fh	Linear Link Position Captured Upper (LLPCU0)—Offset 53Ch	0h
540h	543h	Global Time Synchronization Capture Control (GTSCC1)—Offset 540h	0h
544h	547h	Wall Frame Counter Captured (WALFCC1)—Offset 544h	0h
548h	54Bh	Time Stamp Counter Captured Lower (TSCCL1)—Offset 548h	0h
54Ch	54Fh	Time Stamp Counter Captured Upper (TSCCU1)—Offset 54Ch	0h
554h	557h	Linear Link Position Frame Offset Captured (LLPFOC1)—Offset 554h	0h
558h	55Bh	Linear Link Position Captured Lower (LLPCL1)—Offset 558h	0h
55Ch	55Fh	Linear Link Position Captured Upper (LLPCU1)—Offset 55Ch	0h
800h	803h	Processing Pipe Capability Header (PPCH)—Offset 800h	30500h
804h	807h	Processing Pipe Control (PPCTL)—Offset 804h	0h
808h	80Bh	Processing Pipe Status (PPSTS)—Offset 808h	0h
810h	813h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC0LLPL)—Offset 810h	0h
814h	817h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC0LLPU)—Offset 814h	0h
818h	81Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC0LDPL)—Offset 818h	0h

Table 5-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
81Ch	81Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC0LDPU)—Offset 81Ch	0h
910h	913h	Input/Output Processing Pipe's Link Connection x Control (IPPLC0CTL)—Offset 910h	0h
914h	915h	Input/Output Processing Pipe's Link Connection x Format (IPPLC0FMT)—Offset 914h	0h
918h	91Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC0LLPL)—Offset 918h	0h
91Ch	91Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC0LLPU)—Offset 91Ch	0h
C00h	C03h	Multiple Links Capability Header (MLCH)—Offset C00h	20800h
C04h	C07h	Multiple Links Capability Declaration (MLCD)—Offset C04h	1h
C40h	C43h	Link x Capabilities (LCAP0)—Offset C40h	7h
C44h	C47h	Link Control 0 (LCTL0)—Offset C44h	10002h
C48h	C4Bh	Link x Output Stream ID Mapping Valid (LOSIDV0)—Offset C48h	FFFEh
C4Ch	C4Fh	Link 0 SDI Identifier (LSDIID0)—Offset C4Ch	3h
C50h	C50h	Link x Per Stream Output Overhead (LPSOO0)—Offset C50h	0h
C52h	C52h	Link x Per Stream Input Overhead (LPSIO0)—Offset C52h	0h
C58h	C5Bh	Link x Wall Frame Counter (LWALFC0)—Offset C58h	0h
C80h	C83h	Link x Capabilities (LCAP1)—Offset C80h	1Fh
C84h	C87h	Link x Control (LCTL1)—Offset C84h	10004h
C88h	C8Bh	Link 1 Output Stream ID Mapping Valid (LOSIDV1)—Offset C88h	FFFEh
C8Ch	C8Fh	Link 1 SDI Identifier (LSDIID1)—Offset C8Ch	4h
C90h	C90h	Link x Per Stream Output Overhead (LPSOO1)—Offset C90h	0h
C92h	C92h	Link x Per Stream Input Overhead (LPSIO1)—Offset C92h	0h
C98h	C9Bh	Link 1 Wall Frame Counter (LWALFC1)—Offset C98h	0h
4A10h	4A13h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC7LLPL)—Offset 4A10h	0h
4A14h	4A17h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC7LLPU)—Offset 4A14h	0h
4A18h	4A1Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC7LDPL)—Offset 4A18h	0h
4A1Ch	4A1Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC7LDPU)—Offset 4A1Ch	0h
4A20h	4A23h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC8LLPL)—Offset 4A20h	0h
4A24h	4A27h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC8LLPU)—Offset 4A24h	0h
4A28h	4A2Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC8LDPL)—Offset 4A28h	0h
4A2Ch	4A2Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC8LDPU)—Offset 4A2Ch	0h
4A30h	4A33h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC9LLPL)—Offset 4A30h	0h
4A34h	4A37h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC9LLPU)—Offset 4A34h	0h
4A38h	4A3Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC9LDPL)—Offset 4A38h	0h

Table 5-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4A3Ch	4A3Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC9LDPU)—Offset 4A3Ch	0h
4A40h	4A43h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC10LLPL)—Offset 4A40h	0h
4A44h	4A47h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC10LLPU)—Offset 4A44h	0h
4A48h	4A4Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC10LDPL)—Offset 4A48h	0h
4A4Ch	4A4Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC10LDPU)—Offset 4A4Ch	0h
4A50h	4A53h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC11LLPL)—Offset 4A50h	0h
4A54h	4A57h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC11LLPU)—Offset 4A54h	0h
4A58h	4A5Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC11LDPL)—Offset 4A58h	0h
4A5Ch	4A5Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC11LDPU)—Offset 4A5Ch	0h
4A60h	4A63h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC12LLPL)—Offset 4A60h	0h
4A64h	4A67h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC12LLPU)—Offset 4A64h	0h
4A68h	4A6Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC12LDPL)—Offset 4A68h	0h
4A6Ch	4A6Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC12LDPU)—Offset 4A6Ch	0h
4A70h	4A73h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC13LLPL)—Offset 4A70h	0h
4A74h	4A77h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC13LLPU)—Offset 4A74h	0h
4A78h	4A7Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC13LDPL)—Offset 4A78h	0h
4A7Ch	4A7Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC13LDPU)—Offset 4A7Ch	0h
4A80h	4A83h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC14LLPL)—Offset 4A80h	0h
4A84h	4A87h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC14LLPU)—Offset 4A84h	0h
4A88h	4A8Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC14LDPL)—Offset 4A88h	0h
4A8Ch	4A8Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC14LDPU)—Offset 4A8Ch	0h
4A90h	4A93h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC9LLPL)—Offset 4A90h	0h
4A94h	4A97h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC9LLPU)—Offset 4A94h	0h
4A98h	4A9Bh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC9LDPL)—Offset 4A98h	0h
4A9Ch	4A9Fh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC9LDPU)—Offset 4A9Ch	0h

Table 5-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4AA0h	4AA3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC10LLPL)—Offset 4AA0h	0h
4AA4h	4AA7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC10LLPU)—Offset 4AA4h	0h
4AA8h	4AABh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC10LDPL)—Offset 4AA8h	0h
4AACh	4AAFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC10LDPU)—Offset 4AACh	0h
4AB0h	4AB3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC11LLPL)—Offset 4AB0h	0h
4AB4h	4AB7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC11LLPU)—Offset 4AB4h	0h
4AB8h	4ABBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC11LDPL)—Offset 4AB8h	0h
4ABCh	4ABFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC11LDPU)—Offset 4ABCh	0h
4AC0h	4AC3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC12LLPL)—Offset 4AC0h	0h
4AC4h	4AC7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC12LLPU)—Offset 4AC4h	0h
4AC8h	4ACBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC12LDPL)—Offset 4AC8h	0h
4ACCh	4ACFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC12LDPU)—Offset 4ACCh	0h
4AD0h	4AD3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC13LLPL)—Offset 4AD0h	0h
4AD4h	4AD7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC13LLPU)—Offset 4AD4h	0h
4AD8h	4ADBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC13LDPL)—Offset 4AD8h	0h
4ADCh	4ADFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC13LDPU)—Offset 4ADCh	0h
4AE0h	4AE3h	Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC14LLPL)—Offset 4AE0h	0h
4AE4h	4AE7h	Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC14LLPU)—Offset 4AE4h	0h
4AE8h	4AEBh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC14LDPL)—Offset 4AE8h	0h
4AECh	4AEFh	Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC14LDPU)—Offset 4AECh	0h
4AF0h	4AF3h	Input/Output Processing Pipe's Link Connection x Control (IPPLC7CTL)—Offset 4AF0h	0h
4AF4h	4AF5h	Input/Output Processing Pipe's Link Connection x Format (IPPLC7FMT)—Offset 4AF4h	0h
4AF8h	4AFBh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC7LLPL)—Offset 4AF8h	0h
4AFCh	4AFFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC7LLPU)—Offset 4AFCh	0h
4B00h	4B03h	Input/Output Processing Pipe's Link Connection x Control (IPPLC8CTL)—Offset 4B00h	0h
4B04h	4B05h	Input/Output Processing Pipe's Link Connection x Format (IPPLC8FMT)—Offset 4B04h	0h
4B08h	4B0Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC8LLPL)—Offset 4B08h	0h

Table 5-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4B0Ch	4B0Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC8LLPU)—Offset 4B0Ch	0h
4B10h	4B13h	Input/Output Processing Pipe's Link Connection x Control (IPPLC9CTL)—Offset 4B10h	0h
4B14h	4B15h	Input/Output Processing Pipe's Link Connection x Format (IPPLC9FMT)—Offset 4B14h	0h
4B18h	4B1Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC9LLPL)—Offset 4B18h	0h
4B1Ch	4B1Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC9LLPU)—Offset 4B1Ch	0h
4B20h	4B23h	Input/Output Processing Pipe's Link Connection x Control (IPPLC10CTL)—Offset 4B20h	0h
4B24h	4B25h	Input/Output Processing Pipe's Link Connection x Format (IPPLC10FMT)—Offset 4B24h	0h
4B28h	4B2Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC10LLPL)—Offset 4B28h	0h
4B2Ch	4B2Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC10LLPU)—Offset 4B2Ch	0h
4B30h	4B33h	Input/Output Processing Pipe's Link Connection x Control (IPPLC11CTL)—Offset 4B30h	0h
4B34h	4B35h	Input/Output Processing Pipe's Link Connection x Format (IPPLC11FMT)—Offset 4B34h	0h
4B38h	4B3Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC11LLPL)—Offset 4B38h	0h
4B3Ch	4B3Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC11LLPU)—Offset 4B3Ch	0h
4B40h	4B43h	Input/Output Processing Pipe's Link Connection x Control (IPPLC12CTL)—Offset 4B40h	0h
4B44h	4B45h	Input/Output Processing Pipe's Link Connection x Format (IPPLC12FMT)—Offset 4B44h	0h
4B48h	4B4Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC12LLPL)—Offset 4B48h	0h
4B4Ch	4B4Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC12LLPU)—Offset 4B4Ch	0h
4B50h	4B53h	Input/Output Processing Pipe's Link Connection x Control (IPPLC13CTL)—Offset 4B50h	0h
4B54h	4B55h	Input/Output Processing Pipe's Link Connection x Format (IPPLC13FMT)—Offset 4B54h	0h
4B58h	4B5Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC13LLPL)—Offset 4B58h	0h
4B5Ch	4B5Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC13LLPU)—Offset 4B5Ch	0h
4B60h	4B63h	Input/Output Processing Pipe's Link Connection x Control (IPPLC14CTL)—Offset 4B60h	0h
4B64h	4B65h	Input/Output Processing Pipe's Link Connection x Format (IPPLC14FMT)—Offset 4B64h	0h
4B68h	4B6Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC14LLPL)—Offset 4B68h	0h
4B6Ch	4B6Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC14LLPU)—Offset 4B6Ch	0h
4B70h	4B73h	Input/Output Processing Pipe's Link Connection x Control (OPPLC9CTL)—Offset 4B70h	0h

Table 5-2. Summary of High Definition Audio Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
4B74h	4B75h	Input/Output Processing Pipe's Link Connection x Format (OPPLC9FMT)—Offset 4B74h	0h
4B78h	4B7Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC9LLPL)—Offset 4B78h	0h
4B7Ch	4B7Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC9LLPU)—Offset 4B7Ch	0h
4B80h	4B83h	Input/Output Processing Pipe's Link Connection x Control (OPPLC10CTL)—Offset 4B80h	0h
4B84h	4B85h	Input/Output Processing Pipe's Link Connection x Format (OPPLC10FMT)—Offset 4B84h	0h
4B88h	4B8Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC10LLPL)—Offset 4B88h	0h
4B8Ch	4B8Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC10LLPU)—Offset 4B8Ch	0h
4B90h	4B93h	Input/Output Processing Pipe's Link Connection x Control (OPPLC11CTL)—Offset 4B90h	0h
4B94h	4B95h	Input/Output Processing Pipe's Link Connection x Format (OPPLC11FMT)—Offset 4B94h	0h
4B98h	4B9Bh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC11LLPL)—Offset 4B98h	0h
4B9Ch	4B9Fh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC11LLPU)—Offset 4B9Ch	0h
4BA0h	4BA3h	Input/Output Processing Pipe's Link Connection x Control (OPPLC12CTL)—Offset 4BA0h	0h
4BA4h	4BA5h	Input/Output Processing Pipe's Link Connection x Format (OPPLC12FMT)—Offset 4BA4h	0h
4BA8h	4BABh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC12LLPL)—Offset 4BA8h	0h
4BACh	4BAFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC12LLPU)—Offset 4BACh	0h
4BB0h	4BB3h	Input/Output Processing Pipe's Link Connection x Control (OPPLC13CTL)—Offset 4BB0h	0h
4BB4h	4BB5h	Input/Output Processing Pipe's Link Connection x Format (OPPLC13FMT)—Offset 4BB4h	0h
4BB8h	4BBBh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC13LLPL)—Offset 4BB8h	0h
4BBCh	4BBFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC13LLPU)—Offset 4BBCh	0h
4BC0h	4BC3h	Input/Output Processing Pipe's Link Connection x Control (OPPLC14CTL)—Offset 4BC0h	0h
4BC4h	4BC5h	Input/Output Processing Pipe's Link Connection x Format (OPPLC14FMT)—Offset 4BC4h	0h
4BC8h	4BCBh	Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC14LLPL)—Offset 4BC8h	0h
4BCCh	4BCFh	Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC14LLPU)—Offset 4BCCh	0h

5.2.1 Global Capabilities (GCAP)—Offset 0h

This register indicates the capabilities of the controller.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 9701h

Bit Range	Default and Access	Field Name (ID): Description
15:12	9h RW/L	**Number of Output Streams Supported (OSS):** 0100b indicates that the Intel HD Audio controller supports four output streams. Reset value is hardcoded to parameter HSTOSC. Locked when FNCFG.BCLD = 1.
11:8	7h RW/L	**Number of Input Streams Supported (ISS):** 0100b indicates that the Intel HD Audio controller supports four input streams. Reset value is hardcoded to parameter HSTISC. Locked when FNCFG.BCLD = 1.
7:3	0h RO	**Number of Bidirectional Streams Supported (BSS):** 00000b indicates that the Intel HD Audio controller supports 0 bidirectional streams.
2:1	0h RW/L	**Number of Serial Data Out Signals (NSDO):** 00b indicates that the Intel HD Audio controller supports one Serial Data Output signal. For the case of multiple link segments is supported, this field indicates the number of SDO for link 0. Locked when FNCFG.BCLD = 1.
0	1h RW/L	**64 Bit Address Supported (ADD64OK):** A 1 indicates that the Intel HD Audio controller supports 64 bit addressing for BDL addresses, data buffer addresses, and command buffer addresses. Locked when FNCFG.BCLD = 1.

5.2.2 Minor Version (VMIN)—Offset 2h

This register indicates minor revision number of the High Definition Audio specification.

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW/L	**Minor Version (VMIN):** Indicates the Intel HD Audio controller supports minor revision number 00h of the Intel HD Audio specification.

5.2.3 Major Version (VMAJ)—Offset 3h

This register indicates major revision number of the High Definition Audio specification.

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
7:0	1h RW/L	**Major Version (VMAJ):** Indicates the Intel HD Audio controller supports major revision number 1 of the Intel HD Audio specification.

5.2.4 Output Payload Capability (OUTPAY)—Offset 4h

This register indicates the total output payload available on the link.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 3Ch

Bit Range	Default and Access	Field Name (ID): Description
15:0	3Ch RW/L	**Output Payload Capability (OUTPAY):** Indicates the total output payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 kHz frame. The default link clock speed of 24.000 MHz (the data is double pumped) provides 1000 bits per frame, or 62.5 words in total. 40 bits are used for command and control, leaving 60 words available for data payload. Note that this value does not reflect any bandwidth increase due to support for multiple SDO lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Note: In the event that multiple links is supported (GCAP2.LCOUNT) 0), the payload advertised will be the lowest common denominator offered by the default clock frequency on each link. Locked when FNCFG.BCLD = 1.

5.2.5 Input Payload Capability (INPAY)—Offset 6h

This register indicates the total input payload available on the link.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 1Dh

Bit Range	Default and Access	Field Name (ID): Description
15:0	1Dh RW/L	**Input Payload Capability (INPAY):** Indicates the total input payload available on the link. This does not include bandwidth used for response. This measurement is in 16-bit word quantities per 48 kHz frame. The default link clock speed of 24.000 MHz provides 500 bits per frame, or 31.25 words in total. 36 bits are used for response, leaving 29 words for data payload. Note that this value does not reflect any bandwidth increase due to support for multiple SDI lines. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload Note: In the event that multiple links is supported (GCAP2.LCOUNT) 0), the payload advertised will be the lowest common denominator offered by the default clock frequency on each link. Locked when FNCFG.BCLD = 1.

5.2.6 Global Control (GCTL)—Offset 8h

CRSTB bit is not affected by controller reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Accept Unsolicited Response Enable (UNSOL):** If UNSOL is a 1, Unsolicited Responses from the codecs are accepted by the controller and placed into the Response Input Ring Buffer. If UNSOL is a 0, unsolicited responses are not accepted, and dropped on the floor.
7:2	0h RO	Reserved.
1	0h RW/1S/V	**Flush Control (FCNTRL):** Writing a 1 to this bit initiates a flush. When the flush completion is received by the controller, hardware sets the Flush Status bit and clears this Flush Control bit. Before a flush cycle is initiated, the DMA Position Buffer must be programmed with a valid memory address by software, but the DMA Position Buffer bit 0 need not be set to enable the position reporting mechanism. Also, all streams must be stopped (the associated RUN bit must be 0). When the flush is initiated, the controller will flush pipelines to memory to guarantee that the hardware is ready to transition to a D3 state. Setting this bit is not a critical step in the power state transition if the content of the FIFOs is not critical.
0	0h RW/V	**Controller Reset# (CRSTB):** After the hardware has completed sequencing into the reset state, it will report a 0 in this bit. Software must read a 0 from this bit to verify that the controller is in reset. Writing a 1 to this bit causes the controller to exit its reset state and deassert the Intel HD Audio link RESET# signal. Software is responsible for setting/clearing this bit such that the minimum Intel HD Audio link RESET# signal assertion pulse width specification is met. When the controller hardware is ready to begin operation, it will report a 1 in this bit. Software must read a 1 from this bit before accessing any controller registers. The CRST bit defaults to a 0 after hardware reset, therefore software needs to write a 1 to this bit to begin operation. Note that the CORB/RIRB RUN bits and all Stream RUN bits must be verified cleared to zero before CRST bit is written to 0 (asserted) in order to assure a clean re-start. When setting or clearing CRST, software must ensure that minimum link timing requirements (minimum RESET# assertion time, etc.) are met. When CRST is 0 indicating that the controller is in reset, writes to all Intel HD Audio memory mapped registers are ignored as if the device is not present. The only exception is the Global Control register containing the CRST bit itself. The Global Control register is write-able as a DWord, Word, or Byte even when CRST is 0 if the byte enable for the byte containing the CRST bit (Byte Enable 0) is active. If Byte Enable 0 is not active, writes to the Global Control register will be ignored when CRST is 0. When CRST is 0, reads to Intel HD Audio memory mapped registers will return their default value except for registers that are not reset with PLTRST# or on a D3hot to D0 transition.

5.2.7 Wake Enable (WAKEEN)—Offset Ch

This register indicates which bits in the WAKESTS register may cause either a wake event or an interrupt.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:3	0h RO	Reserved.
2:0	0h RW	**SDIN Wake Enable Flags (WAKEEN):** Bits which control which SDI signal(s) may generate a wake event. A 1 bit in the bit mask indicates that the associated SDIN signal is enabled to generate a wake. These bits are cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

5.2.8 Wake Status (WAKESTS)—Offset Eh

This register indicates that a Status Change event has occurred on the link, which usually indicates that either the codec has just come out of reset and is requesting an address, or that a codec is signaling a wake event.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:3	0h RO	Reserved.
2:0	0h RW/1C/V	**SDIN State Change Status Flags (WAKESTS):** Flag bits that indicate which SDI signal(s) received a State Change event. The bits are cleared by writing 1's to them. These bits are cleared on a power-on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

5.2.9 Global Status (GSTS)—Offset 10h

This register provides global level status of the controller.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:2	0h RO	Reserved.
1	0h RW/1C/V	**Flush Status (FSTS):** This bit is set to a 1 by the hardware to indicate that the flush cycle initiated when the FCNTRL bit was set has completed. Software must write a 1to clear this bit before the next time FCNTRL is set.
0	0h RO	Reserved.

5.2.10 Global Capabilities 2 (GCAP2)—Offset 12h

This register indicates the additional capabilities of the controller.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
15:1	0h RO	Reserved.
0	1h RW/V/L	**Energy Efficient Audio Capability (EEAC):** Indicates whether the energy efficient audio with deeper buffering is supported or not. 0 = Not supported. FIFOL register and FIFOLC bit behave as RO. 1 = Supported. FIFOL register and FIFOLC bit behave as RW. Locked when FNCFG.BCLD = 1.

5.2.11 Linked List Capabilities Header (LLCH)—Offset 14h

This register provides the pointer to the first capability structure, if exists.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: C00h

Bit Range	Default and Access	Field Name (ID): Description
15:0	C00h RW/L	**First Capability Pointer (PTR):** This field contains the offset to the first capability structure of the linked list capabilities, or 0000h if no linked list capabilities exist. Point to Multiple Links Capability. Locked when FNCFG.BCLD = 1.

5.2.12 Output Stream Payload Capability (OUTSTRMPAY)—Offset 18h

This register indicates the maximum number of Words per frame for any single output stream.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 30h

Bit Range	Default and Access	Field Name (ID): Description
15:0	30h RO	**Output Stream Payload Capability (OUTSTRMPAY):** Indicates maximum number of words per frame for any single output stream. This measurement is in 16 bit word quantities per 48 kHz frame. 48 Words (96B) is the maximum supported, therefore a value of 30h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Output Stream Descriptor register. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload

5.2.13 Input Stream Payload Capability (INSTRMPAY)—Offset 1Ah

This register indicates the maximum number of Words per frame for any single input stream.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 18h

Bit Range	Default and Access	Field Name (ID): Description
15:0	18h RO	**Input Stream Payload Capability (INSTRMPAY):** Indicates maximum number of words per frame for any single input stream. This measurement is in 16 bit word quantities per 48 kHz frame. 24 Words (48B) is the maximum supported, therefore a value of 18h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Input Stream Descriptor register. 00h: 0 words 01h: 1 word payload ... FFh: 255h word payload

5.2.14 Interrupt Control (INTCTL)—Offset 20h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**Global Interrupt Enable (GIE):** Global bit to enable device interrupt generation. When set to 1 the Intel HD Audio function is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space, such as the Interrupt Enable bit in the PCI Configuration Space.

Bit Range	Default and Access	Field Name (ID): Description
30	0h RW	**Controller Interrupt Enable (CIE):** Enables the general interrupt for controller functions. When set to 1 (and GIE is enabled), the controller generates an interrupt when the CIS bit gets set.
29:16	0h RO	Reserved.
15:0	0h RW	**Stream Interrupt Enable (SIE):** When set to 1 the individual Streams are enabled to generate an interrupt when the corresponding stream status bits get set. A stream interrupt will be caused as a result of a buffer with IOC=1 in the BDL entry being completed, or as a result of a FIFO error (underrun or overrun) occurring. Control over the generation of each of these sources is in the associated Stream Descriptor. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set.

5.2.15 Interrupt Status (INTSTS)—Offset 24h

GIS and CIS bits are not affected by controller reset.
The number of SIS bits in this register is depending on the total number of stream DMA implemented.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO/V	**Global Interrupt Status (GIS):** This bit is an OR of all of the interrupt status bits in this register and PPSTS register
30	0h RW/V	**Controller Interrupt Status (CIS):** Status of general controller interrupt. A 1 indicates that an interrupt condition occurred due to a Response Interrupt, a Response Buffer Overrun Interrupt, CORB Memory Error Interrupt, or a SDIN State Change event. The exact cause can be determined by interrogating other registers. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of the stated interrupt status bits for this register.
29:16	0h RO	Reserved.
15:0	0h RW/V	**Stream Interrupt Status (SIS):** A 1 indicates that an interrupt condition occurred on the corresponding Stream. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of an individual stream s interrupt status bits. The streams are numbered and the SIS bits assigned sequentially, based on their order in the register set.

5.2.16 Wall Clock Counter (WALCLK)—Offset 30h

The 32 bit monotonic counter provides a 'wall clock' that can be used by system software to synchronize independent audio controllers.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Wall Clock Counter (WALCLK):** 32 bit counter that is incremented on each link BCLK period and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds. This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset. With the introduction of multiple link segments for the Intel HD Audio controller, and the capability of running each link segment at different clock speed, the BCLK definition for this counter is fixed at 24 MHz equivalent rate always, independent of the physical link clock speed, and reports the link 0 wall clock value.

5.2.17 Stream Synchronization (SSYNC)—Offset 38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Stream Synchronization Bits (SSYNC):** The Stream Synchronization bits, when set to 1, block data from being sent on or received from the link. Each bit controls the associated Stream Descriptor, bit 0 corresponds to the first Stream Descriptor, etc. To synchronously start a set of DMA engines, the bits in the SSYNC register are first set to a 1. The RUN bits for the associated Stream Descriptors are then set to a 1 to start the DMA engines. When all streams are ready (FIFORDY=1), the associated SSYNC bits can all be set to 0 at the same time, and transmission or reception of bits to or from the link will begin together at the start of the next full link frame. To synchronously stop streams, first the bits are set in the SSYNC register, and then the individual RUN bits in the Stream Descriptors are cleared by software. The streams are numbered and the SSYNC bits assigned sequentially, based on their order in the register set.

5.2.18 CORB Lower Base Address (CORBLBASE)—Offset 40h

This register specifies the address (lower 32 bits) of the Command Output Ring Buffer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:7	0h RW	**CORB Lower Base Address (CORBLBASE):** Lower address of the Command Output Ring Buffer, allowing the CORB Base Address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	0h RO	Reserved.

5.2.19 CORB Upper Base Address (CORBUBASE)—Offset 44h

This register specifies the address (upper 32 bits) of the Command Output Ring Buffer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**CORB Upper Base Address (CORBUBASE):** Upper 32 bits of address of the Command Output Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.ADD64OK = 0.

5.2.20 CORB Write Pointer (CORBWP)—Offset 48h

This register specifies the write pointer of the Command Output Ring Buffer.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:0	0h RW	**CORB Write Pointer (CORBWP):** Software writes the last valid CORB entry offset into this field in Dword granularity. The DMA engine fetches commands from the CORB until the Read Pointer matches the Write Pointer. Supports 256 CORB entries (256 x 4B=1KB). This field may be written while the DMA engine is running.

5.2.21 CORB Read Pointer (CORBRP)—Offset 4Ah

This register reports the read pointer of the Command Output Ring Buffer.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RW/V	**CORB Read Pointer Reset (CORBRPRST):** Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual pre-fetched commands in the CORB hardware buffer within the Intel Audio controller. The hardware will physically update this bit to 1 when the CORB Pointer reset is complete. Software must read a 1 to verify that the reset completed correctly. Software must clear this bit back to 0 and read back the 0 to verify that the clear completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted.
14:8	0h RO	Reserved.
7:0	0h RO/V	**CORB Read Pointer (CORBRP):** Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB Read Pointer offset in Dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports 256 CORB entries (256 x 4B=1KB). This field may be read while the DMA engine is running.

5.2.22 CORB Control (CORBCTL)—Offset 4Ch

This register provides the control of the Command Output Ring Buffer.

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:2	0h RO	Reserved.
1	0h RW/V	**Enable CORB DMA Engine (CORBRUN):** 0 = DMA Stop 1 = DMA Run After SW writes a 0 to this bit, the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.
0	0h RW	**CORB Memory Error Interrupt Enable (CMEIE):** If this bit is set (and GIE and CIE are enabled), the controller will generate an interrupt if the MEI status bit is set.

5.2.23 CORB Status (CORBSTS)—Offset 4Dh

This register provides the status of the Command Output Ring Buffer.

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:1	0h RO	Reserved.
0	0h RW/1C/V	**CORB Memory Error Indication (CMEI):** If this status bit is set, the controller has detected an error in the pathway between the controller and memory. This may be an ECC bit error or any other type of detectable data error which renders the command data fetched invalid. Software can clear this bit by writing a 1 to it. However, this type of error leaves the audio subsystem in an unavailable state and typically requires CRST#.

5.2.24 CORB Size (CORBSIZE)—Offset 4Eh

This register declares the size of the Command Output Ring Buffer.

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 42h

Bit Range	Default and Access	Field Name (ID): Description
7:4	4h RO	**CORB Size Capability (CORBSZCAP):** 0100b indicates that the ICH9 only supports a CORB size of 256 CORB entries (1024B).
3:2	0h RO	Reserved.
1:0	2h RO	**CORB Size (CORBSIZE):** Hardwired to 10b which sets the CORB size to 256 entries (1024B).

5.2.25 RIRB Lower Base Address (RIRBLBASE)—Offset 50h

This register specifies the address (lower 32 bits) of the Response Input Ring Buffer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:7	0h RW	**RIRB Lower Base Address (RIRBLBASE):** Lower address of the Response Input Ring Buffer, allowing the RIRB Base Address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	0h RO	Reserved.

5.2.26 RIRB Upper Base Address (RIRBUBASE)—Offset 54h

This register specifies the address (upper 32 bits) of the Response Input Ring Buffer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**RIRB Upper Base Address (RIRBUBASE):** Upper 32 bits of address of the Command Output Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

5.2.27 RIRB Write Pointer (RIRBWP)—Offset 58h

This register reports the write pointer of the Response Input Ring Buffer.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15	0h WO	**RIRB Write Pointer Reset (RIRBWPRST):** Software writes a 1 to this bit to reset the RIRB Write Pointer to 0's. The RIRB DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit will always be read as 0.
14:8	0h RO	Reserved.
7:0	0h RO/V	**RIRB Write Pointer (RIRBWP):** Indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in 2 Dword RIRB entry units (since each RIRB entry is 2 Dwords long). Supports up to 256 RIRB entries (256 x 8B=2KB). This field may be read while the DMA engine is running.

5.2.28 Response Interrupt Count (RINTCNT)—Offset 5Ah

This register specifies the threshold of Response Input Ring Buffer that triggers an interrupt.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:0	0h RW	**N Response Interrupt Count (RINTCNT):** 0000_0001b = 1 Response sent to RIRB ... 1111_1111b = 255 Responses sent to RIRB 0000_0000b = 256 Responses sent to RIRB The DMA engine should be stopped when changing this field or else an interrupt may be lost. Note that each Response occupies 2 Dwords in the RIRB. This is compared to the total number of responses that have been returned, as opposed to the number of frames in which there were responses. If more than one codec responds in one frame, then the count is increased by the number of responses received in the frame.

5.2.29 RIRB Control (RIRBCTL)—Offset 5Ch

This register provides the control of the Response Input Ring Buffer.

Access Method

Type: MEM Register (Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RW	**Response Overrun Interrupt Control (RIRBOIC):** If this bit is set (and GIE and CIE are enabled), the hardware will generate an interrupt when the Response Overrun Interrupt Status bit is set.
1	0h RW/V	**RIRB DMA Enable (RIRBRUN):** 0 = DMA Stop 1 = DMA Run After SW writes a 0 to this bit, the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.
0	0h RW	**Response Interrupt Control (RINTCTL):** 0 = Disable Interrupt 1 = Generate an interrupt (if GIE and CIE are enabled) after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI_x inputs (whichever occurs first). The N counter is reset when the interrupt is generated.

5.2.30 RIRB Status (RIRBSTS)—Offset 5Dh

This register provides the status of the Response Input Ring Buffer.

Access Method

Type: MEM Register (Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RW/1C/V	**Response Overrun Interrupt Status (RIRBOIS):** Hardware sets this bit to a 1 when the RIRB DMA engine is not able to write the incoming responses to memory before additional incoming responses overrun the internal FIFO. When the overrun occurs, the hardware will drop the responses which overrun the buffer. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.
1	0h RO	Reserved.
0	0h RW/1C/V	**Response Interrupt (RINTFL):** Hardware sets this bit to a 1 when an interrupt has been generated after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI(x) inputs (whichever occurs first). Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.

5.2.31 RIRB Size (RIRBSIZE)—Offset 5Eh

This register declares the size of the Response Input Ring Buffer.

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 42h

Bit Range	Default and Access	Field Name (ID): Description
7:4	4h RO	**RIRB Size Capability (RIRBSZCAP):** 0100b indicates that the PCH only supports a RIRB size of 256 RIRB entries (2048B).
3:2	0h RO	Reserved.
1:0	2h RO	**RIRB Size (RIRBSIZE):** Hardwired to 10b which sets the RIRB size to 256 entries (2048B).

5.2.32 Immediate Command (IC)—Offset 60h

This register provides the control of the immediate command.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Immediate Command (IC):** The command to be sent to the codec via the Immediate Command mechanism is written to this register. The command stored in this register is sent out over the link during the next available frame after a 1 is written to the ICB bit.

5.2.33 Immediate Response (IR)—Offset 64h

This register reports the response received for the immediate command.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Immediate Response (IR):** This register contains the response received from a codec resulting from a command sent via the Immediate Command mechanism. If multiple codecs responded in the same frame, there is no guarantee as to which response will be latched. Therefore broadcast-type commands must not be issued via the Immediate Command mechanism.

5.2.34 Immediate Command Status (ICS)—Offset 68h

This register provides the status of the immediate command.

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:2	0h RO	Reserved.
1	0h RW/1C/V	**Immediate Result Valid (IRV):** This bit is set to a 1 by hardware when a new response is latched into the IR register. This is a status flag indicating that software may read the response from the Immediate Response register. Software must clear this bit (by writing a one to it) before issuing a new command so that the software may determine when a new response has arrived.
0	0h RW/V	**Immediate Command Busy (ICB):** When this bit as read as a 0 it indicates that a new command may be issued using the Immediate Command mechanism. When this bit transitions from a 0 to a 1 (via software writing a 1), the controller issues the command currently stored in the Immediate Command register to the codec over the link. When the corresponding response is latched into the Immediate Response register, the controller hardware sets the IRV flag and clears the ICB bit back to 0. SW may write this bit to a 0 if the bit fails to return to 0 after a reasonable timeout period. Note that an Immediate Command must not be issued while the CORB/RIRB mechanism is operating, otherwise the responses conflict. This must be enforced by software.

5.2.35 DMA Position Lower Base Address (DPLBASE)—Offset 70h

This register specifies the base address (lower 32 bits) of DMA Position Buffer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:7	0h RW	**DMA Position Lower Base Address (DPLBASE):** Lower 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control, and must be programmed with a valid value before the FLCNRTL bit is set.
6:1	0h RO	Reserved.
0	0h RW	**DMA Position Buffer Enable (DPBE):** When this bit is set to a '1', the controller will write the DMA positions of each of the DMA engines to the buffer in main memory periodically (typically once/frame). Software can use this value to know what data in memory is valid data. The controller must guarantee that the values in the DMA Position Buffer that the software can read represent positions in the stream for which valid data exists in the Stream's DMA buffer. This has particular relevance in systems which support isochronous transfer, the stream positions in the software-visible memory buffer must represent stream data which has reached the Global Observation point.

5.2.36 DMA Position Upper Base Address (DPUBASE)—Offset 74h

This register specifies the base address (upper 32 bits) of DMA Position Buffer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**DMA Position Upper Base Address (DPUBASE):** Upper 32 bits of address of the DMA Position Buffer Base Address. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. Locked when GCAP.ADD64OK = 0.

5.2.37 Input/Output Stream Descriptor x Control (ISD0CTL)—Offset 80h

NOTE: This register definition applies to all of the following input and output streams at the corresponding offsets:
Input stream 0: offset 80h
Input stream 1: offset A0h
Input stream 2: offset C0h
Input stream 3: offset E0h
Input stream 4: offset 100h
Input stream 5: offset 120h
Input stream 6: offset 140h
Input stream 7: offset 280h
Input stream 8: offset 2A0h
Input stream 9: offset 2C0h
Input stream 10: offset 2E0h
Input stream 11: offset 300h
Input stream 12: offset 320h
Input stream 13: offset 340h
Input stream 14: offset 360h

Output stream 0: offset 160h
Output stream 1: offset 180h
Output stream 2: offset 1A0h
Output stream 3: offset 1C0h
Output stream 4: offset 1E0h
Output stream 5: offset 200h
Output stream 6: offset 220h
output stream 7: offset 240h
Output stream 8: offset 260h
Output stream 9: offset 380h
Output stream 10: offset 3A0h
Output stream 11: offset 3C0h
Output stream 12: offset 3E0h
Output stream 13: offset 400h
Output stream 14: offset 420h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 40000h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19	0h RO	**Bidirectional Direction Control (DIR):** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	1h RO	**Traffic Priority (TP):** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RW/L	**Stripe Control (STRIPE):** Input Stream: This field is meaningless for input streams. Output Stream: For output streams it controls the number of SDO signals to stripe data across. Locked when GCAP.NSDO = 00b.
15:6	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
5	0h RW/V/L	**FIFO Limit Change (FIFOLC):** Writing a 1 to this bit indicates a new update to the FIFOL register has been made. After the HW has completed sequencing into the new effective FIFO size, it will clear this bit. This bit is RO if GCAP2.EEAC = 0. If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 0 (static), this bit will only have effect when the stream is idle (before the first time RUN bit is set). If GCAP2.EEAC = 1 and GCAP2.DFIFOLCC = 1 (dynamic), on top of supporting the static behavior describe above, this bit also has effect when the stream is active (after the first time RUN bit is set).
4	0h RW	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	0h RW	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	0h RW	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.38 Input/Output Stream Descriptor x Status (ISD0STS)—Offset 83h

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 83h
Input stream 1: offset A3h
Input stream 2: offset C3h
Input stream 3: offset E3h
Input stream 4: offset 103h
Input stream 5: offset 123h
Input stream 6: offset 143h
Input stream 7: offset 283h
Input stream 8: offset 2A3h
Input stream 9: offset 2C3h
Input stream 10: offset 2E3h
Input stream 11: offset 303h
Input stream 12: offset 323h
Input stream 13: offset 343h
Input stream 14: offset 363h

Output stream 0: offset 163h
Output stream 1: offset 183h
Output stream 2: offset 1A3h
Output stream 3: offset 1C3h
Output stream 4: offset 1E3h
Output stream 5: offset 203h

Output stream 6: offset 223h
output stream 7: offset 243h
Output stream 8: offset 263h
Output stream 9: offset 383h
Output stream 10: offset 3A3h
Output stream 11: offset 3C3h
Output stream 12: offset 3E3h
Output stream 13: offset 403h
Output stream 14: offset 423h

Access Method

Type: MEM Register (Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:6	0h RO	Reserved.
5	0h RO/V	**FIFO Ready (FIFORDY):** This bit defaults to 0 on reset because the FIFO is cleared on a reset. Input Stream: For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set. Output Stream: For output streams, the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link.
4	0h RW/1C/V	**Descriptor Error (DESE):** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
3	0h RW/1C/V	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. Input Stream: For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers do not increment and the incoming data is not written into the FIFO, thereby being lost. Output Stream: For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	0h RW/1C/V	**Buffer Completion Interrupt Status (BCIS):** This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
1:0	0h RO	Reserved.

5.2.39 Input/Output Stream Descriptor x Link Position in Buffer (ISD0LPIB)—Offset 84h

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 84h
Input stream 1: offset A4h
Input stream 2: offset C4h
Input stream 3: offset E4h

Input stream 4: offset 104h
Input stream 5: offset 124h
Input stream 6: offset 144h
Input stream 7: offset 284h
Input stream 8: offset 2A4h
Input stream 9: offset 2C4h
Input stream 10: offset 2E4h
Input stream 11: offset 304h
Input stream 12: offset 324h
Input stream 13: offset 344h
Input stream 14: offset 364h

Output stream 0: offset 164h
Output stream 1: offset 184h
Output stream 2: offset 1A4h
Output stream 3: offset 1C4h
Output stream 4: offset 1E4h
Output stream 5: offset 204h
Output stream 6: offset 224h
output stream 7: offset 244h
Output stream 8: offset 264h
Output stream 9: offset 384h
Output stream 10: offset 3A4h
Output stream 11: offset 3C4h
Output stream 12: offset 3E4h
Output stream 13: offset 404h
Output stream 14: offset 324h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register (inclusive) for the first round, and then repeat counting from 1 to the value in the Cyclic Buffer Length register again for subsequent rounds Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.40 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD0CBL)—Offset 88h

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 88h
Input stream 1: offset A8h
Input stream 2: offset C8h
Input stream 3: offset E8h
Input stream 4: offset 108h
Input stream 5: offset 128h

Input stream 6: offset 148h
Input stream 7: offset 288h
Input stream 8: offset 2A8h
Input stream 9: offset 2C8h
Input stream 10: offset 2E8h
Input stream 11: offset 308h
Input stream 12: offset 328h
Input stream 13: offset 348h
Input stream 14: offset 368h

Output stream 0: offset 168h
Output stream 1: offset 188h
Output stream 2: offset 1A8h
Output stream 3: offset 1C8h
Output stream 4: offset 1E8h
Output stream 5: offset 208h
Output stream 6: offset 228h
output stream 7: offset 248h
Output stream 8: offset 268h
Output stream 9: offset 388h
Output stream 10: offset 3A8h
Output stream 11: offset 3C8h
Output stream 12: offset 3E8h
Output stream 13: offset 408h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is '0'. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfers may be corrupted.

5.2.41 Input/Output Stream Descriptor x Last Valid Index (ISD0LVI)—Offset 8Ch

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 8Ch
Input stream 1: offset ACh
Input stream 2: offset CCh
Input stream 3: offset ECh
Input stream 4: offset 10Ch
Input stream 5: offset 12Ch
Input stream 6: offset 14Ch
Input stream 7: offset 28Ch

Input stream 8: offset 2ACh
Input stream 9: offset 2CCh
Input stream 10: offset 2ECh
Input stream 11: offset 30Ch
Input stream 12: offset 32Ch
Input stream 13: offset 34Ch
Input stream 14: offset 36Ch

Output stream 0: offset 16Ch
Output stream 1: offset 18Ch
Output stream 2: offset 1ACh
Output stream 3: offset 1CCh
Output stream 4: offset 1ECh
Output stream 5: offset 20Ch
Output stream 6: offset 22Ch
output stream 7: offset 24Ch
Output stream 8: offset 26Ch
Output stream 9: offset 38Ch
Output stream 10: offset 3ACh
Output stream 11: offset 3CCh
Output stream 12: offset 3ECh
Output stream 13: offset 40Ch
Output stream 14: offset 42Ch

Access Method

Type: MEM Register (Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:0	0h RW	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, i.e., there must be at least two valid entries in the b uffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is '0'

5.2.42 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD0FIFOW)—Offset 8Eh

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 8Eh
Input stream 1: offset AEh
Input stream 2: offset CEh
Input stream 3: offset EEh
Input stream 4: offset 10Eh
Input stream 5: offset 12Eh
Input stream 6: offset 14Eh
Input stream 7: offset 28Eh

Input stream 8: offset 2AEh
Input stream 9: offset 2CEh
Input stream 10: offset 2EEh
Input stream 11: offset 30Eh
Input stream 12: offset 32Eh
Input stream 13: offset 34Eh
Input stream 14: offset 36Eh

Output stream 0: offset 16Eh
Output stream 1: offset 18Eh
Output stream 2: offset 1AEh
Output stream 3: offset 1CEh
Output stream 4: offset 1EEh
Output stream 5: offset 20Eh
Output stream 6: offset 22Eh
output stream 7: offset 24Eh
Output stream 8: offset 26Eh
Output stream 9: offset 38Eh
Output stream 10: offset 3AEh
Output stream 11: offset 3CEh
Output stream 12: offset 3EEh
Output stream 13: offset 40Eh
Output stream 14: offset 42Eh

Access Method

Type: MEM Register (Size: 16 bits)

Device:
Function:

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
15:3	0h RO	Reserved.
2:0	4h RO/V	**FIFOW (FIFOW):** Indicates the minimum number of bytes accumulated (for input) or free (for output) in the FIFO before the controller will start an eviction (for input) or fetch (for output) of data. The PCH HD Audio controller hardwires the FIFO Watermark, either 32B or 64B based on the following. Bit(2:0) Description 000-011 Reserved 100 32 B Supported. The 32 B request is aligned to 32 B boundaries. 101 64 B Supported. The 64 B request is aligned to 64 B boundaries. 110-111 Reserved Input Stream: For input streams, the FIFOW value is determined by the EM3.ISRWS (SEM3.ISRWS) field. Output Stream: For output streams, the FIFOW value is determined by the EM4.OSRWS (SEM4.OSRWS) field.

5.2.43 Input/Output Stream Descriptor x FIFO Size (ISD0FIFOS)—Offset 90h

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 90h

Input stream 1: offset B0h
Input stream 2: offset D0h
Input stream 3: offset F0h
Input stream 4: offset 110h
Input stream 5: offset 130h
Input stream 6: offset 150h
Input stream 7: offset 290h
Input stream 8: offset 2B0h
Input stream 9: offset 2D0h
Input stream 10: offset 2F0h
Input stream 11: offset 310h
Input stream 12: offset 330h
Input stream 13: offset 350h
Input stream 14: offset 370h

Output stream 0: offset 170h
Output stream 1: offset 190h
Output stream 2: offset 1B0h
Output stream 3: offset 1D0h
Output stream 4: offset 1F0h
Output stream 5: offset 210h
Output stream 6: offset 230h
output stream 7: offset 250h
Output stream 8: offset 270h
Output stream 9: offset 390h
Output stream 10: offset 3B0h
Output stream 11: offset 3D0h
Output stream 12: offset 3F0h
Output stream 13: offset 410h
Output stream 14: offset 430h

Access Method

Type: MEM Register (Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW/V	**FIFO Size (FIFOS):** When GCAP2.EEAC = 0, indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on the stream format programmed in (I/O)SDxFMT register, the min frame of buffering setting in EM(3/4)(SEM(3/4)).(I/O)SBSMFA[1:0] field, and the minimum buffer size threshold setting in EM2.BSMT[1:0] field. As the default value is zero, SW must write to the (I/O)SDxFMT register to kick off the FIFO size calculation, and read back to find out the HW allocated FIFO size. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised. In this case, the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time, the maximum number of bytes that may have been received into the HW buffer but not yet transferred out, and also the maximum possible value that the PICB count will increase by one time, all these maximum value could be larger than FIFOS value, depending on the FIFOL register setting. When EM2.HWFIFOL = 1, this FIFOS value will reflect the larger FIFO size of up to 10 ms, if extra buffer space is available.

5.2.44 Input/Output Stream Descriptor x Format (ISD0FMT)—Offset 92h

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 92h
Input stream 1: offset B2h
Input stream 2: offset D2h
Input stream 3: offset F2h
Input stream 4: offset 112h
Input stream 5: offset 132h
Input stream 6: offset 152h
Input stream 7: offset 292h
Input stream 8: offset 2B2h
Input stream 9: offset 2D2h
Input stream 10: offset 2F2h
Input stream 11: offset 312h
Input stream 12: offset 332h
Input stream 13: offset 352h
Input stream 14: offset 372h

Output stream 0: offset 172h
Output stream 1: offset 192h
Output stream 2: offset 1B2h
Output stream 3: offset 1D2h
Output stream 4: offset 1F2h
Output stream 5: offset 212h
Output stream 6: offset 232h
output stream 7: offset 252h
Output stream 8: offset 272h
Output stream 9: offset 392h
Output stream 10: offset 3B2h
Output stream 11: offset 3D2h
Output stream 12: offset 3F2h
Output stream 13: offset 412h
Output stream 14: offset 432h

Access Method

Type: MEM Register (Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8bit containers on 16bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.45 Input/Output Stream Descriptor x FIFO Limit (ISD0FIFOL)—Offset 94h

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 94h
Input stream 1: offset B4h
Input stream 2: offset D4h
Input stream 3: offset F4h
Input stream 4: offset 114h
Input stream 5: offset 134h
Input stream 6: offset 154h
Input stream 7: offset 294h
Input stream 8: offset 2B4h
Input stream 9: offset 2D4h
Input stream 10: offset 2F4h
Input stream 11: offset 314h
Input stream 12: offset 334h
Input stream 13: offset 354h
Input stream 14: offset 374h

Output stream 0: offset 174h
Output stream 1: offset 194h
Output stream 2: offset 1B4h
Output stream 3: offset 1D4h

Output stream 4: offset 1F4h
Output stream 5: offset 214h
Output stream 6: offset 234h
output stream 7: offset 254h
Output stream 8: offset 274h
Output stream 9: offset 394h
Output stream 10: offset 3B4h
Output stream 11: offset 3D4h
Output stream 12: offset 3F4h
Output stream 13: offset 414h
Output stream 14: offset 434h

Access Method

Type: MEM Register (Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW/L	**Granularity (GNL):** Granularity associated with LMT field definition. The LMT value needs to be multiplied with 125 us or 1 ms to get the access limit in time domain. 0 = 125 us 1 = 1 ms This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).
13:0	0h RW/L	**FIFO Limit (FIFOL):** Indicate how far the media player / application intend to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data in the cyclic buffer beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to multiply with the granularity (125 us vs. 1 ms) as defined in GNL bit, to get the actual processing ahead time. 0 = Disabled (FIFOS is the limit) 0001h 3FFFh = 1 16383 units When value) 0 (enabled), setting FIFOLC bit will trigger HW to evaluate the access limit change and update effective FIFO size (depending on the capability supported). SW shall make sure the FIFOL field is not changed in the progress of access limit change sequence. This bit is locked if GCAP2.EEAC = 0 (thus appear to be RO).

5.2.46 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD0BDLPLBA)—Offset 98h

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 98h
Input stream 1: offset B8h
Input stream 2: offset D8h
Input stream 3: offset F8h
Input stream 4: offset 118h
Input stream 5: offset 138h
Input stream 6: offset 158h
Input stream 7: offset 298h
Input stream 8: offset 2B8h
Input stream 9: offset 2D8h
Input stream 10: offset 2F8h
Input stream 11: offset 318h

Input stream 12: offset 338h
Input stream 13: offset 358h
Input stream 14: offset 378h

Output stream 0: offset 178h
Output stream 1: offset 198h
Output stream 2: offset 1B8h
Output stream 3: offset 1D8h
Output stream 4: offset 1F8h
Output stream 5: offset 218h
Output stream 6: offset 238h
output stream 7: offset 258h
Output stream 8: offset 278h
Output stream 9: offset 398h
Output stream 10: offset 3B8h
Output stream 11: offset 3D8h
Output stream 12: offset 3F8h
Output stream 13: offset 418h
Output stream 14: offset 438h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:7	0h RW	**Buffer Descriptor List Lower Base Address (BDLPLBA):** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted.
6:0	0h RO	Reserved.

5.2.47 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD0BDLPUBA)—Offset 9Ch

NOTE: This register applies to the following input and output streams at the corresponding offsets:
Input stream 0: offset 9Ch
Input stream 1: offset BCh
Input stream 2: offset DCh
Input stream 3: offset FCh
Input stream 4: offset 11Ch
Input stream 5: offset 13Ch
Input stream 6: offset 15Ch
Input stream 7: offset 29Ch
Input stream 8: offset 2BCh
Input stream 9: offset 2DCh
Input stream 10: offset 2FCh
Input stream 11: offset 31Ch
Input stream 12: offset 33Ch
Input stream 13: offset 35Ch

Input stream 14: offset 37Ch

Output stream 0: offset 17Ch
Output stream 1: offset 19Ch
Output stream 2: offset 1BCh
Output stream 3: offset 1DCh
Output stream 4: offset 1FCh
Output stream 5: offset 21Ch
Output stream 6: offset 23Ch
output stream 7: offset 25Ch
Output stream 8: offset 27Ch
Output stream 9: offset 39Ch
Output stream 10: offset 3BCh
Output stream 11: offset 3DCh
Output stream 12: offset 4FCh
Output stream 13: offset 41Ch
Output stream 14: offset 43Ch

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/L	**Buffer Descriptor List Upper Base Address (BDLPUBA):** Upper 32bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted. Locked when GCAP.64OK = 0.

5.2.48 Input/Output Stream Descriptor x Control (ISD1CTLB0)—Offset A0h

SRST bit is not affected by stream reset.

5.2.49 Input/Output Stream Descriptor x Control (ISD1CTL)—Offset A0h

Same description as ISD0CTL register at offset 80h.

5.2.50 Input/Output Stream Descriptor x Control (ISD1CTLB2)—Offset A2h

SRST bit is not affected by stream reset.

5.2.51 Input/Output Stream Descriptor x Status (ISD1STS)—Offset A3h

Same description as ISD0STS register at offset 83h.

5.2.52 Input/Output Stream Descriptor x Link Position in Buffer (ISD1LPIB)—Offset A4h

Same description as ISD0LPIB register at offset 84h.

5.2.53 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD1CBL)—Offset A8h

Same description as ISD0CBL register at offset 88h.

5.2.54 Input/Output Stream Descriptor x Last Valid Index (ISD1LVI)—Offset ACh

Same description as ISD0LVI register at offset 8Ch.

5.2.55 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD1FIFOW)—Offset AEh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.56 Input/Output Stream Descriptor x FIFO Size (ISD1FIFOS)—Offset B0h

Same description as ISD0FIFOS register at offset 90h.

5.2.57 Input/Output Stream Descriptor x Format (ISD1FMT)—Offset B2h

Same description as ISD0FMT register at offset 92h.

5.2.58 Input/Output Stream Descriptor x FIFO Limit (ISD1FIFOL)—Offset B4h

Same description as ISD0FIFOL register at offset 94h.

5.2.59 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD1BDLPLBA)—Offset B8h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.60 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD1BDLPUBA)—Offset BCh

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.61 Input/Output Stream Descriptor x Control (ISD2CTL)—Offset C0h

Same description as ISD0CTL register at offset 80h.

5.2.62 Input/Output Stream Descriptor x Status (ISD2STS)—Offset C3h

Same description as ISD0STS register at offset 83h.

5.2.63 Input/Output Stream Descriptor x Link Position in Buffer (ISD2LPIB)—Offset C4h

Same description as ISD0LPIB register at offset 84h.

5.2.64 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD2CBL)—Offset C8h

Same description as ISD0CBL register at offset 88h.

5.2.65 Input/Output Stream Descriptor x Last Valid Index (ISD2LVI)—Offset CCh

Same description as ISD0LVI register at offset 8Ch.

5.2.66 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD2FIFOW)—Offset CEh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.67 Input/Output Stream Descriptor x FIFO Size (ISD2FIFOS)—Offset D0h

Same description as ISD0FIFOS register at offset 90h.

5.2.68 Input/Output Stream Descriptor x Format (ISD2FMT)—Offset D2h

Same description as ISD0FMT register at offset 92h.

5.2.69 Input/Output Stream Descriptor x FIFO Limit (ISD2FIFOL)—Offset D4h

Same description as ISD0FIFOL register at offset 94h.

5.2.70 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD2BDLPLBA)—Offset D8h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.71 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD2BDLPUBA)—Offset DCh

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.72 Input/Output Stream Descriptor x Control (ISD3CTL)—Offset E0h

Same description as ISD0CTL register at offset 80h.

5.2.73 Input/Output Stream Descriptor x Control (ISD3CTLB0)—Offset E0h

SRST bit is not affected by stream reset.

5.2.74 Input/Output Stream Descriptor x Status (ISD3STS)—Offset E3h

Same description as ISD0STS register at offset 83h.

5.2.75 Input/Output Stream Descriptor x Link Position in Buffer (ISD3LPIB)—Offset E4h

Same description as ISD0LPIB register at offset 84h.

5.2.76 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD3CBL)—Offset E8h

Same description as ISD0CBL register at offset 88h.

5.2.77 Input/Output Stream Descriptor x Last Valid Index (ISD3LVI)—Offset ECh

Same description as ISD0LVI register at offset 8Ch.

5.2.78 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD3FIFOW)—Offset EEh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.79 Input/Output Stream Descriptor x FIFO Size (ISD3FIFOS)—Offset F0h

Same description as ISD0FIFOS register at offset 90h.

5.2.80 Input/Output Stream Descriptor x Format (ISD3FMT)—Offset F2h

Same description as ISD0FMT register at offset 92h.

5.2.81 Input/Output Stream Descriptor x FIFO Limit (ISD3FIFOL)—Offset F4h

Same description as ISD0FIFOL register at offset 94h.

5.2.82 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD3BDLPLBA)—Offset F8h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.83 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD3BDLPUBA)—Offset FCh

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.84 Input/Output Stream Descriptor x Control (ISD4CTL)—Offset 100h

Same description as ISD0CTL register at offset 80h.

5.2.85 Input/Output Stream Descriptor x Status (ISD4STS)—Offset 103h

Same description as ISD0STS register at offset 83h.

5.2.86 Input/Output Stream Descriptor x Link Position in Buffer (ISD4LPIB)—Offset 104h

Same description as ISD0LPIB register at offset 84h.

5.2.87 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD4CBL)—Offset 108h

Same description as ISD0CBL register at offset 88h.

5.2.88 Input/Output Stream Descriptor x Last Valid Index (ISD4LVI)—Offset 10Ch

Same description as ISD0LVI register at offset 8Ch.

5.2.89 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD4FIFOW)—Offset 10Eh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.90 Input/Output Stream Descriptor x FIFO Size (ISD4FIFOS)—Offset 110h

Same description as ISD0FIFOS register at offset 90h.

5.2.91 Input/Output Stream Descriptor x Format (ISD4FMT)—Offset 112h

Same description as ISD0FMT register at offset 92h.

5.2.92 Input/Output Stream Descriptor x FIFO Limit (ISD4FIFOL)—Offset 114h

Same description as ISD0FIFOL register at offset 94h.

5.2.93 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD4BDLPLBA)—Offset 118h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.94 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD4BDLPUBA)—Offset 11Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.95 Input/Output Stream Descriptor x Control (ISD5CTL)—Offset 120h

Same description as ISD0CTL register at offset 80h.

5.2.96 Input/Output Stream Descriptor x Status (ISD5STS)—Offset 123h

Same description as ISD0STS register at offset 83h.

5.2.97 Input/Output Stream Descriptor x Link Position in Buffer (ISD5LPIB)—Offset 124h

Same description as ISD0LPIB register at offset 84h.

5.2.98 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD5CBL)—Offset 128h

Same description as ISD0CBL register at offset 88h.

5.2.99 Input/Output Stream Descriptor x Last Valid Index (ISD5LVI)—Offset 12Ch

Same description as ISD0LVI register at offset 8Ch.

5.2.100 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD5FIFOW)—Offset 12Eh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.101 Input/Output Stream Descriptor x FIFO Size (ISD5FIFOS)—Offset 130h

Same description as ISD0FIFOS register at offset 90h.

5.2.102 Input/Output Stream Descriptor x Format (ISD5FMT)—Offset 132h

Same description as ISD0FMT register at offset 92h.

5.2.103 Input/Output Stream Descriptor x FIFO Limit (ISD5FIFOL)—Offset 134h

Same description as ISD0FIFOL register at offset 94h.

5.2.104 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD5BDLPLBA)—Offset 138h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.105 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD5BDLPUBA)—Offset 13Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.106 Input/Output Stream Descriptor x Control (ISD6CTL)—Offset 140h

Same description as ISD0CTL register at offset 80h.

5.2.107 Input/Output Stream Descriptor x Status (ISD6STS)—Offset 143h

Same description as ISD0STS register at offset 83h.

5.2.108 Input/Output Stream Descriptor x Link Position in Buffer (ISD6LPIB)—Offset 144h

Same description as ISD0LPIB register at offset 84h.

5.2.109 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD6CBL)—Offset 148h

Same description as ISD0CBL register at offset 88h.

5.2.110 Input/Output Stream Descriptor x Last Valid Index (ISD6LVI)—Offset 14Ch

Same description as ISD0LVI register at offset 8Ch.

5.2.111 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD6FIFOW)—Offset 14Eh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.112 Input/Output Stream Descriptor x FIFO Size (ISD6FIFOS)—Offset 150h

Same description as ISD0FIFOS register at offset 90h.

5.2.113 Input/Output Stream Descriptor x Format (ISD6FMT)—Offset 152h

Same description as ISD0FMT register at offset 92h.

5.2.114 Input/Output Stream Descriptor x FIFO Limit (ISD6FIFOL)—Offset 154h

Same description as ISD0FIFOL register at offset 94h.

5.2.115 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD6BDLPLBA)—Offset 158h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.116 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD6BDLPUBA)—Offset 15Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.117 Input/Output Stream Descriptor x Control (OSD1CTL)—Offset 180h

Same description as ISD0CTL register at offset 80h.

5.2.118 Input/Output Stream Descriptor x Status (OSD1STS)—Offset 183h

Same description as ISD0STS register at offset 83h.

5.2.119 Input/Output Stream Descriptor x Link Position in Buffer (OSD1LPIB)—Offset 184h

Same description as ISD0LPIB register at offset 84h.

5.2.120 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD1CBL)—Offset 188h

Same description as ISD0CBL register at offset 88h.

5.2.121 Input/Output Stream Descriptor x Last Valid Index (OSD1LVI)—Offset 18Ch

Same description as ISD0LVI register at offset 8Ch.

5.2.122 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD1FIFOW)—Offset 18Eh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.123 Input/Output Stream Descriptor x FIFO Size (OSD1FIFOS)—Offset 190h

Same description as ISD0FIFOS register at offset 90h.

5.2.124 Input/Output Stream Descriptor x Format (OSD1FMT)—Offset 192h

Same description as ISD0FMT register at offset 92h.

5.2.125 Input/Output Stream Descriptor x FIFO Limit (OSD1FIFOL)—Offset 194h

Same description as ISD0FIFOL register at offset 94h.

5.2.126 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD1BDLPLBA)—Offset 198h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.127 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD1BDLPUBA)—Offset 19Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.128 Input/Output Stream Descriptor x Control (OSD2CTL)—Offset 1A0h

Same description as ISD0CTL register at offset 80h.

5.2.129 Input/Output Stream Descriptor x Status (OSD2STS)—Offset 1A3h

Same description as ISD0STS register at offset 83h.

5.2.130 Input/Output Stream Descriptor x Link Position in Buffer (OSD2LPIB)—Offset 1A4h

Same description as ISD0LPIB register at offset 84h.

5.2.131 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD2CBL)—Offset 1A8h

Same description as ISD0CBL register at offset 88h.

5.2.132 Input/Output Stream Descriptor x Last Valid Index (OSD2LVI)—Offset 1ACh

Same description as ISD0LVI register at offset 8Ch.

5.2.133 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD2FIFOW)—Offset 1AEh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.134 Input/Output Stream Descriptor x FIFO Size (OSD2FIFOS)—Offset 1B0h

Same description as ISD0FIFOS register at offset 90h.

5.2.135 Input/Output Stream Descriptor x Format (OSD2FMT)—Offset 1B2h

Same description as ISD0FMT register at offset 92h.

5.2.136 Input/Output Stream Descriptor x FIFO Limit (OSD2FIFOL)—Offset 1B4h

Same description as ISD0FIFOL register at offset 94h.

5.2.137 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD2BDLPLBA)—Offset 1B8h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.138 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD2BDLPUBA)—Offset 1BCh

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.139 Input/Output Stream Descriptor x Control (OSD3CTLB0)—Offset 1C0h

SRST bit is not affected by stream reset.

5.2.140 Input/Output Stream Descriptor x Control (OSD3CTL)—Offset 1C0h

Same description as ISD0CTL register at offset 80h.

5.2.141 Input/Output Stream Descriptor x Control (OSD3CTLB2)—Offset 1C2h

SRST bit is not affected by stream reset.

5.2.142 Input/Output Stream Descriptor x Status (OSD3STS)—Offset 1C3h

Same description as ISD0STS register at offset 83h.

5.2.143 Input/Output Stream Descriptor x Link Position in Buffer (OSD3LPIB)—Offset 1C4h

Same description as ISD0LPIB register at offset 84h.

5.2.144 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD3CBL)—Offset 1C8h

Same description as ISD0CBL register at offset 88h.

5.2.145 Input/Output Stream Descriptor x Last Valid Index (OSD3LVI)—Offset 1CCh

Same description as ISD0LVI register at offset 8Ch.

5.2.146 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD3FIFOW)—Offset 1CEh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.147 Input/Output Stream Descriptor x FIFO Size (OSD3FIFOS)—Offset 1D0h

Same description as ISD0FIFOS register at offset 90h.

5.2.148 Input/Output Stream Descriptor x Format (OSD3FMT)—Offset 1D2h

Same description as ISD0FMT register at offset 92h.

5.2.149 Input/Output Stream Descriptor x FIFO Limit (OSD3FIFOL)—Offset 1D4h

Same description as ISD0FIFOL register at offset 94h.

5.2.150 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD3BDLPLBA)—Offset 1D8h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.151 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD3BDLPUBA)—Offset 1DCh

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.152 Input/Output Stream Descriptor x Control (OSD4CTL)—Offset 1E0h

Same description as ISD0CTL register at offset 80h.

5.2.153 Input/Output Stream Descriptor x Status (OSD4STS)—Offset 1E3h

Same description as ISD0STS register at offset 83h.

5.2.154 Input/Output Stream Descriptor x Link Position in Buffer (OSD4LPIB)—Offset 1E4h

Same description as ISD0LPIB register at offset 84h.

5.2.155 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD4CBL)—Offset 1E8h

Same description as ISD0CBL register at offset 88h.

5.2.156 Input/Output Stream Descriptor x Last Valid Index (OSD4LVI)—Offset 1ECh

Same description as ISD0LVI register at offset 8Ch.

5.2.157 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD4FIFOW)—Offset 1EEh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.158 Input/Output Stream Descriptor x FIFO Size (OSD4FIFOS)—Offset 1F0h

Same description as ISD0FIFOS register at offset 90h.

5.2.159 Input/Output Stream Descriptor x Format (OSD4FMT)—Offset 1F2h

Same description as ISD0FMT register at offset 92h.

5.2.160 Input/Output Stream Descriptor x FIFO Limit (OSD4FIFOL)—Offset 1F4h

Same description as ISD0FIFOL register at offset 94h.

5.2.161 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD4BDLPLBA)—Offset 1F8h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.162 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD4BDLPUBA)—Offset 1FCh

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.163 Input/Output Stream Descriptor x Control (OSD5CTL)—Offset 200h

Same description as ISD0CTL register at offset 80h.

5.2.164 Input/Output Stream Descriptor x Status (OSD5STS)—Offset 203h

Same description as ISD0STS register at offset 83h.

5.2.165 Input/Output Stream Descriptor x Link Position in Buffer (OSD5LPIB)—Offset 204h

Same description as ISD0LPIB register at offset 84h.

5.2.166 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD5CBL)—Offset 208h

Same description as ISD0CBL register at offset 88h.

5.2.167 Input/Output Stream Descriptor x Last Valid Index (OSD5LVI)—Offset 20Ch

Same description as ISD0LVI register at offset 8Ch.

5.2.168 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD5FIFOW)—Offset 20Eh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.169 Input/Output Stream Descriptor x FIFO Size (OSD5FIFOS)—Offset 210h

Same description as ISD0FIFOS register at offset 90h.

5.2.170 Input/Output Stream Descriptor x Format (OSD5FMT)—Offset 212h

Same description as ISD0FMT register at offset 92h.

5.2.171 Input/Output Stream Descriptor x FIFO Limit (OSD5FIFOL)—Offset 214h

Same description as ISD0FIFOL register at offset 94h.

5.2.172 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD5BDLPLBA)—Offset 218h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.173 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD5BDLPUBA)—Offset 21Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.174 Input/Output Stream Descriptor x Control (OSD6CTL)—Offset 220h

Same description as ISD0CTL register at offset 80h.

5.2.175 Input/Output Stream Descriptor x Status (OSD6STS)—Offset 223h

Same description as ISD0STS register at offset 83h.

5.2.176 Input/Output Stream Descriptor x Link Position in Buffer (OSD6LPIB)—Offset 224h

Same description as ISD0LPIB register at offset 84h.

5.2.177 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD6CBL)—Offset 228h

Same description as ISD0CBL register at offset 88h.

5.2.178 Input/Output Stream Descriptor x Last Valid Index (OSD6LVI)—Offset 22Ch

Same description as ISD0LVI register at offset 8Ch.

5.2.179 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD6FIFOW)—Offset 22Eh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.180 Input/Output Stream Descriptor x FIFO Size (OSD6FIFOS)—Offset 230h

Same description as ISD0FIFOS register at offset 90h.

5.2.181 Input/Output Stream Descriptor x Format (OSD6FMT)—Offset 232h

Same description as ISD0FMT register at offset 92h.

5.2.182 Input/Output Stream Descriptor x FIFO Limit (OSD6FIFOL)—Offset 234h

Same description as ISD0FIFOL register at offset 94h.

5.2.183 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD6BDLPLBA)—Offset 238h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.184 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD6BDLPUBA)—Offset 23Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.185 Input/Output Stream Descriptor x Control (OSD7CTLB0)—Offset 240h

SRST bit is not affected by stream reset.

5.2.186 Input/Output Stream Descriptor x Control (OSD7CTL)—Offset 240h

Same description as ISD0CTL register at offset 80h.

5.2.187 Input/Output Stream Descriptor x Control (OSD7CTLB2)—Offset 242h

SRST bit is not affected by stream reset.

5.2.188 Input/Output Stream Descriptor x Status (OSD7STS)—Offset 243h

Same description as ISD0STS register at offset 83h.

5.2.189 Input/Output Stream Descriptor x Link Position in Buffer (OSD7LPIB)—Offset 244h

Same description as ISD0LPIB register at offset 84h.

5.2.190 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD7CBL)—Offset 248h

Same description as ISD0CBL register at offset 88h.

5.2.191 Input/Output Stream Descriptor x Last Valid Index (OSD7LVI)—Offset 24Ch

Same description as ISD0LVI register at offset 8Ch.

5.2.192 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD7FIFOW)—Offset 24Eh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.193 Input/Output Stream Descriptor x FIFO Size (OSD7FIFOS)—Offset 250h

Same description as ISD0FIFOS register at offset 90h.

5.2.194 Input/Output Stream Descriptor x Format (OSD7FMT)—Offset 252h

Same description as ISD0FMT register at offset 92h.

5.2.195 Input/Output Stream Descriptor x FIFO Limit (OSD7FIFOL)—Offset 254h

Same description as ISD0FIFOL register at offset 94h.

5.2.196 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD7BDLPLBA)—Offset 258h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.197 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD7BDLPUBA)—Offset 25Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.198 Input/Output Stream Descriptor x Control (OSD8CTL)—Offset 260h

Same description as ISD0CTL register at offset 80h.

5.2.199 Input/Output Stream Descriptor x Status (OSD8STS)—Offset 263h

Same description as ISD0STS register at offset 83h.

5.2.200 Input/Output Stream Descriptor x Link Position in Buffer (OSD8LPIB)—Offset 264h

Same description as ISD0LPIB register at offset 84h.

5.2.201 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD8CBL)—Offset 268h

Same description as ISD0CBL register at offset 88h.

5.2.202 Input/Output Stream Descriptor x Last Valid Index (OSD8LVI)—Offset 26Ch

Same description as ISD0LVI register at offset 8Ch.

5.2.203 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD8FIFOW)—Offset 26Eh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.204 Input/Output Stream Descriptor x FIFO Size (OSD8FIFOS)—Offset 270h

Same description as ISD0FIFOS register at offset 90h.

5.2.205 Input/Output Stream Descriptor x Format (OSD8FMT)—Offset 272h

Same description as ISD0FMT register at offset 92h.

5.2.206 Input/Output Stream Descriptor x FIFO Limit (OSD8FIFOL)—Offset 274h

Same description as ISD0FIFOL register at offset 94h.

5.2.207 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD8BDLPLBA)—Offset 278h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.208 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD8BDLPUBA)—Offset 27Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.209 Input/Output Stream Descriptor x Control (ISD7CTL)—Offset 280h

Same description as ISD0CTL register at offset 80h.

5.2.210 Input/Output Stream Descriptor x Status (ISD7STS)—Offset 283h

Same description as ISD0STS register at offset 83h.

5.2.211 Input/Output Stream Descriptor x Link Position in Buffer (ISD7LPIB)—Offset 284h

Same description as ISD0LPIB register at offset 84h.

5.2.212 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD7CBL)—Offset 288h

Same description as ISD0CBL register at offset 88h.

5.2.213 Input/Output Stream Descriptor x Last Valid Index (ISD7LVI)—Offset 28Ch

Same description as ISD0LVI register at offset 8Ch.

5.2.214 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD7FIFOW)—Offset 28Eh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.215 Input/Output Stream Descriptor x FIFO Size (ISD7FIFOS)—Offset 290h

Same description as ISD0FIFOS register at offset 90h.

5.2.216 Input/Output Stream Descriptor x Format (ISD7FMT)—Offset 292h

Same description as ISD0FMT register at offset 92h.

5.2.217 Input/Output Stream Descriptor x FIFO Limit (ISD7FIFOL)—Offset 294h

Same description as ISD0FIFOL register at offset 94h.

5.2.218 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD7BDLPLBA)—Offset 298h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.219 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD7BDLPUBA)—Offset 29Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.220 Input/Output Stream Descriptor x Control (ISD8CTL)—Offset 2A0h

Same description as ISD0CTL register at offset 80h.

5.2.221 Input/Output Stream Descriptor x Status (ISD8STS)—Offset 2A3h

Same description as ISD0STS register at offset 83h.

5.2.222 Input/Output Stream Descriptor x Link Position in Buffer (ISD8LPIB)—Offset 2A4h

Same description as ISD0LPIB register at offset 84h.

5.2.223 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD8CBL)—Offset 2A8h

Same description as ISD0CBL register at offset 88h.

5.2.224 Input/Output Stream Descriptor x Last Valid Index (ISD8LVI)—Offset 2ACh

Same description as ISD0LVI register at offset 8Ch.

5.2.225 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD8FIFOW)—Offset 2AEh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.226 Input/Output Stream Descriptor x FIFO Size (ISD8FIFOS)—Offset 2B0h

Same description as ISD0FIFOS register at offset 90h.

5.2.227 Input/Output Stream Descriptor x Format (ISD8FMT)—Offset 2B2h

Same description as ISD0FMT register at offset 92h.

5.2.228 Input/Output Stream Descriptor x FIFO Limit (ISD8FIFOL)—Offset 2B4h

Same description as ISD0FIFOL register at offset 94h.

5.2.229 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD8BDLPLBA)—Offset 2B8h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.230 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD8BDLPUBA)—Offset 2BCh

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.231 Input/Output Stream Descriptor x Control (ISD9CTL)—Offset 2C0h

Same description as ISD0CTL register at offset 80h.

5.2.232 Input/Output Stream Descriptor x Status (ISD9STS)—Offset 2C3h

Same description as ISD0STS register at offset 83h.

5.2.233 Input/Output Stream Descriptor x Link Position in Buffer (ISD9LPIB)—Offset 2C4h

Same description as ISD0LPIB register at offset 84h.

5.2.234 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD9CBL)—Offset 2C8h

Same description as ISD0CBL register at offset 88h.

5.2.235 Input/Output Stream Descriptor x Last Valid Index (ISD9LVI)—Offset 2CCh

Same description as ISD0LVI register at offset 8Ch.

5.2.236 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD9FIFOW)—Offset 2CEh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.237 Input/Output Stream Descriptor x FIFO Size (ISD9FIFOS)—Offset 2D0h

Same description as ISD0FIFOS register at offset 90h.

5.2.238 Input/Output Stream Descriptor x Format (ISD9FMT)—Offset 2D2h

Same description as ISD0FMT register at offset 92h.

5.2.239 Input/Output Stream Descriptor x FIFO Limit (ISD9FIFOL)—Offset 2D4h

Same description as ISD0FIFOL register at offset 94h.

5.2.240 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD9BDLPLBA)—Offset 2D8h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.241 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD9BDLPUBA)—Offset 2DCh

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.242 Input/Output Stream Descriptor x Control (ISD10CTL)—Offset 2E0h

Same description as ISD0CTL register at offset 80h.

5.2.243 Input/Output Stream Descriptor x Status (ISD10STS)—Offset 2E3h

Same description as ISD0STS register at offset 83h.

5.2.244 Input/Output Stream Descriptor x Link Position in Buffer (ISD10LPIB)—Offset 2E4h

Same description as ISD0LPIB register at offset 84h.

5.2.245 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD10CBL)—Offset 2E8h

Same description as ISD0CBL register at offset 88h.

5.2.246 Input/Output Stream Descriptor x Last Valid Index (ISD10LVI)—Offset 2ECh

Same description as ISD0LVI register at offset 8Ch.

5.2.247 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD10FIFOW)—Offset 2EEh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.248 Input/Output Stream Descriptor x FIFO Size (ISD10FIFOS)—Offset 2F0h

Same description as ISD0FIFOS register at offset 90h.

5.2.249 Input/Output Stream Descriptor x Format (ISD10FMT)—Offset 2F2h

Same description as ISD0FMT register at offset 92h.

5.2.250 Input/Output Stream Descriptor x FIFO Limit (ISD10FIFOL)—Offset 2F4h

Same description as ISD0FIFOL register at offset 94h.

5.2.251 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD10BDLPLBA)—Offset 2F8h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.252 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD10BDLPUBA)—Offset 2FCh

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.253 Input/Output Stream Descriptor x Control (ISD11CTL)—Offset 300h

Same description as ISD0CTL register at offset 80h.

5.2.254 Input/Output Stream Descriptor x Status (ISD11STS)—Offset 303h

Same description as ISD0STS register at offset 83h.

5.2.255 Input/Output Stream Descriptor x Link Position in Buffer (ISD11LPIB)—Offset 304h

Same description as ISD0LPIB register at offset 84h.

5.2.256 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD11CBL)—Offset 308h

Same description as ISD0CBL register at offset 88h.

5.2.257 Input/Output Stream Descriptor x Last Valid Index (ISD11LVI)—Offset 30Ch

Same description as ISD0LVI register at offset 8Ch.

5.2.258 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD11FIFOW)—Offset 30Eh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.259 Input/Output Stream Descriptor x FIFO Size (ISD11FIFOS)—Offset 310h

Same description as ISD0FIFOS register at offset 90h.

5.2.260 Input/Output Stream Descriptor x Format (ISD11FMT)—Offset 312h

Same description as ISD0FMT register at offset 92h.

5.2.261 Input/Output Stream Descriptor x FIFO Limit (ISD11FIFOL)—Offset 314h

Same description as ISD0FIFOL register at offset 94h.

5.2.262 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD11BDLPLBA)—Offset 318h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.263 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD11BDLPUBA)—Offset 31Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.264 Input/Output Stream Descriptor x Control (ISD12CTL)—Offset 320h

Same description as ISD0CTL register at offset 80h.

5.2.265 Input/Output Stream Descriptor x Status (ISD12STS)—Offset 323h

Same description as ISD0STS register at offset 83h.

5.2.266 Input/Output Stream Descriptor x Link Position in Buffer (ISD12LPIB)—Offset 324h

Same description as ISD0LPIB register at offset 84h.

5.2.267 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD12CBL)—Offset 328h

Same description as ISD0CBL register at offset 88h.

5.2.268 Input/Output Stream Descriptor x Last Valid Index (ISD12LVI)—Offset 32Ch

Same description as ISD0LVI register at offset 8Ch.

5.2.269 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD12FIFOW)—Offset 32Eh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.270 Input/Output Stream Descriptor x FIFO Size (ISD12FIFOS)—Offset 330h

Same description as ISD0FIFOS register at offset 90h.

5.2.271 Input/Output Stream Descriptor x Format (ISD12FMT)—Offset 332h

Same description as ISD0FMT register at offset 92h.

5.2.272 Input/Output Stream Descriptor x FIFO Limit (ISD12FIFOL)—Offset 334h

Same description as ISD0FIFOL register at offset 94h.

5.2.273 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD12BDLPLBA)—Offset 338h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.274 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD12BDLPUBA)—Offset 33Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.275 Input/Output Stream Descriptor x Control (ISD13CTL)—Offset 340h

Same description as ISD0CTL register at offset 80h.

5.2.276 Input/Output Stream Descriptor x Status (ISD13STS)—Offset 343h

Same description as ISD0STS register at offset 83h.

5.2.277 Input/Output Stream Descriptor x Link Position in Buffer (ISD13LPIB)—Offset 344h

Same description as ISD0LPIB register at offset 84h.

5.2.278 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD13CBL)—Offset 348h

Same description as ISD0CBL register at offset 88h.

5.2.279 Input/Output Stream Descriptor x Last Valid Index (ISD13LVI)—Offset 34Ch

Same description as ISD0LVI register at offset 8Ch.

5.2.280 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD13FIFOW)—Offset 34Eh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.281 Input/Output Stream Descriptor x FIFO Size (ISD13FIFOS)—Offset 350h

Same description as ISD0FIFOS register at offset 90h.

5.2.282 Input/Output Stream Descriptor x Format (ISD13FMT)—Offset 352h

Same description as ISD0FMT register at offset 92h.

5.2.283 Input/Output Stream Descriptor x FIFO Limit (ISD13FIFOL)—Offset 354h

Same description as ISD0FIFOL register at offset 94h.

5.2.284 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD13BDLPLBA)—Offset 358h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.285 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD13BDLPUBA)—Offset 35Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.286 Input/Output Stream Descriptor x Control (ISD14CTL)—Offset 360h

Same description as ISD0CTL register at offset 80h.

5.2.287 Input/Output Stream Descriptor x Status (ISD14STS)—Offset 363h

Same description as ISD0STS register at offset 83h.

5.2.288 Input/Output Stream Descriptor x Link Position in Buffer (ISD14LPIB)—Offset 364h

Same description as ISD0LPIB register at offset 84h.

5.2.289 Input/Output Stream Descriptor x Cyclic Buffer Length (ISD14CBL)—Offset 368h

Same description as ISD0CBL register at offset 88h.

5.2.290 Input/Output Stream Descriptor x Last Valid Index (ISD14LVI)—Offset 36Ch

Same description as ISD0LVI register at offset 8Ch.

5.2.291 Input/Output Stream Descriptor x FIFO Eviction Watermark (ISD14FIFOW)—Offset 36Eh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.292 Input/Output Stream Descriptor x FIFO Size (ISD14FIFOS)—Offset 370h

Same description as ISD0FIFOS register at offset 90h.

5.2.293 Input/Output Stream Descriptor x Format (ISD14FMT)—Offset 372h

Same description as ISD0FMT register at offset 92h.

5.2.294 Input/Output Stream Descriptor x FIFO Limit (ISD14FIFOL)—Offset 374h

Same description as ISD0FIFOL register at offset 94h.

5.2.295 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (ISD14BDLPLBA)—Offset 378h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.296 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (ISD14BDLPUBA)—Offset 37Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.297 Input/Output Stream Descriptor x Control (OSD9CTL)—Offset 380h

Same description as ISD0CTL register at offset 80h.

5.2.298 Input/Output Stream Descriptor x Status (OSD9STS)—Offset 383h

Same description as ISD0STS register at offset 83h.

5.2.299 Input/Output Stream Descriptor x Link Position in Buffer (OSD9LPIB)—Offset 384h

Same description as ISD0LPIB register at offset 84h.

5.2.300 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD9CBL)—Offset 388h

Same description as ISD0CBL register at offset 88h.

5.2.301 Input/Output Stream Descriptor x Last Valid Index (OSD9LVI)—Offset 38Ch

Same description as ISD0LVI register at offset 8Ch.

5.2.302 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD9FIFOW)—Offset 38Eh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.303 Input/Output Stream Descriptor x FIFO Size (OSD9FIFOS)—Offset 390h

Same description as ISD0FIFOS register at offset 90h.

5.2.304 Input/Output Stream Descriptor x Format (OSD9FMT)—Offset 392h

Same description as ISD0FMT register at offset 92h.

5.2.305 Input/Output Stream Descriptor x FIFO Limit (OSD9FIFOL)—Offset 394h

Same description as ISD0FIFOL register at offset 94h.

5.2.306 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD9BDLPLBA)—Offset 398h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.307 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD9BDLPUBA)—Offset 39Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.308 Input/Output Stream Descriptor x Control (OSD10CTL)—Offset 3A0h

Same description as ISD0CTL register at offset 80h.

5.2.309 Input/Output Stream Descriptor x Status (OSD10STS)—Offset 3A3h

Same description as ISD0STS register at offset 83h.

5.2.310 Input/Output Stream Descriptor x Link Position in Buffer (OSD10LPIB)—Offset 3A4h

Same description as ISD0LPIB register at offset 84h.

5.2.311 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD10CBL)—Offset 3A8h

Same description as ISD0CBL register at offset 88h.

5.2.312 Input/Output Stream Descriptor x Last Valid Index (OSD10LVI)—Offset 3ACh

Same description as ISD0LVI register at offset 8Ch.

5.2.313 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD10FIFOW)—Offset 3AEh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.314 Input/Output Stream Descriptor x FIFO Size (OSD10FIFOS)—Offset 3B0h

Same description as ISD0FIFOS register at offset 90h.

5.2.315 Input/Output Stream Descriptor x Format (OSD10FMT)—Offset 3B2h

Same description as ISD0FMT register at offset 92h.

5.2.316 Input/Output Stream Descriptor x FIFO Limit (OSD10FIFOL)—Offset 3B4h

Same description as ISD0FIFOL register at offset 94h.

5.2.317 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD10BDLPLBA)—Offset 3B8h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.318 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD10BDLPUBA)—Offset 3BCh

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.319 Input/Output Stream Descriptor x Control (OSD11CTL)—Offset 3C0h

Same description as ISD0CTL register at offset 80h.

5.2.320 Input/Output Stream Descriptor x Status (OSD11STS)—Offset 3C3h

Same description as ISD0STS register at offset 83h.

5.2.321 Input/Output Stream Descriptor x Link Position in Buffer (OSD11LPIB)—Offset 3C4h

Same description as ISD0LPIB register at offset 84h.

5.2.322 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD11CBL)—Offset 3C8h

Same description as ISD0CBL register at offset 88h.

5.2.323 Input/Output Stream Descriptor x Last Valid Index (OSD11LVI)—Offset 3CCh

Same description as ISD0LVI register at offset 8Ch.

5.2.324 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD11FIFOW)—Offset 3CEh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.325 Input/Output Stream Descriptor x FIFO Size (OSD11FIFOS)—Offset 3D0h

Same description as ISD0FIFOS register at offset 90h.

5.2.326 Input/Output Stream Descriptor x Format (OSD11FMT)—Offset 3D2h

Same description as ISD0FMT register at offset 92h.

5.2.327 Input/Output Stream Descriptor x FIFO Limit (OSD11FIFOL)—Offset 3D4h

Same description as ISD0FIFOL register at offset 94h.

5.2.328 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD11BDLPLBA)—Offset 3D8h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.329 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD11BDLPUBA)—Offset 3DCh

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.330 Input/Output Stream Descriptor x Control (OSD12CTL)—Offset 3E0h

Same description as ISD0CTL register at offset 80h.

5.2.331 Input/Output Stream Descriptor x Status (OSD12STS)—Offset 3E3h

Same description as ISD0STS register at offset 83h.

5.2.332 Input/Output Stream Descriptor x Link Position in Buffer (OSD12LPIB)—Offset 3E4h

Same description as ISD0LPIB register at offset 84h.

5.2.333 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD12CBL)—Offset 3E8h

Same description as ISD0CBL register at offset 88h.

5.2.334 Input/Output Stream Descriptor x Last Valid Index (OSD12LVI)—Offset 3ECh

Same description as ISD0LVI register at offset 8Ch.

5.2.335 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD12FIFOW)—Offset 3EEh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.336 Input/Output Stream Descriptor x FIFO Size (OSD12FIFOS)—Offset 3F0h

Same description as ISD0FIFOS register at offset 90h.

5.2.337 Input/Output Stream Descriptor x Format (OSD12FMT)—Offset 3F2h

Same description as ISD0FMT register at offset 92h.

5.2.338 Input/Output Stream Descriptor x FIFO Limit (OSD12FIFOL)—Offset 3F4h

Same description as ISD0FIFOL register at offset 94h.

5.2.339 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD12BDLPLBA)—Offset 3F8h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.340 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD12BDLPUBA)—Offset 3FCh

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.341 Input/Output Stream Descriptor x Control (OSD13CTL)—Offset 400h

Same description as ISD0CTL register at offset 80h.

5.2.342 Input/Output Stream Descriptor x Status (OSD13STS)—Offset 403h

Same description as ISD0STS register at offset 83h.

5.2.343 Input/Output Stream Descriptor x Link Position in Buffer (OSD13LPIB)—Offset 404h

Same description as ISD0LPIB register at offset 84h.

5.2.344 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD13CBL)—Offset 408h

Same description as ISD0CBL register at offset 88h.

5.2.345 Input/Output Stream Descriptor x Last Valid Index (OSD13LVI)—Offset 40Ch

Same description as ISD0LVI register at offset 8Ch.

5.2.346 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD13FIFOW)—Offset 40Eh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.347 Input/Output Stream Descriptor x FIFO Size (OSD13FIFOS)—Offset 410h

Same description as ISD0FIFOS register at offset 90h.

5.2.348 Input/Output Stream Descriptor x Format (OSD13FMT)—Offset 412h

Same description as ISD0FMT register at offset 92h.

5.2.349 Input/Output Stream Descriptor x FIFO Limit (OSD13FIFOL)—Offset 414h

Same description as ISD0FIFOL register at offset 94h.

5.2.350 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD13BDLPLBA)—Offset 418h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.351 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD13BDLPUBA)—Offset 41Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.352 Input/Output Stream Descriptor x Control (OSD14CTL)—Offset 420h

Same description as ISD0CTL register at offset 80h.

5.2.353 Input/Output Stream Descriptor x Status (OSD14STS)—Offset 423h

Same description as ISD0STS register at offset 83h.

5.2.354 Input/Output Stream Descriptor x Link Position in Buffer (OSD14LPIB)—Offset 424h

Same description as ISD0LPIB register at offset 84h.

5.2.355 Input/Output Stream Descriptor x Cyclic Buffer Length (OSD14CBL)—Offset 428h

Same description as ISD0CBL register at offset 88h.

5.2.356 Input/Output Stream Descriptor x Last Valid Index (OSD14LVI)—Offset 42Ch

Same description as ISD0LVI register at offset 8Ch.

5.2.357 Input/Output Stream Descriptor x FIFO Eviction Watermark (OSD14FIFOW)—Offset 42Eh

Same description as ISD0FIFOW register at offset 8Eh.

5.2.358 Input/Output Stream Descriptor x FIFO Size (OSD14FIFOS)—Offset 430h

Same description as ISD0FIFOS register at offset 90h.

5.2.359 Input/Output Stream Descriptor x Format (OSD14FMT)—Offset 432h

Same description as ISD0FMT register at offset 92h.

5.2.360 Input/Output Stream Descriptor x FIFO Limit (OSD14FIFOL)—Offset 434h

Same description as ISD0FIFOL register at offset 94h.

5.2.361 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Lower Base Address (OSD14BDLPLBA)—Offset 438h

Same description as ISD0BDLPLBA register at offset 98h.

5.2.362 Input/Output Stream Descriptor x Buffer Descriptor List Pointer Upper Base Address (OSD14BDLPUBA)—Offset 43Ch

Same description as ISD0BDLPUBA register at offset 9Ch.

5.2.363 Global Time Synchronization Capability Header (GTSCH)—Offset 500h

This register declares the global time synchronization capability structure.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 11F00h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1.
27:16	1h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1.
15:0	1F00h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. Point to DMA resume capability. Locked when FNCFG.BCLD = 1.

5.2.364 Global Time Synchronization Capability Declaration (GTSCD)—Offset 504h

This register identifies the general global time synchronization associated capabilities.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RO	**Controller Based Synchronization Adjust Supported (CTLSAS):** When set, it indicates that the controller based synchronization adjustment is supported. By adjusting the global link clock which is used as reference clock for the codecs DAC / ADC, the codec will indirectly changing the rate of all its active streams. Locked when FNCFG.BCLD = 1.
1:0	0h RO	Reserved.

5.2.365 Global Time Synchronization Capture Control (GTSCC0)—Offset 520h

This register controls the global time synchronization capture operation, and snapshots ART value as the global time stamp counter value.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/1C/V	**Time Stamp Counter Capture Done (TSCCD):** This bit is set when a valid TSC value has been captured: WALFCC, TSCCL, TSCCU, LLPFOC, LLPCL, and LLPCH contain valid data. The Intel HD Audio driver software must acknowledge the completion by writing 1 to clear this bit.
30	0h RW	**Time Stamp Counter Capture Done Interrupt Enable (TSCCDIE):** If set to 1, TSCCD bit can pass through to cause an interrupt status reported in INTSTS.CIS bit, and cause an interrupt to CPU if INTCTL.CIE = 1 and INTCTL.GIE = 1.
29:6	0h RO	Reserved.
5	0h RW/1S/V	**Time Stamp Counter Capture Initiate (TSCCI):** Write to 1 to initiate Global Time Synchronization capture for measuring TSC offset to local wall frame info. Cleared to 0 by hardware when the process is completed.
4:0	0h RW	**Capture DMA Select (CDMAS):** To select which DMA's LLPL, and LLPU value to be captured together with the TSC value. Bit 4 = 1 for ODMA, 0 for IDMA Bit 3:0 indicates the respective DMA engine index. Programmed before TSCCI = 1.

5.2.366 Wall Frame Counter Captured (WALFCC0)—Offset 524h

This register reports the wall frame counter captured.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:9	0h RO/V	**Frame Number (FN):** Indicates the 23 bit frame number captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.
8:0	0h RO/V	**Clock in Frame (CIF):** Indicates the 9 bit clock in frame value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

5.2.367 Time Stamp Counter Captured Lower (TSCCL0)—Offset 528h

This register reports the ART value snapshot as the global time stamp counter captured (lower 32 bits).

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Counter Captured Lower (CCL):** Indicates the lower 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

5.2.368 Time Stamp Counter Captured Upper (TSCCU0)—Offset 52Ch

This register reports the ART value snapshot as the global time stamp counter captured (upper 32 bits).

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Counter Captured Upper (CCU):** Indicates the upper 32 bit TSC value captured as a result of Global Time Synchronization capture request. Valid and static when GTSCC.TSCCD = 1.

5.2.369 Linear Link Position Frame Offset Captured (LLPFOC0)—Offset 534h

This register is to report additional accuracy details for captures made in between of two updates of LLP values, in number of 48 KHz HD Audio frames of the corresponding link. Audio streams with 44.1 KHz base rate and non zero divider FMT value will skip frames periodically on the Intel HD Audio link and Intel iDisplay Audio link in order to normalize its sampling rate to the 48 KHz HD Audio frame rate; hence; the frame offset will be useful in these cases.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RO/V	**Frame Offset Captured (FOC):** When the LLPCL and LLPCU registers are updated, this field records the elapsed number of 48 KHz HD Audio frames since the last LLP value change. Valid and static when GTSCC.TSCCD = 1

5.2.370 Linear Link Position Captured Lower (LLPCL0)—Offset 538h

This register reports the linear link position counter captured (lower 32 bits).

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Linear Link Position Captured Lower (LLPCL):** Indicates the lower 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request. Note that the LLPCL value that is captured is the LLPL value at the previous HD Audio frame boundary, not the live LLPL register value which may be changing in the middle of the current frame. Valid and static when GTSCC.TSCCD = 1.

5.2.371 Linear Link Position Captured Upper (LLPCU0)—Offset 53Ch

This register reports the time stamp counter captured (upper 32 bits).

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Linear Link Position Captured Upper (LLPCU):** Indicates the upper 32 bit linear link position value of the link DMA captured as a result of Global Time Synchronization capture request. Note that the LLPCU value that is captured is the LLPU value at the previous HD Audio frame boundary, not the live LLPU register value which may be changing in the middle of the current frame. Valid and static when GTSCC.TSCCD = 1.

5.2.372 Global Time Synchronization Capture Control (GTSCC1)—Offset 540h

Same definition as GTSCC0 at offset 520h.

5.2.373 Wall Frame Counter Captured (WALFCC1)—Offset 544h

Same definition as WALFCC0 at offset 524h.

5.2.374 Time Stamp Counter Captured Lower (TSCCL1)—Offset 548h

Same definition as TSCCL0 at offset 528h.

5.2.375 Time Stamp Counter Captured Upper (TSCCU1)—Offset 54Ch

Same definition as TSCCU0 at offset 52Ch.

5.2.376 Linear Link Position Frame Offset Captured (LLPFOC1)—Offset 554h

Same definition as LLPFOC0 at offset 534h.

5.2.377 Linear Link Position Captured Lower (LLPCL1)—Offset 558h

Same definition as LLPCL0 at offset 538h.

5.2.378 Linear Link Position Captured Upper (LLPCU1)—Offset 55Ch

Same definition as LLPCU0 at offset 53Ch.

5.2.379 Processing Pipe Capability Header (PPCH)—Offset 800h

This register declares the processing pipe capability structure.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 30500h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1.
27:16	3h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1.
15:0	500h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. Point to Global Time Synchronization capability. Locked when FNCFG.BCLD = 1.

5.2.380 Processing Pipe Control (PPCTL)—Offset 804h

This register is not affected by stream reset.
Note that the PROCEN bit should only be modified when the corresponding host DMA and link DMA are idle, i.e. RUN bits are cleared, and the DMA contexts have been destroyed through SRST bits if it was previously activated.
Note that GPROCEN bit does not really enable or disable the Audio DSP operation, but mainly to workaround some legacy Intel HD Audio driver software such that if GPROCEN = 0, ADSPxBA (BAR2) is mapped to the Intel HD Audio memory mapped configuration registers, for compliancy with some legacy SW implementation. If GPROCEN = 1, only then ADSPxBA (BAR2) is mapped to the actual Audio DSP memory mapped configuration registers.
The number of PROCEN bits in this register is depending on the total number of stream DMA implemented.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**Processing Interrupt Enable (PIE):** Enables the general interrupt for the Audio DSP function. When set to 1 (and GIE is enabled), the Audio DSP generates an interrupt when the PIS bit gets set.
30:16	0h RO	Reserved.
15:0	0h RW	**Processing Enable (PROCEN):** When set to 1 the DMA engine associated with this stream will be enabled to route the audio stream to DSP audio pipes in the Audio DSP for processing. When cleared to 0 the DMA engine associated with this stream will be bypassing the Audio DSP and route the audio stream directly to the audio link.

5.2.381 Processing Pipe Status (PPSTS)—Offset 808h

This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO/V	**Processing Interrupt Status (PIS):** Status of general interrupt for the Audio DSP function. A 1 indicates that an interrupt condition occurred in the Audio DSP function. The exact cause can be determined by interrogating the ADSPIS register. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of the interrupt status bits in ADSPIS register.
30:0	0h RO	Reserved.

5.2.382 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC0LLPL)—Offset 810h

Detail description is in their respective fields. There can be up to 15 input / output processing pipes with each pipe having their own register set. Offset for IPPHCxLLPL for each pipe is below.

Input stream 0: Offset 810h
Input stream 1: Offset 820h
Input stream 2: Offset 830h
Input stream 3: Offset 840h
Input stream 4: Offset 850h
Input stream 5: Offset 860h
Input stream 6: Offset 870h
Input stream 7: Offset 4A10h
Input stream 8: Offset 4A20h
Input stream 9: Offset 4A30h
Input stream 10: Offset 4A40h
Input stream 11: Offset 4A50h
Input stream 12: Offset 4A60h
Input stream 13: Offset 4A70h
Input stream 14: Offset 4A80h

Output stream 0: Offset 880h
Output stream 1: Offset 890h
Output stream 2: Offset 8A0h
Output stream 3: Offset 8B0h
Output stream 4: Offset 8C0h
Output stream 5: Offset 8D0h
output stream 6: Offset 8E0h
Output stream 7: Offset 8F0h
Output stream 8: Offset 900h
Output stream 9: Offset 4A90h
Output stream 10: Offset 4AA0h
Output stream 11: Offset 4AB0h
Output stream 12: Offset 4AC0h
Output stream 13: Offset 4AD0h
Output stream 14: Offset 4AE0h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.383 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC0LLPU)—Offset 814h

Detail description is in their respective fields. There can be up to 15 input / output processing pipes with each pipe having their own register set. Offset for IPPHCxLLPU for each pipe is below.

Input stream 0: Offset 814h
Input stream 1: Offset 824h
Input stream 2: Offset 834h
Input stream 3: Offset 844h
Input stream 4: Offset 854h
Input stream 5: Offset 864h
Input stream 6: Offset 874h
Input stream 7: Offset 4A10h
Input stream 8: Offset 4A24h
Input stream 9: Offset 4A34h
Input stream 10: Offset 4A44h
Input stream 11: Offset 4A54h
Input stream 12: Offset 4A64h
Input stream 13: Offset 4A74h
Input stream 14: Offset 4A84h

Output stream 0: Offset 884h
Output stream 1: Offset 894h
Output stream 2: Offset 8A4h
Output stream 3: Offset 8B4h
Output stream 4: Offset 8C4h
Output stream 5: Offset 8D4h
output stream 6: Offset 8E4h
Output stream 7: Offset 8F4h
Output stream 8: Offset 904h
Output stream 9: Offset 4A94h
Output stream 10: Offset 4AA4h
Output stream 11: Offset 4AB4h
Output stream 12: Offset 4AC4h
Output stream 13: Offset 4AD4h
Output stream 14: Offset 4AE4h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.384 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC0LDPL)—Offset 818h

Detail description is in their respective fields. There can be up to 15 input / output processing pipes with each pipe having their own register set. Offset for IPPHCxLDPL for each pipe is below.

Input stream 0: Offset 818h
Input stream 1: Offset 828h
Input stream 2: Offset 838h
Input stream 3: Offset 848h
Input stream 4: Offset 858h
Input stream 5: Offset 868h
Input stream 6: Offset 878h
Input stream 7: Offset 4A18h
Input stream 8: Offset 4A28h
Input stream 9: Offset 4A38h
Input stream 10: Offset 4A48h
Input stream 11: Offset 4A58h
Input stream 12: Offset 4A60h
Input stream 13: Offset 4A70h
Input stream 14: Offset 4A88h

Output stream 0: Offset 888h
Output stream 1: Offset 898h
Output stream 2: Offset 8A8h
Output stream 3: Offset 8B8h
Output stream 4: Offset 8C8h
Output stream 5: Offset 8D8h
output stream 6: Offset 8E8h
Output stream 7: Offset 8F8h
Output stream 8: Offset 908h
Output stream 9: Offset 4A98h
Output stream 10: Offset 4AA8h
Output stream 11: Offset 4AB8h
Output stream 12: Offset 4AC8h
Output stream 13: Offset 4AD8h
Output stream 14: Offset 4AE8h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.385 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC0LDPU)—Offset 81Ch

Detail description is in their respective fields. There can be up to 15 input / output processing pipes with each pipe having their own register set. Offset for IPPHCxLDPU for each pipe is below.

Input stream 0: Offset 81Ch
Input stream 1: Offset 82Ch
Input stream 2: Offset 83Ch
Input stream 3: Offset 84Ch
Input stream 4: Offset 85Ch
Input stream 5: Offset 86Ch
Input stream 6: Offset 87Ch
Input stream 7: Offset 4A1Ch
Input stream 8: Offset 4A2Ch
Input stream 9: Offset 4A3Ch
Input stream 10: Offset 4A4Ch
Input stream 11: Offset 4A5Ch
Input stream 12: Offset 4A6Ch
Input stream 13: Offset 4A7Ch
Input stream 14: Offset 4A8Ch

Output stream 0: Offset 88Ch
Output stream 1: Offset 89Ch
Output stream 2: Offset 8ACh
Output stream 3: Offset 8BCh
Output stream 4: Offset 8CCh
Output stream 5: Offset 8DCh
output stream 6: Offset 8ECh
Output stream 7: Offset 8FCh
Output stream 8: Offset 90Ch
Output stream 9: Offset 4A9Ch
Output stream 10: Offset 4AACh
Output stream 11: Offset 4ABCh
Output stream 12: Offset 4ACCh
Output stream 13: Offset 4ADCh
Output stream 14: Offset 4AECh

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.386 Input/Output Processing Pipe's Link Connection x Control (IPPLC0CTL)—Offset 910h

Detail description is in their respective fields. There can be up to 15 input / output processing pipes with each pipe having their own register set. Offset for IPPLCxCTL for each pipe is below.

Input stream 0: Offset 910h
Input stream 1: Offset 920h
Input stream 2: Offset 930h
Input stream 3: Offset 940h
Input stream 4: Offset 950h
Input stream 5: Offset 960h
Input stream 6: Offset 970h
Input stream 7: Offset 4AF0h
Input stream 8: Offset 4B00h
Input stream 9: Offset 4B10h
Input stream 10: Offset 4B20h
Input stream 11: Offset 4B30h
Input stream 12: Offset 4B40h
Input stream 13: Offset 4B50h
Input stream 14: Offset 4B60h

Output stream 0: Offset 980h
Output stream 1: Offset 990h
Output stream 2: Offset 9A0h
Output stream 3: Offset 9B0h
Output stream 4: Offset 9C0h
Output stream 5: Offset 9D0h
output stream 6: Offset 9E0h
Output stream 7: Offset 9F0h
Output stream 8: Offset A00h
Output stream 9: Offset 4B70h
Output stream 10: Offset 4B80h
Output stream 11: Offset 4B90h
Output stream 12: Offset 4BA0h
Output stream 13: Offset 4BB0h
Output stream 14: Offset 4BC0h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	0h RW	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. 0000=Reserved (Indicates Unused) 0001=Stream 1 ... 1110=Stream 14 1111=Stream 15 Input Stream: When an input stream is detected on any of the SDIx signals that match this value, the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number, two different SDIx inputs may not be configured with the same stream number. Output Stream: When data controlled by this descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal.
19:2	0h RO	Reserved.
1	0h RW/V	**Stream Run (RUN):** When set to 1 the DMA engine associated with this stream will be enabled to transfer data between FIFO and main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW/V	**Stream Reset (SRST):** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFO's for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

5.2.387 Input/Output Processing Pipe's Link Connection x Format (IPPLC0FMT)—Offset 914h

Detail description is in their respective fields. There can be up to 15 input / output processing pipes with each pipe having their own register set. Offset for IPPLCxFMT for each pipe is below.

Input stream 0: Offset 914h
Input stream 1: Offset 924h
Input stream 2: Offset 934h
Input stream 3: Offset 944h
Input stream 4: Offset 954h
Input stream 5: Offset 964h
Input stream 6: Offset 974h
Input stream 7: Offset 4AF4h
Input stream 8: Offset 4B04h
Input stream 9: Offset 4B14h
Input stream 10: Offset 4B24h
Input stream 11: Offset 4B34h
Input stream 12: Offset 4B44h
Input stream 13: Offset 4B54h
Input stream 14: Offset 4B64h

Output stream 0: Offset 984h
Output stream 1: Offset 994h
Output stream 2: Offset 9A4h
Output stream 3: Offset 9B4h
Output stream 4: Offset 9C4h
Output stream 5: Offset 9D4h
output stream 6: Offset 9E4h
Output stream 7: Offset 9F4h

Output stream 8: Offset A04h
Output stream 9: Offset 4B74h
Output stream 10: Offset 4B84h
Output stream 11: Offset 4B94h
Output stream 12: Offset 4BA4h
Output stream 13: Offset 4BB4h
Output stream 14: Offset 4BC4h

Access Method

Type: MEM Register (Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RO	Reserved.
14	0h RW	**Sample Base Rate (BASE):** 0=48 kHz 1=44.1 kHz
13:11	0h RW	**Sample Base Rate Multiple (MULT):** 000=48 kHz/44.1 kHz or less 001=x2 (96 kHz, 88.2 kHz, 32 kHz) 010=x3 (144 kHz) 011=x4 (192 kHz, 176.4 kHz) 100-111=Reserved
10:8	0h RW	**Sample Base Rate Divisor (DIV):** 000=Divide by 1 (48 kHz, 44.1 kHz) 001=Divide by 2 (24 kHz, 22.05 kHz) 010=Divide by 3 (16 kHz, 32 kHz) 011=Divide by 4 (11.025 kHz) 100=Divide by 5 (9.6 kHz) 101=Divide by 6 (8 kHz) 110=Divide by 7 111=Divide by 8 (6 kHz)
7	0h RO	Reserved.
6:4	0h RW	**Bits per Sample (BITS):** 000=8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001=16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010=20 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 011=24 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 100=32 bits. The data will be packed in memory in 32-bit containers on 32- bit boundaries 101-111=Reserved
3:0	0h RW	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000=1 0001=2 ... 1111=16

5.2.388 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC0LLPL)—Offset 918h

Detail description is in their respective fields. There can be up to 15 input / output processing pipes with each pipe having their own register set. Offset for IPPLCxLLPL for each pipe is below.

Input stream 0: Offset 918h
Input stream 1: Offset 928h
Input stream 2: Offset 938h
Input stream 3: Offset 948h
Input stream 4: Offset 958h
Input stream 5: Offset 968h
Input stream 6: Offset 978h
Input stream 7: Offset 4AF8h
Input stream 8: Offset 4B08h
Input stream 9: Offset 4B18h

Input stream 10: Offset 4B28h
Input stream 11: Offset 4B38h
Input stream 12: Offset 4B48h
Input stream 13: Offset 4B58h
Input stream 14: Offset 4B68h

Output stream 0: Offset 988h
Output stream 1: Offset 998h
Output stream 2: Offset 9A8h
Output stream 3: Offset 9B8h
Output stream 4: Offset 9C8h
Output stream 5: Offset 9D8h
output stream 6: Offset 9E8h
Output stream 7: Offset 9F8h
Output stream 8: Offset A08h
Output stream 9: Offset 4B78h
Output stream 10: Offset 4B88h
Output stream 11: Offset 4B98h
Output stream 12: Offset 4BA8h
Output stream 13: Offset 4BB8h
Output stream 14: Offset 4BC8h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.389 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC0LLPU)—Offset 91Ch

Detail description is in their respective fields. There can be up to 15 input / output processing pipes with each pipe having their own register set. Offset for IPPLCxLLPU for each pipe is below.

Input stream 0: Offset 91ch
Input stream 1: Offset 92ch
Input stream 2: Offset 93Ch
Input stream 3: Offset 94Ch
Input stream 4: Offset 95Ch
Input stream 5: Offset 96Ch
Input stream 6: Offset 97Ch
Input stream 7: Offset 4AFCh
Input stream 8: Offset 4B0Ch
Input stream 9: Offset 4B1Ch

Input stream 10: Offset 4B2Ch
Input stream 11: Offset 4B3Ch
Input stream 12: Offset 4B4Ch
Input stream 13: Offset 4B5Ch
Input stream 14: Offset 4B6Ch

Output stream 0: Offset 98Ch
Output stream 1: Offset 99Ch
Output stream 2: Offset 9ACh
Output stream 3: Offset 9BCh
Output stream 4: Offset 9CCh
Output stream 5: Offset 9DCh
output stream 6: Offset 9ECh
Output stream 7: Offset 9FCh
Output stream 8: Offset A0Ch
Output stream 9: Offset 4B7Ch
Output stream 10: Offset 4B8Ch
Output stream 11: Offset 4B9Ch
Output stream 12: Offset 4BACh
Output stream 13: Offset 4BBCh
Output stream 14: Offset 4BCCh

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits linear link position value. The 64 bits linear link position value increments on every sample block being transferred over the audio link. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.390 Multiple Links Capability Header (MLCH)—Offset C00h

This register declares the multiple links capability structure.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 20800h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RW/L	**Capability Version (VER):** This field is an Intel HD Audio Specification defined version number that indicates the version of the capability structure present. Locked when FNCFG.BCLD = 1.
27:16	2h RW/L	**Capability Identifier (ID):** This field is an Intel HD Audio Specification defined ID number that indicates the nature and format of the capability. Locked when FNCFG.BCLD = 1.
15:0	800h RW/L	**Next Capability Pointer (PTR):** This field contains the offset to the next capability structure or 000h if no other items exist in the linked list of capabilities. Point to Processing Pipe capability. Locked when FNCFG.BCLD = 1.

5.2.391 Multiple Links Capability Declaration (MLCD)—Offset C04h

This register identifies the general multiple links associated capabilities.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	1h RO	**Link Count (LCOUNT):** Indicates the number of links. Up to 15 links can be supported. A '0' indicates 1 link, and '1110' indicates 15 links. Note: '1111' is reserved. Note that this Link Count is the cumulative total number of links where the links can be heterogeneous.

5.2.392 Link x Capabilities (LCAP0)—Offset C40h

This register identifies the specific link associated capabilities

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 7h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RW/L	**Audio Link Type (ALT):** Indicates which Link Type this link belongs to. 0001-1111 = Reserved 0000 = Intel HD Audio Link Reset value is hardcoded to parameter LCAPALT[x*4+3:x*4]. Locked when FNCFG.BCLD = 1.
27:26	0h RO	Reserved.
25:24	0h RW/L	**Number of Serial Data Out Signals (NSDO):** 00b indicates that the Intel HD Audio controller supports one Serial Data Output signal. Locked when FNCFG.BCLD = 1.

Bit Range	Default and Access	Field Name (ID): Description
23:6	0h RO	Reserved.
5	0h RW/L	**192 MHz Supported (S192):** Indicates 192 MHz clock is supported. Reset value is hardcoded to parameter DEFLCAPS192[x]. Locked when FNCFG.BCLD = 1.
4	0h RW/L	**96 MHz Supported (S96):** Indicates 96 MHz clock is supported. Reset value is hardcoded to parameter DEFLCAPS96[x]. Locked when FNCFG.BCLD = 1.
3	0h RW/L	**48 MHz Supported (S48):** Indicates 48 MHz clock is supported. Reset value is hardcoded to parameter DEFLCAPS48[x]. Locked when FNCFG.BCLD = 1.
2	1h RW/L	**24 MHz Supported (S24):** Indicates 24 MHz clock is supported. Reset value is hardcoded to parameter DEFLCAPS24[x]. Locked when FNCFG.BCLD = 1.
1	1h RW/L	**12 MHz Supported (S12):** Indicates 12 MHz clock is supported. Reset value is hardcoded to parameter DEFLCAPS12[x]. Locked when FNCFG.BCLD = 1.
0	1h RW/L	**6 MHz Supported (S6):** Indicates 6 MHz clock is supported. Reset value is hardcoded to parameter DEFLCAPS6[x]. Locked when FNCFG.BCLD = 1.

5.2.393 Link Control 0 (LCTL0)—Offset C44h

Link x Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 10002h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RO/V	**Current Power Active (CPA):** This value changes to the value set by SPA when the power of the link has reached that state. Software sets SPA, then monitors CPA to know when the link has changed state.
22:17	0h RO	Reserved.
16	1h RW	**Set Power Active (SPA):** Software sets this bit to '1' to turn the link on (provided CRSTB = 1), and clears it to '0' when it wishes to turn the link off. When CPA matches the value of this bit, the achieved power state has been reached. Software is expected to wait for CPA to match SPA before it can program SPA again. Any deviation may result in undefined behaviour
15:4	0h RO	Reserved.
3:0	2h RW	**Set Clock Frequency (SCF):** Indicates the frequency that software wishes the link to run at. Changing this value to a value not supported by Link Capabilities shall result in indeterminate results. The possible encodings are: Encoding Frequency 0000 6 MHz 0001 12 MHz 0010 24 MHz 0011 48 MHz 0100 96 MHz 0101 Reserved for 192 MHz 0110-1111 Reserved

5.2.394 Link x Output Stream ID Mapping Valid (LOSIDV0)—Offset C48h

This register maps the output stream connection for specific link.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FFFEh

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	1h RW	**Output Stream ID of 15 is Valid for this Link (L1OSIDV15):** This link will claim / forward output cycles with Stream ID = 1111b.
14	1h RW	**Output Stream ID of 14 is Valid for this Link (L1OSIDV14):** This link will claim / forward output cycles with Stream ID = 1110b.
13	1h RW	**Output Stream ID of 13 is Valid for this Link (L1OSIDV13):** This link will claim / forward output cycles with Stream ID = 1101b.
12	1h RW	**Output Stream ID of 12 is Valid for this Link (L1OSIDV12):** This link will claim / forward output cycles with Stream ID = 1100b.
11	1h RW	**Output Stream ID of 11 is Valid for this Link (L1OSIDV11):** This link will claim / forward output cycles with Stream ID = 1011b.
10	1h RW	**Output Stream ID of 10 is Valid for this Link (L1OSIDV10):** This link will claim / forward output cycles with Stream ID = 1010b.
9	1h RW	**Output Stream ID of 9 is Valid for this Link (L1OSIDV9):** This link will claim / forward output cycles with Stream ID = 1001b.
8	1h RW	**Output Stream ID of 8 is Valid for this Link (L1OSIDV8):** This link will claim / forward output cycles with Stream ID = 1000b.
7	1h RW	**Output Stream ID of 7 is Valid for this Link (L1OSIDV7):** This link will claim / forward output cycles with Stream ID = 0111b.
6	1h RW	**Output Stream ID of 6 is Valid for this Link (L1OSIDV6):** This link will claim / forward output cycles with Stream ID = 0110b.
5	1h RW	**Output Stream ID of 5 is Valid for this Link (L1OSIDV5):** This link will claim / forward output cycles with Stream ID = 0101b.
4	1h RW	**Output Stream ID of 4 is Valid for this Link (L1OSIDV4):** This link will claim / forward output cycles with Stream ID = 0100b.
3	1h RW	**Output Stream ID of 3 is Valid for this Link (L1OSIDV3):** This link will claim / forward output cycles with Stream ID = 0011b.
2	1h RW	**Output Stream ID of 2 is Valid for this Link (L1OSIDV2):** This link will claim / forward output cycles with Stream ID = 0010b.
1	1h RW	**Output Stream ID of 1 is Valid for this Link (L1OSIDV1):** This link will claim / forward output cycles with Stream ID = 0001b.
0	0h RO	Reserved.

5.2.395 Link 0 SDI Identifier (LSDIID0)—Offset C4Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 3h

Bit Range	Default and Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14	0h RO	**SDI 14 (SDIID14):** This link uses SDI 14. This bit is hardcoded per parameter LSDIID14 assignment.
13	0h RO	**SDI 13 (SDIID13):** This link uses SDI 13. This bit is hardcoded per parameter LSDIID13 assignment.
12	0h RO	**SDI 12 (SDIID12):** This link uses SDI 12. This bit is hardcoded per parameter LSDIID12 assignment.
11	0h RO	**SDI 11 (SDIID11):** This link uses SDI 11. This bit is hardcoded per parameter LSDIID11 assignment.
10	0h RO	**SDI 10 (SDIID10):** This link uses SDI 10. This bit is hardcoded per parameter LSDIID10 assignment.
9	0h RO	**SDI 9 (SDIID9):** This link uses SDI 9. This bit is hardcoded per parameter LSDIID9 assignment.
8	0h RO	**SDI 8 (SDIID8):** This link uses SDI 8. This bit is hardcoded per parameter LSDIID8 assignment.
7	0h RO	**SDI 7 (SDIID7):** This link uses SDI 7. This bit is hardcoded per parameter LSDIID7 assignment.
6	0h RO	**SDI 6 (SDIID6):** This link uses SDI 6. This bit is hardcoded per parameter LSDIID6 assignment.
5	0h RO	**SDI 5 (SDIID5):** This link uses SDI 5. This bit is hardcoded per parameter LSDIID5 assignment.
4	0h RO	**SDI 4 (SDIID4):** This link uses SDI 4. This bit is hardcoded per parameter LSDIID4 assignment.
3	0h RO	**SDI 3 (SDIID3):** This link uses SDI 3. This bit is hardcoded per parameter LSDIID3 assignment.
2	0h RO	**SDI 2 (SDIID2):** This link uses SDI 2. This bit is hardcoded per parameter LSDIID2 assignment.
1	1h RO	**SDI 1 (SDIID1):** This link uses SDI 1. This bit is hardcoded per parameter LSDIID1 assignment.
0	1h RO	**SDI 0 (SDIID0):** This link uses SDI 0. This bit is hardcoded per parameter LSDIID0 assignment.

5.2.396 Link x Per Stream Output Overhead (LPSOO0)—Offset C50h

This register reports the output stream overhead for specific link.

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO/V	**Per Stream Output Overhead (PSOO):** Indicates the SDO Output Overhead on a per stream basis. This does not include bandwidth used for command and control. This measurement is in byte quantities per 48 kHz frame. Software calculates available link bandwidth in bytes with the following formula: (2 * LOUTPAY) - (NumOfStreams * LPSOO).

5.2.397 Link x Per Stream Input Overhead (LPSIO0)—Offset C52h

This register reports the input stream overhead for specific link.

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO/V	**Per Stream Input Overhead (PSIO):** Indicates the SDI Input Overhead on a per stream basis. This does not include bandwidth used for response. This measurement is in byte quantities per 48 kHz frame. Software calculates available link bandwidth in bytes with the following formula: (2 * LINPAY) - (NumOfStreams * LPSIO).

5.2.398 Link x Wall Frame Counter (LWALFC0)—Offset C58h

This register reports the wall frame counter for specific link.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:9	0h RO/V	**Frame Number (FN):** 23 bit counter that is incremented when CIF rolls over from 499 to 0. This counter will roll over to zero with a period of approximately 174 seconds.
8:0	0h RO/V	**Clock in Frame (CIF):** 9 bit counter that is incremented on each link BCLK period and rolls over from 499 to 0. This counter will roll over to zero with a period of 48 KHz HD Audio frame. With the introduction of multiple link segments for the Intel HD Audio controller, and the capability of running each link segment at different clock speed, the BCLK definition is fixed at 24 MHz equivalent rate always, independent of the physical link clock speed.

5.2.399 Link x Capabilities (LCAP1)—Offset C80h

This register identifies the specific link associated capabilities

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1Fh

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RW/L	**Audio Link Type (ALT):** Indicates which Link Type this link belongs to. 0001-1111 = Reserved 0000 = Intel HD Audio Link Locked when FNCFG.BCLD = 1.
27:26	0h RO	Reserved.
25:24	0h RW/L	**Number of Serial Data Out Signals (NSDO):** 00b indicates that the Intel HD Audio controller supports one Serial Data Output signal. Locked when FNCFG.BCLD = 1.
23:6	0h RO	Reserved.
5	0h RW/L	**192 MHz Supported (S192):** Indicates 192 MHz clock is supported. Locked when FNCFG.BCLD = 1.
4	1h RW/L	**96 MHz Supported (S96):** Indicates 96 MHz clock is supported. Locked when FNCFG.BCLD = 1.
3	1h RW/L	**48 MHz Supported (S48):** Indicates 48 MHz clock is supported. Locked when FNCFG.BCLD = 1.
2	1h RW/L	**24 MHz Supported (S24):** Indicates 24 MHz clock is supported. Locked when FNCFG.BCLD = 1.
1	1h RW/L	**12 MHz Supported (S12):** Indicates 12 MHz clock is supported. Locked when FNCFG.BCLD = 1.
0	1h RW/L	**6 MHz Supported (S6):** Indicates 6 MHz clock is supported. Locked when FNCFG.BCLD = 1.

5.2.400 Link x Control (LCTL1)—Offset C84h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 10004h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RO/V	**Current Power Active (CPA):** This value changes to the value set by SPA when the power of the link has reached that state. Software sets SPA, then monitors CPA to know when the link has changed state.
22:17	0h RO	Reserved.
16	1h RW	**Set Power Active (SPA):** Software sets this bit to '1' to turn the link on (provided CRSTB = 1), and clears it to '0' when it wishes to turn the link off. When CPA matches the value of this bit, the achieved power state has been reached. Software is expected to wait for CPA to match SPA before it can program SPA again. Any deviation may result in undefined behaviour
15:4	0h RO	Reserved.
3:0	4h RW	**Set Clock Frequency (SCF):** Indicates the frequency that software wishes the link to run at. Changing this value to a value not supported by Link Capabilities shall result in indeterminate results. The possible encodings are: Encoding Frequency 0000 6 MHz 0001 12 MHz 0010 24 MHz 0011 48 MHz 0100 96 MHz 0101 Reserved for 192 MHz 0110-1111 Reserved

5.2.401 Link 1 Output Stream ID Mapping Valid (LOSIDV1)—Offset C88h

This register maps the output stream connection for specific link.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: FFFEh

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	1h RW	**Output Stream ID of 15 is Valid for this Link (L1OSIDV15):** This link will claim / forward output cycles with Stream ID = 1111b.
14	1h RW	**Output Stream ID of 14 is Valid for this Link (L1OSIDV14):** This link will claim / forward output cycles with Stream ID = 1110b.
13	1h RW	**Output Stream ID of 13 is Valid for this Link (L1OSIDV13):** This link will claim / forward output cycles with Stream ID = 1101b.
12	1h RW	**Output Stream ID of 12 is Valid for this Link (L1OSIDV12):** This link will claim / forward output cycles with Stream ID = 1100b.
11	1h RW	**Output Stream ID of 11 is Valid for this Link (L1OSIDV11):** This link will claim / forward output cycles with Stream ID = 1011b.
10	1h RW	**Output Stream ID of 10 is Valid for this Link (L1OSIDV10):** This link will claim / forward output cycles with Stream ID = 1010b.

Bit Range	Default and Access	Field Name (ID): Description
9	1h RW	**Output Stream ID of 9 is Valid for this Link (L1OSIDV9):** This link will claim / forward output cycles with Stream ID = 1001b.
8	1h RW	**Output Stream ID of 8 is Valid for this Link (L1OSIDV8):** This link will claim / forward output cycles with Stream ID = 1000b.
7	1h RW	**Output Stream ID of 7 is Valid for this Link (L1OSIDV7):** This link will claim / forward output cycles with Stream ID = 0111b.
6	1h RW	**Output Stream ID of 6 is Valid for this Link (L1OSIDV6):** This link will claim / forward output cycles with Stream ID = 0110b.
5	1h RW	**Output Stream ID of 5 is Valid for this Link (L1OSIDV5):** This link will claim / forward output cycles with Stream ID = 0101b.
4	1h RW	**Output Stream ID of 4 is Valid for this Link (L1OSIDV4):** This link will claim / forward output cycles with Stream ID = 0100b.
3	1h RW	**Output Stream ID of 3 is Valid for this Link (L1OSIDV3):** This link will claim / forward output cycles with Stream ID = 0011b.
2	1h RW	**Output Stream ID of 2 is Valid for this Link (L1OSIDV2):** This link will claim / forward output cycles with Stream ID = 0010b.
1	1h RW	**Output Stream ID of 1 is Valid for this Link (L1OSIDV1):** This link will claim / forward output cycles with Stream ID = 0001b.
0	0h RO	Reserved.

5.2.402 Link 1 SDI Identifier (LSDIID1)—Offset C8Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14	0h RO	**SDI 14 (SDIID14):** This link uses SDI 14.
13	0h RO	**SDI 13 (SDIID13):** This link uses SDI 13.
12	0h RO	**SDI 12 (SDIID12):** This link uses SDI 12.
11	0h RO	**SDI 11 (SDIID11):** This link uses SDI 11.
10	0h RO	**SDI 10 (SDIID10):** This link uses SDI 10.
9	0h RO	**SDI 9 (SDIID9):** This link uses SDI 9.

Bit Range	Default and Access	Field Name (ID): Description
8	0h RO	**SDI 8 (SDIID8):** This link uses SDI 8.
7	0h RO	**SDI 7 (SDIID7):** This link uses SDI 7.
6	0h RO	**SDI 6 (SDIID6):** This link uses SDI 6.
5	0h RO	**SDI 5 (SDIID5):** This link uses SDI 5.
4	0h RO	**SDI 4 (SDIID4):** This link uses SDI 4.
3	0h RO	**SDI 3 (SDIID3):** This link uses SDI 3.
2	1h RO	**SDI 2 (SDIID2):** This link uses SDI 2.
1	0h RO	**SDI 1 (SDIID1):** This link uses SDI 1.
0	0h RO	**SDI 0 (SDIID0):** This link uses SDI 0.

5.2.403 Link x Per Stream Output Overhead (LPSOO1)—Offset C90h

This register reports the output stream overhead for specific link.

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO/V	**Per Stream Output Overhead (PSOO):** Indicates the SDO Output Overhead on a per stream basis. This does not include bandwidth used for command and control. This measurement is in byte quantities per 48 kHz frame. Software calculates available link bandwidth in bytes with the following formula: (2 * LOUTPAY) - (NumOfStreams * LPSOO).

5.2.404 Link x Per Stream Input Overhead (LPSIO1)—Offset C92h

This register reports the input stream overhead for specific link.

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO/V	**Per Stream Input Overhead (PSIO):** Indicates the SDI Input Overhead on a per stream basis. This does not include bandwidth used for response. This measurement is in byte quantities per 48 kHz frame. Software calculates available link bandwidth in bytes with the following formula: (2 * LINPAY) - (NumOfStreams * LPSIO).

5.2.405 Link 1 Wall Frame Counter (LWALFC1)—Offset C98h

This register reports the wall frame counter for specific link.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:9	0h RO/V	**Frame Number (FN):** 23 bit counter that is incremented when CIF rolls over from 499 to 0. This counter will roll over to zero with a period of approximately 174 seconds.
8:0	0h RO/V	**Clock in Frame (CIF):** 9 bit counter that is incremented on each link BCLK period and rolls over from 499 to 0. This counter will roll over to zero with a period of 48 KHz HD Audio frame. With the introduction of multiple link segments for the Intel HD Audio controller, and the capability of running each link segment at different clock speed, the BCLK definition is fixed at 24 MHz equivalent rate always, independent of the physical link clock speed.

5.2.406 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC7LLPL)—Offset 4A10h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.407 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC7LLPU)—Offset 4A14h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.408 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC7LDPL)—Offset 4A18h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.409 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC7LDPU)—Offset 4A1Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.410 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC8LLPL)—Offset 4A20h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.411 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC8LLPU)—Offset 4A24h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.412 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC8LDPL)—Offset 4A28h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.413 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC8LDPU)—Offset 4A2Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.414 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC9LLPL)—Offset 4A30h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.415 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC9LLPU)—Offset 4A34h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.416 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC9LDPL)—Offset 4A38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.417 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC9LDPU)—Offset 4A3Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.418 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC10LLPL)—Offset 4A40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.419 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC10LLPU)—Offset 4A44h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.420 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC10LDPL)—Offset 4A48h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.421 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC10LDPU)—Offset 4A4Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.422 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC11LLPL)—Offset 4A50h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.423 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC11LLPU)—Offset 4A54h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.424 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC11LDPL)—Offset 4A58h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.425 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC11LDPU)—Offset 4A5Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.426 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC12LLPL)—Offset 4A60h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.427 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC12LLPU)—Offset 4A64h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.428 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC12LDPL)—Offset 4A68h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.429 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC12LDPU)—Offset 4A6Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.430 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC13LLPL)—Offset 4A70h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.431 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC13LLPU)—Offset 4A74h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.432 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC13LDPL)—Offset 4A78h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.433 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC13LDPU)—Offset 4A7Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.434 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (IPPHC14LLPL)—Offset 4A80h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.435 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (IPPHC14LLPU)—Offset 4A84h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.436 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (IPPHC14LDPL)—Offset 4A88h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.437 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (IPPHC14LDPU)—Offset 4A8Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.438 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC9LLPL)—Offset 4A90h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.439 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC9LLPU)—Offset 4A94h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.440 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC9LDPL)—Offset 4A98h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.441 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC9LDPU)—Offset 4A9Ch

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.442 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC10LLPL)—Offset 4AA0h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.443 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC10LLPU)—Offset 4AA4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.444 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC10LDPL)—Offset 4AA8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.445 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC10LDPU)—Offset 4AACh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.446 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC11LLPL)—Offset 4AB0h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.447 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC11LLPU)—Offset 4AB4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.448 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC11LDPL)—Offset 4AB8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.449 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC11LDPU)—Offset 4ABCh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.450 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC12LLPL)—Offset 4AC0h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.451 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC12LLPU)—Offset 4AC4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.452 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC12LDPL)—Offset 4AC8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.453 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC12LDPU)—Offset 4ACCh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.454 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC13LLPL)—Offset 4AD0h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.455 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC13LLPU)—Offset 4AD4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.456 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC13LDPL)—Offset 4AD8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.457 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC13LDPU)—Offset 4ADCh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.458 Input/Output Processing Pipe's Host Connection x Linear Link Position Lower (OPPHC14LLPL)—Offset 4AE0h

his register reports the linear link position (lower 32 bits) on the host connection end of the processing pipe. This register provides the status of the processing pipe operation.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Lower (LLPL):** Indicates the lower 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.459 Input/Output Processing Pipe's Host Connection x Linear Link Position Upper (OPPHC14LLPU)—Offset 4AE4h

This register reports the linear link position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear Link Position Upper (LLPU):** Indicates the upper 32 bits of the 64 bits relative linear link position value, w.r.t. to the associated processing pipe's link connection linear link position. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.460 Input/Output Processing Pipe's Host Connection x Linear DMA Position Lower (OPPHC14LDPL)—Offset 4AE8h

This register reports the linear DMA position (lower 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Lower (LDPL):** Indicates the lower 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.461 Input/Output Processing Pipe's Host Connection x Linear DMA Position Upper (OPPHC14LDPU)—Offset 4AECh

This register reports the linear DMA position (upper 32 bits) on the host connection end of the processing pipe.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Linear DMA Position Offset Upper (LDPU):** Indicates the upper 32 bits of the 64 bits linear DMA position value. Input Stream: For an input stream the 64 bits value is incremented when data is written to the PCH backbone. Output Stream: For an output stream the 64 bits value is incremented when a read completion is loaded into the DSP host gateway buffer. Note that SW may initialize the value for resume operation usage before RUN bit is set for the first time (and if RSM = 1). Once RUN bit is set, the register will become read only until SRST occurs.

5.2.462 Input/Output Processing Pipe's Link Connection x Control (IPPLC7CTL)—Offset 4AF0h

SRST bit is not affected by stream reset.

5.2.463 Input/Output Processing Pipe's Link Connection x Format (IPPLC7FMT)—Offset 4AF4h

This register specifies the audio format on the link connection end of the processing pipe.

5.2.464 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC7LLPL)—Offset 4AF8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

5.2.465 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC7LLPU)—Offset 4AFCh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

5.2.466 Input/Output Processing Pipe's Link Connection x Control (IPPLC8CTL)—Offset 4B00h

SRST bit is not affected by stream reset.

5.2.467 Input/Output Processing Pipe's Link Connection x Format (IPPLC8FMT)—Offset 4B04h

This register specifies the audio format on the link connection end of the processing pipe.

5.2.468 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC8LLPL)—Offset 4B08h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

5.2.469 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC8LLPU)—Offset 4B0Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

5.2.470 Input/Output Processing Pipe's Link Connection x Control (IPPLC9CTL)—Offset 4B10h

SRST bit is not affected by stream reset.

5.2.471 Input/Output Processing Pipe's Link Connection x Format (IPPLC9FMT)—Offset 4B14h

This register specifies the audio format on the link connection end of the processing pipe.

5.2.472 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC9LLPL)—Offset 4B18h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

5.2.473 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC9LLPU)—Offset 4B1Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

5.2.474 Input/Output Processing Pipe's Link Connection x Control (IPPLC10CTL)—Offset 4B20h

SRST bit is not affected by stream reset.

5.2.475 Input/Output Processing Pipe's Link Connection x Format (IPPLC10FMT)—Offset 4B24h

This register specifies the audio format on the link connection end of the processing pipe.

5.2.476 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC10LLPL)—Offset 4B28h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

5.2.477 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC10LLPU)—Offset 4B2Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

5.2.478 Input/Output Processing Pipe's Link Connection x Control (IPPLC11CTL)—Offset 4B30h

SRST bit is not affected by stream reset.

5.2.479 Input/Output Processing Pipe's Link Connection x Format (IPPLC11FMT)—Offset 4B34h

This register specifies the audio format on the link connection end of the processing pipe.

5.2.480 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC11LLPL)—Offset 4B38h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

5.2.481 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC11LLPU)—Offset 4B3Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

5.2.482 Input/Output Processing Pipe's Link Connection x Control (IPPLC12CTL)—Offset 4B40h

SRST bit is not affected by stream reset.

5.2.483 Input/Output Processing Pipe's Link Connection x Format (IPPLC12FMT)—Offset 4B44h

This register specifies the audio format on the link connection end of the processing pipe.

5.2.484 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC12LLPL)—Offset 4B48h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

5.2.485 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC12LLPU)—Offset 4B4Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

5.2.486 Input/Output Processing Pipe's Link Connection x Control (IPPLC13CTL)—Offset 4B50h

SRST bit is not affected by stream reset.

5.2.487 Input/Output Processing Pipe's Link Connection x Format (IPPLC13FMT)—Offset 4B54h

This register specifies the audio format on the link connection end of the processing pipe.

5.2.488 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC13LLPL)—Offset 4B58h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

5.2.489 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC13LLPU)—Offset 4B5Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

5.2.490 Input/Output Processing Pipe's Link Connection x Control (IPPLC14CTL)—Offset 4B60h

SRST bit is not affected by stream reset.

5.2.491 Input/Output Processing Pipe's Link Connection x Format (IPPLC14FMT)—Offset 4B64h

This register specifies the audio format on the link connection end of the processing pipe.

5.2.492 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (IPPLC14LLPL)—Offset 4B68h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

5.2.493 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (IPPLC14LLPU)—Offset 4B6Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

5.2.494 Input/Output Processing Pipe's Link Connection x Control (OPPLC9CTL)—Offset 4B70h

SRST bit is not affected by stream reset.

5.2.495 Input/Output Processing Pipe's Link Connection x Format (OPPLC9FMT)—Offset 4B74h

This register specifies the audio format on the link connection end of the processing pipe.

5.2.496 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC9LLPL)—Offset 4B78h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

5.2.497 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC9LLPU)—Offset 4B7Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

5.2.498 Input/Output Processing Pipe's Link Connection x Control (OPPLC10CTL)—Offset 4B80h

SRST bit is not affected by stream reset.

5.2.499 Input/Output Processing Pipe's Link Connection x Format (OPPLC10FMT)—Offset 4B84h

This register specifies the audio format on the link connection end of the processing pipe.

5.2.500 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC10LLPL)—Offset 4B88h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

5.2.501 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC10LLPU)—Offset 4B8Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

5.2.502 Input/Output Processing Pipe's Link Connection x Control (OPPLC11CTL)—Offset 4B90h

SRST bit is not affected by stream reset.

5.2.503 Input/Output Processing Pipe's Link Connection x Format (OPPLC11FMT)—Offset 4B94h

This register specifies the audio format on the link connection end of the processing pipe.

5.2.504 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC11LLPL)—Offset 4B98h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

5.2.505 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC11LLPU)—Offset 4B9Ch

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

5.2.506 Input/Output Processing Pipe's Link Connection x Control (OPPLC12CTL)—Offset 4BA0h

SRST bit is not affected by stream reset.

5.2.507 Input/Output Processing Pipe's Link Connection x Format (OPPLC12FMT)—Offset 4BA4h

This register specifies the audio format on the link connection end of the processing pipe.

5.2.508 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC12LLPL)—Offset 4BA8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

5.2.509 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC12LLPU)—Offset 4BACh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

5.2.510 Input/Output Processing Pipe's Link Connection x Control (OPPLC13CTL)—Offset 4BB0h

SRST bit is not affected by stream reset.

5.2.511 Input/Output Processing Pipe's Link Connection x Format (OPPLC13FMT)—Offset 4BB4h

This register specifies the audio format on the link connection end of the processing pipe.

5.2.512 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC13LLPL)—Offset 4BB8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

5.2.513 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC13LLPU)—Offset 4BBCh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

5.2.514 Input/Output Processing Pipe's Link Connection x Control (OPPLC14CTL)—Offset 4BC0h

SRST bit is not affected by stream reset.

5.2.515 Input/Output Processing Pipe's Link Connection x Format (OPPLC14FMT)—Offset 4BC4h

This register specifies the audio format on the link connection end of the processing pipe.

5.2.516 Input/Output Processing Pipe's Link Connection x Linear Link Position Lower (OPPLC14LLPL)—Offset 4BC8h

This register reports the linear link position (lower 32 bits) on the link connection end of the processing pipe.

5.2.517 Input/Output Processing Pipe's Link Connection x Linear Link Position Upper (OPPLC14LLPU)—Offset 4BCCh

This register reports the linear link position (upper 32 bits) on the link connection end of the processing pipe.

5.3 HDA PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 5-3. Summary of HDA PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
530h	533h	Function Configuration (FNCFG)—Offset 530h	2Ah

5.3.1 Function Configuration (FNCFG)—Offset 530h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2Ah

Bit Range	Default and Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	1h RW	**Power Gating Disable (PGDIS):** When cleared, it allows power gating to take place per their associated enable and idle conditions. When set, it globally disables all power gating.
4	0h RW/O/L	**BIOS Configuration Lock Down (BCLD):** BIOS Configuration Lock Down (BCLD): When set, it indicates BIOS configuration is done and ready for operations. It also locks down related RW/L bits.
3	1h RW	**Clock Gating Disable (CGD):** Clock Gating Disabled (CGD): When cleared, it allows local / dynamic clock gating and trunk clock gating to take place per their associated enable and idle conditions. When set, it globally disables all clock gating.
2	0h RW/L	**Audio DSP Disable (ADSPD):** Audio DSP Disable (ADSPD): When set, the Audio DSP is disabled and all register access associated with Audio DSP are treated as unsupported request, and return UR response if it is non-posted cycle. This bit does not affect cycles from IOSF Sideband Interface. Locked when FNCFG.BCLD = 1.
1	1h RW/L	**HD Audio Subsystem as PCI Device (HDASPCID):** HD Audio Subsystem as PCI Device (HDASPCID): When this bit is set to 1, the Intel HD Audio subsystem will appear as a PCI device to SW. When this bit is 0, the Intel HD Audio subsystem will appear as a PCI-Express device to SW. Locked when FNCFG.BCLD = 1.
0	0h RW/L	**HD Audio Subsystem Disable (HDASD):** HD Audio Subsystem Disable (HDASD): When set, the Intel HD Audio subsystem (including Audio DSP) is disabled and all register access are treated as unsupported request, and return UR response if it is non-posted cycle. This bit does not affect cycles from IOSF Sideband Interface. Locked when FNCFG.BCLD = 1.

6 SMBus Interface (D31:F4)

6.1 SMBus Configuration Registers Summary

Table 6-1. Summary of SMBus Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Vendor ID (VID)—Offset 0h	8086h
2h	3h	Device ID (DID)—Offset 2h	XXXXh
4h	5h	Command Register (CMD)—Offset 4h	0h
6h	7h	Device Status (DS)—Offset 6h	280h
8h	8h	Revision ID (RID)—Offset 8h	XXh
9h	9h	Programming Interface (PI)—Offset 9h	0h
Ah	Ah	Sub Class Code (SCC)—Offset Ah	5h
Bh	Bh	Base Class Code (BCC)—Offset Bh	Ch
10h	13h	SMBus Memory Base Address_31_0 (SMBMBAR_31_0)—Offset 10h	4h
14h	17h	SMBus Memory Base Address_63_32 (SMBMBAR_63_32)—Offset 14h	0h
20h	23h	SMB Base Address (SBA)—Offset 20h	1h
2Ch	2Dh	Subsystem Vendor Identifiers (SVID)—Offset 2Ch	0h
2Eh	2Fh	Subsystem Identifiers (SID)—Offset 2Eh	0h
3Ch	3Ch	Interrupt Line (INTLN)—Offset 3Ch	0h
3Dh	3Dh	Interrupt Pin (INTPN)—Offset 3Dh	1h
40h	40h	Host Configuration (HCFG)—Offset 40h	0h
50h	53h	TCO Base Address (TCOBASE)—Offset 50h	1h
54h	57h	TCO Control (TCOCTL)—Offset 54h	0h
80h	83h	SMBus Power Gating (SMBSM)—Offset 80h	0h

6.1.1 Vendor ID (VID)—Offset 0h

Vendor ID

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 8086h

Bit Range	Default and Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID):** Value indicates Intel as the vendor

6.1.2 Device ID (DID)—Offset 2h

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 4

Default: XXXXh

Bit Range	Default and Access	Field Name (ID): Description
15:0	-- RO/V	**Device ID (DID):** Indicates the value assigned to the PCH SMBus controller. Refer to the Device and Revision ID Table in Volume 1 for default setting.

6.1.3 Command Register (CMD)—Offset 4h

Command Register

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTD):** 1 = Disables SMBus to assert its PIRQB# signal. Defaults to 0.
9	0h RO	**Fast Back to Back Enable (FBE):** Reserved as 0. Read Only.
8	0h RW	**SERR# Enable (SERRE):** 1 = Enables SERR# generation
7	0h RO	**Wait Cycle Control (WCC):** Reserved as 0. Read Only.
6	0h RW	**Parity Error Response (PER):** 1 = Sets Detected Parity Error bit when parity error is detected
5	0h RO	**VGA Palette Snoop (VGAPS):** Reserved as 0. Read Only.
4	0h RO	**Postable Memory Write Enable (PMWE):** Reserved as 0. Read Only.
3	0h RO	**Special Cycle Enable (SCE):** Reserved as 0. Read Only.

Bit Range	Default and Access	Field Name (ID): Description
2	0h RO	**Bus Master Enable (BME):** Reserved as 0. Read Only.
1	0h RW	**Memory Space Enable (MSE):** 1= Enables memory mapped config space.
0	0h RW	**I/O Space Enable (IOSE):** 1= enables access to the SM Bus I/O space registers as defined by the Base Address Register.

6.1.4 Device Status (DS)—Offset 6h

Device Status

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 280h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RW/1C	**Detected Parity Error (DPE):** 1 = Parity error detected
14	0h RW/1C	**Signaled System Error (SSE):** 1 = System error detected
13	0h RO	**Received Master Abort (RMA):** Reserved as 0.
12	0h RO	**Received Target Abort (RTA):** Reserved as '0'.
11	0h RW/1C	**Signaled Target-Abort Status (STA):** Reserved as 0.
10:9	1h RO	**DEVSEL# Timing Status (DEVT):** This 2-bit field defines the timing for DEVSEL# assertion. These read only bits indicate the Intel PCH's DEVSEL# timing when performing a positive decode. Note: Intel PCH generates DEVSEL# with medium time.
8	0h RO	**Data Parity Error Detected (DPED):** Reserved as 0.
7	1h RO	**Fast Back-to-Back Capable (FBC):** Reserved as '1'.
6	0h RO	**User Definable Features (UDF):** Reserved as 0.
5	0h RO	**66 MHz Capable (C_66M):** Reserved as 0.
4	0h RO	**Capabilities List Indicator (CLI):** Hardwired to 0 because there are no capability list structures in this function.
3	0h RO	**Interrupt Status (INTS):** This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the command register.
2:0	0h RO	Reserved.

6.1.5 Revision ID (RID)—Offset 8h

Revision ID

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: XXh

Bit Range	Default and Access	Field Name (ID): Description
7:0	-- RO	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

6.1.6 Programming Interface (PI)—Offset 9h

Programming Interface

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO	**Programming Interface (PI):** No programming interface defined.

6.1.7 Sub Class Code (SCC)—Offset Ah

Sub Class Code

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 5h

Bit Range	Default and Access	Field Name (ID): Description
7:0	5h RO	**Sub Class Code (SCC):** A value of 05h indicates that this device is a SM Bus serial controller.

6.1.8 Base Class Code (BCC)—Offset Bh

Base Class Code

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: Ch

Bit Range	Default and Access	Field Name (ID): Description
7:0	Ch RO	**Base Class Code (BCC):** A value of 0Ch indicates that this device is a serial controller

6.1.9 SMBus Memory Base Address_31_0 (SMBMBAR_31_0)—Offset 10h

SMBus Memory Base Address_31_0

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 4

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RW	**Base Address (BA):** Provides the 32 byte system memory base address for the Intel PCH SMB logic.
7:4	0h RO	**Hardwired_0 (HARDWIRED_0):** Hardwired to 0.
3	0h RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that SMBMBAR is not pre- fetchable
2:1	2h RO	**Address Range (ADDRNG):** Indicates that this SMBMBAR can be located anywhere in 64 bit address space
0	0h RO	**Memory Space Indicator (MSI):** Indicates that the SMB logic is memory mapped.

6.1.10 SMBus Memory Base Address_63_32 (SMBMBAR_63_32)—Offset 14h

SMBus Memory Base Address_63_32

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 4

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address (BA):** Bits 63-32 of SMbus Memory Base Address

6.1.11 SMB Base Address (SBA)—Offset 20h

SMB Base Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 4

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:5	0h RW	**Base Address (BA):** Provides the 32 byte t system I/O base address for the SMB logic.
4:1	0h RO	Reserved.
0	1h RO	**IO Space Indicator (IOSI):** This read-only bit always is 1, indicating that the SMB logic is I/O mapped.

6.1.12 Subsystem Vendor Identifiers (SVID)—Offset 2Ch

Subsystem Vendor ID

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW/O	**Subsystem Vendor ID (SVID):** BIOS sets the value in this register to identify the Subsystem Vendor ID. The SMBus SVID register, in combination with the SMBus Subsystem ID register, enables the operating system to distinguish each subsystem from the others. Note: The software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

6.1.13 Subsystem Identifiers (SID)—Offset 2Eh

Subsystem ID

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 31
Function: 4

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW/O	**Subsystem ID (SID):** BIOS can write to this register to identify the Subsystem ID. The SID register, in combination with the SVID, enable the operating system to distinguish each subsystem from other(s). Note: The software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

6.1.14 Interrupt Line (INTLN)—Offset 3Ch

Interrupt Line

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Line (INTLN):** This data is not used by the hardware. It is to communicate to software the interrupt line that the interrupt pin is connected to PIRQB#.

6.1.15 Interrupt Pin (INTPN)—Offset 3Dh

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
7:0	1h RW/O	**Interrupt Pin (INTPN):** This defines the interrupt pin to be used by the SMBus controller. Bits : Pins 0h : No Interrupt 1h : INTA# 2h : INTB# 3h : INTC# 4h : INTD# 5h-Fh : Reserved

6.1.16 Host Configuration (HCFG)—Offset 40h

Host Configuration

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 31
Function: 4

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:5	0h RO	Reserved.
4	0h RW/1L	**SPD Write Disable (SPDWD):** When this bit is set to 1, writes to SMBus addresses 50h – 57h are disabled. Note: This bit is R/WO and will be reset on PLTRST# assertion. This bit should be set by BIOS to '1'. Software can only program this bit when both the START bit and Host Busy bit are '0'; otherwise, the write may result in undefined behavior.
3	0h RW	**SSRESET (SSRESET):** Soft SMBUS Reset: When this bit is 1, the SMbus state machine and logic in PCH is reset. The HW will reset this bit to 0 when reset operation is completed.
2	0h RW	**I2C_EN (I2CEN):** When this bit is 1, the Intel PCH is enabled to communicate with I2C devices. This will change the formatting of some commands. When this bit is 0, behavior is for SMBus.
1	0h RW	**SMB_SMI_EN (SSEN):** When this bit is set, any source of an SMB interrupt will instead be routed to generate an SMI#.
0	0h RW	**HST_EN (HSTEN):** When set, the SMB Host Controller interface is enabled to execute commands. The HST_INT_EN bit needs to be enabled in order for the SMB Host Controller to interrupt or SMI#. Additionally, the SMB Host Controller will not respond to any new requests until all interrupt requests have been cleared.

6.1.17 TCO Base Address (TCOBASE)—Offset 50h

TCO Base Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 4

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:5	0h RW/L	**TCO Base Address (TCOBA):** Provides the 32 bytes of I/O space for TCO logic, mappable anywhere in the 64k I/O space on 32-byte boundaries.
4:1	0h RO	Reserved.
0	1h RO	**I/O Space (IOS):** Indicates an I/O Space

6.1.18 TCO Control (TCOCTL)—Offset 54h

TCO Control

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 4

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**TCO Base Enable (TCO_BASE_EN):** When set, decode of the I/O range pointed to by the TCO base register is enabled.
7:1	0h RO	Reserved.
0	0h RW/O	**TCO Base Lock (TCO_BASE_LOCK):** When set to 1, this bit locks down the TCO Base Address Register (TCOBASE) at offset 50h. The Base Address Field becomes read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset.

6.1.19 SMBus Power Gating (SMBSM)—Offset 80h

6.2 SMBus I/O and Memory Mapped I/O Registers Summary

The SMBus registers can be accessed through I/O BAR or Memory BAR registers in PCI configuration space. The offsets are the same for both I/O and Memory Mapped I/O registers.

Table 6-2. Summary of SMBus I/O and Memory Mapped I/O Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	0h	Host Status Register Address (HSTS)—Offset 0h	0h
2h	2h	Host Control Register (HCTL)—Offset 2h	0h
3h	3h	Host Command Register (HCMD)—Offset 3h	0h
4h	4h	Transmit Slave Address Register (TSA)—Offset 4h	0h
5h	5h	Data 0 Register (HD0)—Offset 5h	0h
6h	6h	Data 1 Register (HD1)—Offset 6h	0h
7h	7h	Host Block Data (HBD)—Offset 7h	0h
8h	8h	Packet Error Check Data Register (PEC)—Offset 8h	0h
9h	9h	Receive Slave Address Register (RSA)—Offset 9h	44h
Ah	Bh	Slave Data Register (SD)—Offset Ah	0h
Ch	Ch	Auxiliary Status (AUXS)—Offset Ch	0h
Dh	Dh	Auxiliary Control (AUXC)—Offset Dh	0h
Eh	Eh	SMLINK_PIN_CTL Register (SMLC)—Offset Eh	4h
Fh	Fh	SMBUS_PIN_CTL Register (SMBC)—Offset Fh	4h
10h	10h	Slave Status Register (SSTS)—Offset 10h	0h

Table 6-2. Summary of SMBus I/O and Memory Mapped I/O Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
11h	11h	Slave Command Register (SCMD)—Offset 11h	0h
14h	14h	Notify Device Address Register (NDA)—Offset 14h	0h
16h	16h	Notify Data Low Byte Register (NDLB)—Offset 16h	0h
17h	17h	Notify Data High Byte Register (NDHB)—Offset 17h	0h

6.2.1 Host Status Register Address (HSTS)—Offset 0h

All status bits are set by hardware and cleared by the software writing a one to the particular bit position. Writing a zero to any bit position has no affect.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RW/1C	**BYTE_DONE_STS (BDS):** This bit will be set to 1 when the host controller has received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands) when the 32-byte buffer is not being used. Note that this bit will be set, even on the last byte of the transfer. Software clears the bit by writing a 1 to the bit position. This bit has no meaning for block transfers when the 32- byte buffer is enabled. Note: When the last byte of a block message is received, the host controller will set this bit. However, it will not immediately set the INTR bit (bit 1 in this register). When the interrupt handler clears the BYTE_DONE_STS bit, the message is considered complete, and the host controller will then set the INTR bit (and generate another interrupt). Thus, for a block message of n bytes, the Intel PCH will generate n+1 interrupts. The interrupt handler needs to be implemented to handle these cases.
6	0h RW/1C	**In Use Status (IUS):** After a full PCI reset, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the host controller. This bit has no other effect on the hardware, and is only used as semaphore among various independent software threads that may need to use the Intel PCHs SMBus logic.
5	0h RW/1C	**SMBALERT_STS (SMSTS):** Intel PCH sets this bit to a 1 to indicates source of the interrupt or SMI# was the SMBAlert# signal. Software resets this bit by writing a 1 to this location. This bit should also be cleared by RSMRST# (but not PLTRST#).
4	0h RW/1C	**Failed (FAIL):** When set, this indicates that the source of the interrupt or SMI# was a failed bus transaction. This is set in response to the KILL bit being set to terminate the host transaction.
3	0h RW/1C	**Bus Error (BERR):** When set, this indicates the source of the interrupt or SMI# was a transaction collision.
2	0h RW/1C	**Device Error (DERR):** When set, this indicates that the source of the interrupt or SMI# was due one of the following: unsupported Command Field Unclaimed Cycle (host initiated) Host Device Time-out Error. CRC Error
1	0h RW/1C	**Interrupt (INTR):** When set, this indicates that the source of the interrupt or SMI# was the successful completion of its last command.
0	0h RW/1C	**Host Busy (HBSY):** A 1 indicates that the Intel PCH is running a command from the host interface. No SMB registers should be accessed while this bit is set. Exception: The BLOCK DATA REGISTER can be accessed when this bit is set ONLY when the SMB_CMD bits (in Host control register) are programmed for Block command or I2C Read command. This is necessary in order to check the DONE_STS bit.

6.2.2 Host Control Register (HCTL)—Offset 2h

Note: A read to this register will clear the pointer in the 32-byte buffer.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RW	**PEC_EN (PEC_EN):** When set to 1, this bit causes the host controller to perform the SMBus transaction with the Packet Error Checking phase appended. For writes, the value of the PEC byte is transferred from the PEC Register. For reads, the PEC byte is loaded in to the PEC Register. When this bit is cleared to 0, the SMBus host controller does not perform the transaction with the PEC phase appended. This bit must be written prior to the write in which the START bit is set.
6	0h RW	**START (START):** This write-only bit is used to initiate the command described in the SMB_CMD field. All registers should be setup prior to writing a 1 to this bit position. This bit always reads zero. The HOST_BUSY bit in the Host Status register (offset 00h) can be used to identify when the Intel PCH has finished the command.
5	0h RW	**LAST_BYTE (LAST_BYTE):** This bit is used for I2C Read commands. Software sets this bit to indicate that the next byte will be the last byte to be received for the block. This causes the PCH to send a NACK (instead of an ACK) after receiving the last byte. Note: This bit may be set when the TCO timer causes the SECOND_TO_STS bit to be set. SW should clear the LAST_BYTE bit (if it is set) before starting any new command. Note: In addition to I2C Read Commands, the LAST_BYTE bit will also cause Block Read/Write cycles to stop prematurely (at the end of the next byte).
4:2	0h RW	**SMB_CMD (SMB_CMD):** As shown by the bit encoding below, indicates which command the PCH is to perform. If enabled, the Intel PCH will generate an interrupt or SMI# when the command has completed. If the value is for a non-supported or reserved command, the PCH will set the device error(DEV_ERR) status bit and generate an interrupt when the START bit is set. The PCH will perform no command, and will not operate until DEV_ERR is cleared.Val. 000 - Quick: The slave address and read/write value (bit 0) are stored in the tx slave address register. 001 - Byte: This command uses the transmit slave address and command registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes the DATA0 register will contain the read data. 010 - Byte Data: This command uses the transmit slave address, command, and DATA0 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, the DATA0 register will contain the read data. 011 - Word Data: This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes the DATA0 and DATA1 registers will contain the read data. 100 - Process Call: This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. After the command completes, the DATA0 and DATA1 registers will contain the read data. 101 - Block: This command uses the transmit slave address, command, and DATA0 registers, and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block reads, the count is received and stored in the DATA0 register. Bit 0 of the slave address register selects if this is a read or write command. For writes, data is retrieved from the first n (where n is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. 110 - I2C Read: This command uses the transmit slave address, command, DATA0, DATA1 registers, and the Block Data Byte register. The read data is stored in the Block Data Byte register. The Intel PCH will continue reading data until the NAK is received. 111 - Block-Process: This command uses the transmit slave address, command, DATA0 and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block read, the count is received and stored in the DATA0 register. Bit 0 of the slave address register always indicate a write command. For writes, data is retrieved from the first m (where m is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. Note: E32B bit in the Auxiliary Control Register must be set for this command to work.
1	0h RW	**KILL (KILL):** When set, kills the current host transaction taking place, sets the FAILED status bit, and asserts the interrupt (or SMI#) selected by the SMB_INTRSEL field. This bit, once set, must be cleared to allow the SMB Host Controller to function normally.
0	0h RW	**INTREN (INTREN):** Enable the generation of an interrupt or SMI# upon the completion of the command.

6.2.3 Host Command Register (HCMD)—Offset 3h

Host Command Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Host Command Register (HCMD):** This eight bit field is transmitted by the host controller in the command field of the SMB protocol during the execution of any command.

6.2.4 Transmit Slave Address Register (TSA)—Offset 4h

This register is transmitted by the host controller in the slave address field of the SMB protocol. This is the address of the target.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:1	0h RW	**ADDRESS (ADDR):** 7-bit address of the targeted slave. Note: Writes to TSA values of A0h - AEh are blocked depending on the setting of the SPD write disable bit in HCFG - HostConfiguration.
0	0h RW	**RW (RW):** Direction of the host transfer. 1 = read, 0 = write

6.2.5 Data 0 Register (HD0)—Offset 5h

Data 0 Registe

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**DATA0/COUNT (DATA0_COUNT):** This field contains the eight bit data sent in the DATA0 field of the SMB protocol. For block write commands, this register reflects the number of bytes to transfer. This register should be programmed to a value between 1 and 32 for block counts. A count of 0 or a count above 32 will result in unpredictable behavior. The host controller does not check or log unsupported block counts.

6.2.6 Data 1 Register (HD1)—Offset 6h

Data 1 Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**DATA1 (DATA1):** This eight bit register is transmitted in the DATA1 field of the SMB protocol during the execution of any command.

6.2.7 Host Block Data (HBD)—Offset 7h

Host Block Data

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Block Data (BDTA):** This is either a register, or a pointer into a 32- byte block array, depending upon whether the E32B bit is set in the Auxiliary Control register. When the E32B bit is cleared, this is a register containing a byte of data to be sent on a block write or read from on a block read, just as it behaved on the INTEL PCH. When the E32B bit is set, reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array, which is reset to 0 by reading the HCTL register (offset 02h). The index pointer then increments automatically upon each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0. When the E2B bit is set, for writes, software will write up to 32-bytes to this register as part of the setup for the command. After the Host Controller has sent the Address, Command, and Byte Count fields, it will send the bytes in the SRAM pointed to by this register. When the E2B bit is cleared for writes, software will place a single byte in this register. After the host controller has sent the address, command, and byte count fields, it will send the byte in this register. If there is more data to send, software will write the next series of bytes to the SRAM pointed to by this register and clear the DONE_STS bit. The controller will then send the next byte. During the time between the last byte being transmitted to the next byte being transmitted, the controller will insert wait-states on the interface. When the E2B bit is set for reads, after receiving the byte count into the Data0 register, the first series of data bytes go into the SRAM pointed to by this register. If the byte count has been exhausted or the 32-byte SRAM has been filled, the controller will generate an SMI# or interrupt (depending on configuration) and set the DONE_STS bit. Software will then read the data. During the time between when the last byte is read from the SRAM to when the DONE_STS bit is cleared, the controller will insert waitstates on the interface.

6.2.8 Packet Error Check Data Register (PEC)—Offset 8h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**PEC_DATA (PEC_DATA):** This 8-bit register is written with the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software. Software must ensure that the INUSE_STS bit is properly maintained to avoid having this field over-written by a write transaction following a read transaction.

6.2.9 Receive Slave Address Register (RSA)—Offset 9h

Receive Slave Address Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 44h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO	Reserved.
6:0	44h RW	**SLAVE_ADDR[6:0] (SA_6_0):** This field is the slave address that the Intel PCH decodes for read and write cycles. The default is not 0 so that it can respond even before the CPU comes up (or if the CPU is dead). This register is reset by RSMRST#, but not by PLTRST#.

6.2.10 Slave Data Register (SD)—Offset Ah

Slave Data Register

Access Method

Type: IO Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RO/V	**SLAVE_DATA[15:0] (SD_15_0):** This field is the 16-bit data value written by the external SMBus master. The CPU can then read the value from this register. This register is reset by RSMRST#, but not by PLTRST#. SLAVE_DATA[7:0] corresponds to the Data Message Byte 0 at Slave Write Register 4 in the table. SLAVE_[15:8] corresponds to the Data Message Byte 1 at Slave Write Register 5 in the table.

6.2.11 Auxiliary Status (AUXS)—Offset Ch

All bits in this register are in the core well.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:1	0h RO	Reserved.
0	0h RW/1C	**CRC Error (CRCE):** This bit is set if a received message contained a CRC error. When this bit is set, the DERR bit of the host status register will also be set. This bit will be set by the controller if a software abort occurs in the middle of the CRC portion of the cycle or an abort happens after Intel PCH has received the final data bit transmitted by external slave.

6.2.12 Auxiliary Control (AUXC)—Offset Dh

All bits in this register are in the resume well.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:2	0h RO	Reserved.
1	0h RW	**Enable 32-byte Buffer (E32B):** When set, the Host Block Data register is a pointer into a 32-byte buffer, as opposed to a single register. This enables the block commands to transfer or receive up to 32-bytes before the Intel PCH generates an interrupt.
0	0h RW	**Automatically Append CRC (AAC):** When set, the Intel PCH will automatically append the CRC. This bit must not be changed during SM Bus transactions, or undetermined behavior will result. It should be programmed only once during the lifetime of the function.

6.2.13 SMLINK_PIN_CTL Register (SMLC)—Offset Eh

Note: This register is in the resume well and is reset by RSMRST#

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	1h RW	**SMLINK_CLK_CTL (SMLINK_CLK_CTL):** 0 = Intel PCH will drive the SMLINK[0] pin low, independent of what the other SMLINK logic would otherwise indicate for the SMLINK(0) pin. 1 = The SMLINK[0] pin is Not overdriven low. The other SMLINK logic controls the state of the pin.
1	0h RO/V	**SMLINK[1]_CUR_STS (SMLINK1_CUR_STS):** This bit has a default value that is dependent on an external signal level. This returns the value on the SMLINK[1] pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.
0	0h RO/V	**SMLINK[0]_CUR_STS (SMLINK0_CUR_STS):** This bit has a default value that is dependent on an external signal level. This returns the value on the SMLINK[0] pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.

6.2.14 SMBUS_PIN_CTL Register (SMBC)—Offset Fh

Note: This register is in the resume well and is reset by RSMRST#

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	1h RW	**SMBCLK_CTL (SMBCLK_CTL):** 0 = Intel PCH will drive the SMBCLK pin low, independent of what the other SMB logic would otherwise indicate for the SMBCLK pin. 1 = The SMBCLK pin is Not overdriven low. The other SMBus logic controls the state of the pin.
1	0h RO/V	**SMBDATA_CUR_STS (SMBDATA_CUR_STS):** This bit has a default value that is dependent on an external signal level. This returns the value on the SMBDATA pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.
0	0h RO/V	**SMBCLK_CUR_STS (SMBCLK_CUR_STS):** This bit has a default value that is dependent on an external signal level. This returns the value on the SMBCLK pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.

6.2.15 Slave Status Register (SSTS)—Offset 10h

All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:1	0h RO	Reserved.
0	0h RW/1C	**HOST_NOTIFY_STS (HNS):** The Intel PCH sets this bit to a 1 when it has completely received a successful Host Notify Command on the SMBus pins. Software reads this bit to determine that the source of the interrupt or SMI# was the reception of the Host Notify Command. Software clears this bit after reading any information needed from the Notify address and data registers by writing a 1 to this bit. Note that the Intel PCH will allow the Notify Address and Data registers to be over-written once this bit has been cleared. When this bit is 1, the Intel PCH will NACK the first byte (host address) of any new Host Notify commands on the SMBus. Writing a 0 to this bit has no effect.

6.2.16 Slave Command Register (SCMD)—Offset 11h

All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally. Also, software must confirm the prior written value before writing to the register again.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RW	**SMBALERT_DIS (SMB_D):** Software sets this bit to 1 to block the generation of the interrupt or SMI# due to the SMBALERT# source. This bit is logically inverted and ANDed with the SMBALERT_STS bit. The resulting signal is distributed to the SMI# and/or interrupt generation logic. This bit does not effect the wake logic.
1	0h RW	**HOST_NOTIFY_WKEN (HNW):** Software sets this bit to 1 to enable the reception of a Host Notify command as a wake event. When enabled this event is ORed in with the other SMBus wake events and is reflected in the SMB_WAK_STS bit of the General Purpose Event 0 Status register.
0	0h RW	**HOST_NOTIFY_INTREN (HNI):** Software sets this bit to 1 to enable the generation of interrupt or SMI# when HOST_NOTIFY_STS is 1. This enable does not affect the setting of the HOST_NOTIFY_STS bit. When the interrupt is generated, either PIRQB or SMI# is generated, depending on the value of the SMB_SMI_EN bit (D31, F3, Off40h, B1). If the HOST_NOTIFY_STS bit is set when this bit is written to a 1, then the interrupt (or SMI#) will be generated. The interrupt (or SMI#) is logically generated by ANDing the STS and INTREN bits.

6.2.17 Notify Device Address Register (NDA)—Offset 14h

Notify Device Address Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:1	0h RO/V	**DEVICE_ADDRESS (DEV_ADDR):** This field contains the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.
0	0h RO	Reserved.

6.2.18 Notify Data Low Byte Register (NDLB)—Offset 16h

Notify Data Low Byte Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO	**DATA_LOW_BYTE (DLB):** This field contains the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

6.2.19 Notify Data High Byte Register (NDHB)—Offset 17h

Notify Data High Byte Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO	**DATA_HIGH_BYTE (DHB):** This field contains the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

6.3 SMBus PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset). The offsets are DWORD aligned byte addresses.

Table 6-3. Summary of SMBus PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	TCO Configuration (TCOCFG)—Offset 0h	0h
Ch	Fh	General Control (GC)—Offset Ch	0h
10h	13h	Power Control Enable (PCE)—Offset 10h	9h

6.3.1 TCO Configuration (TCOCFG)—Offset 0h

TCO Configuration

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**TCO IRQ Enable (IE):** When set, TCO IRQ is enabled, as selected by the TCO_IRQ_SEL field. When cleared, TCO IRQ is disabled.
6:0	0h RO	Reserved.

6.3.2 General Control (GC)—Offset Ch

General Control

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**Function Disable (FD):** When set to one, this disables the PCI config register space for the SMBus device.

6.3.3 Power Control Enable (PCE)—Offset 10h

Power Control Enable

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 9h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	1h RO	**Sleep Enable (SE):** When this bit is clear, the SMBus will never asset sleep to the controller. If set, then SMBus may assert sleep during power gating.
2	0h RO	**D3-Hot Enable (D3HE):** No support for D3 Hot power gating.
1	0h RO	**I3 Enable (I3E):** No support for S0i3 power gating.
0	1h RW	**PMC Request Enable (PMCRE):** When set to 1, the SMBus will engage power gating if it is idle and other conditions are met.

7 SPI Interface (D31:F5)

7.1 SPI Configuration Registers Summary

Table 7-1. Summary of SPI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID (BIOS_SPI_DID_VID)—Offset 0h	XXXX8086h
4h	7h	Status and Command (BIOS_SPI_STS_CMD)—Offset 4h	400h
8h	Bh	Revision ID and Class Code (BIOS_SPI_CC_RID)—Offset 8h	C800000h
Ch	Fh	BIST, Header Type, Latency Timer, Cache Line Size (BIOS_SPI_BIST_HTYPE_LT_CLS)—Offset Ch	0h
10h	13h	SPI BAR0 MMIO (BIOS_SPI_BAR0)—Offset 10h	0h
D0h	D3h	SPI Unsupported Request Status (BIOS_SPI_UR_STS_CTL)—Offset D0h	0h
D8h	DBh	BIOS Decode Enable (BIOS_SPI_BDE)—Offset D8h	FFCFh
DCh	DFh	BIOS Control (BIOS_SPI_BC)—Offset DCh	28h

7.1.1 Device ID and Vendor ID (BIOS_SPI_DID_VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 5

Default: XXXX8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO/V	**Device Identification (DID):** Identifier for the SPI Flash Controller in Host Root Space. Refer to the Device and Version ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor Identification (VID):** This field identifies the manufacturer of the device. 0x8086 indicates Intel

7.1.2 Status and Command (BIOS_SPI_STS_CMD)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 400h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Detected Parity Error (DPE): 0 = No parity error detected by the controller. 1 = The controller detects a parity error on its interface.
30	0h RW/1C/V	**Signaled System Error (SSE):** Signaled System Error (SSE): 0 = No SERR# detected by the controller. 1 = The controller detects a SERR# on its interface.
29	0h RO	**Received Master Abort (RMA):** Hardwired to 0.
28	0h RO	**Received Target Abort (RTA):** Hardwired to 0.
27	0h RW/1C/V	**Signaled Target Abort (STA)**
26:25	0h RO	Reserved.
24	0h RO	**Master Data Parity Error (MDPE):** See the PCI spec.
23:22	0h RO	Reserved.
21	0h RO	**66 Mhz Capable (MCAP):** Hardwired to 0. Has no meaning on the HW.
20	0h RO	**Capablities List (CAPL):** Hardwired to 0 indicating that a Capabilities List is not present.
19	0h RO	**Interrupt Status (INTS):** Hardwired to 0.
18:11	0h RO	Reserved.
10	1h RO	**Interrupt Disable (INTD):** Hardwired to 1 br]0 = Interrupt is enabled1 = interrupt is disabled
9	0h RO	**Fast Back to Back Enable (FBTBEN):** Hardwired to 0.
8	0h RW	**System Error Enable (SERREN):** 0 = SERR# is disabled 1 = SERR# is Enabled
7	0h RO	Reserved.
6	0h RW	**Parity Error Response (PERRR):** Hardwired to 0. No response to parity errors from the controller.
5	0h RO	Reserved.
4	0h RO	**Memory Write and Invalidate Enable (MWRIEN):** Hardwired to 0. 0 = Disabled 1 = Enabled
3	0h RO	**Special Cycles (SPCYC):** Hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Bus Master Enable (BME):** 0 = Disabled 1 = Enabled
1	0h RW	**Memory Space Enable (MSE):** 0 = Disables memory mappedConfiguration space.1 = Enables memory mapped Configuration space.
0	0h RO	**IO Space Enable (IOSE):** 0 = Disabled 1 = Enabled

7.1.3 Revision ID and Class Code (BIOS_SPI_CC_RID)—Offset 8h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 31
Function: 5

Default: C8000XXh

Bit Range	Default & Access	Field Name (ID): Description
31:24	Ch RO	**Base Class Code (BCC):** Base Class Code
23:16	80h RO	**Sub-Class Code (SCC):** Sub-Class Code
15:8	0h RO	**Programming Interface (PI):** Programming Interface
7:0	0h RO/V	**Revision ID (RID):** Revision ID (RID): Indicates the part revision. Refer to the Device and Version ID Table in Volume 1 for the default value.

7.1.4 BIST, Header Type, Latency Timer, Cache Line Size (BIOS_SPI_BIST_HTYPE_LT_CLS)—Offset Ch

Access Method

Type: CFG Register (Size: 32 bits)

Device: 31
Function: 5

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:16	0h RO	**Header Type (HTYPE):** Implements Type 0 Configuration.
15:8	0h RO	**Latency Timer (LT):** Does not apply. Hardwired to 0.
7:0	0h RO	**Cacheline Size (CLSZ):** Does not apply. Hardwired to 0.

7.1.5 SPI BAR0 MMIO (BIOS_SPI_BAR0)—Offset 10h

Base Address for BAR0 - MMIO Registers

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Memory BAR (MEMBAR):** Software programs this register with the base address of the device's memory region. The Host/BIOS MMIO registers in the flash controller are offset from this BAR.
11:4	0h RO	**Memory Size (MEMSIZE):** Hardwired to 0 to indicate 4KB of memory space
3	0h RO	**Prefetchable (PREFETCH):** A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables. Hardwired to 1 to indicate the device's memory space as prefetchable.
2:1	0h RO	**Type (TYP):** Hardwired to 0 to indicate that Base register is 32 bits wide and mapping can be done anywhere in the 32-bit Memory Space.
0	0h RO	**Memory Space Indicator (MEMSPACE):** Hardwired to 0 to identify a Memory BAR.

7.1.6 SPI Unsupported Request Status (BIOS_SPI_UR_STS_CTL)—Offset D0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW/1C/V	**Unsupported Request Detected (URD):** Set to 1 by hardware upon detecting an Unspported Request that is not considered an Advisory Non-Fatal error. Cleared to 0 when software writes a 1 to this register.
0	0h RW	**Unsupported Request Reporting Enabled (URRE):** If set to 1 by software, the flash controller generates a DoSERR sideband message when the URD bit transitions from 0 to 1.

7.1.7 BIOS Decode Enable (BIOS_SPI_BDE)—Offset D8h

This register only effects BIOS decode if BIOS is resident on SPI.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 5

Default: FFCFh

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**BDE Lock Enable (BLE):** When this bit is set, the RW bits of this BDE register are locked down. Once set, this bit can only be cleared by PLTRST#.
30:16	0h RO	Reserved.
15	1h RO	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS ranges: FFF80000h - FFFFFFFFh FFB80000h - FFBFFFFFh
14	1h RW/L	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS ranges: FFF00000h - FFF7FFFFh FFB00000h - FFB7FFFFh
13	1h RW/L	**E8-EF Enable (EE8):** Enables decoding of 512K of the following BIOS ranges: FFE80000h - FFEFFFFFh FFA80000h - FFAFFFFFh
12	1h RW/L	**E0-E8 Enable (EE0):** Enables decoding of 512K of the following BIOS ranges: FFE00000h - FFE7FFFFh FFA00000h - FFA7FFFFh
11	1h RW/L	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS ranges: FFD80000h - FFDFFFFFh FF980000h - FF9FFFFFh
10	1h RW/L	**D0-D7 Enable (ED0):** Enables decoding of 512K of the following BIOS ranges: FFD00000h - FFD7FFFFh FF900000h - FF97FFFFh
9	1h RW/L	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS ranges: FFC80000h - FFCFFFFFh FF880000h - FF8FFFFFh
8	1h RW/L	**C0-C7 Enable (EC0):** Enables decoding of 512K of the following BIOS ranges: FFC00000h - FFC7FFFFh FF800000h - FF87FFFFh
7	1h RW/L	**Legacy F Segment Enable (LFE):** Legacy F Segment Enable (LFE): This enables the decoding of the legacy 64KB range at F0000h - FFFFFh

Bit Range	Default & Access	Field Name (ID): Description
6	1h RW/L	**Legacy E Segment Enable (LEE):** Legacy E Segment Enable (LFE): This enables the decoding of the legacy 64KB range at E0000h - EFFFFh
5:4	0h RO	Reserved.
3	1h RW/L	**70-7F Enable (E70):** Enables decoding of 1MB of the following BIOS ranges: FF700000h - FF7FFFFFh FF300000h - FF3FFFFFh
2	1h RW/L	**60-6F Enable (E60):** Enables decoding of 1MB of the following BIOS ranges: FF600000h - FF6FFFFFh FF200000h - FF2FFFFFh
1	1h RW/L	**50-5F Enable (E50):** Enables decoding of 1MB of the following BIOS ranges: FF500000h - FF5FFFFFh FF100000h - FF1FFFFFh
0	1h RW/L	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS ranges: FF400000h - FF4FFFFFh FF000000h - FF0FFFFFh

7.1.8 BIOS Control (BIOS_SPI_BC)—Offset DCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 5

Default: 28h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
11	0h RW/L	**Async SMI Enable for BIOS Write Protection (ASE_BWP):** When set to '1' the flash controller will generate an SMI when it blocks a BIOS write or erase due to WPD = 0. The value in this field can be written by software as long as the BIOS Interface Lock-Down (BILD) is not set.
10	0h RO/V	**Asynchronous SMI Status (SPI_ASYNC_SS):** Status indication that the SPI Flash Controller has asserted an asynchronous SMI. Hardware clears the bit when it sends the De-assert SMI message. 0 : default state 1 : SPI flash controller asserted asynchronous SMI
9	0h RO	Reserved.
8	0h RW/1C/V	**Synchronous SMI Status (SPI_SYNC_SS):** Status indication that the SPI Flash Controller has asserted a synchronous SMI. Hardware clears the bit when it sends the De-assert Synchronous SMI message. 0 : default state 1 : SPI flash controller asserted Synchronous SMI
7	0h RW/L	**BIOS Interface Lock-Down (BILD):** When set, prevents TS and BBS from being changed. This bit can only be written from 0 to 1 once.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/V/L	Boot BIOS Strap (BBS): This field determines the destination of accesses to the BIOS memory range. 0 = SPI 1 = eSPI When SPI or eSPI is selected, the range that is decoded is further qualified by BIOS Decode Enable. The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down (BILD) is not set
5	1h RW/L	**Enable InSMM.STS (EISS):** When this bit is set, the BIOS region is not writable until the CPU sets the InSMM.STS bit. If this bit [5] is set, then WPD must be a '1' and InSMM.STS(0xFED3_0880[0]) must be '1' also in order to write to BIOS region of SPI Flash. If this bit [5] is clear, then the InSMM.STS is a don't care. This bit is locked by LE.
4	0h RO/V	**Top Swap Status (TSS):** This bit provides a read-only path to view the state of the Top Swap bit. It is duplicated here to be consistent with the eSPI version of the BC register.
3:2	2h RW	**SPI Read Configuration (SRC):** These bits are located in PCI Config space to allow them to be set early in the boot flow. This 2-bit field controls two policies related to BIOS reads on the SPI interface: Bit 3- Prefetch Enable Bit 2- Cache Disable Settings are summarized below: 00 = No prefetching, but caching enabled. Direct Memory reads load the read buffer cache with valid data, allowing repeated reads to the same range to complete quickly 01 = No prefetching and no caching. One-to-one correspondence of host BIOS reads to SPI cycles. This value can be used to invalidate the cache. 10 = Prefetching and Caching enabled. This mode is used for long sequences of short reads to consecutive addresses (i.e. shadowing) 11 = unsupported. Caching must be enabled when Prefetching is enabled.
1	0h RW/L	**Lock Enable (LE):** When set, setting the WPD bit will cause SMI. When cleared, setting the WPD bit will not cause SMI. Once set, this bit can only be cleared by a PLTRST#. When this bit is set, EISS - bit [5] of this register is locked down.
0	0h RW	**Write Protect Disable (WPD):** When set, access to the BIOS space is enabled for both read and write cycles to BIOS. When cleared, only read cycles are permitted to the FWH or SPI flash. When this bit is written from a '0' to a '1' and the LE bit is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

7.2 SPI Memory Mapped Registers Summary

The SPI memory mapped registers are accessed based upon offsets from SPI_BAR0 (in PCI config SPI_BAR0 register).

Table 7-2. Summary of SPI Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	BIOS Flash Primary Region (BIOS_BFPREG)—Offset 0h	0h
4h	7h	Hardware Sequencing Flash Status and Control (BIOS_HSFSTS_CTL)—Offset 4h	2000h
8h	Bh	Flash Address (BIOS_FADDR)—Offset 8h	0h
Ch	Fh	Discrete Lock Bits (BIOS_DLOCK)—Offset Ch	0h
10h	13h	Flash Data 0 (BIOS_FDATA0)—Offset 10h	0h
14h	17h	Flash Data 1 (BIOS_FDATA1)—Offset 14h	0h
18h	1Bh	Flash Data 2 (BIOS_FDATA2)—Offset 18h	0h
1Ch	1Fh	Flash Data 3 (BIOS_FDATA3)—Offset 1Ch	0h
20h	23h	Flash Data 4 (BIOS_FDATA4)—Offset 20h	0h
24h	27h	Flash Data 5 (BIOS_FDATA5)—Offset 24h	0h
28h	2Bh	Flash Data 6 (BIOS_FDATA6)—Offset 28h	0h
2Ch	2Fh	Flash Data 7 (BIOS_FDATA7)—Offset 2Ch	0h
30h	33h	Flash Data 8 (BIOS_FDATA8)—Offset 30h	0h
34h	37h	Flash Data 9 (BIOS_FDATA9)—Offset 34h	0h
38h	3Bh	Flash Data 10 (BIOS_FDATA10)—Offset 38h	0h
3Ch	3Fh	Flash Data 11 (BIOS_FDATA11)—Offset 3Ch	0h
40h	43h	Flash Data 12 (BIOS_FDATA12)—Offset 40h	0h
44h	47h	Flash Data 13 (BIOS_FDATA13)—Offset 44h	0h
48h	4Bh	Flash Data 14 (BIOS_FDATA14)—Offset 48h	0h
4Ch	4Fh	Flash Data 15 (BIOS_FDATA15)—Offset 4Ch	0h
50h	53h	Flash Region Access Permissions (BIOS_FRACC)—Offset 50h	42C2h
54h	57h	Flash Region 0 (BIOS_FREG0)—Offset 54h	0h
58h	5Bh	Flash Region 1 (BIOS_FREG1)—Offset 58h	7FFFh
5Ch	5Fh	Flash Region 2 (BIOS_FREG2)—Offset 5Ch	7FFFh
60h	63h	Flash Region 3 (BIOS_FREG3)—Offset 60h	7FFFh
64h	67h	Flash Region 4 (BIOS_FREG4)—Offset 64h	7FFFh
68h	6Bh	Flash Region 5 (BIOS_FREG5)—Offset 68h	7FFFh
84h	87h	Flash Protected Range 0 (BIOS_FPR0)—Offset 84h	0h
88h	8Bh	Flash Protected Range 1 (BIOS_FPR1)—Offset 88h	0h
8Ch	8Fh	Flash Protected Range 2 (BIOS_FPR2)—Offset 8Ch	0h
90h	93h	Flash Protected Range 3 (BIOS_FPR3)—Offset 90h	0h
94h	97h	Flash Protected Range 4 (BIOS_FPR4)—Offset 94h	0h
98h	9Bh	Global Protected Range 0 (BIOS_GPR0)—Offset 98h	0h
B0h	B3h	Secondary Flash Region Access Permissions (BIOS_SFRACC)—Offset B0h	0h
B4h	B7h	Flash Descriptor Observability Control (BIOS_FDOC)—Offset B4h	0h
B8h	BBh	Flash Descriptor Observability Data (BIOS_FDOD)—Offset B8h	0h
C0h	C3h	Additional Flash Control (BIOS_AFC)—Offset C0h	0h
C4h	C7h	Vendor Specific Component Capabilities for Component 0 (BIOS_SFDP0_VSCC0)—Offset C4h	2000h

Table 7-2. Summary of SPI Memory Mapped Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C8h	CBh	Vendor Specific Component Capabilities for Component 1 (BIOS_SFDP1_VSCC1)—Offset C8h	2000h
CCh	CFh	Parameter Table Index (BIOS_PTINX)—Offset CCh	0h
D0h	D3h	Parameter Table Data (BIOS_PTDATA)—Offset D0h	0h
D4h	D7h	SPI Bus Requester Status (BIOS_SBRS)—Offset D4h	0h

7.2.1 BIOS Flash Primary Region (BIOS_BFPREG)—Offset 0h

BIOS Flash Primary Region

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**BIOS Flash Primary Region Limit (PRL):** This specifies address bits 26:12 for the Primary Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit, or the Flash Descriptor.FLREG6.Region Limit depending on the BFPREG.SBRS bit.
15	0h RO	Reserved.
14:0	0h RO/V	**BIOS Flash Primary Region Base (PRB):** This specifies address bits 26:12 for the Primary Region Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base, or the Flash Descriptor.FLREG6.Region Base depending on the BFPREG.SBRS bit.

7.2.2 Hardware Sequencing Flash Status and Control (BIOS_HSFSTS_CTL)—Offset 4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2000h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**Flash SPI SMI# Enable (FSMIE):** When set to 1, the SPI asserts an SMI# request whenever the Flash Cycle Done bit is 1.
30	0h RO	Reserved.
29:24	0h RW	**Flash Data Byte Count (FDBC):** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The contents of this register are 0s based with 0b representing 1 byte and 3Fh representing 64 bytes. The number of bytes transferred is the value of this field plus 1. This field is ignored for the Block Erase command.
23:22	0h RO	Reserved.
21	0h RW	**Write Enable Type (WET):** 0: Use 06h as the write enable instruction 1: Use 50h as the write enable instruction. Note that this setting is not supported as no supported flash devices require the 50h opcode to enable a non-volatile status register write.
20:17	0h RW	**Flash Cycle (FCYCLE):** This field defines the Flash SPI cycle type generated to the FLASH when the FGO bit is set as defined below: 0 Read (1 up to 64 bytes by setting FDBC) 1 Reserved 2 Write (1 up to 64 bytes by setting FDBC) 3 4k Block Erase 4 64k Sector erase 5 Read SFDP 6 Read JEDEC ID 7 write status 8 read status 9 RPMC Op1 A RPMC Op2 Flash controller hardware automatically inserts a write enable opcode prior to Write and erase operations. Hardware automatically polls for device not-busy using read status after write and erase operations. If the device does not support 64k erase size (or if it does not support SFDP) then only 4k is allowed. Note: if reserved 1 is programmed to this field, flash controller will handle it as if it is 0 (Read)
16	0h RW/1S/V	**Flash Cycle Go (FGO):** A write to this register with a 1 in this bit initiates a request to the Flash SPI Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the SPI arbiter to run the cycle on the SPI bus. When the cycle is complete, the FDONE bit is set. Software is forbidden to write to any register in the HSFLCTL register between the FGO bit getting set and the FDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit always returns 0 on reads.
15	0h RW/L	**Flash Configuration Lock-Down (FLOCKDN):** When set to 1, those Flash Program Registers that are locked down by this FLOCKDN bit cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
14	0h RO/V	**Flash Descriptor Valid (FDV):** This bit is set to a 1 if the Flash Controller read the correct Flash Descriptor Signature. If the Flash Descriptor Valid bit is not 1 , software cannot use the Hardware Sequencing registers, but must use the software sequencing registers. Any attempt to use the Hardware Sequencing registers will result in the FCERR bit being set
13	1h RO/V	**Flash Descriptor Override Pin-Strap Status (FDOPSS):** This register reflects the value the Flash Descriptor Override Pin-Strap. '1': No override '0': The Flash Descriptor Override strap is set
12	0h RW/L	**PRR3 PRR4 Lock-Down (PRR34_LOCKDN):** When set to 1, the BIOS PRR3 and PRR4 registers cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
11	0h RW/L	**Write Status Disable (WRSDIS):** 0 = Write status operation may be issued using Hardware Sequencing. 1 = Write status is not allowed as a Hardware Sequencing operation. The flash controller will block the operation and set the FCERR bit when software sets the 'go' bit. This bit is locked when FLOCKDN is set.
10:6	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
5	0h RO/V	**SPI Cycle In Progress (H_SCIP):** Hardware sets this bit when software sets the Flash Cycle Go (FGO) bit in the Hardware Sequencing Flash Control register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.
4:3	0h RO	Reserved.
2	0h RW/1C/V	**Access Error Log (H_AEL):** Hardware sets this bit to a 1 when an attempt was made to access the BIOS region using the direct access method or an access to the BIOS Program Registers that violated the security restrictions. This bit is simply a log of an access security violation. This bit is cleared by software writing a '1'.
1	0h RW/1C/V	**Flash Cycle Error (FCERR):** Hardware sets this bit to 1 when a program register access is blocked to the FLASH due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or until hardware reset occurs. Software must clear this bit before setting the FLASH Cycle GO bit in this register.
0	0h RW/1C/V	**Flash Cycle Done (FDONE):** The PCH sets this bit to 1 when the SPI Cycle completes after software previously set the FGO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.

7.2.3 Flash Address (BIOS_FADDR)—Offset 8h

Flash Address

Access Method

Type: MEM Register (Size: 32 bits)

Device:

Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26:0	0h RW	**Flash Linear Address (FLA):** The FLA is the starting byte linear address of a SPI Read or Write cycle or an address within a Block for the Block Erase command. The Flash Linear Address must fall within a region for which BIOS has access permissions. Hardware must convert the FLA into a Flash Physical Address (FPA) before running this cycle on the SPI bus.

7.2.4 Discrete Lock Bits (BIOS_DLOCK)—Offset Ch

Lockable BIOS registers may be locked by either the global FLOCKDN bit or by the individual DLOCK bit. Each lockable bit in this register is locked either by itself or by the FLOCKDN bit.

Access Method

Type: MEM Register (Size: 32 bits)

Device:

Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW/L	**SSEQ Lock-Down (SSEQLOCKDN):** BIOS Software Sequencing registers are locked when the logical OR of this bit and FLOCKDN is true. The affected registers are SSFSTS_CTL.SCF, PREOP_OPTYPE, OPMENU0, and OPMENU1. Once set to 1 this register is only cleared by host partition reset.
15	0h RW/L	**Spare1 (SPARE1):** Once set to 1 this register is only cleared by host partition reset.
14	0h RW/L	**Spare2 (SPARE2):** Once set to 1 this register is only cleared by host partition reset.
13	0h RW/L	**Spare3 (SPARE3):** Once set to 1 this register is only cleared by host partition reset.
12	0h RW/L	**PR4 Lock-Down (PR4LOCKDN):** BIOS PR4 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset.
11	0h RW/L	**PR3 Lock-Down (PR3LOCKDN):** BIOS PR3 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset.
10	0h RW/L	**PR2 Lock-Down (PR2LOCKDN):** BIOS PR2 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset.
9	0h RW/L	**PR1 Lock-Down (PR1LOCKDN):** BIOS PR1 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset.
8	0h RW/L	**PR0 Lock-Down (PR0LOCKDN):** BIOS PR0 register is locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by BIOS partition reset.
7	0h RW/L	**Spare4 (SPARE4):** Once set to 1 this register is only cleared by host partition reset.
6	0h RW/L	**Spare5 (SPARE5):** Once set to 1 this register is only cleared by host partition reset.
5	0h RW/L	**Spare6 (SPARE6):** Once set to 1 this register is only cleared by host partition reset.
4	0h RW/L	**Spare7 (SPARE7):** Once set to 1 this register is only cleared by host partition reset.
3	0h RW/L	**SBMRAG Lock-Down (SBMRAGLOCKDN):** BIOS SFRACC.BMRAG register bits are locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by host partition reset.
2	0h RW/L	**SBMWAG Lock-Down (SBMWAGLOCKDN):** BIOS SFRACC.BMWAG register bits are locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by host partition reset.
1	0h RW/L	**BMRAG Lock-Down (BMRAGLOCKDN):** BIOS FRACC.BMRAG register bits are locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by host partition reset.
0	0h RW/L	**BMWAG Lock-Down (BMWAGLOCKDN):** BIOS FRACC.BMWAG register bits are locked when the logical OR of this bit and FLOCKDN is true. Once set to 1 this register is only cleared by host partition reset.

7.2.5 Flash Data 0 (BIOS_FDATA0)—Offset 10h

Flash Data 0

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 0 (FD0):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13-...8-23-22-...16-31...24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

7.2.6 Flash Data 1 (BIOS_FDATA1)—Offset 14h

Flash Data 1

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 1 (FD1):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD0 has completely shifted in/out.

7.2.7 Flash Data 2 (BIOS_FDATA2)—Offset 18h

Flash Data 2

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 2 (FD2):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD1 has completely shifted in/out.

7.2.8 Flash Data 3 (BIOS_FDATA3)—Offset 1Ch

Flash Data 3

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 3 (FD3):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD2 has completely shifted in/out.

7.2.9 Flash Data 4 (BIOS_FDATA4)—Offset 20h

Flash Data 4

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 4 (FD4):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD3 has completely shifted in/out.

7.2.10 Flash Data 5 (BIOS_FDATA5)—Offset 24h

Flash Data 5

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 5 (FD5):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD4 has completely shifted in/out.

7.2.11 Flash Data 6 (BIOS_FDATA6)—Offset 28h

Flash Data 6

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 6 (FD6):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD5 has completely shifted in/out.

7.2.12 Flash Data 7 (BIOS_FDATA7)—Offset 2Ch

Flash Data 7

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 7 (FD7):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD6 has completely shifted in/out.

7.2.13 Flash Data 8 (BIOS_FDATA8)—Offset 30h

Flash Data 8

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 8 (FD8):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD7 has completely shifted in/out.

7.2.14 Flash Data 9 (BIOS_FDATA9)—Offset 34h

Flash Data 9

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 9 (FD9):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD8 has completely shifted in/out.

7.2.15 Flash Data 10 (BIOS_FDATA10)—Offset 38h

Flash Data 10

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 10 (FD10):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD9 has completely shifted in/out.

7.2.16 Flash Data 11 (BIOS_FDATA11)—Offset 3Ch

Flash Data 11

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 11 (FD11):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD10 has completely shifted in/out.

7.2.17 Flash Data 12 (BIOS_FDATA12)—Offset 40h

Flash Data 12

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 12 (FD12):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD11 has completely shifted in/out.

7.2.18 Flash Data 13 (BIOS_FDATA13)—Offset 44h

Flash Data 13

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 13 (FD13):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD12 has completely shifted in/out.

7.2.19 Flash Data 14 (BIOS_FDATA14)—Offset 48h

Flash Data 14

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 14 (FD14):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD13 has completely shifted in/out.

7.2.20 Flash Data 15 (BIOS_FDATA15)—Offset 4Ch

Flash Data 15

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Flash Data 15 (FD15):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD14 has completely shifted in/out.

7.2.21 Flash Region Access Permissions (BIOS_FRACC)—Offset 50h

Flash Region Access Permissions

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 42C2h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RW/L	**BIOS Master Write Access Grant (BMWAG):** BIOS Master Write Access Grant (BMWAG): Each bit [31:24] corresponds to Master[7:0]. BIOS can grant one or more masters write access to the BIOS region 1 overriding the permissions in the Flash Descriptor. The contents of this register are locked by the FLOCKDN bit.

Bit Range	Default and Access	Field Name (ID): Description
23:16	0h RW/L	**BIOS Master Read Access Grant (BMRAG):** BIOS Master Read Access Grant (BMRAG): Each bit [23:16] corresponds to Master[7:0]. BIOS can grant one or more masters read access to the BIOS region 1 overriding the read permissions in the Flash Descriptor. The contents of this register are locked by the FLOCKDN bit
15:8	42h RO/V	**BIOS Region Write Access (BRWA):** BIOS Region Write Access (BRWA): Each bit [15:8] corresponds to Regions [7:0]. If the bit is set, this master can erase and write that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS write permissions in their Master Write Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS always have the write access to its own Region 1 and Region 6 by default.
7:0	C2h RO/V	**BIOS Region Read Access (BRRA):** BIOS Region Read Access (BRRA): Each bit [7:0] corresponds to Regions [7:0]. If the bit is set, this master can read that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS read permissions in their Master Read Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS always have the read access to its own Region 1 and Region 6 by default.

7.2.22 Flash Region 0 (BIOS_FREG0)—Offset 54h

Flash Region 0

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region 0 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Limit.
15	0h RO	Reserved.
14:0	0h RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region 0 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Base.

7.2.23 Flash Region 1 (BIOS_FREG1)—Offset 58h

Flash Region 1

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 7FFFh

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region 1 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit.
15	0h RO	Reserved.
14:0	7FFFh RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region 1 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base.

7.2.24 Flash Region 2 (BIOS_FREG2)—Offset 5Ch

Flash Region 2

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 7FFFh

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region 2 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Limit.
15	0h RO	Reserved.
14:0	7FFFh RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region 2 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Base.

7.2.25 Flash Region 3 (BIOS_FREG3)—Offset 60h

Flash Region 3

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 7FFFh

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region 3 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Limit.
15	0h RO	Reserved.
14:0	7FFFh RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region 3 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base.

7.2.26 Flash Region 4 (BIOS_FREG4)—Offset 64h

Flash Region 4

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 7FFFh

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region 4 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Limit.
15	0h RO	Reserved.
14:0	7FFFh RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region 4 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Base.

7.2.27 Flash Region 5 (BIOS_FREG5)—Offset 68h

Flash Region 5

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 7FFFh

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	Reserved.
30:16	0h RO/V	**Region Limit (RL):** This specifies address bits 26:12 for the Region 5 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG5.Region Limit.
15	0h RO	Reserved.
14:0	7FFFh RO/V	**Region Base (RB):** This specifies address bits 26:12 for the Region 5 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG5.Region Base.

7.2.28 Flash Protected Range 0 (BIOS_FPR0)—Offset 84h

This register cannot be written when the FLOCKDN bit is set to 1.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

7.2.29 Flash Protected Range 1 (BIOS_FPR1)—Offset 88h

This register cannot be written when the FLOCKDN bit is set to 1.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

7.2.30 Flash Protected Range 2 (BIOS_FPR2)—Offset 8Ch

This register cannot be written when the FLOCKDN bit is set to 1.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

7.2.31 Flash Protected Range 3 (BIOS_FPR3)—Offset 90h

This register cannot be written when the PRR34_LOCKDN bit is set to 1

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

7.2.32 Flash Protected Range 4 (BIOS_FPR4)—Offset 94h

This register cannot be written when the PRR34_LOCKDN bit is set to 1

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0h RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

7.2.33 Global Protected Range 0 (BIOS_GPR0)—Offset 98h

This register is initialized via softstraps. This protected range applies globally to all masters / flash requesters.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO/V	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:16	0h RO/V	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 26:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. Note: If either Write or Read protection is enabled, then Limit must be configured greater than or equal to Base.
15	0h RO/V	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:0	0h RO/V	**Protected Range Base (PRB):** This field corresponds to FLA address bits 26:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. Note: If either Write or Read protection is enabled, then Limit must be configured greater than or equal to Base.

7.2.34 Secondary Flash Region Access Permissions (BIOS_SFRACC)—Offset B0h

Secondary Flash Region Access Permissions

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RW/L	**Secondary BIOS Master Write Access Grant (SECONDARYBIOS_MWAG):** Each bit 31:29 corresponds to Master7:0. BIOS can grant one or more masters write access to the Secondary BIOS region 6 overriding the permissions in the Flash Descriptor. Bits for unassigned masters are reserved. The contents of this register are locked by the FLOCKDN bit.
23:16	0h RW/L	**Secondary BIOS Master Read Access Grant (SECONDARYBIOS_MRAG):** Each bit 28:16 corresponds to Master7:0. BIOS can grant one or more masters read access to the Secondary BIOS region 6 overriding the read permissions in the Flash Descriptor. Bits for unassigned masters are reserved. The contents of this register are locked by the FLOCKDN bit.
15:0	0h RO	Reserved.

7.2.35 Flash Descriptor Observability Control (BIOS_FDOC)—Offset B4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:12	0h RW	**Flash Descriptor Section Select (FDSS):** Selects which section within the loaded Flash Descriptor to observe. 000: Flash Signature and Descriptor Map 001: Component 010: Region 011: Master Others: Reserved
11:2	0h RW	**Flash Descriptor Section Index (FDSI):** Selects the DW offset within the Flash Descriptor Section to observe.
1:0	0h RO	Reserved.

7.2.36 Flash Descriptor Observability Data (BIOS_FDOD)—Offset B8h

Flash Descriptor Observability Data

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Flash Descriptor Section Data (FDSD):** Returns the DW of data to observe as selected in the Flash Descriptor Observability Control.

7.2.37 Additional Flash Control (BIOS_AFC)—Offset C0h

Additional Flash Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/V/P	**Stop Prefetch on Flush Pending (SPFP):** When set to 1, the in progress of a prefetch will be ended if subsequence access from the master of the same interface is detected to be a cache-miss and read cache will be flushed. When set to 0, the prefetch will be allowed to complete prior to flushing.

7.2.38 Vendor Specific Component Capabilities for Component 0 (BIOS_SFDP0_VSCC0)—Offset C4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2000h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO/V	**Component Property Parameter Table Valid (CPPTV):** This bit is set to a 1 if the Flash Controller detects a valid SFDP Component Property Parameter Table in Component 0. Note: If this bit is set software must not overwrite bits that were initialized by hardware via SFDP discovery.
30	0h RW/L	**Vendor Component Lock (VCL):** 0: The lock bit is not set 1: The Vendor Component Lock bit is set. This register locks itself when set.
29	0h RW/V/L	**64k Erase Valid (EO_64K_VALID):** 0: The EO_64k opcode is not valid. 1: The EO_64k opcode is valid.
28	0h RW/V/L	**4k Erase Valid (EO_4K_VALID):** 0: The EO_4k opcode is not valid. 1: The EO_4k opcode is valid.
27	0h RW/L	**RPMC Supported (RPMC_SUPPORTED):** 0: The device does not support RPMC. 1: The device supports RPMC.
26	0h RW/V/L	**Deep Powerdown Supported (DEEP_PWRDN_SUPPORTED):** 0: The device does not support Deep Powerdown. 1: The device supports Deep Powerdown.
25	0h RW/V/L	**Suspend/Resume Supported (SUSPEND_RESUME_SUPPORTED):** 1: The device does not support Suspend/Resume. 0: The device supports Suspend/Resume.
24	0h RW/V/L	**Soft Reset Supported (SOFT_RST_SUPPORTED):** 0: The device does not support Soft Reset. 1: The device supports Soft Reset.
23:16	0h RW/V/L	**64k Erase Opcode (EO_64K):** This register is programmed with the Flash 64k sector erase instruction opcode for component 0. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
15:8	20h RW/V/L	**4k Erase Opcode (EO_4K):** This register is programmed with the Flash 64k sector erase instruction opcode for component 0. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
7:5	0h RW/V/L	**Quad Enable Requirements (QER):** 000 = Part does not require a Quad Enable bit to be set, either because Quad is not supported or because the manufacturer somehow permanently enables Quad capability. 001 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to status register clears all bits in register 2, therefore status register writes MUST be two bytes. 010 = Part requires bit 6 of status register 1 to be set to enable quad IO. 011 = Part requires bit 7 of the configuration register to be set to enable Quad. 100 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to the status register does not clear the second byte. This register is locked by the Vendor Component Lock (VCL) bit. If the SFDP table contains this information, the flash controller loads these bits from the table. The flash controller uses this information to prevent clearing the QE bit in the flash device's status register when WSR=1.
4	0h RW/V/L	**Write Enable on Write Status (WEWS):** 0 = 50h is the opcode to enable a status register write 1 : 06h is the opcode to enable a status register write This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. Note: Hardware ignores the state of this bit.

Bit Range	Default and Access	Field Name (ID): Description
3	0h RW/V/L	**Write Status Required (WSR):** 0 = No requirement to write to the Write Status Register prior to a write 1 = A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. Note: Hardware ignores the state of this bit.
2	0h RW/V/L	**Write Granularity (WG):** 0 : Reserved 1 : 64 Byte This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit. Note: Hardware ignores the state of this bit.
1:0	0h RO	Reserved.

7.2.39 Vendor Specific Component Capabilities for Component 1 (BIOS_SFDP1_VSCC1)—Offset C8h

This register pertain to cycles targeting addresses outside of Component 0. The lockable bits in this register are locked when either CPPTV is set to 1 by hardware or when VCL is 1.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2000h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO/V	**Component Property Parameter Table Valid (CPPTV):** This bit is set to a 1 if the Flash Controller detects a valid SFDP Component Property Parameter Table in Component 1. Note: If this bit is set software must not overwrite bits that were initialized by hardware via SFDP discovery RO
30	0h RO	Reserved.
29	0h RW/V/L	**64k Erase Valid (EO_64K_VALID):** 0: The EO_64k opcode is not valid. 1: The EO_64k opcode is valid.
28	0h RW/V/L	**4k Erase Valid (EO_4K_VALID):** 0: The EO_4k opcode is not valid. 1: The EO_4k opcode is valid.
27	0h RW/L	**RPMC Supported (RPMC_SUPPORTED):** 0 The device does not support RPMC. 1 The device supports RPMC.
26	0h RW/V/L	**Deep Powerdown Supported (DEEP_PWRDN_SUPPORTED):** 0 The device does not support Deep Powerdown. 1 The device supports Deep Powerdown.
25	0h RW/V/L	**Suspend/Resume Supported (SUSPEND_RESUME_SUPPORTED):** 1 the device supports Suspend/Resume
24	0h RW/V/L	**Soft Reset Supported (SOFT_RST_SUPPORTED):** 0: The device does not support Soft Reset. 1: The device supports Soft Reset.
23:16	0h RW/V/L	**64k Erase Opcode (EO_64K):** This register is programmed with the Flash 64k sector erase instruction opcode for component 1. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.

Bit Range	Default and Access	Field Name (ID): Description
15:8	20h RW/V/L	**4k Erase Opcode (EO_4K):** This register is programmed with the Flash 4k subsector erase instruction opcode for component 1. Software must program this register if the SFDP table for this component does not show 4 kByte erase capability. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
7:5	0h RW/V/L	**Quad Enable Requirements (QER):** 000 = Part does not require a Quad Enable bit to be set, either because Quad is not supported or because the manufacturer somehow permanently enables Quad capability. 001 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to status register clears all bits in register 2, therefore status register writes MUST be two bytes. 010 = Part requires bit 6 of status register 1 to be set to enable quad IO. 011 = Part requires bit 7 of the configuration register to be set to enable Quad. 100 = Part requires bit 9 in status register 2 to be set to enable quad IO. Writing one byte to the status register does not clear the second byte. This register is locked by the Vendor Component Lock (VCL) bit. If the SFDP table contains this information, the flash controller loads these bits from the table. The flash controller uses this information to prevent clearing the QE bit in the flash device's status register when WSR=1.
4	0h RW/V/L	**Write Enable on Write Status (WEWS):** 0 : 50h is the opcode to enable a status register write 1 : 06h is the opcode to enable a status register write This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
3	0h RW/V/L	**Write Status Required (WSR):** 0: No requirement to write to the Write Status Register prior to a write 1: A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This register is locked by the Vendor Component Lock (VCL) bit or the CPPTV bit.
2	0h RW/V/L	**Write Granularity (WG):** 0 : Reserved 1 : 64 Byte This register is locked by the Vendor Component Lock (VCL) bit orthe CPPTV bit. Note: Hardware ignores the state of this bit.
1:0	0h RO	Reserved.

7.2.40 Parameter Table Index (BIOS_PTINX)—Offset CCh

Observability control for Component Property Tables. Note: The PTINX and PTDATA registers do not have any meaning in slave-attach flash mode because the SPI controller does not perform SFDP discovery.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:14	0h RW	**Supported Parameter Table (SPT):** Selects which supported parameter table to observe. 00 : Component 0 Property Parameter Table 01 : Component 1 Property Parameter Table 10 - 11 : Reserved

Bit Range	Default and Access	Field Name (ID): Description
13:12	0h RW	**Header or Data (HORD):** Select parameter table header DW vs Data DW. 00 : SFDP Header 01 : Parameter Table Header 10 : Data 11 : Reserved
11:2	0h RW	**Parameter Table DW Index (PTDWI):** Selects the DW offset within the parameter table to observe.
1:0	0h RO	Reserved.

7.2.41 Parameter Table Data (BIOS_PTDATA)—Offset D0h

Parameter Table Data

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Parameter Table DW Data (PTDWD):** Returns the DW of data to observe as selected in the Parameter Table Index register. Note: The returned value of reserved fields in the SFDP header or table must be ignored by software. The flash controller may return either 0 or 1 for these fields.

7.2.42 SPI Bus Requester Status (BIOS_SBRS)—Offset D4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO/V	**TPM Access Ongoing (TPM_ACC_ONG):** Indicates that a TPM access is in progress.
30	0h RO/V	**eSPI Access Ongoing (ESPI_ACC_ONG):** This bit is only defined if eSPI and SPI are sharing the SPI bus.
29:18	0h RO	Reserved.
17:15	0h RO/V	**Master 5 Status (M5STATUS):** Refer description under M1STATUS.
14:12	0h RO/V	**Master 6 Status (M6STATUS):** Refer description under M1STATUS.

Bit Range	Default and Access	Field Name (ID): Description
11:9	0h RO/V	**Master 4 Status (M4STATUS):** Refer description under M1STATUS.
8:6	0h RO/V	**Master 3 Status (M3STATUS):** Refer description under M1STATUS.
5:3	0h RO/V	**Master 2 Status (M2STATUS):** Refer description under M1STATUS.
2:0	0h RO/V	**Master 1 Status (M1STATUS):** Indicates whether this master has an outstanding transaction enqueued or in flight and the transaction type. 0xx : no transaction 100 : flash read transaction 101 : flash write transaction 110 : flash erase transaction 111 : flash RPMC transaction

8 Integrated GbE (D31:F6)

8.1 GbE Configuration Registers Summary

Table 8-1. Summary of GbE Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	GbE Vendor and Device Identification Register (GBE_VID_DID)—Offset 0h	15B78086h
4h	7h	PCI Command & Status Register (PCICMD_STS)—Offset 4h	100000h
8h	Bh	Revision Identification & Class Code Register (RID_CC)—Offset 8h	20000XXh
Ch	Fh	Cache Line Size Primary Latency Timer & Header Type Register (CLS_PLT_HEADTYP)—Offset Ch	0h
10h	13h	Memory Base Address Register A (MBARA)—Offset 10h	0h
2Ch	2Fh	Subsystem Vendor & Subsytem ID (DMI_CONFIG11)—Offset 2Ch	8086h
30h	33h	Expansion ROM Base Address Register (ERBA)—Offset 30h	0h
34h	37h	Capabilities List Pointer Register (CAPP)—Offset 34h	C8h
3Ch	3Fh	Interrupt Information & Maximum Latency/Minimum GrantRegister (INTR_MLMG)—Offset 3Ch	100h
A0h	A3h	LAN Disable Control (LANDISCTRL)—Offset A0h	0h
A4h	A7h	Lock LAN Disable (LOCKLANDIS)—Offset A4h	0h
A8h	ABh	System Time Control High Register (LTRCAP)—Offset A8h	0h
C8h	CBh	Capabilities List and Power Managment Capabilities Register (CLIST1_PMC)—Offset C8h	23D001h
CCh	CFh	PCI Power Management Control Status & Data Register (PMCS_DR)—Offset CCh	0h
D0h	D3h	Capabilities List 2 & Message Control Register (CLIST2_MCTL)—Offset D0h	80E005h
D4h	D7h	Message Address Low Register (MADDL)—Offset D4h	0h
D8h	DBh	Message Address High Register (MADDH)—Offset D8h	0h
DCh	DFh	Message Data Register (MDAT)—Offset DCh	0h

8.1.1 GbE Vendor and Device Identification Register (GBE_VID_DID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 15B78086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	15B7h RW/V	**Device ID (DID):** This is a 16-bit value assigned to the PCH Gigabit LAN controller. The field may be auto-loaded from the NVM word 0Dh during initialization time depending on the "Load Vendor/ Device ID" bit field in NVM word 0Ah.
15:0	8086h RO/V	**Vendor ID (VID):** This is a 16-bit value assigned to Intel. The field may be auto-loaded from the NVM at address 0Dh during INIT time depending on the "Load Vendor/Device ID" bit field in NVM word 0Ah with a default value of 8086h.

8.1.2 PCI Command & Status Register (PCICMD_STS)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Detected Parity Error (DPE):** 0 = No parity error detected. 1 = Set when the Gb LAN controller receives a command or data from the backbone with a parity error. This is set even if PCIMD.PER (D25:F0, bit 6) is not set.
30	0h RW/V	**Signaled System Error (SSE):** 0 = No system error signaled. 1 = Set when the Gb LAN controller signals a system error to the internal SERR# logic.
29	0h RW/V	**Received Master Abort (RMA):** 0 = Root port has not received a completion with unsupported request status from the backbone. 1 = Set when the GbE LAN controller receives a completion with unsupported request status from the backbone.
28	0h RW/V	**Received Target Abort (RTA):** 0 = Root port has not received a completion with completer abort from the backbone. 1 = Set when the Gb LAN controller receives a completion with completer abort from the backbone.
27	0h RW/V	**Signaled Target Abort (STA):** 0 = No target abort received. 1 = Set whenever the Gb LAN controller forwards a target abort received from the downstream device onto the backbone.
26:25	0h RW/V	**DEVSEL# Timing Status (DEV_STS):** Hardwired to 0.
24	0h RW/V	**Master Data Parity Error Detected (DPED):** 0 = No data parity error received. 1 = Set when the Gb LAN Controller receives a completion with a data parity error on the backbone and PCIMD.PER (D25:F0, bit 6) is set.
23	0h RW/V	**Fast Back to Back Capable (FB2BC):** Hardwired to 0.
22	0h RO	Reserved.
21	0h RW/V	**66 MHz Capable (MHZ_66_CPBL):** Hardwired to 0.
20	1h RW/V	**Capabilities List (NEW_CPBL):** Hardwired to 1. Indicates the presence of a capabilities list.
19	0h RW/V	**Interrupt Status (INT_STAT):** Indicates status of hot-plug and power management interrupts on the root port that result in INTx# message generation. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of PCICMD.Interrupt Disable bit (D25:F0:04h:bit 10).

Bit Range	Default & Access	Field Name (ID): Description
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INT_DIS):** This disables pin-based INTx# interrupts on enabled hot-plug and power management events. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt for hot-plug or power management and MSI is not enabled. 1 = Internal INTx# messages will not be generated. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and de-assert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set.
9	0h RW/V	**Fast Back to Back Enable (FBE):** Hardwired to 0.
8	0h RW	**SERR# Enable (SEE):** 0 = Disable 1 = Enables the Gb LAN controller to generate an SERR# message when PSTS.SSE is set.
7	0h RW/V	**Wait Cycle Control (WCC):** Hardwired to 0.
6	0h RW	**Parity Error Response (PER):** 0 = Disable. 1 = Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0h RW/V	**Palette Snoop Enable (PSE):** Hardwired to 0.
4	0h RW/V	**Postable Memory Write Enable (PMWE):** Hardwired to 0.
3	0h RW/V	**Special Cycle Enable (SCE):** Hardwired to 0.
2	0h RW	**Bus Master Enable (BME):** 0 = Disable. All cycles from the device are master aborted 1 = Enable. Allows the root port to forward cycles onto the backbone from a Gigabit LAN device.
1	0h RW	**Memory Space Enable (MSE):** 0 = Disable. Memory cycles within the range specified by the memory base and limit registers are master aborted on the backbone. 1 = Enable. Allows memory cycles within the range specified by the memory base and limit registers can be forwarded to the Gigabit LAN device.
0	0h RW/V	**I/O Space Enable (IOSE):** This bit controls access to the I/O space registers. 0 = Disable. I/O cycles within the range specified by the I/O base and limit registers are master aborted on the backbone. 1 = Enable. Allows I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the Gigabit LAN device.

8.1.3 Revision Identification & Class Code Register (RID_CC)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 2000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	20000h RW/V	**Class Code (Class_Code):** Identifies the device as an Ethernet Adapter. 020000h = Ethernet Adapter.
7:0	0h RW/V	**Revision ID (REV_ID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

8.1.4 Cache Line Size Primary Latency Timer & Header Type Register (CLS_PLT_HEADTYP)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	0h RW/V	**Header Type (HT):** 00h = Indicates this is a single function device.
15:8	0h RW/V	**Latency Timer (LT):** Hardwired to 0.
7:0	0h RW/V	**Cache Line Size (CLS):** This field is implemented by PCI devices as a read/write field for legacy compatibility purposes but has no impact on any device functionality.

8.1.5 Memory Base Address Register A (MBARA)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RW	**Base Address (BA):** Software programs this field with the base address of this region.
16:4	0h RW/V	**Memory Size (MSIZE):** Memory size is 128KB.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/V	**Prefetchable Memory (PM):** The GbE LAN controller does not implement prefetchable memory.
2:1	0h RW/V	**Memory Type (MT):** Set to 00b indicating a 32-bit BAR.
0	0h RW/V	**Memory/I/O Space (MIOS):** Set to 0 indicating a Memory Space BAR.

8.1.6 Subsystem Vendor & Subsytem ID (DMI_CONFIG11)—Offset 2Ch

Access Method

Type: CFG Register (Size: 32 bits)

Device: 31
Function: 6

Default: 8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/V	**Subsystem ID (SID):** This value may be loaded automatically from the NVM Word 0Bh upon power up or reset depending on the "Load Subsystem ID" bit field in NVM word 0Ah with a default value of 0000h. This value is loadable from NVM word location 0Ah.
15:0	8086h RW/V	**Subsystem Vendor ID (SVID):** This value may be loaded automatically from the NVM Word 0Ch upon power up or reset depending on the "Load Subsystem ID" bit field in NVM word 0Ah. A value of 8086h is default for this field upon power up if the NVM does not respond or is not programmed. All functions are initialized to the same value.

8.1.7 Expansion ROM Base Address Register (ERBA)—Offset 30h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 31
Function: 6

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Expansion ROM Base Address (ERBA):** This register is used to define the address and size information for boot-time access to the optional FLASH memory. If no Flash memory exists, this register reports 00000000h.

8.1.8 Capabilities List Pointer Register (CAPP)—Offset 34h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 6

Default: C8h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	C8h RW/V	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list is at C8h in configuration space.

8.1.9 Interrupt Information & Maximum Latency/Minimum GrantRegister (INTR_MLMG)—Offset 3Ch

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 6

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V	**Maximum Latency (ML):** Not used. Hardwired to 00h.
23:16	0h RW/V	**Minimum Grant (MG):** Not used. Hardwired to 00h.
15:8	1h RW/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the GbE LAN controller. 01h = The GbE LAN controller implements legacy interrupts on INTA.
7:0	0h RW	**Interrupt Line (ILINE):** Default = 00h. Software written value indicates which interrupt line (vector) the interrupt is connected. No hardware action is taken on this register.

8.1.10 LAN Disable Control (LANDISCTRL)—Offset A0h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 6

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**LAN Disable (LD):** Setting this bit to 1 will disable the LAN Controller functionality.

8.1.11 Lock LAN Disable (LOCKLANDIS)—Offset A4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**Lock LAN Disable (LLD):** When set this bit blocks writes to the LANDISCTRL register. Note: Once set this bit will only be cleared on host reset.

8.1.12 System Time Control High Register (LTRCAP)—Offset A8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:26	0h RW	**Maximum Non-Snoop Latency Scale (MNSLS):** Provides a scale for the value contained within the Maximum Non-Snoop Latency Value field. 000b = Value times 1 ns 001b = Value times 32 ns 010b = Value times 1,024 ns 011b = Value times 32,768 ns 100b = Value times 1,048,576 ns 101b = Value times 33,554,432 ns 110b–111b = Reserved
25:16	0h RW	**Maximum Non-Snoop Latency (MNSL):** Specifies the maximum non-snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less. This field is also an indicator of the platforms maximum latency, should an endpoint send up LTR Latency Values with the Requirement bit not set.

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12:10	0h RW	**Maximum Snoop Latency Scale (MSLS):** Provides a scale for the value contained within the Maximum Snoop Latency Value field. 000b = Value times 1 ns 001b = Value times 32 ns 010b = Value times 1,024 ns 011b = Value times 32,768 ns 100b = Value times 1,048,576 ns 101b = Value times 33,554,432 ns 110b–111b = Reserved
9:0	0h RW	**Maximum Snoop Latency (MSL):** Specifies the maximum snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less. This field is also an indicator of the platforms maximum latency, should an endpoint send up LTR Latency Values with the Requirement bit not set.

8.1.13 Capabilities List and Power Managment Capabilities Register (CLIST1_PMC)—Offset C8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 23D001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RW/V	**PME_SUPPORT (PMES):** This five-bit field indicates the power states in which the function may assert PME#. It depend on PM Ena and AUX-PWR bits in word 0Ah in the NVM: Condition Functionality Value PM Ena=0 No PME at all states 0000b PM Ena and AUX-PWR=0 PME at D0 and D3HOT 01001b PM Ena and AUX-PWR=1 PME at D0, D3HOT and D3COLD 11001b These bits are not reset by Function Level Reset.
26	0h RW/V	**D2_SUPPORT (D2S):** The D2 state is not supported.
25	0h RW/V	**D1_SUPPORT (D1S):** The D1 state is not supported.
24:22	0h RW/V	**AUX_CURRENT (AC):** Required current defined in the Data register.
21	1h RW/V	**Device Specific Initialization (DSI):** Set to 1. The GbE LAN Controller requires its device driver to be executed following transition to the D0 un-initialized state.
20	0h RO	Reserved.
19	0h RW/V	**PME Clock (PMEC):** Hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
18:16	3h RW/V	**Version (VER):** Hardwired to 010b to indicate support for Revision 1.1 of the PCI Power Management Specification.
15:8	D0h RW/V	**Next Capability (NEXT):** Value of D0h indicates the location of the next pointer.
7:0	1h RW/V	**Capability ID (CID):** Indicates the linked list item is a PCI Power Management Register.

8.1.14 PCI Power Management Control Status & Data Register (PMCS_DR)—Offset CCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/V	**PME STATUS (PMES):** This bit is set to 1 when the function detects a wake-up event independent of the state of the PMEE bit. Writing a 1 will clear this bit.
14:13	0h RW/V	**DATA SCALE (DSC):** This field indicates the scaling factor to be used when interpreting the value of the Data register. For the GbE LAN and common functions this field equals 01b (indicating 0.1 watt units) if the PM is enabled in the NVM, and the Data_Select field is set to 0, 3, 4, 7, (or 8 for Function 0). Otherwise, it equals 00b. For the manageability functions, this field equals 10b (indicating 0.01 watt units) if the PM is enabled in the NVM, and the Data_Select field is set to 0, 3, 4, 7. Otherwise, it equals 00b.
12:9	0h RW	**Data Select (DSL):** This four-bit field is used to select which data is to be reported through the Data register (offset CFh) and Data_Scale field. These bits are writeable only when Power Management is enabled using NVM. 0h = D0 Power Consumption 3h = D3 Power Consumption 4h = D0 Power Dissipation 7h = D3 Power Dissipation 8h = Common Power All other values are reserved.
8	0h RW	**PME Enable (PMEE):** If Power Management is enabled in the NVM, writing a 1 to this bit will enable Wakeup. If Power Management is disabled in the NVM, writing a 1 to this bit has no affect, and will not set the bit to 1. This bit is not reset by Function Level Reset.
7:2	0h RO	Reserved.
1:0	0h RW/V	**Power State (PS):** This field is used both to determine the current power state of the GbE LAN Controller and to set a new power state. The values are: 00 = D0 state (default) 01 = Ignored 10 = Ignored 11 = D3 state (Power Management must be enabled in the NVM or this cycle will be ignored).

8.1.15 Capabilities List 2 & Message Control Register (CLIST2_MCTL)—Offset D0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 80E005h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RW/V	**64-bit Capable (64BC):** Set to 1 to indicate that the GbE LAN Controller is capable of generating 64-bit message addresses.
22:20	0h RW/V	**Multiple Message Enable (MME):** Returns 000b to indicate that the GbE LAN controller only supports a single message.
19:17	0h RW/V	**Multiple Message Capable (MMC):** The GbE LAN controller does not support multiple messages.
16	0h RW	**Message Signal Interrupt Enable (MSIE):** 0 = MSI generation is disabled. 1 = The Gb LAN controller will generate MSI for interrupt assertion instead of INTx signaling.
15:8	E0h RW/V	**Next Capability (NEXT):** Value of E0h points to the Function Level Reset capability structure. These bits are not reset by Function Level Reset.
7:0	5h RW/V	**Capability ID (CID):** Indicates the linked list item is a Message Signaled Interrupt Register.

8.1.16 Message Address Low Register (MADDL)—Offset D4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 6

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW/V	**Message Address Low (MADDL):** These bits combine with MADDL2 to create one 32 bit field which is written by the system to indicate the lower 32 bits of the address to use for the MSI memory write transaction.
1:0	0h RW/V	**Message Address Low 2 (MADDL2):** These bits combine with MADDL to create one 32 bit field which is written by the system to indicate the lower 32 bits of the address to use for the MSI memory write transaction. These lower two bits will always return 0.

8.1.17 Message Address High Register (MADDH)—Offset D8h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 6

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Message Address High (MADDH):** Written by the system to indicate the upper 32 bits of the address to use for the MSI memory write transaction.

8.1.18 Message Data Register (MDAT)—Offset DCh

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 6

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Message Data (MDAT):** Written by the system to indicate the lower 16 bits of the data written in the MSI memory write DWord transaction. The upper 16 bits of the transaction are written as 0000h.

8.2 GbE Memory Mapped I/O Registers Summary

Table 8-2. Summary of GbE Memory Mapped I/O Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Gigabit Ethernet Capabilities and Status (GBECSR_00)—Offset 0h	0h
18h	1Bh	Gigabit Ethernet Capabilities and Status (GBECSR_18)—Offset 18h	0h
20h	23h	Gigabit Ethernet Capabilities and Status (GBECSR_20)—Offset 20h	10000000h
F00h	F03h	Gigabit Ethernet Capabilities and Status (GBECSR_F00)—Offset F00h	0h
F10h	F13h	Gigabit Ethernet Capabilities and Status F10 (GBECSR_F10)—Offset F10h	Ch
5400h	5403h	Gigabit Ethernet Capabilities and Status (GBECSR_5400)—Offset 5400h	0h
5404h	5407h	Gigabit Ethernet Capabilities and Status (GBECSR_5404)—Offset 5404h	0h
5800h	5803h	Gigabit Ethernet Capabilities and Status (GBECSR_5800)—Offset 5800h	0h
5B54h	5B57h	Gigabit Ethernet Capabilities and Status (GBECSR_5B54)—Offset 5B54h	0h

8.2.1 Gigabit Ethernet Capabilities and Status (GBECSR_00)—Offset 0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW	**PHY Power Down (PHYPDN):** When cleared (0b), the PHY power down setting is controlled by the internal logic of PCH.
23:0	0h RO	Reserved.

8.2.2 Gigabit Ethernet Capabilities and Status (GBECSR_18)—Offset 18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved.
20	0h RW	**PHY Power Down Enable (PHYPDEN):** When set, this bit enables the PHY to enter a low-power state when the LAN controller is at the DMOff/ D3 or with no WOL.
19:0	0h RO	Reserved.

8.2.3 Gigabit Ethernet Capabilities and Status (GBECSR_20)—Offset 20h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 10000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V	**Wait:** Set to 1 by the Gigabit Ethernet Controller to indicate that a PCI Express* to SMBus transition is taking place. The ME/Host should not issue new MDIC transactions while this bit is set to 1. This bit is auto cleared by hardware after the transition has occurred.
30	0h RW/V	**Error:** Set to 1 by the Gigabit Ethernet Controller when it fails to complete an MDI read. Software should make sure this bit is clear before making an MDI read or write command.
29	0h RW/V	**Interrupt Enable (IE):** hen set to 1 by software, it will cause an Interrupt to be asserted to indicate the end of an MDI cycle.
28	1h RW/V	**Ready Bit (RB):** Set to 1 by the Gigabit Ethernet Controller at the end of the MDI transaction. This bit should be reset to 0 by software at the same time the command is written.
27:26	0h RW/V	**MDI Type:** 01 = MDI Write 10 = MDI Read All other values are reserved.
25:21	0h RW/V	**LAN Connected Device Address (PHYADD)**
20:16	0h RW/V	**LAN Connected Device Register Address (REGADD)**
15:0	0h RW/V	**DATA:** In a Write command, software places the data bits and the MAC shifts them out to the LAN Connected Device. In a Read command, the MAC reads these bits serially from the LAN Connected Device and software can read them from this location.

8.2.4 Gigabit Ethernet Capabilities and Status (GBECSR_F00)—Offset F00h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	0h RW/V	**Software Semaphore FLAG (SWFLAG):** This bit is set by the device driver to gain access permission to shared CSR registers with the firmware and hardware.
4:0	0h RO	Reserved.

8.2.5 Gigabit Ethernet Capabilities and Status F10 (GBECSR_F10)—Offset F10h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: Ch

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	Reserved.
6	0h RW	**Global GbE Disable (GGD):** Prevents the PHY from auto-negotiating 1000Mb/s link in all power states.
5:4	0h RO	Reserved.
3	1h RW	**GbE Disable at non D0a—:** Prevents the PHY from auto-negotiating 1000Mb/s link in all power states except D0a. This bit must be set since GbE is not supported in Sx states.
2	1h RW	**LPLU in non D0a (LPLUND):** Enables the PHY to negotiate for the slowest possible link in all power states except D0a.
1	0h RW	**LPLU in D0a (LPLUD):** Enables the PHY to negotiate for the slowest possible link in all power states. This bit overrides bit 2.
0	0h RO	Reserved.

8.2.6 Gigabit Ethernet Capabilities and Status (GBECSR_5400)—Offset 5400h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Receive Address Low (RAL):** The lower 32 bits of the 48-bit Ethernet Address.

8.2.7 Gigabit Ethernet Capabilities and Status (GBECSR_5404)—Offset 5404h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Address Valid (AV)**
30:16	0h RO	Reserved.
15:0	0h RW	**Receive Address High (RAH):** The lower 16 bits of the 48-bit Ethernet Address.

8.2.8 Gigabit Ethernet Capabilities and Status (GBECSR_5800)—Offset 5800h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**Advanced Power Management Enable (APME):** 1 = APM Wakeup is enabled 0 = APM Wakeup is disabled

8.2.9 Gigabit Ethernet Capabilities and Status (GBECSR_5B54)—Offset 5B54h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Firmware Valid Bit (FWVAL):** 1 = Firmware is ready 0 = Firmware is not ready
14:0	0h RO	Reserved.

9 UART Interface (D30:F0/F1 and D25:F2)

9.1 UART PCI Configuration Registers Summary

Table 9-1. Summary of UART PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID (DEVVENDID)—Offset 0h	XXXX8086h
4h	7h	Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	Revision ID and Class Code (REVCLASSCODE)—Offset 8h	C8000XXh
Ch	Fh	Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	800000h
10h	13h	Base Address (BAR)—Offset 10h	4h
14h	17h	Base Address High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	Base Address 1 (BAR1)—Offset 18h	4h
1Ch	1Fh	Base Address 1 High (BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	EXPANSION ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	Interrupt Register (INTERRUPTREG)—Offset 3Ch	0h
80h	83h	Power Management Capability ID (POWERCAPID)—Offset 80h	39001h
84h	87h	Power Management Control and Status (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	SW LTR update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	2101h
9Ch	9Fh	Device IDLE Pointer (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	24C1h
A0h	A3h	Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	F0800h
B0h	B3h	General Purpose Read Write Register1 (GEN_REGRW1)—Offset B0h	0h
B4h	B7h	General Purpose Read Write 2 (GEN_REGRW2)—Offset B4h	0h
B8h	BBh	General Purpose PCI Read Write 3 (GEN_REGRW3)—Offset B8h	0h
BCh	BFh	General Purpose Read Write 4 (GEN_REGRW4)—Offset BCh	0h
C0h	C3h	General Purpose Input (GEN_INPUT_REG)—Offset C0h	0h

9.1.1 Device ID and Vendor ID (DEVVENDID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: XXXX8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	-- RO/P	**Device ID Field (DEVICEID):** This is a 16-bit value assigned to the controller. See the Device and Revision ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor ID Field (VENDORID):** Identifies the manufacturer of the device. 8086h = Intel.

9.1.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 100000h

Bit Range	Default and Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**RMA Field (RMA):** S/W writes a '1' to this bit to clear it.
28	0h RW/1C	**RTA Field (RTA):** S/W writes a '1' to this bit to clear it.
27:21	0h RO	Reserved.
20	1h RO	**Cap List Field (CAPLIST):** Indicates that the controller contains a capabilities pointer list.
19	0h RO	**Intrerrupt Status Field (INTR_STATUS):** This bit reflects state of interrupt in the device.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Setting this bit disables INTx assertion. The interrupt disabled is legacy INTx# interrupt. This bit has no connection with interrupt status bit.
9	0h RO	Reserved.
8	0h RW	**SERR Enable Field (SERR_ENABLE):** Not implemented.
7:3	0h RO	Reserved.
2	0h RW	**BME Field (BME):** If this bit is 0, the controller does not generate any new upstream transaction as a master.
1	0h RW	**MSE Field (MSE):** 0 = Disables memory mapped Configuration space. 1 = Enables memory mapped configuration space.
0	0h RO	Reserved.

9.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: C8000XXh

Bit Range	Default and Access	Field Name (ID): Description
31:8	C8000h RO	**Class Code (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	-- RO/P	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

9.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 800000h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**MultiFunction Device Field (MULFNDEV):** 0 = Single Function Device 1 = Multi Function device
22:16	0h RO	**Header Type Field (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	0h RO	**Latency Timer Field (LATTIMER):** Hardwired to 0.
7:0	0h RW/P	**Cache Line Size Field (CACHELINE_SIZE)**

9.1.5 Base Address (BAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW	**Base Address Field (BASEADDR):** Provides system memory base address for the controller.
11:4	0h RO	**Size Field (SIZEINDICATOR):** Always returns 0. The size of this register depends on the size of the memory space.
3	0h RO	**Prefetchable Field (PREFETCHABLE):** 0 indicates that this BAR is not prefetchable.
2:1	2h RO	**Type Field (TYPE):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** 0 indicates this BAR is present in the memory space.

9.1.6 Base Address High (BAR_HIGH)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address High Field (BASEADDR_HIGH)**

9.1.7 Base Address 1 (BAR1)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW	**Base Address Field (BASEADDR1):** This field is present if BAR1 is enabled.
11:4	0h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** 0 indicates that this BAR is not prefetchable.
2:1	2h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** 0 indicates this BAR is present in the memory space.

9.1.8 Base Address 1 High (BAR1_HIGH)—Offset 1Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address High Field (BASEADDR1_HIGH)**

9.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** The register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other. This register is a Read Write Once type register.
15:0	0h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** The register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

9.1.10 EXPANSION ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address register is a RO indicates support for expansion ROMs

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION ROM base address field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

9.1.11 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Capabilities Pointer register indicates what the next capability is

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Indicates what the next capability is.

9.1.12 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**Min Gnt Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	Reserved.
11:8	0h RO	**Interrupt Pin Field (INTPIN)**
7:0	0h RW/P	**Int Line Field (INTLINE):** It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

9.1.13 Power Management Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 39001h

Bit Range	Default and Access	Field Name (ID): Description
31:27	0h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for for a bit indicates that the function is not capable of asserting the PME# signal while in that power state. Bit 27 = 1: PME# can be asserted from D0. Bit 30 = 1: PME# can be asserted from D3 hot. Other bits are not used.
26:19	0h RO	Reserved.
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**Next Cap Field (NXTCAP):** Points to the next capability structure.
7:0	1h RO	**Power Capability ID Field (POWER_CAP):** Indicates power management capability is supported.

9.1.14 Power Management Control and Status (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C/P	**PME Status Field (PMESTATUS)**
14:9	0h RO	Reserved.
8	0h RW/P	**PME Enable Field (PMEENABLE):** 0 = PME message is disabled 1 = PME message is enabled.
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	Reserved.
1:0	0h RW	**Power State Field (POWERSTATE):** This field is used both to determine the current power state and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field,the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked.

9.1.15 PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: F0140009h

Bit Range	Default and Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision ID (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	0h RO	**Next Capability Field (NEXT_CAP):** Points to the next capability structure. This points to NULL.
7:0	9h RO	**Capability ID Field (CAPID)**

9.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG)—Offset 94h

Extended Vendor capability register for VSEC Length revision and ID

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 1400010h

Bit Range	Default and Access	Field Name (ID): Description
31:20	14h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor specific Extended Capability revision
15:0	10h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

9.1.17 SW LTR update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Software location pointer in MMIO space as an offset specified by BAR

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 2101h

Bit Range	Default and Access	Field Name (ID): Description
31:4	210h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR BAR Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	1h RO	**SW LTR Valid Field (SW_LAT_VALID)**

9.1.18 Device IDLE Pointer (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset location BAR NUM and D0i3 Valid Strap

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 24C1h

Bit Range	Default and Access	Field Name (ID): Description
31:4	24Ch RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** Indicates that the D0i3 MMIO location is always at BAR0.
0	1h RO	**D0i3 Valid Field (VALID):** 0 = Not valid 1 = Valid

9.1.19 Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: F0800h

Bit Range	Default and Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/P	**HAE Field (HAE)**
20	0h RO	Reserved.
19	1h RW/P	**Sleep Enable Field (SLEEP_EN)**
18	1h RW/P	**D3 Hen Field (PGE):** If clear, the controller will never request a PG. If 1, then the function will power gate when idle and the DevIdle bit is set.
17	1h RW/P	**Device Idle En Field (I3_ENABLE):** If 1, then function will power gate when idle and the PMCSR[1:0] register in the function = 11 (D3).
16	1h RW/P	**PMC Request Enable Field (PMCRE):** If this bit is set to '1', the function will power gate when idle.
15:13	0h RO	Reserved.
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** This value is written by BIOS to communicate to the Driver.
9:0	0h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** This value is written by BIOS to communicate to the Driver.

9.1.20 General Purpose Read Write Register1 (GEN_REGRW1)—Offset B0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW1):** General purpose read write PCI register.

9.1.21 General Purpose Read Write 2 (GEN_REGRW2)—Offset B4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW2):** General purpose read write PCI register.

9.1.22 General Purpose PCI Read Write 3 (GEN_REGRW3)—Offset B8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW3):** General purpose read write PCI register.

9.1.23 General Purpose Read Write 4 (GEN_REGRW4)—Offset BCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW4):** General purpose read write PCI register.

9.1.24 General Purpose Input (GEN_INPUT_REG)—Offset C0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register.

9.2 UART Memory Mapped Registers Summary

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Table 9-2. Summary of UART Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Receive Buffer Register (RBR)—Offset 0h	0h
0h	3h	Transmit Holding Register (THR)—Offset 0h	0h
0h	3h	Divisor Latch Low Register (DLL)—Offset 0h	0h
4h	7h	Divisor Latch High (DLH)—Offset 4h	0h
4h	7h	Interrupt Enable Register (IER)—Offset 4h	0h
8h	Bh	Interrupt Identification (IIR)—Offset 8h	1h
8h	Bh	FIFO Control (FCR)—Offset 8h	1h
Ch	Fh	Line Control Register (LCR)—Offset Ch	0h
10h	13h	Modem Control Register (MCR)—Offset 10h	0h
14h	17h	Line Status Register (LSR)—Offset 14h	60h
18h	1Bh	Modem Status Register (MSR)—Offset 18h	0h
1Ch	1Fh	Scratchpad Register (SCR)—Offset 1Ch	0h
30h	33h	Shadow Receive Buffer and Shadow Transmit Holding 0 (SRBR_STHR0)—Offset 30h	0h
70h	73h	FIFO Access Register (FAR)—Offset 70h	0h
74h	77h	Transmit FIFO Read (TFR)—Offset 74h	0h
78h	7Bh	Receive FIFO Write (RFW)—Offset 78h	0h
7Ch	7Fh	UART Status Register (USR)—Offset 7Ch	6h
80h	83h	Transmit FIFO Level (TFL)—Offset 80h	0h
84h	87h	Receive FIFO Level (RFL)—Offset 84h	0h
88h	8Bh	Software Reset (SRR)—Offset 88h	0h
8Ch	8Fh	Shadow Request to Send (SRTS)—Offset 8Ch	0h
90h	93h	Shadow Break Control (SBCR)—Offset 90h	0h
94h	97h	Shadow DMA Mode (SDMAM)—Offset 94h	0h
98h	9Bh	Shadow FIFO Enable (SFE)—Offset 98h	0h
9Ch	9Fh	Shadow RCVR Trigger (SRT)—Offset 9Ch	0h
A0h	A3h	Shadow TX Empty Trigger (STET)—Offset A0h	0h
A4h	A7h	Halt TX (HTX)—Offset A4h	0h
A8h	ABh	DMA Software Acknowledge (DMASA)—Offset A8h	0h
F4h	F7h	Component Parameter (CPR)—Offset F4h	43F32h

9.2.1 Receive Buffer Register (RBR)—Offset 0h

RBR mode is only available when LCR register, DLAB bit = 0.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RO	**rbr (rbr):** Data byte received on the serial input port in UART mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an over-run error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an over-run error occurs.

9.2.2 Transmit Holding Register (THR)—Offset 0h

THR mode is only available when LCR register, DLAB bit = 0.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h WO	**thr (thr):** Data to be transmitted on the serial output port in UART mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFOs are disabled (FCR[0] = 0) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFOs are enabled (FCR[0] = 1) and THRE is set, 64 characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.

9.2.3 Divisor Latch Low Register (DLL)—Offset 0h

DLL mode is only available when LCR register, DLAB bit = 1.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**dll (dll):** Lower 8 bits of a 16-bit, read/write Divisor Latch register that contains the baud rate divisor for the UART. This register may be accessed only when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur.

9.2.4 Divisor Latch High (DLH)—Offset 4h

DLH mode is only available when LCR register [7] (DLAB bit) = 1

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h NA	**dlh (dlh):** Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may be accessed only when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur.

9.2.5 Interrupt Enable Register (IER)—Offset 4h

IER mode is only available when LCR register [7] (DLAB bit) = 0.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**PTIME (PTIME):** THRE Interrupt Mode Enable: This is used to enable/disable the generation of THRE Interrupt. 0 = disabled 1 = enabled
6:4	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
3	0h RW	**EDSSI (EDSSI):** Enable Modem Status Interrupt: This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0 = disabled 1 = enabled
2	0h RW	**ELSI (ELSI):** Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0 = disabled 1 = enabled
1	0h RW	**ETBEI (ETBEI):** Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0 = disabled 1 = enabled
0	0h RW	**ERBFI (ERBFI):** Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0 = disabled 1 = enabled

9.2.6 Interrupt Identification (IIR)—Offset 8h

Note that the register can also be used as FIFO Control Register (FCR) when it is written to.

Access Method

Type: MEM Register (Size: 32 bits)

Device:

Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:6	0h RO	**FIFOSE (FIFOSE):** FIFOs Enabled. This is used to indicate whether the FIFOs are enabled or disabled. 00 = disabled 11 = enabled
5:4	0h RO	Reserved.
3:0	1h RO	**IID (IID):** This indicates the highest priority pending interrupt which can be one of the following types: 0000 = modem status 0001 = no interrupt pending 0010 = THR empty 0100 = received data available 0110 = receiver line status 0111 = busy detect 1100 = character timeout Note: An interrupt of type 0111 (busy detect) is never indicated because the controller is compatible with UART_16550 mode. Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.

9.2.7 FIFO Control (FCR)—Offset 8h

Note that the register can also be used as Interrupt Identification register (IIR)when it is read from.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:6	0h WO	**RCVR (RCVR):** This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO ¼ full 10 = FIFO ½ full 11 = FIFO 2 less than full
5:4	0h WO	**TET (TET):** This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO ¼ full 11 = FIFO ½ full
3	0h RO	Reserved.
2	0h WO	**XFIFOR (XFIFOR):** This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	0h WO	**RFIFOR (RFIFOR):** This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	1h WO	**FIFOE (FIFOE):** This is used to indicate whether the FIFOs are enabled or disabled. 00 = disabled 11 = enabled

9.2.8 Line Control Register (LCR)—Offset Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h NA	**Res_31_8 (Res_31_8):** Reserved
7	0h RW	**DLAB (DLAB):** This bit is used to enable reading and writing of the Divisor Latch register(DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers
6	0h RW	**Break (Break):** This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the serial out line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.

Bit Range	Default and Access	Field Name (ID): Description
5	0h RO	Reserved.
4	0h RW	**EPS (EPS):** Even Parity Select. If UART_16550_COMPATIBLE == NO, then writable only when UART is not busy (USR[0] is zero); otherwise always writable, always readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked. Reset Value: 0x0
3	0h RW	**PEN (PEN):** This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 0 = parity disabled 1 = parity enabled
2	0h RW	**STOP (STOP):** This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 0 = 1 stop bit 1 = 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	0h RW	**DLS (DLS):** This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits

9.2.9 Modem Control Register (MCR)—Offset 10h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	0h RW	**AFCE (AFCE):** Auto Flow Control Enable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set. The bit is used to help for flow control using external IO pins with the pairing device. 0 = Auto Flow Control Mode disabled 1 = Auto Flow Control Mode enabled
4	0h RW	**LoopBack (LoopBack):** LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes. Data on the serial out line is held high, while serial data output is looped back to the serial in line, internally. In this mode all the interrupts are fully functional. Also, in loop back mode, the modem control input (cts_n,) are disconnected and the modem control output (rts_n) are looped back to the inputs, internally.

Bit Range	Default and Access	Field Name (ID): Description
3:2	0h RO	Reserved.
1	0h RW	**RTS (RTS):** Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	0h RO	Reserved.

9.2.10 Line Status Register (LSR)—Offset 14h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 60h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**RFE (RFE):** Receiver FIFO Error bit. This bit is only relevant when FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 0 = no error in RX FIFO 1 = error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO
6	1h RW	**TEMT (TEMT):** Transmitter Empty bit. If FIFOs enabled(FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	1h RW	**THRE (THRE):** Transmit Holding Register Empty bit. If THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If both THRE Interrupt and FIFO modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting
4	0h RW	**BI (BI):** Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data. It is set whenever the serial input (sin) is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.

Bit Range	Default and Access	Field Name (ID): Description
3	0h RW	**FE (FE):** Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit(LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit(LSR[4]). 0 = no framing error 1 = framing error Reading the LSR clears the FE bit.
2	0h RW	**PE (PE):** Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = no parity error 1 = parity error Reading the LSR clears the PE bit.
1	0h RW	**OE (OE):** Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and anew character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0 = no overrun error 1 = overrun error Reading the LSR clears the OE bit.
0	0h RW	**DR (DR):** Data Ready bit. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. 0 = no data ready 1 = data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

9.2.11 Modem Status Register (MSR)—Offset 18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**CTS (CTS):** Clear to Send. This is used to indicate the current state of the modem control line cts_n.This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it isan indication that the modem or data set is ready to exchange data with the UART. 0 = cts_n input is de-asserted (logic 1) 1 = cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3:1	0h RO	Reserved.
0	0h RO	**DCTS (DCTS):** Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. 0 = no change on cts_n since last read of MSR 1 = change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS).Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs(software or otherwise), then the DCTS bit is set when the reset is removed if the cts_nsignal remains asserted.

9.2.12 Scratchpad Register (SCR)—Offset 1Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h NA	**Reserrved (Reserrved):** Reserved
7:0	0h RW	**scr (scr):** This register is for programmers to use as a temporary storage space.

9.2.13 Shadow Receive Buffer and Shadow Transmit Holding 0 (SRBR_STHR0)—Offset 30h

NOTE: There are a total of 16 Shadow Receive Buffer Registers (SRBR_STHR[15:0]. The register description is the same for all of them. The other registers are at the following offsets:
SRBR_STHR1 at offset 34h
SRBR_STHR2 at offset 38h
SRBR_STHR3 at offset 3Ch
.....
SRBR_STHR14 at offset 68h
SRBR_STHR15 at offset 6Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**srbr_sthr0 (srbr_sthr0):** Used as SRBR: This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set. If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs. Used as STHR: This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If FIFOs are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten. If FIFOs are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.

9.2.14 FIFO Access Register (FAR)—Offset 70h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**srbr_sthr (srbr_sthr):** Writes have no effect when FIFO_ACCESS == No, always readable. This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master. 0 = FIFO access mode disabled 1 = FIFO access mode enabled Note, that when the FIFO access mode is enabled/disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty. Reset Value: 0x0

9.2.15 Transmit FIFO Read (TFR)—Offset 74h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RO	**tfr (tfr):** Transmit FIFO Read. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO. When FIFOs are not implemented or not enabled, reading this register gives the data in the THR. Reset Value: 0x0

9.2.16 Receive FIFO Write (RFW)—Offset 78h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9	0h WO	**RFFE (RFFE):** Receive FIFO Framing Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR.
8	0h WO	**RFPE (RFPE):** Receive FIFO Parity Error. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR.
7:0	0h WO	**RFWD (RFWD):** Receive FIFO Write Data. These bits are only valid when FIFO access mode is enabled(FAR[0] is set to one). When FIFOs are enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR.

9.2.17 UART Status Register (USR)—Offset 7Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 6h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**RFF (RFF):** Receive FIFO Full. This is used to indicate that the receive FIFO is completely full. 0 = Receive FIFO not full 1 = Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	0h RO	**RFNE (RFNE):** Receive FIFO Not Empty. This is used to indicate that the receive FIFO contains one or more entries. 0 = Receive FIFO is empty 1 = Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.
2	1h RO	**TFE (TFE):** Transmit FIFO Empty. This is used to indicate that the transmit FIFO is completely empty. 0 = Transmit FIFO is not empty 1 = Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty
1	1h RO	**TFNF (TFNF):** Transmit FIFO Not Full. This is used to indicate that the transmit FIFO in not full. 0 = Transmit FIFO is full 1 = Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	0h RO	Reserved.

9.2.18 Transmit FIFO Level (TFL)—Offset 80h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:0	0h RO	**tfl (tfl):** Transmit FIFO Level. This is indicates the number of data entries in the transmit FIFO. Reset Value: 0x0

9.2.19 Receive FIFO Level (RFL)—Offset 84h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:0	0h RO	**rfl (rfl):** Receive FIFO Level. This is indicates the number of data entries in the receive FIFO. Reset Value: 0x0

9.2.20 Software Reset (SRR)—Offset 88h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**XFR (XFR):** XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
1	0h RW	**RFR (RFR):** RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO This resets the control portion of the receive FIFO and treats the FIFO as empty. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.
0	0h RW	**UR (UR):** UART Reset. This asynchronously resets the UART controller and synchronously removes the reset assertion.

9.2.21 Shadow Request to Send (SRTS)—Offset 8Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**srts (srts):** Shadow Request to Send. This is a shadow register for the RTS bit (MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the DW_apb_uart is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). Note that in Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input. Reset Value: 0x0

9.2.22 Shadow Break Control (SBCR)—Offset 90h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**sbcb (sbcb):** Shadow Break Control Register. This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. When in Loopback Mode, the break condition is internally looped back to the receiver.

9.2.23 Shadow DMA Mode (SDMAM)—Offset 94h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**sdmam (sdmam):** Shadow DMA Mode. This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. 0 = mode 0 1 = mode 1

9.2.24 Shadow FIFO Enable (SFE)—Offset 98h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**sfe (sfe):** Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated.This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset. Reset Value: 0x0

9.2.25 Shadow RCVR Trigger (SRT)—Offset 9Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RW	**srt (srt):** Shadow RCVR Trigger. This is a shadow register for the RCVR trigger bits(FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO ¼ full 10 = FIFO ½ full 11 = FIFO 2 less than full

9.2.26 Shadow TX Empty Trigger (STET)—Offset A0h

Shadow TX Empty Trigger. This is a shadow register for the TX empty trigger bits(FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TXempty trigger bit gets updated. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RW	**stet (stet):** Shadow TX Empty Trigger: This is a shadow register for the TX empty trigger bits(FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated. 165 This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO ¼ full 11 = FIFO ½ full

9.2.27 Halt TX (HTX)—Offset A4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**htx (htx):** This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 = Halt TX disabled 1 = Halt TX enabled Note, if FIFOs are not enabled, the setting of the halt TX register has no effect on operation.

9.2.28 DMA Software Acknowledge (DMASA)—Offset A8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h WO	**dmasa (dmasa):** This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the UART should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. Note that this bit is 'self-clearing'. It is not necessary to clear this bit.

9.2.29 Component Parameter (CPR)—Offset F4h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 43F32h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	4h RO	**FIFO_MODE (FIFO_MODE):** 0x00 = 0 0x01 = 16 0x02 = 32 to 0x80 = 2048
15:14	0h RO	Reserved.
13	1h RO	**DMA_EXTRA (DMA_EXTRA):** 0 = FALSE, 1 = TRUE
12	1h RO	**UART_ADD_ENCODED_PARAMS (UART_ADD_ENCODED_PARAMS):** 0 = FALSE, 1 = TRUE
11	1h RO	**SHADOW (SHADOW):** 0 = FALSE, 1 = TRUE
10	1h RO	**FIFO_STAT (FIFO_STAT):** 0 = FALSE, 1 = TRUE
9	1h RO	**FIFO_ACCESS (FIFO_ACCESS):** 0 = FALSE, 1 = TRUE
8	1h RO	**ADDITIONAL_FEAT (ADDITIONAL_FEAT):** 0 = FALSE, 1 = TRUE
7	0h RO	**SIR_LP_MODE (SIR_LP_MODE):** 0 = FALSE, 1 = TRUE
6	0h RO	**SIR_MODE (SIR_MODE):** 0 = FALSE, 1 = TRUE
5	1h RO	**THRE_MODE (THRE_MODE):** 0 = FALSE, 1 = TRUE
4	1h RO	**AFCE_MODE (AFCE_MODE):** 0 = FALSE, 1 = TRUE
3:2	0h RO	Reserved.
1:0	2h RO	**APB_DATA_WIDTH (APB_DATA_WIDTH):** 00 = 8 bits

9.3 UART Additional Memory Mapped Registers Summary

Table 9-3. Summary of UART Additional Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
200h	203h	Clock Configuration (CLOCKS)—Offset 200h	0h
204h	207h	Resets (RESETS)—Offset 204h	0h
210h	213h	Active LTR (ACTIVELTR_VALUE)—Offset 210h	800h
214h	217h	Idle LTR (IDLELTR_VALUE)—Offset 214h	800h
218h	21Bh	Tx Byte Count (TX_BYTE_COUNT)—Offset 218h	0h
21Ch	21Fh	Rx Byte Count (RX_BYTE_COUNT)—Offset 21Ch	0h
228h	22Bh	SW Scratch 0 (SW_SCRATCH_0)—Offset 228h	0h
238h	23Bh	clock Gate (CLOCK_GATE)—Offset 238h	0h
240h	243h	Address Low (REMAP_ADDR_LO)—Offset 240h	0h
244h	247h	Address High (REMAP_ADDR_HI)—Offset 244h	0h
24Ch	24Fh	Device Idle Control (DEVIDLE_CONTROL)—Offset 24Ch	8h
2FCh	2FFh	Capabilities (CAPABLITIES)—Offset 2FCh	10h

9.3.1 Clock Configuration (CLOCKS)—Offset 200h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**clk_update (clk_update):** Update the clock divider after setting new m and n values. 0 - No clock Update 1 - Clock gets updated.
30:16	0h RW	**n_val (n_val):** This is the denominator value (N) for the M over N divider logic that creates CLK_OUT. Used to generate the input clk to the UART.
15:1	0h RW	**m_val (m_val):** The numerator value (M) for the M over N divider logic that creates the CLK_OUT. Used to generate the input clk to the UART.
0	0h RW	**clk_en (clk_en):** UART Serial Clock (output of M/N, input to UART) Clock Enable 0 – Clock disabled 1 – Clock Enabled.

9.3.2 Resets (RESETS)—Offset 204h

software reset

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**reset_dma (reset_dma):** Reset the DMA controller 0 = DMA controller is in reset (Reset Asserted) 1 = DMA controller is NOT at reset (Reset Released)
1:0	0h RO	Reserved.

9.3.3 Active LTR (ACTIVELTR_VALUE)—Offset 210h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 800h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**snoop_requirment (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10 -bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**snoop_latency_scale (snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which do not match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**snoop_value (snoop_value):** 10-bit latency value

9.3.4 Idle LTR (IDLELTR_VALUE)—Offset 214h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 800h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**snoop_requirment (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10 -bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**snoop_latency_scale (snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**snoop_value (snoop_value):** 10-bit latency value

9.3.5 Tx Byte Count (TX_BYTE_COUNT)—Offset 218h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**tx_count_overflow (tx_count_overflow):** 0 = count valid 1 = count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**tx_byte_count (tx_byte_count)**

9.3.6 Rx Byte Count (RX_BYTE_COUNT)—Offset 21Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**rx_count_overflow (rx_count_overflow):** [be] 0= count valid 1= count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**rx_byte_count (rx_byte_count):** rx_byte_count

9.3.7 SW Scratch 0 (SW_SCRATCH_0)—Offset 228h

NOTE: The same registers are available at the following offsets:
SW SCRATCH 1: offset 22Ch
SW SCRATCH 2: offset 230h
SW SCRATCH 3: offset 234h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SW_Scratch_0 (SW_Scratch_0):** Scratch Pad Register for SW to generated Local DATA for iDMA

9.3.8 clock Gate (CLOCK_GATE)—Offset 238h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:2	0h RW	**sw_dma_clk_ctl (sw_dma_clk_ctl):** DMA clock gate cntrol bits. 00: hw clk enable 01: Reserved 10: force off 11: force on
1:0	0h RW	**sw_ip_clk_ctl (sw_ip_clk_ctl):** Clock gate cntrol bits.{br] 00: HW clk enable 01: Reserved 10: force clock off 11: force clock on

9.3.9 Address Low (REMAP_ADDR_LO)—Offset 240h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**uart_remap_addr_low (uart_remap_addr_low):** Low 32 bits of BAR address read by SW

9.3.10 Address High (REMAP_ADDR_HI)—Offset 244h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**uart_remap_addr_high (uart_remap_addr_high):** High 32 bits of BAR address read by SW

9.3.11 Device Idle Control (DEVIDLE_CONTROL)—Offset 24Ch

This register allows a device driver to enable/disable a devices entry into DevIdle. By enabling DevIdle, SW specifies that it will not touch the device without accessing this register prior to accessing any other MMIO device register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**intr_req_capable (intr_req_capable):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0.
3	1h RW/1C	**restore_required (restore_required):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.

Bit Range	Default and Access	Field Name (ID): Description
2	0h RW	**devidle (devidle):** SW sets this bit to 1 to move the function into the DevIdle state. Writing this bit to 0 will return the function to the fully active D0 state (D0i0)
1	0h RO	Reserved.
0	0h RO	**cmd_in_progress (cmd_in_progress):** HW sets this bit on a 1->0 or 0->1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is unsupported for SW to write to any bit in this register. HW clears this bit upon completing the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

9.3.12 Capabilities (CAPABLITIES)—Offset 2FCh

capabilities register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 10h

Bit Range	Default and Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RO	**iDMA_present (iDMA_present):** 0= DMA present 1= DMA not present
7:4	1h RO	**instance_type (instance_type):** 0000 = IC2 0001 = UART 0010 = SPI 0011 – 1111 = Reserved
3:0	0h RO	**instance_number (instance_number)**

9.4 UART DMA Controller Registers Summary

Table 9-4. Summary of UART DMA Controller Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
800h	803h	DMA Transfer Source Address Low (SAR_LO0)—Offset 800h	0h
804h	807h	DMA Transfer Source Address High (SAR_HI0)—Offset 804h	0h
808h	80Bh	DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h	0h
80Ch	80Fh	DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch	0h
810h	813h	Linked List Pointer Low (LLP_LO0)—Offset 810h	0h
814h	817h	Linked List Pointer High (LLP_HI0)—Offset 814h	0h
818h	81Bh	Control Register Low (CTL_LO0)—Offset 818h	0h

Table 9-4. Summary of UART DMA Controller Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
81Ch	81Fh	Control Register High (CTL_HI0)—Offset 81Ch	0h
820h	823h	Source Status (SSTAT0)—Offset 820h	0h
828h	82Bh	Destination Status (DSTAT0)—Offset 828h	0h
830h	833h	Source Status Address Low (SSTATAR_LO0)—Offset 830h	0h
834h	837h	Source Status Address High (SSTATAR_HI0)—Offset 834h	0h
838h	83Bh	Destination Status Address Low (DSTATAR_LO0)—Offset 838h	0h
83Ch	83Fh	Destination Status Address High (DSTATAR_HI0)—Offset 83Ch	0h
840h	843h	DMA Transfer Configuration Low (CFG_LO0)—Offset 840h	203h
844h	847h	DMA Transfer Configuration High (CFG_HI0)—Offset 844h	0h
848h	84Bh	Source Gather (SGR0)—Offset 848h	0h
850h	853h	Destination Scatter (DSR0)—Offset 850h	0h
AC0h	AC3h	Raw Interrupt Status (RawTfr)—Offset AC0h	0h
AC8h	ACBh	Raw Status for Block Interrupts (RawBlock)—Offset AC8h	0h
AD0h	AD3h	Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h	0h
AD8h	ADBh	Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h	0h
AE0h	AE3h	Raw Status for Error Interrupts (RawErr)—Offset AE0h	0h
AE8h	AEBh	Interrupt Status (StatusTfr)—Offset AE8h	0h
AF0h	AF3h	Status for Block Interrupts (StatusBlock)—Offset AF0h	0h
AF8h	AFBh	Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h	0h
B00h	B03h	Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h	0h
B08h	B0Bh	Status for Error Interrupts (StatusErr)—Offset B08h	0h
B10h	B13h	Mask for Transfer Interrupts (MaskTfr)—Offset B10h	0h
B18h	B1Bh	Mask for Block Interrupts (MaskBlock)—Offset B18h	0h
B20h	B23h	Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h	0h
B28h	B2Bh	Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h	0h
B30h	B33h	Mask for Error Interrupts (MaskErr)—Offset B30h	0h
B38h	B3Bh	Clear for Transfer Interrupts (ClearTfr)—Offset B38h	0h
B40h	B43h	Clear for Block Interrupts (ClearBlock)—Offset B40h	0h
B48h	B4Bh	Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h	0h
B50h	B53h	Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h	0h
B58h	B5Bh	Clear for Error Interrupts (ClearErr)—Offset B58h	0h
B60h	B63h	Combined Status register (StatusInt)—Offset B60h	0h
B98h	B9Bh	DMA Configuration (DmaCfgReg)—Offset B98h	0h
BA0h	BA3h	DMA Channel Enable (ChEnReg)—Offset BA0h	0h

9.4.1 DMA Transfer Source Address Low (SAR_LO0)—Offset 800h

NOTE: SAR_LO0 is for DMA Channel 0. The same register definition,SAR_LO1, is available for Channel 1 at address 858h.
SAR_LO0 (CH0): offset 800h

SAR_LO1 (CH1): offset 858h
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SAR_LO (SAR_LO):** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected). 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

9.4.2 DMA Transfer Source Address High (SAR_HI0)—Offset 804h

NOTE: SAR_HI0 is for DMA Channel 0. The same register definition, SAR_HI1, is available for Channel 1 at address 85Ch.
SAR_HI0 (CH0): offset 804h
SAR_HI1 (CH1): offset 85Ch
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SAR_HI (SAR_HI):** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

9.4.3 DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h

NOTE: DAR_LO0 is for DMA Channel 0. The same register definition, DAR_LO1, is available for Channel 1 at address 860h.
DAR_LO0 (CH0): offset 808h
DAR_LO1 (CH1): offset 860h
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DAR_LO (DAR_LO):** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

9.4.4 DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch

NOTE: DAR_HI0 is for DMA Channel 0. The same register definition, DAR_HI1, is available for Channel 1 at address 864h.
DAR_HI0 (CH0): offset 80Ch
DAR_HI1 (CH1): offset 864h
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DAR_HI (DAR_HI):** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

9.4.5 Linked List Pointer Low (LLP_LO0)—Offset 810h

NOTE: LLP_LO0 is for DMA Channel 0. The same register definition, LLP_LO1, is available for Channel 1 at address 868h.
LLP_LO0 (CH0): offset 810h
LLP_LO1 (CH1): offset 868h
The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**LOC (LOC):** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	Reserved.

9.4.6 Linked List Pointer High (LLP_HI0)—Offset 814h

NOTE: LLP_HI0 is for DMA Channel 0. The same register definition, LLP_HI1, is available for Channel 1 at address 86Ch.
LLP_HI0 (CH0): offset 814h
LLP_LO1 (CH1): offset 86Ch
The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**LOC (LOC):** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.

9.4.7 Control Register Low (CTL_LO0)—Offset 818h

NOTE: CTL_LO0 is for DMA Channel 0. The same register definition, CTL_LO1, is available for Channel 1 at address 870h.
LLP_HI0 (CH0): offset 818h
LLP_LO1 (CH1): offset 870h
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RW	**LLP_SRC_EN (LLP_SRC_EN):** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN (LLP_DST_EN):** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	Reserved.
21:20	0h RW	**TT_FC (TT_FC):** The following transfer types are supported. 00 = Reserved 01 = Memory to Peripheral 10 = Peripheral to Memory 11 = Reserved Flow Control is always assigned to the DMA.
19	0h RO	Reserved.
18	0h RW	**DST_SCATTER_EN (DST_SCATTER_EN):** Destination scatter enable bit: 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.

Bit Range	Default and Access	Field Name (ID): Description
17	0h RW	**SRC_GATHER_EN (SRC_GATHER_EN):** Source gather enable bit: 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control
16:14	0h RW	**SRC_MSIZE (SRC_MSIZE):** Source Burst Transaction Length. Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. Source BURST SIZE (in DW) = (2 ^ SRC_TR_WIDTH) Table 24 Encoding for SRC_MSIZE and DST_MSIZE
13:11	0h RW	**DEST_MSIZE (DEST_MSIZE):** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**SINC (SINC):** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	Reserved.
8	0h RW	**DINC (DINC):** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	Reserved.
6:4	0h RW	**SRC_TR_WIDTH (SRC_TR_WIDTH):** BURST_SIZE = (2 ^ MSIZE) 1. Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
3:1	0h RW	**DST_TR_WIDTH (DST_TR_WIDTH):** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
0	0h RW	**INT_EN (INT_EN):** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

9.4.8 Control Register High (CTL_HI0)—Offset 81Ch

NOTE: CTL_HI0 is for DMA Channel 0. The same register definition, CTL_HI1, is available for Channel 1 at address 874h.
CTL_HI0 (CH0): offset 81Ch
CTL_HI1 (CH1): offset 874h
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS (CH_CLASS):** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.
28:18	0h NA	**RESERVED (RESERVED0):** Reserved
17	0h RW	**DONE (DONE):** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS (BLOCK_TS):** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register.

9.4.9 Source Status (SSTAT0)—Offset 820h

NOTE: SSTAT0 is for DMA Channel 0. The same register definition, SSTAT1, is available for Channel 1 at address 878h.
SSTAT0 (CH0): offset 820h
SSTAT1 (CH1): offset 878h
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.
Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SSTAT (SSTAT):** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

9.4.10 Destination Status (DSTAT0)—Offset 828h

NOTE: DSTAT0 is for DMA Channel 0. The same register definition, DSTAT1, is available for Channel 1 at address 880h.
DSTAT0 (CH0): offset 828h
DSTAT1 (CH1): offset 880h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.
Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DSTAT (DSTAT):** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface

9.4.11 Source Status Address Low (SSTATAR_LO0)—Offset 830h

NOTE: SSTATAR_LO0 is for DMA Channel 0. The same register definition, SSTATAR_LO1, is available for Channel 1 at address 888h.
SSTATAR_LO0(CH0): offset 830h
SSTATAR_LO1(CH1): offset 888h
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_LO (SSTATAR_LO):** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

9.4.12 Source Status Address High (SSTATAR_HI0)—Offset 834h

NOTE: SSTATAR_HI0 is for DMA Channel 0. The same register definition, SSTATAR_HI1, is available for Channel 1 at address 88Ch.
SSTATAR_HI0(CH0): offset 834h
SSTATAR_HI1(CH1): offset 88Ch
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_HI (SSTATAR_HI):** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

9.4.13 Destination Status Address Low (DSTATAR_LO0)—Offset 838h

NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_LO1, is available for Channel 1 at address 890h.
DSTATAR_LO0(CH0): offset 838h
DSTATAR_LO1(CH1): offset 890h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR_LO (DSTATAR_LO):** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

9.4.14 Destination Status Address High (DSTATAR_HI0)—Offset 83Ch

NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_HI1, is available for Channel 1 at address 894h.
DSTATAR_HI0(CH0): offset 83Ch
DSTATAR_HI1(CH1): offset 894h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR_HI (DSTATAR_HI):** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

9.4.15 DMA Transfer Configuration Low (CFG_LO0)—Offset 840h

NOTE: CFG_LO0 is for DMA Channel 0. The same register definition, CFG_LO1, is available for Channel 1 at address 898h.
CFG_LO0(CH0): offset 840h
CFG_LO1(CH1): offset 898h
This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 203h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST (RELOAD_DST):** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated
30	0h RW	**RELOAD_SRC (RELOAD_SRC):** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	Reserved.
21	0h RW	**SRC_OPT_BL (SRC_OPT_BL):** Optimize Source Burst Length: 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE))
20	0h RW	**DST_OPT_BL (DST_OPT_BL):** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE))
19	0h RW	**SRC_HS_POL (SRC_HS_POL):** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL (DST_HS_POL):** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17:11	0h RO	Reserved.
10	0h RW	**CH_DRAIN (CH_DRAIN):** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1h RO	**FIFO_EMPTY (FIFO_EMPTY):** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty

Bit Range	Default and Access	Field Name (ID): Description
8	0h RW	**CH_SUSP (CH_SUSP):** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN (SS_UPD_EN):** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0
6	0h RW	**DS_UPD_EN (DS_UPD_EN):** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN (CTL_HI_UPD_EN):** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	Reserved.
3	0h RW	**HSHAKE_NP_WR (HSHAKE_NP_WR):** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port. 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-ofblock writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR (ALL_NP_WR):** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port. 0x0 : Non-Posted Writes will only be used at end of block transfers and in HWHandshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used
1	1h RW	**SRC_BURST_ALIGN (SRC_BURST_ALIGN):** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary. 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN (DST_BURST_ALIGN):** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary. 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

9.4.16 DMA Transfer Configuration High (CFG_HI0)—Offset 844h

NOTE: CFG_HI0 is for DMA Channel 0. The same register definition, CFG_HI1, is available for Channel 1 at address 89Ch.
CFG_HI0(CH0): offset 844h
CFG_HI1(CH1): offset 89Ch
This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:18	0h RW	**WR_ISSUE_THD (WR_ISSUE_THD):** Write Issue Threshold. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD (RD_ISSUE_THD):** Read Issue Threshold. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER (DST_PER):** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface.
3:0	0h RW	**SRC_PER (SRC_PER):** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface.

9.4.17 Source Gather (SGR0)—Offset 848h

NOTE: SGR0 is for DMA Channel 0. The same register definition, SGR1, is available for Channel 1 at address 8A0h.
SGR0(CH0): offset 848h
SGR1(CH1): offset 8A0h
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RW	**SGC (SGC):** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI (SGI):** Source gather interval.

9.4.18 Destination Scatter (DSR0)—Offset 850h

NOTE: DSR0 is for DMA Channel 0. The same register definition, DSR1, is available for Channel 1 at address 8A8h.
DSR0(CH0): offset 850h
DSR1(CH1): offset 8A8h
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of

CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RW	**DSC (DSC):** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries
19:0	0h RW	**DSI (DSI):** Destination scatter interval.

9.4.19 Raw Interrupt Status (RawTfr)—Offset AC0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Raw interrupt status for ch1 and ch0

9.4.20 Raw Status for Block Interrupts (RawBlock)—Offset AC8h

RawBlock - Raw Status for Block Interrupts Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Raw interrupt status for ch1 and ch0

9.4.21 Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h

RawSrcTran - Raw Status for Source Transaction Interrupts Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Raw interrupt status for ch 1 and ch0

9.4.22 Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h

RawDstTran - Raw Status for Destination Transaction Interrupts Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Raw interrupt status for ch 1 and ch0

9.4.23 Raw Status for Error Interrupts (RawErr)—Offset AE0h

RawErr - Raw Status for Error Interrupts Register Error interrupt will be asserted by the DMA in the following cases: IOSF Fabric returns an Unsuccessful Completion with UR Completion Status for a Non-Posted transaction issued by the DMA to Memory. This error occurs when an invalid address range is programed into the DMA SRC/Dest Field outside of the Host memory region on the memory side of the DMA transaction IOSF2OCP bridge will return error (triggering error interrupt from DMA) if the IOSF2OCP Bridge is programmed incorrectly. Peripheral side trasactions where invalid addressing can result in an OCP fabric error which will be translated into an Error Interupt. The SW should view this error as a serious programming error and handle it according to the specified error handling procedures for the product and OS.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Raw interrupt status for ch1 and ch0

9.4.24 Interrupt Status (StatusTfr)—Offset AE8h

Status for Transfer Interrupts Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Status for interrtup for ch 1 and ch0

9.4.25 Status for Block Interrupts (StatusBlock)—Offset AF0h

statusBlock: Status for Block Interrupts Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Status for interrtup for ch 1 and ch0

9.4.26 Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Status for interrtup for ch 1 and ch0

9.4.27 Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Status for interrtup for ch 1 and ch0

9.4.28 Status for Error Interrupts (StatusErr)—Offset B08h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Status for interrtup for ch 1 and ch0

9.4.29 Mask for Transfer Interrupts (MaskTfr)—Offset B10h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch 1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask per ch1 and ch0 . 0-mask 1-unmask

9.4.30 Mask for Block Interrupts (MaskBlock)—Offset B18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask ch1 and ch0. 0-mask 1-unmask

9.4.31 Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask ch1 and ch0. 0-mask 1-unmask

9.4.32 Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask ch1 and ch0. 0-mask 1-unmask

9.4.33 Mask for Error Interrupts (MaskErr)—Offset B30h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask ch1 and ch0. 0-mask 1-unmask

9.4.34 Clear for Transfer Interrupts (ClearTfr)—Offset B38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

9.4.35 Clear for Block Interrupts (ClearBlock)—Offset B40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

9.4.36 Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

9.4.37 Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h

Clear for Destination Transaction Interrupts Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

9.4.38 Clear for Error Interrupts (ClearErr)—Offset B58h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

9.4.39 Combined Status register (StatusInt)—Offset B60h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is Ored to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**ERR (ERR):** OR of the contents of StatusErr register.
3	0h RO	**DSTT (DSTT):** OR of the contents of StatusDst register.

Bit Range	Default and Access	Field Name (ID): Description
2	0h RO	**SRCT (SRCT):** OR of the contents of StatusSrcTran register
1	0h RO	**BLOCK (BLOCK):** OR of the contents of StatusBlock register.
0	0h RO	**TFR (TFR):** OR of the contents of StatusTfr register.

9.4.40 DMA Configuration (DmaCfgReg)—Offset B98h

This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**DMA_EN (DMA_EN):** DMA Enable bit. 0 = DMA Disabled 1 = DMA Enabled

9.4.41 DMA Channel Enable (ChEnReg)—Offset BA0h

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority. All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Channel enable write enable.
7:2	0h RO	Reserved.
1:0	0h RW	**CH_EN (CH_EN):** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

9.5 UART PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 9-5. Summary of UART PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
220h	223h	PCI Configuration Control for UART0 (PCICFGCTR9)—Offset 220h	0h
224h	227h	PCI Configuration Control for UART1 (PCICFGCTR10)—Offset 224h	0h
228h	22Bh	PCI Configuration Control for UART2 (PCICFGCTR11)—Offset 228h	0h
22Ch	22Fh	PCI Configuration Control for UART3 (PCICFGCTR12)—Offset 22Ch	0h

9.5.1 PCI Configuration Control for UART0 (PCICFGCTR9)—Offset 220h

Controls the PCI Configuration Space

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:20	0h RW	**PCICFGCTR1 - PCI IRQ Num Field (PCI_IRQ1):** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	0h RW	**PCICFGCTR1 - ACPI IRQ Field (ACPI_IRQ1):** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message

Bit Range	Default and Access	Field Name (ID): Description
11:8	0h RW	**Interrupt Pin (IPIN1):** This register indicates the values to be used for Global Interrupts. 0 = No interrupt Pin 1 = INTA 2 = INTB 3 = INTC 4 = INTD 5 - FF: Reserved
7	0h RW	**BAR1 Disable (BAR1_DISABLE1):** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	0h RW	**PME Support (PME_SUPPORT1):** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI Interrupt Enable Field (ACPI_INTR_EN1):** When set, ACPI IRQ number field (bits 19:12) will be used for IRQ messages. When 0, PCI IRQ number field (bits 27:20) will be used for IRQ message.
0	0h RW	**PCICFGCTR1 - PCI CFG Disable Field (PCI_CFG_DIS1):** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

9.5.2 PCI Configuration Control for UART1 (PCICFGCTR10)—Offset 224h

Same definition as PCICFGCTR9.

9.5.3 PCI Configuration Control for UART2 (PCICFGCTR11)—Offset 228h

Same definition as PCICFGCTR9.

9.5.4 PCI Configuration Control for UART3 (PCICFGCTR12)—Offset 22Ch

Same definition as PCICFGCTR9.

10 Intel® Trace Hub

10.1 Intel® Trace Hub Configuration Registers Summary

Table 10-1. Summary of Intel® Trace Hub Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Vendor ID (VID)—Offset 0h	XXXX8086h
4h	7h	Command (CMD)—Offset 4h	100000h
8h	Bh	Revision ID (RID)—Offset 8h	130000XXh
Ch	Fh	Header Type (HT)—Offset Ch	0h
10h	13h	Trace Buffer Lower BAR (MTB_LBAR)—Offset 10h	4h
14h	17h	Trace Buffer Upper BAR (MTB_UBAR)—Offset 14h	0h
18h	1Bh	Software Lower BAR (SW_LBAR)—Offset 18h	4h
1Ch	1Fh	Software Upper BAR (SW_UBAR)—Offset 1Ch	0h
20h	23h	RTIT Lower BAR (RTIT_LBAR)—Offset 20h	4h
24h	27h	RTIT Upper BAR (RTIT_UBAR)—Offset 24h	0h
2Ch	2Fh	Subsystem Vendor ID (SVID)—Offset 2Ch	0h
34h	37h	Capabilities Pointer (CAP)—Offset 34h	40h
3Ch	3Fh	Interrupt Line (INTL)—Offset 3Ch	1FFh
40h	43h	MSI Capability ID (MSICID)—Offset 40h	860000h
44h	47h	MSI Lower Message Address (MSILMA)—Offset 44h	0h
48h	4Bh	MSI Upper Message Address (MSIUMA)—Offset 48h	0h
4Ch	4Fh	MSI Message Data (MSIMD)—Offset 4Ch	0h
70h	73h	Firmware Lower Bar (FW_LBAR)—Offset 70h	4h
74h	77h	Firmware Upper Bar (FW_UBAR)—Offset 74h	0h
80h	83h	Device Specific Control (NPKDSC)—Offset 80h	0h
B4h	B7h	Power Control Enable Register (DEVIDLEPCE)—Offset B4h	8h

10.1.1 Vendor ID (VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 9638086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	963h RO	**DID:** The value that uniquely identifies the Intel Trace Hub.
15:0	8086h RO	**Vendor ID (VID):** 8086 is Intel Vendor Identification code.

10.1.2 Command (CMD)—Offset 4h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 31

Function: 7

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	0h RW/1C	**Signaled System Error (SSE):** This bit is set when the device has detected an un-correctable error and reported it via SERR message over sideband. This requires SERR Enable bit to be set in Command register.
29	0h RW/1C	**Received Master Abort Status (RMA):** This bit is set when device receives a Completion transaction with Unsupported Request completion status. No error will be reported.
28	0h RW/1C	**Received Target Abort Status (RTA):** This bit is set when device receives a Completion transaction with Completer Abort completion status. No error will be reported
27	0h RW/1C	**Signaled Target Abort Status (STA):** Set by the device when aborting a request that violates the device programming model. When SERR Enable is set SERR message will be send over sideband.
26:25	0h RO	Reserved.
24	0h RW/1C	**MDPE:** Master Data Parity Error
23:21	0h RO	Reserved.
20	1h RO	**Capabilities List (CLIST):** Indicates the controller contains a capabilities pointer list and the capability pointer register is implemented at offset 0x40 in the configuration space
19	0h RO	**Interrupt Status (INSTAT):** Reflects the state of the interrupt pin at the input of the enable/disable circuit. When the interrupt is asserted, and cleared when the interrupt is cleared (independent of the state of Interrupt Disable bit in command register. This bit is only associated with the INTx messages and has no meaning if the device is using MSI.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (IntDis):** Disables the function to generate INTx interrupt. A value of 0 enables the function to generate INTA messages on IOSF sideband. Note: this bit has no effect on MSI generation.
9	0h RO	Reserved.
8	0h RW	**System Error Enable (SERREn):** Setting this bit enables the generation of System Error message, when required through sideband interface.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6	0h RW	**PERE:** Parity Error Response Enable
5:3	0h RO	Reserved.
2	0h RW	**Bus Master Enable (BME):** When set enables the ability to issue Memory or IO requests, including MSI.
1	0h RW	**Memory Space Enable (MEM):** When set, Memory Space Decoding is enabled and memory transactions targeting the device are accepted. Note: The MSE has to be set to accept any memory transaction on the primary interface targeting any of Trace Hub's BARs.
0	0h RO	Reserved.

10.1.3 Revision ID (RID)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 13000001h

Bit Range	Default & Access	Field Name (ID): Description
31:8	130000h & RO	**Class Code (Class):** Class Code
7:0	1h & RO	**Revision ID (RID):** Indicates the device specific revision identifier.

10.1.4 Header Type (HT)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:16	0h RO	**Header Type (HT):** Implements a Type 0 configuration header
15:0	0h RO	Reserved.

10.1.5 Trace Buffer Lower BAR (MTB_LBAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Lower Base Address (ADDR):** Lower programmable Base Address.
19:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PF):** Value of 0 indicates the BAR cannot be prefetched.
2:1	2h RO	**Address Range (ADRNG):** Value of 0x2 indicates that the BAR is located anywhere system memory space (i.e. 64-bit addressing)
0	0h RO	**Space Type (SPTY):** Value of 0 indicates the BAR is located in memory space.

10.1.6 Trace Buffer Upper BAR (MTB_UBAR)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Upper Base Address (ADDR):** Upper programmable Base Address.

10.1.7 Software Lower BAR (SW_LBAR)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RW	**Lower Base Address (ADDR):** Lower programmable Base Address.
22:4	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Prefetchable (PF):** Value of 0 indicates the BAR cannot be prefetched.
2:1	2h RO	**Address Range (ADRNG):** Value of 0x2 indicates that the BAR is located anywhere system memory space (i.e. 64-bit addressing)
0	0h RO	**Space Type (SPTY):** Value of 0 indicates the BAR is located in memory space

10.1.8 Software Upper BAR (SW_UBAR)—Offset 1Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Upper Base Address (ADDR):** Upper programmable Base Address.

10.1.9 RTIT Lower BAR (RTIT_LBAR)—Offset 20h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RW	**Lower Base Address (ADDR):** Lower Base Address: Lower programmable Base Address
13:4	0h RO	Reserved.
3	0h RO	**PF:** Prefetchable: Value of 0 indicates the BAR cannot be prefetched
2:1	2h RO	**TYPE:** Address Range: Value of 0x2 indicates that the BAR is located anywhere system memory space (i.e. 64-bit addressing)
0	0h RO	**MEM:** Space Type: Value of 0 indicates the BAR is located in memory space

10.1.10 RTIT Upper BAR (RTIT_UBAR)—Offset 24h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Upper Base Address (ADDR):** Upper Base Address: Upper programmable Base Address

10.1.11 Subsystem Vendor ID (SVID)—Offset 2Ch

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Subsystem ID (SID):** Writable only once
15:0	0h RW	**Subsystem Vendor ID (SVID):** Be set once by BIOS then becomes RO.

10.1.12 Capabilities Pointer (CAP)—Offset 34h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 7

Default: 40h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	40h RO	**Capability Pointer: (CAPPTR):** Pointer to first capability structure at 40h.

10.1.13 Interrupt Line (INTL)—Offset 3Ch

Access Method

Type: CFG Register (Size: 32 bits)
Device: 31
Function: 7

Default: 1FFh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	1h RW/O	**Interrupt Pin (INTPIN):** Trace Hub uses a single INTx interrupt bonded to INTA.
7:0	FFh RW	**Interrupt Line (INTL):** Hardware does not use this field. Rather it is programmed by system software and device drivers to communicate interrupt line routing information.

10.1.14 MSI Capability ID (MSICID)—Offset 40h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 860000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**Multiple Message Capable (AC64b):** Value of 0 indicates the device only support single interrupt message.
22:20	0h RW	**MSI Enable (MME):** If set, MSI is enabled and the legacy interrupts messages (over IOSF sideband) will not be generated
19:17	3h RO	**MSI Next Capability Pointer (MMC):** Value of 0 indicates there are no further capabilities (i.e. the capability linked list is ended)
16	0h RW	**MSI Capability ID (MSIE):** MSI Capability ID with a value of 05h indicating the presence of the MSI capability register set
15:8	0h RO	**64-bit Address Capable (MSINCP):** Trace Hub is capable of generating 64-bit memory addresses
7:0	0h RO	Reserved.

10.1.15 MSI Lower Message Address (MSILMA)—Offset 44h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**MSI Message Lower Address (MSILMA):** Lower 32-bits of system software assigned message address to the device with bits[1:0] always cleared indicating message address has to always be DW aligned.
1:0	0h RO	Reserved.

10.1.16 MSI Upper Message Address (MSIUMA)—Offset 48h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**MSI Message Upper Address (MSIUMA):** Upper 32 bits of system software assigned message address to the device.

10.1.17 MSI Message Data (MSIMD)—Offset 4Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**MSI Message Data (MSIMD):** 16 bit message data pattern assigned by the system software to the device. When MSI is generated the actual data is 32 bit and the upper 16 bits are always 0.

10.1.18 Firmware Lower Bar (FW_LBAR)—Offset 70h

Firmware Lower Bar

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RW	**ADDR:** Lower Base Address: Lower programmable Base Address
20:4	0h RO	Reserved.
3	0h RO	**PF:** Prefetchable: Value of 0 indicates the BAR cannot be prefetched
2:1	2h RO	**TYPE:** Address Range: Value of 0x2 indicates that the BAR is located anywhere system memory space (i.e. 64-bit addressing)
0	0h RO	**MEM:** Space Type: Value of 0 indicates the BAR is located in memory space

10.1.19 Firmware Upper Bar (FW_UBAR)—Offset 74h

Firmware Upper Bar

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**UADDR:** Upper Base Address: Upper programmable Base Address

10.1.20 Device Specific Control (NPKDSC)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10	0h RW/1C	**Unsupported Request Detect (URD):** This bit is set when an unsupported request is detected.
9:4	0h RO	Reserved.
3	0h RW	**Unsupported Request Reporting Enable (URRE):** When set, this bit enables the reporting unsupported requests as system errors
2	0h RW/1C	**Capture Done Interrupt Status (CDINTS):** Formerly Legacy Interrupt Asserted. Equivalent to MSUSTS.MSU_INT, for software compatibility. This this bit indicates when the capture done event has occurred. Software can clear the capture done interrupt event by writing a 1 to this bit, or writing a 1 to the MSUSTS.MSU_INT bit
1	0h RW	**Software Reset: (FLR):** Writing a 1 to this bit will assert the reset signals. Reading this bit will always return a zero.
0	0h RO	Reserved.

10.1.21 Power Control Enable Register (DEVIDLEPCE)—Offset B4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 31
Function: 7

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	1h RW	**Sleep Enable (SE):** If clear, Trace Hub will never assert sleep. If set, it will assert sleep during power gating
2	0h RO	Reserved.
1	0h RO	**Device Idle Enable (DEVIDLEN):** It set, Trace Hub will power gate when idle and D0I3C[2] is programmed to 1h (D0I3C[2] = 0x1)
0	0h RO	Reserved.

11 Generic SPI Interface (D30:F2/F3 and D18:F6)

11.1 GSPI PCI Configuration Registers Summary

Table 11-1. Summary of GSPI PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID (DEVVENDID)—Offset 0h	XXXX8086h
4h	7h	Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	Revision ID and Class Code (REVCLASSCODE)—Offset 8h	78000XXh
Ch	Fh	Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	800000h
10h	13h	Base Address (BAR)—Offset 10h	4h
14h	17h	Base Address High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	Base Address High (BAR1)—Offset 18h	4h
1Ch	1Fh	Base Address 1 High (BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
30h	33h	EXPANSION ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	Interrupt (INTERRUPTREG)—Offset 3Ch	0h
80h	83h	Power Management Capability ID (POWERCAPID)—Offset 80h	39001h
84h	87h	Power Management Control and Status (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	SW LTR Update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	2101h
9Ch	9Fh	Device IDLE Pointer (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	24C1h
A0h	A3h	Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	F0800h
B0h	B3h	General Purpose Read Write 1 (GEN_REGRW1)—Offset B0h	0h
B4h	B7h	General Purpose Read Write 2 (GEN_REGRW2)—Offset B4h	0h
B8h	BBh	General Purpose Read Write 3 (GEN_REGRW3)—Offset B8h	0h
BCh	BFh	General Purpose Read Write 4 (GEN_REGRW4)—Offset BCh	0h
C0h	C3h	General Purpose Input (GEN_INPUT_REG)—Offset C0h	0h

11.1.1 Device ID and Vendor ID (DEVVENDID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: XXXX8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	-- RO/P	**Device ID Field (DEVICEID):** This is a 16-bit value assigned to the controller. See the Device and Revision ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor ID Field (VENDORID):** Identifies the manufacturer of the device. 8086h = Intel.

11.1.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 100000h

Bit Range	Default and Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**RMA Field (RMA):** S/W writes a '1' to this bit to clear it.
28	0h RW/1C	**RTA Field (RTA):** S/W writes a '1' to this bit to clear it.
27:21	0h RO	Reserved.
20	1h RO	**Cap List Field (CAPLIST):** Indicates that the controller contains a capabilities pointer list.
19	0h RO	**Intrerrupt Status Field (INTR_STATUS):** This bit reflects state of interrupt in the device.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Setting this bit disables INTx assertion. The interrupt disabled is legacy INTx# interrupt. This bit has no connection with interrupt status bit.
9	0h RO	Reserved.
8	0h RW	**SERR Enable Field (SERR_ENABLE):** Not implemented.
7:3	0h RO	Reserved.
2	0h RW	**BME Field (BME):** If this bit is 0, the controller does not generate any new upstream transaction as a master.
1	0h RW	**MSE Field (MSE):** 0 = Disables memory mapped Configuration space. 1 = Enables memory mapped Configuration space.
0	0h RO	Reserved.

11.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 78000XXh

Bit Range	Default and Access	Field Name (ID): Description
31:8	78000h RO	**Class Code (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	-- RO/P	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

11.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 800000h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**MultiFunction Device Field (MULFNDEV):** 0 = Single Function Device 1 = Multi Function device.
22:16	0h RO	**Header Type Field (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	0h RO	**Latency Timer Field (LATTIMER):** Hardwired to 0.
7:0	0h RW/P	**Cache Line Size Field (CACHELINE_SIZE)**

11.1.5 Base Address (BAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW	**Base Address Field (BASEADDR):** Provides system memory base address for the controller.
11:4	0h RO	**Size Field (SIZEINDICATOR):** Always returns 0. The size of this register depends on the size of the memory space.
3	0h RO	**Prefetchable Field (PREFETCHABLE):** 0 indicates that this BAR is not prefetchable.
2:1	2h RO	**Type Field (TYPE):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** 0 indicates this BAR is present in the memory space.

11.1.6 Base Address High (BAR_HIGH)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address High Field (BASEADDR_HIGH)**

11.1.7 Base Address High (BAR1)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW	**Base Address Field (BASEADDR1):** This field is present if BAR1 is enabled.
11:4	0h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** 0 indicates that this BAR is not prefetchable.
2:1	2h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** 0 Indicates this BAR is present in the memory space.

11.1.8 Base Address 1 High (BAR1_HIGH)—Offset 1Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address High Field (BASEADDR1_HIGH)**

11.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** The register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other. This register is a Read Write Once type register.
15:0	0h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** The register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

11.1.10 EXPANSION ROM Base Address (EXPANSION_ROM_BASEADDR)—Offset 30h

EXPANSION ROM base address register is a RO indicates support for expansion ROMs

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO	**EXPANSION ROM base address field (EXPANSION_ROM_BASE):** Expansion ROM Base Address: Value of all zeros indicates no support for Expansion ROM

11.1.11 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Capabilities Pointer register indicates what the next capability is

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Indicates what the next capability is.

11.1.12 Interrupt (INTERRUPTREG)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**Min Gnt Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma
15:12	0h RO	Reserved.
11:8	0h RO	**Interrupt Pin Field (INTPIN)**
7:0	0h RW/P	**Int Line Field (INTLINE):** It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

11.1.13 Power Management Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 39001h

Bit Range	Default and Access	Field Name (ID): Description
31:27	0h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for for a bit indicates that the function is not capable of asserting the PME# signal while in that power state. Bit 27 = 1: PME# can be asserted from D0. Bit 30 = 1: PME# can be asserted from D3 hot. Other bits are not used.
26:19	0h RO	Reserved.
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**Next Cap Field (NXTCAP):** Points to the next capability structure.
7:0	1h RO	**Power Capability ID Field (POWER_CAP):** Indicates power management capability.

11.1.14 Power Management Control and Status (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C/P	**PME Status Field (PMESTATUS)**
14:9	0h RO	Reserved.
8	0h RW/P	**PME Enable Field (PMEENABLE):** 0 = PME message is disabled 1 = PME message is enabled.
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	Reserved.
1:0	0h RW	**Power State Field (POWERSTATE):** This field is used both to determine the current power state and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field,the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked.

11.1.15 PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: F0140009h

Bit Range	Default and Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision IDField (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	0h RO	**Next Capability Field (NEXT_CAP):** Points to the next capability structure. This points to NULL.
7:0	9h RO	**Capability ID Field (CAPID)**

11.1.16 Vendor Specific Extended Capability Register (DEVID_VEND_SPECIFIC_REG)—Offset 94h

Extended Vendor capability register for VSEC Length revision and ID

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 1400010h

Bit Range	Default and Access	Field Name (ID): Description
31:20	14h RO	**Vendor Specific ID Field (VSEC_LENGTH):** Vendor Specific Extended Capability Length
19:16	0h RO	**Vendor Specific Revision Field (VSEC_REV):** Vendor specific Extended Capability revision
15:0	10h RO	**Vendor Specific Length Field (VSECID):** Vendor Specific Extended Capability ID

11.1.17 SW LTR Update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Software location pointer in MMIO space as an offset specified by BAR

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 2101h

Bit Range	Default and Access	Field Name (ID): Description
31:4	210h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR BAR Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	1h RO	**SW LTR Valid Field (SW_LAT_VALID)**

11.1.18 Device IDLE Pointer (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset location BAR NUM and D0i3 Valid Strap

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 24C1h

Bit Range	Default and Access	Field Name (ID): Description
31:4	24Ch RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** Indicates that the D0i3 MMIO location is always at BAR0.
0	1h RO	**D0i3 Valid Field (VALID):** 0 = Not valid 1 = Valid

11.1.19 Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: F0800h

Bit Range	Default and Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/P	**HAE Field (HAE)**
20	0h RO	Reserved.
19	1h RW/P	**Sleep Enable Field (SLEEP_EN)**
18	1h RW/P	**D3 Hen Field (PGE):** If clear, the controller will never request a PG. If 1, then the function will power gate when idle and the DevIdle bit is set.
17	1h RW/P	**Device Idle En Field (I3_ENABLE):** If 1, then function will power gate when idle and the POWERSTATE bits in the function = 11 (D3).
16	1h RW/P	**PMC Request Enable Field (PMCRE):** If this bit is set to '1', the function will power gate when idle.
15:13	0h RO	Reserved.
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** This value is written by BIOS to communicate to the Driver.
9:0	0h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** This value is written by BIOS to communicate to the Driver.

11.1.20 General Purpose Read Write 1 (GEN_REGRW1)—Offset B0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW1):** General purpose read write PCI register.

11.1.21 General Purpose Read Write 2 (GEN_REGRW2)—Offset B4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW2):** General purpose read write PCI register.

11.1.22 General Purpose Read Write 3 (GEN_REGRW3)—Offset B8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW3):** General purpose read write PCI register.

11.1.23 General Purpose Read Write 4 (GEN_REGRW4)—Offset BCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW4):** General purpose read write PCI register.

11.1.24 General Purpose Input (GEN_INPUT_REG)—Offset C0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 30
Function: 1

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General Purpose Input Register.

11.2 Generic SPI (GSPI) Memory Mapped Registers Summary

Table 11-2. Summary of Generic SPI (GSPI) Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	SSP (GSPI) Control Register 0 (SSCR0)—Offset 0h	0h
4h	7h	SSP (GSPI) Control Register 1 (SSCR1)—Offset 4h	0h
8h	Bh	SSP (GSPI) Status Register (SSSR)—Offset 8h	4h
10h	13h	SSP (GSPI) Data (SSDR)—Offset 10h	0h
28h	2Bh	SSP (GSPI) Time Out (SSTO)—Offset 28h	0h
44h	47h	REG SITF (SITF)—Offset 44h	0h
48h	4Bh	REG SIRF (SIRF)—Offset 48h	0h

11.2.1 SSP (GSPI) Control Register 0 (SSCR0)—Offset 0h

All bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**MOD (MOD):** Mode Set to 0 - Normal SSP Mode : Full Duplex Serial peripheral interface. 1 = reserved
30	0h RW	**ACS (ACS):** Set to 0 for Clock selection which is determined by the NCS and ECS bits in this register. 1 = reserved
29:24	0h RO	Reserved.
23	0h RW	**TIM (TIM):** Transmit FIFO Under Run Interrupt Mask When set, this bit will mask the Transmit FIFO Under Run (TUR) event from generating an SSP interrupt. The SSSR status register will still indicate that an TUR event has occurred. This bit can be written to at any time (before or after SSP is enabled). 0 = Transmit FIFO Under Run(TUR) events will generate an SSP interrupt 1 = TUR events will be masked
22	0h RW	**RIM (RIM):** Receive FIFO Over Run Interrupt Mask When set, this bit will mask the Receive FIFO Over Run (ROR) event from generating an SSP interrupt. The SSSR status register will still indicate that an ROR event has occurred. This bit can be written to at any time (before or after SSP is enabled) 0 = receive FIFO Over Run(ROR) events will generate an SSP interrupt 1 = ROR events will be masked
21	0h RW	**NCS (NCS):** Network Clock Select The SSCR0.NCS bit in conjunction with SSCR0.ECS determines which clock is used. 0 - Clock selection is determined by ECS bit 1 – Reserved

Bit Range	Default and Access	Field Name (ID): Description
20	0h RW	**EDSS (EDSS):** Extended Data Size Select The 1-bit extended field is used in conjunction with the data size select SSCR0.DSS bits to select the size of the data transmitted and received by the Enhanced SSP. 0 = A zero is prepended to the DSS value which sets the DSS range from 4-16 bits 1 = A one is pre-appended to the DSS value which sets the DSS range from 17-32 bits
19:8	0h RW	**SCR (SCR):** Serial Clock Rate Value used to generate transmission rate of SSP. Note: The SPI Interface Controller (SSP) baud rate (or Serial bit-rate clock SPI_CLK_OUT) can be generated either by the M/N divider or internally to the SSP (SSCR0.SCR) by dividing the on-chip SSP_CLK (output of M/N) to generate baud rates
7	0h RW	**SSE (SSE):** Synchronous Serial Port Enable The SSP enable bit, SSCR0.SSE, enables and disables all SSP operations. When SSCR0.SSE=0, the Enhanced SSP is disabled; when SSCR0.SSE=1, it is enabled. When the Enhanced SSP is disabled, all of its clocks can be stopped by programmers to minimize power consumption. On reset, the Enhanced SSP is disabled. When the SSCR0.SSE bit is cleared during active operation, the Enhanced SSP is disabled immediately, terminating the current frame being transmitted or received. Clearing SSCR0.SSE resets the Enhanced SSP FIFOs and the Enhanced SSP status bits; however, the Enhanced SSP Control registers are not reset. Note: After reset or after clearing the SSCR0.SSE, users must ensure that the SSCR1, SSITR and SSTO control registers are properly re-configured and that the SSSR register is reset before re- enabling the Enhanced SSP with the SSCR0.SSE. Also, the SSCR0.SSE bit must be cleared before reconfiguring the SSCR0, SSCR1, registers; other control bits in SSCR0 can be written at the same time as the SSCR0.SSE. When any SSP is disabled, its five pins can be used as GPIOs. 0 = SSP operation disabled 1 = SSP operation enabled.
6	0h RW	**ECS (ECS):** External Clock Select: 0 = use On-chip clock (output of M/N Divider) to produce the SSP's serial clock (SSPSCLK). Selects the use of the the output of the M/N Divider (MBAR0 + 0x800, CLOCKS) to create the SSP's serial clock (SSPCLK) Note: Setting M=N=1 will provide a pass through of the M/N Divider of the serial clock. See SCR for Serial Clock Rate generation. 1 = Reserved
5:4	0h RW	**FRF (FRF):** Frame Format Set to 00 - Motorola Serial Peripheral Interface (SPI) 01 - 10 = reserved
3:0	0h RW	**DSS (DSS):** Data Size Select With EDSS as MSB. The CPU or DMA access data through the Enhanced SSP Ports Transmit and Receive FIFOs. A CPU access takes the form of programmed I/O, transferring one FIFO entry per access. CPU accesses would normally be triggered off of an SSSR Interrupt and must always be 32 bits wide. CPU Writes to the FIFOs are 32 bits wide, but the serializing logic will ignore all bits beyond the programmed FIFO data size (EDSS/DSS value). CPU Reads to the FIFOs are also 32 bits wide, but the Receive data written into the RX FIFO (from the RXD line) is stored with zeroes in the MSBs down to the programmed data size. The FIFOs can also be accessed by DMA Single transactions, which must be 1, 2 or 4 bytes, depending upon the EDSS value, and must also transfer one FIFO entry per access. When the SSCR0.EDSS bit is set, DMA Single transactions must be 4 bytes (the DMA must have the Enhanced SSP configured as a 32-bit peripheral).The DMAs _TR.width register must be at least the SSP data size programmed into the SSP control registers EDSS and DSS. The FIFO is seen as one 32-bit location by the processor. For Writes, the Enhanced SSP port takes the data from the Transmit FIFO, serializes it, and sends it over the serial wire (SSPTXD) to the external peripheral. Receive data from the external peripheral (on SSPRXD) is converted to parallel words and stored in the Receive FIFO. A programmable FIFO trigger threshold, when exceeded, generates an Interrupt or DMA service request that, if enabled, signals the CPU or DMA respectively to empty the Receive FIFO or to refill the Transmit FIFO. The Transmit and Receive FIFOs are differentiated by whether the access is a Read or a Write transfer. Reads automatically target the Receive FIFO, while Writes will write data to the Transmit FIFO. From a memory-map perspective, they are at the same address. FIFOs are 64 samples deep by 32 bits wide. Each read or write is to 1 SSP sample. The 4-bit Data Size Select SSCR0.DSS field is used in conjunction with the extended data size select SSCR0.EDSS bit to select the size of the data transmitted and received by the Enhanced SSP. The concatenated 5-bit value of SSCR0.EDSS and SSCR0.DSS provides a data range from 4 to 32 bits in length. Note: When data is programmed to be less than 32 bits, the FIFO should be programmed right-justified. Although it is possible to program data sizes of 1, 2, and 3 bits, these sizes are reserved and produce unpredictable results in the Enhanced SSP. 0011 4 bits 0111 8 bits 1111 16, 32 bits (Note: To differentiate between 16 bits and 32 bits check the EDSS bit, for 32 bit data EDSS = 1)

11.2.2 SSP (GSPI) Control Register 1 (SSCR1)—Offset 4h

The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP. Note that Writes to reserved bits should be zeroes, and Read value of these bits are undetermined.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**RWOT (RWOT):** Receive With Out Transmit 0 = Transmit/Receive mode 1 = Receive without transmit mode
22	0h RW	**TRAIL (TRAIL):** Trailing Byte 0 = Processor based, trailing bytes are handled by processor 1 - DMA based, trailing bytes are handled by DMA
21	0h RW	**TSRE (TSRE):** Transmit Service Request Enable 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
20	0h RW	**RSRE (RSRE):** Receive Service Request Enable 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	0h RW	**TINTE (TINTE):** Receive FIFO Time-out Interrupt Enable The SSCR1.TINTE is a read-write bit used to mask or enable the Receiver Time-out Interrupt. When SSCR1.TINTE=0, the Interrupt is masked and the state of the SSSR.TINT bit is ignored by the Interrupt controller. When SSCR1.TINTE=1, the Interrupt is enabled, and whenever the SSSR.TINT bit is set to one an Interrupt request is made to the Interrupt controller. Note that programming SSCR1.TINTE=0 does not affect the current state of the SSSR.TINT or the ability of logic to set and clear the SSSR.TINT; it only blocks the generation of the Interrupt request. 0 = Receiver Time-out interrupts are disabled 1 = Receiver Time-out interrupts are enabled
18:17	0h RO	Reserved.
16	0h RW	**IFS (IFS):** Invert Frame Signal 0 = Frame signal (Chip Select) is active low 1 = Frame signal (Chip Select) is active high
15:5	0h RO	Reserved.
4	0h RW	**SPH (SPH):** Motorola SPI SSPSCLK phase setting 0 = SSPSCLK is inactive one sycle at the start of a frame and cycle at the end of a frame 1 = SSPSCLK is inactive for one half cycle at the start of a frame and one cycle at the end of a frame
3	0h RW	**SPO (SPO):** Motorola SPI SSPSCLK polarity setting 0 = The inactive or idle state of SSPSCLK is low 1 = The inactive or idle state of SSPSCLK is high
2	0h RO	Reserved.
1	0h RW	**TIE (TIE):** Transmit FIFO Interrupt Enable 0 = Transmit FIFO level interrupt is disabled 1 = Transmit FIFO level interrupt is enabled
0	0h RW	**RIE (RIE):** Receive FIFO Interrupt Enable 0 = Receive FIFO level interrupt is disabled 1 = Receive FIFO level interrupt is enabled

11.2.3 SSP (GSPI) Status Register (SSSR)—Offset 8h

The Enhanced SSP Status registers contain bits that signal overrun errors as well as the Transmit and Receive FIFO service requests. Each of these hardware-detected events signals an Interrupt request to the Interrupt controller. The Status register also contains flags that indicate when the Enhanced SSP is actively transmitting data, when the Transmit FIFO is not full, and when the Receive FIFO is not empty. One Interrupt

signal is sent to the Interrupt Controller for each SSP. These events can cause an Interrupt: End-of-Chain, Receiver Time-out, Peripheral Trailing Byte, Receive FIFO overrun, Receive FIFO request, and Transmit FIFO request

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/1C	**TUR (TUR):** Transmit FIFO Under Run 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	0h RO	Reserved.
19	0h RW/1C	**TINT (TINT):** Receiver Time-out Interrupt 0 = No receiver time-out pending 1 = Receiver time-out pending
18	0h RW/1C	**PINT (PINT):** Peripheral Trailing Byte Interrupt 0 - No peripheral trailing byte interrupt pending 1 - Peripheral trailing byte interrupt pending
17:8	0h RO	Reserved.
7	0h RW/1C	**ROR (ROR):** Receive FIFO Overrun 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	0h RO	**RFS (RFS):** Receive FIFO Service Request 0 = Receive FIFO level is at or below RFT threshold (RFT), or SSP disabled 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	0h RO	**TFS (TFS):** Transmit FIFO Service Request 0 = Transmit FIFO level exceeds the Low Water Mark Transmit FIFO (SITF.LWMTF), or SSP disabled 1 = Transmit FIFO level is at or below the Low Water Mark Transmit FIFO (SITF.LWMTF), request interrupt
4	0h RO	**BSY (BSY):** SSP Busy 0 = SSP is idle or disabled 1 = SSP currently transmitting or receiving a frame
3	0h RO	**RNE (RNE):** Receive FIOF Not Empty 0 = Receive FIFO is empty 1 = Receive FIFO is not empty
2	1h RO	**TNF (TNF):** Transmit FIFO Not Full 0 = Transmit FIFO is full 1 = Transmit FIFO is not full
1:0	0h RO	Reserved.

11.2.4 SSP (GSPI) Data (SSDR)—Offset 10h

The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DATA (DATA):** Data word to be written to/read from transmit/receive FIFO

11.2.5 SSP (GSPI) Time Out (SSTO)—Offset 28h

The Enhanced SSP Time-Out registers have single bit fields that specify the time-out value used to signal a period of inactivity within the Receive FIFO. Note that Writes to reserved bits must be zeroes, and Read value of these bits are undetermined.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**TIMEOUT (TIMEOUT):** Timeout Value Is the value that defines the timeout interval for the rcv FIFO. The Interval is given by TIMEOUT/Parallel (Bus) Clock Frequency. When the number of samples in the Receive FIFO is less than rcv FIFO trigger threshold level, and no additional data is received, the Timeout timer will decrement. The time-out timer is reset after a new sample is received. In DMA Mode of operation this value needs to be set when the Rcv FIFO Trigger Threshold is greater than 1 Rcv FIFO Entry (the required MSize (Single Burst) for SSP DMA peripheral transfers) When in PIO mode of operation this value needs to be set when the total transfer size is not a even divison of the Rcv FIFO trigger threshold level. Is such a case the TIMEOUT value is calculated to be greater than the time to transfer the FIFO Entry size at the desired Bit Rate.

11.2.6 REG SITF (SITF)—Offset 44h

The SPI Transmit FIFO register is for writing the water mark for the SPI transmit FIFO and also for reading the number of entries in the SPI transmit FIFO

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21:16	0h RO	**SITFL (SITFL):** SPI Transmit FIFO Level Number of entries in SPI Transmit FIFO.
15:14	0h RO	Reserved.
13:8	0h RW	**LWMTF (LWMTF):** Low Water Mark Transmit FIFO. Set the low water mark of the SPI transmit FIFO. 6'b000000 = 1 entry through 6'b111111 = 64 entries
7:6	0h RO	Reserved.
5:0	0h RW	**HWMTF (HWMTF):** High Water Mark Transmit FIFO. Set the high water mark of the SPI transmit FIFO. 6'b000000 = 1 entry through 6'b111111 = 64 entries

11.2.7 REG SIRF (SIRF)—Offset 48h

The SPI Receive FIFO register is for writing the water mark for the SPI receive FIFO and also for reading the number of entries in the SPI receive FIFO

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:8	0h RO	**SIRFL (SIRFL):** SPI Receive FIFO Level Number of entries in SPI Receive FIFO.
7:6	0h RO	Reserved.
5:0	0h RW	**WMRF (WMRF):** Water Mark Receive FIFO. Set the water mark of the SPI receive FIFO. 6'b000000 = 1 entry through 6'b111111 = 64 entries

11.3 Generic SPI (GSPI) Additional Registers Summary

The registers in this section are memory mapped based on the BAR defined in PCI configuration space.

Table 11-3. Summary of Generic SPI (GSPI) Additional Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
200h	203h	Clocks (CLOCKS)—Offset 200h	0h
204h	207h	Resets (RESETS)—Offset 204h	0h
210h	213h	Active LTR (ACTIVELTR_VALUE)—Offset 210h	800h
214h	217h	Idle LTR Value (IDLELTR_VALUE)—Offset 214h	800h
218h	21Bh	TX Bit Count (TX_BIT_COUNT)—Offset 218h	0h
21Ch	21Fh	Rx Bit Count (RX_BIT_COUNT)—Offset 21Ch	0h
220h	223h	REG SSP_REG (SSP_REG)—Offset 220h	0h
224h	227h	GSPI CS Control (SPI_CS_CONTROL)—Offset 224h	3000h
228h	22Bh	SW Scratch 0 (SW_SCRATCH)—Offset 228h	0h
22Ch	22Fh	SW Scratch 1 (SW_SCRATCH_1)—Offset 22Ch	0h
230h	233h	SW Scratch 2 (SW_SCRATCH_2)—Offset 230h	0h
234h	237h	SW Scratch 3 (SW_SCRATCH_3)—Offset 234h	0h
238h	23Bh	Clock Gate (CLOCK_GATE)—Offset 238h	0h
240h	243h	Remap Address Low (REMAP_ADDR_LO)—Offset 240h	0h
244h	247h	Remap Address High (REMAP_ADDR_HI)—Offset 244h	0h
24Ch	24Fh	Device Idle Control (DEVIDLE_CONTROL)—Offset 24Ch	8h
250h	253h	Delay Rx Clock (DEL_RX_CLK)—Offset 250h	0h
2FCh	2FFh	Capabilities (CAPABLITIES)—Offset 2FCh	620h

11.3.1 Clocks (CLOCKS)—Offset 200h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**Clock Update (clk_update):** Update the clock divider after seeing new m and n values 0 = No clock Update. 1 – Clock gets updated.
30:16	0h RW	**N Value (n_val):** This is the denominator value (N) for the M over N divider logic that creates the SPI_ CLK_OUT for the SSP.Used to generate the input clk to SSP.
15:1	0h RW	**M Value (m_val):** The numerator value (M) for the M over N divider logic that creates the SPI_CLK_OUT for the SSP.Used to generate the input clk to SSP.
0	0h RW	**Clock Enable (clk_en):** Clock Enable of the m over n divider 0 = Clock disabled 1 = Clock Enabled.

11.3.2 Resets (RESETS)—Offset 204h

software reset

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**DMA Reset (reset_dma):** DMA Software Reset Control 0 = DMA is in reset (Reset Asserted) 1 = DMA is NOT at reset (Reset Released)
1:0	0h RW	**Controller Reset (reset_ip):** Used to reset the GSPI Host Controller by SW control. All GSPI Configuration State and Operational State will be forced to the Default state. There is no timing requirement (SW can assert and de-assert in back to back transactions. Driver should re-initialize registers related to Driver context following a controller reset. 00 = Host Controller is in reset 01 = Reserved 10 = Reserved 11 = Host Controller is NOT at reset.

11.3.3 Active LTR (ACTIVELTR_VALUE)—Offset 210h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 800h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Snoop Requirement (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**Snoop Latency Scale (snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop Value (snoop_value):** 10-bit latency value

11.3.4 Idle LTR Value (IDLELTR_VALUE)—Offset 214h

IdleLTR_Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 800h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Snoop Requirement (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10 -bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	0h RO	Reserved.
12:10	2h RW	**Snoop Latency Scale (snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop Value (snoop_value):** 10-bit latency value

11.3.5 TX Bit Count (TX_BIT_COUNT)—Offset 218h

TX_BIT_COUNT_Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**Tx Count Overflow (tx_count_overflow):** 0 = Count valid 1 = count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**Tx Bit Count (tx_bit_count):** 24-bit up-counter which counts the number of TX bits on the Serial bus. The counter is forced to be cleared by software Read

11.3.6 Rx Bit Count (RX_BIT_COUNT)—Offset 21Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**Rx Count Overflow (rx_count_overflow):** 0 = count valid 1 = count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**Rx Bit Count (rx_bit_count):** 24-bit up-counter which counts the number of RX Bits on the Serial bus. The counter is forced to be cleared by software Read

11.3.7 REG SSP_REG (SSP_REG)—Offset 220h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**Disable DMA Finish (disable_ssp_dma_finish):** This bit needs to be set to 1 if GSPI is using DMA multi-Block Chaining and the SW driver does not plan to re-enable the DMA manually after every Link List completion 1 = DMA finish Disabled Note: Required for multi-block transfer 0 – DMA finish not disabled.

11.3.8 GSPI CS Control (SPI_CS_CONTROL)—Offset 224h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 3000h

Bit Range	Default and Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	1h RW	**CS1 Polarity (cs1_polarity):** This Bit selects the Inactive/Idle polarity of SPI CS1 Signal. 0 = low 1 = high **Note:** When program the CS polarity existing S0ix, the CS may not be toggling unless dynamic clock gating is disabled or SSE bit in SSP Control register is set
12	1h RW	**CS0 Polarity (cs0_polarity):** This Bit selects the Inactive/Idle polarity of SPI CS0 Signal. 0 = Low 1 = High **Note:** When program the CS polarity existing S0ix, the CS may not be toggling unless dynamic clock gating is disabled or SSE bit in SSP Control register is set

Bit Range	Default and Access	Field Name (ID): Description
11:10	0h RO	Reserved.
9:8	0h RW	**Chip Select 1 Output Select (cs1_output_sel):** These Bits select which GSPI CS Signal is to be driven by the SSP Frame (CS). 00 = GSPI CS0 01 = GSPI CS1, if applicable 10 = GSPI CS2, if applicable 11= GSPI CS3, if applicable
7:2	0h RO	Reserved.
1	0h RW	**Chip Select State (cs_state):** Manual SW control of SPI Chip Select (CS) 0 = CS is set to low 1 = CS is set to high
0	0h RW	**Chip Select Mode (cs_mode):** GSPI Chip Select Mode. 0 = HW Mode- CS is under HW control 1 = SW Mode – CS is under SW Control using cs_state bit

11.3.9 SW Scratch 0 (SW_SCRATCH)—Offset 228h

NOTE: The same registers are available at the following offsets:
SW SCRATCH 1: offset 22Ch
SW SCRATCH 2: offset 230h
SW SCRATCH 3: offset 234h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Scratch 0 (reg_SW_Scratch_0):** Scratch Pad Register for SW to generate Local DATA for DMA.

11.3.10 SW Scratch 1 (SW_SCRATCH_1)—Offset 22Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Scratch 1 (reg_SW_Scratch_1):** Scratch Pad Register for SW to generated Local DATA for iDMA

11.3.11 SW Scratch 2 (SW_SCRATCH_2)—Offset 230h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Scratch 2 (reg_SW_Scratch_2):** Scratch Pad Register for SW to generate Local DATA for DMA.

11.3.12 SW Scratch 3 (SW_SCRATCH_3)—Offset 234h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Scratch 3 (reg_SW_Scratch_3):** Scratch Pad Register for SW to generate Local DATA for DMA.

11.3.13 Clock Gate (CLOCK_GATE)—Offset 238h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:2	0h RW	**DMA Clock Control (sw_dma_clk_ctl):** DMA Clock Control 00 = Dyanamic Clock Gate Enable 01 = Reserved 10 = Force DMA Clock off 11 = Force DMA Clock on
1:0	0h RW	**Clock Control (sw_ip_clk_ctl):** Clock Control 00 = Dynamic Clock Gate Enable 01 = Reserved 10 = Force Clocks off 11 = Force Clocks on

11.3.14 Remap Address Low (REMAP_ADDR_LO)—Offset 240h

REMAP_ADDR_LO_Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Remap Address Low (spi_remap_addr_low):** Low 32 bits of BAR address read by SW

11.3.15 Remap Address High (REMAP_ADDR_HI)—Offset 244h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Remap address High (spi_remap_addr_high):** High 32 bits of BAR address read by SW

11.3.16 Device Idle Control (DEVIDLE_CONTROL)—Offset 24Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**Interrupt Request Capable (intr_req_capable):** Set to '1' by HW if it is capable of generating an interrupt on command completion, else '0'.
3	1h RW/1C	**Restore Required (restore_required):** When set (by HW), SW must restore state to the controller. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a '1'. This bit will be set on initial power up.

Bit Range	Default and Access	Field Name (ID): Description
2	0h RW	**Device Idle (devidle):** SW sets this bit to '1' to move the function into the DevIdle state. Writing this bit to '0' will return the function to the fully active D0 state (D0i0).
1	0h RO	Reserved.
0	0h RO	**Command In Progress (cmd_in_progress):** HW sets this bit on a 1->0 or 0->1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is unsupported for SW to write to any bit in this register. HW clears this bit upon completing the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

11.3.17 Delay Rx Clock (DEL_RX_CLK)—Offset 250h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RW	**Rx Clock Select (RX_CLK_SEL):** 00 = The output of the internal (M/N and/or baud rate) clock divider is used as-is to clock in the receive data to the RxFIFO. 01 = An internally delayed version of the internal clock divider output is used to clock in the receive data to the RxFIFO. This allows some additional setup time on the PCH side. 10 = The receive data is clocked on the subsequent negedge of the Tx clock, allowing a full cycle propagation delay on the platform. 11: The receive data is clocked on the subsequent negedge of the delayed Rx clock, maximizing the amount of delay allowed for capturing the receive data. Note: This capability is only supported for default SSP configuration with active high clocks (SSCR1.SPO = 0 and SSCR1.SPH = 0). Other combinations of SPO and SPH setting are not supported for non-zero settings of this field.

11.3.18 Capabilities (CAPABLITIES)—Offset 2FCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 620h

Bit Range	Default and Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10	1h RO	**SPI CS1 Support (spi_cs1_oe_stat):** 0 = Not Supported; 1 = Supported
9	1h RO	**SPI CS0 Support (spi_cs0_oe_stat):** 0 = Not Supported; 1 = Supported
8	0h RO	**DMA Present (iDMA_present):** 0= DMA present 1= DMA not present
7:4	2h RO	**Instance Type (instance_type):** 0000 = I2C 0001 = UART 0010 = GSPI 0011 – 1111 = Reserved
3:0	0h RO	**Instance Number (instance_number):** 0h: SPI0 1h: SPI1

11.4 Generic SPI (GSPI) DMA Controller Registers Summary

The registers in this section are memory mapped based on the BAR defined in PCI configuration space.

Table 11-4. Summary of Generic SPI (GSPI) DMA Controller Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
800h	803h	DMA Transfer Source Address Low (SAR_LO0)—Offset 800h	0h
804h	807h	DMA Transfer Source Address High (SAR_HI0)—Offset 804h	0h
808h	80Bh	DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h	0h
80Ch	80Fh	DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch	0h
810h	813h	Linked List Pointer Low (LLP_LO0)—Offset 810h	0h
814h	817h	Linked List Pointer High (LLP_HI0)—Offset 814h	0h
818h	81Bh	Control Register Low (CTL_LO0)—Offset 818h	0h
81Ch	81Fh	Control Register High (CTL_HI0)—Offset 81Ch	0h
820h	823h	Source Status (SSTAT0)—Offset 820h	0h
828h	82Bh	Destination Status (DSTAT0)—Offset 828h	0h
830h	833h	Source Status Address Low (SSTATAR_LO0)—Offset 830h	0h
834h	837h	Source Status Address High (SSTATAR_HI0)—Offset 834h	0h
838h	83Bh	Destination Status Address Low (DSTATAR_LO0)—Offset 838h	0h
83Ch	83Fh	Destination Status Address High (DSTATAR_HI0)—Offset 83Ch	0h
840h	843h	DMA Transfer Configuration Low (CFG_LO0)—Offset 840h	203h
844h	847h	DMA Transfer Configuration High (CFG_HI0)—Offset 844h	0h
848h	84Bh	Source Gather (SGR0)—Offset 848h	0h
850h	853h	Destination Scatter (DSR0)—Offset 850h	0h
858h	85Bh	DMA Transfer Source Address Low (SAR_LO1)—Offset 858h	0h

Table 11-4. Summary of Generic SPI (GSPI) DMA Controller Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
85Ch	85Fh	DMA Transfer Source Address High (SAR_HI1)—Offset 85Ch	0h
860h	863h	DMA Transfer Destination Address Low (DAR_LO1)—Offset 860h	0h
864h	867h	DMA Transfer Destination Address High (DAR_HI1)—Offset 864h	0h
868h	86Bh	Linked List Pointer Low (LLP_LO1)—Offset 868h	0h
86Ch	86Fh	Linked List Pointer High (LLP_HI1)—Offset 86Ch	0h
870h	873h	Control Register Low 1 (CTL_LO1)—Offset 870h	0h
874h	877h	Control Register High 1 (CTL_HI1)—Offset 874h	0h
878h	87Bh	Source Status 1 (SSTAT1)—Offset 878h	0h
880h	883h	Destination Status 1 (DSTAT1)—Offset 880h	0h
888h	88Bh	Source Status Address Low (SSTATAR_LO1)—Offset 888h	0h
88Ch	88Fh	Source Status Address High (SSTATAR_HI1)—Offset 88Ch	0h
890h	893h	Destination Status Address Low (DSTATAR_LO1)—Offset 890h	0h
894h	897h	Destination Status Address High (DSTATAR_HI1)—Offset 894h	0h
898h	89Bh	DMA Transfer Configuration Low (CFG_LO1)—Offset 898h	0h
89Ch	89Fh	DMA Transfer Configuration High 1 (CFG_HI1)—Offset 89Ch	0h
8A0h	8A3h	Source Gather 1 (SGR1)—Offset 8A0h	0h
8A8h	8ABh	Destination Scatter 1 (DSR1)—Offset 8A8h	0h
AC0h	AC3h	Raw Interrupt Status (RawTfr)—Offset AC0h	0h
AC8h	ACBh	Raw Status for Block Interrupts (RawBlock)—Offset AC8h	0h
AD0h	AD3h	Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h	0h
AD8h	ADBh	Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h	0h
AE0h	AE3h	Raw Status for Error Interrupts (RawErr)—Offset AE0h	0h
AE8h	AEBh	Interrupt Status (StatusTfr)—Offset AE8h	0h
AF0h	AF3h	Status for Block Interrupts (StatusBlock)—Offset AF0h	0h
AF8h	AFBh	Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h	0h
B00h	B03h	Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h	0h
B08h	B0Bh	Status for Error Interrupts (StatusErr)—Offset B08h	0h
B10h	B13h	Mask for Transfer Interrupts (MaskTfr)—Offset B10h	0h
B18h	B1Bh	Mask for Block Interrupts (MaskBlock)—Offset B18h	0h
B20h	B23h	Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h	0h
B28h	B2Bh	Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h	0h
B30h	B33h	Mask for Error Interrupts (MaskErr)—Offset B30h	0h
B38h	B3Bh	Clear for Transfer Interrupts (ClearTfr)—Offset B38h	0h
B40h	B43h	Clear for Block Interrupts (ClearBlock)—Offset B40h	0h
B48h	B4Bh	Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h	0h
B50h	B53h	Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h	0h
B58h	B5Bh	Clear for Error Interrupts (ClearErr)—Offset B58h	0h
B60h	B63h	Combined Status register (StatusInt)—Offset B60h	0h
B98h	B9Bh	DMA Configuration (DmaCfgReg)—Offset B98h	0h
BA0h	BA3h	DMA Channel Enable (ChEnReg)—Offset BA0h	0h

11.4.1 DMA Transfer Source Address Low (SAR_LO0)—Offset 800h

NOTE: SAR_LO0 is for DMA Channel 0. The same register definition,SAR_LO1, is available for Channel 1 at address 858h.
SAR_LO0 (CH0): offset 800h
SAR_LO1 (CH1): offset 858h
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SAR_LO (SAR_LO):** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

11.4.2 DMA Transfer Source Address High (SAR_HI0)—Offset 804h

NOTE: SAR_HI0 is for DMA Channel 0. The same register definition, SAR_HI1, is available for Channel 1 at address 85Ch.
SAR_HI0 (CH0): offset 804h
SAR_HI1 (CH1): offset 85Ch
The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SAR_HI (SAR_HI):** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length) 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

11.4.3 DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h

NOTE: DAR_LO0 is for DMA Channel 0. The same register definition, DAR_LO1, is available for Channel 1 at address 860h.
DAR_LO0 (CH0): offset 808h
DAR_LO1 (CH1): offset 860h
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DAR_LO (DAR_LO):** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

11.4.4 DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch

NOTE: DAR_HI0 is for DMA Channel 0. The same register definition, DAR_HI1, is available for Channel 1 at address 864h.
DAR_HI0 (CH0): offset 80Ch
DAR_HI1 (CH1): offset 864h
The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DAR_HI (DAR_HI):** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length) 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported

11.4.5 Linked List Pointer Low (LLP_LO0)—Offset 810h

NOTE: LLP_LO0 is for DMA Channel 0. The same register definition, LLP_LO1, is available for Channel 1 at address 868h.
LLP_LO0 (CH0): offset 810h
LLP_LO1 (CH1): offset 868h
The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**LOC (LOC):** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	Reserved.

11.4.6 Linked List Pointer High (LLP_HI0)—Offset 814h

NOTE: LLP_HI0 is for DMA Channel 0. The same register definition, LLP_HI1, is available for Channel 1 at address 86Ch.
LLP_HI0 (CH0): offset 814h
LLP_LO1 (CH1): offset 86Ch
The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

11.4.7 Control Register Low (CTL_LO0)—Offset 818h

NOTE: CTL_LO0 is for DMA Channel 0. The same register definition, CTL_LO1, is available for Channel 1 at address 870h.
LLP_HI0 (CH0): offset 818h
LLP_LO1 (CH1): offset 870h
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled. If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RW	**LLP_SRC_EN (LLP_SRC_EN):** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN (LLP_DST_EN):** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	Reserved.
21:20	0h RW	**TT_FC (TT_FC):** The following transfer types are supported. 00: Reserved 01: Memory to Peripheral 10: Peripheral to Memory 11: Peripheral to Peripheral Flow Control is always assigned to the DMA.

Bit Range	Default and Access	Field Name (ID): Description
19	0h RO	Reserved.
18	0h RW	**DST_SCATTER_EN (DST_SCATTER_EN):** 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN (SRC_GATHER_EN):** 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE (SRC_MSIZE):** Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source.
13:11	0h RW	**DEST_MSIZE (DEST_MSIZE):** Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**SINC (SINC):** Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	Reserved.
8	0h RW	**DINC (DINC):** Indicates whether to increment or decrement the destination address on every destination transfer. If the device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	Reserved.
6:4	0h RW	**SRC_TR_WIDTH (SRC_TR_WIDTH):** BURST_SIZE (IN DW) = (2^ MSIZE) (i.e. 2 to-the-power-of MSIZE) 1.Transferred Bytes Per Burst = BURST_SIZE * (2 ^ TR_WIDTH) Since Max Burst Length is limited to 16 DW, encodings 101 (32 DW), 110 (64 DW) and 111 (128 DW) are not supported. 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported.
3:1	0h RW	**DST_TR_WIDTH (DST_TR_WIDTH):** Destination Transfer Width. BURST_SIZE = (2 ^ MSIZE) 1.Transferred Bytes Per Burst = (BURST_SIZE * TR_WIDTH) 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported (due to OCP limitations)
0	0h RW	**INT_EN (INT_EN):** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

11.4.8 Control Register High (CTL_HI0)—Offset 81Ch

NOTE: CTL_HI0 is for DMA Channel 0. The same register definition, CTL_HI1, is available for Channel 1 at address 874h.
CTL_HI0 (CH0): offset 81Ch
CTL_HI1 (CH1): offset 874h
This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS (CH_CLASS):** A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.
28:18	0h NA	**RESERVED (RESERVED0):** Reserved
17	0h RW	**DONE (DONE):** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS (BLOCK_TS):** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register.

11.4.9 Source Status (SSTAT0)—Offset 820h

NOTE: SSTAT0 is for DMA Channel 0. The same register definition, SSTAT1, is available for Channel 1 at address 878h.
SSTAT0 (CH0): offset 820h
SSTAT1 (CH1): offset 878h
After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block.
Note : This register is a temporary placeholder for the source status information on its way to the SSTATx register location of the LLI. The source status information should be retrieved by software from the SSTATx register location of the LLI, and not by a read of this register over the DMA slave interface.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SSTAT (SSTAT):** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

11.4.10 Destination Status (DSTAT0)—Offset 828h

NOTE: DSTAT0 is for DMA Channel 0. The same register definition, DSTAT1, is available for Channel 1 at address 880h.
DSTAT0 (CH0): offset 828h
DSTAT1 (CH1): offset 880h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI.
Note : This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DSTAT (DSTAT):** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface

11.4.11 Source Status Address Low (SSTATAR_LO0)—Offset 830h

NOTE: SSTATAR_LO0 is for DMA Channel 0. The same register definition, SSTATAR_LO1, is available for Channel 1 at address 888h.
SSTATAR_LO0(CH0): offset 830h
SSTATAR_LO1(CH1): offset 888h
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_LO (SSTATAR_LO):** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

11.4.12 Source Status Address High (SSTATAR_HI0)—Offset 834h

NOTE: SSTATAR_HI0 is for DMA Channel 0. The same register definition, SSTATAR_HI1, is available for Channel 1 at address 88Ch.
SSTATAR_HI0(CH0): offset 834h
SSTATAR_HI1(CH1): offset 88Ch
After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_HI (SSTATAR_HI):** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

11.4.13 Destination Status Address Low (DSTATAR_LO0)—Offset 838h

NOTE: DSTATAR_LO0 is for DMA Channel 0. The same register definition, DSTATAR_LO1, is available for Channel 1 at address 890h.
DSTATAR_LO0(CH0): offset 838h
DSTATAR_LO1(CH1): offset 890h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR_LO (DSTATAR_LO):** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

11.4.14 Destination Status Address High (DSTATAR_HI0)—Offset 83Ch

NOTE: DSTATAR_HI0 is for DMA Channel 0. The same register definition, DSTATAR_HI1, is available for Channel 1 at address 894h.
DSTATAR_HI0(CH0): offset 83Ch

DSTATAR_HI1(CH1): offset 894h
After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR_HI (DSTATAR_HI):** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

11.4.15 DMA Transfer Configuration Low (CFG_LO0)—Offset 840h

NOTE: CFG_LO0 is for DMA Channel 0. The same register definition, CFG_LO1, is available for Channel 1 at address 898h.
CFG_LO0(CH0): offset 840h
CFG_LO1(CH1): offset 898h
This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 203h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST (RELOAD_DST):** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated
30	0h RW	**RELOAD_SRC (RELOAD_SRC):** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	Reserved.
21	0h RW	**SRC_OPT_BL (SRC_OPT_BL):** Optimize Source Burst Length: 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ SRC_MSIZE)) This bit should be set to (0) if Source HW-Handshake is enabled
20	0h RW	**DST_OPT_BL (DST_OPT_BL):** Optimize Destination Burst Length : 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 <= BL <= (2 ^ DST_MSIZE)) This bit should be set to (0) if Destination HW-Handshake is enabled

Bit Range	Default and Access	Field Name (ID): Description
19	0h RW	**SRC_HS_POL (SRC_HS_POL):** Source Handshaking Interface Polarity. 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL (DST_HS_POL):** Destination Handshaking Interface Polarity. 0 = Active high 1 = Active low
17:11	0h RO	Reserved.
10	0h RW	**CH_DRAIN (CH_DRAIN):** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1h RO	**FIFO_EMPTY (FIFO_EMPTY):** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP (CH_SUSP):** Channel Suspend. Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN (SS_UPD_EN):** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0
6	0h RW	**DS_UPD_EN (DS_UPD_EN):** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN (CTL_HI_UPD_EN):** CTL_HI Update Enable. If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	Reserved.
3	0h RW	**HSHAKE_NP_WR (HSHAKE_NP_WR):** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-of-block writes which will be Non-Posted)
2	0h RW	**ALL_NP_WR (ALL_NP_WR):** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW-Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used.
1	1h RW	**SRC_BURST_ALIGN (SRC_BURST_ALIGN):** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary
0	1h RW	**DST_BURST_ALIGN (DST_BURST_ALIGN):** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary.

11.4.16 DMA Transfer Configuration High (CFG_HI0)—Offset 844h

NOTE: CFG_HI0 is for DMA Channel 0. The same register definition, CFG_HI1, is available for Channel 1 at address 89Ch.
CFG_HI0(CH0): offset 844h
CFG_HI1(CH1): offset 89Ch
This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:18	0h RW	**WR_ISSUE_THD (WR_ISSUE_THD):** Write Issue Threshold. Used to relax the issue criterion for Writes. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD (RD_ISSUE_THD):** Read Issue Threshold. Used to relax the issue criterion for Reads. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER (DST_PER):** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.
3:0	0h RW	**SRC_PER (SRC_PER):** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface. NOTE: For correct DMA operation, only one peripheral (source or destination) should be assigned to the same handshaking interface.

11.4.17 Source Gather (SGR0)—Offset 848h

NOTE: SGR0 is for DMA Channel 0. The same register definition, SGR1, is available for Channel 1 at address 8A0h.
SGR0(CH0): offset 848h
SGR1(CH1): offset 8A0h
The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RW	**SGC (SGC):** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI (SGI)**

11.4.18 Destination Scatter (DSR0)—Offset 850h

NOTE: DSR0 is for DMA Channel 0. The same register definition, DSR1, is available for Channel 1 at address 8A8h.
DSR0(CH0): offset 850h
DSR1(CH1): offset 8A8h
The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RW	**DSC (DSC)**
19:0	0h RW	**DSI (DSI)**

11.4.19 DMA Transfer Source Address Low (SAR_LO1)—Offset 858h

This register is for DMA Channel 1 and has the same definition as SAR_LO0 register at offset 800h.

11.4.20 DMA Transfer Source Address High (SAR_HI1)—Offset 85Ch

This register is for DMA channel 1 and has the same definition as SAR_HI0 at offset 804h.

11.4.21 DMA Transfer Destination Address Low (DAR_LO1)—Offset 860h

This register is for DMA channel 1 and has the same definition as DAR_LO0 at offset 808h.

11.4.22 DMA Transfer Destination Address High (DAR_HI1)—Offset 864h

This register is for DMA channel 1 and has the same definition as DAR_HI0 at offset 80Ch.

11.4.23 Linked List Pointer Low (LLP_LO1)—Offset 868h

This register is for DMA channel 1 and has the same definition as LLP_LO0 at offset 810h.

11.4.24 Linked List Pointer High (LLP_HI1)—Offset 86Ch

This register is for DMA channel 1 and has the same definition as LLP_HI0 at offset 814h.

11.4.25 Control Register Low 1 (CTL_LO1)—Offset 870h

This register is for DMA channel 1 and has the same definition as CTL_LO0 at offset 818h.

11.4.26 Control Register High 1 (CTL_HI1)—Offset 874h

This register is for DMA channel 1 and has the same definition as CTL_HI0 at offset 81Ch.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:18	0h NA	**RESERVED (RESERVED0):** Reserved
17:0	0h RO	Reserved.

11.4.27 Source Status 1 (SSTAT1)—Offset 878h

This register is for DMA channel 1 and has the same definition as SSTAT0 at offset 820h.

11.4.28 Destination Status 1 (DSTAT1)—Offset 880h

This register is for DMA channel 1 and has the same definition as DSTAT0 at offset 828h.

11.4.29 Source Status Address Low (SSTATAR_LO1)—Offset 888h

This register is for DMA channel 1 and has the same definition as SSTATAR_LO0 at offset 830h.

11.4.30 Source Status Address High (SSTATAR_HI1)—Offset 88Ch

This register is for DMA channel 1 and has the same definition as SSTATAR_HI0 at offset 834h.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_HI (SSTATAR_HI):** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

11.4.31 Destination Status Address Low (DSTATAR_LO1)—Offset 890h

This register is for DMA channel 1 and has the same definition as DSTATAR_LO0 at offset 838h.

11.4.32 Destination Status Address High (DSTATAR_HI1)—Offset 894h

This register is for DMA channel 1 and has the same definition as DSTATAR_HI0 at offset 83Ch.

11.4.33 DMA Transfer Configuration Low (CFG_LO1)—Offset 898h

This register is for DMA channel 1 and has the same definition as CFG_LO0 at offset 840h.

11.4.34 DMA Transfer Configuration High 1 (CFG_HI1)—Offset 89Ch

This register is for DMA channel 1 and has the same definition as CFG_HI0 at offset 844h.

11.4.35 Source Gather 1 (SGR1)—Offset 8A0h

This register is for DMA channel 1 and has the same definition as SDR0 at offset 848h.

11.4.36 Destination Scatter 1 (DSR1)—Offset 8A8h

This register is for DMA channel 1 and has the same definition as DSR0 at offset 850h.

11.4.37 Raw Interrupt Status (RawTfr)—Offset AC0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit0 for channel 0 and bit 1 for channel 1.

11.4.38 Raw Status for Block Interrupts (RawBlock)—Offset AC8h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

11.4.39 Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

11.4.40 Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

11.4.41 Raw Status for Error Interrupts (RawErr)—Offset AE0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

11.4.42 Interrupt Status (StatusTfr)—Offset AE8h

Status for Transfer Interrupts Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 for channel 0 and bit 1 for channel 1.

11.4.43 Status for Block Interrupts (StatusBlock)—Offset AF0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 for channel 0 and bit 1 for channel 1.

11.4.44 Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 is for channel 0 and bit 1 is for channel 1.

11.4.45 Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 is for channel 0 and bit 1 is for channel 1.

11.4.46 Status for Error Interrupts (StatusErr)—Offset B08h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 is for channel 0 and bit 1 is for channel 1.

11.4.47 Mask for Transfer Interrupts (MaskTfr)—Offset B10h

Mask for Transfer Interrupts Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch 1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** 0-mask 1-unmask

11.4.48 Mask for Block Interrupts (MaskBlock)—Offset B18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** 0-mask 1-unmask

11.4.49 Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** 0-mask 1-unmask

11.4.50 Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** 0-mask 1-unmask

11.4.51 Mask for Error Interrupts (MaskErr)—Offset B30h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** 0-mask 1-unmask

11.4.52 Clear for Transfer Interrupts (ClearTfr)—Offset B38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

11.4.53 Clear for Block Interrupts (ClearBlock)—Offset B40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

11.4.54 Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

11.4.55 Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

11.4.56 Clear for Error Interrupts (ClearErr)—Offset B58h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

11.4.57 Combined Status register (StatusInt)—Offset B60h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is Ored to produce a single bit for each interrupt type in the Combined Status register (StatusInt). Th is register is read-only

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**ERR (ERR):** OR of the contents of StatusErr register.
3	0h RO	**DSTT (DSTT):** OR of the contents of StatusDst register.
2	0h RO	**SRCT (SRCT):** OR of the contents of StatusSrcTran register
1	0h RO	**BLOCK (BLOCK):** OR of the contents of StatusBlock register.
0	0h RO	**TFR (TFR):** OR of the contents of StatusTfr register.

11.4.58 DMA Configuration (DmaCfgReg)—Offset B98h

This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**DMA_EN (DMA_EN):** 0 = DMA Disabled 1 = DMA Enabled

11.4.59 DMA Channel Enable (ChEnReg)—Offset BA0h

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority. All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**Channel Enable Write Enable (CH_EN_WE):** Channel enable write enable.
7:2	0h RO	Reserved.
1:0	0h RW	**CH_EN (CH_EN):** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

11.5 GSPI PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 11-5. Summary of GSPI PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
240h	243h	PCI Configuration Control for GSPI0 - Offset 240h	0h
244h	247h	PCI Configuration Control for GSPI1 - Offset 244h	0h
248h	24Bh	PCI Configuration Control for GSPI2 - Offset 248h	0h

11.5.1 PCI Configuration Control for GSPI0 — Offset 240h

Controls the PCI Configuration Space

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:20	0h RW	**PCI IRQ Num Field (PCI_IRQ):** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	0h RW	**PCICFGCTR1 - ACPI IRQ Field (ACPI_IRQ):** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	0h RW	**Interrupt Pin (IPIN7):** This register indicates the values to be used for Global Interrupts. 0 = No interrupt Pin 1 = INTA 2 = INTB 3 = INTC 4 = INTD 5 - FF: Reserved
7	0h RW	**BAR1 Disable (BAR1_DISABLE):** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	0h RW	**PME Support (PME_SUPPORT):** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI Interrupt Enable Field (ACPI_INTR_EN):** When set, the Bridge uses ACPI Sideband opcodes for messages. When cleared, the Bridge uses global IOSF opcodes
0	0h RW	**PCI CFG Disable Field (PCI_CFG_DIS):** When set, PCI configuration accesses return UR response. When 0, PCI configuration accesses are supported

11.5.2 PCI Configuration Control for GSPI1 — Offset 244h

Same definition as PCI Configuration Control for GSPI0.

11.5.3 PCI Configuration Control for GSPI2 — Offset 248h

Same definition as PCI Configuration Control for GSPI0.

12 PCIe* Interface (D29:F0-F7, D28:F0-F7, and D27: F0-F7)

12.1 PCI Express* (PCIe*) Interface (D28:F0-F7 and D29:PF0-F3) Registers Summary

There are twelve sets of the following configuration registers used for PCH PCI Express* Port Configurations. Each PCH PCI Express* Configuration Register set covers a single PCI Express* Port and maps out as the following Device/Function:
D28/F0 = Port1
D28/F1 = Port2
D28/F2 = Port3
D28/F3 = Port4
D28/F4 = Port5
D28/F5 = Port6
D28/F6 = Port7
D28/F7 = Port8
D29/F0 = Port9
D29/F1 = Port10
D29/F2 = Port11
D29/F3 = Port12

Table 5. Summary of PCI Express* (PCIe*) Interface (D28:F0-F7 and D29:PF0-F3) Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Identifiers (ID)—Offset 0h	XXXX8068h
4h	7h	Device Command And Primary Status (CMD_PSTS)—Offset 4h	0h
8h	Bh	Revision ID And Class Code (RID_CC)—Offset 8h	60400FXh
Ch	Fh	Cache Line Size, Primary Latency Timer And Header Type (CLS_PLT_HTYPE)—Offset Ch	810000h
18h	1Bh	Bus Numbers And Secondary Latency Timer (BNUM_SLT)—Offset 18h	0h
1Ch	1Fh	I/O Base And Limit And Secondary Status (IOBL_SSTS)—Offset 1Ch	0h
20h	23h	Memory Base And Limit (MBL)—Offset 20h	0h
24h	27h	Prefetchable Memory Base And Limit (PMBL)—Offset 24h	10001h
28h	2Bh	Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h	0h
2Ch	2Fh	Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch	0h
34h	37h	Capabilities List Pointer (CAPP)—Offset 34h	40h
3Ch	3Fh	Interrupt Information And Bridge Control (INTR_BCTRL)—Offset 3Ch	0h
40h	43h	Capabilities List And PCI Express Capabilities (CLIST_XCAP)—Offset 40h	428010h
44h	47h	Device Capabilities (DCAP)—Offset 44h	8001h
48h	4Bh	Device Control And Device Status (DCTL_DSTS)—Offset 48h	100000h
4Ch	4Fh	Link Capabilities (LCAP)—Offset 4Ch	710C00h
50h	53h	Link Control And Link Status (LCTL_LSTS)—Offset 50h	10000h
54h	57h	Slot Capabilities (SLCAP)—Offset 54h	40060h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
58h	5Bh	Slot Control And Slot Status (SLCTL_SLSTS)—Offset 58h	0h
5Ch	5Fh	Root Control (RCTL)—Offset 5Ch	0h
60h	63h	Root Status (RSTS)—Offset 60h	0h
64h	67h	Device Capabilities 2 (DCAP2)—Offset 64h	80837h
68h	6Bh	Device Control 2 And Device Status 2 (DCTL2_DSTS2)—Offset 68h	0h
6Ch	6Fh	Link Capabilities 2 (LCAP2)—Offset 6Ch	0h
70h	73h	Link Control 2 And Link Status 2 (LCTL2_LSTS2)—Offset 70h	1h
80h	83h	Message Signaled Interrupt Identifiers And Message Signaled Interrupt Message Control (MID_MC)—Offset 80h	9005h
84h	87h	Message Signaled Interrupt Message Address (MA)—Offset 84h	0h
88h	8Bh	Message Signaled Interrupt Message Data (MD)—Offset 88h	0h
90h	93h	Subsystem Vendor Capability (SVCAP)—Offset 90h	A00Dh
94h	97h	Subsystem Vendor IDs (SVID)—Offset 94h	0h
A0h	A3h	Power Management Capability And PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h	C8030001h
A4h	A7h	PCI Power Management Control And Status (PMCS)—Offset A4h	8h
D0h	D3h	Additional Configuration 1 (CCFG)—Offset D0h	0h
D4h	D7h	Miscellaneous Port Configuration 2 (MPC2)—Offset D4h	0h
D8h	DBh	Miscellaneous Port Configuration (MPC)—Offset D8h	1110000h
DCh	DFh	SMI And SCI Status (SMSCS)—Offset DCh	0h
E0h	E3h	Scratch Pad Register, Root Port Dynamic Clock Gate Enable And Root Port Power Gating Enable (SPR_RPDCGEN_RPPGEN)—Offset E0h	0h
ECh	EFh	Chipset Initialization Register 0EC (DC)—Offset ECh	0h
F0h	F3h	Chipset Initialization Register 0F0 (IPCS)—Offset F0h	0h
100h	103h	Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h	0h
104h	107h	Uncorrectable Error Status (UES)—Offset 104h	0h
108h	10Bh	Uncorrectable Error Mask (UEM)—Offset 108h	0h
10Ch	10Fh	Uncorrectable Error Severity (UEV)—Offset 10Ch	60011h
110h	113h	Correctable Error Status (CES)—Offset 110h	0h
114h	117h	Correctable Error Mask (CEM)—Offset 114h	2000h
118h	11Bh	Advanced Error Capabilities And Control (AECC)—Offset 118h	0h
12Ch	12Fh	Root Error Command (REC)—Offset 12Ch	0h
130h	133h	Root Error Status (RES)—Offset 130h	0h
134h	137h	Error Source Identification (ESID)—Offset 134h	0h
200h	203h	L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h	0h
204h	207h	L1 Sub-States Capabilities (L1SCAP)—Offset 204h	28281Fh
208h	20Bh	L1 Sub-States Control 1 (L1SCTL1)—Offset 208h	0h
20Ch	20Fh	L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch	28h
220h	223h	ACS Extended Capability Header (ACSECH)—Offset 220h	0h
224h	227h	ACS Capability Register And ACS Control Register (ACSCAPR_ACSCTLR)—Offset 224h	1Bh
300h	303h	PCI Express Replay Timer Policy 1 (PCIERTP1)—Offset 300h	A64F96h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
314h	317h	PCI Express NFTS (PCIENFTS)—Offset 314h	0h
318h	31Bh	PCI Express L0s Control (PCIEL0SC)—Offset 318h	0h
320h	323h	PCI Express Configuration (PCIECFG2)—Offset 320h	0h
39Ch	39Fh	Chipset Initialization Register 39C (PTMPSDC1)—Offset 39Ch	0h
3A0h	3A3h	Chipset Initialization Register 3A0 (PTMPSDC2)—Offset 3A0h	0h
3A4h	3A7h	Chipset Initialization Register 3A4 (PTMPSDC3)—Offset 3A4h	0h
3A8h	3ABh	Chipset Initialization Register 3A8 (PTMPSDC4)—Offset 3A8h	0h
3ACh	3AFh	Chipset Initialization Register 3AC (PTMPSDC5)—Offset 3ACh	0h
3B0h	3B3h	Chipset Initialization Register 3B0 (PTMECFG)—Offset 3B0h	0h
400h	403h	Chipset Initialization Register 400 (LTROVR)—Offset 400h	0h
404h	407h	Chipset Initialization Register 404 (LTROVR2)—Offset 404h	0h
408h	40Bh	Chipset Initialization Register 408 (PHYCTL4)—Offset 408h	0h
420h	423h	Chipset Initialization Register 420 (PCIEPMECTL)—Offset 420h	0h
424h	427h	Chipset Initialization Register 424 (PCIEPMECTL2)—Offset 424h	0h
428h	42Bh	Chipset Initialization Register 428 (PCE)—Offset 428h	0h
450h	453h	Chipset Initialization Register 450 (EQCFG1)—Offset 450h	0h
454h	457h	Chipset Initialization Register 454 (RTPCL1)—Offset 454h	0h
458h	45Bh	Chipset Initialization Register 458 (RTPCL2)—Offset 458h	0h
45Ch	45Fh	Chipset Initialization Register 45C (RTPCL3)—Offset 45Ch	0h
460h	463h	Chipset Initialization Register 460 (RTPCL4)—Offset 460h	0h
464h	467h	Chipset Initialization Register 464 (FOMS)—Offset 464h	0h
468h	46Bh	Chipset Initialization Register 468 (HAEQ)—Offset 468h	0h
470h	473h	Chipset Initialization Register 470 (LTCO1)—Offset 470h	0h
474h	477h	Chipset Initialization Register 474 (LTCO2)—Offset 474h	0h
478h	47Bh	Chipset Initialization Register 478 (G3L0SCTL)—Offset 478h	0h
47Ch	47Fh	Chipset Initialization Register 47C (EQCFG2)—Offset 47Ch	0h
480h	483h	Chipset Initialization Register 480 (MM)—Offset 480h	0h
A00h	A03h	DPC Extended Capability Header (DPCECH)—Offset A00h	0h
A30h	A33h	Secondary PCI Express Extended Capability Header (SPEECH)—Offset A30h	0h

12.1.1 Identifiers (ID)—Offset 0h

This is Identifiers register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V	**Device Identification (DID):** The value of this ID is product specific. Refer to the Device and Revision ID Table in Volume 1 for default value.
15:0	8086h RO	**Vendor Identification (VID):** Indicates Intel

12.1.2 Device Command And Primary Status (CMD_PSTS)—Offset 4h

This is Device Command and Primary Status register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10	0h RW/V2	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above.
9	0h RO	**Fast Back to Back Enable (FBE):** Reserved per PCI-Express spec.
8	0h RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set.
7	0h RO	**Wait Cycle Control (WCC):** Reserved per PCI-Express spec.
6	0h RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0h RO	**VGA Palette Snoop (VGA_PSE):** Reserved per PCI-Express spec.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Reserved per PCI-Express spec.
3	0h RO	**Special Cycle Enable (SCE):** Reserved per PCI-Express and PCI bridge spec.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit.
1	0h RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone.
0	0h RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone..

12.1.3 Revision ID And Class Code (RID_CC)—Offset 8h

This is Revision ID and Class Code register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 60400F0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	6h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	4h RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge. If the MPC.Bridge Type register is set to a '1' for a Host Bridge, this register reads 00h.
15:8	0h RO/V	**Programming Interface (PI):** PCI-to-PCI bridge.
7:0	F0h RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

12.1.4 Cache Line Size, Primary Latency Timer And Header Type (CLS_PLT_HTYPE)—Offset Ch

This is Cache Line Size, Primary Latency Timer and Header Type register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 810000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**Multi-function Device (MFD):** This bit is '1' to indicate a multi-function device.
22:16	1h RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge. If the MPC.Bridge Type register is set to a '1' for a Host Bridge, this register reads 00h.
15:11	0h RO	**Latency Count (CT):** Reserved per PCI-Express spec
10:8	0h RO	Reserved.
7:0	0h RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec

12.1.5 Bus Numbers And Secondary Latency Timer (BNUM_SLT)—Offset 18h

This is Bus Numbers and Secondary Latency Timer register. Refer to register field for more details

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V2	**Secondary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is a RW register; else this register is RO and returns 0. This register does not affect the behavior of any HW logic.
23:16	0h RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge.
15:8	0h RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port.
7:0	0h RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone.

12.1.6 I/O Base And Limit And Secondary Status (IOBL_SSTS)—Offset 1Ch

This is I/O Base and Limit and Secondary Status register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP.
30	0h RW/1C/V	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device.
29	0h RW/1C/V	**Received Master Abort (RMA):** Set when the port receives a completion with Unsupported Request status to the device.
28	0h RW/1C/V	**Received Target Abort (RTA):** Set when the port receives a completion with Completion Abort status to the device.
27	0h RW/1C/V	**Signaled Target Abort (STA):** Set when the port generates a completion with Completion Abort status to the device.
26:25	0h RO/V	**Secondary DEVSEL# Timing Status (SDTS):** Reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b.
24	0h RW/1C/V	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side.
23	0h RO/V	**Secondary Fast Back to Back Capable (SFBC):** Reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b.
22	0h RO	Reserved.
21	0h RO	**Secondary 66 MHz Capable (SC66):** Reserved per PCI Express spec
20:16	0h RO	Reserved.
15:12	0h RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	0h RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing.
7:4	0h RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	0h RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing.

12.1.7 Memory Base And Limit (MBL)—Offset 20h

Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	0h RO	Reserved.
15:4	0h RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	0h RO	Reserved.

12.1.8 Prefetchable Memory Base And Limit (PMBL)—Offset 24h

Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is PMBU32:PMB [gt]= AD[lb]63:32[rb]:AD[lb]31:20[rb] [lt]= PMLU32:PML.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 10001h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	1h RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing.
15:4	0h RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	1h RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing.

12.1.9 Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h

Size:32 bits

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base.

12.1.10 Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)
Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit.

12.1.11 Capabilities List Pointer (CAPP)—Offset 34h

This is Capabilities List Pointer register. Refer to register field for more details

Access Method

Type: CFG Register (Size: 32 bits)
Device: 28
Function: 0

Default: 40h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	40h RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) Offset Capability Next Pointer 40h PCI Express 80h 80h Message Signaled Interrupt (MSI)90h 90h Subsystem Vendor A0h A0h PCI Power Management 00h Extended PCIe Capability Linked List Offset Capability Next Pointer 100h Advanced Error Reporting 000h

12.1.12 Interrupt Information And Bridge Control (INTR_BCTRL)—Offset 3Ch

This is Interrupt Information and Bridge Control register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27	0h RW/V2	**Discard Timer SERR# Enable (DTSE):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
26	0h RO	**Discard Timer Status (DTS):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set.
25	0h RW/V2	**Secondary Discard Timer (SDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
24	0h RW/V2	**Primary Discard Timer (PDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
23	0h RO	**Fast Back to Back Enable (FBE):** Reserved per Express spec.
22	0h RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW/V2	**Master Abort Mode (MAM):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
20	0h RW	**VGA 16-Bit Decode (V16):** When set, indicates that the I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled. 0: Execute 10-bit address decode on VGA I/O accesses. 1: Execute 16-bit address decode on VGA I/O accesses.
19	0h RW	**VGA Enable (VE):** When set, the following ranges will be claimed off the backbone by the root port: Memory ranges A0000h-BFFFFh I/O ranges 3B0h 3BBh and 3C0h 3DFh, and all aliases of bits 15:10 in any combination of 1's
18	0h RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh).
17	0h RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not.
16	0h RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD.
15:8	0h RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. 0000 0001 = INTA# 0000 0010 = INTB# 0000 0011 = INTC# 0000 0100 = INTD# Others = Reserved
7:0	0h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

12.1.13 Capabilities List And PCI Express Capabilities (CLIST_XCAP)—Offset 40h

This is Capabilities List and PCI Express Capabilities register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 428010h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:25	0h RO	**Interrupt Message Number (IMN):** The Root Port does not have multiple MSI interrupt numbers.
24	0h RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
23:20	4h RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port

Bit Range	Default & Access	Field Name (ID): Description
19:16	2h RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 and 3.0 specification which incorporates the Register Expansion ECN.
15:8	80h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	10h RO	**Capability ID (CID):** Indicates this is a PCI Express capability

12.1.14 Device Capabilities (DCAP)—Offset 44h

This is Device Capabilities register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 8001h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports
27:26	0h RO	**Captured Slot Power Limit Scale (CSPS):** Not supported
25:18	0h RO	**Captured Slot Power Limit Value (CSPV):** Not supported
17:16	0h RO	Reserved.
15	1h RO	**Role Based Error Reporting (RBER):** Indicates that this device implements the functionality defined in the Error Reporting ECN as required by the PCI Express 1.1 spec.
14:12	0h RO	Reserved.
11:9	0h RO	**Endpoint L1 Acceptable Latency (E1AL):** Reserved for root ports.
8:6	0h RO	**Endpoint L0 Acceptable Latency (E0AL):** Reserved for Root port.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**Extended Tag Field Supported (ETFS):** The Root Port never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags.
4:3	0h RO	**Phantom Functions Supported (PFS):** No phantom functions supported
2:0	1h RW/O	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Max Payload Size of up to 256B is supported. Programming this field to any values other than 128B or 256B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. A separate register is defined for the IOSF interface. Register Attribute: Static

12.1.15 Device Control And Device Status (DCTL_DSTS)—Offset 48h

This is Device Control and Device Status register. Refer to register field for more details

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28

Function: 0

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID.
20	1h RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup
19	0h RW/1C/V	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected.
18	0h RW/1C/V	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed tlp
17	0h RW/1C/V	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned tlp, unexpected completions, unsupported requests, completor abort, or completer timeout
16	0h RW/1C/V	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, tlp crc error, dllp crc error, replay num rollover, replay timeout.
15	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
14:12	0h RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface. A separate register is defined for the IOSF interface.
11	0h RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests.
10	0h RW/P	**Aux Power PM Enable (APME):** Must be RW for OS testing. The OS will set this bit to '1' if the device connected has detected aux power. It has no effect on the root port otherwise.
9	0h RO	**Phantom Functions Enable (PFE):** Not supported
8	0h RO	**Extended Tag Field Enable (ETFE):** Not supported
7:5	0h RW	**Max Payload Size (MPS):** The root port only supports up to 256B max payload. Programming this field to any values greater than DCAP.MPS will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. A separate register is defined for the IOSF interface.Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME. Register Attribute: Static.
4	0h RO	**Enable Relaxed Ordering (ERO):** Not supported
3	0h RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	0h RW	**Fatal Error Reporting Enable (FEE):** enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	0h RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	0h RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

12.1.16 Link Capabilities (LCAP)—Offset 4Ch

This is Link Capabilities register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 710C00h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h 4 04h : : x 0Xh Note: Depending on the platform, the number of Root Ports supported may vary. In this case, the encodings defined in this register will be scaled accordingly.
23	0h RO	Reserved.
22	1h RW/O	**ASPM Optionality Compliance (ASPMOC):** ASPM Optionality Compliance(ASPMOC): This bit must be set to 1b for PCIe 3.0 compliant port. Components implemented against certain earlier versions of this specification will have this bit set to 0b. Software is permitted to use the value of this bit to help determine whether to enable ASPM or whether to run ASPM compliance tests.
21	1h RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms.
20	1h RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	0h RO	**Surprise Down Error Reporting Capable (SDERC):** Set to '0' to indicate the Root Port does not support Surprise Down Error Reporting
18	0h RO	**Clock Power Management (CPM):** '0' Indicates that root ports do not support the CLKREQ# mechanism.
17:15	2h RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b Less than 1 us 001b 1 us to less than 2 us 010b 2 us to less than 4 us 011b 4 us to less than 8 us 100b 8 us to less than 16 us 101b 16 us to less than 32 us 110b 32 us to 64 us 111b More than 64 us Note: If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency.
14:12	0h RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration: LCTL.CCC Value 0 MPC.UCEL 1 MPC.CCEL
11:10	3h RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00 No ASPM Supported 01 L0s Supported 10 L1 Supported 11 L0s and L1 supported.
9:4	0h RO/V	**Maximum Link Width (MLW):** Indicates the maximum link width of the root port. 01h = x1 02h = x2 04h = x4 Others: Reserved.
3:0	0h RO/V	**Max Link Speeds (MLS):** Indicates the supported link speeds of the Root Port 1h = Gen 1 speed 2h = Gen 2 speed 3h = Gen 3 speed Others: Reserved.

12.1.17 Link Control And Link Status (LCTL_LSTS)—Offset 50h

This is Link Control and Link Status register. Refer to register field for more details

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28

Function: 0

Default: 10000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b.
30	0h RW/1C/V	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b.
29	0h RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise.
28	0h RO/V	**Slot Clock Configuration (SCC):** In normal mode, root port uses the same reference clock as on the platform and does not generate its own clock. Note: When operating in PCI Express mode, the default of this register bit is dependent on the [quote]PCIe Non-Common Clock With SSC Mode Enable Strap[/quote]. If the strap enables non-common clock with SSC support, this bit shall default to '0'. Otherwise, this bit shall default to '1'.
27	0h RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training.
26	0h RO	Reserved.
25:20	0h RO/V	**Negotiated Link Width (NLW):** For the root ports, this register could take on several values: Port # Value of PN field RPC 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h The value of this register is undefined if the link has not successfully trained.
19:16	1h RO/V	**Current Link Speed (CLS):** 0001b: 2.5Gb/s Link 0010b: 5.0 GT/s Link
15:12	0h RO	Reserved.
11	0h RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. Default value of this bit is 0b.
9	0h RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Default value of this bit is 0b. Note: When operating as PCI Express, this bit defines the value of the Link Upconfigure Capability in TS2 Ordered Sets.
8	0h RO	**Enable Clock Power Management (ECPM):** Reserved. Not supported on Root Ports.
7	0h RW	**Extended Synch (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. Note: This functionality is not applicable for Mobile Express.
6	0h RW	**Common Clock Configuration (CCC):** When set, indicates that the Root Port and device are operating with a distributed common reference clock.
5	0h WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns '0' when read. Software uses LSTS.LT and LSTS.LTE to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	0h RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state.
3	0h RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes.
2	0h RO	Reserved.
1:0	0h RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used.

12.1.18 Slot Capabilities (SLCAP)—Offset 54h

This is Slot Capabilities register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 40060h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/O	**Physical Slot Number (PSN__31_24):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
23:19	0h RW/O	**Physical Slot Number (PSN__23_19):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
18	1h RO	**No Command Completed Support (NCCS):** Set to '1' as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes.
17	0h RO	**Electromechanical Interlock Present (EMIP):** Set to 0 to indicate that no electro-mechanical interlock is implemented.
16:15	0h RW/O	**Slot Power Limit Scale (SLS):** specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:8	0h RW/O	**Slot Power Limit Value (SLV__14_8):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
7	0h RW/O	**Slot Power Limit Value (SLV__7_7):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	1h RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported.
5	1h RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification.
4	0h RO	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot.
3	0h RO	**Attention Indicator Present (AIP):** Indicates that an attention indicator LED is not present for this slot.
2	0h RO	**MRL Sensor Present (MSP):** Indicates that an MRL sensor is not present
1	0h RO	**Power Controller Present (PCP):** Indicates that a power controller is not implemented for this slot
0	0h RO	**Attention Button Present (ABP):** Indicates that an attention button is not implemented for this slot.

12.1.19 Slot Control And Slot Status (SLCTL_SLSTS)—Offset 58h

This is Slot Control and Slot Status register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW/1C/V	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
23	0h RO	**Electromechanical Interlock Status (EMIS):** Reserved as this port does not support and electromechanical interlock.
22	0h RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected ('1') or empty ('0'). If XCAP.SI is cleared, this bit is a '1'.
21	0h RO	**MRL Sensor State (MS):** Reserved as the MRL sensor is not implemented.
20	0h RO	**Command Completed (CC):** This register is RO as this port does not implement a Hot Plug Controller..
19	0h RW/1C/V	**Presence Detect Changed (PDC):** This bit is set by the root port when the PDS bit changes state.
18	0h RO	**MRL Sensor Changed (MSC):** Reserved as the MRL sensor is not implemented.
17	0h RO	**Power Fault Detected (PFD):** Reserved as a power controller is not implemented.
16	0h RO	**Attention Button Pressed (ABP):** This register is RO as this port does not implement an attention button
15:13	0h RO	Reserved.
12	0h RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed
11	0h RO	**Electromechanical Interlock Control (EMIC):** Reserved as this port does not support an Electromechanical Interlock.
10	0h RO	**Power Controller Control (PCC):** This bit has no meaning for module based hot plug.
9:8	0h RO	**Power Indicator Control (PIC):** This register is RO as this port does not implement a Hot Plug Controller..
7:6	0h RO	**Attention Indicator Control (AIC):** This register is RO as this port does not implement a Hot Plug Controller..
5	0h RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events.
4	0h RO	**Command Completed Interrupt Enable (CCE):** This register is RO as this port does not implement a Hot Plug Controller..
3	0h RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state.
2	0h RO	**MRL Sensor Changed Enable (MSE):** This register is RO as this port does not implement a Hot Plug Controller..
1	0h RO	**Power Fault Detected Enable (PFE):** This register is RO as this port does not implement a Hot Plug Controller...
0	0h RO	**Attention Button Pressed Enable (ABE):** This register is RO as this port does not implement a Hot Plug Controller..

12.1.20 Root Control (RCTL)—Offset 5Ch

This is Root Control register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	0h RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0' to '1' transition, or due to this bit being set with RSTS.PS already set).
2	0h RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set.
1	0h RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set.
0	0h RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set.

12.1.21 Root Status (RSTS)—Offset 60h

This is Root Status register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. Root ports have a one deep PME pending queue.
16	0h RW/1C/V	**PME Status (PS):** Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	0h RO/V	**PME Requestor ID (RID):** Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set. Root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped.

12.1.22 Device Capabilities 2 (DCAP2)—Offset 64h

This is Device Capabilities 2 register. Refer to register field for more details

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28

Function: 0

Default: 80837h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:18	2h RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b - OBFF is not supported. 01b - OBFF is supported using Message signaling only. 10b - OBFF is supported using WAKE# signaling only. 11b - OBFF is supported using WAKE# and Message signaling. BIOS shall program this field to 00b since OBFF messaging is not supported.
17:12	0h RO	Reserved.
11	1h RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1' or a '0' to enable/disable the root port from declaring support for the LTR capability.
10:6	0h RO	Reserved.
5	1h RO	**ARI Forwarding Supported (AFS):** ARI Forwarding Supported (AFS): Applicable only to Switch Downstream Ports and Root Ports; must be 0b for other Function types. This bit must be set to 1b if a Switch Downstream Port or Root Port supports this optional capability. Note: This bit is not made RWO to simplify implementation, since there is a requirement that the ARI Forwarding Enable bit must be hardwired to 0b if ARI Forwarding Supported bit is 0b. It is low risk to keep this risk 1b. Register Attribute: Static.
4	1h RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	7h RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A [amp] B 0110b Ranges B [amp] C 0111b Ranges A, B [amp] C [lt]-- This is what PCH supports 1110b Ranges B, C [amp] D 1111b Ranges A, B, C [amp] D All other values are reserved.

12.1.23 Device Control 2 And Device Status 2 (DCTL2_DSTS2)—Offset 68h

This is Device Control 2 and Device Status 2 register. Refer to register field for more details

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28

Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10	0h RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect.
9:6	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**ARI Forwarding Enable (AFE):** ARI Forwarding Enable (AFE): When set, the Downstream Port disables its traditional Device Number field being 0b enforcement when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to Extended Functions in an ARI Device immediately below the Port. Register Attribute: Dynamic.
4	0h RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.
3:0	0h RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. The root port targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range A (50us to 10 ms) programmability range is supported: 0001b 90-100us (spec range is 50 us to 100 us) 0010b 9-10ms (spec range is 1ms to 10 ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either on when this value was changed or on when each request was issued.

12.1.24 Link Capabilities 2 (LCAP2)—Offset 6Ch

This is Link Capabilities 2 register. Refer to register field for more details

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28

Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22:16	0h RO	**Lower SKP OS Reception Supported Speeds Vector (LSOSRSS):** Lower SKP OS Reception Supported Speeds Vector(LSOSRSS): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports receiving SKP OS at the rate defined for SRNS while running in SRIS. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
15:9	0h RO	**Lower SKP OS Generation Supported Speeds Vector (LSOSGSSV):** Lower SKP OS Generation Supported Speeds Vector(LSOSGSSV): If this field is non-zero, it indicates that the Port, when operating at the indicated speed(s) supports SRIS and also supports software control of the SKP Ordered Set transmission scheduling rate. Bit definitions within this field are: Bit 0 2.5 GT/s Bit 1 5.0 GT/s Bit 2 8.0 GT/s Bits 6:3 RsvdP Behavior is undefined if a bit is set in this field and the corresponding bit is not set in the Supported Link Speeds Vector.
8	0h RO	**Crosslink Supported (CS):** Crosslink Supported (CS): No support for Crosslink. Register Attribute: Static.
7:1	0h RO/V	**Supported Link Speeds Vector (SLSV):** Supported Link Speeds Vector (SLSV): This field indicates the supported Link speed of the associated Port. For each bit, a value of 1b indicates that the corresponding Link speed is supported; otherwise, the Link speed is not supported. Bit definitions within this field are: Bit 0: 2.5 GT/s. Bit 1: 5.0 GT/s. Bit 2: 8.0 GT/s. Bits [6:3]: Reserved.
0	0h RO	Reserved.

12.1.25 Link Control 2 And Link Status 2 (LCTL2_LSTS2)—Offset 70h

This is Link Control 2 and Link Status 2 register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/1C/V/P	**Link Equalization Request (LER):** Link Equalization Request (LER): This bit is set by hardware to request the Link equalization process to be performed on the Link. Register Attribute: Dynamic.
20	0h RO/V/P	**Equalization Phase 3 Successful (EQP3S):** Equalization Phase 3 Successful (EQP3S): When set to 1, this bit indicates that Phase 3 of the Transmitter Equalization procedure has successfully completed.
19	0h RO/V/P	**Equalization Phase 2 Successful (EQP2S):** Equalization Phase 2 Successful (EQP2S): When set to 1, this bit indicates that Phase 2 of the Transmitter Equalization procedure has successfully completed.
18	0h RO/V/P	**Equalization Phase 1 Successful (EQP1S):** Equalization Phase 1 Successful (EQP1S): When set to 1, this bit indicates that Phase 1 of the Transmitter Equalization procedure has successfully completed.
17	0h RO/V/P	**Equalization Complete (EQC):** Equalization Complete (EC): When set to 1, this bit indicates that the Transmitter Equalization procedure has completed
16	0h RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5.0 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed.
15:12	0h RW/P	**Compliance Preset/De-emphasis (CD):** For 8.0 GT/s Data Rate: This field sets the Transmitter Preset in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Results are undefined if a reserved preset encoding is used when entering Polling.Compliance in this way. For 5.0 GT/s Data Rate: This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 0001b -3.5 dB 0000b -6 dB When the Link is not operating at 2.5 GT/s speed, the setting of this bit has no effect. The default value of this field is 0000b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this field is set to the default value.
11	0h RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b. This bit is applicable when the Link is operating at 2.5 GT/s or 5.0 GT/s data rates only. Register Attribute: Static.
10	0h RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.

Bit Range	Default & Access	Field Name (ID): Description
9:7	0h RW/P	**Transmit Margin (TM):** This field controls the value of the nondeemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate. Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
6	0h RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is not operating at 5.0 GT/s speed, the setting of this bit has no effect. When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.
5	0h RO	**Hardware Autonomous Speed Disable (HASD):** Reserved. This port cannot autonomously change speeds.
4	0h RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b. This bit is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this bit only during debug or compliance testing. In all other cases, the system must ensure that this bit is set to the default value. Register Attribute: Static.
3:0	1h RW/V/P	**Target Link Speed (TLS):** Indicates the target link speed. 1h = Gen 1 speed 2h = Gen 2 speed 3h = Gen 3 speed If a value is written to this field that does not correspond to a supported speed, theresult is undefined. The default value of this field is Gen 1.

12.1.26 Message Signaled Interrupt Identifiers And Message Signaled Interrupt Message Control (MID_MC)—Offset 80h

This is Message Signaled Interrupt Identifiers and Message Signaled Interrupt Message Control register. Refer to register field for more details

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28

Function: 0

Default: 9005h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only.
22:20	0h RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port.
19:17	0h RO	**Multiple Message Capable (MMC):** Only one message is required.
16	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.
15:8	90h RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	5h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

12.1.27 Message Signaled Interrupt Message Address (MA)—Offset 84h

This is Message Signaled Interrupt Message Address register. Refer to register field for more details

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DW aligned.
1:0	0h RO	Reserved.

12.1.28 Message Signaled Interrupt Message Data (MD)—Offset 88h

This is Message Signaled Interrupt Message Data register. Refer to register field for more details

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[lb]15:0[rb]) during the data phase of the MSI memory write transaction.

12.1.29 Subsystem Vendor Capability (SVCAP)—Offset 90h

This is Subsystem Vendor Capability register. Refer to register field for more details

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28
Function: 0

Default: A00Dh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	A0h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	Dh RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

12.1.30 Subsystem Vendor IDs (SVID)—Offset 94h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	0h RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

12.1.31 Power Management Capability And PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28
Function: 0

Default: C8030001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	19h RO	**PME Support (PMES):** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy operating systems to enable PME# in devices connected behind this root port.
26	0h RO	**D2_Support (D2S):** The D2 state is not supported.
25	0h RO	**D1_Support (D1S):** The D1 state is not supported.
24:22	0h RO	**Aux_Current (AC):** Reports 375mA maximum suspend well current required when in the D3COLD state.
21	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
20	0h RO	Reserved.
19	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
18:16	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	0h RO	**Next Capability (NEXT):** Indicates this is the last item in the list.
7:0	1h RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability.

12.1.32 PCI Power Management Control And Status (PMCS)—Offset A4h

This is PCI Power Management Control And Status register. Refer to register field for more details

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28

Function: 0

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Data (DTA):** Reserved
23	0h RO	**Bus Power / Clock Control Enable (BPCE):** Reserved per PCI Express specification
22	0h RO	**B2/B3 Support (B23S):** Reserved per PCI Express specification.
21:16	0h RO	Reserved.
15	0h RO	**PME Status (PMES):** Indicates a PME was received on the downstream link.
14:13	0h RO	**Data Scale (DSC):** Reserved
12:9	0h RO	**Data Select (DSEL):** Reserved
8	0h RW/P	**PME Enable (PMEE):** Indicates PME is enabled. The root port takes no action on this bit, but it must be RW for legacy operating systems to enable PME# on devices connected to this root port.
7:4	0h RO	Reserved.
3	1h RW/O	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 - D0 state 11 - D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10' or '01' to these bits, the write will be ignored.

12.1.33 Additional Configuration 1 (CCFG)—Offset D0h

BIOS may need to program this register.

12.1.34 Miscellaneous Port Configuration 2 (MPC2)—Offset D4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW	**ASPM Control Override Enable (ASPMCOEN):** When set to '1', the PCIe Root Port will use the values in the ASPM Control Override registers instead of ASPM Registers in the Link Control register. This register allows BIOS to control the DMI ASPM settings instead of the OS.
3:2	0h RW	**ASPM Control Override (ASPMCO):** Provides BIOS control of whether root port should enter L0s or L1 or both. 00 = Disabled 01 = L0s Entry Enabled 10 = L1 Entry Enabled 11 = L0s and L1 Entry Enabled.
1	0h RW	**EOI Forwarding Disable (EOIFD):** 0 = Broadcast EOI messages that are sent on the backbone are claimed by this port and forwarded across the PCIe* link. 1 = Broadcast EOI messages are not claimed on the backbone by this port and will not be forwarded across the PCIe* Link.
0	0h RW	**L1 Completion Timeout Mode (L1CTM):** 0 = PCI Express* Specification Compliant. Completion timeout is disabled during software initiated L1, and enabled during ASPM initiate L1. 1 = Completion timeout is enabled during L1, regardless of how L1 entry was initiated.

12.1.35 Miscellaneous Port Configuration (MPC)—Offset D8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 1110000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Power Management SCI Enable (PMCE):** 0 = SCI generation based on a power management event is disabled. 1 = Enables the root port to generate SCI whenever a power management event is detected.
30	0h RW	**Hot Plug SCI Enable (HPCE):** 0 = SCI generation based on a hot-plug event is disabled. 1 = Enables the root port to generate SCI whenever a hot-plug event is detected.
29	0h RW/L	**Link Hold Off (LHO):** When set, the port will not take any TLP. This is used during loopback mode to fill up the downstream queue. This register bit is Read-Only when the MPC.SRL bit is set.
28	0h RW/L	**Address Translater Enable (ATE):** Used to enable address translation via the AT bits in this register during loopback mode. 0: Disable 1: Enable
27	0h RO	Reserved.
26	0h RW/L	**Port8xh Decode Enable (P8XDE):** When set, allows PCIe Root Port to claim I/O cycles within the range from 80h - 8Fh inclusive and forwarding the cycle to the link. The claiming of these cycles are independent of I/O Base/Limit and IO Space Enable bits. BIOS must ensure that at any one time, no more than one PCIe Root Port are enabled to claim Port 8xh cycles.
25	0h RW/L	**Invalid Receive Range Check Enable (IRRCE):** When set, the receive transaction layer will treat the TLP as an Unsupported Request error if the address range of a Memory request does not fall outside the range between prefetchable and non-prefetchable base and limit. Messages, IO, Config, and Completions are never checked for valid address ranges This register bit is Read-Only when the MPC.SRL bit is set.
24	1h RW/L	**BME Receive Check Enable (BMERCE):** When set, the receive transaction layer will treat the TLP as an Unsupported Request error if a memory or I/O read or write request is received and the Bus Master Enable bit is not set. Messages, Config, and Completions are never checked for BME. This register bit is Read-Only when the MPC.SRL bit is set.
23	0h RW/O	**Secured Register Lock (SRL):** When this bit is set, all the secured registers will be locked and will be Read-Only. The following fields are locked by MPC.SRL: CCFG.CRE. CCFG.IORE. MPC.LHO. MPC.ATE. MPC.P8XDE. MPC.IRRCE. MPC.BMERCE. MPC.FORCEDET. MPC.MCTPSE. MPC.MMBNCE. PCIECMMPC.START. PCIEDBG.REUTLPBKME PCIEDBG.REUTFLPBKME. PCIEDBG.NEDLBE. PCIEDBG.IRFELB. PCIEDBG.SCMBB. PCIE.SE.
22	0h RO	Reserved.
21	0h RW	**Flow Control During L1 Entry (FCDL1E):** br]0: No flow control update DLLPs sent during L1 Ack transmission 1: Flow control update DLLPs sent during L1 Ack transmission as required to meet the 30us periodic flow control update.
20:18	4h RW	**Unique Clock Exit Latency (UCEL):** This value represents the L0s Exit Latency for unique-clock configurations (LCTL.CCC = '0'). It defaults to 512ns to less than 1us, but may be overridden by BIOS.
17:15	2h RW	**Common Clock Exit Latency (CCEL):** This value represents the L0s Exit Latency for common-clock configurations (LCTL.CCC = '1'). It defaults to 128ns to less than 256ns, but may be overridden by BIOS.

Bit Range	Default & Access	Field Name (ID): Description
14:13	0h RW	**PCIe MEx Speed Disable (PCIEMEXSD):** When operating as PCI Express: 00: PCIe supported data rate is as defined by the Supported Link Speed and Target Link Speed register. 01: PCIe supported data rate is limited to just 2.5 GT/s. Supported Link Speed field will reflect 0000001b. Max Link Speed field will reflect 0001b. 10: PCIe supported data rate is limited to 2.5 GT/s and 5.0 GT/s. Supported Link Speed register will reflect 0000011b. Max Link Speed field will reflect 0010b. 11: Reserved. When operating as Mobile Express: 00: MEx supported data rate is as defined by the Supported Link Speed and Target Link Speed register. 01: MEx supported data rate is limited to just HS-G1. Supported Link Speed field will reflect 0000001b. Max Link Speed field will reflect 0000b. 10: PCIe supported data rate is limited to HS-G1 and HS-G2. Supported Link Speed register will reflect 0000001b. Max Link Speed field will reflect 0000b. 11: Reserved. When this bit is changed, link retrain needs to be performed for the change to be effective. Register Attribute: Static.
12:8	0h RO	Reserved.
7	0h RW	**Port I/OxApic Enable (PAE):** When set, a range is opened through the bridge for the following memory addresses: Port# Address 1 FEC1_0000h - FEC1_7FFFh 2 FEC1_8000h - FEC1_FFFFh 3 FEC2_0000h - FEC2_7FFFh 4 FEC2_8000h - FEC2_FFFFh 5 FEC3_0000h - FEC3_7FFFh 6 FEC3_8000h - FEC3_FFFFh 7 FEC4_0000h - FEC4_7FFFh 8 FEC4_8000h - FEC4_FFFFh When cleared, the hole is disabled.
6:3	0h RO	Reserved.
2	0h RW/O	**Bridge Type (BT):** This register can be used to modify the Base Class and Header Type fields from the default PCI-to-PCI bridge to a Host Bridge. Having the root port appear as a Host Bridge is useful in some server configurations. 0 = The root port bridge type is a PCI-to-PCI Bridge, Header Sub-Class = 04h, and Header Type = Type 1. 1 = The root port bridge type is a PCI-to-PCI Bridge, Header Sub-Class = 00h, and Header Type = Type 0.
1	0h RW	**Hot Plug SMI Enable (HPME):** 0 = SMI generation based on a hot-plug event is disabled. 1 = Enables the root port to generate SMI whenever a hot-plug event is detected.
0	0h RW	**Power Management SMI Enable (PMME):** 0 = SMI generation based on a power management event is disabled. 1 = Enables the root port to generate SMI whenever a power management event is detected.

12.1.36 SMI And SCI Status (SMSCS)—Offset DCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C/V	**Power Management SCI Status (PMCS):** This bit is set if the root port PME control logic needs to generate an interrupt, and this interrupt has been routed to generate an SCI.
30	0h RW/1C/V	**Hot Plug SCI Status (HPCS):** This bit is set if the hot plug controller needs to generate an interrupt, and has this interrupt been routed to generate an SCI.
29:5	0h RO	Reserved.
4	0h RW/1C/V	**Hot Plug Link Active State Changed SMI Status (HPLAS):** This bit is set when SLSTS.DLLSC transitions from '0' to '1', and MPC.HPME is set. When this bit is set, an SMI# will be generated.
3:2	0h RO	Reserved.
1	0h RW/1C/V	**Hot Plug Presence Detect SMI Status (HPPDM):** This bit is set when SLSTS.PDC transitions from '0' to'1', and MPC.HPME is set. When this bit is set, an SMI# will be generated.
0	0h RW/1C/V	**Power Management SMI Status (PMMS):** This bit is set when RSTS.PS transitions from '0' to'1', and MPC.PMME is set.

12.1.37 Scratch Pad Register, Root Port Dynamic Clock Gate Enable And Root Port Power Gating Enable (SPR_RPDCGEN_RPPGEN)—Offset E0h

BIOS may program this register.

12.1.38 Chipset Initialization Register 0EC (DC)—Offset ECh

BIOS may program this register.

12.1.39 Chipset Initialization Register 0F0 (IPCS)—Offset F0h

BIOS may program this register.

12.1.40 Advanced Error Extended Reporting Capability Header (AECH)—Offset 100h

Size:32 bits
The AER capability can optionally be included or excluded from the capabilities list. The full AER is supported.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Set to 000h as this is the last capability in the list. Point to the next capability.
19:16	0h RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0
15:0	0h RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0

12.1.41 Uncorrectable Error Status (UES)—Offset 104h

This register must maintain its state through a platform reset. It loses its state upon loss of core power.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/1C/V/P	**ACS Violation Status (AVS):** Indicates an ACS Violation is logged
20	0h RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0h RO	**ECRC Error Status (EE):** ECRC is not supported.
18	0h RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0h RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0h RW/1C/V/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received.
15	0h RW/1C/V/P	**Completor Abort Status (CA):** Indicates a completer abort was received
14	0h RW/1C/V/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value
13	0h RO	**Flow Control Protocol Error Status (FCPE):** Not supported.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.
11:6	0h RO	Reserved.
5	0h RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported.
4	0h RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	0h RO	Reserved.
0	0h RO	**Training Error Status (TE):** Not supported.

12.1.42 Uncorrectable Error Mask (UEM)—Offset 108h

When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/P	**ACS Violation Mask (AVM):** Mask for ACS Violation errors
20	0h RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0h RO	**ECRC Error Mask (EE):** ECRC is not supported.
18	0h RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs
17	0h RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.
16	0h RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions.
15	0h RW/P	**Completor Abort Mask (CM):** Mask for completer abort.
14	0h RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**Flow Control Protocol Error Mask (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:6	0h RO	Reserved.
5	0h RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported.
4	0h RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	0h RO	Reserved.
0	0h RO	**Training Error Mask (TE):** Not supported.

12.1.43 Uncorrectable Error Severity (UEV)—Offset 10Ch

This register gives the option to make an uncorrectable error fatal or non-fatal. An error is fatal if the bit is set. An error is non-fatal if the bit is cleared. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28
Function: 0

Default: 60011h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/P	**ACS Violation Severity (AVS):** Severity for ACS violation.
20	0h RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0h RO	**ECRC Error Severity (EE):** ECRC is not supported.
18	1h RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.
17	1h RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0h RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception.
15	0h RW/P	**Completor Abort Severity (CA):** Severity for completer abort.
14	0h RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout.

Bit Range	Default & Access	Field Name (ID): Description
13	0h RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.
11:6	0h RO	Reserved.
5	0h RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported.
4	1h RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	0h RO	Reserved.
0	1h RO	**Training Error Severity (TE):** TE not supported. This bit is left as RO='1' for ease of implementation..

12.1.44 Correctable Error Status (CES)—Offset 110h

This register is only reset by a loss of core power

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that an Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.
11:9	0h RO	Reserved.
8	0h RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.
7	0h RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	0h RO	Reserved.
0	0h RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

12.1.45 Correctable Error Mask (CEM)—Offset 114h

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28

Function: 0

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	1h RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0h RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	0h RO	Reserved.
8	0h RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0h RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.
6	0h RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.
5:1	0h RO	Reserved.
0	0h RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

12.1.46 Advanced Error Capabilities And Control (AECC)—Offset 118h

This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RO	**ECRC Check Enable (ECE):** ECRC is not supported.
7	0h RO	**ECRC Check Capable (ECC):** ECRC is not supported.
6	0h RO	**ECRC Generation Enable (EGE):** ECRC is not supported.
5	0h RO	**ECRC Generation Capabile (EGC):** ECRC is not supported.
4:0	0h RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register.

12.1.47 Root Error Command (REC)—Offset 12Ch

This register allows errors to generate interrupts.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device.
1	0h RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device.
0	0h RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device.

12.1.48 Root Error Status (RES)—Offset 130h

This register can track more than one error and set the multiple bits if a second or subsequent error occurs and the first has not been serviced. This register is only reset by a loss of power.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Advanced Error Interrupt Message Number (AEMN):** Reserved. There is only one error interrupt allocated.
26:7	0h RO	Reserved.
6	0h RW/1C/V/P	**Fatal Error Message Received (FEMR):** Set when one or more Fatal Uncorrectable Error Messages have been received.
5	0h RW/1C/V/P	**Non-Fatal Error Messages Received (NFEMR):** Set when one or more Non-Fatal Uncorrectable error messages have been received
4	0h RW/1C/V/P	**First Uncorrectable Fatal (FUF):** Set when the first Uncorrectable Error message received is for a fatal error.
3	0h RW/1C/V/P	**Multiple ERR_FATAL/NONFATAL Received (MENR):** Set when either a fatal or a non-fatal error is received and the ENR bit is already set.
2	0h RW/1C/V/P	**ERR_FATAL/NONFATAL Received (ENR):** Set when either a fatal or a non-fatal error message is received.
1	0h RW/1C/V/P	**Multiple ERR_COR Received (MCR):** Set when a correctable error message is received and the CR bit is already set.
0	0h RW/1C/V/P	**ERR_COR Received (CR):** Set when a correctable error message is received.

12.1.49 Error Source Identification (ESID)—Offset 134h

Size:32 bits
Identifies the source (Requester ID) of the first correctable and uncorrectable (Non-Fatal / Fatal) errors reported in the Root Error Status register. This register is only reset by a loss of core power.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message with the ERR_FATAL/NONFATAL Received register is not already set.
15:0	0h RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the Requester ID indicated in the received ERR_COR Message with the ERR_COR Received register is not already set.

12.1.50 L1 Sub-States Extended Capability Header (L1SECH)—Offset 200h

Size:32 bits
Note: When operating in Mobile Express mode, this capability should not be enabled.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 1h
15:0	0h RW/O	**PCI Express Extended Capability ID (PCIEEC):** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. For systems that support L1 Sub-State Extended Capability, BIOS should set this field to 001Eh. .

12.1.51 L1 Sub-States Capabilities (L1SCAP)—Offset 204h

This is L1 Sub-States Capabilities register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 28281Fh

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:19	5h RW/O	**Port Tpower_on Value (PTV):** Along with the Port T_POWER_ON Scale Field in the L1 Substates Capabilities register sets theTime (in us) that this Port requires the port on the opposite side of Link to wait in L1.OFF_EXIT after sampling CLKREQ# asserted before actively driving the interface. Port Tpower_on is calculated by multiplying the value in this field by the value in the Port Tpower_on scale field in the L1 Sub-States Capabilities 2 register. Required for all Ports that support L1.OFF.
18	0h RO	Reserved.
17:16	0h RW/O	**Port Tpower_on Scale (PTPOS):** Specifies the scale used for Tpower_on value field in the L1 Substates Capabilities register. 00b: 2us 01b: 10us 10b: 100us 11b: Reserved Required for all Ports that support L1.OFF.
15:8	28h RW/O	**Port Common Mode Restore Time (PCMRT):** This is the time (in us) required for this Port to re-establish common mode. Required for all ports that support L1.OFF.
7	0h RO	Reserved.
6	0h RW/1C/V	**L1-Substate Exit Interrupt Status (L1SSEIS):** CLKREQ# Acceleration Interrupt Status - For a Downstream Port that has both the CLKREQ# Acceleration Supported and CLKREQ# Acceleration Interrupt Enable bits Set, when set this bit indicates that the Port has completed the CLKREQ# Acceleration Link Activation process, and that the Link has reached L0. Software must then clear this bit by writing a 1b to this bit. Must be hardwired to 0b for Upstream Ports. Default value is 0b.
5	0h RO	Reserved.
4	1h RW/O	**L1 PM Substates Supported (L1PSS):** When Set this bit indicates that this Port supports L1 PM Substates. For compatibility with possible future extensions, software must not enable L1 PM Substates unless this bit is set. This RWO field must be programmed prior to enabling ASPM. Required for both Upstream and Downstream Ports.
3	1h RW/O	**ASPM L1.1 Substates Supported (AL11S):** When set, this bit indicates that this port supports L1 substates for ASPM L1.SNOOZ is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
2	1h RW/O	**ASPM L1.2 Supported (AL12S):** When set, this bit indicates that ASPM_L1.OFF is supported. Required for both Upstream and Downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
1	1h RW/O	**PCI-PM L1.1 Supported (PPL11S):** When set, this bit indicates that L1.SNOOZ sub-state is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static
0	1h RW/O	**PCI-PM L1.2 Supported (PPL12S):** When set, this bit indicates that PCI-PM L1.OFF power management feature is supported. Required for both upstream and downstream ports. This RWO field must be programmed prior to enabling ASPM. Register Attribute: Static

12.1.52 L1 Sub-States Control 1 (L1SCTL1)—Offset 208h

This is L1 Sub-States Control 1 register. Refer to register field for more details

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**L1.2 LTR Threshold Latency ScaleValue (L12LTRTLSV):** This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular PCIe Root Port. The value in this field, together with L12LTRTLV is compared against both the snoop and non-snoop LTR values of the device. 000: L12LTRSTLV times 1 ns 001: L12LTRSTLV times 32 ns 010: L12LTRSTLV times 1024 ns 011: L12LTRSTLV times 32768 ns 100: L12LTRSTLV times 1048576 ns 101: L12LTRSTLV times 33554432 ns Others: Not Permitted. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
28:26	0h RO	Reserved.
25:16	0h RW	**L1.2 LTR Threshold Latency Value (L12OFFLTRTLV):** This field contains the L1.2 LTR Threshold Latency Value for this particular PCIe Root Port. The value in this field, together with L12LTRTLSV is compared against both the snoop and non-snoop LTR values of the device. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
15:8	0h RW	**Common Mode Restore Time (CMRT):** This is the Tcommon_mode time (in us) the PCIe Root Port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
7:6	0h RO	Reserved.
5	0h RW	**L1-Substate Exit Control (L1SSEC):** L1 Substate Exit Control - For a Downstream Port, when any one or more of the PCI-PM L1.2 Enable, PCI-PM L1.1 Enable, {ASPM L1.2 Enable, ASPM L1.1 Enable} bit are Set, then when this bit is Set, the Port must initiate the CLKREQ# Acceleration Link Activation process, and once the Link reaches L0, the Port continues to attempt to maintain the Link in L0 for as long as this bit remains Set.
4	0h RO	Reserved.
3	0h RW	**ASPM L1.1 Enabled (AL11E):** When set, this bit indicates that ASPM L1.SNOOZ substates are enabled for ASPM. Required for both upstream and downstream ports. Register Attribute: Dynamic

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**ASPM L1.2 Enable (AL12E):** When set, this bit indicates that ASPM L1.OFF substates are enabled for PCI-PM. Required for both upstream and downstream ports. Register Attribute: Dynamic.
1	0h RW	**PCI-PM L1.SNOOZ Enable (PPL11E):** When set, this bit indicates that PCI-PM L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled. This field must be programmed prior to enabling ASPM L1. Register Attribute: Dynamic.
0	0h RW	**PCI-PM L1.2 Enabled (PPL12E):** When set, this bit indicates that PCI-PM L1.OFF power management feature is enabled. L1.OFF can only be enabled if the platform supports bi-directional CLKREQPLUS#. This field must be programmed prior to enabling ASPM L1. Ports that support L1.OFF shall support Latency Tolerance Reporting. Register Attribute: Dynamic

12.1.53 L1 Sub-States Control 2 (L1SCTL2)—Offset 20Ch

This is L1 Sub-States Control 2 register. Refer to register field for more details

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28

Function: 0

Default: 28h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:3	5h RW	**Power On Wait Time (POWT):** Along with the Tpower_on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# is sampled asserts in L1.OFF state. Tpower_on value is calculated by multiplying the value in this field by the value in the TPOS field. This field must be programmed prior to enabling L1.OFF. Register Attribute: Static
2	0h RO	Reserved.
1:0	0h RW	**Tpower_on Scale (TPOS):** Specifies the scale used for Tpower_on value. 00b: 2 us 01b: 10 us 10b: 100us 11b: Reserved. Required for all Ports that support L1.OFF. Register Attribute: Static

12.1.54 ACS Extended Capability Header (ACSECH)—Offset 220h

Size:32 bits

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): For systems that support ACS Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0h RW/O	**Capability ID (CID):** Capability ID (CID): For systems that support ACS Extended Capability, BIOS should write a 000Dh to this register else it should write 0.

12.1.55 ACS Capability Register And ACS Control Register (ACSCAPR_ACSCTLR)—Offset 224h

This is ACS Capability Register and ACS Control register. Refer to register field for more details

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28
Function: 0

Default: 1Bh

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22	0h RO	**ACS Direct Translated P2P Enable (TE):** ACS Direct Translated P2P Enable (T): ACS Direct Translated P2P is not supported.
21	0h RO	**ACS P2P Egress Control Enable (EE):** ACS P2P Egress Control Enable (E): ACS P2P Egress Control is not supported.
20	0h RW	**ACS Upstream Forwarding Enable (UE):** When set, the component forwards upstream any Request or Completion TLPs it receives that were redirected upstream by a component lower in the hierarchy. Note that the U bit only applies to upstream TLPs arriving at a Downstream Port, and whose normal routing targets the same Downstream Port. Upstream I/O, Configuration, VDM Message, Message are never affected by ACS Upstream Forwarding Enable. Register Attribute: Static
19	0h RW	**ACS P2P Completion Redirect Enable (CE):** ACS P2P Completion Redirect (C): Determines when the component redirects peer-to-peer Completions upstream; applicable only to Read Completions whose Relaxed Ordering Attribute is clear. Requests are never affected by ACS P2P Completion Redirect. Default value of this field is 0b. Register Attribute: Static.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**ACS P2P Request Redirect Enable (RE):** ACS P2P Request Redirect Enable (R): Determines when the component redirects peer-to-peer memory Requests targeting another peer port upstream. I/O, Configuration, VDM Messages and Completions are never affected by ACS P2P Request Redirect. Default value of this field is 0b. Register Attribute: Static.
17	0h RW	**ACS Translation Blocking Enable (BE):** ACS Translation Blocking Enable (B): When set, the component blocks all upstream Memory Requests whose Address Translation (AT) field is not set to the default value. I/O, Configuration, Completions and Messages are never affected by ACS Translation Blocking. Default value of this field is 0b. Register Attribute: Static.
16:7	0h RO	Reserved.
6	0h RO	**ACS Direct Translated P2P (T):** ACS Direct Translated P2P (T): ACS Direct Translated P2P is not supported.
5	0h RO	**ACS P2P Egress Control (E):** ACS P2P Egress Control (E): ACS P2P Egress Control is not supported.
4	1h RW/O	**ACS Upstream Forwarding (U):** Required for Root Ports if the RC supports Redirected Request Validation: required for Switch Downstream Ports: must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Upstream Forwarding Register Attribute: Static
3	1h RW/O	**ACS P2P Completion Redirect (C):** ACS P2P Completion Redirect (C): Required for all Functions that support ACS P2P Request Redirect; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS P2P Completion Redirect. Register Attribute: Static.
2	0h RO	Reserved.
1	1h RW/O	**ACS Translation Blocking (B):** ACS Translation Blocking (B): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Translation Blocking. Register Attribute: Static.
0	1h RW/O	**ACS Source Validation (V):** ACS Source Validation (V): Required for Root Ports and Switch Downstream Ports; must be hardwired to 0b otherwise. If 1b, indicates that the component implements ACS Source Validation. Register Attribute: Static.

12.1.56 PCI Express Replay Timer Policy 1 (PCIERTP1)—Offset 300h

The Replay Timer controlled by the Replay Timeout field is started when the Retry Buffer is empty and a TLP is placed into it or an Ack/Nak DLLP is received and there are still non-acknowledged packets within the Retry Buffer. The counter continues to count until the next valid Ack DLLP or a NAK DLLP that acknowledges unacknowledged TLPs is received, or it reaches the timeout value specified by this register. When a valid Ack/Nak DLLP is received, the timer is reset to zero and restarted if there are still non-acknowledged packets within the Retry Buffer. Otherwise if the Retry Buffer is empty, the counter is just reset to zero. If the timer reaches the timeout value, the non-acknowledged packets within the Retry Buffer will be replayed.
The default for this register is dependant on the MAX_PAYLOAD_SIZE , the NEGOTIATED_WIDTH, and the NEGOTIATED_SPEED.

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28

Function: 0

Default: A64F96h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	Ah RW	**Gen 2 x1 (G2X1):** Gen 2 x1 (G2X1): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 7) * 64 link clocks. For PCIE Gen 2 speed and x1 width For Mobile Express HS-Gear 3 speed and x1 width. Register Attribute: Static.
19:16	6h RW	**Gen 2 x2 (G2X2):** Gen 2 x2 (G2X2): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 4) * 64 link clocks. For PCIe Gen 2 speed and x2 width. For Mobile Express HS-Gear 3 speed and x2 width. Register Attribute: Static.
15:12	4h RW	**Gen 2 x4 (G2X4):** Gen 2 x4 (G2X4): Determines how many link clock cycles the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For PCIe Gen 2 speed and x4 width. For Mobile Express HS-Gear 3 speed and x4 width. Register Attribute: Static.

Bit Range	Default & Access	Field Name (ID): Description
11:8	Fh RW	**Gen 1 x1 (G1X1):** Gen 1 x1 (G1X1): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 10) * 64 link clocks. For 512B MPS: (nnn + 17) * 64 link clocks. For PCIe Gen 1 speed and x1 width. For Mobile Express HS-Gear 2 speed and x1 width. Register Attribute: Static.
7:4	9h RW	**Gen 1 x2 (G1X2):** Gen 1 x2 (G1X2): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 4) * 64 link clocks. For 512B MPS: (nnn + 8) * 64 link clocks. For PCIe Gen 1 speed and x2 width. For Mobile Express HS-Gear 2 speed and x2 width. Register Attribute: Static.
3:0	6h RW	**Gen 1 x4 (G1X4):** Gen 1 x4 (G1X4): Determines how many symbol times (i.e. number of link clock cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. The Replay Timeout value to be used varies based on the effective Maximum Payload Size. For 128B MPS: nnn * 64 link clocks. For 256B MPS: (nnn + 2) * 64 link clocks. For 512B MPS: (nnn + 3) * 64 link clocks. For PCIe Gen 1 speed and x4 width. For Mobile Express HS-Gear 2 speed and x4 width. Register Attribute: Static.

12.1.57 PCI Express NFTS (PCIENFTS)—Offset 314h

BIOS may program this register.

12.1.58 PCI Express L0s Control (PCIEL0SC)—Offset 318h

BIOS may program this register.

12.1.59 PCI Express Configuration (PCIECFG2)—Offset 320h

BIOS may program this register.

12.1.60 Chipset Initialization Register 39C (PTMPSDC1)—Offset 39Ch

BIOS may program this register.

12.1.61 Chipset Initialization Register 3A0 (PTMPSDC2)—Offset 3A0h

BIOS may program this register.

12.1.62 Chipset Initialization Register 3A4 (PTMPSDC3)—Offset 3A4h

BIOS may program this register.

12.1.63 Chipset Initialization Register 3A8 (PTMPSDC4)—Offset 3A8h

BIOS may program this register.

12.1.64 Chipset Initialization Register 3AC (PTMPSDC5)—Offset 3ACh

BIOS may program this register.

12.1.65 Chipset Initialization Register 3B0 (PTMECFG)—Offset 3B0h

BIOS may program this register.

12.1.66 Chipset Initialization Register 400 (LTROVR)—Offset 400h

BIOS may program this register.

12.1.67 Chipset Initialization Register 404 (LTROVR2)—Offset 404h

BIOS may program this register.

12.1.68 Chipset Initialization Register 408 (PHYCTL4)—Offset 408h

BIOS may program this register.

12.1.69 Chipset Initialization Register 420 (PCIEPMECTL)—Offset 420h

BIOS may program this register.

12.1.70 Chipset Initialization Register 424 (PCIEPMECTL2)—Offset 424h

BIOS may program this register.

12.1.71 Chipset Initialization Register 428 (PCE)—Offset 428h

BIOS may program this register.

12.1.72 Chipset Initialization Register 450 (EQCFG1)—Offset 450h

BIOS may program this register.

12.1.73 Chipset Initialization Register 454 (RTPCL1)—Offset 454h

BIOS may program this register.

12.1.74 Chipset Initialization Register 458 (RTPCL2)—Offset 458h

BIOS may program this register.

12.1.75 Chipset Initialization Register 45C (RTPCL3)—Offset 45Ch

BIOS may program this register.

12.1.76 Chipset Initialization Register 460 (RTPCL4)—Offset 460h

BIOS may program this register.

12.1.77 Chipset Initialization Register 464 (FOMS)—Offset 464h

BIOS may program this register.

12.1.78 Chipset Initialization Register 468 (HAEQ)—Offset 468h

BIOS may program this register.

12.1.79 Chipset Initialization Register 470 (LTCO1)—Offset 470h

BIOS may program this register.

12.1.80 Chipset Initialization Register 474 (LTCO2)—Offset 474h

BIOS may program this register.

12.1.81 Chipset Initialization Register 478 (G3L0SCTL)—Offset 478h

BIOS may program this register.

12.1.82 Chipset Initialization Register 47C (EQCFG2)—Offset 47Ch

BIOS may program this register.

12.1.83 Chipset Initialization Register 480 (MM)—Offset 480h

BIOS may program this register.

12.1.84 DPC Extended Capability Header (DPCECH)—Offset A00h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Points to the next capability.
19:16	0h RW/O	**Capability Version (CV):** For systems that support DPC Extended Capability, BIOS should write a 1h to this register else it should write 0.
15:0	0h RW/O	**Capability ID (CID):** For systems that support DPC Extended Capability, BIOS should write a 001Dh to this register else it should write 0.

12.1.85 Secondary PCI Express Extended Capability Header (SPEECH)—Offset A30h

Note: When operating in Mobile Express mode, this capability should not be enabled.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 28
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/O	**Next Capability Offset (NCO):** Next Capability Offset (NCO): This field contains the offset to the next PCI Express Capability structure or 000h if no other items exist in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible Configuration Space and thus must always be either 000h (for terminating list of Capabilities) or greater than 0FFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b and software must mask them to allow for future uses of these bits.
19:16	0h RW/O	**Capability Version (CV):** Capability Version (CV): This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 1h to this register else it should write 0
15:0	0h RW/O	**PCI Express Extended Capability ID (PCIEECID):** PCI Express Extended Capability ID (PCIEECID): This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. PCI Express Extended Capability ID for the Secondary PCI Express Extended Capability is 0019h. For systems that support Secondary PCI Express Extended Capability, BIOS should write a 0019h to this register else it should write 0.

13 I2C Interface (D25: F0-F2, D21:F0-F3)

13.1 I2C PCI Configuration Registers Summary

Table 13-1. Summary of I2C PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID (DEVVENDID)—Offset 0h	XXXX8086h
4h	7h	Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	Revision ID and Class Code (REVCLASSCODE)—Offset 8h	C8000XXh
Ch	Fh	Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	800000h
10h	13h	Base Address (BAR)—Offset 10h	4h
14h	17h	Base Address Register High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	Base Address 1 (BAR1)—Offset 18h	4h
1Ch	1Fh	Base Address 1 High (BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	Interrupt Register (INTERRUPTREG)—Offset 3Ch	0h
80h	83h	Power Management Capability ID (POWERCAPID)—Offset 80h	39001h
84h	87h	Power Management Control and Status (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
98h	9Bh	SW LTR update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	2101h
9Ch	9Fh	Device IDLE Pointer (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	24C1h
A0h	A3h	Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	F0800h
B0h	B3h	General Purpose Read Write 1 (GEN_REGRW1)—Offset B0h	0h
B4h	B7h	General Purpose PCI Read Write 2 (GEN_REGRW2)—Offset B4h	0h
B8h	BBh	General Purpose PCI Read Write 3 (GEN_REGRW3)—Offset B8h	0h
BCh	BFh	General Purpose PCI Read Write 4 (GEN_REGRW4)—Offset BCh	0h
C0h	C3h	General Purpose Input (GEN_INPUT_REG)—Offset C0h	0h

13.1.1 Device ID and Vendor ID (DEVVENDID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: XXXX8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	-- RO/P	**Device ID Field (DEVICEID):** This is a 16-bit value assigned to the controller. Refer the Device and Revision ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor ID Field (VENDORID):** Identifies the manufacturer of the device. 8086h = Intel.

13.1.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 100000h

Bit Range	Default and Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**RMA Field (RMA):** S/W writes a '1' to this bit to clear it.
28	0h RW/1C	**RTA Field (RTA):** S/W writes a '1' to this bit to clear it.
27:21	0h RO	Reserved.
20	1h RO	**Cap List Field (CAPLIST):** Indicates that the controller contains a capabilities pointer list.
19	0h RO	**Intrerrupt Status Field (INTR_STATUS):** This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit is a 0 and this Interrupt Status bit is a 1, will the device's/function's interrupt message be sent. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable Field (INTR_DISABLE):** Setting this bit disables INTx assertion. The interrupt disabled is legacy INTx# interrupt. This bit has no connection with interrupt status bit.
9	0h RO	Reserved.
8	0h RW	**SERR Enable Field (SERR_ENABLE):** Not implemented.
7:3	0h RO	Reserved.
2	0h RW	**BME Field (BME):** If this bit is 0, the controller does not generate any new upstream transaction as a master.
1	0h RW	**MSE Field (MSE):** 0 = Disables memory mapped Configuration space. 1 = Enables memory mapped Configuration space.
0	0h RO	Reserved.

13.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: C8000XXh

Bit Range	Default and Access	Field Name (ID): Description
31:8	C8000h RO	**Class Code (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	-- RO/P	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

13.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 800000h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**MultiFunction Device Field (MULFNDEV):** 0 = Single Function Device 1 = Multi Function device
22:16	0h RO	**Header Type Field (HEADERTYPE):** Implements Type 0 Configuration header.
15:8	0h RO	**Latency Timer Field (LATTIMER):** Hardwired to 0.
7:0	0h RW/P	**Cache Line Size Field (CACHELINE_SIZE)**

13.1.5 Base Address (BAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW	**Base Address Field (BASEADDR):** Provides system memory base address for the controller.
11:4	0h RO	**Size Field (SIZEINDICATOR):** Always returns 0. The size of this register depends on the size of the memory space.
3	0h RO	**Prefetchable Field (PREFETCHABLE):** 0 indicates that this BAR is not prefetchable.
2:1	2h RO	**Type Field (TYPE):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE):** 0 indicates this BAR is present in the memory space.

13.1.6 Base Address Register High (BAR_HIGH)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address High Field (BASEADDR_HIGH)**

13.1.7 Base Address 1 (BAR1)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW	**Base Address Field (BASEADDR1):** This field is present if BAR1 is enabled.
11:4	0h RO	**Size Field (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable Field (PREFETCHABLE1):** 0 indicates that this BAR is not prefetchable.
2:1	2h RO	**Type Field (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Message Space Field (MESSAGE_SPACE1):** 0 Indicates this BAR is present in the memory space.

13.1.8 Base Address 1 High (BAR1_HIGH)—Offset 1Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address High Field (BASEADDR1_HIGH)**

13.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/O/P	**Subsystem ID Field (SUBSYSTEMID):** The register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other. This register is a Read Write Once type register.
15:0	0h RW/O/P	**Subsystem Vendor Field (SUBSYSTEMVENDORID):** The register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other. This register is a Read Write Once register.

13.1.10 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Capabilities Pointer register indicates what the next capability is

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**Capabilities Pointer Field (CAPPTR_POWER):** Indicates what the next capability is.

13.1.11 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	**Max Latency Field (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**Min Gnt Field (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma
15:12	0h RO	Reserved.
11:8	0h RO	**Interrupt Pin Field (INTPIN)**
7:0	0h RW/P	**Int Line Field (INTLINE):** It is used to communicate to software, the interrupt line to which the interrupt pin is connected.

13.1.12 Power Management Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 39001h

Bit Range	Default and Access	Field Name (ID): Description
31:27	0h RO	**PME Support Field (PMESUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for for a bit indicates that the function is not capable of asserting the PME# signal while in that power state. Bit 27 = 1: PME# can be asserted from D0. Bit 30 = 1: PME# can be asserted from D3 hot. Other bits are not used.
26:19	0h RO	Reserved.
18:16	3h RO	**Version Field (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**Next Cap Field (NXTCAP):** Points to the next capability structure.
7:0	1h RO	**Power Capability ID Field (POWER_CAP):** Indicates power management capability.

13.1.13 Power Management Control and Status (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C/P	**PME Status Field (PMESTATUS)**
14:9	0h RO	Reserved.
8	0h RW/P	**PME Enable Field (PMEENABLE):** 0 = PME message is disabled 1 = PME message is enabled.
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset Field (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	Reserved.
1:0	0h RW	**Power State Field (POWERSTATE):** This field is used both to determine the current power state and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state Others = Reserved Notes: If software attempts to write a value of 01b or 10b in to this field,the data is discarded and no state change occurs. When in the D3HOT states, interrupts are blocked.

13.1.14 PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: F0140009h

Bit Range	Default and Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision IDField (REVID):** Revision ID of capability structure

Bit Range	Default and Access	Field Name (ID): Description
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	0h RO	**Next Capability Field (NEXT_CAP):** Points to the next capability structure. This points to NULL.
7:0	9h RO	**Capability ID Field (CAPID)**

13.1.15 SW LTR update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Software location pointer in MMIO space as an offset specified by BAR

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 2101h

Bit Range	Default and Access	Field Name (ID): Description
31:4	210h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR BAR Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	1h RO	**SW LTR Valid Field (SW_LAT_VALID)**

13.1.16 Device IDLE Pointer (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register giving details on Device MMIO offset location BAR NUM and D0i3 Valid Strap

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 24C1h

Bit Range	Default and Access	Field Name (ID): Description
31:4	24Ch RO	**D0i3 Dword Offset Field (DWORD_OFFSET):** contains the location pointer to the SW LTR register in MMIO space as an offset from the specified BAR
3:1	0h RO	**BAR NUM Field (BAR_NUM):** Indicates that the D0i3 MMIO location is always at BAR0.
0	1h RO	**D0i3 Valid Field (VALID):** 0 = Not valid 1 = Valid

13.1.17 Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: F0800h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19	1h RW/P	**Sleep Enable Field (SLEEP_EN)**
18	1h RW/P	**D3 Hen Field (PGE):** If clear, the controller will never request a PG. If 1, then the function will power gate when idle and the DevIdle bit is set.
17	1h RW/P	**Device Idle En Field (I3_ENABLE):** If 1, then function will power gate when idle and the POWERSTATE bits in the function = 11 (D3).
16	1h RW/P	**PMC Request Enable Field (PMCRE):** If this bit is set to '1', the function will power gate when idle.
15:13	0h RO	Reserved.
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** This value is written by BIOS to communicate to the Driver.
9:0	0h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** This value is written by BIOS to communicate to the Driver.

13.1.18 General Purpose Read Write 1 (GEN_REGRW1)—Offset B0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW1):** General purpose read write PCI register.

13.1.19 General Purpose PCI Read Write 2 (GEN_REGRW2)—Offset B4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW2):** General purpose read write PCI register.

13.1.20 General Purpose PCI Read Write 3 (GEN_REGRW3)—Offset B8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW3):** General purpose read write PCI register.

13.1.21 General Purpose PCI Read Write 4 (GEN_REGRW4)—Offset BCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**General Purpose Read Write Field (GEN_REG_RW4):** General purpose read write PCI register.

13.1.22 General Purpose Input (GEN_INPUT_REG)—Offset C0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 21
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO	**General Purpose Input Field (GEN_REG_INPUT_RW):** General purpose input register.

13.2 I2C Memory Mapped Registers Summary

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Table 13-2. Summary of I2C Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	I2C Control (IC_CON)—Offset 0h	77h
4h	7h	I2C Target Address (IC_TAR)—Offset 4h	1055h
Ch	Fh	I2C High Speed Master Mode Code Address (IC_HS_MADDR)—Offset Ch	1h
10h	13h	Rx/Tx Data Buffer and Command (IC_DATA_CMD)—Offset 10h	0h
14h	17h	Standard Speed I2C Clock SCL High Count (IC_SS_SCL_HCNT)—Offset 14h	1F4h
18h	1Bh	Standard Speed I2C Clock SCL Low Count (IC_SS_SCL_LCNT)—Offset 18h	24Ch
1Ch	1Fh	Fast Speed I2C Clock SCL High Count (IC_FS_SCL_HCNT)—Offset 1Ch	4Bh
20h	23h	Fast Speed I2C Clock SCL Low Count (IC_FS_SCL_LCNT)—Offset 20h	A3h
24h	27h	High Speed I2C Clock SCL High Count (IC_HS_SCL_HCNT)—Offset 24h	8h
28h	2Bh	High Speed I2C Clock SCL Low Count (IC_HS_SCL_LCNT)—Offset 28h	14h
2Ch	2Fh	I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch	0h
30h	33h	Interrupt Mask Register (IC_INTR_MASK)—Offset 30h	8FFh
34h	37h	Raw Interrupt Status (IC_RAW_INTR_STAT)—Offset 34h	0h
38h	3Bh	Receive FIFO Threshold (IC_RX_TL)—Offset 38h	0h
3Ch	3Fh	Transmit FIFO Threshold (IC_TX_TL)—Offset 3Ch	0h
40h	43h	Clear Combined and Individual Interrupt (IC_CLR_INTR)—Offset 40h	0h
44h	47h	Clear RX_UNDER Interrupt (IC_CLR_RX_UNDER)—Offset 44h	0h
48h	4Bh	Clear RX_OVER Interrupt (IC_CLR_RX_OVER)—Offset 48h	0h
4Ch	4Fh	Clear TX_OVER Interrupt (IC_CLR_TX_OVER)—Offset 4Ch	0h
50h	53h	Clear RD_REQ Interrupt (IC_CLR_RD_REQ)—Offset 50h	0h
54h	57h	Clear TX_ABRT Interrupt (IC_CLR_TX_ABRT)—Offset 54h	0h
58h	5Bh	Clear RX_DONE Interrupt (IC_CLR_RX_DONE)—Offset 58h	0h
5Ch	5Fh	Clear ACTIVITY Interrupt (IC_CLR_ACTIVITY)—Offset 5Ch	0h
60h	63h	Clear STOP_DET Interrupt (IC_CLR_STOP_DET)—Offset 60h	0h
64h	67h	Clear START_DET Interrupt (IC_CLR_START_DET)—Offset 64h	0h
68h	6Bh	Clear GEN_CALL Interrupt (IC_CLR_GEN_CALL)—Offset 68h	0h
6Ch	6Fh	I2C Enable (IC_ENABLE)—Offset 6Ch	0h
70h	73h	I2C Status (IC_STATUS)—Offset 70h	6h
74h	77h	I2C Transmit FIFO Level (IC_TXFLR)—Offset 74h	0h
78h	7Bh	Receive FIFO Level (IC_RXFLR)—Offset 78h	0h
7Ch	7Fh	SDA Hold Time Length (IC_SDA_HOLD)—Offset 7Ch	1h
80h	83h	Transmit Abort Source (IC_TX_ABRT_SOURCE)—Offset 80h	0h
88h	8Bh	DMA Control (IC_DMA_CR)—Offset 88h	0h
8Ch	8Fh	DMA Transmit Data Level (IC_DMA_TDLR)—Offset 8Ch	0h
90h	93h	Receive Data Level (IC_DMA_RDLR)—Offset 90h	0h
98h	9Bh	ACK General Call (IC_ACK_GENERAL_CALL)—Offset 98h	1h
9Ch	9Fh	I2C Enable Status (IC_ENABLE_STATUS)—Offset 9Ch	0h
A0h	A3h	SS and FS Spike Suppression Limit (IC_FS_SPKLEN)—Offset A0h	7h

13.2.1 I2C Control (IC_CON)—Offset 0h

I2C Control Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 77h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**TX_EMPTY_CTRL (TX_EMPTY_CTRL):** This bit controls the generation of the TX_EMPTY interrupt, asdescribed in the IC_RAW_INTR_STAT register.
7	0h RO	Reserved.
6	1h RW	**IC_SLAVE_DISABLE (IC_SLAVE_DISABLE):** This bit controls whether I2C has its slave disabled. If this bit is set (slave is disabled), the function only works as a master and does not perform any action that requires a slave. 0:Reserved 1: slave is disabled
5	1h RW	**IC_RESTART_EN (IC_RESTART_EN):** Determines whether RESTART conditions may be sent when I2C is acting as a master. 0: Restart disable 1: Restart enable When the RESTART is disabled, the IP isincapable of performing the following functions: • Sending a START BYTE • Performing any high-speed mode operation • Performing direction changes in combined format mode • Performing a read operation with a 10-bit address By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple transfers. If the above operations are performed, it will result in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register.
4	1h RO	**IC_10BITADDR_MASTER_rd_only (IC_10BITADDR_MASTER_rd_only):** Identifies if I2C operates in 7 or 10 bit addressing. 0: 7-bit addressing 1: 10-bit addressing
3	0h RO	Reserved.
2:1	3h RW	**SPEED (SPEED):** These bits control at which speed the I2C operates. 01: staard mode (0 to 100 kbit/s) nd10: fast mode (<= 400 kbit/s) 11: High Speed Mode (<= 3.4 Mbit/s)
0	1h RW	**MASTER_MODE (MASTER_MODE):** This bit controls whether I2C master is enabled. 0 = Reserved 1 = Master Enabled Note: For Master Device Configuration Software must ensure that this bit is set to 1, and bit 6 must also be set to 1. Else this will result in configuration error.

13.2.2 I2C Target Address (IC_TAR)—Offset 4h

The register should only be updated when the I2C is not enabled (IC_ENABLE=0) or No Master mode operations are active (IC_STATUS[5] = 0 and IC_CON[0] = 1 and IC_STATUS[2] = 1).

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 1055h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	1h RW	**IC_10BITADDR_MASTER (IC_10BITADDR_MASTER):** This bit controls whether the I2C starts its transfers in 7-or 10-bit addressing mode when acting as a master. 0: 7 bit addressing 1: 10-bit addressing
11	0h RW	**SPECIAL (SPECIAL):** This bit indicates whether software performs a General Call or START BYTE command. 0: ignore bit 10 GC_OR_START and use IC_TAR normally. 1: perform special I2C command as specified in GC_OR_START bit.
10	0h RW	**GC_OR_START (GC_OR_START):** If bit 11 (SPECIAL) is set to 1, then this bit indicates whether a General Call or START byte command is to be performed by the I2C. 0: General Call Address – after issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TX_ABRT) of the IC_RAW_INTR_STAT register. The I2C remains in General Call mode until the SPECIAL bit value (bit 11) is cleared. 1: START BYTE
9:0	55h RW	**IC_TAR (IC_TAR):** This is the target address for any master transaction. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the CPU needs to write only once into these bits.

13.2.3 I2C High Speed Master Mode Code Address (IC_HS_MADDR)—Offset Ch

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2:0	1h RW	**IC_HS_MAR (IC_HS_MAR):** This bit field holds the value of the I2C HS mode master code. HS-mode master codes are reserved 8-bit codes (00001xxx) that are not used for slave addressing or other purposes. Each master has its unique master code; up to eight highspeed mode masters can be present on the same I2C bus system. Valid values are from 0 to 7. This register goes away and becomes read-only returning 0s if the IC_MAX_SPEED_MODE configuration parameter is set to either Standard (1) or Fast (2).

13.2.4 Rx/Tx Data Buffer and Command (IC_DATA_CMD)—Offset 10h

I2C Data Command Register

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10	0h WO	**RESTART (RESTART):** This bit controls whether a RESTART is issued before the byte is sent or received. 1: a RESTART is issued before the data is sent/received (according to the value of CMD), regardless of whether or not the transfer direction is changing from the previous command. 0: a RESTART is issued only if the transfer direction is changing from the previous command.

Bit Range	Default & Access	Field Name (ID): Description
9	0h WO	**STOP (STOP):** This bit controls whether a STOP is issued after the byte is sent or received. 1: STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus. 0: STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO.
8	0h WO	**CMD (CMD):** This bit controls whether a read or a write is performed. 1 = Read. 0 = Write When a command is entered in the TX FIFO, this bit distinguishes the write and read commands. In slave-receiver mode, this bit is a don't care because writes to this register are not required. In slave-transmitter mode, a 0 indicates that the data in IC_DATA_CMD is to be transmitted. When programming this bit, note the following: attempting to perform a read operation after a General Call command has been sent results in a TX_ABRT interrupt (bit 6 of the IC_RAW_INTR_STAT register), unless bit 11(SPECIAL) in the IC_TAR register has been cleared. If a “1” is written to this bit after receiving a RD_REQ interrupt, then a TX_ABRTinterrupt occurs.
7:0	0h RW	**DAT (DAT):** This register contains the data to be transmitted or received on the I2C bus. If you are writing to this register and want to perform a read, bits 7:0 (DAT) are ignored by the I2C. However, when you read this register, these bits return the value of data received on the I2C interface.

13.2.5 Standard Speed I2C Clock SCL High Count (IC_SS_SCL_HCNT)—Offset 14h

This register sets the SCL clock high-period count for standard speed. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The register is only used in Master mode.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1F4h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	1F4h RW	**IC_SS_SCL_HCNT (IC_SS_SCL_HCNT):** This register sets the SCL clock high-period count for standard speed. The value of the registers should be within the range {6, 65525}.

13.2.6 Standard Speed I2C Clock SCL Low Count (IC_SS_SCL_LCNT)—Offset 18h

This register sets the SCL clock low-period countfor standard speed.. This register can be written only when the I2C interface is disabled which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 24Ch

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	24Ch RW	**IC_SS_SCL_LCNT (IC_SS_SCL_LCNT):** Standard Speed I2C Clock SCL Low Count Register. The register value should always be >= 8

13.2.7 Fast Speed I2C Clock SCL High Count (IC_FS_SCL_HCNT)—Offset 1Ch

Fast Speed I2C Clock SCL High Count Register. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 4Bh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	4Bh RW	**IC_FS_SCL_HCNT (IC_FS_SCL_HCNT):** This register sets the SCL clock high-period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL.. The minimum value of this field is 6.

13.2.8 Fast Speed I2C Clock SCL Low Count (IC_FS_SCL_LCNT)—Offset 20h

Fast Speed I2C Clock SCL Low Count Register. This register must be set before any I2C bus transaction can take place to ensure proper I/O timing.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: A3h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	A3h RW	**IC_FS_SCL_LCNT (IC_FS_SCL_LCNT):** This register sets the SCL clock low period count for fast speed. It is used in high-speed mode to send the Master Code and START BYTE or General CALL. The register should be programmed with a minimum value of 8.

13.2.9 High Speed I2C Clock SCL High Count (IC_HS_SCL_HCNT)—Offset 24h

High Speed I2C Clock SCL High Count Register. This register must be set before any I2C bus transaction can take place to ensure proper I/O timing.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	8h RW	**IC_HS_SCL_HCNT (IC_HS_SCL_HCNT):** This register sets the SCL clock high period count for high speed.

13.2.10 High Speed I2C Clock SCL Low Count (IC_HS_SCL_LCNT)—Offset 28h

High Speed I2C Clock SCL Low Count Register. This register must be set before any I2C bus transaction can take place to ensure proper I/O timing.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 14h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	14h RW	**IC_HS_SCL_LCNT (IC_HS_SCL_LCNT):** This register sets the SCL clock low period count for high speed.

13.2.11 I2C Interrupt Status Register (IC_INTR_STAT)—Offset 2Ch

I2C Interrupt Status Register. Each bit in this register has a corresponding mask bit in the IC_INTR_MASK register. These bits are cleared by reading the matching interrupt clear register

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h RO	**R_MASTER_ON_HOLD (R_MASTER_ON_HOLD):** Indicates whether a master is holding the bus and the TX FIFO is empty. Enabled only when I2C_DYNAMIC_TAR_UPDATE = 1 and IC_EMPTYFIFO_HOLD_MASTER_EN = 1
12	0h RO	Reserved.
11	0h RO	**R_GEN_CALL (R_GEN_CALL):** Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling the controller or when the processor reads bit 0 of the IC_CLR_GEN_CALL register
10	0h RO	**R_START_DET (R_START_DET):** Indicates whether a START or RESTART condition has occurred on the I2C interface.
9	0h RO	**R_STOP_DET (R_STOP_DET):** Indicates whether a STOP condition has occurred on the I2C interface.
8	0h RO	**R_ACTIVITY (R_ACTIVITY):** This bit captures the controller activity and stays set until it is cleared. There are four ways to clear it:1. Disabling the controller,2. Reading the IC_CLR_ACTIVITY register,3. Reading the IC_CLR_INTR register,4. System reset Note: Once this bit is set, it stays set unless one of the four methods is used to clear it. Even if the controller is idle, this bit remains set until cleared, indicating that there was activity on the bus.
7	0h RO	Reserved.
6	0h RO	**R_TX_ABRT (R_TX_ABRT):** This bit indicates if the controller, as an I2C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. When this bit is set to 1, the IC_TX_ABRT_SOURCE register indicates the reason why the transmit abort takes places. NOTE: The controller flushes/resets/empties the TX FIFO whenever this bit is set. The TX FIFO remains in this flushed state until the register IC_CLR_TX_ABRT is read. Once this read is performed, the TX FIFO is then ready to accept more data bytes.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	Reserved.
4	0h RO	**R_TX_EMPTY (R_TX_EMPTY):** The behavior of the TX_EMPTY interrupt status differs based on the TX_EMPTY_CTRL selection in the IC_CON register. When TX_EMPTY_CTRL = 0: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register. When TX_EMPTY_CTRL = 1: This bit is set to 1 when the transmit buffer is at or below the threshold value set in the IC_TX_TL register and the transmission of the address/data from the internal shift register for the most recently popped command is completed. It is automatically cleared by hardware when the buffer level goes above the threshold. When IC_ENABLE[0] is set to 0, the TX FIFO is flushed and held in reset. There the TX FIFO looks like it has no data within it, so this bit is set to 1, provided there is activity in the master or slave state machines. When there is no longer any activity, then with ic_en=0, this bit is set to 0.
3	0h RO	**R_TX_OVER (R_TX_OVER):** Set during transmit if the transmit buffer is filled to IC_TX_BUFFER_DEPTH and the processor attempts to issue another I2C command by writing to the IC_DATA_CMD register. When the module is disabled, this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared.
2	0h RO	**R_RX_FULL (R_RX_FULL):** Set when the receive buffer reaches or goes above the RX_TL threshold in the IC_RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold. If the module is disabled (IC_ENABLE[0]=0), the RX FIFO is flushed and held in reset; therefore the RX FIFO is not full. So this bit is cleared once the IC_ENABLE bit 0 is programmed with a 0, regardless of the activity that continues.
1	0h RO	**R_RX_OVER (R_RX_OVER):** Set if the receive buffer is completely filled to IC_RX_BUFFER_DEPTH and an additional byte is received from an external I2C device. The controller acknowledges this, but any data bytes received after the FIFO is full are lost. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master goes into idle, and when ic_en goes to 0, this interrupt is cleared.
0	0h RO	**R_RX_UNDER (R_RX_UNDER):** Set if the processor attempts to read the receive buffer when it is empty by reading from the IC_DATA_CMD register. If the module is disabled (IC_ENABLE[0]=0), this bit keeps its level until the master or slave state machines go into idle, and when ic_en goes to 0, this interrupt is cleared

13.2.12 Interrupt Mask Register (IC_INTR_MASK)—Offset 30h

These bits mask their corresponding interrupt status bits in the IC_INTR_STAT register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8FFh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h RW	**M_MASTER_ON_HOLD (M_MASTER_ON_HOLD):** This bit masks the R_MST_ON_HOLD interrupt bit in the IC_INTR_STAT register.
12	0h RO	Reserved.
11	1h RW	**M_GEN_CALL (M_GEN_CALL):** M_GEN_CALL_field

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**M_START_DET (M_START_DET):** M_START_DET_field
9	0h RW	**M_STOP_DET (M_STOP_DET):** M_STOP_DET_field
8	0h RW	**M_ACTIVITY (M_ACTIVITY):** M_ACTIVITY_field
7	1h RW	**M_RX_DONE (M_RX_DONE):** M_RX_DONE_field
6	1h RW	**M_TX_ABRT (M_TX_ABRT):** M_TX_ABRT_field
5	1h RW	**M_RD_REQ (M_RD_REQ):** M_RD_REQ_field
4	1h RW	**M_TX_EMPTY (M_TX_EMPTY):** M_TX_EMPTY_field
3	1h RW	**M_TX_OVER (M_TX_OVER):** M_TX_OVER_field
2	1h RW	**M_RX_FULL (M_RX_FULL):** M_RX_FULL_field
1	1h RW	**M_RX_OVER (M_RX_OVER):** M_RX_OVER_field
0	1h RW	**M_RX_UNDER (M_RX_UNDER):** M_RX_UNDER_field

13.2.13 Raw Interrupt Status (IC_RAW_INTR_STAT)—Offset 34h

Unlike the IC_INTR_STAT register, these bits are not masked so they always show the true status of the controller.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h RO	**MASTER_ON_HOLD (MASTER_ON_HOLD):** Same as in reg_IC_INTR_STAT
12	0h RO	Reserved.
11	0h RO	**GEN_CALL (GEN_CALL):** Same as in reg_IC_INTR_STAT
10	0h RO	**START_DET (START_DET):** Same as in reg_IC_INTR_STAT

Bit Range	Default & Access	Field Name (ID): Description
9	0h RO	**STOP_DET (STOP_DET):** Same as in reg_IC_INTR_STAT
8	0h RO	**RAW_INTR_ACTIVITY (RAW_INTR_ACTIVITY):** Same as in reg_IC_INTR_STAT
7	0h RO	**RX_DONE (RX_DONE):** Same as in reg_IC_INTR_STAT
6	0h RO	**TX_ABRT (TX_ABRT):** Same as in reg_IC_INTR_STAT
5	0h RO	**RD_REQ (RD_REQ):** Same as in reg_IC_INTR_STAT
4	0h RO	**TX_EMPTY (TX_EMPTY):** Same as in reg_IC_INTR_STAT
3	0h RO	**TX_OVER (TX_OVER):** Same as in reg_IC_INTR_STAT
2	0h RO	**RX_FULL (RX_FULL):** Same as in reg_IC_INTR_STAT
1	0h RO	**RX_OVER (RX_OVER):** Same as in reg_IC_INTR_STAT
0	0h RO	**RX_UNDER (RX_UNDER):** Same as in reg_IC_INTR_STAT

13.2.14 Receive FIFO Threshold (IC_RX_TL)—Offset 38h

I2C Receive FIFO Threshold Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**RX_TL (RX_TL):** Receive FIFO Threshold Level. Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in IC_RAW_INTR_STAT register). The valid range is 0-0x3F. (Values > 0x3F are set to depth of the buffer). A value of 0 sets the threshold for 1 entry, and a value of 63 sets the threshold for 64 entries.

13.2.15 Transmit FIFO Threshold (IC_TX_TL)—Offset 3Ch

I2C Transmit FIFO Threshold Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**TX_TL (TX_TL):** Transmit FIFO Threshold Level Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in IC_RAW_INTR_STAT register). The valid range is 0-255, with the additional restriction that it may not be set to value larger than the depth of the buffer. If an attempt is made to do that, the actual value set will be the maximum depth of the buffer. A value of 0 sets the threshold for 0 entries, and a value of 255 sets the threshold for 255 entries.

13.2.16 Clear Combined and Individual Interrupt (IC_CLR_INTR)—Offset 40h

Clear Combined and Individual Interrupt Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_INTR (CLR_INTR):** Read this register to clear the combined interrupt, all individual interrupts, and the IC_TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

13.2.17 Clear RX_UNDER Interrupt (IC_CLR_RX_UNDER)—Offset 44h

Clear RX_UNDER Interrupt Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_RX_UNDER (CLR_RX_UNDER):** Read this register to clear the RX_UNDER interrupt (bit 0) of the IC_RAW_INTR_STAT register.

13.2.18 Clear RX_OVER Interrupt (IC_CLR_RX_OVER)—Offset 48h

Clear RX_OVER Interrupt Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_RX_OVER (CLR_RX_OVER):** Read this register to clear the RX_OVER interrupt (bit 1) of the IC_RAW_INTR_STAT register.

13.2.19 Clear TX_OVER Interrupt (IC_CLR_TX_OVER)—Offset 4Ch

Clear TX_OVER Interrupt Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_TX_OVER (CLR_TX_OVER):** Read this register to clear the TX_OVER interrupt (bit 3) of the IC_RAW_INTR_STAT register.

13.2.20 Clear RD_REQ Interrupt (IC_CLR_RD_REQ)—Offset 50h

Clear RD_REQ Interrupt Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_RD_REQ (CLR_RD_REQ):** Read this register to clear the RD_REQ interrupt (bit 5) of the IC_RAW_INTR_STAT register

13.2.21 Clear TX_ABRT Interrupt (IC_CLR_TX_ABRT)—Offset 54h

Clear TX_ABRT Interrupt Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_TX_ABRT (CLR_TX_ABRT):** Read this register to clear the TX_ABRT interrupt (bit 6) of the IC_RAW_INTR_STAT register, and the IC_TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to Bit 9 of the IC_TX_ABRT_SOURCE register for an exception to clearing IC_TX_ABRT_SOURCE.

13.2.22 Clear RX_DONE Interrupt (IC_CLR_RX_DONE)—Offset 58h

Clear RX_DONE Interrupt Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_RX_DONE (CLR_RX_DONE):** Read this register to clear the RX_DONE interrupt (bit 7) of the IC_RAW_INTR_STAT register.

13.2.23 Clear ACTIVITY Interrupt (IC_CLR_ACTIVITY)—Offset 5Ch

Clear ACTIVITY Interrupt Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_ACTIVITY (CLR_ACTIVITY):** Reading this register clears the ACTIVITY interrupt if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register to get status of the ACTIVITY interrupt (bit 8) of the IC_RAW_INTR_STAT register

13.2.24 Clear STOP_DET Interrupt (IC_CLR_STOP_DET)—Offset 60h

Clear STOP_DET Interrupt Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_STOP_DET (CLR_STOP_DET):** Read this register to clear the STOP_DET interrupt (bit 9) of the IC_RAW_INTR_STAT register

13.2.25 Clear START_DET Interrupt (IC_CLR_START_DET)—Offset 64h

Clear START_DET Interrupt Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_START_DET (CLR_START_DET):** Read this register to clear the START_DET interrupt (bit 10) of the IC_RAW_INTR_STAT register.

13.2.26 Clear GEN_CALL Interrupt (IC_CLR_GEN_CALL)—Offset 68h

Clear GEN_CALL Interrupt Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**CLR_GEN_CALL (CLR_GEN_CALL):** Read this register to clear the GEN_CALL interrupt (bit 11) of IC_RAW_INTR_STAT register

13.2.27 I2C Enable (IC_ENABLE)—Offset 6Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**ABORT (ABORT):** Sofware can abort I2C transfer by setting this bit. Hw will clear this ABORT bit once the STOP has been detected
0	0h RW	**ENABLE (ENABLE):** Controls whether the controller is enabled. 0: Disables I2C controller (TX and RX FIFOs are held in an erased state) 1: Enables I2C controller. Software can disable the controller while it is active. However, it is important that care be taken to ensure that the controller is disabled properly. When the controller is disabled, the following occurs: -The TX FIFO and RX FIFO get flushed. -Status bits in the IC_INTR_STAT register are still active until the controller goes into IDLE state. If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. If the module is receiving, the controller stops the current transfer at the end of the current byte and does not acknowledge the transfer.

13.2.28 I2C Status (IC_STATUS)—Offset 70h

I2C Status Register. This is a read-only register used to indicate the current transfer status and FIFO status. The status register may be read at any time. None of the bits in this register request an interrupt. When the I2C is disabled by writing 0 in bit 0 of the IC_ENABLE register:- Bits 1 and 2 are set to 1- Bits 3 and 4 are set to 0. When the master or slave state machines goes to idle and IC_ENABLE=0:- Bits 5 and 6 are set to 0

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 6h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	0h RO	**MST_ACTIVITY (MST_ACTIVITY):** When the Master state machine is not in the IDLE state, this bit is set. 0: Master is in IDLE state 1: Master is not in IDLE
4	0h RO	**RFF (RFF):** When the receive FIFO is completely full, this bit is set. When the receive FIFO contains one or more empty location, this bit is cleared. 0: Receive FIFO is not full 1: Receive FIFO is full
3	0h RO	**RFNE (RFNE):** This bit is set when the receive FIFO contains one or more entries; it is cleared when the receive FIFO is empty. 0: Receive FIFO is empty 1: Receive FIFO is not empty

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO	**TFE (TFE):** When the transmit FIFO is completely empty, this bit is set. When it contains one or more valid entries, this bit is cleared. This bit field does not request an interrupt. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty
1	1h RO	**TFNF (TFNF):** Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full. 0: Transmit FIFO is full 1: Transmit FIFO is not full
0	0h RO	**IC_STATUS_ACTIVITY (IC_STATUS_ACTIVITY):** I2C Activity Status

13.2.29 I2C Transmit FIFO Level (IC_TXFLR)—Offset 74h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	Reserved.
6:0	0h RO	**TXFLR (TXFLR):** Transmit FIFO Level. Contains the number of valid data entries in the transmit FIFO

13.2.30 Receive FIFO Level (IC_RXFLR)—Offset 78h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	Reserved.
6:0	0h RO	**RXFLR (RXFLR):** Receive FIFO Level. Contains the number of valid data entries in the receive FIFO.

13.2.31 SDA Hold Time Length (IC_SDA_HOLD)—Offset 7Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
15:0	1h RW	**IC_SDA_TX_HOLD (IC_SDA_TX_HOLD):** Sets the required SDA hold time in units of ic_clk period, when the I2C Host Controller acts as a transmitter.

13.2.32 Transmit Abort Source (IC_TX_ABRT_SOURCE)—Offset 80h

This register has 32 bits that indicate the source of the TX_ABRT bit. Except for Bit 9, this register is cleared whenever the IC_CLR_TX_ABRT register or the IC_CLR_INTR register is read. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; RESTART must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]).
Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, Bit 9 clears for one cycle and is then re-asserted.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**TX_FLUSH_CNT (TX_FLUSH_CNT):** This field preserves the TXFLR value prior to the last TX_ABRT event. It is cleared whenever I2C is disabled. Mode Applicable: Master-Transmitter
22:17	0h RO	Reserved.
16	0h RO	**ABRT_USER_ABRT (ABRT_USER_ABRT):** This is a master-mode-only bit. Master has detected the user initiated transfer abort (IC_ENABLE[1]) Mode Applicable: Master-Transmitter
15	0h RO	**ABRT_SLVRD_INTX (ABRT_SLVRD_INTX):** 1: When the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of IC_DATA_CMD register. Mode Applicable: Slave Transmitter 14 RO 1'h0
14:13	0h RO	Reserved.
12	0h RO	**ARB_LOST (ARB_LOST):** 1: Master has lost arbitration, or if IC_TX_ABRT_SOURCE[14] is also set, then the slave transmitter has lost arbitration. Mode Applicable: Master or Slave Transmitter

Bit Range	Default & Access	Field Name (ID): Description
11	0h RO	**ABRT_MASTER_DIS (ABRT_MASTER_DIS):** 1: User tries to initiate a Master operation with the Master mode disabled. Mode Applicable: Master Transmitter or Receiver
10	0h RO	**ABRT_10B_RD_NORSTRT (ABRT_10B_RD_NORSTRT):** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the master sends a read command in 10-bit addressing mode. Mode Applicable: Master Receiver
9	0h RO	**ABRT_SBYTE_NORSTRT (ABRT_SBYTE_NORSTRT):** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to send a START Byte. To clear Bit 9, the source of the ABRT_SBYTE_NORSTRT must be fixed first; restart must be enabled (IC_CON[5]=1), the SPECIAL bit must be cleared (IC_TAR[11]), or the GC_OR_START bit must be cleared (IC_TAR[10]). Once the source of the ABRT_SBYTE_NORSTRT is fixed, then this bit can be cleared in the same manner as other bits in this register. If the source of the ABRT_SBYTE_NORSTRT is not fixed before attempting to clear this bit, bit 9 clears for one cycle and then gets re-asserted.
8	0h RO	**ABRT_HS_NORSTRT (ABRT_HS_NORSTRT):** 1: The restart is disabled (IC_RESTART_EN bit (IC_CON[5]) = 0) and the user is trying to use the master to transfer data in High Speed mode. Mode Applicable: Master Transmitter or Receiver
7	0h RO	**ABRT_SBYTE_ACKDET (ABRT_SBYTE_ACKDET):** 1: Master has sent a START Byte and the START Byte was acknowledged (wrong behavior). Mode Applicable: Master
6	0h RO	**ABRT_HS_ACKDET (ABRT_HS_ACKDET):** 1: Master is in High Speed mode and the High Speed Master code was acknowledged (wrong behavior). Mode Applicable: Master
5	0h RO	**ABRT_GCALL_READ (ABRT_GCALL_READ):** 1: Controller in master mode sent a General Call but the user programmed the byte following the General Call to be a read from the bus (IC_DATA_CMD[9] is set to 1).
4	0h RO	**ABRT_GCALL_NOACK (ABRT_GCALL_NOACK):** 1: DW_apb_i2c in master mode sent a General Call and no slave on the bus acknowledged the General Call. Mode Applicable: Master Transmitter
3	0h RO	**ABRT_TXDATA_NOACK (ABRT_TXDATA_NOACK):** 1: This is a master-mode only bit. Master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s). Mode Applicable: Master Transmitter
2	0h RO	**ABRT_10ADDR2_NOACK (ABRT_10ADDR2_NOACK):** 1: Master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave. Mode Applicable: Master Transmitter or Receiver
1	0h RO	**ABRT_10ADDR1_NOACK (ABRT_10ADDR1_NOACK):** 1: Master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave. Mode Applicable: Master Transmitter or Receiver
0	0h RO	**ABRT_7B_ADDR_NOACK (ABRT_7B_ADDR_NOACK):** 1: Master is in 7-bit addressing mode and the address sent was not acknowledged by any slave. Mode Applicable: Master Transmitter or Receiver

13.2.33 DMA Control (IC_DMA_CR)—Offset 88h

This register is only valid when the controller is configured with a set of DMA Controller interface signals (IC_HAS_DMA = 1).
When the controller is not configured for DMA operation, this register does not exist and writing to the register's address has no effect and reading from this register address will return zero.
The register is used to enable the DMA Controller interface operation. There is a separate bit for transmit and receive. This can be programmed regardless of the state of IC_ENABLE.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**TDMAE (TDMAE):** Transmit DMA Enable. This bit enables/disables the transmit FIFO DMA channel. 0 = Transmit DMA disabled 1 = Transmit DMA enabled
0	0h RW	**RDMAE (RDMAE):** Receive DMA Enable. This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled 1 = Receive DMA enabled

13.2.34 DMA Transmit Data Level (IC_DMA_TDLR)—Offset 8Ch

DMA Transmit Data Level Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5:0	0h RW	**DMATDL (DMATDL):** Transmit Data Level. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and TDMAE = 1.

13.2.35 Receive Data Level (IC_DMA_RDLR)—Offset 90h

I2C Receive Data Level Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5:0	0h RW	**DMARDL (DMARDL):** Receive Data Level. This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value + 1, and RDMAE =1. For instance, when DMARDL is 0, then dma_rx_req is asserted when 1 or more data entries are present in the receive FIFO.

13.2.36 ACK General Call (IC_ACK_GENERAL_CALL)—Offset 98h

I2C ACK General Call Register. The register controls whether DW_apb_i2c responds with a ACK or NACK when it receives an I2C General Call address

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**ACK_GEN_CALL (ACK_GEN_CALL):** When set to 1, the controller responds with a ACK when it receives a General Call. When set to 0, the controller does not generate General Call interrupts.

13.2.37 I2C Enable Status (IC_ENABLE_STATUS)—Offset 9Ch

The register is used to report the hardware status when the IC_ENABLE register is set from 1 to 0; that is, when the controller is disabled.
If IC_ENABLE has been set to 1, bits 2:1 are forced to 0, and bit 0 is forced to 1.
If IC_ENABLE has been set to 0, bits 2:1 is only be valid as soon as bit 0 is read as '0'.
When IC_ENABLE has been written with '0,' a delay occurs for bit 0 to be read as '0' because disabling the controller depends on I2C bus activities.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**IC_EN (IC_EN):** When read as 1, the controller is deemed to be in an enabled state.When read as 0, the controller is deemed completely inactive.

13.2.38 SS and FS Spike Suppression Limit (IC_FS_SPKLEN)—Offset A0h

This register is used to store the duration, measured in ic_clk cycles, of the longest spike that is filtered out by the spike suppression logic when the component is operating in SS or FS modes.
The relevant I2Crequirement is tSP as detailed in the I2C Bus Specification. This register must be programmed with a minimum value of 1.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 7h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	7h RW	**IC_FS_SPKLEN (IC_FS_SPKLEN):** This register must be set before any I2C bus transaction can take place to ensure stable operation. This register sets the duration, measured in ic_clk cycles, of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic; for more information, refer to Spike Suppression. This register can be written only when the I2C interface is disabled, which corresponds to the IC_ENABLE register being set to 0. Writes at other times have no effect. The minimum valid value is 1; hardware prevents values less than this being written, and if attempted results in 2 being set.

13.3 I2C Additional Registers Summary

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Table 13-3. Summary of I2C Additional Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
204h	207h	Soft Reset (RESETS)—Offset 204h	0h
210h	213h	Active LTR (ACTIVELTR_VALUE)—Offset 210h	800h
214h	217h	Idle LTR (IDLELTR_VALUE)—Offset 214h	800h
218h	21Bh	TX ACK Count (TX_ACK_COUNT)—Offset 218h	0h
21Ch	21Fh	RX ACK Count (RX_BYTE_COUNT)—Offset 21Ch	0h
220h	223h	Interrupt Status for Tx Complete (TX_COMPLETE_INTR_STAT)—Offset 220h	0h

Table 13-3. Summary of I2C Additional Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
224h	227h	Tx Complete Interrupt Clear (TX_COMPLETE_INTR_CLR)—Offset 224h	0h
228h	22Bh	SW Scratch Register 0 (SW_SCRATCH_0)—Offset 228h	0h
22Ch	22Fh	SW Scratch Register 1 (SW_SCRATCH_1)—Offset 22Ch	0h
230h	233h	SW Scratch Register 2 (SW_SCRATCH_2)—Offset 230h	0h
234h	237h	SW Scratch Register 3 (SW_SCRATCH_3)—Offset 234h	0h
238h	23Bh	Clock Gate (CLOCK_GATE)—Offset 238h	0h
240h	243h	Remap Address Low (REMAP_ADDR_LO)—Offset 240h	0h
244h	247h	Remap Address High (REMAP_ADDR_HI)—Offset 244h	0h
24Ch	24Fh	Device Idle Control (DEVIDLE_CONTROL)—Offset 24Ch	8h
2FCh	2FFh	Capabilities (CAPABLITIES)—Offset 2FCh	0h

13.3.1 Soft Reset (RESETS)—Offset 204h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW	**reset_dma (reset_dma):** DMA Software Reset Control. 0 = IP is in reset (Reset Asserted) 1 = IP is NOT at reset (Reset Released)
1:0	0h RW	**reset_ip (reset_ip):** Used to reset the I2C Host Controller by SW control. All I2C Configuration State and Operational State will be forced to the Default state. There is no timing requirement (SW can assert and de-assert in back to back transactions). This reset does NOT impact the settings by BIOS, the PCI configuration header information, DMA channel configuration and interrupt assignment/mapping/etc. Driver should re-initialize registers related to Driver context following an I2C host controller reset. 00 = I2C Host Controller is in reset (Reset Asserted) 01 = Reserved 10 = Reserved 11 = I2C Host Controller is NOT at reset (Reset Released)

13.3.2 Active LTR (ACTIVELTR_VALUE)—Offset 210h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 800h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**Snoop Requirement (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10 -bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time
14:13	0h RO	Reserved.
12:10	2h RW	**i2c_sw_ltr_snoop_scale_reg_12_10 (i2c_sw_ltr_snoop_scale_reg_12_10):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**Snoop Value (snoop_value):** 10-bit latency value

13.3.3 Idle LTR (IDLELTR_VALUE)—Offset 214h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 800h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW	**snoop_requirement (snoop_requirment):** If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (i.e. it can wait for service indefinitely). If the 10 -bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time
14:13	0h RO	Reserved.
12:10	2h RW	**snoop_latency_scale (snoop_latency_scale):** Support for codes 010 (1us) or 011 (32us) for Snoop Latency Scale(1us -> 32ms total span) only. Writes to this CSR which dont match those values will be dropped completely, next read will return previous value.
9:0	0h RW	**snoop_value (snoop_value):** 10-bit latency value.

13.3.4 TX ACK Count (TX_ACK_COUNT)—Offset 218h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**TX Count Overflow (tx_ack_count_overflow):** Count overflow indication. 0= Count valid 1= Count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**TX Ack Count (tx_ack_count):** Count ACK seen on Write commands, 24-bit up-counter which counts the number of TX ACKs on the I2C bus. The Counter is forced to be cleared by software Read.

13.3.5 RX ACK Count (RX_BYTE_COUNT)—Offset 21Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**RX ACK Count Overflow (rx_ack_count_overflow):** Rx ACK count overflow 0= count valid 1= count overflow/invalid
30:24	0h RO	Reserved.
23:0	0h RO	**RX ACK Count (rx_ack_count):** Counts ACK seen on Read commands, 24-bit readable (MMIO) up-counter which counts the number of RX bytes received on the I2C bus. The Counter is forced to be cleared by software Read

13.3.6 Interrupt Status for Tx Complete (TX_COMPLETE_INTR_STAT)—Offset 220h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**TX Completion Interrupt Mask (tx_intr_stat_mask):** 0 = Unmask 1= Mask
0	0h RO	**TX Completion Interrupt (tx_intr_stat):** 0 = Low 1 = High

13.3.7 Tx Complete Interrupt Clear (TX_COMPLETE_INTR_CLR)—Offset 224h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RO	**TX Completion Interrupt Clear (i2c_tx_complete_intr_clr_0):** Read this register to clear the TX_COMPLETE_INTR_STAT register

13.3.8 SW Scratch Register 0 (SW_SCRATCH_0)—Offset 228h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SW Scratch 0 (SW_Scratch_0):** Scratch Pad Register for SW to generated Local CMD or DATA for DMA.

13.3.9 SW Scratch Register 1 (SW_SCRATCH_1)—Offset 22Ch

Same definition as SW_SCRATCH_0.

13.3.10 SW Scratch Register 2 (SW_SCRATCH_2)—Offset 230h

Same definition as SW_SCRATCH_0.

13.3.11 SW Scratch Register 3 (SW_SCRATCH_3)—Offset 234h

Same definition as SW_SCRATCH_0.

13.3.12 Clock Gate (CLOCK_GATE)—Offset 238h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:2	0h RW	**DMA Clock Control (sw_dma_clk_ctl):** 00 = Dyanamic Clock Gate Enable 01 = Reserved 10 = Force iDMA Clock off 11 = Force iDMA Clock on
1:0	0h RW	**Controller Clock Control (sw_ip_clk_ctl):** 00 = Dynamic Clock Gate Enable 01 = Reserved 10 = Force Clocks off 11 = Force Clocks on

13.3.13 Remap Address Low (REMAP_ADDR_LO)—Offset 240h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Remap Address Low (i2c_remap_addr_lo_reg):** Must be programmed to the same value as low 32 bits (0x 010 BAR Low) Note: Must be programed for all I2C controllers configurations (DMA or PIO only)

13.3.14 Remap Address High (REMAP_ADDR_HI)—Offset 244h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Remap Address High (i2c_remap_addr_hi):** Must be programmed to the same value as low 32 bits (0x 014 BAR High)

13.3.15 Device Idle Control (DEVIDLE_CONTROL)—Offset 24Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**Interrupt Request Capable (intr_req_capable):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0.
3	1h RW/1C	**Restore Required (restore_required):** When set (by HW), SW must restore state to the controller. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up. Note: If SW is setting bit 3 together with any other bit of this register, only bit 3 is written; SW is required to do 2 writes in this case : bit 3 first and all other bits second.
2	0h RW	**Device Idle (devidle):** SW sets this bit to 1 to move the function into the DevIdle state. Writing this bit to 0 will return the function to the fully active D0 state.
1	0h RO	Reserved.
0	0h RO	**Command In Progress (cmd_in_progress):** HW sets this bit on a 1->0 or 0->1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is unsupported for SW to write to any bit in this register. HW clears this bit upon completing the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

13.3.16 Capabilities (CAPABLITIES)—Offset 2FCh

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9	0h RO	**Serial Clock Frequency (serial_clk_freq):** 1 indicates 133 MHz clock.
8	0h RO	**DMA Present (iDMA_present):** 0= DMA present 1= DMA not present
7:4	0h RO	**Instance Type (instance_type):** 0000 = I2C 0001 = UART 0010 = SPI 0011 – 1111 = Reserved
3:0	0h RO	**instance_number (instance_number):** 0h: I2C0 1h: I2C1 2h: I2C2 ... 5h: I2C5

13.4 I2C DMA Controller Registers Summary

The registers in this section are memory-mapped registers based on the BAR defined in PCH Configuration space.

Table 13-4. Summary of I2C DMA Controller Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
800h	803h	DMA Transfer Source Address Low (SAR_LO0)—Offset 800h	0h
804h	807h	DMA Transfer Source Address High (SAR_HI0)—Offset 804h	0h
808h	80Bh	DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h	0h
80Ch	80Fh	DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch	0h
810h	813h	Linked List Pointer Low (LLP_LO0)—Offset 810h	0h
814h	817h	Linked List Pointer High (LLP_HI0)—Offset 814h	0h
818h	81Bh	Control Register Low (CTL_LO0)—Offset 818h	0h
81Ch	81Fh	Control Register High (CTL_HI0)—Offset 81Ch	0h
820h	823h	Source Status (SSTAT0)—Offset 820h	0h
828h	82Bh	Destination Status (DSTAT0)—Offset 828h	0h
830h	833h	Source Status Address Low (SSTATAR_LO0)—Offset 830h	0h
834h	837h	Source Status Address High (SSTATAR_HI0)—Offset 834h	0h
838h	83Bh	Destination Status Address Low (DSTATAR_LO0)—Offset 838h	0h
83Ch	83Fh	Destination Status Address High (DSTATAR_HI0)—Offset 83Ch	0h
840h	843h	DMA Transfer Configuration Low (CFG_LO0)—Offset 840h	203h
844h	847h	DMA Transfer Configuration High (CFG_HI0)—Offset 844h	0h
848h	84Bh	Source Gather (SGR0)—Offset 848h	0h
850h	853h	Destination Scatter (DSR0)—Offset 850h	0h
AC0h	AC3h	Raw Interrupt Status (RawTfr)—Offset AC0h	0h
AC8h	ACBh	Raw Status for Block Interrupts (RawBlock)—Offset AC8h	0h
AD0h	AD3h	Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h	0h
AD8h	ADBh	Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h	0h
AE0h	AE3h	Raw Status for Error Interrupts (RawErr)—Offset AE0h	0h
AE8h	AEBh	Status for Transfer Interrupts (StatusTfr)—Offset AE8h	0h
AF0h	AF3h	Status for Block Interrupts (StatusBlock)—Offset AF0h	0h
AF8h	AFBh	Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h	0h
B00h	B03h	Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h	0h
B08h	B0Bh	Status for Error Interrupts (StatusErr)—Offset B08h	0h
B10h	B13h	Mask for Transfer Interrupts (MaskTfr)—Offset B10h	0h
B18h	B1Bh	Mask for Block Interrupts (MaskBlock)—Offset B18h	0h
B20h	B23h	Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h	0h
B28h	B2Bh	Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h	0h
B30h	B33h	Mask for Error Interrupts (MaskErr)—Offset B30h	0h
B38h	B3Bh	Clear for Transfer Interrupts (ClearTfr)—Offset B38h	0h
B40h	B43h	Clear for Block Interrupts (ClearBlock)—Offset B40h	0h
B48h	B4Bh	Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h	0h

Table 13-4. Summary of I2C DMA Controller Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
B50h	B53h	Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h	0h
B58h	B5Bh	Clear for Error Interrupts (ClearErr)—Offset B58h	0h
B60h	B63h	Combined Status (StatusInt)—Offset B60h	0h
B98h	B9Bh	DMA Configuration (DmaCfgReg)—Offset B98h	0h
BA0h	BA3h	DMA Channel Enable (ChEnReg)—Offset BA0h	0h

13.4.1 DMA Transfer Source Address Low (SAR_LO0)—Offset 800h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer. Source Address Register for lowe 32-bits for Channels 0-1

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SAR_LO (SAR_LO):** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

13.4.2 DMA Transfer Source Address High (SAR_HI0)—Offset 804h

The starting source address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the source address of the current transfer. Source Address Register for upper 32-bits for Channels 0-1

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SAR_HI (SAR_HI):** Current Source Address of DMA transfer. Updated after each source transfer. The SINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every source transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated source transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Read Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Read address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA read was a burst read (i.e. burst length > 1), the read-back value reflects the first address of the burst read since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA read progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

13.4.3 DMA Transfer Destination Address Low (DAR_LO0)—Offset 808h

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer.Destination Address Register for Channels 0-1

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DAR_LO (DAR_LO):** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

13.4.4 DMA Transfer Destination Address High (DAR_HI0)—Offset 80Ch

The starting destination address is programmed by software before the DMA channel is enabled, or by an LLI update before the start of the DMA transfer. While the DMA transfer is in progress, this register is updated to reflect the destination address of the current transfer. Destination Address Register for Upper 32-bits for Channels 0-1

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DAR_HI (DAR_HI):** Current Destination Address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL_LO[n]: Control Register determines whether the address increments or is left unchanged on every destination transfer throughout the block transfer. When the channel is enabled (i.e. CH_EN is 1), the read back value will reflect the updated destination transfer addresses. However, when the channel is disabled, the original programmed value will be reflected when reading this register. It's important to notice the following: 1. Once the block transfer is in progress (i.e. when channel is enabled), the read-back value correlates with the OCP Write Address that one would see in an OCP tracker. 2. If the read to this register comes during a block transfer, the LAST DMA Write address sent on the OCP before the register read is what's reflected in the read-back value. 3. If the last DMA write was a burst write (i.e. burst length > 1), the read-back value reflects the first address of the burst write since this is what gets sent on the OCP fabric. 4. If the read to the register occurred after the whole block got transferred, then the channel gets disabled and the returned value would be the original programmed value. 5. Since the read-back value is OCP based, only DW aligned addresses will be reflected (i.e. OCP Byte-Enable values would not be reflected) 6. Based on the above remarks, this value should be used as pseudo DMA write progress indicator when the channel is enabled and not an absolute one. Decrementing addresses are not supported.

13.4.5 Linked List Pointer Low (LLP_LO0)—Offset 810h

The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**LOC (LOC):** Starting Address In Memory of next LLI if block chaining is enabled. Note that the two LSBs of the starting address are not stored because the address is assumed to be aligned to a 32-bit boundary. LLI accesses are always 32-bit accesses and cannot be changed or programmed to anything other than 32-bit.
1:0	0h RO	Reserved.

13.4.6 Linked List Pointer High (LLP_HI0)—Offset 814h

The register needs to be programmed to point to the first Linked List Item (LLI) in memory prior to enabling the channel if block chaining is enabled.

13.4.7 Control Register Low (CTL_LO0)—Offset 818h

This register contains fields that control the DMA transfer.The CTL_LO register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	0h RW	**LLP_SRC_EN (LLP_SRC_EN):** Block chaining is enabled on the source side only if the LLP_SRC_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
27	0h RW	**LLP_DST_EN (LLP_DST_EN):** Block chaining is enabled on the destination side only if the LLP_DST_EN field is high and LLPn.LOC is non-zero and (LLP_EN == 1)
26:22	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
21:20	0h RW	**TT_FC (TT_FC):** The following transfer types are supported. 00: Reserved 01: Memory to Peripheral 10: Peripheral to Memory 11: Reserved Flow Control is always assigned to the DMA.
19	0h RO	Reserved.
18	0h RW	**DST_SCATTER_EN (DST_SCATTER_EN):** 0 = Scatter disabled 1 = Scatter enabled Scatter on the destination side is applicable only when the CTL_LOn.DINC bit indicates an incrementing address control.
17	0h RW	**SRC_GATHER_EN (SRC_GATHER_EN):** 0 = Gather disabled 1 = Gather enabled Gather on the source side is applicable only when the CTL_LOn.SINC bit indicates an incrementing address control.
16:14	0h RW	**SRC_MSIZE (SRC_MSIZE):** Number of data items, each of width CTL_LOn.SRC_TR_WIDTH, to be read from the source. Source BURST SIZE (in DW) = (2 ^ SRC_TR_WIDTH)
13:11	0h RW	**DEST_MSIZE (DEST_MSIZE):** Destination Burst Transaction Length. Number of data items, each of width CTL_LOn.DST_TR_WIDTH, to be written to the destination.
10	0h RW	**SINC (SINC):** Source Address Increment. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No Change)
9	0h RO	Reserved.
8	0h RW	**DINC (DINC):** Destination Address Increment. Indicates whether to increment or decrement the destination address on every destination transfer. If your device is writing data to a destination peripheral FIFO with a fixed address, then set this field to No change. 0 = Increment 1 = Fixed (No change)
7	0h RO	Reserved.
6:4	0h RW	**SRC_TR_WIDTH (SRC_TR_WIDTH):** BURST_SIZE (IN DW) = (2^ MSIZE) (i.e. 2 to-the-power-of MSIZE) 1.Transferred Bytes Per Burst = BURST_SIZE * (2 ^ TR_WIDTH) Note that encodings 101 (32 DW), 110 (64 DW) and 111 (128 DW) are not supported. 2.For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported.
3:1	0h RW	**DST_TR_WIDTH (DST_TR_WIDTH):** BURST SIZE (in DW) = (2^ MSIZE) (i.e. 2 to-the-power-of MSIZE) Transferred Bytes Per Burst = BURST_SIZE * (2 ^ TR_WIDTH) Since Max Burst Length is limited to 16 DW, encodings 101 (32 DW), 110 (64 DW) and 111 (128 DW) are not supported. For incrementing addresses and (Transfer_Width < 4 Bytes), the MSIZE parameter is ignored since only single transactions are supported.
0	0h RW	**INT_EN (INT_EN):** Interrupt Enable Bit. If set, then all interrupt-generating sources are enabled.

13.4.8 Control Register High (CTL_HI0)—Offset 81Ch

This register contains fields that control the DMA transfer. The CTL_HI register is part of the block descriptor (linked list item - LLI) when block chaining is enabled. It can be varied on a block-by-block basis within a DMA transfer when block chaining is enabled.If status write-back is enabled, CTL_HI is written to then control registers location of the LLI in system memory at the end of the block transfer.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RW	**CH_CLASS (CH_CLASS):** Channel Class. A Class of (N_CHNLS-1) is the highest priority, and 0 is the lowest. This field must be programmed within 0 to (N_CHNLS-1). A programmed value outside this range will cause erroneous behavior.
28:18	0h NA	**RESERVED (RESERVED0):** Reserved
17	0h RW	**DONE (DONE):** If status write-back is enabled, the upper word of the control register, CTL_HIn, is written to the control register location of the Linked List Item (LLI) in system memory at the end of the block transfer with the done bit set. Software can poll the LLI CTL_HI.DONE bit to see when a block transfer is complete. The LLI CTL_HI.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. The DMA will not transfer the block if the DONE bit in the LLI is not cleared.
16:0	0h RW	**BLOCK_TS (BLOCK_TS):** Block Transfer Size (in Bytes). Since the DMA is always the flow controller, the user needs to write this field before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of bytes to transfer for every block transfer. Once the transfer starts (i.e. channel is enabled), the read-back value is the total number of bytes for which Read Commands have already been sent to the source. It doesnt mean Bytes that are already in the FIFO. However, when the channel is disabled, the original programmed value will be reflected when reading this register.

13.4.9 Source Status (SSTAT0)—Offset 820h

After each block transfer completes, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register. This status information is then stored in the SSTATx register and written out to the SSTATx register location of the LLI before the start of the next block

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SSTAT (SSTAT):** Source status information retrieved by hardware from the address pointed to by the contents of the Source Status Address Register. This register is a temporary placeholder for the source status information on its way to the SSTATn register location of the LLI. The source status information should be retrieved by software from the SSTATn register location of the LLI, and not by a read of this register over the DMA slave interface.

13.4.10 Destination Status (DSTAT0)—Offset 828h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register. This status information is then stored in the DSTATx register and written out to the DSTATx register location of the LLI. Note: This register is a temporary placeholder for the destination status information on its way to the DSTATx register location of the

LLI. The destination status information should be retrieved by software from the DSTATx register location of the LLI and not by a read of this register over the DMA slave interface.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DSTAT (DSTAT):** Destination status information retrieved by hardware from the address pointed to by the contents of the Destination Status Address Register. This register is a temporary placeholder for the destination status information on its way to the DSTATn register location of the LLI. The destination status information should be retrieved by software from the DSTATn register location of the LLI and not by a read of this register over the DMA slave interface

13.4.11 Source Status Address Low (SSTATAR_LO0)—Offset 830h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx registe

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_LO (SSTATAR_LO):** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

13.4.12 Source Status Address High (SSTATAR_HI0)—Offset 834h

After the completion of each block transfer, hardware can retrieve the source status information from the address pointed to by the contents of the SSTATARx register

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**SSTATAR_HI (SSTATAR_HI):** Pointer from where hardware can fetch the source status information, which is registered in the SSTATn register and written out to the SSTATn register location of the LLI before the start of the next block

13.4.13 Destination Status Address Low (DSTATAR_LO0)—Offset 838h

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR_LO (DSTATAR_LO):** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

13.4.14 Destination Status Address High (DSTATAR_HI0)—Offset 83Ch

After the completion of each block transfer, hardware can retrieve the destination status information from the address pointed to by the contents of the DSTATARx register.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**DSTATAR_HI (DSTATAR_HI):** Pointer from where hardware can fetch the destination status information, which is registered in the DSTATn register and written out to the DSTATn register location of the LLI before the start of the next block.

13.4.15 DMA Transfer Configuration Low (CFG_LO0)—Offset 840h

This register contains fields that configure the DMA transfer. The channel configuration register remains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register (Size: 32 bits)

Device:

Function:

Default: 203h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**RELOAD_DST (RELOAD_DST):** Automatic Destination Reload. The DARn register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated
30	0h RW	**RELOAD_SRC (RELOAD_SRC):** Automatic Source Reload. The SARx register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. A new block transfer is then initiated.
29:22	0h RO	Reserved.
21	0h RW	**SRC_OPT_BL (SRC_OPT_BL):** 0 = Writes will use only BL=1 or BL=(2 ^ SRC_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ SRC_MSIZE))
20	0h RW	**DST_OPT_BL (DST_OPT_BL):** 0 = Writes will use only BL=1 or BL=(2 ^ DST_MSIZE) 1 = Writes will use (1 (= BL (= (2 ^ DST_MSIZE))
19	0h RW	**SRC_HS_POL (SRC_HS_POL):** 0 = Active high 1 = Active low
18	0h RW	**DST_HS_POL (DST_HS_POL):** 0 = Active high 1 = Active low
17:11	0h RO	Reserved.
10	0h RW	**CH_DRAIN (CH_DRAIN):** Forces channel FIFO to drain while in suspension. This bit has effect only when CH_SUSPEND ia asserted
9	1h RO	**FIFO_EMPTY (FIFO_EMPTY):** Indicates if there is data left in the channel FIFO. Can be used in conjunction with CFGx.CH_SUSP to cleanly disable a channel. 1 = Channel FIFO empty 0 = Channel FIFO not empty
8	0h RW	**CH_SUSP (CH_SUSP):** Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFGx.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.
7	0h RW	**SS_UPD_EN (SS_UPD_EN):** Source Status Update Enable. Source status information is fetched only from the location pointed to by the SSTATARn register, stored in the SSTATn register and written out to the SSTATn location of the LLI if SS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0
6	0h RW	**DS_UPD_EN (DS_UPD_EN):** Destination Status Update Enable. Destination status information is fetched only from the location pointed to by the DSTATARn register, stored in the DSTATn register and written out to the DSTATn location of the LLI if DS_UPD_EN is high. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
5	0h RW	**CTL_HI_UPD_EN (CTL_HI_UPD_EN):** If set, the CTL_HI register is written out to the CTL_HIn location of the LLI. This bit is ignored if (LLP_EN == 0) or (LLP_WB_EN == 0)
4	0h RO	Reserved.
3	0h RW	**HSHAKE_NP_WR (HSHAKE_NP_WR):** 0x1 : Issues Non-Posted writes on HW-Handshake on DMA Write Port. 0x0 : Issues Posted writes on HW-Handshake on DMA Write Port (Except end-ofblock writes which will be Non-Posted)

Bit Range	Default and Access	Field Name (ID): Description
2	0h RW	**ALL_NP_WR (ALL_NP_WR):** 0x1 : Forces ALL writes to be Non-Posted on DMA Write Port. 0x0 : Non-Posted Writes will only be used at end of block transfers and in HW Handshake (if HW_NP_WR=1); for all other cases, Posted Writes will be used
1	1h RW	**SRC_BURST_ALIGN (SRC_BURST_ALIGN):** 0x1 : SRC Burst Transfers are broken at a Burst Length aligned boundary. 0x0 : SRC Burst Transfers are not broken at a Burst Length aligned boundary.
0	1h RW	**DST_BURST_ALIGN (DST_BURST_ALIGN):** 0x1 : DST Burst Transfers are broken at a Burst Length aligned boundary. 0x0 : DST Burst Transfers are not broken at a Burst Length aligned boundary

13.4.16 DMA Transfer Configuration High (CFG_HI0)—Offset 844h

This register contains fields that configure the DMA transfer. The channel configuration registerremains fixed for all blocks of a multi-block transfer. This Register should be programmed to enabling the channel

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:18	0h RW	**WR_ISSUE_THD (WR_ISSUE_THD):** Write Issue Threshold. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Write burst size = (2 ^ DST_MSIZE)*TW.
17:8	0h RW	**RD_ISSUE_THD (RD_ISSUE_THD):** Read Issue Threshold. Value ranges from 0 to (2^10-1 = 1023) but should not exceed maximum Read burst size = (2 ^ SRC_MSIZE)*TW.
7:4	0h RW	**DST_PER (DST_PER):** Destination Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the destination of channel n. The channel can then communicate with the destination peripheral connected to that interface through the assigned hardware handshaking interface.
3:0	0h RW	**SRC_PER (SRC_PER):** Source Peripheral ID : Assigns a hardware handshaking interface (0 - 15) to the source of channel n. The channel can then communicate with the source peripheral connected to that interface through the assigned hardware handshaking interface.

13.4.17 Source Gather (SGR0)—Offset 848h

The Source Gather register contains two fields: Source gather count field (SGRx.SGC). Specifies the number of contiguous source transfers of CTLx.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary. Source gather interval field (SGRx.SGI). Specifies the source address increment/decrement in multiples of CTLx.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTLx.SINC field controls whether the address increments or decrements. When the CTLx.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGRx register is ignored.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RW	**SGC (SGC):** Source gather count. Source contiguous transfer count between successive gather boundaries.
19:0	0h RW	**SGI (SGI)**

13.4.18 Destination Scatter (DSR0)—Offset 850h

The Destination Scatter register contains two fields: Destination scatter count field (DSRx.DSC) . Specifies the number of contiguous destination transfers of CTLx.DST_TR_WIDTH between successive scatter boundaries. Destination scatter interval field (DSRx.DSI) . Specifies the destination address increment/decrement in multiples of CTLx.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTLx.DINC field controls whether the address increments or decrements. When the CTLx.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSRx register is ignored.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RW	**DSC (DSC):** Destination scatter count. Destination contiguous transfer count between successive scatter boundaries
19:0	0h RW	**DSI (DSI)**

13.4.19 Raw Interrupt Status (RawTfr)—Offset AC0h

Interrupt events are stored in these Raw Interrupt Status registers before masking: RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr. Each Raw Interrupt Status register has a bit allocated per channel, for example, RawTfr(2) is the Channel 2 raw transfer complete interrupt. Each bit in these registers is cleared by writing a 1 to the corresponding location in the ClearTfr, ClearBlock, ClearSrcTran, ClearDstTran, ClearErr registers

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit0 for channel 0 and bit 1 for channel 1.

13.4.20 Raw Status for Block Interrupts (RawBlock)—Offset AC8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

13.4.21 Raw Status for Source Transaction Interrupts (RawSrcTran)—Offset AD0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

13.4.22 Raw Status for Destination Transaction Interrupts (RawDstTran)—Offset AD8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

13.4.23 Raw Status for Error Interrupts (RawErr)—Offset AE0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**RAW (RAW):** Bit 0 for channel 0 and bit 1 for channel 1.

13.4.24 Status for Transfer Interrupts (StatusTfr)—Offset AE8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 for channel 0 and bit 1 for channel 1.

13.4.25 Status for Block Interrupts (StatusBlock)—Offset AF0h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 for channel 0 and bit 1 for channel 1.

13.4.26 Status for Source Transaction Interrupts (StatusSrcTran)—Offset AF8h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 for channel 0 and bit 1 for channel 1.

13.4.27 Status for Destination Transaction Interrupts (StatusDstTran)—Offset B00h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 for channel 0 and bit 1 for channel 1.

13.4.28 Status for Error Interrupts (StatusErr)—Offset B08h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h RO	**STATUS (STATUS):** Bit 0 for channel 0 and bit 1 for channel 1.

13.4.29 Mask for Transfer Interrupts (MaskTfr)—Offset B10h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch 1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask per ch1 and ch0 . 0-mask 1-unmask

13.4.30 Mask for Block Interrupts (MaskBlock)—Offset B18h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask ch1 and ch0. 0-mask 1-unmask

13.4.31 Mask for Source Transaction Interrupts (MaskSrcTran)—Offset B20h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask ch1 and ch0. 0-mask 1-unmask

13.4.32 Mask for Destination Transaction Interrupts (MaskDstTran)—Offset B28h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask ch1 and ch0. 0-mask 1-unmask

13.4.33 Mask for Error Interrupts (MaskErr)—Offset B30h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Interrupt Mask Write Enable ch1 and ch0. 0 = write disabled 1 = write enabled
7:2	0h RO	Reserved.
1:0	0h RW	**INT_MASK (INT_MASK):** Interrupt mask ch1 and ch0. 0-mask 1-unmask

13.4.34 Clear for Transfer Interrupts (ClearTfr)—Offset B38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

13.4.35 Clear for Block Interrupts (ClearBlock)—Offset B40h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

13.4.36 Clear for Source Transaction Interrupts (ClearSrcTran)—Offset B48h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

13.4.37 Clear for Destination Transaction Interrupts (ClearDstTran)—Offset B50h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

13.4.38 Clear for Error Interrupts (ClearErr)—Offset B58h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1:0	0h WO	**CLEAR (CLEAR):** Interrupt clear ch1 and ch0. 0 = no effect 1 = clear interrupt

13.4.39 Combined Status (StatusInt)—Offset B60h

The contents of each of the five Status registers StatusTfr, StatusBlock, StatusSrcTran, StatusDstTran,StatusErr is Ored to produce a single bit for each interrupt type in the Combined Status register (StatusInt). This register is read-only

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**ERR (ERR):** OR of the contents of StatusErr register.
3	0h RO	**DSTT (DSTT):** OR of the contents of StatusDst register.

Bit Range	Default and Access	Field Name (ID): Description
2	0h RO	**SRCT (SRCT):** OR of the contents of StatusSrcTran register
1	0h RO	**BLOCK (BLOCK):** OR of the contents of StatusBlock register.
0	0h RO	**TFR (TFR):** OR of the contents of StatusTfr register.

13.4.40 DMA Configuration (DmaCfgReg)—Offset B98h

This register is used to enable the DMA, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then DmaCfgReg.DMA_EN still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the DmaCfgReg.DMA_EN bit returns 0.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW	**DMA_EN (DMA_EN):** DMA Enable bit. 0 = DMA Disabled 1 = DMA Enabled

13.4.41 DMA Channel Enable (ChEnReg)—Offset BA0h

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive, it can then enable an inactive channel with the required priority. All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg(0), is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH_EN_WE, is asserted on the same OCP write transfer.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:8	0h WO	**RESERVED (RESERVED0):** Channel enable write enable.
7:2	0h RO	Reserved.
1:0	0h RW	**CH_EN (CH_EN):** Enables/Disables the channel. Setting this bit enables a channel, clearing this bit disables the channel. 0 = Disable the Channel 1 = Enable the Channel The ChEnReg.CH_EN bit is automatically cleared by hardware to disable the channel after the last OCP transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer.

13.5 I2C PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 13-5. Summary of I2C PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
200h	203h	PCI Configuration Control for I2C0 (PCICFGCTR1)—Offset 200h	0h
204h	207h	PCI Configuration Control for I2C1 (PCICFGCTR2)—Offset 204h	0h
208h	20Bh	PCI Configuration Control for I2C2 (PCICFGCTR3)—Offset 208h	0h
20Ch	20Fh	PCI Configuration Control for I2C3 (PCICFGCTR4)—Offset 20Ch	0h
210h	213h	PCI Configuration Control for I2C4 (PCICFGCTR5)—Offset 210h	0h
214h	217h	PCI Configuration Control for I2C5 (PCICFGCTR6)—Offset 214h	0h
218h	21Bh	PCI Configuration Control for I2C6 (PCICFGCTR7)—Offset 218h	0h
21Ch	21Fh	PCI Configuration Control for I2C7 (PCICFGCTR8)—Offset 21Ch	0h

13.5.1 PCI Configuration Control for I2C0 (PCICFGCTR1)—Offset 200h

Controls the PCI Configuration Space

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:20	0h RW	**PCICFGCTR1 - PCI IRQ Num Field (PCI_IRQ1):** IRQ number to be sent in the message with data field for PCI Assert_IRQ and PCI_Deassert_IRQ message
19:12	0h RW	**PCICFGCTR1 - ACPI IRQ Field (ACPI_IRQ1):** IRQ number to be sent in the message with data field for ACPI Assert_IRQ and ACPI_Deassert_IRQ message
11:8	0h RW	**Interrupt Pin (IPIN1):** This register indicates the values to be used for Global Interrupts. 0 = No interrupt Pin 1 = INTA 2 = INTB 3 = INTC 4 = INTD 5 - FF: Reserved
7	0h RW	**BAR1 Disable (BAR1_DISABLE1):** BAR1_Disable: BAR1 register in the PCOS space becomes Read only when this bit is set.
6:2	0h RW	**PME Support (PME_SUPPORT1):** The value in this register is XOR with the value in the PME_support strap and reflected in the PME_Support register in the PCI configuration space
1	0h RW	**ACPI Interrupt Enable Field (ACPI_INTR_EN1):** When set, ACPI IRQ number field (bits 19:12) will be used for IRQ messages. When 0, PCI IRQ number field (bits 27:20) will be used for IRQ message.
0	0h RW	**PCICFGCTR1 - PCI CFG Disable Field (PCI_CFG_DIS1):** When set, PCI configuration accesses return UR response When 0, PCI configuration accesses are supported

13.5.2 PCI Configuration Control for I2C1 (PCICFGCTR2)—Offset 204h

Same definition as PCICFGCTR1

13.5.3 PCI Configuration Control for I2C2 (PCICFGCTR3)—Offset 208h

Same definition as PCICFGCTR1.

13.5.4 PCI Configuration Control for I2C3 (PCICFGCTR4)—Offset 20Ch

Same definition as PCICFGCTR1.

13.5.5 PCI Configuration Control for I2C4 (PCICFGCTR5)—Offset 210h

Same definition as PCICFGCTR1.

13.5.6 PCI Configuration Control for I2C5 (PCICFGCTR6)—Offset 214h

Same definition as PCICFGCTR1.

13.5.7 PCI Configuration Control for I2C6 (PCICFGCTR7)—Offset 218h

Same definition as PCICFGCTR1.

13.5.8 PCI Configuration Control for I2C7 (PCICFGCTR8)—Offset 21Ch

Same definition as PCICFGCTR1.

14 SATA Interface (D23: F0)

14.1 SATA Configuration Registers Summary

Table 7. Summary of SATA Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Identifiers (ID)—Offset 0h	XXXX8086h
4h	5h	Command (CMD)—Offset 4h	0h
6h	7h	Device Status (STS)—Offset 6h	210h
8h	8h	Revision ID (RID)—Offset 8h	XXh
9h	9h	Programming Interface (PI)—Offset 9h	1h
Ah	Bh	Class Code (CC)—Offset Ah	106h
Ch	Ch	Cache Line Size (CLS)—Offset Ch	0h
Dh	Dh	Master Latency Timer (MLT)—Offset Dh	0h
Eh	Eh	Header Type (HTYPE)—Offset Eh	0h
10h	13h	MSI-X Table Base Address (MXTBA)—Offset 10h	0h
14h	17h	MSI-X Pending Bit Array Base Address (MXPBA)—Offset 14h	0h
20h	23h	AHCI Index Data Pair Base Address (AIDPBA)—Offset 20h	1h
24h	27h	AHCI Base Address (ABAR)—Offset 24h	0h
2Ch	2Fh	Sub System Identifiers (SS)—Offset 2Ch	0h
34h	34h	Capabilities Pointer (CAP)—Offset 34h	80h
3Ch	3Dh	Interrupt Information (INTR)—Offset 3Ch	100h
70h	71h	PCI Power Management Capability ID (PID)—Offset 70h	A801h
72h	73h	PCI Power Management Capabilities (PC)—Offset 72h	4003h
74h	75h	PCI Power Management Control And Status (PMCS)—Offset 74h	8h
80h	81h	Message Signalled Interrupt Identifier (MID)—Offset 80h	7005h
82h	83h	Message Signalled Interrupt Message Control (MC)—Offset 82h	0h
84h	87h	Message Signalled Interrupt Message Address (MA)—Offset 84h	0h
88h	89h	Message Signalled Interrupt Message Data (MD)—Offset 88h	0h
90h	93h	Port Mapping Register (MAP)—Offset 90h	0h
94h	97h	Port Control And Status (PCS)—Offset 94h	0h
9Ch	9Fh	SATA General Configuration (SATAGC)—Offset 9Ch	0h
A0h	A0h	SATA Initialization Register Index (SIRI)—Offset A0h	0h
A4h	A7h	SATA Initialization Register Data (SIRD)—Offset A4h	0h
A8h	ABh	Serial ATA Capability Register 0 (SATACR0)—Offset A8h	100012h
ACh	AFh	Serial ATA Capability Register 1 (SATACR1)—Offset ACh	48h
C0h	C3h	Scratch Pad (SP)—Offset C0h	0h
D0h	D1h	MSI-X Identifiers (MXID)—Offset D0h	11h
D2h	D3h	MSI-X Message Control (MXC)—Offset D2h	0h
D4h	D7h	MSI-X Table Offset And Table BIR (MXT)—Offset D4h	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
D8h	DBh	MSI-X PBA Offset And PBA BIR (MXP)—Offset D8h	1h
E0h	E3h	BIST FIS Control/Status (BFCS)—Offset E0h	0h
E4h	E7h	BIST FIS Transmit Data 1 (BFTD1)—Offset E4h	0h
E8h	EBh	BIST FIS Transmit Data 2 (BFTD2)—Offset E8h	0h

14.1.1 Identifiers (ID)—Offset 0h

When the MMIO RUN.RUNE=1, read access to this double-word is return with UR.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: XXXX8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO	**Device ID (DID):** Indicates the Device ID of the SATA controller. Refer to the Device and Revision ID Table in Volume 1 for default value.
15:0	8086h RO	**Vendor ID (VID):** 16-bit field which indicates the company vendor as Intel.

14.1.2 Command (CMD)—Offset 4h

Command

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt and MSI is not enabled. 1 = Internal INTx# messages will not be generated.
9	0h RO	Reserved.
8	0h RW	**SERR# Enable (SEE):** 0 = SERR# messages will not be generated. 1 = SERR# messages are generated if STS.DPD register is set or bit 8 of the SATAGC.URD register is set.

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	Reserved.
6	0h RW	**Parity Error Response Enable (PEE):** 0 = Disabled. SATA controller will not generate PERR# when a data parity error is detected. 1 = Enabled. SATA controller will generate PERR# when a data parity error is detected.
5:3	0h RO	Reserved.
2	0h RW	**Bus Master Enable (BME):** Controls the SATA Controller's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands.
1	0h RW	**Memory Space Enable (MSE):** Controls access to the SATA Controller's target memory space (for AHCI).
0	0h RW	**I/O Space Enable (IOSE):** Controls access to the SATA Controller's target I/O space.

14.1.3 Device Status (STS)—Offset 6h

Device Status

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 210h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**Detected Parity Error (DPE):** 0 = No parity error detected by SATA controller. 1 = SATA controller detects a parity error on its interface.
14	0h RW/1C/V	**Signalled System Error (SSE):** 0 = No SERR# detected by SATA controller. 1 = SATA controller detects a SERR# on its interface.
13	0h RW/1C/V	**Received Master-Abort Status (RMA):** 0 = Master abort not generated. 1 = SATA controller received a master abort.
12	0h RW/1C/V	**Received Target-Abort Status (RTA):** 0 = Target abort not generated. 1 = SATA controller received a target abort.
11	0h RW/1C/V	**Signalled Target-Abort Status (STA):** This bit must be set by a target device whenever it terminates a transaction with Target-Abort. Devices that will never signal Target-Abort do not need to implement this bit.
10:9	1h RO	**DEVSEL# Timing Status (DEVT):** 01 = Hardwired; Controls the device select time for the SATA controller’s PCI interface.
8	0h RW/1C/V	**Master Data Parity Error Detected (DPD):** For PCH, this bit can only be set on read completions received from the bus when there is a parity error. 0 = No data parity error received. 1 = SATA controller, as a master, either detects a parity error or sees the parity error line asserted, and the parity error response bit (bit 6 of the command register) is set.
7:5	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	1h RO	**Capabilities List (CL):** Indicates the presence of a capabilities list. The minimum requirement for the capabilities list must be PCI power management for the SATA Controller.
3	0h RO/V	**Interrupt Status (IS):** Reflects the state of INTx# messages, IRQ14 or IRQ15. 0 = Interrupt is cleared (independent of the state of CMD.ID). 1 = Interrupt is to be asserted
2:0	0h RO	Reserved.

14.1.4 Revision ID (RID)—Offset 8h

Revision ID

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 23
Function: 0

Default: XXh

Bit Range	Default & Access	Field Name (ID): Description
7:0	-- RO	**Revision ID (RID):** Indicates stepping of the host controller hardware. Refer to Device ID and Revision Table in Vol1 for specific value.

14.1.5 Programming Interface (PI)—Offset 9h

Programming Interface

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 23
Function: 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
7:0	1h RO	**Interface (IF):** If CC.SCC=06h (AHCI mode), it indicates that this is an AHCI HBA that has a major revision of 1. If CC.SCC=04h (RAID mode), it indicates that there is no programming interface (IF=00h).

14.1.6 Class Code (CC)—Offset Ah

Class Code

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 106h

Bit Range	Default & Access	Field Name (ID): Description
15:8	1h RO	**Base Class Code (BCC):** Indicates that this is a mass storage device.
7:0	6h RO	**Sub Class Code (SCC):** This field specifies the sub-class code of the controller, per the table below: MAP.SMS SCC Register Value 0b 06h (AHCI Controller) 1b 04h (RAID Controller)

14.1.7 Cache Line Size (CLS)—Offset Ch

Cache Line Size

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Cache Line Size (CLS):** This register has no meaning for the SATA controller.

14.1.8 Master Latency Timer (MLT)—Offset Dh

Master Latency Timer

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**Master Latency Timer (MLT):** This register has no meaning for the SATA controller.

14.1.9 Header Type (HTYPE)—Offset Eh

Header Type

Access Method

Type: CFG Register (Size: 8 bits)	**Device:** 23 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Multi-function Device (MFD):** 1: indicates this controller is part of a multi-function device. 0: indicates this controller is a single function device.
6:0	0h RO	**Header Layout (HL):** Indicates that the controller uses a target device layout.

14.1.10 MSI-X Table Base Address (MXTBA)—Offset 10h

This BAR is used to allocate 32K, 16K or 8K Memory space for the MSI-X Table. The Memory space size is determined by BIOS by making bit-14 and bit-13 Read-Only '1' or Read-Write '0' based on SATAGC.MSS[1:0].

Access Method

Type: CFG Register (Size: 32 bits)	**Device:** 23 **Function:** 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RW	**Base Address (BA):** Base address of memory space.
14	0h RW	**Base Address Bit 14 (BAB14):** When SATAGC.MSS[1:0]=00, this bit is Read Only '0' else it's Read Write '0'.
13	0h RW	**Base Address Bit 13 (BAB13):** When SATAGC.MSS[1:0]=00 or 01, this bit is Read Only '0' else it's Read Write '0'.
12:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PF):** Indicates that this range is not pre-fetchable.
2:1	0h RO	**Type (TP):** Indicates that this range can be mapped anywhere in 32-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for Memory space.

14.1.11 MSI-X Pending Bit Array Base Address (MXPBA)—Offset 14h

This BAR is used to allocate 256-byte Memory space for the MSI-X PBA.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RW	**Base Address (BA):** Base address of memory space (aligned to 256B).
7:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PF):** Indicates that this range is not pre-fetchable.
2:1	0h RO	**Type (TP):** Indicates that this range can be mapped anywhere in 32-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for Memory space.

14.1.12 AHCI Index Data Pair Base Address (AIDPBA)—Offset 20h

This BAR is used to allocate I/O space for the AHCI index/data pair mechanism.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:5	0h RW	**Base Address (BA):** Base address of the I/O space.
4:1	0h RO	Reserved.
0	1h RO	**Resource Type Indicator (RTE):** Indicates a request for IO space.

14.1.13 AHCI Base Address (ABAR)—Offset 24h

This register represents a memory BAR allocating space for the AHCI memory registers. Note that Bit[31:16] of this register must be programmed to a value greater than 0 to ensure the memory is mapped to an address of 1 MBytes and greater (i.e. ABAR must be 00010000h or greater). Otherwise, memory cycle targeting the ABAR range may not be accepted. The Memory space size is determined by BIOS by making bit 15:11 Read-Only 1 or Read-Write 0 based on SATAGC.ASSEL[1:0].

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RW	**Base Address (BA):** Base address of register memory space.
18	0h RW	**Base Address Bit 18 (BAB18):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 256K, this bit is Read Only '0' else it's Read Write '0'.
17	0h RW	**Base Address Bit 17 (BAB17):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 128K, this bit is Read Only '0' else it's Read Write '0'.
16	0h RW	**Base Address Bit 16 (BAB16):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 64K, this bit is Read Only '0' else it's Read Write '0'.
15	0h RW	**Base Address Bit 15 (BAB15):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 32K, this bit is Read Only '0' else it's Read Write '0'.
14	0h RW	**Base Address Bit 14 (BAB14):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 16K, this bit is Read Only '0' else it's Read Write '0'.
13:11	0h RW	**Base Address Bit 13-11 (BAB1311):** When SATAGC.ASSEL[2:0] selects an ABAR size bigger than 2K, this bit is Read Only '0' else it's Read Write '0'.
10:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PF):** Indicates that this range is not pre-fetchable
2:1	0h RO	**Type (TP):** Indicates that this range can be mapped anywhere in 32-bit address space
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for register memory space.

14.1.14 Sub System Identifiers (SS)—Offset 2Ch

This register is initialized to logic 0 by the assertion of PLTRST#. This register can be written only once after PLTRST# de-assertion.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value.

14.1.15 Capabilities Pointer (CAP)—Offset 34h

Capabilities Pointer

Access Method

Type: CFG Register (Size: 8 bits)
Device: 23
Function: 0

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
7:0	80h RW/L	**Capability Pointer (CP):** Indicates that the first capability pointer offset is 80h. Note: Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR.

14.1.16 Interrupt Information (INTR)—Offset 3Ch

Interrupt Information

Access Method

Type: CFG Register (Size: 16 bits)
Device: 23
Function: 0

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
15:8	1h RW/O	**Interrupt Pin (IPIN):** This register tells which interrupt pin the device function uses. A value of 1 corresponds to INTA#. A value of 2 corresponds to INTB#. A value of 3 corresponds to INTC#. A value of 4 corresponds to INTD#. This register is not reset by FLR.
7:0	0h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. Interrupt Line register is not reset by FLR.

14.1.17 PCI Power Management Capability ID (PID)—Offset 70h

PCI Power Management Capability ID

Access Method

Type: CFG Register (Size: 16 bits)
Device: 23
Function: 0

Default: A801h

Bit Range	Default & Access	Field Name (ID): Description
15:8	A8h RW/L	**Next Capability (NEXT):** A8h is the location of the Serial ATA capability structure. Note: Refer to the SGC.REGLOCK description in order to lock the register to become RO.
7:0	1h RO	**Cap ID (CID):** Indicates that this pointer is a PCI power management capability.

14.1.18 PCI Power Management Capabilities (PC)—Offset 72h

PCI Power Management Capabilities

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 4003h

Bit Range	Default & Access	Field Name (ID): Description
15:11	8h RO	**PME_Support (PME_SUPPORT):** The default value 01000 which indicates PME# can be generated from the D3HOT state in the SATA controller.
10	0h RO	**D2_Support (D2_SUPPORT):** The D2 state is not supported.
9	0h RO	**D1_Support (D1_SUPPORT):** The D1 state is not supported.
8:6	0h RO	**Aux_Current (AUX_CURRENT):** PME# from D3COLD state is not supported, therefore this field is 000b.
5	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	0h RO	Reserved.
3	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.

14.1.19 PCI Power Management Control And Status (PMCS)—Offset 74h

PCI Power Management Control And Status

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**PME Status (PMES):** Bit is set when a PME event is to be requested, and if this bit and PMEE is set, a PME# will be generated from the SATA controller.
14:9	0h RO	Reserved.
8	0h RW	**PME Enable (PMEE):** When set, the SATA controller asserts PME# when exiting D3HOT on a wake event. Note: Software is advised to clear PMEE and PMES together prior to changing CC.SCC through MAP.SMS.
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NSFRST):** These bits are used to indicate whether devices transitioning from D3HOT state to D0 state will perform an internal reset. 0 = Device transitioning from D3HOT state to D0 state perform an internal reset. 1 = Device transitioning from D3HOT state to D0 state do not perform an internal reset. Configuration content is preserved. Upon transition from the D3HOT state to D0 state initialized state, no additional operating system intervention is required to preserve configuration context beyond writing to the PowerState bits. Regardless of this bit, the controller transition from D3HOT state to D0 state by a system or bus segment reset will return to the state D0 uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PS):** These bits are used both to determine the current power state of the SATA controller and to set a new power state. 00 = D0 state 11 = D3HOT state When in the D3HOTstate, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked.

14.1.20 Message Signalled Interrupt Identifier (MID)—Offset 80h

Message Signalled Interrupt Identifier

Access Method

Type: CFG Register (Size: 16 bits)

Device: 23

Function: 0

Default: 7005h

Bit Range	Default & Access	Field Name (ID): Description
15:8	70h RW/L	**Next Pointer (NEXT):** Indicates the next item in the list is the PCI power management pointer. BIOS may program this field to A8h indicating that the next item is Serial ATA Capability Structure. Note: Refer the SGC.REGLOCK description in order to lock the register to become RO.
7:0	5h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

14.1.21 Message Signalled Interrupt Message Control (MC)—Offset 82h

Message Signalled Interrupt Message Control

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	0h RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only.
6:4	0h RO	**Multiple Message Enable (MME):** When this field is cleared to 000 (and MSIE is set), only a single MSI message will be generated for all SATA ports, and bits [15:0] of the message vector will be driven from MD[15:0].
3:1	0h RO	**Multiple Message Capable (MMC):** Not supported.
0	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. Note that CMD.ID bit has not effect on MSI. Software must clear this bit to 0 to disable MSI first before changing the number of messages allocated in the MMC field.

14.1.22 Message Signalled Interrupt Message Address (MA)—Offset 84h

Message Signalled Interrupt Message Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DWORD aligned.
1:0	0h RO	Reserved.

14.1.23 Message Signalled Interrupt Message Data (MD)—Offset 88h

Message Signalled Interrupt Message Data

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word of the data bus of the MSI memory write transaction.

14.1.24 Port Mapping Register (MAP)—Offset 90h

Port Mapping Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW/O	**SATA Port 1 Disable (SPD1):** Similar to SPD0 but for port 1. This bit is only applicable to project(s) that has port 1 physically.
16	0h RW/O	**SATA Port 0 Disable (SPD0):** A 1 prevents the SATA port from being enabled via config PCS.PxE. Write of 1 to PCS.PxE has no effect when the corresponding SPD[x] bit is 1. In preventing a port(s) from being enabled, BIOS shall first configure MAP.SPDx. And only then BIOS configures the PCS.PxE. This bit is only applicable to project(s) that has port 0 physically.
15:8	0h RO	Reserved.
7:0	0h RW	**Port Clock Disable (PCD):** When any of these bits is set to 1, the clock driven to the associated port logic is gated and will not toggle. When this bit is cleared to 0, all clocks to the associated port logic will operate normally. Assignment of the bits is: Bit 0: Port 0 Bit 1: Port 1 ... Bit 7: Port 7 NOTE: if a port is not available, the bit is not applicable and reserved.

14.1.25 Port Control And Status (PCS)—Offset 94h

By default, the SATA ports are set (by hardware) to the disabled state (e.g. bits[5:0] == '0') as a result of an initial power on reset. When enabled by software, the ports can transition between the on, partial, and slumber states and can detect devices. When disabled, the port is in the off state and cannot detect any devices. Note: This register is not reset by FLR. Note: AHCI specific notes: If an AHCI-aware or RAID enabled operating system is being booted then system BIOS shall insure that all supported SATA ports are enabled prior to passing control to the OS. Once the AHCI aware OS is booted it becomes the enabling/disabling policy owner for the individual SATA ports. This is accomplished by manipulating a port's PxSCTL.DET and PxCMD.SUD fields. Because an AHCI or RAID aware OS will typically not have knowledge of the PxE bits and because the PxE bits act as master on/off switches for the ports, pre-boot software must insure that these bits are set to '1' prior to booting the OS, regardless as to whether or not a device is currently on the port.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RO/V	**Port 1 Present (P1P):** This bit is set when COMINIT is received as a response to COMRESET. 0 = No device detected. 1 = The presence of a device on Port 1 has been detected. The status of this bit may change at any time. This bit is cleared when the port is disabled using P1E. This bit is not cleared upon surprise removal of a device.
16	0h RO/V	**Port 0 Present (P0P):** This bit is set when COMINIT is received as a response to COMRESET. 0 = No device detected. 1 = The presence of a device on Port 0 has been detected. The status of this bit may change at any time. This bit is cleared when the port is disabled using P0E. This bit is not cleared upon surprise removal of a device.
15:2	0h RO	Reserved.
1	0h RW/V	**Port 1 Enabled (P1E):** 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. Note: This bit takes precedence over P1CMD.SUD (offset ABAR+198h:bit 1). When MAP.SPD[1] is 1, this is reserved and is read-only 0.
0	0h RW/V	**Port 0 Enabled (P0E):** 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. Note: This bit takes precedence over P0CMD.SUD (offset ABAR+118h:bit 1). When MAP.SPD[0] is 1, this is reserved and is read-only 0.

14.1.26 SATA General Configuration (SATAGC)—Offset 9Ch

SATA General Configuration

Access Method

Type: CFG Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/O	**Register Lock (REGLOCK):** 0 = Will not lock CAP.CP, PID.NEXT, MID.NEXT, or SATACR0.NEXT 1 = Setting this bit will lock CAP.CP, PID.NEXT, MID.NEXT, and SATACR0.NEXT. Once locked, these register bits will become RO. BIOS is requested to program this field to '1' prior to OS handoff. Note: This field is not reset by FLR.
30:16	0h RO	Reserved.
15	0h RW	**Data Phase Parity Error Enable (DPPEE):** When '1', IOSF data phase parity error handling is enabled. When '0', the data phase parity error handling is disabled. Note: This field is not reset by FLR.
14:12	0h RW	**Write Request_Size Select/Max_Payload_Size (WRRSELMPS):** These two bits select the max write request size that SATA host controller will initiate for DMA write to memory. SATA host controller will internally break up larger write request based on these bits. The request is address-aligned to the selected size. Defined encodings for this field are: 000b = 128 address aligned bytes max payload size 111b = 64 address aligned bytes max payload size. All other values are reserved for SATA host controller. Note: This field is not reset by FLR (not supported).
11	0h RW	**Command Parity Error Enable (CPEE):** When '1', command parity error handing is enable. When '0' the command parity error handling is disabled. Note: This field is not reset by FLR.
10	0h RW	**SATA Controller Function Disable (SCFD):** BIOS program this bit to 1 to disable the SATA Controller function. When 0, SATA Controller function is enabled. When disable, SATA Host Controller will not claimed the register access targeting its Configuration Space. In IOSF primary Fabric Decode scheme, it's expected BIOS also program the corresponding bit used by the Fabric Decoder accordingly hence both SATA SIP and Fabric Decoder are in sync, and BIOS need to program this bit before programming the one in Fabric Decoder. Once this bit is set, BIOS isnot able to revert it back to Function Enable until next round of platform reset. This register field is not reset by FLR.
9	0h RW	**Unsupported Request Reporting Enable (URRE):** If set to 1 by software, it allows reporting of an Unsupported Request as a system error. If both URRE and PCI configuration SERR# Enable registers are set to a 1, then the agent must set the Signaled System Error bit in the PCI Status register and send a DO_SERR message in IOSF-SB interface.
8	0h RW/1C/V	**Unsupported Request Detected (URD):** Set to 1 by hardware upon detecting an Unsupported Request on IOSF Primary interface that is not considered Advisory Non-Fatal. Cleared to 0 by SW. URD bit is only set based on IOSF primary bus interface activity. Its not set based on IOSF sideband bus interface activity.
7	0h RW/O	**Alternate ID Enable (AIE):** 0 = Clearing this bit when in RAID mode, the SATA Controller located at Device 23: Function 0 will report its Device ID as 2822h for Desktop SKUs or 282Ah for Mobile SKUs of the PCH. Clearing this bit is required for the Intel® Rapid Storage Technology driver (including the Windows* Vista operating system and later in-box version of the driver) to load on the platform. Intel® Smart Response Technology also requires that the bit be cleared in order to be enabled on the platform. 1 = Setting this bit when in RAID mode, the SATA Controller located at Device 23: Function 0 will report its Device ID as A107h for Desktop SKUs or 9D07h for Mobile SKUs of the Chipset. This setting will prevent the Intel® Rapid Storage Technology driver (including the Windows* operating system in-box version of the driver) from loading on the platform. During the Windows* OS installation, the user will be required to "load" (formerly done by pressing the F6 button on the keyboard) the appropriate RAID storage driver that is enabled by this setting. Note: BIOS is recommended to program this bit prior to programming the MAP.SMS field to reflect RAID. This field is reset by PLTRST# and BIOS is required to reprogram the value (either 0 or 1) after resuming from S3, S4 or S5. This insures that the value is properly and cannot be changed during runtime. Note: This field is not reset by FLR (not supported).
6	0h RW/O/V	**AIE0 DevID Selection (DEVIDSEL):** This register allows BIOS to select Device ID when AIE=0. This bit only has effect in Desktop SKU. In Mobile SKU this bit has no effect at all. Refer to config register offset 09h PI for usage. 0 : 2822h 1 : 2826h Note: This field is not reset by FLR.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/O	**FLR Capability Selection (FLRCSSEL):** This allows the FLR Capability to be bypassed. Refer to config offset B0h. BIOS is required to program this bit to 1 and config offset A8h SATACR0.NEXT to 00h. Note: This field is not reset by FLR.
4:3	0h RW/O	**MXTBA Size Select (MSS):** These 2 bits select the size of the Memory space for the MSI-X Table defined in BAR 0 (Configuration space offset 10h). MSS[1:0] MSI-X Table Memory space size 00 32K 01 16K 10 8K 11 Reserved Note: This field is not reset by FLR (not supported).
2:0	0h RW/O	**ABAR Size Select (ASSEL):** These 3 bits select the size of the Memory space for the ABAR in BAR 5 (Configuration space offset 24h). ASSEL[2:0] ABAR Memory space size 000 2K 001 16K 010 32K 011 64K 100 128K 101 256K 110 512K 111 Reserved Note: This field is not reset by FLR (not supported).

14.1.27 SATA Initialization Register Index (SIRI)—Offset A0h

SATA Initialization Register Index

Access Method

Type: CFG Register (Size: 8 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
7:2	0h RW	**Index (IDX):** 6-bit index pointer into the 256-byte space. Data is written into the SIRD (DFTD) register and read from the SIRD register. This point to a DWord register. The byte enables on the SIRD register affect what will be written.
1:0	0h RO	Reserved.

14.1.28 SATA Initialization Register Data (SIRD)—Offset A4h

SATA Initialization Register Data

Access Method

Type: CFG Register (Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**Data (DTA):** 32-bit data value that is written to the register pointed to by SIRI, or read from the register pointed to by SIRI.

14.1.29 Serial ATA Capability Register 0 (SATACR0)—Offset A8h

The SATACR0.NEXT is not changed from RO to become RWO because there is an existing method (SATAGC.FLRCSSEL bit) to bypass the FLR Capability structure, and since the FLR Capability ID.NEXT is already indicating end of capability structure, it does not need change to be RWO.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 100012h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:20	1h RO	**Major Revision (MAJREV):** Major revision number of the SATA Capability Pointer implemented.
19:16	0h RO	**Minor Revision (MINREV):** Minor revision number of the SATA Capability Pointer implemented.
15:8	0h RW/L	**Next Capability Pointer (NEXT):** 00h indicating the final item in the Capability List. The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR.
7:0	12h RO	**Capability ID (CAP):** The value of 12h has been assigned by the PCI SIG to designate the SATA Capability pointer.

14.1.30 Serial ATA Capability Register 1 (SATACR1)—Offset ACh

Serial ATA Capability Register 1

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 48h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:4	4h RO	**BAR Offset (BAROFST):** Indicates the offset into the BAR where the Index/Data pair are located (in DWord granularity). The Index and Data I/O registers are located at offset 10h within the I/O space defined by LBAR. A value of 004h indicates offset 10h. 000h = 0h offset 001h = 4h offset 002h = 8h offset 003h = Bh offset 004h = 10h offset ... FFFh = 3FFFh offset (maximum 16KB)
3:0	8h RO	**BAR Location (BARLOC):** Indicates the absolute PCI Configuration register address of the BAR containing the Index/Data pair (in DWord granularity). The Index and Data I/O registers reside within the space defined by LBAR in the SATA controller. A value of 8h indicates offset 20h, which is LBAR. 0000 - 0011b = reserved 0100b = 10h => BAR0 0101b = 14h => BAR1 0110b = 18h => BAR2 0111b = 1Ch => BAR3 1000b = 20h => LBAR 1001b = 24h => BAR5 1010–1110b = reserved 1111b = Index/Data pair in PCI Configuration space. This is not supported in the PCH.

14.1.31 Scratch Pad (SP)—Offset C0h

Scratch Pad

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DT):** This is a read/write register that is available for software to use. No hardware action is taken on this register.

14.1.32 MSI-X Identifiers (MXID)—Offset D0h

MSI-X Identifiers

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 11h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW/L	**Next Pointer (NEXT):** Indicates the next item in the list. This may be other capability pointers or it may be the last item in the list.The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO. This register is not reset by FLR.
7:0	11h RO	**Capability ID (CID):** Capabilities ID indicates this is an MSI-X capability.

14.1.33 MSI-X Message Control (MXC)—Offset D2h

MSI-X Message Control

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**MSI-X Enable (MXE):** If set to '1' and the MSI Enable bit in the MSI Message Control register is cleared to '0', the function is permitted to use MSI-X to request service and is prohibited from using its INTx# pin (if implemented). If cleared to '0', the function is prohibited from using MSI-X to request service.
14	0h RW	**Function Mask (FM):** If set to '1', all of the vectors associated with the function are masked, regardless of their per vector Mask bit states. If cleared to '0', each vector's Mask bit determines whether the vector is masked or not. Setting or clearing the MSI-X Function Mask bit has no effect on the state of the per vector Mask bits.
13:11	0h RO	Reserved.
10:0	0h RO	**Table Size (TS):** This value indicates the size of the MSI-X Table as the value n, which is encoded as n - 1. For example, a returned value of 3h corresponds to a table size of 4..

14.1.34 MSI-X Table Offset And Table BIR (MXT)—Offset D4h

MSI-X Table Offset And Table BIR

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RW/O	**Table Offset (TO):** Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X Table. The lower three Table BIR bits are masked off (cleared to 000b) by system software to form a 32-bit Qword-aligned offset.
2:0	0h RO	**Table BIR (TBIR):** This field indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X Table into system memory. A read-only value of '0' means 10h.

14.1.35 MSI-X PBA Offset And PBA BIR (MXP)—Offset D8h

MSI-X PBA Offset And PBA BIR

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RW/O	**PBA Offset (PBAO):** Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X PBA. The lower three PBA BIR bits are masked off (cleared to 000b) by software to form a 32-bit Qword-aligned offset.
2:0	1h RO	**PBA BIR (PBIR):** This field indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X PBA into system memory. A read-only value of '1' means 14h.

14.1.36 BIST FIS Control/Status (BFCS)—Offset E0h

BIST FIS Control/Status

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RW	**Port 2 BIST FIS Initiate (P2BFI):** When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 2,using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 2 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PCS.P2E prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P2BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully. Note: Bit may be Reserved depending on if port is available in the given SKU.
11	0h RW/1C/V	**BIST FIS Successful (BFS):** 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a BIST FIS transmitted by PCH receives an R_OK completion status from the device. Note: This bit must be cleared by software prior to initiating a BIST FIS.
10	0h RW/1C/V	**BIST FIS Failed (BFF):** 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a BIST FIS transmitted by PCH receives an R_ERR completion status from the device. Note: This bit must be cleared by software prior to initiating a BIST FIS.
9	0h RW	**Port 1 BIST FIS Initiate (P1BFI):** When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 1,using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 1 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PCS.P1E prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P1BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully.
8	0h RW	**Port 0 BIST FIS Initiate (P0BFI):** When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 0,using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 0 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PCS.P0E prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P0BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully.
7:2	0h RW	**BIST FIS Parameters (BFP):** These 6 bits form the contents of the upper 6 bits of the BIST FIS Pattern Definition in any BIST FIS transmitted by the PCH. This field is not port specific—its contents will be used for any BIST FIS initiated on port 0, port 1, port 2, or port 3. The specific bit definitions are: Bit 7: T – Far End Transmit mode Bit 6: A – Align Bypass mode Bit 5: S – Bypass Scrambling Bit 4: L – Far End Retimed Loopback Bit 3: F – Far End Analog Loopback Bit 2: P – Primitive bit for use with Transmit mode
1:0	0h RO	Reserved.

14.1.37 BIST FIS Transmit Data 1 (BFTD1)—Offset E4h

BIST FIS Transmit Data 1

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DATA):** The data programmed into this register will form the contents of the second DW of any BIST FIS initiated by the SATA controller. This register is not port specific - its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the T bit of the BIST FIS is set to indicate Far-End Transmit mode, this register's contents will be transmitted as the BIST FIS 2nd DW regardless of whether or not the T bit is indicated in the BFCS register.

14.1.38 BIST FIS Transmit Data 2 (BFTD2)—Offset E8h

BIST FIS Transmit Data 2

Access Method

Type: CFG Register (Size: 32 bits)

Device: 23

Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Data (DATA):** The data programmed into this register will form the contents of the third DW of any BIST FIS initiated by the SATA controller. This register is not port specific - its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the T bit of the BIST FIS is set to indicate Far-End Transmit mode, this register's contents will be transmitted as the BIST FIS 3rd DW regardless of whether or not the T bit is set in the BFCS register.

14.2 SATA ABAR Registers Summary

Table 14-1. Summary of SATA ABAR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	HBA Capabilities (GHC_CAP)—Offset 0h	FF34FF07h
4h	7h	Global HBA Control (GHC)—Offset 4h	80000000h
8h	Bh	Interrupt Status Register (IS)—Offset 8h	0h
Ch	Fh	Ports Implemented (GHC_PI)—Offset Ch	0h
10h	13h	AHCI Version (VS)—Offset 10h	10300h
1Ch	1Fh	Enclosure Management Location (EM_LOC)—Offset 1Ch	1600002h
20h	23h	Enclosure Management Control (EM_CTL)—Offset 20h	7010000h
24h	27h	HBA Capabilities Extended (GHC_CAP2)—Offset 24h	3Ch
A0h	A3h	Vendor Specific (VSP)—Offset A0h	48h
A4h	A7h	Vendor Specific Capabilities Register (VS_CAP)—Offset A4h	1002DEh
C0h	C3h	RAID Platform ID (RPID)—Offset C0h	311C02h
C4h	C5h	Premium Feature Block (PFB)—Offset C4h	0h
C8h	C9h	SW Feature Mask (SFM)—Offset C8h	3Fh
100h	103h	Port 0 Command List Base Address (P0CLB)—Offset 100h	0h
104h	107h	Port 0 Command List Base Address Upper 32-bits (P0CLBU)—Offset 104h	0h

Table 14-1. Summary of SATA ABAR Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
108h	10Bh	Port 0 FIS Base Address (P0FB)—Offset 108h	0h
10Ch	10Fh	Port 0 FIS Base Address Upper 32-bits (P0FBU)—Offset 10Ch	0h
110h	113h	Port 0 Interrupt Status (P0IS)—Offset 110h	0h
114h	117h	Port 0 Interrupt Enable (P0IE)—Offset 114h	0h
118h	11Bh	Port 0 Command (P0CMD)—Offset 118h	4h
120h	123h	Port 0 Task File Data (P0TFD)—Offset 120h	9h
124h	127h	Port 0 Signature (P0SIG)—Offset 124h	FFFFFFFFh
128h	12Bh	Port 0 Serial ATA Status (P0SSTS)—Offset 128h	0h
12Ch	12Fh	Port 0 Serial ATA Control (P0SCTL)—Offset 12Ch	0h
130h	133h	Port 0 Serial ATA Error (P0SERR)—Offset 130h	0h
134h	137h	Port 0 Serial ATA Active (P0SACT)—Offset 134h	0h
138h	13Bh	Port 0 Command Issue (P0CI)—Offset 138h	0h
144h	147h	Port 0 Device Sleep (P0DEVSLP)—Offset 144h	1E022852h
180h	183h	Port 1 Command List Base Address (P1CLB)—Offset 180h	0h
184h	187h	Port 1 Command List Base Address Upper 32-bits (P1CLBU)—Offset 184h	0h
188h	18Bh	Port 1 FIS Base Address (P1FB)—Offset 188h	0h
18Ch	18Fh	Port 1 FIS Base Address Upper 32-bits (P1FBU)—Offset 18Ch	0h
190h	193h	Port 1 Interrupt Status (P1IS)—Offset 190h	0h
194h	197h	Port 1 Interrupt Enable (P1IE)—Offset 194h	0h
198h	19Bh	Port 1 Command (P1CMD)—Offset 198h	0h
1A0h	1A3h	Port 1 Task File Data (P1TFD)—Offset 1A0h	0h
1A4h	1A7h	Port 1 Signature (P1SIG)—Offset 1A4h	0h
1A8h	1ABh	Port 1 Serial ATA Status (P1SSTS)—Offset 1A8h	0h
1ACh	1AFh	Port 1 Serial ATA Control (P1SCTL)—Offset 1ACh	0h
1B0h	1B3h	Port 1 Serial ATA Error (P1SERR)—Offset 1B0h	0h
1B4h	1B7h	Port 1 Serial ATA Active (P1SACT)—Offset 1B4h	0h
1B8h	1BBh	Port 1 Command Issue (P1CI)—Offset 1B8h	0h
1C4h	1C7h	Port 1 Device Sleep (P1DEVSLP)—Offset 1C4h	0h

14.2.1 HBA Capabilities (GHC_CAP)—Offset 0h

HBA Capabilities. This register indicates basic capabilities of the HBA to driver software. The RWO bits in this register are only cleared upon PLTRST#. This register is not reset by FLR.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 23
Function: 0

Default: FF34FF07h

Bit Range	Default and Access	Field Name (ID): Description
31	1h RW/O	**Supports 64-bit Addressing (S64A):** Indicates that the SATA controller can access 64-bit data structures. The 32-bit upper bits of the port DMA Descriptor, the PRD Base, and each PRD entry are read/write.
30	1h RW/O	**Supports Native Command Queuing Acceleration (SCQA):** When set to 1, indicates that the SATA controller supports SATA command queuing using the DMA Setup FIS. The PCH handles DMA Setup FISes natively, and can handle auto-activate optimization through that FIS.
29	1h RW/O	**Supports SNotification Register (SSNTF):** When set to 1, indicates the SATA controller supports the PxSNTF (SNotification) register and its associated functionality. When cleared to 0, the SATA controller does not support the PxSNTF (SNotification) register and its associated functionality.
28	1h RW/O	**Supports Mechanical Presence Switch (SMPS):** When set to 1, indicates whether the SATA controller supports mechanical presence switches on its ports for use in hot-plug operations. This value is loaded by platform BIOS prior to operating system initialization. If this bit is set, BIOS must also map the SATAGP pins to the SATA controller through GPIO space.
27	1h RW/O	**Supports Staggered Spin-up (SSS):** Indicates whether the SATA controller supports staggered spin-up on its ports, for use in balancing power spikes. This value is loaded by platform BIOS prior to OS initialization. 0 = Staggered spin-up not supported. 1 = Staggered spin-up supported.
26	1h RW/O	**Supports Aggressive Link Power Management (SALP):** 0 = Software shall treat the PxCMD.ALPEand PxCMD.ASP bits as reserved. 1 = The SATA controller supports auto-generating link requests to the partial or slumber states when there are no commands to process.
25	1h RW/O	**Supports Activity LED (SAL):** Indicates the SATA controller supports a single output pin (SATALED#) which indicates activity.
24	1h RW/O	**Supports Command List Override (SCLO):** When set to 1, indicates that the HBA supports the PxCMD.CLO bit and it's associated function. When cleared to 0., The HBA is not capable of clearing the BSY and DRQ bits in the Status register in order to issue a software reset if these bits are still set from a previous operation.
23:20	3h RW/O	**Interface Speed Support (ISS):** Indicates the maximum speed the SATA controller can support on its ports. 1h = 1.5Gb/s 2h = 3Gb/s 3h = 6Gb/s The default of this field is dependent upon the PCH SKU. If at least one PCH SATA port supports 6Gb/s, the default will be 3h. If no PCH SATA ports support 6Gb/s, then the default will be 2h and writes of 3h will be ignored by the PCH. Refer to Volume 1, Chapter 1 for details on 6Gb/s port availability.
19	0h RO	Reserved.
18	1h RO	**Supports AHCI mode only (SAM):** The SATA controller may optionally support AHCI access mechanism only. 0 = SATA controller supports both IDE and AHCI Modes 1 = SATA controller supports AHCI Mode Only Note: BIOS should program this field as “1” since IDE mode is not supported.
17	0h RO	**Supports Port Multiplier (SMP):** Not supported.
16	0h RO	Reserved.
15	1h RO	**PIO Multiple DRQ Block (PMD):** Hardwired to 1. The SATA controller supports PIO Multiple DRQ Command Block.
14	1h RW/O	**Slumber State Capable (SSC):** When set to 1, the SATA controller supports the slumber state.
13	1h RW/O	**Partial State Capable (PSC):** When set to 1, the SATA controller supports the partial state.
12:8	1Fh RO	**Number of Command Slots (NCS):** Hardwired to 1Fh to indicate support for 32 slots.
7	0h RO	**Command Completion Coalescing Supported (CCCS):** 0 = Command Completion Coalescing Not Supported 1 = Command Completion Coalescing Supported

Bit Range	Default and Access	Field Name (ID): Description
6	0h RO	**Enclosure Management Supported (EMS):** 0 = Enclosure Management Not Supported 1 = Enclosure Management Supported
5	0h RW/O	**Supports External SATA (SXS):** 0 = External SATA is not supported on any ports 1 = External SATA is supported on one or more ports When set, software can examine each SATA port's Command register (PxCMD.ESP) to determine which port is routed externally.
4:0	7h RO	**Number of Ports (NP):** Indicates number of supported ports. The number of ports indicated in this field may be more than the number of ports indicated in the PI (ABAR + 0Ch) register. Field value dependent on number of ports available in a given SKU.

14.2.2 Global HBA Control (GHC)—Offset 4h

Global HBA Control. This register controls various global actions of the HBA.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 80000000h

Bit Range	Default and Access	Field Name (ID): Description
31	1h RO	**AHCI Enable (AE):** When set, indicates that an AHCI driver is loaded and communication to the HBA shall be via AHCI mechanisms. This can be used by an HBA that supports both legacy mechanisms (such as SFF-8038i) and AHCI to know when the HBA is running under an AHCI driver. 0 = Software will only communicate with the HBA using legacy mechanisms. 1 = Software shall only talk to the HBA using AHCI. The HBA will not have to allow command processing via both AHCI and legacy mechanisms. Note: Software shall set this bit to 1 before accessing other AHCI registers. Note: The implementation of this bit is dependent upon the value of the CAP.SAM bit. If CAP.SAM is '0', then GHC.AE should be RW and shall have a reset value of '0'. If CAP.SAM is '1', then GHC.AE shall be read only and shall have a reset value of '1'.
30:3	0h RO	Reserved.
2	0h RO	**MSI Revert to Single Message (MRSM):** When set to 1 by hardware, indicates that the HBA requested more than one MSI vector but has reverted to using the first vector only. When this bit is cleared to 0, the HBA has not reverted to single MSI mode (i.e. hardware is already in single MSI mode, software has allocated the number of messages requested, or hardware is sharing interrupt vectors if MC.MME < MC.MMC). The HBA may revert to single MSI mode when the number of vectors allocated by the host is less than the number requested. This bit shall only be set to 1 when the following conditions hold: MC.MSIE = 1 (MSI is enabled) MC.MMC > 0 (multiple messages requested) MC.MME > 0 (more than one message allocated) MC.MME != MC.MMC (messages allocated not equal to number requested) When this bit is set to 1, single MSI mode operation is in use and software is responsible for clearing bits in the IS register to clear interrupts. This bit shall be cleared to 0 by hardware when any of the four conditions stated is false. This bit is also cleared to 0 when MC.MSIE = 1 and MC.MME = 0h. In this case, the hardware has been programmed to use single MSI mode, and is not reverting to that mode. For PCH, the HBA shall always revert to single MSI mode when the number of vectors allocated by the host is leass than the number requested. Value of MRSM is a don't care when GHC.HR=1.
1	0h RW	**Interrupt Enable (IE):** This global bit enables interrupts from the PCH. 0 = All interrupt sources from all ports are disabled. 1 = Interrupts are allowed from the AHCI controller.
0	0h RW/1S	**HBA Reset (HR):** Resets the PCH AHCI controller. 0 = No effect. 1 = When set by software, this bit causes an internal reset of the PCH AHCI controller. All state machines that relate to data transfers and native command queuing will return to an idle condition, and all ports are re-initialized using COMRESET.

14.2.3 Interrupt Status Register (IS)—Offset 8h

Interrupt Status Register. This register indicates which of the ports within the controller have an interrupt pending and require service.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW/1C	**Interrupt Pending Status Port 2 (IPS2):** This bit is only applicable to system that has Port 2 physically. 0 = No interrupt pending. 1 = Port 2 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt
1	0h RW/1C	**Interrupt Pending Status Port 1 (IPS1):** This bit is only applicable to system that has Port 1 physically. 0 = No interrupt pending. 1 = Port 1 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
0	0h RW/1C	**Interrupt Pending Status Port 0 (IPS0):** This bit is only applicable to system that has Port 0 physically. 0 = No interrupt pending. 1 = Port 0 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.

14.2.4 Ports Implemented (GHC_PI)—Offset Ch

Ports Implemented. This register indicates which ports are exposed to the HBA. It is loaded by platform BIOS. It indicates which ports that the device supports are available for software to use. Any available port may not be implemented. This register is not reset by FLR. There is BIOS programming requirement on the PI register.

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
2	0h RW/O	**Port 2 Implemented (PI2):** 0 = The port is not implemented. 1 = The port is implemented. Note: This bit may be Reserved and is RO '0' depending on if port is available in the given SKU. Refer to Volume 1, Chapter 1 for details if port is available.
1	0h RW/O	**Port 1 Implemented (PI1):** 0 = The port is not implemented. 1 = The port is implemented.
0	0h RW/O	**Port 0 Implemented (PI0):** 0 = The port is not implemented. 1 = The port is implemented.

14.2.5 AHCI Version (VS)—Offset 10h

AHCI Version. This register indicates the major and minor version of the AHCI specification. It is BCD encoded. The upper two bytes represent the major version number, and the lower two bytes represent the minor version number. Example: Version 3.12 would be represented as 00030102h.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 23
Function: 0

Default: 10300h

Bit Range	Default and Access	Field Name (ID): Description
31:16	1h RO	**Major Version Number (MJR):** Indicates the major version is 1
15:0	300h RO	**Minor Version Number (MNR):** Indicates the minor version is 30

14.2.6 Enclosure Management Location (EM_LOC)—Offset 1Ch

Enclosure Management Location. The enclosure management location register identifies the location and size of the enclosure management message buffer. This register is not implemented if enclosure management is not supported (i.e. CAP.EMS = 0).

Access Method

Type: MEM Register (Size: 32 bits)

Device: 23
Function: 0

Default: 1600002h

Bit Range	Default and Access	Field Name (ID): Description
31:16	160h RO	**Offset (OFST):** The offset of the message buffer in Dwords from the beginning of the ABAR.
15:0	2h RO	**Buffer Size (SZ):** Specifies the size of the transmit message buffer area in Dwords. If both transmit and receive buffers are supported, then the transmit buffer begins at ABAR[EM_LOC.OFST*4] and the receive buffer directly follows it. If both transmit and receive buffers are supported, both buffers are of the size indicated in the Buffer Size field. A value of 0 is invalid. Note that SATA controller only supports transmit buffer.

14.2.7 Enclosure Management Control (EM_CTL)—Offset 20h

Enclosure Management Control. This register is used to control and obtain status for the enclosure management interface. The register incluldes information on the attributes of the implementation, enclosure management messages supported, the status of the interface, whether any messages are pending, and is used to initiate sending messages. This register is not implemented if enclosure management is not supported (i.e. CAP.EMS = 0).

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 7010000h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27	0h RO	**Port Multiplier Support (ATTR_PM):** The HBA does not support enclosure management messages for devices attached via a Port Multiplier. Software should use the Serial ATA enclosure management bridge that is built into many Port Multipliers for enclosure services with these devices. For more information on Serial ATA enclosure management bridges, refer to the Serial ATA II: Extensions to Serial ATA 1.0a revision 1.2 specification.
26	1h RW/O	**Activity LED Hardware Driven (ATTR_ALHD):** If set to 1, the HBA drives the activity LED for the LED message type in hardware and does not utilize software settings for this LED. The HBA does not begin transmitting the hardware based activity signal until after software has written CTL.TM=1 after a reset condition.
25	1h RO	**Transmit Only (ATTR_XMT):** If set to 1, the HBA only supports transmitting messages and does not support receiving messages. If cleared to 0, the HBA supports transmitting and receiving messages.
24	1h RO	**Single Message Buffer (ATTR_SMB):** If set to 1, the HBA has one message buffer that is shared for messages to transmit and messages received. In this case, unsolicited receive messages are not supported and it is software's responsibility to manage access to this buffer. If cleared to 0, there are separate receive and transmit buffers such that unsolicited messages could be supported.
23:20	0h RO	Reserved.
19	0h RO	**SGPIO Enclosure Management Messages (SUPP_SGPIO):** If set to 1, the HBA supports the SGPIO register interface message type.
18	0h RO	**SES-2 Enclosure Management Messages (SUPP_SES2):** If set to 1, the HBA supports the SES-2 message type.
17	0h RO	**SAF-TE Enclosure Management Messages (SUPP_SAFTE):** If set to 1, the HBA supports the SAF-TE message type.

Bit Range	Default and Access	Field Name (ID): Description
16	1h RO	**LED Message Types (SUPP_LED):** If set to 1, the HBA supports the LED message type defined in LED Message Type.
15:10	0h RO	Reserved.
9	0h RW/1S	**Reset (RST):** When set to 1 by software, the HBA shall reset all enclosure management message logic and take all appropriate reset actions to ensure messages can be transmitted/received after the reset. After the HBA completes the reset operation, the HBA shall set the value to 0. A write of 0 by software to this field shall have no effect.
8	0h RW/1S	**Transmit Message (CTL_TM):** When set to 1 by software, the HBA shall transmit the message contained in the message buffer. When the message is completely sent, the HBA shall clear this bit to 0. A write of 0 to this bit by software shall have no effect. Software shall not change the contents of the message buffer while CTL.TM is set to 1.
7:1	0h RO	Reserved.
0	0h RO	**Message Received (STS_MR):** Message received is not supported.

14.2.8 HBA Capabilities Extended (GHC_CAP2)—Offset 24h

HBA Capabilities Extended. This register indicates basic capabilities of the HBA to driver software. The RWO bits in this register are only cleared upon PLTRST#. This register is not reset by FLR.

Access Method

Type: MEM Register (Size: 32 bits)

Device: 23
Function: 0

Default: 3Ch

Bit Range	Default and Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	1h RW/O	**DEVSLP Entrance from Slumber Only (DESO):** This bit specifies that the HBA shall only assert DEVSLP if the interface is in Slumber. 0 = The host may enter DEVSLP from any link state (active, Partial, or Slumber). 1 = The host shall ignore software directed entrance to DEVSLP by means of PxCMD.ICC bit unless PxSSTS.IPM = 6h.
4	1h RW/O	**Supports Aggressive DEVSLP Management (SADM):** 0 = Aggressive DEVSLP Management is not supported and software shall treat the PxDEVSLP.ADSE field as reserved. 1 = The host supports hardware assertion of the DEVSLP signal after the idle timeout expires.
3	1h RW/O	**Supports DEVSLP (SDS):** 0 = DEVSLP is not supported. 1 = Supports the DEVSLP feature.
2	1h RW/O	**Automatic Partial to Slumber Transitions (APST):** 0 = Automatic Partial to Slumber Transition is not supported. 1 = Supports Automatic Partial to Slumber Transitions.
1	0h RO	Reserved.
0	0h RO	**BIOS/OS Handoff (BOH):** Not supported.

14.2.9 Vendor Specific (VSP)—Offset A0h

Vendor Specific

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 48h

Bit Range	Default and Access	Field Name (ID): Description
31:7	0h RO	Reserved.
6	1h RO	**Software Feature Mask Supported (SFMS):** Set to 1 if the platform is enabled for premium storage features mask (SFM) as described in VS MMIO space at offset ABAR[RPID.(OFST*4)+4].
5	0h RO	**Premium Features Supported (PFS):** Set to 1 if the platform is enabled for premium storage features (PFB) as described in VS MMIO space at offset ABAR[RPID.OFST*4]. Set to 0 if the platform is not enabled for premium storage features.
4	0h RO	**Platform Type (PT):** Set to 1 if mobile platform. Clear (0) if desktop.
3	1h RO	**Supports RAID Platform ID Reporting (SRPIR):** If set to 1, then indicates that the RAID Platform ID is reported via ABAR + C0h. Set to 0 if this ID is not reported via MMIO space.
2:0	0h RO	Reserved.

14.2.10 Vendor Specific Capabilities Register (VS_CAP)—Offset A4h

Vendor Specific Capabilities Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 1002DEh

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:16	10h RW/O	**NVM Remapped Register Offset (NRMO):** Specifies the offset (in 128B unit) within ABAR as to where the PCIe NAND memory BAR register space is remapped. For example, NRMO=1 means ABAR + 128B. This allows the remapped offset to shift between ABAR + 0B, and ABAR + 512KK - 128B, with 128B step. The remapped offset into the AHCI memory space must not overlap with the memory space used for SATA. The remapped offset into the AHCI memory space and the remapped size must not exceed the allocated AHCI memory space of the integrated AHCI controller. Only valid when NRMBE = 1. The reset default of this field is 10h, this places the start of the PCIe NAND memory BAR register space at ABAR + 2K. This field is not reset by FLR.

Bit Range	Default and Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12:1	16Fh RW/O	**Memory Space Limit. (MSL):** This field specifies the size (in 128B unit) of the remapped memory space for the PCIe NAND device. It is a 0-based field. For example, MSL=1 means 256B. This allows the remapped size to shift between 128B and 512K with the step of 128B.Memory BAR offset from 0 to MSL of the PCIe NAND device are remapped under the integrated AHCI controller memory space.The remapped offset into the AHCI memory space and the value programmed in this field must not exceed the allocated AHCI memory space of the integrated AHCI controller. Only valid when NRMBE = 1. The reset default of this field is 16Fh which specifies the size of the remapped memory space as 34k.This field is not reset by FLR.
0	0h RW/O	**PCIe NAND Memory BAR Remapped Enable (NRMBE):** Set to 1 if a PCIe NAND device is present and remapping of its memory BAR register space is enabled. Cleared to 0 if there is no PCIe NAND device present or the remapping of its memory BAR register space is disabled. This bit is not reset by FLR.

14.2.11 RAID Platform ID (RPID)—Offset C0h

RAID Platform ID. This register is used by the Intel Matrix Storage Manager OROM to match the features supported by the OROM with the platform on which the OROM is executing. This prevents the use of an OROM designed for newer chipsets from being use on older chipsets as this could reduce up-sell potential.

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 311C02h

Bit Range	Default and Access	Field Name (ID): Description
31:16	31h RO	**Offset (OFST):** The offset of the Premium Feature Block (PFB) in DWords from the beginning of the ABAR. SFM follows directly after PFB.
15:0	1C02h RO	**RAID Platform ID (RPID):** Specifies the DID value that has been assigned to the platform. This is the same DID that is reported by the SATA controller when SATAGC.AIE is set to 1 except that the DID is always reported through this register, regardless if the programming of SATAGC.AIE.

14.2.12 Premium Feature Block (PFB)—Offset C4h

Access Method

Type: MEM Register
(Size: 16 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:5	0h RO	Reserved.
4	0h RO	**Reserved (Reserved):** Read value is the same as VSP.PFS.
3	0h RO	**Reserved (Reserved):** Read value is the same as VSP.PFS.
2	0h RO	**Reserved (Reserved):** Read value is the same as VSP.PFS.
1	0h RO	**Supports Email Alert (SEA):** Read value is the same as VSP.PFS. If set to 1, then this feature is supported as part of the premium feature set.
0	0h RO	**Supports OEM IOCTL (SOI):** Read value is the same as VSP.PFS. If set to 1, then this feature is supported as part of the premium feature set.

14.2.13 SW Feature Mask (SFM)—Offset C8h

SW Feature Mask. The following will be programmed by the BIOS when VS_CAP.SFMS == 1. The feature mask is used by SW to determine which non-premium features shall be supported by SW. These register bits are not reset by FLR since they are programmed by BIOS.

Access Method

Type: MEM Register (Size: 16 bits)

Device: 23
Function: 0

Default: 3Fh

Bit Range	Default and Access	Field Name (ID): Description
15:12	0h RO	Reserved.
11:10	0h RW/O	**OROM UI Normal Delay. (OROM_UI_Normal_Delay):** Values of these bits specify the delay of the OROM UI Splash Screen in a normal status. 00 = 2 secs (default and previous value); 01 = 4 secs; 10 = 6 secs; 11 = 8 secs. If bit 5 == 0, then these values are disregarded.
9	0h RW/O	**Smart Response Technology. (Smart_Response_Technology):** If set to '1', then Smart Response Technology is enabled. If cleared to '0', the feature is disabled.
8	0h RW/O	**RRT Only on ESATA (IRRT_Only_on_ESATA):** If set to 1, then only RRT volumes can span internal and external SATA ports (e.g. eSATA). If cleared to 0, then any RAID volume can span internal and external SATA ports (e.g. eSATA).
7	0h RW/O	**LED Locate (LED_Locate):** If set to 1, then LED/SGPIO hardware is attached and the ping to locate feature is enabled in the OS.
6	0h RW/O	**HDDUNLOCK (HDDUNLOCK):** If set to 1, then HDD password unlock is enabled in the OS.
5	1h RW/O	**OROM UI and BANNER (OROM_UI_and_BANNER):** If set to 1, then the OROM UI is displayed. When cleared to 0, the OROM UI and BANNER are not displayed if all disks and volumes have a normal status.
4	1h RW/O	**RRT (IRRT):** If set to 1, then Rapid Recovery Technology is enabled.

Bit Range	Default and Access	Field Name (ID): Description
3	1h RW/O	**R5 (R5):** If set to 1, then RAID5 is enabled
2	1h RW/O	**R10 (R10):** If set to 1, then RAID10 is enabled
1	1h RW/O	**R1 (R1):** If set to 1, then RAID1 is enabled
0	1h RW/O	**R0 (R0):** If set to 1, then RAID0 is enabled

14.2.14 Port 0 Command List Base Address (P0CLB)—Offset 100h

Port 0 Command List Base Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RW	**Command List Base Address (CLB):** Indicates the 32-bit base for the command list for this port. This base is used when fetching commands to execute. This address must be 1K aligned as indicated by bits 31:10 being read/write. Note that these bits are not reset on a HBA reset.
9:0	0h RO	Reserved.

14.2.15 Port 0 Command List Base Address Upper 32-bits (P0CLBU)—Offset 104h

Port 0 Command List Base Address Upper 32-bits

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Command List Base Address Upper (CLBU):** Indicates the upper 32-bits for the command list base address for this port. This base is used when fetching commands to execute. Note that these bits are not reset on a HBA reset.

14.2.16 Port 0 FIS Base Address (P0FB)—Offset 108h

Port 0 FIS Base Address

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RW	**FIS Base Address (FB):** Indicates the 32-bit base for received FISes. This address must be 256-byte aligned as indicated by bits 31:08 being read/write. When FIS-based switching is in use, this structure is 4KB in length and the address shall be 4KB aligned. Note that these bits are not reset on a HBA reset.
7:0	0h RO	Reserved.

14.2.17 Port 0 FIS Base Address Upper 32-bits (P0FBU)—Offset 10Ch

Port 0 FIS Base Address Upper 32-bits

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**FIS Base Address Upper (FBU):** Indicates the upper 32-bits for the received FIS base for this port. Note that these bits are not reset on a HBA reset.

14.2.18 Port 0 Interrupt Status (P0IS)—Offset 110h

Port 0 Interrupt Status

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**Cold Presence Detect Status (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW/1C	**Task File Error Status (TFES):** This bit is set whenever the status register is updated by the device and the error bit (bit 0 of the Status field in the received FIS) is set.
29	0h RW/1C	**Host Bus Fatal Error Status (HBFS):** Indicates that the HBA encountered a host bus error that it cannot recover from, such as a bad software pointer. In PCI, such an indication would be a target or master abort.
28	0h RW/1C	**Host Bus Data Error Status (HBDS):** Indicates that the HBA encountered a data error (uncorrectable ECC / parity) when reading from or writing to system memory.
27	0h RW/1C	**Interface Fatal Error Status (IFS):** Indicates that the HBA encountered an error on the SATA interface which caused the transfer to stop.
26	0h RW/1C	**Interface Non-fatal Error Status (INFS):** Indicates that the HBA encountered an error on the SATA interface but was able to continue operation.
25	0h RO	Reserved.
24	0h RW/1C	**Overflow Status (OFS):** Indicates that the HBA received more bytes from a device than was specified in the PRD table for the command.
23	0h RW/1C	**Incorrect Port Multiplier Status (IPMS):** Indicates that the HBA received a FIS from a device whose port multiplier field did not match what was expected. The IPMS bit may be set during emuneration process. It is recommended that IPMS only be used after enumeration is complete on the Port Multiplier.
22	0h RO	**PhyRdy Change Status (PRCS):** When set to one indicates the internal PhyRdy signal changed state. This bit reflects the state of PxSERR.DIAG.N. This bit is RO and is only cleared when PxSERR.DIAG.N is cleared.
21:8	0h RO	Reserved.
7	0h RW/1C	**Device Mechanical Presence Status (DMPS):** When set, indicates that a platform mechanical presence switch has been opened or closed, which may lead to a change in the connection state of the device. This bit is only valid in systems that support mechanical presence switch (CAP.SMPS and PxCMD.MPSP are set).
6	0h RO	**Port Connect Change Status (PCS):** This bit reflects the state of PxSERR.DIAG.X. This bit is only cleared when PxSERR.DIAG.X is cleared. 1 = Change in Current Connect Status. 0 = No change in Current Connect Status.
5	0h RW/1C	**Descriptor Processed (DPS):** A PRD with the I. bit set has transferred all of its data.
4	0h RO	**Unknown FIS Interrupt (UFS):** When set to 1 indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by software clearing the PxSERR.DIAG.F bit to 0. Note that this bit does not directly reflect the PxSERR.DIAG.F bit. PxSERR.DIAG.F is set immediately when an unknown FIS is detected, whereas this bit is set when the FIS is posted to memory. Software should wait to act on an unknown FIS until this bit is set to 1 or the two bits may become out of sync.
3	0h RW/1C	**Set Device Bits Interrupt (SDBS):** A Set Device Bits FIS has been received with the I. bit set and has been copied into system memory.
2	0h RW/1C	**DMA Setup FIS Interrupt (DSS):** A DMA Setup FIS has been received with the I. bit set and has been copied into system memory.
1	0h RW/1C	**PIO Setup FIS Interrupt (PSS):** A PIO Setup FIS has been received with the I. bit set, it has been copied into system memory, and the data related to that FIS has been transferred. This bit shall be set even if the data transfer resulted in an error.
0	0h RW/1C	**Device to Host Register FIS Interrupt (DHRS):** A D2H register FIS has been received with the I. bit set, and has been copied into system memory.

14.2.19 Port 0 Interrupt Enable (P0IE)—Offset 114h

Port 0 Interrupt Enable

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**Cold Presence Detect Enable (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW	**Task File Error Enable (TFEE):** When set, GHC.IE is set, and P0S.TFES is set, the HBA shall generate an interrupt.
29	0h RW	**Host Bus Fatal Error Enable (HBFE):** When set, GHC.IE is set, and P0IS.HBFS is set, the HBA shall generate an interrupt.
28	0h RW	**Host Bus Data Error Enable (HBDE):** When set, GHC.IE is set, and P0IS.HBDS is set, the HBA shall generate an interrupt.
27	0h RW	**Interface Fatal Error Enable (IFE):** When set, GHC.IE is set, and P0IS.IFS is set, the HBA shall generate an interrupt.
26	0h RW	**Interface Non-fatal Error Enable (INFE):** When set, GHC.IE is set, and P0IS.INFS is set, the HBA shall generate an interrupt.
25	0h RO	Reserved.
24	0h RW	**Overflow Enable (OFE):** When set, and GHC.IE and P0IS.OFS are set, the HBA shall generate an interupt.
23	0h RW	**Incorrect Port Multiplier Enable (IPME):** When set, and GHC.IE and P0IS.IPMS are set, the HBA shall generate an interupt. BIOS is required to program this field to '0'. The same applies to AHCI driver.
22	0h RW	**PhyRdy Change Interrupt Enable (PRCE):** When set, and GHC.IE is set, and PxIS.PRCS is set, the HBA shall generate an interrupt.
21:8	0h RO	Reserved.
7	0h RW	**Device Mechanical Enable (DMPE):** When set, and P0IS.DMPS is set, the HBA shall generate an interrupt.
6	0h RW	**Port Change Interrupt Enable (PCE):** When set, GHC.IE is set, and P0IS.PCS is set, the HBA shall generate an interrupt.
5	0h RW	**Descriptor Processed Interrupt Enable (DPE):** When set, GHC.IE is set, and P0IS.DPS is set, the HBA shall generate an interrupt.
4	0h RW	**Unknown FIS Interrupt Enable (UFE):** When set, GHC.IE is set, and PxIS.UFS is set to 1, the HBA shall generate an interrupt.
3	0h RW	**Set Device Bits FIS Interrupt Enable (SDBE):** When set, GHC.IE is set, and P0IS.SDBS is set, the HBA shall generate an interrupt.
2	0h RW	**DMA Setup FIS Interrupt Enable (DSE):** When set, GHC.IE is set, and P0IS.DSS is set, the HBA shall generate an interrupt.
1	0h RW	**PIO Setup FIS Interrupt Enable (PSE):** When set, GHC.IE is set, and P0IS.PSS is set, the HBA shall generate an interrupt.
0	0h RW	**Device to Host Register FIS Interrupt Enable (DHRE):** When set, GHC.IE is set, and P0IS.DHRS is set, the HBA shall generate an interrupt.

14.2.20 Port 0 Command (P0CMD)—Offset 118h

Port 0 Command

Access Method

Type: MEM Register
(Size: 32 bits)

Device: 23
Function: 0

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RW	**Interface Communication Control (ICC):** This is a four bit field which can be used to control reset and power states of the interface. Writes to this field will cause actions on the interface, either as primitives or an OOB sequence, and the resulting status of the interface will be reported in the PxSSTS register. Value Definition Fh–9h Reserved 8h DEVSLP: This will cause the PCH to assert the DEVSLP signal associated with the port. The PCH will ignore the DEVSLP idle timeout value that is specified by PxDEVSLP.DITO. Software will only request DEVSLP when the interface is in an idle state (that is, PxCI is cleared to 0h and PxSACT is cleared to 0h). If the interface is not idle at the time this register is written, then the PCH will take no action and the interface will remain in its current state. If PxCAP2.DESO is set to '1' and PxSSTS.IPM is not set to '6h', then the host will take no action on the interface and will remain in its current state. Additionally, the HBA shall not assert the DEVSLP signal until PHYRDY has been achieved (after a previous de-assertion). 7h Reserved 6h Slumber: This will cause the PCH to request a transition of the interface to the slumber state. The SATA device may reject the request and the interface will remain in its current state. 5h–3h Reserved 2h Partial: This will cause the PCH to request a transition of the interface to the partial state. The SATA device may reject the request and the interface will remain in its current state. 1h Active: This will cause the PCH to request a transition of the interface into the active state. If the requested transition is from the DEVSLP state, then the host controller shall wait until PxDEVSLP.DMAT has expired before deasserting the DEVSLP Signal. 0h No-Op/Idle: When software reads this value, it indicates the PCH is not in the process of changing the interface state or sending a device reset, and a new link command may be issued. When system software writes a non-reserved value other than No-Op (0h), the HBA shall perform the action and update this field back to Idle (0h). If software writes to this field to change the state to a state the link is already in (i.e. interface is in the active state and a request is made to go to the active state), the HBA shall take no action and return this field to Idle. If the interface is in a low power state and the software wants to transition to a different low power state, software must first bring the link to active and then initiate the transition to the desired low power state (with the exception of DEVSLP). The transition to DEVSLP may occur from any other state if CAP2.DESO is cleared to '0'. If CAP2.DESO is set to '1', then DEVSLP may only be transitioned to if the link is in Slumber.
27	0h RW	**Aggressive Slumber Partial (ASP):** When set to 1, and the ALPE bit is set, the HBA shall aggressively enter the Slumber state when it clears a bit in the PxCI or PxSACT register and the register values are then PxCI = 0h and PxSACT = 0h. When cleared, and the ALPE bit is set, the HBA will aggressively enter the Partial state when it clears a bit in the PxCI or PxSACT register and the register values are then PxCI = 0h and PxSACT = 0h. If CAP.SALP is cleard to 0., software shall treat this bit as reserved.
26	0h RW	**Aggressive Link Power Management Enable (ALPE):** When set, the HBA will aggressively enter a lower link power state (Partial or Slumber) based upon the setting of the ASP bit. Software shall only set this bit to 1 if CAP.SALP is set to 1. If CAP.SALP is cleared to 0, software shall treat this bit as reserved. BIOS is recommeded to program this field to 1.
25	0h RW	**Drive LED on ATAPI Enable (DLAE):** When set, the HBA will drive the LED pin active for commands regardless of the state of PxCMD.ATAPI. When cleared, the HBA will only drive the LED pin active for commands if PxCMD.ATAPI is set to 0.. This bit is set by software
24	0h RW	**Device is ATAPI (ATAPI):** When set, the connected device is an ATAPI device. This bit is used by the HBA to control whether or not to generate the desktop LED when commands are active.
23	0h RW	**Automatic Partial to Slumber Transitions Enabled (APSTE):** 0 = This port will not perform Automatic Partial to Slumber Transitions. 1 = The HBA may perform Automatic Partial to Slumber Transitions. Note: Software shall only set this bit to '1' if CAP2.APST is set to '1'; if CAP2.APST is cleared to '0' software shall treat this bit as reserved.
22	0h RO	**FIS-based Switching Capable Port (FBSCP):** The SATA controller does not support FIS-Based Switching.

Bit Range	Default and Access	Field Name (ID): Description
21	0h RW/O	**External SATA Port (ESP):** 0 = This port supports internal SATA devices only. 1 = This port will be used with an external SATA device and hot-plug is supported. When set, CAP.SXS must also be set. This bit is not reset by Function Level Reset.
20	0h RO	**Cold Presence Detection (CPD):** The SATA controller does not support cold presence detect.
19	0h RW/O	**Mechanical Presence Switch Attached to Port (MPSP):** If set to 1, the platform supports a mechanical presence switch attached to this port. If cleared to 0, the platform does not support a mechanical presence switch attached to this port.
18	0h RW/O	**Hot Plug Capable Port (HPCP):** This indicates whether the this port is connected to a device which can be hot plugged. SATA by definition is hot-pluggable, but not all platforms are constructed to allow the device to be removed (it may be screwed into the chassis, for example). This bit can be used by system software to indicate a feature such as eject device to the end-user. 0 = Port is not capable of hot-plug. 1 = Port is hot-plug capable. The HBA takes no action on the state of this bit – it is for system software only. For example, if this bit is cleared, and a hot plug event occurs, the HBA shall still treat it as a proper hot plug event. Note: This bit is not reset on a HBA reset. This field is not reset by FLR.
17	0h RO	**Port Multiplier Attached (PMA):** When set, a Port Multiplier is attached to the HBA for this port. When cleared, a Port Multiplier is not attached to the HBA for this port. This bit is a read only 0. when CAP.PMS = 0., and read/write when CAP.PMS = 1.. Note that this bit is set by software; hardware does not auto-detect that a Port Multiplier is attached.
16	0h RO	Reserved.
15	0h RO	**Command List Running (CR):** When this bit is set it indicates that the command list DMA engine for the port is running.
14	0h RO	**FIS Receive Running (FR):** When this bit is set it indicates that the FIS Receive DMA engine for the port is running. Note to software: When FR bit stays set, please read the PxIS.PCS and PxSERR.DET.X to service the PCS interrupt accordingly if any
13	0h RO	**Mechanical Presence Switch State (MPSS):** The MPSS bit reports the state of a mechanical presence switch attached to this port. If CAP.SMPS is set to 1 and the mechanical presence switch is closed then this bit is cleared to 0. If CAP.SMPS is set to 1 and the mechanical presence switch is open then this bit is set to 1. If CAP.SMPS is set to 0 then this bit is cleared to 0. Software should only use this bit if both CAP.SMPS and PxCMD.MPSP are set to 1.
12:8	0h RO	**Current Command Slot (CCS):** Indicates the current command slot the HBA is processing. This field is valid when the PxCMD.ST bit is set, and is constantly updated by the HBA. This field can be updated as soon as the HBA recognizes an active command slot, or at some point soon after when it begins processing the command. When PxCMD.ST transitions from a 1 to a 0, the HBA will reset this field to 0. After PxCMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is PxCMD.CCS + 1. For example, after the HBA has issued its first command, if PxCMD.CCS = 0h and PxCI is set to 3h, the next command that will be issued is from command slot 1.
7	0h RO	Reserved.
6	0h RO	**PHYSLP Present (PSP):** If set to '1', the platform supports PHYSLP on this port. If cleared to '0', the platform does not support PHYSLP on this port. This bit may only be set to '1' if CAP2.SPS is set to '1'.
5	0h RO	Reserved.
4	0h RW	**FIS Receive Enable (FRE):** When set, the HBA may post received FISes into the FIS receive area pointed to by PxFB and PxFBU. When cleared, received FISes are not accepted by the HBA, except for the first D2H register FIS after the initialization sequence.
3	0h RW/1S	**Command List Override (CLO):** Setting this bit to 1 causes PxTFD.STS.BSY and PxTFD.STS.DRQ to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The HBA sets this bit to 0 when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to 0. A write to this register with a value of 0 shall have no effect.

Bit Range	Default and Access	Field Name (ID): Description
2	1h RO	**Power On Device (POD):** The SATA controller does not support cold presence detect.
1	0h RW	**Spin-Up Device (SUD):** This bit is read/write and default to 0 for HBAs that support staggered spin-up via CAP.SSS. This bit is read only 1 for HBAs that do not support staggered spin-up. 0 = No Action 1 = On an edge detect from 0 to 1, the PCH shall start a COMRESET initialization sequence to the device. Clearing this bit causes no action on the interface. Clearing this bit to 0 does not cause any OOB signal to be sent on the interface. When this bit is cleared to 0 and PxSCTL.DET = 0h, the HBA will enter listen mode.
0	0h RW	**Start (ST):** When set, the HBA may process the command list. When cleared, the HBA may not process the command list. Whenever this bit is changed from a 0 to a 1, the HBA starts processing the command list at entry 0. Whenever this bit is changed from a 1 ot a 0, the PxCI and PxSACT register is cleared by the HBA upon the HBA putting the controller into an idle state. PxTFD shall be updated also.

14.2.21 Port 0 Task File Data (P0TFD)—Offset 120h

Port 0 Task File Data

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 9h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	0h RO	**Error (ERR):** Contains the latest copy of the task file error register.
7	0h RO	**Status Busy (STS_BSY):** Status - Indicates the interface is busy.
6:4	0h RO	Reserved.
3	1h RO	**Status Drq (STS_DRQ):** Status - Indicates a data transfer is requested.
2:1	0h RO	Reserved.
0	1h RO	**Status Err (STS_ERR):** Status - Indicates an error during the transfer.

14.2.22 Port 0 Signature (P0SIG)—Offset 124h

Port 0 Signature

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: FFFFFFFFh

Bit Range	Default and Access	Field Name (ID): Description
31:0	FFFFFFFFh RO	**Signature (SIG):** Contains the signature received from a device on the first D2H Register FIS. The bit order is as follows: Bit Field 31:24 LBA High Register 23:16 LBA Mid Register 15:8 LBA Low Register 7:0 Sector Count Register

14.2.23 Port 0 Serial ATA Status (P0SSTS)—Offset 128h

Port 0 Serial ATA Status

Access Method

Type: MEM Register (Size: 32 bits)

Device: 23

Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11:8	0h RO	**Interface Power Management (IPM):** Indicates the current interface state. Value Description 0h Device not present or communication not established 1h Interface in active state 2h Interface in PARTIAL power management state 6h Interface in SLUMBER power management state 8h DEVSLP asserted All other values reserved. This field reflects the interface power management state for both device and host initiated power management. Note: If an Automatic Partial to Slumber Transition occurs, PxSSTS.IPM shall reflect that the host has entered Slumber (PxSSTS.IPM = '6h').
7:4	0h RO	**Current Interface Speed (SPD):** Indicates the negotiated interface communication speed. Value Description 0h Device not present or communication not established 1h Generation 1 communication rate negotiated 2h Generation 2 communication rate negotiated 3h Generation 3 communication rate negotiated All other values reserved.
3:0	0h RO	**Device Detection (DET):** Indicates the interface device detection and Phy state. Value Description 0h No device detected and Phy communication not established 1h Device presence detected but Phy communication not established 3h Device presence detected and Phy communication established 4h Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode All other values reserved. Note: While the true reset default value of this register is 0h, the value read from this register depends on drive presence and the point in time within the initialization process when the register is read. Note: The means by which the implementation determines device presence may be vendor specific. However, device presence shall always be indicated anytime a COMINIT signal is received.

14.2.24 Port 0 Serial ATA Control (P0SCTL)—Offset 12Ch

Port 0 Serial ATA Control

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:16	0h RW	**Port Multiplier Port (PMP):** This field is not used by AHCI.
15:12	0h RW	**Select Power Management (SPM):** This field is not used by AHCI.
11:8	0h RW	**Interface Power Management Transitions Allowed (IPM):** Indicates which power states the HBA is allowed to transition to. If an interface power management state is not allowed via this register field, the HBA will not initiate that state and the HBA will PMNAKp any request from the device to enter that state. Value Description 0h No interface restrictions 1h Transitions to the PARTIAL state disabled 2h Transitions to the SLUMBER state disabled 3h Transitions to both PARTIAL and SLUMBER states disabled 4h Transitions to the DEVSLP power management state are disabled 5h Transitions to the Partial and DEVSLP power management states are disabled 6h Transitions to the Slumber and DEVSLP power management states are disabled 7h Transitions to the Partial, Slumber and DEVSLP power management states are disabled All other values reserved.
7:4	0h RW	**Speed Allowed (SPD):** Indicates the highest allowable speed of the interface. Value Description 0h No speed negotiation restrictions 1h Limit speed negotiation to Generation 1 communication rate 2h Limit speed negotiation to a rate not greater than Generation 2 communication rate 3h Limit speed negotiation to a rate not greater than Generation 3 communication rate All other values reserved Note: If software changes SPD after port has been enabled, software is required to perform a port reset via DET=1h.
3:0	0h RW	**Device Detection Initialization (DET):** Controls the HBA.s device detection and interface initialization. Value Description 0h No device detection or initialization action requested. 1h Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized. While this field is 1h, COMRESET is continuously transmitted on the interface. Software should leave the DET field set to 1h for a minimum of 1 millisecond to ensure that a COMRESET is sent on the interface. 4h Disable the Serial ATA interface and put Phy in offline mode. All other values reserved. This field may only be changed when PxCMD.ST is '0'. Changing this field while the HBA is running results in undefined behavior. When PxCMD.ST is set to '1', this field should have a value of 0h. Note: It is permissible to implement any of the Serial ATA defined behaviors for transmission of COMRESET when PxSCTL.DET = 1h.

14.2.25 Port 0 Serial ATA Error (P0SERR)—Offset 130h

Port 0 Serial ATA Error

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/1C	**Diagnostics (DIAG):** Contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. Bit Field 31:27 Reserved 26 Exchanged (X): When set to one this bit indicates that a change in device presence has been detected since the last time this bit was cleared. The means by which the implementation determines that the device presence has changed is vendor specific. This bit shall always be set to one anytime a COMINIT signal is received. This bit is reflected in the P0IS.PCS bit. 25 Unrecognized FIS Type (F): Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized/known. 24 Transport state transition error (T): Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared. 23 Link Sequence Error (S): Indicates that one or more Link state machine error conditions were encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition. 22 Handshake Error (H): Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame. 21 CRC Error (C): Indicates that one or more CRC errors occurred with the Link Layer. 20 Disparity Error (D): This field is not used by AHCI. 19 10B to 8B Decode Error (B): Indicates that one or more 10B to 8B decoding errors occurred. 18 Comm Wake (W): Indicates that a Comm Wake signal was detected by the Phy. 17 Phy Internal Error (I): Indicates that the Phy detected some internal error. 16 PhyRdy Change (N): When set to 1 this bit indicates that the internal PhyRdy signal changed state since the last time this bit was cleared. The state of this bit is reflected in the PxIS.PRCS interrupt status bit and an interrupt will be generated if enabled.
15:0	0h RW/1C	**Error (ERR):** The ERR field contains error information for use by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer. Bit Field 15:12 Reserved 11 Internal Error (E): The SATA controller failed due to a master or target abort when attempting to access system memory. 10 Protocol Error (P): A violation of the Serial ATA protocol was detected. 9 Persistent Communication or Data Integrity Error (C): A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes. 8 Transient Data Integrity Error (T): A data integrity error occurred that was not recovered by the interface. 7:2 Reserved 1 Recovered Communications Error (M): Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers. 0 Recovered Data Integrity Error (I): A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

14.2.26 Port 0 Serial ATA Active (P0SACT)—Offset 134h

Port 0 Serial ATA Active

Access Method

Type: MEM Register (Size: 32 bits)

Device: 23

Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/1S	**Device Status (DS):** System software sets this bit for native command queuing commands prior to setting the PxCI.CI bit in the same command slot entry. This field is cleared via the Set Device Bits FIS. This field is also cleared when PxCMD.ST is cleared by software. Note that this field is not cleared by COMRESET or SRST.

14.2.27 Port 0 Command Issue (P0CI)—Offset 138h

Port 0 Commands Issued

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Commands Issued (CI):** This field is set by software to indicate to the HBA that a command has been built in system memory for a command slot and may be sent to the device. When the HBA receives a FIS which clears the BSY, ERR, and DRQ bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to '1' by software when PxCMD.ST is set to '1'. This field is also cleared when PxCMD.ST is written from a ‘1’ to a ‘0’ by software.

14.2.28 Port 0 Device Sleep (P0DEVSLP)—Offset 144h

Port 0 Device Sleep

Access Method

Type: MEM Register (Size: 32 bits)
Device: 23
Function: 0

Default: 1E022852h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:25	Fh RW/O	**DITO Multiplier (DM):** DITO multiplier that the HBA applies to the specified DITO value, effectively extending the range of DITO from 1ms to 16368ms. A value of 0h indicates a multiplier of 1. A maximum multiplier of 16 may be applied. The HBA computes the total idle timeout as a product of DM and DITO (i.e. DITO actual = DITO * (DM+1)). Note: These bits are not reset by controller reset.
24:15	4h RW	**DEVSLP Idle Timeout (DITO):** This field specifies the amount of the time (in approximate 1ms granularity) that the HBA shall wait before driving the DEVSLP signal. Hardware reloads its port specific DEVSLP timer with this value each time the port transitions out of DEVSLP state. For example: from DEVSLP to active or PxDEVSLP.ADSE transitions from 0 to a 1. If CAP2.SDS or CAP2.SADM or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0 and PxDEVSLP.ADSE is cleared to 0. Note: These bits are not reset by controller reset.
14:10	Ah RW	**DEVSLP Minimum Assertion Time (MDAT):** This field specifies the minimum amount of time (in 1ms granulatity) that the HBA must assert the DEVSLP signal before it may be de-asserted. The norminal value is 10ms and the minimum is 1ms depending on device identification information. If CAP2.SDS is cleared to 0 or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0, PxDEVSLP.ADSE is cleared to 0, and prior to setting PxCMD.ICC to 8h. Note: These bits are not reset by controller reset.
9:2	14h RW	**DEVSLP Exit Timeout (DETO):** This field specifies the maximum duration (in approximate 1ms granularity) from DEVSLP de-assertion until the device is ready to accept OOB. The norminal value is 20ms while the max value is 255ms depending on device identification information. If CAP2.SDS is cleared to 0 or PxDEVSLP.DSP is cleared to 0 then these bits are read-only 0h and software shall treat these bits as reserved. Software shall only set this value when PxCMD.ST is cleared to 0, PxDEVSLP.ADSE is cleared to 0, and prior to setting PxCMD.ICC to 8h. Note: These bits are not reset by controller reset.
1	1h RW/O	**DEVSLP Present (DSP):** If set to '1', the platform supports DEVSLP on this port. If cleared to '0', the platform does not support DEVSLP on this port. This bit may only be set to '1' if CAP2.SDS is set to '1'. DSP is mutually exclusive with the PxCMD.HPCP bit and PxCMD.ESP bit. BIOS is required to program this field to ‘1’ if the system supports the DEVSLP feature. Note: These bits are not reset by controller reset.
0	0h RW	**Aggressive DEVSLP Enable (ADSE):** This bit is read/write for HBAs that support aggressive DEVSLP management (CAP2. SADM = '1'). When this bit is set to '1', the HBA shall assert the DEVSLP signal after the port has been idle (PxCI = 0h and PxSACT = 0h) for the amount of time specified by the PxDEVSLP.DITO register and the interface is in Slumber (PxSSTS.IPM = 6h). When this bit is cleared to '0', the HBA does not enter DEVSLP unless software directed via PxCMD.ICC. This bit shall only be set to '1' if PxDEVSLP.DSP is set to '1'. If this bit is set to '1' and software clears the bit to '0', then the HBA shall de-assert the DEVSLP signal if asserted. Note that these bits are not reset on a HBA reset. BIOS is recommended to program this field to '1' if the platform support the DEVSLP feature. If CAP2.SDS is cleared to '0' or CAP2.SADM is cleared to '0', or if PxDEVSLP.DSP is cleared to '0' then these bits are read-only 0h and software shall treat these bits as reserved.

14.2.29 Port 1 Command List Base Address (P1CLB)—Offset 180h

Same bit definition as P0CLB.

14.2.30 Port 1 Command List Base Address Upper 32-bits (P1CLBU)—Offset 184h

Same bit definition as P0CLBU.

14.2.31 Port 1 FIS Base Address (P1FB)—Offset 188h

Same bit definition as P0FB.

14.2.32 Port 1 FIS Base Address Upper 32-bits (P1FBU)—Offset 18Ch

Same bit definition as P0FBU.

14.2.33 Port 1 Interrupt Status (P1IS)—Offset 190h

Same bit definition as P0IS.

14.2.34 Port 1 Interrupt Enable (P1IE)—Offset 194h

Same bit definition as P0IE.

14.2.35 Port 1 Command (P1CMD)—Offset 198h

Same bit definition as P0CMD.

14.2.36 Port 1 Task File Data (P1TFD)—Offset 1A0h

Same bit definition as P0TFD.

14.2.37 Port 1 Signature (P1SIG)—Offset 1A4h

Same bit definition as P0SIG.

14.2.38 Port 1 Serial ATA Status (P1SSTS)—Offset 1A8h

Same bit definition as P0SSTS.

14.2.39 Port 1 Serial ATA Control (P1SCTL)—Offset 1ACh

Same bit definition as P0SCTL.

14.2.40 Port 1 Serial ATA Error (P1SERR)—Offset 1B0h

Same bit definition as P0SERR.

14.2.41 Port 1 Serial ATA Active (P1SACT)—Offset 1B4h

Same bit definition as P0SACT.

14.2.42 Port 1 Command Issue (P1CI)—Offset 1B8h

Same bit definition as P0CI.

14.2.43 Port 1 Device Sleep (P1DEVSLP)—Offset 1C4h

Same bit definition as P0DEVSLP.

14.3 SATA AIDP Registers Summary

SATA AHCI IO INDEX + DATA Registers

Table 14-2. Summary of SATA AIDP Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
10h	13h	AHCI Index Register (INDEX)—Offset 10h	0h
14h	17h	AHCI Data Register (DATA)—Offset 14h	0h

14.3.1 AHCI Index Register (INDEX)—Offset 10h

This registers are only available if CC.SCC is not 01h to index into all memory registers defined in Memory Registers and the message buffer used for enclosure management. If CC.SCC is 01h, these AHCI Index Data Pair registers are not accessible and SINDEX/SDATA register pair shall be used to index into a subset of the memory registers.(See Memory Registers for more information on which registers could be indexed).

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18:2	0h RW	**Index (INDEX):** This Index register is used to select the Dword offset of the Memory Mapped AHCI register to be accessed. A Dword, Word or Byte access is specified by the active byte enables of the I/O access to the Data register.
1:0	0h RO	Reserved.

14.3.2 AHCI Data Register (DATA)—Offset 14h

This registers are index into all memory registers defined in Memory Registers and the message buffer used for enclosure management.

Access Method

Type: IO Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Data (DATA):** This Data register is a window through which data is read or written to the memory mapped register pointed to by the Index register. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the default value is the same as the default value of the register pointed to by Index.

14.4 SATA MXPBA Registers Summary

SATA MSI-X Pending Bit Array Registers

Table 14-3. Summary of SATA MXPBA Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	MSI-X Pending Bit Array QW 0 (MXPQW0_DW0)—Offset 0h	0h

14.4.1 MSI-X Pending Bit Array QW 0 (MXPQW0_DW0)—Offset 0h

MSI-X Pending Bit Array QW 0

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RO/V	**MSI-X vector Pending (MXVP):** For each Pending Bit that is set, the function has a pending message for the associated MSI-X Table entry. Pending bits that have no associated MSI-X Table entry are reserved. After reset, the state of reserved Pending bits must be 0. Software should never write, and should only read Pending Bits. If software writes to Pending Bits, the result is undefined. Each Pending Bit's state after reset is 0 (no message pending).

14.5 SATA MXTBA Registers Summary

SATA MSI-X Table Entry Registers

Table 14-4. Summary of SATA MXTBA Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	MSI-X Table Entries 0 Message Lower Address (MXTE0MLA)—Offset 0h	0h
4h	7h	MSI-X Table Entries 0 Message Upper Address (MXTE0MUA)—Offset 4h	0h
8h	Bh	MSI-X Table Entries 0 Message Data (MXTE0MD)—Offset 8h	0h
Ch	Fh	MSI-X Table Entries 0 Vector Control (MXTE0VC)—Offset Ch	1h
10h	13h	MSI-X Table Entries 1 Message Lower Address (MXTE1MLA)—Offset 10h	0h
14h	17h	MSI-X Table Entries 1 Message Upper Address (MXTE1MUA)—Offset 14h	0h
18h	1Bh	MSI-X Table Entries 1 Message Data (MXTE1MD)—Offset 18h	0h
1Ch	1Fh	MSI-X Table Entries 1 Vector Control (MXTE1VC)—Offset 1Ch	1h
20h	23h	MSI-X Table Entries 2 Message Lower Address (MXTE2MLA)—Offset 20h	0h
24h	27h	MSI-X Table Entries 2 Message Upper Address (MXTE2MUA)—Offset 24h	0h
28h	2Bh	MSI-X Table Entries 2 Message Data (MXTE2MD)—Offset 28h	0h
2Ch	2Fh	MSI-X Table Entries 2 Vector Control (MXTE2VC)—Offset 2Ch	1h
30h	33h	MSI-X Table Entries 3 Message Lower Address (MXTE3MLA)—Offset 30h	0h
34h	37h	MSI-X Table Entries 3 Message Upper Address (MXTE3MUA)—Offset 34h	0h
38h	3Bh	MSI-X Table Entries 3 Message Data (MXTE3MD)—Offset 38h	0h
3Ch	3Fh	MSI-X Table Entries 3 Vector Control (MXTE3VC)—Offset 3Ch	1h
40h	43h	MSI-X Table Entries 4 Message Lower Address (MXTE4MLA)—Offset 40h	0h
44h	47h	MSI-X Table Entries 4 Message Upper Address (MXTE4MUA)—Offset 44h	0h
48h	4Bh	MSI-X Table Entries 4 Message Data (MXTE4MD)—Offset 48h	0h
4Ch	4Fh	MSI-X Table Entries 4 Vector Control (MXTE4VC)—Offset 4Ch	1h
50h	53h	MSI-X Table Entries 5 Message Lower Address (MXTE5MLA)—Offset 50h	0h
54h	57h	MSI-X Table Entries 5 Message Upper Address (MXTE5MUA)—Offset 54h	0h
58h	5Bh	MSI-X Table Entries 5 Message Data (MXTE5MD)—Offset 58h	0h
5Ch	5Fh	MSI-X Table Entries 5 Vector Control (MXTE5VC)—Offset 5Ch	1h
60h	63h	MSI-X Table Entries 6 Message Lower Address (MXTE6MLA)—Offset 60h	0h
64h	67h	MSI-X Table Entries 6 Message Upper Address (MXTE6MUA)—Offset 64h	0h
68h	6Bh	MSI-X Table Entries 6 Message Data (MXTE6MD)—Offset 68h	0h
6Ch	6Fh	MSI-X Table Entries 6 Vector Control (MXTE6VC)—Offset 6Ch	1h
70h	73h	MSI-X Table Entries 7 Message Lower Address (MXTE7MLA)—Offset 70h	0h
74h	77h	MSI-X Table Entries 7 Message Upper Address (MXTE7MUA)—Offset 74h	0h
78h	7Bh	MSI-X Table Entries 7 Message Data (MXTE7MD)—Offset 78h	0h
7Ch	7Fh	MSI-X Table Entries 7 Vector Control (MXTE7VC)—Offset 7Ch	1h

14.5.1 MSI-X Table Entries 0 Message Lower Address (MXTE0MLA)—Offset 0h

MSI-X Table Entries 0 Message Lower Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI-X message lower address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	0h RO	Reserved.

14.5.2 MSI-X Table Entries 0 Message Upper Address (MXTE0MUA)—Offset 4h

MSI-X Table Entries 0 Message Upper Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message upper 32-bit address (MXMUA):** Specifies the upper 32-bit of the MSI-X Message.

14.5.3 MSI-X Table Entries 0 Message Data (MXTE0MD)—Offset 8h

MSI-X Table Entries 0 Message Data

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

14.5.4 MSI-X Table Entries 0 Vector Control (MXTE0VC)—Offset Ch

MSI-X Table Entries 0 Vector Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

14.5.5 MSI-X Table Entries 1 Message Lower Address (MXTE1MLA)—Offset 10h

MSI-X Table Entries 1 Message Lower Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI-X message lower address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	0h RO	Reserved.

14.5.6 MSI-X Table Entries 1 Message Upper Address (MXTE1MUA)—Offset 14h

MSI-X Table Entries 1 Message Upper Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message upper 32-bit address (MXMUA):** Specifies the upper 32-bit of the MSI-X Message

14.5.7 MSI-X Table Entries 1 Message Data (MXTE1MD)—Offset 18h

MSI-X Table Entries 1 Message Data

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

14.5.8 MSI-X Table Entries 1 Vector Control (MXTE1VC)—Offset 1Ch

MSI-X Table Entries 1 Vector Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

14.5.9 MSI-X Table Entries 2 Message Lower Address (MXTE2MLA)—Offset 20h

MSI-X Table Entries 2 Message Lower Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI-X message lower address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	0h RO	Reserved.

14.5.10 MSI-X Table Entries 2 Message Upper Address (MXTE2MUA)—Offset 24h

MSI-X Table Entries 2 Message Upper Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message upper 32-bit address (MXMUA):** Specifies the upper 32-bit of the MSI-X Message

14.5.11 MSI-X Table Entries 2 Message Data (MXTE2MD)—Offset 28h

MSI-X Table Entries 2 Message Data

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

14.5.12 MSI-X Table Entries 2 Vector Control (MXTE2VC)—Offset 2Ch

MSI-X Table Entries 2 Vector Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

14.5.13 MSI-X Table Entries 3 Message Lower Address (MXTE3MLA)—Offset 30h

MSI-X Table Entries 3 Message Lower Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI-X message lower address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	0h RO	Reserved.

14.5.14 MSI-X Table Entries 3 Message Upper Address (MXTE3MUA)—Offset 34h

MSI-X Table Entries 3 Message Upper Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message upper 32-bit address (MXMUA):** Specifies the upper 32-bit of the MSI-X Message

14.5.15 MSI-X Table Entries 3 Message Data (MXTE3MD)—Offset 38h

MSI-X Table Entries 3 Message Data

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

14.5.16 MSI-X Table Entries 3 Vector Control (MXTE3VC)—Offset 3Ch

MSI-X Table Entries 3 Vector Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

14.5.17 MSI-X Table Entries 4 Message Lower Address (MXTE4MLA)—Offset 40h

MSI-X Table Entries 4 Message Lower Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI-X message lower address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	0h RO	Reserved.

14.5.18 MSI-X Table Entries 4 Message Upper Address (MXTE4MUA)—Offset 44h

MSI-X Table Entries 4 Message Upper Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message upper 32-bit address (MXMUA):** Specifies the upper 32-bit of the MSI-X Message

14.5.19 MSI-X Table Entries 4 Message Data (MXTE4MD)—Offset 48h

MSI-X Table Entries 4 Message Data

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

14.5.20 MSI-X Table Entries 4 Vector Control (MXTE4VC)—Offset 4Ch

MSI-X Table Entries 4 Vector Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

14.5.21 MSI-X Table Entries 5 Message Lower Address (MXTE5MLA)—Offset 50h

MSI-X Table Entries 5 Message Lower Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI-X message lower address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	0h RO	Reserved.

14.5.22 MSI-X Table Entries 5 Message Upper Address (MXTE5MUA)—Offset 54h

MSI-X Table Entries 5 Message Upper Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message upper 32-bit address (MXMUA):** Specifies the upper 32-bit of the MSI-X Message

14.5.23 MSI-X Table Entries 5 Message Data (MXTE5MD)—Offset 58h

MSI-X Table Entries 5 Message Data

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

14.5.24 MSI-X Table Entries 5 Vector Control (MXTE5VC)—Offset 5Ch

MSI-X Table Entries 5 Vector Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

14.5.25 MSI-X Table Entries 6 Message Lower Address (MXTE6MLA)—Offset 60h

MSI-X Table Entries 6 Message Lower Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI-X message lower address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	0h RO	Reserved.

14.5.26 MSI-X Table Entries 6 Message Upper Address (MXTE6MUA)—Offset 64h

MSI-X Table Entries 6 Message Upper Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message upper 32-bit address (MXMUA):** Specifies the upper 32-bit of the MSI-X Message

14.5.27 MSI-X Table Entries 6 Message Data (MXTE6MD)—Offset 68h

MSI-X Table Entries 6 Message Data

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

14.5.28 MSI-X Table Entries 6 Vector Control (MXTE6VC)—Offset 6Ch

MSI-X Table Entries 6 Vector Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

14.5.29 MSI-X Table Entries 7 Message Lower Address (MXTE7MLA)—Offset 70h

MSI-X Table Entries 7 Message Lower Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**MSI-X message lower address (MXMLA):** Specifies the lower 32-bit of the DWORD-aligned address (Addr[31:02]) of the MSI-X Message.
1:0	0h RO	Reserved.

14.5.30 MSI-X Table Entries 7 Message Upper Address (MXTE7MUA)—Offset 74h

MSI-X Table Entries 7 Message Upper Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message upper 32-bit address (MXMUA):** Specifies the upper 32-bit of the MSI-X Message

14.5.31 MSI-X Table Entries 7 Message Data (MXTE7MD)—Offset 78h

MSI-X Table Entries 7 Message Data

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**MSI-X message Data (MXMD):** Specifies the 32-bit Data of the MSI-X Message.

14.5.32 MSI-X Table Entries 7 Vector Control (MXTE7VC)—Offset 7Ch

MSI-X Table Entries 7 Vector Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	1h RW	**MSI-X vector Mask (MXVM):** When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked).

15 Intel® Management Interface (Intel® MEI) (D22:F0/F1/F4/F5)

15.1 Intel® Management Engine Interface PCI Configuration Registers Summary

The registers in this section apply to the following Intel® Management Engine Interfaces (MEI):
MEI 1 at Device 22:Function 0
MEI 2 at Device 22:Function 1
MEI 3 at Device 22:Function 4
MEI 4 at Device 22:Function 5

Table 15-1. Summary of Intel® Management Engine Interface PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	HECI ID (HECI1_ID)—Offset 0h	XXXX8086h
4h	5h	HECI Command (HECI1_CMD)—Offset 4h	0h
6h	7h	HECI Status (HECI1_STS)—Offset 6h	10h
8h	Bh	Revision ID And Class Code (HECI1_RID_CC)—Offset 8h	78000XXh
Ch	Ch	Cache Line Size (HECI1_CLS)—Offset Ch	0h
Dh	Dh	Master Latency Timer (HECI1_MLT)—Offset Dh	0h
Eh	Eh	Header Type (HECI1_HTYPE)—Offset Eh	80h
Fh	Fh	Built In Self-Test (HECI1_BIST)—Offset Fh	0h
10h	13h	HECI MMIO Base Address Low (HECI1_MMIO_MBAR_LO)—Offset 10h	4h
14h	17h	HECI MMIO Base Address High (HECI1_MMIO_MBAR_HI)—Offset 14h	0h
2Ch	2Fh	Sub System Identifiers (HECI1_SS)—Offset 2Ch	0h
34h	37h	Capabilities Pointer (HECI1_CAP)—Offset 34h	50h
3Fh	3Fh	Maximum Latency (HECI1_MLAT)—Offset 3Fh	0h
40h	43h	Host Firmware Status (HECI1_HFS)—Offset 40h	0h
44h	47h	Miscellaneous Shadow (HECI1_MISC_SHDW)—Offset 44h	80000000h
48h	4Bh	General Status Shadow 1 (HECI1_GS_SHDW1)—Offset 48h	0h
4Ch	4Fh	Host General Status (HECI1_H_GS1)—Offset 4Ch	0h
50h	51h	PCI Power Management Capability ID (HECI1_PID)—Offset 50h	8C01h
52h	53h	PCI Power Management Capabilities (HECI1_PC)—Offset 52h	4003h
64h	67h	General Status Shadow 3 (HECI1_GS_SHDW3)—Offset 64h	0h
68h	6Bh	General Status Shadow 4 (HECI1_GS_SHDW4)—Offset 68h	0h
6Ch	6Fh	General Status Shadow 5 (HECI1_GS_SHDW5)—Offset 6Ch	0h
70h	73h	Host General Status 2 (HECI1_H_GS2)—Offset 70h	0h

Table 15-1. Summary of Intel® Management Engine Interface PCI Configuration Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
74h	77h	Host General Status 3 (HECI1_H_GS3)—Offset 74h	0h
8Ch	8Dh	Message Signaled Interrupt Identifiers (HECI1_MID)—Offset 8Ch	A405h
8Eh	8Fh	Message Signaled Interrupt Message Control (HECI1_MC)—Offset 8Eh	80h
90h	93h	Message Signaled Interrupt Message Address (HECI1_MA)—Offset 90h	0h
94h	97h	Message Signaled Interrupt Upper Address (HECI1_MUA)—Offset 94h	0h
98h	99h	Message Signaled Interrupt Message Data (HECI1_MD)—Offset 98h	0h
A0h	A0h	HECI Interrupt Delivery Mode (HECI1_HIDM)—Offset A0h	0h
ACh	AFh	SW LTR Pointer Register (HECI1_SWLTRPTR)—Offset ACh	0h
B0h	B3h	Device Idle Pointer Register (HECI1_DEVIDLEPTR)—Offset B0h	8001h
B6h	B7h	DevIdle Power Control Enabled Register (HECI1_PWRCTRLEN)—Offset B6h	Eh
CCh	CFh	Host Extend Register DW4 (HECI1_HER4)—Offset CCh	0h
D4h	D7h	Host Extend Register DW6 (HECI1_HER6)—Offset D4h	0h
D8h	DBh	Host Extend Register DW7 (HECI1_HER7)—Offset D8h	0h
DCh	DFh	Host Extend Register DW8 (HECI1_HER8)—Offset DCh	0h

15.1.1 HECI ID (HECI1_ID)—Offset 0h

Identification

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: XXXX8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	-- RO/V	**Device ID (DID):** Indicates what device number assigned by Intel. Refer to the Device and Revision ID Table in Volume 1 for default value.
15:0	8086h RO	**Vendor ID (VID):** 16-bit field which indicates Intel is the vendor.

15.1.2 HECI Command (HECI1_CMD)—Offset 4h

Command

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (ID):** Disables this device from generating PCI line based interrupts. This bit does not have any effect on MSI operation.
9	0h RO	**Fast Back-to-Back Enable (FBE):** Not implemented, hardwired to 0.
8	0h RO	**SERR# Enable (SEE):** Not implemented, hardwired to 0.
7	0h RO	**Wait Cycle Enable (WCC):** Not implemented, hardwired to 0.
6	0h RO	**Parity Error Response Enable (PEE):** Not implemented, hardwired to 0.
5	0h RO	**VGA Palette Snooping Enable (VAG):** Not implemented, hardwired to 0
4	0h RO	**Memory Write And Invalidate Enable (MWIE):** Not implemented, hardwired to 0.
3	0h RO	**Special Cycle Enable (SCE):** Not implemented, hardwired to 0.
2	0h RW	**Bus Master Enable (BME):** Controls the HECI host controller's abiity to act as a system memory master for data transfers. When this bit is cleared, HECI bus master activity stops and any active DMA engines return to an idle condition. This bit is made visible to firmware through the H_PCI_CSR register, and changes to this bit may be configured by the H_PCI_CSR register to generate an MSI to mIA. When this bit is '0', HECI is blocked from generating MSI to the host CPU. Note that this bit does not block HECI accesses to CSE-UMA.
1	0h RW	**Memory Space Enable (MSE):** Controls access to the HECI host controller's memory mapped register space.
0	0h RO	**I/O Space Enable (IOSE):** Not implemented, hardwired to 0.

15.1.3 HECI Status (HECI1_STS)—Offset 6h

Status

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 10h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RO	**Detected Parity Error (DPE):** Not implemented, hardwired to 0.
14	0h RO	**Signaled System Error (SSE):** Not implemented, hardwired to 0.
13	0h RO	**Received Master-Abort (RMA):** Not implemented, hardwired to 0.
12	0h RO	**Received Target Abort (RTA):** Not implemented, hardwired to 0.

Bit Range	Default and Access	Field Name (ID): Description
11	0h RO	**Signaled Target-Abort (STA):** Not implemented, hardwired to 0.
10:9	0h RO	**DEVSEL# Timing (DEVT):** These bits are hardwired to 00.
8	0h RO	**Master Data Pariy Error Detected (DPD):** Not implemented, hardwired to 0.
7	0h RO	**Fast Back-to-Back Capable (FBC):** Not implemented, hardwired to 0.
6	0h RO	Reserved.
5	0h RO	**66 MHz Capable (C66):** Not implemented, hardwired to 0.
4	1h RO	**Capabilities List (CL):** Indicates the presence of a capabilities list, hardwired to 1.
3	0h RO/V	**Interrupt Status (IS):** Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted. This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register). Note that this bit is not set by an MSI.
2:0	0h RO	Reserved.

15.1.4 Revision ID And Class Code (HECI1_RID_CC)—Offset 8h

Revision ID And Class Code

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 78000XXh

Bit Range	Default and Access	Field Name (ID): Description
31:24	7h RO	**Base Class Code (BCC):** Indicates the base class code of the HECI host controller device.
23:16	80h RO	**Sub Class Code (SCC):** Indicates the sub class code of the HECI host controller device.
15:8	0h RO	**Programming Interface (PI):** Indicates the programming interface of the HECI host controller device.
7:0	-- RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

15.1.5 Cache Line Size (HECI1_CLS)—Offset Ch

Cache Line Size

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO	**Cache Line Size (CLS):** Not implemented, hardwired to 0.

15.1.6 Master Latency Timer (HECI1_MLT)—Offset Dh

Master Latency Timer

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO	**Master Latency Timer (MLT):** Not implemented, hardwired to 0.

15.1.7 Header Type (HECI1_HTYPE)—Offset Eh

Header Type

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RO	**Multi-Function Device (MFD):** Indicates the HECI host controller is part of a multi- function device.
6:0	0h RO	**Header Layout (HL):** Indicates that the HECI host controller uses a target device layout.

15.1.8 Built In Self-Test (HECI1_BIST)—Offset Fh

Built In Self-Test

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO	**BIST Capable (BC):** Not implemented, hardwired to 0.
6:0	0h RO	Reserved.

15.1.9 HECI MMIO Base Address Low (HECI1_MMIO_MBAR_LO)—Offset 10h

HECI MMIO Base Address Low

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW	**Base Address Low (BA_LO):** Lower 32 bits of base address of register memory space.
11:4	0h RO	**Memory Size (MS):** This field is hardwired to 0 to indicate that HECI device requests 4KB of memory space.
3	0h RO	**Prefetchable (PF):** Indicates that this range is not pre-fetchable.
2:1	2h RO	**Type (TP):** Indicates that this range can be mapped anywhere in 64-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** Indicates a request for register memory space.

15.1.10 HECI MMIO Base Address High (HECI1_MMIO_MBAR_HI)—Offset 14h

HECI MMIO Base Address High

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address High (BA_HI):** Upper 32 bits of base address of register memory space.

15.1.11 Sub System Identifiers (HECI1_SS)—Offset 2Ch

Sub System Identifiers

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** Indicates the subsystem identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** Indicates the subsystem vendor identifier. This field should be programmed by BIOS during boot- up. Once written, this register becomes Read Only.

15.1.12 Capabilities Pointer (HECI1_CAP)—Offset 34h

Capabilities Pointer

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 50h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	50h RO	**Capability Pointer (CP):** Indicates the first capability pointer offset. It points to the PCI power management capability offset.

15.1.13 Maximum Latency (HECI1_MLAT)—Offset 3Fh

Maximum Latency

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO	**Latency (LAT):** Not implemented, hardwired to 0.

15.1.14 Host Firmware Status (HECI1_HFS)—Offset 40h

Host Firmware Status

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Firmware Status Host Access (FS_HA):** Indicates current status of the firmware for the HECI controller. This field is the host's read only access to the FS field in the CSE Firmware Status register.

15.1.15 Miscellaneous Shadow (HECI1_MISC_SHDW)—Offset 44h

Miscellaneous Shadow

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 80000000h

Bit Range	Default and Access	Field Name (ID): Description
31	1h RO	**Miscellaneous Shadow Valid (MSVLD):** This bit is hardwired to 1 to indicate that this HECI device implements the Miscellaneous Shadow register. This bit can be used by host software that is bus/dev/function number agnostic (such as HECI operating system driver) to discover whether the Miscellaneous Shadow register is implemented or not.
30:17	0h RO	Reserved.
16	0h RO/V	**CSE UMA Size Valid (CUSZV):** This bit indicates that FW has written the CUSZ field. This field reflects the value of CSE CUBA.CUSZV.
15:12	0h RO	Reserved.
11:0	0h RO/V	**CSE UMA Size (CUSZ):** These bits reflect firmware's desired size of CSEUMA memory region at 1MB granularity, 1-based. It is configured by firmware prior to bring up core power and allowing BIOS to initialize memory. Example: 000h (0MB, no CSEUMA) 003h (3MB) 040h (64MB) FFFh (4GB) This field reflects the value of CSE CUBA.CUSZ.

15.1.16 General Status Shadow 1 (HECI1_GS_SHDW1)—Offset 48h

General Status Shadow 1

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**General Status Shadow 1 (GSS1):** This field is host side shadow of CSE General Status 1 (CSE_GS1).

15.1.17 Host General Status (HECI1_H_GS1)—Offset 4Ch

Host General Status

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Host General Status (H_GS1):** General status of Host. This field is not used by hardware.

15.1.18 PCI Power Management Capability ID (HECI1_PID)—Offset 50h

PCI Power Management Capability ID

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 8C01h

Bit Range	Default and Access	Field Name (ID): Description
15:8	8Ch RO	**Next Capability (NEXT):** Indicates the location of the next capability item in the list. This is the Message Signaled Interrupts capability.
7:0	1h RO	**Cap ID (CID):** Indicates that this pointer is a PCI power management.

15.1.19 PCI Power Management Capabilities (HECI1_PC)—Offset 52h

PCI Power Management Capabilities

Access Method

Type: CFG Register (Size: 16 bits)
Device: 22
Function: 0

Default: 4003h

Bit Range	Default and Access	Field Name (ID): Description
15:11	8h RO	**PME Support (PSUP):** Indicates the states that can generate PME#. HECI can assert PME# from D3hot only.
10	0h RO	**D2 Support (D2S):** The D2 state is not supported for the HECI host controller.
9	0h RO	**D1 Support (D1S):** The D1 state is not supported for the HECI host controller.
8:6	0h RO	**Aux Current (AUXC):** Reports the maximum Suspend well current required when in the D3COLD state. Value of 0 is reported.
5	0h RO	**Device Specific Initialization (DSI):** Indicates whether device-specific initialization is required.
4	0h RO	Reserved.
3	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.

15.1.20 General Status Shadow 3 (HECI1_GS_SHDW3)—Offset 64h

General Status Shadow 3

Access Method

Type: CFG Register (Size: 32 bits)
Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**General Status Shadow 3 (GSS3):** This field is host side shadow of CSE General Status 3 (CSE_GS3).

15.1.21 General Status Shadow 4 (HECI1_GS_SHDW4)—Offset 68h

General Status Shadow 4

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**General Status Shadow 4 (GSS4):** This field is host side shadow of CSE General Status 4 (CSE_GS4).

15.1.22 General Status Shadow 5 (HECI1_GS_SHDW5)—Offset 6Ch

General Status Shadow 5

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**General Status Shadow 5 (GSS5):** This field is host side shadow of CSE General Status 5 (CSE_GS5).

15.1.23 Host General Status 2 (HECI1_H_GS2)—Offset 70h

Host General Status 2

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Host General Status 2 (H_GS2):** General status of Host. This field is not used by hardware.

15.1.24 Host General Status 3 (HECI1_H_GS3)—Offset 74h

Host General Status 3

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Host General Status 3 (H_GS3):** General status of Host. This field is not used by hardware.

15.1.25 Message Signaled Interrupt Identifiers (HECI1_MID)—Offset 8Ch

Message Signaled Interrupt Identifiers

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: A405h

Bit Range	Default and Access	Field Name (ID): Description
15:8	A4h RO	**Next Pointer (NEXT):** Indicates the location of the next capability item in the list. This is the DevIdle conventional PCI vendor specific capability.
7:0	5h RO	**Capability ID (CID):** Indicates MSI.

15.1.26 Message Signaled Interrupt Message Control (HECI1_MC)—Offset 8Eh

Message Signaled Interrupt Message Control

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7	1h RO	**64 Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages.
6:4	0h RO	**Multiple Message Enable (MME):** Not implemented, hardwired to 0.
3:1	0h RO	**Multiple Message Capable (MMC):** Not implemented, hardwired to 0.
0	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and INTx virtual wires are not used to generate interrupts.

15.1.27 Message Signaled Interrupt Message Address (HECI1_MA)—Offset 90h

Message Signaled Interrupt Message Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DW aligned.
1:0	0h RO	Reserved.

15.1.28 Message Signaled Interrupt Upper Address (HECI1_MUA)—Offset 94h

Message Signaled Interrupt Upper Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Upper Address (UADDR):** Upper 32 bits of the system specified message address. This register is optional and only implemented if MC.C64=1.

15.1.29 Message Signaled Interrupt Message Data (HECI1_MD)—Offset 98h

Message Signaled Interrupt Message Data

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the FSB during the data phase of the MSI memory write transaction.

15.1.30 HECI Interrupt Delivery Mode (HECI1_HIDM)—Offset A0h

HECI Interrupt Delivery Mode

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2	0h RW/1S/V	**HIDM Lock (HIDM_L):** Writing 1 to this bit locks the HIDM field.
1:0	0h RW/L	**HECI Interrupt Delivery Mode (HIDM):** These bits control what type of interrupt the HECI will send when CSE FW writes to set the CSE_IG bit. They are interpreted as follows: 00 - Generate Legacy or MSI interrupt; 01 - Generate SCI; 10 - Generate SMI; This field may be locked by writing 1 to HIDM_L bit.

15.1.31 SW LTR Pointer Register (HECI1_SWLTRPTR)—Offset ACh

Software Latency Tolerance Reporting (LTR) Pointer Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	**SW LTR Update MMIO Offset Location (SWLTRLOC):** This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR. The value of this register is not valid, if the Valid bit is not set.
3:1	0h RO	**Base Address Register Number (BARNUM):** Contains the 0's based AR Number of the BAR which contains the location of the SW LTR MMIO register. When counting BAR Numbers, all BARs, regardless of size and type, consume one BAR Number. Bar 0 is the 1st BAR. The value of this register is not valid, if the Valid bit is not set.
0	0h RO	**Valid (Valid):** Set to 1'b1 to indicate that the function has implemented a SW LTR register as specified in the DevIdle that can be located using the SWLTRLOC register and BARNUM. Set to 1'b0 to indicate that the function has not implemented a SW LTR register that is compliant to the DevIdle definition. This could be because the function has not implemented SW LTR at all, or has a device specific version of SW LTR.

15.1.32 Device Idle Pointer Register (HECI1_DEVIDLEPTR)—Offset B0h

Device Idle Pointer Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 8001h

Bit Range	Default and Access	Field Name (ID): Description
31:4	800h RO	**Device Idle MMIO Offset Location (DEVIDLELOC):** This register contains the location pointer to the DevIdle register in MMIO space, as an offset from the specified BAR. The value of this register is not valid, if the Valid bit is not set.
3:1	0h RO	**Base Address Register Number (BARNUM):** Contains the 0's based AR Number of the BAR which contains the location of the SW LTR MMIO register. When counting BAR Numbers, all BARs, regardless of size and type, consume one BAR Number. Bar 0 is the 1st BAR. The value of this register is not valid, if the Valid bit is not set.
0	1h RO	**Valid (Valid):** Set to 1'b1 to indicate that the function has implemented a SW LTR register as specified DevIdle that can be located using the DEVIDLELOC register and BARNUM. Set to 1'b0 to indicate that the function has not implemented a DevIdle register that is compliant to the DevIdle definition. This could be because the function has not implemented SW LTR at all, or has a device specific version of device idle.

15.1.33 DevIdle Power Control Enabled Register (HECI1_PWRCTRLEN)—Offset B6h

DevIdle Power Control Enabled Register

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 22
Function: 0

Default: Eh

Bit Range	Default and Access	Field Name (ID): Description
15:6	0h RO	Reserved.
5	0h RO	**Hardware Autonomous Enable (HAE):** CSE does not support autonomous power gating on idle.
4	0h RO	Reserved.
3	1h RO	**Sleep Enable (SE):** CSE always asserts the sleep signal during power gating.
2	1h RO	**D3-Hot Enable (D3HEN):** CSE could power gate when idle and the PMCSR[1:0] register in the function =2'b11 (D3).
1	1h RO	**DEVIDLE Enable (DEVIDLEN):** CSE could power gate when idle and the DevIdle register (DevIdleC[2] = 1'b1) is set.
0	0h RO	**PMC Request Enable (PMCRE):** CSE will not power gate due to pmc_ip_sw_pg_req_b = LOW.

15.1.34 Host Extend Register DW4 (HECI1_HER4)—Offset CCh

Host Extend Register DW4

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Host Extend Register DW4 (ERDW4):** Host Extend Register DW4.

15.1.35 Host Extend Register DW6 (HECI1_HER6)—Offset D4h

Host Extend Register DW6

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Host Extend Register DW6 (ERDW6):** Host Extend Register DW6.

15.1.36 Host Extend Register DW7 (HECI1_HER7)—Offset D8h

Host Extend Register DW7

Access Method

Type: CFG Register (Size: 32 bits)
Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Host Extend Register DW7 (ERDW7):** Host Extend Register DW7.

15.1.37 Host Extend Register DW8 (HECI1_HER8)—Offset DCh

Host Extend Register DW8

Access Method

Type: CFG Register (Size: 32 bits)
Device: 22
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Host Extend Register DW8 (ERDW8):** Host Extend Register DW8.

15.2 Intel® MEI MMIO Registers Summary

The registers in this section apply to the following Intel(R) Management Engine Interfaces (MEI):
MEI 1 at Device 22:Function 0
MEI 2 at Device 22:Function 1
MEI 3 at Device 22:Function 4
MEI 4 at Device 22:Function 5

Table 8. Summary of Intel(R) MEI MMIO Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
800h	803h	DEVIDLE Control (HECI1_DEVIDLEC)—Offset 800h	0h
CBCh	CBFh	Host Enhanced Extend Register Status (HECI1_ENH_HERS)—Offset CBCh	40000000h

15.2.1 DEVIDLE Control (HECI1_DEVIDLEC)—Offset 800h

This register allows host to configure the power mode using D0i0/D0i3 support.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	0h RO	**Restore Required (RR):** When this bit is set (by HW), SW must restore the state of the IP. This bit is cleared by SW writing a 1. **In CSE this bit is never set so it does not need to be cleared by SW.**
2	0h RW	**DevIdle (DEVIDLE):** SW sets this bit to 1'b1 to move the function into the DevIdle state. Writing this bit to 1'b0 will return the function to the fully active D0 state (D0i0).
1	0h RW	**Interrupt Request (IR):** SW sets this bit to 1'b1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RO/V	**Command-in-Progress (CIP):** HW sets this bit on a 1'b1->1'b0 or 1'b0->1'b1 transition of DEVIDLE. While set, the other bits in this register are not valid and it is unsupported for SW to write to any bit in this register. HW clears this bit when CSE FW clears its own DevIdle interrupt status bit indicating completion of the DevIdle transition command. When clear, all the other bits in the register are valid and SW may write to any bit. If Interrupt Request (IR) was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect.

15.2.2 Host Enhanced Extend Register Status (HECI1_ENH_HERS)—Offset CBCh

This register is used to communicate the CSE FW measurement status information to host.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 40000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Extend Register Valid (ERV):** Set by FW after all FW has been loaded and the measurement data has been stored in HERx registers. If ERA field is SHA-1, the result of the extend operation is in ENH_HER:5-1. If ERA field is SHA-256, the result is in ENH_HER:8-1. If ERA field is SHA-384, the result is in ENH_HER:12-1
30	1h RO	**Extend Feature Present (EFP):** This bit is hardwired to 1 to allow driver software to easily detect the chipset supports the Extend Registers FW measurement feature.

Bit Range	Default & Access	Field Name (ID): Description
29	0h RO/V	**Extend Complete (ERC):** This bit is set by OCS hardware at the end of an extend operation if the EXTEND_OVER bit is set when setting the EXTEND_START bit.
28:4	0h RO	Reserved.
3:0	0h RO/V	**Extend Register Algorithm (ERA):** This field indicates the hash algorithm used in the FW measurement Extend operation. Encodings are: 0x0: SHA-1, 0x2: SHA-256, 0x4: SHA-384. Other values: reserved. This field is set by FW with the used hash algorithm value when the ERV bit is set to 1. This field is meaningless when the ERV bit is 0. This field does NOT have any defined reset value.

16 IDE Redirect (IDE-R) (D22:F2)

16.1 IDE Redirect PCI Configuration (D22:F2) Registers Summary

Table 16-1. Summary of IDE Redirect PCI Configuration (D22:F2) Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID And Vendor ID (IDE_HOST_DID_VID)—Offset 0h	XXXX8086h
4h	7h	Status And Command (IDE_HOST_STS_CMD)—Offset 4h	B00000h
8h	Bh	Class Code And Revision ID (IDE_HOST_CC_RID)—Offset 8h	010185XXh
Ch	Fh	BIST, Header Type, Latency Timer, And Cache Line Size (IDE_HOST_BIST_HTYPE_LT_CLS)—Offset Ch	800000h
10h	13h	IDE Primary Command Block IO BAR (IDE_HOST_PCMDIOBAR)—Offset 10h	1h
14h	17h	IDE Primary Control Block IO BAR (IDE_HOST_PCTLIOBAR)—Offset 14h	1h
18h	1Bh	IDE Secondary Command Block IO BAR (IDE_HOST_SCMDIOBAR)—Offset 18h	1h
1Ch	1Fh	IDE Secondary Control Block IO BAR (IDE_HOST_SCTLIOBAR)—Offset 1Ch	1h
20h	23h	IDE Bus Master Block IO BAR (IDE_HOST_BMIOBAR)—Offset 20h	1h
2Ch	2Fh	Subsystem ID And Subsystem Vendor ID (IDE_HOST_SID_SVID)—Offset 2Ch	8086h
34h	37h	Capabilities List Pointer (IDE_HOST_CAPP)—Offset 34h	40h
3Ch	3Fh	Maximum Latency, Minimum Grant, Interrupt Pin And Interrupt Line (IDE_HOST_MAXL_MING_INTP_INTL)—Offset 3Ch	0h
40h	43h	MSI Message Control, Next Pointer And Capability ID (IDE_HOST_MSIMC_MSINP_MSICID)—Offset 40h	805005h
44h	47h	MSI Message Address (IDE_HOST_MSIMA)—Offset 44h	0h
48h	4Bh	MSI Message Upper Address (IDE_HOST_MSIMUA)—Offset 48h	0h
4Ch	4Fh	MSI Message Data (IDE_HOST_MSIMD)—Offset 4Ch	0h
50h	53h	Power Management Capabilities, Next Pointer And Capability ID (IDE_HOST_PMCAP_PMNP_PMCID)—Offset 50h	230001h
54h	57h	Power Management Data, Control/Status Register Bridge Support Extensions, Control And Status (IDE_HOST_PMD_PMCSRBSE_PMCSR)—Offset 54h	8h

16.1.1 Device ID And Vendor ID (IDE_HOST_DID_VID)—Offset 0h

This register contains the device ID and vendor ID values.

Access Method

Type: CFG Register (Size: 32 bits)

Device: 22
Function: 2

Default: XXXX8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	-- RO/V	**Device ID (DID):** This field identifies the particular device. Refer to the Device and Revision ID Table in Volume 1 for default value.
15:0	8086h RO	**Vendor ID (VID):** This field identifies the manufacturer of the device. The value of 0x8086 indicates Intel.

16.1.2 Status And Command (IDE_HOST_STS_CMD)—Offset 4h

This register contains the PCI status and command registers.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: B00000h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**Detected Parity Error (DPE):** Not implemented. Hardwired to 0.
30	0h RO	**Signaled System Error (SSE):** Not implemented. Hardwired to 0.
29	0h RW/1C/V	**Received Master Abort (RMA):** This bit must be set by a master device whenever its transaction (except for Special Cycle) is completed with Unsupported Request Completion Status (a.k.a. Master-Abort). All master devices must implement this bit.
28	0h RW/1C/V	**Received Target Abort (RTA):** This bit must be set by a master device whenever its transaction is completed with Completer Abort Completion Status (a.k.a. Target-Abort). All master devices must implement this bit.
27	0h RW/1C/V	**Signaled Target Abort (STA):** This bit must be set by a target device whenever it completes a Posted or Non-Posted transaction with a Completer Abort (a.k.a. Target-Abort) error. Devices that will never signal Completer Abort (a.k.a. Target-Abort) do not need to implement this bit.
26:25	0h RO	**Devsel Timing (DEVT):** These bits encode the timing of DEVSEL#. There are three allowable timings for assertion of DEVSEL# as described below: 00b: fast; 01b: medium; 10b: slow; 11b: reserved. These bits are read-only and must indicate the slowest time that a device asserts DEVSEL# for any bus command except Configuration Read and Configuration Write. Hardwired to 00b.
24	0h RO	**Master Data Parity Error (MDPE):** Not implemented. Hardwired to 0.
23	1h RO	**Fast Back To Back Capable (FBTBC):** This bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. This bit can be set to 1 if the device can accept these transactions and must be set to 0 otherwise. Hardwired to 1.
22	0h RO	Reserved.
21	1h RO	**66 Mhz Capable (MCAP):** This bit indicates whether or not this device is capable of running at 66 MHz. A value of 0 indicates 33 MHz. A value of 1 indicates that the device is 66 MHz capable. Hardwired to 1.

Bit Range	Default and Access	Field Name (ID): Description
20	1h RO	**Capabilities List (CAPL):** This optional read-only bit indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. A value of zero indicates that no New Capabilities linked list is available. A value of one indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities.
19	0h RO	**Interrupt Status (INTS):** This read-only bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. Read-only and hardwired to 0 for a device that does NOT support pin-based interrupt.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTD):** This bit disables the device/function from asserting INTx#. A value of 0 enables the assertion of its INTx# signal. A value of 1 disables the assertion of its INTx# signal. This bit's state after RST# is 0.
9	0h RO	**Fast Back To Back Enable (FBTBEN):** Not implemented. Hardwired to 0.
8	0h RO	**System Error Enable (SERREN):** Not implemented. Hardwired to 0.
7	0h RO	Reserved.
6	0h RO	**Parity Error Response (PERRR):** Not implemented. Hardwired to 0.
5	0h RO	**VGA Palette Snoop (VGAPS):** Not implemented. Hardwired to 0.
4	0h RO	**Memory Write And Invalidate Enable (MWRIEN):** Not implemented. Hardwired to 0.
3	0h RO	**Special Cycles (SPCYC):** Not implemented. Hardwired to 0.
2	0h RW	**Bus Master Enable (BME):** Controls the ability of a PCI device to issue Memory and I/O Read/Write Requests, and the ability of a PCI bridge to forward Memory and I/O Read/Write Requests in the Upstream direction. Devices: When this bit is Set, the PCI device function is allowed to issue Memory or I/O Requests. When this bit is Clear, the PCI device function is not allowed to issue any Memory or I/O Requests. Note that as MSI/MSI-X interrupt Messages are in-band memory writes, setting the Bus Master Enable bit to 0b disables MSI/MSI-X interrupt Messages as well. Requests other than Memory or I/O Requests are not controlled by this bit. Bridges: This bit controls forwarding of Memory or I/O Requests by a bridge in the Upstream direction. When this bit is 0b, Memory and I/O Requests received at the Downstream side of a bridge must be handled as Unsupported Requests (UR), and for Non-Posted Requests a Completion with UR completion status must be returned. This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O Requests is not controlled by this bit.
1	0h RO	**Memory Space Enable (MSE):** Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. State after RST# is 0. Read-only and hardwired to 0 because IDE does NOT support Memory Space accesses.
0	0h RW	**IO Space Enable (IOSE):** Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after RST# is 0.

16.1.3 Class Code And Revision ID (IDE_HOST_CC_RID)—Offset 8h

This register contains the class code and revision ID values.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 010185XXh

Bit Range	Default and Access	Field Name (ID): Description
31:24	1h RO	**Base Class Code (BCC):** Identifies the Base Class Code of an external IDE controller device driver.
23:16	1h RO	**Sub-Class Code (SCC):** Identifies the Sub-Class Code of an external IDE controller device driver.
15:8	85h RO	**Programming Interface (PI):** Identifies the Programming Interface of an IDE controller device driver.
7:0	0h RO/V	**Revision ID (RID):** This register specifies a device specific revision identifier. Refer to Device and Revision ID table in Vol1 for specific value.

16.1.4 BIST, Header Type, Latency Timer, And Cache Line Size (IDE_HOST_BIST_HTYPE_LT_CLS)—Offset Ch

This register contains the BIST, header type, latency timer, and cache line size values.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 800000h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	**Built In Self Test (BIST):** Not implemented. Hardwired to 0.
23	1h RO/V	**Header Type 1 (HTYPE1):** This bit identifies whether or not the device contains multiple functions. - If the bit is 0, then the device is single function. - If the bit is 1, then the device has multiple functions.
22:16	0h RO	**Header Type 0 (HTYPE0):** This field identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space). - The encoding 00h specifies the non-bridge Configuration Space Header. - The encoding 01h specifies the PCI-to-PCI bridge Configuration Space Header. - The encoding 02h specifies the CardBus bridge Configuration Space Header. - All other encodings are reserved. Hardwired to 0 to identify the non-bridge Configuration Space Header.
15:8	0h RO	**Latency Timer (LT):** Not implemented. Hardwired to 0.
7:0	0h RO	**Cache Line Size (CLS):** Not implemented. Hardwired to 0.

16.1.5 IDE Primary Command Block IO BAR (IDE_HOST_PCMDIOBAR)—Offset 10h

This is the IO space base address register.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RW	**IO BAR (IOBAR):** Software programs this space with the base address of the device's IO region
2	0h RO	**IO Size (IOSIZE):** Hardwired to 0 to indicate 8B of IO space
1	0h RO	Reserved.
0	1h RO	**IO Space Indicator (IOSPACE):** Hardwired to 1 to identify an IO BAR.

16.1.6 IDE Primary Control Block IO BAR (IDE_HOST_PCTLIOBAR)—Offset 14h

This is the IO space base address register.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**IO BAR (IOBAR):** Software programs this space with the base address of the device's IO region
1	0h RO	Reserved.
0	1h RO	**IO Space Indicator (IOSPACE):** Hardwired to 1 to identify an IO BAR.

16.1.7 IDE Secondary Command Block IO BAR (IDE_HOST_SCMDIOBAR)—Offset 18h

This is the IO space base address register.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RW	**IO BAR (IOBAR):** Software programs this space with the base address of the device's IO region
2	0h RO	**IO Size (IOSIZE):** Hardwired to 0 to indicate 8B of IO space
1	0h RO	Reserved.
0	1h RO	**IO Space Indicator (IOSPACE):** Hardwired to 1 to identify an IO BAR.

16.1.8 IDE Secondary Control Block IO BAR (IDE_HOST_SCTLIOBAR)—Offset 1Ch

This is the IO space base address register.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**IO BAR (IOBAR):** Software programs this space with the base address of the device's IO region
1	0h RO	Reserved.
0	1h RO	**IO Space Indicator (IOSPACE):** Hardwired to 1 to identify an IO BAR.

16.1.9 IDE Bus Master Block IO BAR (IDE_HOST_BMIOBAR)—Offset 20h

This is the IO space base address register.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RW	**IO BAR (IOBAR):** Software programs this space with the base address of the device's IO region
3:2	0h RO	**IO Size (IOSIZE):** Hardwired to 0 to indicate 16B of IO space
1	0h RO	Reserved.
0	1h RO	**IO Space Indicator (IOSPACE):** Hardwired to 1 to identify an IO BAR.

16.1.10 Subsystem ID And Subsystem Vendor ID (IDE_HOST_SID_SVID)—Offset 2Ch

These registers are used to uniquely identify the add-in card or subsystem where the PCI device resides. They provide a mechanism for add-in card vendors to distinguish their add-in cards from one another even though the add-in cards may have the same PCI controller on them (and, therefore, the same Vendor ID and Device ID).

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SID):** Value of this field is vendor-specific. This is written by BIOS. No hardware action will be taken on this value. Implementation Note: The Write-Once lock must be implemented per field. SID should have its own lock.
15:0	8086h RW/O	**Subsystem Vendor ID (SVID):** This field identifies the vendor of the add-in card or subsystem. This is written by BIOS. No hardware action will be taken on this value. Implementation Note: The Write-Once lock must be implemented per field. SVID should have its own lock.

16.1.11 Capabilities List Pointer (IDE_HOST_CAPP)—Offset 34h

This register contains the capabilities list pointer.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 40h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	40h RO	**Capabilities Pointer (CAPP):** Indicates the pointer for the first entry in the capabilities list which is the MSI Capability.

16.1.12 Maximum Latency, Minimum Grant, Interrupt Pin And Interrupt Line (IDE_HOST_MAXL_MING_INTP_INTL)—Offset 3Ch

This register contains the maximum latency, minumum grand, interrupt pin and interrupt level registers.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	**Maximum Latency (MAXL):** Not implemented. Hardwired to 0.
23:16	0h RO	**Minimum Grant (MING):** Not implemented. Hardwired to 0.
15:8	0h RO/V	**Interrupt Pin (INTP):** This register specifies which interrupt pin IDE uses in PCI interrupt mode. Value Decoding 00h The function does NOT use an interrupt pin. 01h INTA 02h INTB 03h INTC 04h INTD 05h - FFh Reserved. Note: this field shadows the IDEHIPINR.IPIN field in the PTIO Host private CR space which is configured by BIOS over IOSF SB.
7:0	0h RW	**Interrupt Line (INTL):** This register is used to communicate interrupt line routing information. POST software will write the routing information into this register as it initializes and configures the system. The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value, rather it is used by device drivers and operating systems. Device drivers and operating systems can use this information to determine priority and vector information. Values in this register are system architecture specific.

16.1.13 MSI Message Control, Next Pointer And Capability ID (IDE_HOST_MSIMC_MSINP_MSICID)—Offset 40h

This register contains the MSI message control, next pointer And capability ID values.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 805005h

Bit Range	Default and Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RO	**Per Vector Masking Capable (PVMC):** Not implemented. Hardwired to 0 to indicate the function does NOT support MSI per-vector masking.
23	1h RO	**64 Bit Address Capable (XAC):** Hardwired to 1 to indicate the function is capable of sending a 64-bit message address.
22:20	0h RW	**Multiple Message Enable (MMEN):** Encoded number of interrupt vectors allocated by SW. This field is RW for software compatibility, but only one interrupt vector is ever sent by the function.
19:17	0h RO	**Multiple Message Capable (MMC):** Encoded number of interrupt vectors requested by a device. Hardwired to 0 to indicate one requested interrupt vector.
16	0h RW	**MSI Enable (MSIE):** If set, MSI interrupt delivery is enabled whereas pin-based interrupt delivery SHALL be disabled. If cleared, prior to returning the configuration write (that clears this field) completion, the function must send any pending MSI(s).
15:8	50h RO	**Next Item Pointer (NP):** Indicates the pointer for the next entry in the capabilities list. Hardwired to 50h to point to the PM Capability list
7:0	5h RO	**Capability ID (CID):** Hardwired to 05h to indicate the linked list item as the MSI Capability registers

16.1.14 MSI Message Address (IDE_HOST_MSIMA)—Offset 44h

This register contains the MSI message address value.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**Message Address (MA):** 32-bit DW-aligned MSI message address.
1:0	0h RO	Reserved.

16.1.15 MSI Message Upper Address (IDE_HOST_MSIMUA)—Offset 48h

This register contains the MSI message upper address value.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Message Upper Address (MUA):** Upper 32-bit of a 64-bit DW-aligned MSI message address.

16.1.16 MSI Message Data (IDE_HOST_MSIMD)—Offset 4Ch

This register contains the MSI message data register.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Message Data (MD):** MSI Message Data

16.1.17 Power Management Capabilities, Next Pointer And Capability ID (IDE_HOST_PMCAP_PMNP_PMCID)—Offset 50h

This register contains the power management capabilities, next pointer And capability ID values.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 230001h

Bit Range	Default and Access	Field Name (ID): Description
31:27	0h RO	**PME Support (PMES):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(27) X XXX1b - PME# can be asserted from D0 bit(28) X XX1Xb - PME# can be asserted from D1 bit(29) X X1XXb - PME# can be asserted from D2 bit(30) X 1XXXb - PME# can be asserted from D3hot bit(31) 1 XXXXb - PME# can be asserted from D3cold
26	0h RO	**D2 Support (D2S):** Hardwired to 0 to indicate that this device does not support D2
25	0h RO	**D1 Support (D1S):** Hardwired to 0 to indicate that this device does not support D1
24:22	0h RO	**Aux Current (AUXC):** Not implemented. Hardwired to 0.
21	1h RO	**Device Specific Initialization (DSI):** indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. A 1 indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state. Hardwired to 1 to indicate Device Specific Initialization is required.
20	0h RO	Reserved.
19	0h RO	**PME Clock (PMECLK):** Not implemented. Hardwired to 0.
18:16	3h RO	**Version (VER):** Hardwired to value of 011b indicates that this function complies with rev 1.2 of PCI Power Management Interface Spec
15:8	0h RO	**Next Item Pointer (NP):** Indicates the pointer for the next entry in the capabilities list. Hardwired to 0 to indicate no more linked list item.
7:0	1h RO	**Capability ID (CID):** Hardwired to 01h to indicate the linked list item as the PCI Power Management registers

16.1.18 Power Management Data, Control/Status Register Bridge Support Extensions, Control And Status (IDE_HOST_PMD_PMCSRBSE_PMCSR)—Offset 54h

This register contains the power management data, control and status register bridge support extensions, control and status registers.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 2

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	**Data (DATA):** Not implemented. Hardwired to 0.
23:16	0h RO	**Control/Status Register Bridge Support Extensions (CSRBSE):** Not implemented. Hardwired to 0.
15	0h RO	**PME Status (PMESTS):** This bit is set when the function would normally assert the PME signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the function to stop asserting a PME (if enabled). Writing a 0 has no effect. If the function supports PME from D3cold, then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded. Not implemented. Hardwired to 0.
14:13	0h RO	**Data Scale (DS):** Not implemented. Hardwired to 0.
12:9	0h RO	**Data Select (DSEL):** Not implemented. Hardwired to 0.
8	0h RO	**PME Enable (PMEEN):** A 1 enables the function to assert PME. When 0, PME assertion is disabled. This bit defaults to 0 if the function does not support PME generation from D3cold. If the function supports PME from D3cold then this bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded. Not implemented. Hardwired to 0.
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NSR):** When set to 1, this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PWRST):** This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below: 00b - D0 01b - D1 10b - D2 11b - D3hot If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs.

17 Keyboard and Text (KT) (D22:F3)

17.1 Keyboard and Text (KT) PCI Configuration Registers Summary

Table 17-1. Summary of Keyboard and Text (KT) PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID And Vendor ID (KT_HOST_DID_VID)—Offset 0h	XXXX8086h
4h	7h	Status And Command (KT_HOST_STS_CMD)—Offset 4h	B00000h
8h	Bh	Class Code And Revision ID (KT_HOST_CC_RID)—Offset 8h	70002XXh
Ch	Fh	BIST, Header Type, Latency Timer, And Cache Line Size (KT_HOST_BIST_HTYPE_LT_CLS)—Offset Ch	800000h
10h	13h	KT IO BAR (KT_HOST_IOBAR)—Offset 10h	1h
14h	17h	KT Memory BAR (KT_HOST_MEMBAR)—Offset 14h	0h
28h	2Bh	Cardbus CIS Pointer (KT_HOST_CCP)—Offset 28h	0h
2Ch	2Fh	Subsystem ID And Subsystem Vendor ID (KT_HOST_SID_SVID)—Offset 2Ch	8086h
30h	33h	Expansion ROM Base Address (KT_HOST_XRBAR)—Offset 30h	0h
34h	37h	Capabilities List Pointer (KT_HOST_CAPP)—Offset 34h	40h
3Ch	3Fh	Maximum Latency, Minimum Grant, Interrupt Pin And Interrupt Line (KT_HOST_MAXL_MING_INTP_INTL)—Offset 3Ch	0h
40h	43h	MSI Message Control, Next Pointer And Capability ID (KT_HOST_MSIMC_MSINP_MSICID)—Offset 40h	805005h
44h	47h	MSI Message Address (KT_HOST_MSIMA)—Offset 44h	0h
48h	4Bh	MSI Message Upper Address (KT_HOST_MSIMUA)—Offset 48h	0h
4Ch	4Fh	MSI Message Data (KT_HOST_MSIMD)—Offset 4Ch	0h
50h	53h	Power Management Capabilities, Next Pointer And Capability ID (KT_HOST_PMCAP_PMNP_PMCID)—Offset 50h	230001h
54h	57h	Power Management Data, Control/Status Register Bridge Support Extensions, Control And Status (KT_HOST_PMD_PMCSRBSE_PMCSR)—Offset 54h	8h

17.1.1 Device ID And Vendor ID (KT_HOST_DID_VID)—Offset 0h

This register contains the device ID and vendor ID values.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 22
Function: 3

Default: XXXX8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	RO/V	**Device ID (DID):** This field identifies the particular device. Refer the Device and Version ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor ID (VID):** This field identifies the manufacturer of the device. The value of 0x8086 indicates Intel.

17.1.2 Status And Command (KT_HOST_STS_CMD)—Offset 4h

This register contins the PCI status and command registers.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: B00000h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	**Detected Parity Error (DPE):** Not implemented. Hardwired to 0.
30	0h RO	**Signaled System Error (SSE):** Not implemented. Hardwired to 0.
29	0h RW/1C/V	**Received Master Abort (RMA):** This bit must be set by a master device whenever its transaction (except for Special Cycle) is completed with Unsupported Request Completion Status (a.k.a. Master-Abort). All master devices must implement this bit.
28	0h RW/1C/V	**Received Target Abort (RTA):** This bit must be set by a master device whenever its transaction is completed with Completer Abort Completion Status (a.k.a. Target-Abort). All master devices must implement this bit.
27	0h RW/1C/V	**Signaled Target Abort (STA):** This bit must be set by a target device whenever it completes a Posted or Non-Posted transaction with a Completer Abort (a.k.a. Target-Abort) error. Devices that will never signal Completer Abort (a.k.a. Target-Abort) do not need to implement this bit.
26:25	0h RO	**Devsel Timing (DEVT):** These bits encode the timing of DEVSEL#. There are three allowable timings for assertion of DEVSEL# as described below: 00b: fast; 01b: medium; 10b: slow; 11b: reserved. These bits are read-only and must indicate the slowest time that a device asserts DEVSEL# for any bus command except Configuration Read and Configuration Write. Hardwired to 00b.
24	0h RO	**Master Data Parity Error (MDPE):** Not implemented. Hardwired to 0.
23	1h RO	**Fast Back To Back Capable (FBTBC):** This bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. This bit can be set to 1 if the device can accept these transactions and must be set to 0 otherwise. Hardwired to 1.
22	0h RO	Reserved.
21	1h RO	**66 Mhz Capable (MCAP):** This bit indicates whether or not this device is capable of running at 66 MHz. A value of 0 indicates 33 MHz. A value of 1 indicates that the device is 66 MHz capable. Hardwired to 1.

Bit Range	Default and Access	Field Name (ID): Description
20	1h RO	**Capabilities List (CAPL):** This optional read-only bit indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. A value of zero indicates that no New Capabilities linked list is available. A value of one indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities.
19	0h RO	**Interrupt Status (INTS):** This read-only bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. Read-only and hardwired to 0 for a device that does NOT support pin-based interrupt.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTD):** This bit disables the device/function from asserting INTx#. A value of 0 enables the assertion of its INTx# signal. A value of 1 disables the assertion of its INTx# signal. This bit's state after RST# is 0.
9	0h RO	**Fast Back To Back Enable (FBTBEN):** Not implemented. Hardwired to 0.
8	0h RO	**System Error Enable (SERREN):** Not implemented. Hardwired to 0.
7	0h RO	Reserved.
6	0h RO	**Parity Error Response (PERRR):** Not implemented. Hardwired to 0.
5	0h RO	**VGA Palette Snoop (VGAPS):** Not implemented. Hardwired to 0.
4	0h RO	**Memory Write And Invalidate Enable (MWRIEN):** Not implemented. Hardwired to 0.
3	0h RO	**Special Cycles (SPCYC):** Not implemented. Hardwired to 0.
2	0h RW	**Bus Master Enable (BME):** Controls the ability of a PCI device to issue Memory and I/O Read/Write Requests, and the ability of a PCI bridge to forward Memory and I/O Read/Write Requests in the Upstream direction. Devices: When this bit is Set, the PCI device function is allowed to issue Memory or I/O Requests. When this bit is Clear, the PCI device function is not allowed to issue any Memory or I/O Requests. Note that as MSI/MSI-X interrupt Messages are in-band memory writes, setting the Bus Master Enable bit to 0b disables MSI/MSI-X interrupt Messages as well. Requests other than Memory or I/O Requests are not controlled by this bit. Default value of this bit is 0b. This bit is hardwired to 0b if a PCI device function does not generate Memory or I/O Requests. Bridges: This bit controls forwarding of Memory or I/O Requests by a bridge in the Upstream direction. When this bit is 0b, Memory and I/O Requests received at the Downstream side of a bridge must be handled as Unsupported Requests (UR), and for Non-Posted Requests a Completion with UR completion status must be returned. This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O Requests is not controlled by this bit. Default value of this bit is 0b.
1	0h RW	**Memory Space Enable (MSE):** Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. State after RST# is 0.
0	0h RW	**IO Space Enable (IOSE):** Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after RST# is 0.

17.1.3 Class Code And Revision ID (KT_HOST_CC_RID)—Offset 8h

This register contains the class code and revision ID values.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 70002XXh

Bit Range	Default and Access	Field Name (ID): Description
31:24	7h RO	**Base Class Code (BCC):** Identifies the Base Class Code of an external 16550-compatible serial controller device driver.
23:16	0h RO	**Sub-Class Code (SCC):** Identifies the Sub-Class Code of an external 16550-compatible serial controller device driver.
15:8	2h RO	**Programming Interface (PI):** Identifies the Programming Interface of an external 16550-compatible serial controller device driver.
7:0	-- RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

17.1.4 BIST, Header Type, Latency Timer, And Cache Line Size (KT_HOST_BIST_HTYPE_LT_CLS)—Offset Ch

This register contains the BIST, header type, latency timer, and cache line size values.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 800000h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	**Built In Self Test (BIST):** Not implemented. Hardwired to 0.
23	1h RO/V	**Header Type 1 (HTYPE1):** This bit identifies whether or not the device contains multiple functions. - If the bit is 0, then the device is single function. - If the bit is 1, then the device has multiple functions.
22:16	0h RO	**Header Type 0 (HTYPE0):** This field identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space). - The encoding 00h specifies the non-bridge Configuration Space Header. - The encoding 01h specifies the PCI-to-PCI bridge Configuration Space Header. - The encoding 02h specifies the CardBus bridge Configuration Space Header. - All other encodings are reserved. Hardwired to 0 to identify the non-bridge Configuration Space Header.
15:8	0h RO	**Latency Timer (LT):** Not implemented. Hardwired to 0.
7:0	0h RO	**Cache Line Size (CLS):** Not implemented. Hardwired to 0.

17.1.5 KT IO BAR (KT_HOST_IOBAR)—Offset 10h

This is the IO space base address register.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RW	**IO BAR (IOBAR):** Software programs this space with the base address of the device's IO region
2	0h RO	**IO Size (IOSIZE):** Hardwired to 0 to indicate 8B of IO space
1	0h RO	Reserved.
0	1h RO	**IO Space Indicator (IOSPACE):** Hardwired to 1 to identify an IO BAR.

17.1.6 KT Memory BAR (KT_HOST_MEMBAR)—Offset 14h

This is the IO space base address register.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW	**Memory BAR (MEMBAR):** Software programs this register with the base address of the device's memory region
11:4	0h RO	**Memory Size (MEMSIZE):** Hardwired to 0 to indicate 4KB of memory space
3	0h RO	**Prefetchable (PREFETCH):** A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables. Hardwired to 0 to indicate the device's memory space as non-prefetchable.
2:1	0h RO	**Type (TYP):** Hardwired to 0 to indicate that Base register is 32 bits wide and mapping can be done anywhere in the 32-bit Memory Space.
0	0h RO	**Memory Space Indicator (MEMSPACE):** Hardwired to 0 to identify a Memory BAR.

17.1.7 Cardbus CIS Pointer (KT_HOST_CCP)—Offset 28h

This register contains the cardbus CIS pointer.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 22
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO	**Cardbus CIS Pointer (CCP):** Not implemented. Hardwired to 0.

17.1.8 Subsystem ID And Subsystem Vendor ID (KT_HOST_SID_SVID)—Offset 2Ch

These registers are used to uniquely identify the add-in card or subsystem where the PCI device resides. They provide a mechanism for add-in card vendors to distinguish their add-in cards from one another even though the add-in cards may have the same PCI controller on them (and, therefore, the same Vendor ID and Device ID).

Access Method

Type: CFG Register (Size: 32 bits)
Device: 22
Function: 3

Default: 8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SID):** Value of this field is vendor-specific. This is written by BIOS. No hardware action will be taken on this value. Implementation Note: The Write-Once lock must be implemented per field. SID should have its own lock.
15:0	8086h RW/O	**Subsystem Vendor ID (SVID):** This field identifies the vendor of the add-in card or subsystem. This is written by BIOS. No hardware action will be taken on this value. Implementation Note: The Write-Once lock must be implemented per field. SVID should have its own lock.

17.1.9 Expansion ROM Base Address (KT_HOST_XRBAR)—Offset 30h

This register contains the expansion read-only memory base address.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 22
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO	**Expansion ROM Base Address (XRBAR):** Not implemented. Hardwired to 0.

17.1.10 Capabilities List Pointer (KT_HOST_CAPP)—Offset 34h

This register contains the capabilities list pointer.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 40h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	40h RO	**Capabilities Pointer (CAPP):** Indicates the pointer for the first entry in the capabilities list which is the MSI Capability.

17.1.11 Maximum Latency, Minimum Grant, Interrupt Pin And Interrupt Line (KT_HOST_MAXL_MING_INTP_INTL)—Offset 3Ch

This register contains the maximum latency, minimum grand, interrupt pin and interrupt level registers.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	**Maximum Latency (MAXL):** Not implemented. Hardwired to 0.
23:16	0h RO	**Minimum Grant (MING):** Not implemented. Hardwired to 0.
15:8	0h RO/V	**Interrupt Pin (INTP):** This register specifies which interrupt pin KT uses in PCI interrupt mode. Value Decoding 00h The function does NOT use an interrupt pin. 01h INTA 02h INTB 03h INTC 04h INTD 05h - FFh Reserved. Note: this field shadows the KTHIPINR.IPIN field in the PTIO Host private CR space which is configured by BIOS over IOSF SB.
7:0	0h RW	**Interrupt Line (INTL):** This register is used to communicate interrupt line routing information. POST software will write the routing information into this register as it initializes and configures the system. The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value, rather it is used by device drivers and operating systems. Device drivers and operating systems can use this information to determine priority and vector information. Values in this register are system architecture specific.

17.1.12 MSI Message Control, Next Pointer And Capability ID (KT_HOST_MSIMC_MSINP_MSICID)—Offset 40h

This register contains the MSI message control, next pointer And capability ID values.

Access Method

Type: CFG Register (Size: 32 bits)

Device: 22

Function: 3

Default: 805005h

Bit Range	Default and Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RO	**Per Vector Masking Capable (PVMC):** Not implemented. Hardwired to 0 to indicate the function does NOT support MSI per-vector masking.
23	1h RO	**64 Bit Address Capable (XAC):** Hardwired to 1 to indicate the function is capable of sending a 64-bit message address.
22:20	0h RW	**Multiple Message Enable (MMEN):** Encoded number of interrupt vectors allocated by SW. This field is RW for software compatibility, but only one interrupt vector is ever sent by the function.
19:17	0h RO	**Multiple Message Capable (MMC):** Encoded number of interrupt vectors requested by a device. Hardwired to 0 to indicate one requested interrupt vector.

Bit Range	Default and Access	Field Name (ID): Description
16	0h RW	**MSI Enable (MSIE):** If set, MSI interrupt delivery is enabled whereas pin-based interrupt delivery SHALL be disabled. If cleared, prior to returning the configuration write (that clears this field) completion, the function must send any pending MSI(s).
15:8	50h RO	**Next Item Pointer (NP):** Indicates the pointer for the next entry in the capabilities list. Hardwired to 50h to point to the PM Capability list
7:0	5h RO	**Capability ID (CID):** Hardwired to 05h to indicate the linked list item as the MSI Capability registers

17.1.13 MSI Message Address (KT_HOST_MSIMA)—Offset 44h

This register contains the MSI message address value.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**Message Address (MA):** 32-bit DW-aligned MSI message address.
1:0	0h RO	Reserved.

17.1.14 MSI Message Upper Address (KT_HOST_MSIMUA)—Offset 48h

This register contains the MSI message upper address value.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Message Upper Address (MUA):** Upper 32-bit of a 64-bit DW-aligned MSI message address.

17.1.15 MSI Message Data (KT_HOST_MSIMD)—Offset 4Ch

This register contains the MSI message data register.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Message Data (MD):** MSI Message Data

17.1.16 Power Management Capabilities, Next Pointer And Capability ID (KT_HOST_PMCAP_PMNP_PMCID)—Offset 50h

This register contains the power management capabilities, next pointer And capability ID values.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 230001h

Bit Range	Default and Access	Field Name (ID): Description
31:27	0h RO	**PME Support (PMES):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(27) X XXX1b - PME# can be asserted from D0 bit(28) X XX1Xb - PME# can be asserted from D1 bit(29) X X1XXb - PME# can be asserted from D2 bit(30) X 1XXXb - PME# can be asserted from D3hot bit(31) 1 XXXXb - PME# can be asserted from D3cold
26	0h RO	**D2 Support (D2S):** Hardwired to 0 to indicate that this device does not support D2
25	0h RO	**D1 Support (D1S):** Hardwired to 0 to indicate that this device does not support D1
24:22	0h RO	**Aux Current (AUXC):** Not implemented. Hardwired to 0.
21	1h RO	**Device Specific Initialization (DSI):** indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. A 1 indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state. Hardwired to 1 to indicate Device Specific Initialization is required.
20	0h RO	Reserved.
19	0h RO	**PME Clock (PMECLK):** Not implemented. Hardwired to 0.

Bit Range	Default and Access	Field Name (ID): Description
18:16	3h RO	**Version (VER):** Hardwired to value of 011b indicates that this function complies with rev 1.2 of PCI Power Management Interface Spec
15:8	0h RO	**Next Item Pointer (NP):** Indicates the pointer for the next entry in the capabilities list. Hardwired to 0 to indicate no more linked list item.
7:0	1h RO	**Capability ID (CID):** Hardwired to 01h to indicate the linked list item as the PCI Power Management registers

17.1.17 Power Management Data, Control/Status Register Bridge Support Extensions, Control And Status (KT_HOST_PMD_PMCSRBSE_PMCSR)—Offset 54h

This register contains the power management data, control and status register bridge support extensions, control and status registers.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 22
Function: 3

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	**Data (DATA):** Not implemented. Hardwired to 0.
23:16	0h RO	**Control/Status Register Bridge Support Extensions (CSRBSE):** Not implemented. Hardwired to 0.
15	0h RO	**PME Status (PMESTS):** This bit is set when the function would normally assert the PME signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the function to stop asserting a PME (if enabled). Writing a 0 has no effect. If the function supports PME from D3cold, then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded. Not implemented. Hardwired to 0.
14:13	0h RO	**Data Scale (DS):** Not implemented. Hardwired to 0.
12:9	0h RO	**Data Select (DSEL):** Not implemented. Hardwired to 0.
8	0h RO	**PME Enable (PMEEN):** A 1 enables the function to assert PME. When 0, PME assertion is disabled. This bit defaults to 0 if the function does not support PME generation from D3cold. If the function supports PME from D3cold then this bit is sticky and must be explicitly cleared by the operating system each time it is initially loaded. Not implemented. Hardwired to 0.
7:4	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
3	1h RO	**No Soft Reset (NSR):** When set to 1, this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.
2	0h RO	Reserved.
1:0	0h RW	**Power State (PWRST):** This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below: 00b - D0 01b - D1 10b - D2 11b - D3hot If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs.

18 USB Interface (D20: F0)

18.1 xHCI Configuration Registers Summary

Table 18-1. Summary of xHCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	Vendor ID (VID)—Offset 0h	8086h
2h	3h	Device ID (DID)—Offset 2h	XXXXh
4h	5h	Command Reg (CMD)—Offset 4h	0h
6h	7h	Device Status (STS)—Offset 6h	290h
8h	8h	Revision ID (RID)—Offset 8h	XXh
9h	9h	Programming Interface (PI)—Offset 9h	30h
Ah	Ah	Sub Class Code (SCC)—Offset Ah	3h
Bh	Bh	Base Class Code (BCC)—Offset Bh	Ch
Dh	Dh	Master Latency Timer (MLT)—Offset Dh	0h
Eh	Eh	Header Type (HT)—Offset Eh	80h
10h	17h	Memory Base Address (MBAR)—Offset 10h	4h
2Ch	2Dh	USB Subsystem Vendor ID (SSVID)—Offset 2Ch	0h
2Eh	2Fh	USB Subsystem ID (SSID)—Offset 2Eh	0h
34h	34h	Capabilities Pointer (CAP_PTR)—Offset 34h	70h
3Ch	3Ch	Interrupt Line (ILINE)—Offset 3Ch	0h
3Dh	3Dh	Interrupt Pin (IPIN)—Offset 3Dh	0h
40h	43h	XHC System Bus Configuration 1 (XHCC1)—Offset 40h	3401FDh
44h	47h	XHC System Bus Configuration 2 (XHCC2)—Offset 44h	3FC688h
50h	53h	Clock Gating (XHCLKGTEN)—Offset 50h	FDF6D3Fh
58h	5Bh	Audio Time Synchronization (AUDSYNC)—Offset 58h	0h
60h	60h	Serial Bus Release Number (SBRN)—Offset 60h	31h
61h	61h	Frame Length Adjustment (FLADJ)—Offset 61h	60h
62h	62h	Best Effort Service Latency (BESL)—Offset 62h	0h
70h	70h	PCI Power Management Capability ID (PM_CID)—Offset 70h	1h
71h	71h	Next Item Pointer 1 (PM_NEXT)—Offset 71h	80h
72h	73h	Power Management Capabilities (PM_CAP)—Offset 72h	C1C2h
74h	75h	Power Management Control/Status (PM_CS)—Offset 74h	8h
80h	80h	Message Signaled Interrupt CID (MSI_CID)—Offset 80h	5h
81h	81h	Next Item Pointer (MSI_NEXT)—Offset 81h	90h
82h	83h	Message Signaled Interrupt Message Control (MSI_MCTL)—Offset 82h	86h
84h	87h	Message Signaled Interrupt Message Address (MSI_MAD)—Offset 84h	0h
88h	8Bh	Message Signaled Interrupt Upper Address (MSI_MUAD)—Offset 88h	0h

Table 18-1. Summary of xHCI Configuration Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8Ch	8Dh	Message Signaled Interrupt Message Data (MSI_MD)—Offset 8Ch	0h
A4h	A7h	High Speed Configuration 2 (HSCFG2)—Offset A4h	3800h
A8h	ABh	Super Speed Configuration 1 (SSCFG1)—Offset A8h	24000h

18.1.1 Vendor ID (VID)—Offset 0h

Vendor ID

Access Method

Type: CFG Register (Size: 16 bits)
Device: 20
Function: 0

Default: 8086h

Bit Range	Default and Access	Field Name (ID): Description
15:0	8086h RO	**Vendor ID (VID):** Vendor ID

18.1.2 Device ID (DID)—Offset 2h

Device ID

Access Method

Type: CFG Register (Size: 16 bits)
Device: 20
Function: 0

Default: XXXXh

Bit Range	Default and Access	Field Name (ID): Description
15:0	-- RO/V	**Device ID (DID):** See the Device and Version ID Table in Volume 1 for the default value.

18.1.3 Command Reg (CMD)—Offset 4h

Command Reg

Access Method

Type: CFG Register (Size: 16 bits)
Device: 20
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTR_DIS):** When cleared to 0, the function is capable of generating interrupts. When 1, the function can not generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit is not affected by the interrupt enable.
9	0h RO	**Fast Back to Back Enable (FBE):** Fast Back to Back Enable
8	0h RW	**SERR# Enable (SERR):** When set to 1, the XHC is capable of generating (internally) SERR#.
7	0h RO	**Wait Cycle Control (WCC):** Wait Cycle Control
6	0h RW	**Parity Error Response (PER):** When set to 1, the XHCI Host Controller will check for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase as recommended by the XHCI specification. Note that this applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#.
5	0h RO	**VGA Palette Snoop (VPS):** VGA Palette Snoop
4	0h RO	**Memory Write Invalidate (MWI):** Memory Write Invalidate
3	0h RO	**Special Cycle Enable (SCE):** Special Cycle Enable
2	0h RW	**Bus Master Enable (BME):** When set, it allows XHC to act as a bus master. When cleared, it disable XHC from initiating transactions on the system bus.
1	0h RW	**Memory Space Enable (MSE):** This bit controls access to the XHC Memory Space registers. If this bit is set, accesses to the XHC registers are enabled. The Base Address register for the XHC should be programmed before this bit is set.
0	0h RO	**I/O Space Enable (IOSE):** Reserved as 0. Read-Only.

18.1.4 Device Status (STS)—Offset 6h

Device Status

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 290h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RW/1C	**Detected Parity Error (DPE):** This bit is set by the Intel PCH whenever a parity error is seen on the internal interface to the XHC host controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions. Software clears this bit by writing a 1 to this bit location.
14	0h RW/1C	**Signaled System Error (SSE):** This bit is set by the Intel PCH whenever it signals SERR# (internally). The SERR_EN bit (bit 8 in the Command Register) must be 1 for this bit to be set.Software clears this bit by writing a 1 to this bit location.
13	0h RW/1C	**Received Master-Abort Status (RMA):** This bit is set when XHC, as a master, receives a master-abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.

Bit Range	Default and Access	Field Name (ID): Description
12	0h RW/1C	**Received Target Abort Status (RTA):** This bit is set when XHC, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.
11	0h RW/1C	**Signaled Target-Abort Status (STA):** This bit is used to indicate when the XHC function responds to a cycle with a target abort.
10:9	1h RO	**DEVSEL# Timing Status (DEVT):** This 2-bit field defines the timing for DEVSEL# assertion. Read-Only.
8	0h RW/1C	**Master Data Parity Error Detected (MDPED):** This bit is set by the Intel PCH whenever a data parity error is detected on a XHC read completion packet on the internal interface to the XHC host controller and bit 6 of the Command register is set to 1. Software clears this bit by writing a 1 to this bit location.
7	1h RO	**Fast Back-to-Back Capable (FBBC):** Reserved as 1 Read-Only.
6	0h RO	**User Definable Features (UDF):** Reserved as 0. Read-Only.
5	0h RO	**66 MHz Capable (MC):** Reserved as 0. Read-Only.
4	1h RO	**Capabilities List (CL):** Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer.
3	0h RO/V	**Interrupt Status (INTR_STS):** This read-only bit reflects the state of this function's interrupt at the input of the enable/disable logic. This bit is a 1 when the interrupt is asserted. This bit will be 0 when the interrupt is deasserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
2:0	0h RO	Reserved.

18.1.5 Revision ID (RID)—Offset 8h

Revision ID

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: XXh

Bit Range	Default and Access	Field Name (ID): Description
7:0	-- RO/V	**Revision ID (RID):** Indicates stepping of the host controller. Refer to Device and Revision ID table in Vol1 for specific value.

18.1.6 Programming Interface (PI)—Offset 9h

Programming Interface

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 30h

Bit Range	Default and Access	Field Name (ID): Description
7:0	30h RO	**Programming Interface (PI):** A value of 30h indicates that this USB Host Controller conforms to the XHCI specification.

18.1.7 Sub Class Code (SCC)—Offset Ah

Sub Class Code

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 3h

Bit Range	Default and Access	Field Name (ID): Description
7:0	3h RO	**Sub Class Code (SCC):** A value of 03h indicates that this is a Universal Serial Bus Host Controller.

18.1.8 Base Class Code (BCC)—Offset Bh

Base Class Code

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: Ch

Bit Range	Default and Access	Field Name (ID): Description
7:0	Ch RO	**Base Class Code (BCC):** A value of 0Ch indicates that this is a Serial Bus controller.

18.1.9 Master Latency Timer (MLT)—Offset Dh

Master Latency Timer

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RO	**Master Latency Timer (MLT):** Because the XHC controller is internally implemented with arbitration on an internal interface, it does not need a master latency timer. The bits will be fixed at 0.

18.1.10 Header Type (HT)—Offset Eh

Header Type

Access Method

Type: CFG Register (Size: 8 bits)
Device: 20
Function: 0

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RO	**Multi-Function Bit (MFB):** Read only indicating single function device.
6:0	0h RO	**Configuration layout (CL):** Hardwired to 0 to indicate a standard PCI configuration layout.

18.1.11 Memory Base Address (MBAR)—Offset 10h

Value in this register will be different after the enumeration process.

Access Method

Type: CFG Register (Size: 64 bits)
Device: 20
Function: 0

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
63:16	0h RW	**Base Address (BA):** Bits (63:16) correspond to memory address signals (63:16), respectively. This gives 64 KB of relocatable memory space aligned to 64 KB boundaries.
15:4	0h RO	Reserved.
3	0h RO	**Prefetchable (PREFETCHABLE):** This bit is hardwired to 0 indicating that this range should not be prefetched.
2:1	2h RO	**Type (MBAR_TYPE):** If this field is hardwired to 00 it indicates that this range can be mapped anywhere within 32-bit address space. If this field is hardwired to 10 it indicates that this range can be mapped anywhere within 64-bit address space.
0	0h RO	**Resource Type Indicator (RTE):** This bit is hardwired to 0 indicating that the base address field in this register maps to memory space

18.1.12 USB Subsystem Vendor ID (SSVID)—Offset 2Ch

This register is modified and maintained by BIOS

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW/L	**USB Subsystem Vendor ID (SSVID):** This register, in combination with the USB Subsystem ID register, enables the operating system to distinguish each subsystem from the others.

18.1.13 USB Subsystem ID (SSID)—Offset 2Eh

This register is modified and maintained by BIOS

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW/L	**USB Subsystem ID (SSID):** BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s).

18.1.14 Capabilities Pointer (CAP_PTR)—Offset 34h

Capabilities Pointer

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 70h

Bit Range	Default and Access	Field Name (ID): Description
7:0	70h RO	**Capabilities Pointer (CAP_PTR):** This register points to the starting offset of the capabilities ranges.

18.1.15 Interrupt Line (ILINE)—Offset 3Ch

Interrupt Line

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Line (ILINE):** This data is not used by the Intel PCH. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

18.1.16 Interrupt Pin (IPIN)—Offset 3Dh

This register is modified and maintained by BIOS

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW/L	**Interrupt pin (IPIN):** Bits 7:0 reflect the Interrupt Pin assigned to the host controller by the platform (and are hardwired).

18.1.17 XHC System Bus Configuration 1 (XHCC1)—Offset 40h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 3401FDh

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/1L	**Access Control (ACCTRL):** This bit is used by BIOS to lock/unlock lockable bits. When set to '1' the write access to bits locked by this bit is disabled (locked state). When set to '0', the write access to bit locked by this bit is enabled (unlocked state). Writable once after platform reset.
30:25	0h RO	Reserved.
24	0h RW	**Master/Target Abort SERR (RMTASERR):** When set, it allows the out-of-band error reporting from the xHCI Controller to be reported as SERR# (if SERR# reporting is enabled) and thus set the STS.SSE bit.
23	0h RW/1C	**Unsupported Request Detected (URD):** Set the HW when xHCI Controller received an unsupported request posted cycle. Cleared by SW when the bit is written with value of '1'.
22	0h RW	**Unsupported Request Report Enable (URRE):** When set this bit allows the URD bit to be reported as SERR# (if SERR# reporting is enabled) and thus set the STS.SSE bit.
21:19	6h RW	**Inactivity Initiated L1 Enable (IIL1E):** If programmed to non-zero, it allows L1 power managed to be enabled after the time-out period specified. 000: Disabled 001: 32 bb_cclk 010: 64 bb_cclk 011: 128 bb_cclk 100: 256 bb_cclk 101: 512 bb_cclk 110: 1024 bb_cclk 111: 131072 bb_cclk
18	1h RW	**XHC Initiated L1 Enable (XHCIL1E):** If set, allow the XHC initiated L1 power management to be enabled.
17	0h RW	**D3 Initiated L1 Enable (D3IL1E):** If set, allow PCI device state D3 initiated L1 power management to be enables.[BR
16:12	0h RO	Reserved.
11	0h RW	**SW Assisted xHC Idle (SWAXHCI):** This bit being set will indicate xHC idleness (through SW means), which must be a '1' to allow L1 entry, and subsequently allow backbone clock to be gated. This bit is to be set by Intel xHCI driver after checking that the xHCI Controller will stay in idle state for a significant period of time, e.g. all ports disconnected. This bit can be cleared under the following conditions (see SWAXHCI Policy bits in xHC System Bus Configuration 2 register) SW: SW could write 0 to clear this bit.n HW: HW, under policy control, will clear this bit on an MMIO access to the Host Controller.n HW: HW, under policy control, will clear this bit when HW exits Idle state.
10:8	1h RW	**L23 to Host Reset Acknowledge Wait Count (L23HRAWC):** If programmed to non zero, it allows a wait period after the L23 PHY has shutdown before returning host reset acknowledge to PMC. 000: Disabled 001: 128 bb_cclk 010: 256 bb_cclk 011: 512 bb_cclk 100: 1024 bb_cclk 101: 2048 bb_cclk 110: 4096 bb_cclk 111: 131072 bb_cclk
7:6	3h RW	**Upstream Type Arbiter Grant Count Posted (UTAGCP):** Grant count for IOSF upstream L2 request type arbiter for posted type
5:4	3h RW	**Upstream Type Arbiter Grant Count Non Posted (UDAGCNP):** Grant count for IOSF upstream L2 type arbiter for non-posted type
3:2	3h RW	**Upstream Type Arbiter Grant Count Completion (UDAGCCP) (UDAGCCP):** Grant count for IOSF upstream L2 type arbiter for completion type
1:0	1h RW	**Upstream Device Arbiter Grant Count (UDAGC) (UDAGC):** Grant count for IOSF upstream L1 device arbiter

18.1.18 XHC System Bus Configuration 2 (XHCC2)—Offset 44h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 3FC688h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**OC Configuration Done (OCCFGDONE):** This bit is used by BIOS to prevent spurious switching during OC configuration. It must be set by BIOS after configuration of the OC mapping bits is complete. Once this bit is set, OC mapping shall not be changed by SW.
30	0h RW	**Enable Relaxed Ordering (RO_EN):** This bit is used to assert Relaxed Ordering bit
29:28	0h RW	**MMIO Back to Back Rd/Wr Delay Count (RW_DLY_CNT):** This field controls the delay in PRIM_CLK clocks applied to the delay inserted between the MMIO Rd/Wr or Wr/Wr back to back scenarios if enabled via XHCC2[11:10] 0x0 - 64 clocks 0x1 - 128 clocks 0x2 - 256 clocks 0x3 - N/A
27:26	0h RO	Reserved.
25	0h RW	**DMA Request Boundary Crossing Control (DREQBCC):** This bit controls the boundary crossing limit of each Read/Write Request. 0: 4KB 1: 64B
24:22	0h RW	**IDMA Write Request Size Control (WRREQSZCTRL):** This bit controls the maximum size of each Write Request. 000: 128B 001: 256B 011 - 110: Reserved 111: 64B
21	1h RW	**XHC Upstream Read Relaxed Ordering Enable (XHCUPRDROE):** This policy controls the Relaxed Ordering attribute for upstream reads. 0 - xHC will clear RO for all upstream read requests. 1 - xHC will set RO for all upstream read requests.
20:14	7Fh RW	**Upstream Non-Posted Pre-Allocation (UNPPA):** This field reserves data sizes, in 64 byte chunks, of the downstream completion resource. This value is zero based. 000000 - 111111: Pre-allocate 64 bytes - 4096 bytes If set greater than the default allows over-allocation If set less than default allows under-allocation Only allowed to be programmed when BME = 0 and no outstanding downstream completion
13:12	0h RW	**SW Assisted xHC Idle Policy (SWAXHCIP):** Note: Irrespective of the setting of this field, SW write of 0 to SWAXHCI will clear the bit. 00b (default): xHC HW clears SWAXHCI bit upon MMIO access to Host Controller OR xHC HW exits Idle state 01b: xHC HW does not autonomously clear SWAXHCI bit. The bit could be cleared only by SW. 10b: xHC HW clears SWAXHCI upon MMIO acces to Host Controller. xHC HW exit from Idle state will not clear SWAXHCI. 11b: Reserved
11	0h RW	**MMIO Read After MMIO Write Delay Disable (RAWDD):** This field controls delay on MMIO Read after MMIO Write. 0b (Default): Delay MMIO Read after MMIO Write 1b: Do not delay MMIO Read after MMIO Write Note that this delay applies after the second of the two DW writes in the case where the IOSF Gasket splits a QW write into two single DW writes to the IP.
10	1h RW	**MMIO Write After MMIO Write Delay Enable (WAWDE):** This field controls delay on MMIO Write after previous MMIO Write. 0b (Default): Do not delay MMIO Write after previous MMIO Write 1b: Delay MMIO Write after previous MMIO Write Note that the delay count does not apply on the second of the two DW writes that are generated by IOSF Gasket when it splits a QW write into two. In other words, the second of the two DW writes could happen without any delay with respect to the first DW write. The delay count, in this case, will apply after the second of the two DW writes.

Bit Range	Default and Access	Field Name (ID): Description
9:8	2h RW	**SW Assisted Cx Inhibit (SWACXIHB):** This field controls how the DMI L1 inhibit signal from USB 3.1 to PMC will behave. 00: Never inhibit Cx 01: Inhibit Cx when Isochronous Endpoint is active (PPT Behavior) 10: Inhibit Cx when Periodic Active as defined in 40.4.3.2. 111: Always inhibit Cx
7:6	2h RW	**SW Assisted DMI L1 Inhibit (SWADMIL1IHB):** This field controls how the DMI L1 inhibit signal from USB 3.1 to DMI will behave.00: Never inhibit DMI L1.01: Inhibit DMI L1 when Isochronous Endpoint is active (PPT Behavior).10: Inhibit DMI L1 when Priodic Active as defined in 40.4.3.2.1.11: Inhibit DMI L1 if XHCC1.SWAXHCI = 0.
5:3	1h RW	**L1 Force P2 Clock Gating Wait Count (L1FP2CGWC):** If programmed to non zero, it allows L1 force P2 gating off the clock to be delayed after the time-out period specified. If wake up event is detected before the time-out, pclk remains alive and trigger L1 exit as though CPU host is causing the wake, 000: Disabled 001: 128 bb_cclk 010: 256 bb_cclk 011: 512 bb_cclk 100: 1024 bb_cclk 101: 2048 bb_cclk 110: 4096 bb_cclk 111: 131072 bb_cclk
2:0	0h RW	**Read Request Size Control (RDREQSZCTRL):** Read Request Size Control: This bit controls the maximum size of each Read Request. 000: 128B 001: 256B 010: 512B 011 - 110: Reserved 111: 64B

18.1.19 Clock Gating (XHCLKGTEN)—Offset 50h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: FDF6D3Fh

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**Enable Frame Clk Gating When Active Periodic EPs On Scheduler (PRDCEP_FRCLK_GATEEN):** Enable Frame Clk Gating When Active Periodic EPs On Scheduler
30	0h RW	**Extend EU3S To U2 (EXTD_EU3S_TO_U2):** Extend EU3S To U2 to gate frame_clk
29	0h RO	Reserved.
28	0h RW	**Nak'ing USB2.0 EPs for Backbone Clock Gating and PLL Shutdown (NUEFBCGPS):** This field controls whether Naking USB2.0 EPs, once in Naking low priority schedule, should be considered as active for the considerations for backbone clock gating and PLL shutdown or not. 0: Naking USB2.0 EPs are not considered to be active for Backbone Clock Gating and PLL Shutdown evaluation. 1: Naking USB2.0 EPs are considered to be active for Backbone clock gating and PLL shutdown evaluation.
27	1h RW	**SRAM Power Gate Enable (SRAMPGTEN):** This register enables the SRAM Power Gating when PLL shutdown conditions for all clock domains have been met 0 - Disallow SRAM Power Gating. 1 - Allow SRAM Power Gating
26	1h RW	**SS Link PLL Shutdown Enable (SSLSE):** This register enables the SS P3 state to be exposed to PXP PLL Shutdown conditions on behalf of all USB SS Ports on top of trunk clock gating. 0 - P3 state NOT allowed to result in PXP PLL shutdown. 1- P3 state allowed to result in PXP PLL shutdown
25	1h RW	**USB2 PLL Shutdown Enable (USB2PLLSE):** When set, this bit allows USB2 PLL to be shutdown when HS Link trunk clock is gated, and xHC can tolerate PLL spin up time for subsequent clock request.
24	1h RW	**IOSF Sideband Trunk Clock Gating Enable (IOSFSTCGE):** When set, this bit allows the IOSF sideband clock trunk to be gated when idle conditions are met.

Bit Range	Default and Access	Field Name (ID): Description
23:20	Dh RW	**HS Backbone PXP Trunk Clock Gate Enable (HSTCGE):** This register determines the HS Ux state(s) which will be exposed to Backbone PXP trunk gating of core clock. Uy is a state allowed to result in trunk gating when ss_tcg_ux_en(x) is asserted. (0) ==) U0 or deeper (1) ==) NA (no support for U1) (2) ==) U2 (L1) or deeper (3) ==) U3 (L2) or deeper
19:16	Fh RW	**SS Backbone PXP Trunk Clock Gate Enable (SSTCGE):** This register determines the SS Ux state(s) which will be exposed to Backbone PXP trunk gating of core clock. Uy is a state allowed to result in trunk gating when ss_tcg_ux_en(x) is asserted. (0) ==> U0 or deeper (1) ==> U1 or deeper (2) ==> U2 or deeper (3) ==> U3 or deeper
15	0h RW	**XHC Ignore_EU3S (XHCIGEU3S):** This register determines if the xHC will use the EU3S as a condition to allow for Frame timer gating. 0 - xHC may allow frame timer to be gated when EU3S is set and all ports are in the required state. 1 - xHC may allow frame timer to be gated regardless of EU3S.
14	1h RW	**XHC Frame Timer Clock Shutdown Enable (XHCFTCLKSE):** This register determines if the xHC will allow the frame timer clock to be gated. 0 - xHC will not allow ICC PLL 96MHz output to be shutdown thus keeping the frame timer running. 1 - xHC will allow ICC PLL 96MHz output to be shutdown under specific conditions.
13	1h RW	**XHC Backbone PXP Trunk Clock Gate In Presence of ISOCH EP (XHCBBTCGIPISO):** This register controls the policy on allowing Backbone PXP trunk clock gate in the presence of IDLE ISOCH EP s with active DB. Allows the periodic active to be used in enabling Backbone PXP trunk clock gating of core clock. 0 - Trunk gate of core clock is not allowed when ISOCH EP DB is set and ISOCH EP s are idle. 1 - Allow trunk gate of core clock when ISOCH EP DB is set and ISOCH EP s are idle.
12	0h RW	**XHC HS Backbone PXP Trunk Clock Gate U2 non RWE (XHCHSTCGU2NRWE):** This register controls the policy on allowing Backbone PXP trunk gating of core clock when there is at least 1 non Remote Wake Enabled HS Port in U2. 0 - Prevent trunk gate of core clock when a non RWE HS Port is in U2. 1 - Allow trunk gate of core clock when a non RWE HS Port is in U2.
11:10	3h RW	**XHC USB2 PLL Shutdown Lx Enable (XHCUSB2PLLSDLE):** This register determines the HS Link state(s) which will be exposed to USB2 PLL Shutdown conditions on behalf of all USB2 HS Ports. Ly is a state allowed to result in USB2 PLL Shutdown when en(x) is asserted. (0) ==> L1 or deeper (1) ==> L2 or deeper
9:8	1h RW	**HS Backbone PXP PLL Shutdown Ux Enable (HSUXDMIPLLSE):** This register determines the Ux state(s) which will be exposed to PXP PLL Shutdown conditions. PLL Shutdown is allowed in: 00b Disabled (Link states shall be disabled for DMI PLL shutdown) 01b U0 or conditions for 10b setting. 10b U2 or conditions for 11b setting. 10b U3, Disconnected, Disabled or Powered-Off.
7:5	1h RW	**SS Backbone PXP PLL Shutdown Ux Enable (SSPLLSUE):** This register determines the Ux state(s) which will be exposed to DMI PLL Shutdown conditions. PLL Shutdown is allowed in: 000b Disabled (Link states shall be ignored for DMI PLL shutdown). 001b U0 or conditions for 010b setting. 010b U1 or conditions for 011b setting. 011b U2 or conditions for 100b setting. 100b U3, Disconnected, Disabled or Powered-Off
4	1h RW	**XHC Backbone Local Clock Gating Enable (XHCBLCGE):** When set, this bit allows XHCI Controller IP backbone clock to be locally gated when idle conditions are met.
3	1h RW	**HS Link Trunk Clock Gating Enable (HSLTCGE):** When set, this bit allows High Speed Link control's 480 MHz and its 48/60 MHz link clock trunk to be gated when idle conditions are met.
2	1h RW	**SS Link Trunk Clock Gating Enable (SSLTCGE):** When set, this bit allows the SuperSpeed Link control's 250 MHz and its divided 125 MHz link clock trunk to ge gated when idle conditions are met.
1	1h RW	**IOSF Backbone Trunk Clock Gating Enable (IOSFBTCGE):** When set, this bit allows the IOSF backbone clock trunk to be gated when idle conditions are met.
0	1h RW	**IOSF Gasket Backbone Local Clock Gating Enable (IOSFBLCGE):** When set, this bit allows the IOSF Gasket backbone clock to be locally gated when idle conditions are met.

18.1.20 Audio Time Synchronization (AUDSYNC)—Offset 58h

This 32 bit register is used for audio stream synchronization across different devices. Global signal sample_now captures a value in AUDSYNC register.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:16	0h RO/V	**Captured Frame List Current Index/Frame Number (CMFI):** The value in this register is updated in response to sample_now signal. Bits (29:16) reflect state of bits (13:0) of FRINDEX
15:13	0h RO	Reserved.
12:0	0h RO/V	**Captured Micro-frame BLIF (CMFB):** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done in FLA.

18.1.21 Serial Bus Release Number (SBRN)—Offset 60h

Serial Bus Release Number

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 31h

Bit Range	Default and Access	Field Name (ID): Description
7:0	31h RO	**Serial Bus Release Number (SBRN):** A value of 30h indicates that this controller follows USB release 3.0.

18.1.22 Frame Length Adjustment (FLADJ)—Offset 61h

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit in the USBSTS register is a one. Changing value of this register while the host controller is operating yields undefined results.

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 60h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO	Reserved.
6	1h RO	**No Frame Length Timing Capability (NO_FRAME_LENGTH_TIMING_CAP):** This flag is set to 1 to indicate that the host controller does not support a programmable Frame Length Timing Value field.
5:0	20h RO	**Frame Length Timing Value (FLTV):** SOF (micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (number of High Speed bit times) FLADJ Value (decimal) (decimal) 59488 0 (00h) 59504 1 (01h) 59520 2 (02h) ... 59984 31 (1Fh) 60000 32 (20h) ... 60480 62 (3Eh) 60496 63 (3Fh) Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (# High Speed bit times) FLADJ Value

18.1.23 Best Effort Service Latency (BESL)—Offset 62h

Bset Effort Service Latency.

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:4	0h RW/L	**Default Best Effort Service Latency Deep (DBESLD):** If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESLD field. This is programmed by BIOS based on platform parameters.
3:0	0h RW/L	**Default Best Effort Service Latency (DBESL):** If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESL field. This is programmed by BIOS based on platform parameters.

18.1.24 PCI Power Management Capability ID (PM_CID)—Offset 70h

PCI Power Management Capability ID

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
7:0	1h RO	**PCI Power Management Capability ID (PM_CID):** A value of 01h indicates that this is a PCI Power Management capabilities field.

18.1.25 Next Item Pointer 1 (PM_NEXT)—Offset 71h

This register is modified and maintained by BIOS

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7:0	80h RW/L	**Next Item Pointer 1 (PM_NEXT):** This register defaults to 80h, which indicates that the next capability registers begin at configuration offset 80h. This register is writable when the Access Control bit is set to '0'. This allows BIOS to effectively hide the next capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Values of: 80h implies next capability is MSI 00h implies that MSI capability is hidden. Note: This value is never expected to be programmed.

18.1.26 Power Management Capabilities (PM_CAP)—Offset 72h

Normally, this register is read-only to report capabilities to the power management software. In order to report different power management capabilities depending on the system in which the Intel PCH is used, the write access to this register is controlled by the Access Control bit (ACCTRL). The value written to this register does not affect the hardware other than changing the value returned during a read. This register is modified and maintained by BIOS

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: C1C2h

Bit Range	Default and Access	Field Name (ID): Description
15:11	18h RW/L	**PME_Support (PME_SUPPORT):** This 5-bit field indicates the power states in which the function may assert PME#. The Intel PCH XHC does not support the D1 or D2 states. For all other states, the Intel PCH XHC is capable of generating PME#. Software should never need to modify this field.
10	0h RW/L	**D2_Support (D2_SUPPORT):** The D2 state is not supported.
9	0h RW/L	**D1_Support (D1_SUPPORT):** The D1 state is not supported.

Bit Range	Default and Access	Field Name (ID): Description
8:6	7h RW/L	**Aux_Current (AUX_CURRENT):** The Intel PCH XHC reports 375mA maximum Suspend well current required when in the D3cold state. This value can be written by BIOS when a more accurate value is known.
5	0h RW/L	**DSI (DSI):** The Intel PCH reports 0, indicating that no device-specific initialization is required.
4	0h RO	Reserved.
3	0h RW/L	**PME Clock (PMECLOCK):** The Intel PCH reports 0, indicating that no PCI clock is required to generate PME#.
2:0	2h RW/L	**Version (VERSION):** The Intel PCH reports 010, indicating that it complies with Revision 1.1 of the PCI Power Management Specification.

18.1.27 Power Management Control/Status (PM_CS)—Offset 74h

Power Management Control/Status

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RW/1C	**PME_Status (PME_STATUS):** This bit is set when the Intel PCH XHC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). Writing a 0 has no effect. This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14:13	0h RO	**Data_Scale (DATA_SCALE):** The Intel PCH hardwires these bits to 00 because it does not support the associated Data register.
12:9	0h RO	**Data_Select (DATA_SELECT):** The Intel PCH hardwires these bits to 0000 because it does not support the associated Data register.
8	0h RW	**PME_En (PME_EN):** A 1 enables the Intel PCH XHC to generate an internal PME signal when PME_Status is 1. This bit must be explicitly cleared by the operating system each time it is initially loaded.
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NSR):** No_Soft_Reset - When set ("1"), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. Transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0h RO	Reserved.
1:0	0h RW	**PowerState (POWERSTATE):** This 2-bit field is used both to determine the current power state of XHC function and to set a new power state. The definition of the field values are: 00b - D0 state 11b - D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3hot state, the Intel PCH must not accept accesses to the XHC memory range, but the configuration space must still be accessible.

18.1.28 Message Signaled Interrupt CID (MSI_CID)—Offset 80h

Message Signaled Interrupt CID

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 5h

Bit Range	Default and Access	Field Name (ID): Description
7:0	5h RO	**Capability ID (CID):** Indicates that this is an MSI capability

18.1.29 Next Item Pointer (MSI_NEXT)—Offset 81h

Next Item Pointer

Access Method

Type: CFG Register
(Size: 8 bits)

Device: 20
Function: 0

Default: 90h

Bit Range	Default and Access	Field Name (ID): Description
7:0	90h RW/L	**Next Pointer (NEXT_POINTER):** Indicates that this is the last item on the capability list

18.1.30 Message Signaled Interrupt Message Control (MSI_MCTL)—Offset 82h

Message Signaled Interrupt Message Control

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 86h

Bit Range	Default and Access	Field Name (ID): Description
15:9	0h RO	Reserved.
8	0h RO	**Per-Vector Masking Capable (PVM):** Specifies whether controller supports MSI per vector masking. Not supported
7	1h RO	**64 Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages. This device is 64-bit capable.
6:4	0h RW	**Multiple Message Enable (MME):** Indicates the number of messages the controller should assert. This device supports multiple message MSI.
3:1	3h RO	**Multiple Message Capable (MMC):** Indicates the number of messages the controller wishes to assert.This field must be set by HW to reflect the number of Interrupters supported. Encoding number of Vectors requested (number of Interrupters) 000 1 001 2 010 4 011 8 100 16 101 32 110-111 Reserved
0	0h RW	**MSI Enable (MSIE):** If set to 1, MSI is enabled and the traditional interrupt pins are not used to generate interrupts. If cleared to 0, MSI operation is disabled and the traditional interrupt pins are used.

18.1.31 Message Signaled Interrupt Message Address (MSI_MAD)—Offset 84h

Message Signaled Interrupt Message Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**Addr (ADDR):** Lower DW of system specified message address, always DWORD aligned
1:0	0h RO	Reserved.

18.1.32 Message Signaled Interrupt Upper Address (MSI_MUAD)—Offset 88h

Message Signaled Interrupt Upper Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Upper Addr (UPPERADDR):** Upper DW of system specified message address.

18.1.33 Message Signaled Interrupt Message Data (MSI_MD)—Offset 8Ch

Message Signaled Interrupt Message Data

Access Method

Type: CFG Register
(Size: 16 bits)

Device: 20
Function: 0

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD(15:0)) during the data phase of the MSI memory write transaction. The Multiple Message Enable field (bits 6-4 of the Message Control register) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010 indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000, the function is not permitted to modify the message data.

18.1.34 High Speed Configuration 2 (HSCFG2)—Offset A4h

High Speed Configuration 2

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 3800h

Bit Range	Default and Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW	**PORT1_HOST_MODE_OVERRIDE (PORT1_HOST_MODE_OVERRIDE):** When set, this bit causes the Host_Device mux on port 1 to be forced into the Host mode.
17:16	0h RW	**eUSB2SEL (EUSB2SEL):** The two bits are associate with USB2 ports 1 - bit 16 and 2 - bit 2 0: Port is mapped to USB2 1: Port is mapped to eUSB2
15	0h RW	**HS ASYNC Active IN Mask (HSAAIM):** Determines if the Async Active will mask/ignore IN EP s. 0 HS ASYNC Active will include IN EP s. 1 HS ASYNC Active will mask/ignore IN EP s.
14	0h RW	**HS OUT ASYNC Active Polling EP Mask (HSOAAPEPM):** Determines if the Async Active for OUT HS/FS/LS masks/ignores EP s that are polling/PINGing (HS) due to NAK. 0 HS OUT ASYNC Active will include EP s that are polling. 1 HS OUT ASYNC Active will mask/ignore EP s that are polling.

Bit Range	Default and Access	Field Name (ID): Description
13	1h RW	**HS IN ASYNC Active Polling EP Mask (HSIAAPEPM):** Determines if the Async Active for IN HS/FS/LS masks/ignores EP s that are polling due to NAK. 0 HS IN ASYNC Active will include EP s that are polling. 1 HS IN ASYNC Active will mask/ignore EP s that are polling.
12:11	3h RW	**HS INTR IN Periodic Active Policy Control (HSIIPAPC):** Controls how the HS INTR IN periodic active is used to generate the global periodic active. This will determine how the smallest service interval among active EP s and number of active EP s are used. 0 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold OR Numb of EP Threshold values meet the requirement. 1 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold AND Numb of EP Threshold values meet the requirement. 2 Always allow HS INTR EP s to be used in the generation of the global Periodic Active indication. 3 Never allow HS INTR EP s to be used in the generation of the global Periodic Active indication
10:4	0h RW	**HS INTR IN Periodic Active Num of EP Threshold (HSIIPANEPT):** Defines the threshold used to determine if Periodic Active may include HS/FS/LS INTR IN EP active indication. If there are more than NumEPThreshold active HS/FS/LS INTR EP s then they may be included as part of the periodic active generation.
3:0	0h RW	**HS INTR IN Periodic Active Service Interval Threshold (HSIIPASIT):** Defines the Service Interval threshold used to determine if Periodic Active will include HS/FS/LS INTR IN EP active indication. If there are any active HS/FS/LS INTR EP s with a service interval less than or equal to this threshold then they may be included as part of the periodic active generation.

18.1.35 Super Speed Configuration 1 (SSCFG1)—Offset A8h

This register is modified and maintained by BIOS

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 0

Default: 24000h

Bit Range	Default and Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	1h RW	**LFPS Power Management Enable (LFPSPME):** This field provides programmability of the USB LFPS Receiver power management capability when USB3.0 ports are Disabled or in Disconnected state. 0: Do not power manage LFPS receiver. LFPS receivers are enabled in all states 1: Power manage LFPS receiver. LFPS receivers will be turned off if USB3.0 port is Disabled or Disconnected
16:15	0h RO	Reserved.
14	1h RW	**MODPHY Power Gate Enable for U2 (MPHYPGEU2):** This bit controls whether xHC will allow PHY power gating or not when a port is in U2 state. Note that this single bit controls all ports of xHC. 0b xHC shall not initiate Power Gate Request when in U2 1b xHC is enabled to initiate Power Gate Request when in U2 if power gating conditions are met.
13:0	0h RO	Reserved.

18.2 xHCI Memory Mapped Registers Summary

Table 18-2. Summary of xHCI Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	0h	Capability Registers Length (CAPLENGTH)—Offset 0h	80h
2h	3h	Host Controller Interface Version Number (HCIVERSION)—Offset 2h	110h
4h	7h	Structural Parameters 1 (HCSPARAMS1)—Offset 4h	10000840h
8h	Bh	Structural Parameters 2 (HCSPARAMS2)—Offset 8h	14200054h
Ch	Fh	Structural Parameters 3 (HCSPARAMS3)—Offset Ch	A0000Ah
10h	13h	Capability Parameters (HCCPARAMS)—Offset 10h	20007FC1h
14h	17h	Doorbell Offset (DBOFF)—Offset 14h	3000h
18h	1Bh	Runtime Register Space Offset (RTSOFF)—Offset 18h	2000h
80h	83h	USB Command (USBCMD)—Offset 80h	0h
84h	87h	USB Status (USBSTS)—Offset 84h	1h
88h	8Bh	Page Size (PAGESIZE)—Offset 88h	1h
94h	97h	Device Notification Control (DNCTRL)—Offset 94h	0h
98h	9Bh	Command Ring Low (CRCR_LO)—Offset 98h	0h
9Ch	9Fh	Command Ring High (CRCR_HI)—Offset 9Ch	0h
B0h	B3h	Device Context Base Address Array Pointer Low (DCBAAP_LO)—Offset B0h	0h
B4h	B7h	Device Context Base Address Array Pointer High (DCBAAP_HI)—Offset B4h	0h
480h	483h	Port N Status and Control USB2 (PORTSCN)—Offset 480h	2A0h
484h	487h	Port Power Management Status Aand Control USB2 (PORTPMSCN)—Offset 484h	0h
48Ch	48Fh	Port N Hardware LPM Control Register (PORTHLPMCN)—Offset 48Ch	0h
540h	543h	Port Status And Control USB3 (PORTSCXUSB3)—Offset 540h	2A0h
544h	547h	Port Power Management Status And Control USB3 (PORTPMSCX)—Offset 544h	0h
548h	54Bh	USB3 Port X Link Info (PORTLIX)—Offset 548h	0h
2000h	2003h	Microframe Index (RTMFINDEX)—Offset 2000h	0h
2020h	2023h	Interrupter x Management (IMANx)—Offset 2020h	0h
2024h	2027h	Interrupter x Moderation (IMODx)—Offset 2024h	FA0h
2028h	202Bh	Event Ring Segment Table Size x (ERSTSZx)—Offset 2028h	0h
2030h	2033h	Event Ring Segment Table Base Address Low x (ERSTBA_LOx)—Offset 2030h	0h
2034h	2037h	Event Ring Segment Table Base Address High x (ERSTBA_HIx)—Offset 2034h	0h
2038h	203Bh	Event Ring Dequeue Pointer Low x (ERDP_LOx)—Offset 2038h	0h
203Ch	203Fh	Event Ring Dequeue Pointer High x (ERDP_HIx)—Offset 203Ch	0h
3000h	3003h	Door Bell x (DBx)—Offset 3000h	0h
8000h	8003h	XECP SUPP USB2_0 (XECP_SUPP_USB2_0)—Offset 8000h	2000802h
8004h	8007h	XECP SUPP USB2_1 (XECP_SUPP_USB2_1)—Offset 8004h	20425355h
8008h	800Bh	XECP SUPP USB2_2 (XECP_SUPP_USB2_2)—Offset 8008h	30180C01h
800Ch	800Fh	XECP SUPP USB3_3 (XECP_SUPP_USB2_3)—Offset 800Ch	0h
8010h	8013h	XECP SUPP USB2_4 Full Speed (XECP_SUPP_USB2_4)—Offset 8010h	C0021h
8014h	8017h	XECP_SUPP USB2_5 Low Speed (XECP_SUPP_USB2_5)—Offset 8014h	5DC0012h
8018h	801Bh	XECP SUPP USB2_6 High Speed (XECP_SUPP_USB2_6)—Offset 8018h	1E00023h

Table 18-2. Summary of xHCI Memory Mapped Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8020h	8023h	XECP SUPP USB3_0 (XECP_SUPP_USB3_0)—Offset 8020h	3101402h
8024h	8027h	XECP SUPP USB3_1 (XECP_SUPP_USB3_1)—Offset 8024h	20425355h
8028h	802Bh	XECP SUPP USB3_2 (XECP_SUPP_USB3_2)—Offset 8028h	8000040Dh
802Ch	802Fh	XECP SUPP USB3_3 (XECP_SUPP_USB3_3)—Offset 802Ch	0h
8030h	8033h	XECP SUPP USB3_4 (XECP_SUPP_USB3_4 Super Speed)—Offset 8030h	50134h
8034h	8037h	XECP SUPP USB3_5 (XECP_SUPP_USB3_5 Super Speed Plus)—Offset 8034h	A0135h
8038h	803Bh	XECP SUPP USB3_6 (XECP_SUPP_USB3_6)—Offset 8038h	4E00126h
803Ch	803Fh	XECP SUPP USB3_7 (XECP_SUPP_USB3_7)—Offset 803Ch	9C00127h
8040h	8043h	XECP SUPP USB3_8 (XECP_SUPP_USB3_8)—Offset 8040h	13800128h
8044h	8047h	XECP SUPP USB3_9 (XECP_SUPP_USB3_9)—Offset 8044h	5B10129h
8094h	8097h	Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h	140h
80A4h	80A7h	Power Management Control (PMCTRL_REG)—Offset 80A4h	492D5094h
80B0h	80B3h	Host Controller Misc Reg (HOST_CTRL_MISC_REG)—Offset 80B0h	37Fh
80B4h	80B7h	Host Controller Misc Reg2 (HOST_CTRL_MISC_REG2)—Offset 80B4h	0h
80B8h	80BBh	Super Speed Port Enable (SSPE_REG)—Offset 80B8h	0h
80E0h	80E3h	AUX Power Management Control (AUX_CTRL_REG1)—Offset 80E0h	8080BCE0h
80ECh	80EFh	SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)—Offset 80ECh	18000C00h
80F0h	80F3h	USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)—Offset 80F0h	314803A0h
80FCh	80FFh	USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)—Offset 80FCh	8003h
8140h	8143h	Power Scheduler Control-0 (PWR_SCHED_CTRL0)—Offset 8140h	A019132h
8144h	8147h	Power Scheduler Control-1 (PWR_SCHED_CTRL2)—Offset 8144h	23Fh
8154h	8157h	AUX Power Management Control (AUX_CTRL_REG2)—Offset 8154h	1192206h
8164h	8167h	USB2 PHY Power Management Control (USB2_PHY_PMC)—Offset 8164h	FCh
816Ch	816Fh	XHCI Aux Clock Control Register (XHCI_AUX_CCR)—Offset 816Ch	F4038h
8174h	8177h	XHC Latency Tolerance Parameters LTV Control (XLTP_LTV1)—Offset 8174h	1400C01h
817Ch	817Fh	XHC Latency Tolerance Parameters High Idle Time Control (XLTP_HITC)—Offset 817Ch	50002h
8180h	8183h	XHC Latency Tolerance Parameters Medium Idle Time Control (XLTP_MITC)—Offset 8180h	50002h
8184h	8187h	XHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)—Offset 8184h	50002h
81B8h	81BBh	LFPS On Count (LFPSONCOUNT_REG)—Offset 81B8h	20C8h
81C4h	81C7h	USB2 PM Control (USB2PMCTRL_REG)—Offset 81C4h	908h
846Ch	846Fh	USB Legacy Support Capability (USBLEGSUP)—Offset 846Ch	2201h
84F4h	84F7h	Port Disable Override Capability Register (PDO_CAPABILITY)—Offset 84F4h	3C6h
8700h	8703h	Debug Capability ID Register (DCID)—Offset 8700h	5100Ah
8E10h	8E13h	Global Time Sync Capability (GLOBAL_TIME_SYNC_CAP_REG)—Offset 8E10h	12C9h
8E14h	8E17h	Global Time Sync Control (GLOBAL_TIME_SYNC_CTRL_REG)—Offset 8E14h	0h
8E18h	8E1Bh	Microframe Time (Local Time) (MICROFRAME_TIME_REG)—Offset 8E18h	0h
8E20h	8E23h	Global Time Low REG (GLOBAL_TIME_LOW_REG)—Offset 8E20h	0h
8E24h	8E27h	Global Time High REG (GLOBAL_TIME_High_REG)—Offset 8E24h	0h

Table 18-2. Summary of xHCI Memory Mapped Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
90A4h	90A7h	XHCI USB2 Overcurrent Pin Mapping (U2OCM1)—Offset 90A4h	0h
90A8h	90ABh	XHCI USB2 Overcurrent Pin Mapping (U2OCM2)—Offset 90A8h	0h
90ACh	90AFh	XHCI USB2 Overcurrent Pin Mapping (U2OCM3)—Offset 90ACh	0h
90B0h	90B3h	XHCI USB2 Overcurrent Pin Mapping (U2OCM4)—Offset 90B0h	0h
90B4h	90B7h	XHCI USB2 Overcurrent Pin Mapping (U2OCM5)—Offset 90B4h	0h
90B8h	90BBh	XHCI USB2 Overcurrent Pin Mapping (U2OCM6)—Offset 90B8h	0h
90BCh	90BFh	XHCI USB2 Overcurrent Pin Mapping (U2OCM7)—Offset 90BCh	0h
90C0h	90C3h	XHCI USB2 Overcurrent Pin Mapping (U2OCM8)—Offset 90C0h	0h
9124h	9127h	XHCI USB3 Overcurrent Pin Mapping (U3OCM1)—Offset 9124h	0h
9128h	912Bh	XHCI USB3 Overcurrent Pin Mapping (U3OCM2)—Offset 9128h	0h
912Ch	912Fh	XHCI USB3 Overcurrent Pin Mapping (U3OCM3)—Offset 912Ch	0h
9130h	9133h	XHCI USB3 Overcurrent Pin Mapping (U3OCM4)—Offset 9130h	0h
9134h	9137h	XHCI USB3 Overcurrent Pin Mapping (U3OCM5)—Offset 9134h	0h
9138h	913Bh	XHCI USB3 Overcurrent Pin Mapping (U3OCM6)—Offset 9138h	0h
913Ch	913Fh	XHCI USB3 Overcurrent Pin Mapping (U3OCM7)—Offset 913Ch	0h
9140h	9143h	XHCI USB3 Overcurrent Pin Mapping (U3OCM8)—Offset 9140h	0h

18.2.1 Capability Registers Length (CAPLENGTH)—Offset 0h

This register is modified and maintained by BIOS

Access Method

Type: MEM Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7:0	80h RW/L	**Capability Registers Length (CAPLENGTH):** This register is used as an offset to add to the Memory Base Register to find the beginning of the Operational Register Space.

18.2.2 Host Controller Interface Version Number (HCIVERSION)—Offset 2h

This register is modified and maintained by BIOS

Access Method

Type: MEM Register
(Size: 16 bits)

Device:
Function:

Default: 110h

Bit Range	Default and Access	Field Name (ID): Description
15:0	110h RW/L	**Host Controller Interface Version Number (HCIVERSION):** This is a two-byte register containing a BCD encoding of the version number of interface that this host controller interface conforms.

18.2.3 Structural Parameters 1 (HCSPARAMS1)—Offset 4h

This register is modified and maintained by BIOS

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 10000840h

Bit Range	Default and Access	Field Name (ID): Description
31:24	10h RW/L	**Number of Ports (MAXPORTS):** This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Default value = 0Eh
23:19	0h RO	Reserved.
18:8	8h RW/L	**Number of Interrupters (MAXINTRS):** This field specifies the number of interrupters implemented on this host controller. Each interrupter is allocated to a vector of MSI and controls its generation and moderation.
7:0	40h RW/L	**Number of Device Slots (MAXSLOTS):** This field specifies the number of Device Context Structures and Doorbell Array entries this host controller can support. Valid values are in the range of 1 to 255.

18.2.4 Structural Parameters 2 (HCSPARAMS2)—Offset 8h

This register is modified and maintained by BIOS

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 14200054h

Bit Range	Default and Access	Field Name (ID): Description
31:27	2h RW/L	**Max Scratchpad Buffers LO (MAXSCRATCHPADBUFS):** Indicates the number of Scratchpad Buffers system software shall reserve for the xHC.
26	1h RW/L	**Scratchpad Restore (SPR):** 0 = Indicates the Scratchpad buffer space may be freed and reallocated between power events. 1 = Indicates that the xHC requires the integrity of the Scratchpad buffer space to be maintained across power events.
25:21	1h RW/L	**Max Scratchpad Buffers HI (MAXSCRATCHPADBUFS_HI):** Max Scratchpad Buffers Hi (MaxScratchpadBufs)

Bit Range	Default and Access	Field Name (ID): Description
20:8	0h RO	Reserved.
7:4	5h RW/L	**Event Ring Segment Table Max (ERSTMAX):** This field determines the maximum value supported by the Event Ring Segment Table Base Size registers.
3:0	4h RW/L	**Isochronous Scheduling Threshold (IST):** This field indicates to system software the minimum distance (in time) that it is required to stay ahead of the xHC while adding TRBs, in order to have the xHC process them at the correct time. The value is specified in the number if frames/ microframes. If bit [3] of IST is cleared to 0b, software can add a TRB no later than IST [2:0] microframes before that TRB is scheduled to be executed. If bit [3] of IST is set to 1b, software can add a TRB no later than IST[2:0] frames before that TRB is scheduled to be executed.

18.2.5 Structural Parameters 3 (HCSPARAMS3)—Offset Ch

This register is modified and maintained by BIOS

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: A0000Ah

Bit Range	Default and Access	Field Name (ID): Description
31:16	A0h RW/L	**U2 Device Exit Latency (U2DEL):** Indicates the worst case latency to transition from U2 to U0. Applies to all root hub ports. The following are permissible values: Value Description 00h Zero 01h Less than 1 µs 02h Less than 2 µs ... 0Bh-FFh Reserved
15:8	0h RO	Reserved.
7:0	Ah RW/L	**U1 Device Exit Latency (U1DEL):** Worst case latency to transition a root hub Port Link State (PLS) from U1 to U0. Applies to all root hub ports. The following are permissible values: Value Description 00h Zero 01h Less than 1 µs 02h Less than 2 µs ... 0800h-FFFFh Reserved

18.2.6 Capability Parameters (HCCPARAMS)—Offset 10h

This register is modified and maintained by BIOS

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 20007FC1h

Bit Range	Default and Access	Field Name (ID): Description
31:16	2000h RW/L	**xHCI Extended Capabilities Pointer (XECP):** This field indicates the existence of a capabilities list. The value of this field indicates a relative offset, in 32-bit words, from Base to the beginning of the first extended capability.
15:12	7h RW/L	**Maximum Primary Stream Array Size (MAXPSASIZE):** RW/L. This fields identifies the maximum size Primary Stream Array that the xHC supports. The Primary Stream Array size = 2MaxPSASize+1. Valid MaxPSASize values are 1 to 15.
11	1h RW/L	**Contiguous Frame ID Capability (CFC):** Contiguous Frame ID Capability (CFC)
10	1h RW/L	**Stopped EDLTA Capabilty (SEC):** This flag indicates that the host controller implementation Stream Context support a Stopped EDLTA field.
9	1h RW/L	**Stopped - Short Packet Capability (SPC):** This flag indicates that the host controller implementation is capable of generating a Stopped-Short Packet Completion Code.
8	1h RW/L	**Parst All Event Data (PAE):** Parse All Event Data (PAE)
7	1h RW/L	**No Secondary SID Support (NSS):** Hardwired to '0' indicating Secondary Stream ID decoding is supported.
6	1h RW/L	**Latency Tolerance Messaging Capability (LTC):** 0 = Latency Tolerance Messaging is not supported. 1 = Latency Tolerance Messaging is supported
5	0h RW/L	**Light HC Reset Capability (LHRC):** 0 = Light Host Controller Reset is not supported. 1 = Light Host Controller Reset is supported
4	0h RW/L	**Port Indicators (PIND):** This bit indicates whether the xHC root hub ports support port indicator control. When this bit is a '1', the port status and control registers include a read/writeable field for controlling the state of the port indicator.
3	0h RW/L	**Port Power Control (PPC):** This bit indicates whether the host controller implementation includes port power control. A '1' in this bit indicates the ports have port power switches. A '0' in this bit indicates the port do not have port power switches.
2	0h RW/L	**Context Size (CSZ):** If this bit is set to '1', then the xHC uses 64 byte Context data structures. If this bit is cleared to '0', then the xHC uses 32 byte Context data structures.
1	0h RW/L	**BW Negotiation Capability (BNC):** 0 = Not capable of BW Negotiation. 1 = Capable of BW Negotiation.
0	1h RW/L	**64-bit Addressing Capability (AC64):** This bit documents the addressing range capability of the xHC. The value of this flag determines whether the xHC has implemented the high order 32- bits of 64-bit register and data structure pointer fields. Values for this flag have the following interpretation: 0 = Supports 32-bit address memory pointers 1 = Supports 64-bit address memory pointers If 32-bit address memory pointers are implemented, the xHC shall ignore the high order 32- bits of 64-bit data structure pointer fields, and system software shall ignore the high order 32- bits of 64-bit xHC registers.

18.2.7 Doorbell Offset (DBOFF)—Offset 14h

Doorbell Offset

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 3000h

Bit Range	Default and Access	Field Name (ID): Description
31:2	C00h RO	**Doorbell Array Offset (DBAO):** This field defines the DWord offset of the Doorbell Array base address from the Base (for example, the base address of the xHCI Capability register address space).
1:0	0h RO	Reserved.

18.2.8 Runtime Register Space Offset (RTSOFF)—Offset 18h

Runtime Register Space Offset

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2000h

Bit Range	Default and Access	Field Name (ID): Description
31:5	100h RO	**Runtime Register Space Offset (RTRSO):** This field defines the 32-byte offset of the xHCI Runtime Registers from the Base. That is, Runtime Register Base Address = Base + Runtime Register Set Offset.
4:0	0h RO	Reserved.

18.2.9 USB Command (USBCMD)—Offset 80h

USB Command

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW	**Enable U3 MFINDEX Stop (EU3S):** When set to 1b, the xHC may stop the MFINDEX counting action if all Root Hub ports are in the U3, Disconnected, Disabled, or Powered-off state. When cleared to 0b, the xHC may stop the MFINDEX counting action if all Root Hub ports are in the Disconnected, Disabled, or Powered-off state.
10	0h RW	**Enable Wrap Event (EWE):** When set to 1b, the xHC shall generate a MFINDEX Wrap Event every time the MFINDEX register transitions from 03FFFh to 0. When cleared to 0b, no MFINDEX Wrap Events are generated.
9	0h RW	**Controller Restore State (CRS):** When set to 1b, MEM_BASE+80h:bit 0= 0b, and MEM_BASE+80h:bit 8 = 1b, the xHC shall perform a Restore State operation and restore its internal state. When set to 1b and MEM_BASE+80h:bit 0= 1b or MEM_BASE+80h:bit 8 = 0b, or when cleared to '0', no Restore State operation shall be performed.

Bit Range	Default and Access	Field Name (ID): Description
8	0h RW	**Controller Save State (CSS):** When written by software with 1b and MEM_BASE+80h:bit 0=0b, the xHC shall save any internal state that will be restored by a subsequent Restore State operation. When written by software with 1b and MEM_BASE+80h:bit 0= 1b, or written with '0', no Save State operation shall be performed.
7	0h RW	**Light Host Controller Reset (LHCRST):** If the Light HC Reset Capability (LHRC) bit (MEM_BASE=10h:bit 5) is 1b, then setting this bit to 1b allows the driver to reset the xHC without affecting the state of the ports. A system software read of this bit as 0b indicates the Light Host Controller Reset has completed and it is safe for software to re-initialize the xHC. A software read of this bit as a 1b indicates the Light Host Controller Reset has not yet completed.
6:4	0h RO	Reserved.
3	0h RW	**Host System Error Enable (HSEE):** When this bit is set to 1b, and the HSE bit (MEM_BASE+84h:bit 2) is set to 1b, the xHC shall assert out-of-band error signaling to the host. The signaling is acknowledged by software clearing the HSE bit.
2	0h RW	**Interrupter Enable (INTE):** This control bit is used by software to reset the host controller. When software sets this bit to 1b, the Host Controller resets its internal pipelines, timers, counters, state machines, and so forth, to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values.
1	0h RW	**Host Controller Reset (HCRST):** This control bit is used by software to reset the host controller. When software sets this bit to 1b, the Host Controller resets its internal pipelines, timers, counters, state machines, and so forth, to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values.
0	0h RW	**Run/Stop (RS):** When set to 1b, the xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to 1b. When this bit is cleared to 0b, the xHC completes the current and any actively pipelined transactions on the USB and then halts. The xHC shall halt within 16 microframes after software clears the Run/ Stop bit. The HCHalted (HCH) bit (MEM_BASE+84h:bit 0) indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. Software shall not write a '1' to this flag unless the xHC is in the Halted state (that is, HCH in the USBSTS register is '1'); doing so will yield undefined results.

18.2.10 USB Status (USBSTS)—Offset 84h

This register indicates pending interrupts and various states of the Host controller. The status resulting from a transaction on the serial bus is not indicated in this register. See the Interrupts description in section 4 of the xHCI specification for additional information concerning interrupt conditions.
Note: For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 has no effect.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RO	**Host Controller Error (HCE):** This flag shall be set to indicate that an internal error condition has been detected which requires software to reset and re-initialize the xHC. 0 = No internal xHC error conditions exist. 1 = Internal xHC error condition exists.
11	0h RO	**Controller Not Ready (CNR):** 0 = Ready 1 = Not Ready Software shall not write any Doorbell or Operational register of the xHC, other than the USBSTS register, until CNR = 0b. This flag is set by the xHC after a Hardware Reset and cleared when the xHC is ready to begin accepting register writes. This flag shall remain cleared (0b) until the next Chip Hardware Reset.
10	0h RW/1C	**Save/Restore Error (SRE):** If an error occurs during a Save or Restore operation this bit shall be set to 1b. This bit shall be cleared to 0b when a Save or Restore operation is initiated or when written with 1b.
9	0h RO	**Restore State Status (RSS):** When the Controller Restore State (CRS) flag in the USB_CMDregister is written with 1b this bit shall be set to 1b and remain set while the xHC restores its internal state. Note: When the Restore State operation is complete, this bit shall be cleared to 0b.
8	0h RO	**Save State Status (SSS):** Save State Status
7:5	0h RO	Reserved.
4	0h RW/1C	**Port Change Detect (PCD):** This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the xHC, this bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, overcurrent change, enable/disable change and connect status change). Regardless of the implementation, when this bit is readable (that is, in the D0 state), it must provide a valid view of the Port Status registers. 0 = No change bit transition from a 0 to 1 or No Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port. 1 = The Host controller sets this bit to 1 when any port for which the Port Owner bit is set to 0 has a change bit transition from a 0 to 1 or a Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port.
3	0h RW/1C	**Event Interrupt (EINT):** The xHC sets this bit to 1b when the Interrupt Pending (IP) bit of any Interrupter is transitions from 0b to 1b. Software that uses EINT shall clear it prior to clearing any IP flags. A race condition will occur if software clears the IP flags then clears the EINT flag, and between the operations another IP ‘0’ to '1' transition occurs. In this case the new IP transition will be lost.
2	0h RW/1C	**Host System Error (HSE):** The xHC sets this bit to 1b when a serious error is detected, either internal to the xHC or during a host system access involving the xHC module. Conditions that set this bit to ‘1’ include PCI Parity error, PCI Master Abort, and PCI Target Abort. When this error occurs, the xHC clears the Run/Stop (R/S) bit in the USB_CMD register to prevent further execution of the scheduled TDs. If the HSEE bit in the USB_CMD register is 1b, the xHC shall also assert out-ofband error signaling to the host.
1	0h RO	Reserved.
0	1h RO	**HCHalted (HCH):** This bit is a ‘0’ whenever the Run/Stop (R/S) bit is set to 1b. The xHC sets this bit to 1b after it has stopped executing as a result of the Run/Stop (R/S) bit being cleared to 0b, either by software or by the xHC hardware (for example, internal error). If this bit is set to1b, then SOFs, microSOFs, or Isochronous Timestamp Packets (ITP) shall not be generated by the xHC.

18.2.11 Page Size (PAGESIZE)—Offset 88h

Page Size

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	1h RO	**Page Size (PAGESIZE):** Hardwired to 1h to indicate support for 4 Kbyte page sizes.

18.2.12 Device Notification Control (DNCTRL)—Offset 94h

Device Notification Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Notification Enable (N0_N15):** When a Notification Enable bit is set, a Device Notification Event will be generated when a Device Notification Transaction Packet is received with the matching value in the Notification Type field. For example, setting N1 to '1' enables Device Notification Event generation if a Device Notification TP is received with its Notification Type field set to '1' (FUNCTION_WAKE), and so on

18.2.13 Command Ring Low (CRCR_LO)—Offset 98h

Command Ring Low

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:6	0h WO	**Command Ring Pointer (CRP):** This field defines low order bits of the initial value of the 64-bit Command Ring Dequeue Pointer. Notes: 1. Writes to this field are ignored when Command Ring Running bit (CRR) = 1b. 2. If the CRCR register is written while the Command Ring is stopped (CRR = 0b), the value of this field shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. 3. If the CRCR register is not written while the Command Ring is stopped (CRR = 0b), then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. 4. Reading this field always returns 0b.
5:4	0h RO	Reserved.
3	0h RO	**Command Ring Running (CRR):** This bit is set to 1b if the Run/Stop (R/S) bit is 1b and the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. It is cleared to 0b when the Command Ring is stopped after writing a 1b to the Command Stop (CS) or Command Abort (CA) bits, or if the R/S bit is cleared to 0b.
2	0h WO	**Command Abort (CA):** Writing a 1b to this bit shall immediately terminate the currently executing command, stop the Command Ring, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Notes: 1. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = 0b. 2. Reading this bit always returns 0b.
1	0h WO	**Command Stop (CS):** Writing a 1b to this bit shall stop the operation of the Command Ring after the completion of the currently executing command, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped and the Command TRB Pointer set to the current value of the Command Ring Dequeue Pointer. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Notes: 1. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) bit = 0b. 2. Reading this bit always returns 0b.
0	0h WO	**Ring Cycle State (RCS):** This bit identifies the value of the xHC Consumer Cycle State (CCS) flag for the TRB referenced by the Command Ring Pointer. Notes: 1. Writes to this bit are ignored when the Command Ring Running (CRR) bit = 1b. 2. If the CRCR register is written while the Command Ring is stopped (CCR = 0b), then the value of this flag shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. 3. If the CRCR register is not written while the Command Ring is stopped (CCR = 0b), then the Command Ring will begin fetching Command TRBs using the current value of the internal Command Ring CCS flag. 4. Reading this flag always returns 0b.

18.2.14 Command Ring High (CRCR_HI)—Offset 9Ch

Command Ring High

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h WO	**Command Ring Pointer (CRP):** Command Ring Pointer—R/W. This field defines high order bits of the initial value of the 64-bit Command Ring Dequeue Pointer. Notes: 1. Writes to this field are ignored when Command Ring Running bit (CRR) = 1b. 2. If the CRCR register is written while the Command Ring is stopped (CRR = 0b), the value of this field shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. 3. If the CRCR register is not written while the Command Ring is stopped (CRR = 0b), then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. 4. Reading this field always returns 0b.

18.2.15 Device Context Base Address Array Pointer Low (DCBAAP_LO)—Offset B0h

Device Context Base Address Array Pointer Low

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:6	0h RW	**Device Context Base Address Array Pointer (DCBAAP):** This field defines low order bits of the 64-bit base address of the Device Context Pointer Array table (a table of address pointers that reference Device Context structures for the devices attached to the host.
5:0	0h RO	Reserved.

18.2.16 Device Context Base Address Array Pointer High (DCBAAP_HI)—Offset B4h

Device Context Base Address Array Pointer High

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Device Context Base Address Array Pointer (DCBAAP):** This field defines high order bits of the 64-bit base address of the Device Context Pointer Array table (a table of address pointers that reference Device Context structures for the devices attached to the host.)

18.2.17 Port N Status and Control USB2 (PORTSCN)—Offset 480h

Note that this USB2 Port Status and Control register is available at the following offsets for all applicable USB2 ports:

USB2 Port 1: 480h
USB2 Port 2: 490h
USB2 Port 3: 4A0h
.....
USB2 Port 9: 500h
USB2 Port 10: 510h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2A0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR):** When software sets this bit to 1b, the Warm Reset sequence is enabled
30	0h RW/L	**Device Removable (DR):** This bit indicates if this port has a removable device. 0 = Device is removable. 1 = Device is non-removable.
29:28	0h RO	Reserved.
27	0h RW/P	**Wake on Over-current Enable (WOE):** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to overcurrent conditions as system wake-up events.
26	0h RW/P	**Wake on Disconnect Enable (WDE):** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device disconnects as system wake-up events.
25	0h RW/P	**Wake on Connect Enable (WCE):** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device connects as system wake-up events.
24	0h RO	**Cold Attach Status (CAS):** This bit indicates that far-end terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable to advance to the Enabled state. Software shall clear this bit by writing a 1b to the WPR bit or the xHC shall clear this bit if the CSS bit transitions to 1.
23	0h RW/1C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/1C	**Port Link State Change (PLC):** 0 = No change 1 = Link Status Change This flag is set to '1' due to the following Port Link State (PLS) transitions:
21	0h RW/1C	**Port Reset Change (PRC):** This flag is set to '1' due a '1' to '0' transition of Port Reset (PR), for example, when any reset processing on this port is complete. 0 = No change 1 = Reset Complete
20	0h RW/1C	**Over-current Change (OCC):** The functionality of this bit is not dependent upon the port owner. Software clears this bit by writing a 1 to it. 0 = No change. (Default) 1 = There is a change to Overcurrent Active.

Bit Range	Default and Access	Field Name (ID): Description
19	0h RW/1C	**Warm Port Reset Change (WRC):** This bit is set when Warm Reset processing on this port completes. 0 = No change. (Default) 1 = Warm reset complete
18	0h RW/1C	**Port Enabled Disabled Change (PEC):** 0 = No change. (Default) 1 = There is a change to PED bit.
17	0h RW/1C	**Connect Status Change (CSC):** R/WC. This flag indicates a change has occurred in the port's Current Connect Status (CCS) or Cold Attach Status (CAS) bits. 0 = No change. (Default) 1 = There is a change to the CCS or CAS bit. The xHC sets this bit to 1b for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (that is, the bit will remain 1b).
16	0h RW	**Port Link State Write Strobe (LWS):** 0 = When 0b, write data in PLS field is ignored. (Default) 1 = When this bit is set to 1b on a write reference to this register, this flag enables writes to the PLS field. Reads to this bit return '0'.
15:14	0h RW/P	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PORTSPEED):** A device attached to this port operates at a speed defined by the following codes: Value Speed 0001b Full-speed 0010b Low speed 0011b Highspeed All other values reserved. Refer to the eXtensible Host Controller Interface for Universal Serial Bus Specification for additional details.
9	1h RW/P	**Port Power (PP):** This indicates that the port does have power.
8:5	5h RW/P	**Port Link State (PLS):** This field is used to power manage the port and reflects its currentlink state.When the port is in the Enabled state, system software may set the link U-state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write Value and Description 0: The link shall transition to a U0 state from any of the U-states. 2: USB 2.0 ports only. The link should transition to the U2 State. 3: The link shall transition to a U3 state from any of the U-states. This action selectively suspends the device connected to this port. While the Port LinkState = U3, the hub does not propagate downstream-directed traffic to this port, but the hub will respond to resume signaling from the port. 5: USB 3.0 ports only. If the port is in the Disabled state (PLS = Disabled, PP= 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 15: USB 2.0 ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3Exit substate, else ignored. All other values are ignored Read Value and Definition 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspended) 4: Link is in the Disabled State 5:Link is in the RxDetect State 6:Link is in the Inactive State 7: Link is in the Polling State 8:Link is in the Recovery State 9: Link is in the Hot Reset State 10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12–14: Reserved 15: Link is in the Resume State
4	0h RW/1S	**Port Reset (PR):** When software writes a 1 to this bit (from a 0), the bus reset sequence as 1=port in reset 0=port not in reset
3	0h RW	**Over-current Active (OCA):** 0 = This port does not have an overcurrent condition. (Default) 1 = This port currently has an overcurrent condition. This bit will automatically transition from 1 to 0 when the overcurrent condition is removed. The PCH automatically disables the port when the overcurrent active bit is 1.

Bit Range	Default and Access	Field Name (ID): Description
2	0h RO	Reserved.
1	0h RW/1C	**Port Enabled Disabled (PED):** Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a 1 to this bit. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. The bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. 0=disable 1=enable(default)
0	0h RW	**Current Connect Status (CCS):** This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 0=no device is present 1=device is present on port.

18.2.18 Port Power Management Status Aand Control USB2 (PORTPMSCN)—Offset 484h

Note that this USB2 Port Power Management Status and Control register is available at the following offsets for all applicable USB2 ports:

USB2 Port 1: 484h
USB2 Port 2: 494h
USB2 Port 3: 4A4h
.....
USB2 Port 9: 504h
USB2 Port 10: 514h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RW/P	**Port Test Control (PTC):** When this field is '0', the port is not operating in a test mode. (Default) A non-zero value indicates that the port is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the Disabled state. If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error. The encoding of the Test Mode bits for a USB 2.0 port are: Value Test Mode 0h Test mode not enabled 1h Test J_STATE 2h Test K_STATE 3h Test SE0_NAK 4h Test Packet 5h Test FORCE_ENABLE 6h–14h Reserved. 15 Port Test Control Error
27:17	0h RO	Reserved.
16	0h RW	**Hardware LPM Enable (HLE):** 0=disable 1=Enable. When this bit is a 1, hardware controlled LPM shall be enabled for this port.
15:8	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
7:4	0h RW/P	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.
3	0h RW/P	**Remote Wake Enable (RWE):** The host system sets this flag to enable or disable the device for remote wake from L1. 0=disable 1=enable The value of this flag will temporarily (while in L1) override the current setting of the Remote Wake feature set by the standard Set/ClearFeature() commands defined in Universal Serial Bus Specification, revision 2.0, Chapter 9.
2:0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

18.2.19 Port N Hardware LPM Control Register (PORTHLPMCN)—Offset 48Ch

Note that this Port Hardware Control register is available at the following offsets for all applicable USB ports:

USB2 Port 1: 48Ch
USB2 Port 2: 49Ch
USB2 Port 3: 4ACh
.....
USB2 Port 9: 50Ch
USB2 Port 10: 51Ch

This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST).The definition for the fields depend on the protocol supported.
For USB3 this register is reserved and shall be treated by software as RsvdP.
For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
13:10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us...Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9:2	0h RW/P	**L1 Timeout (L1_TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us....FFh: 65,280us
1:0	0h RW/P	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

18.2.20 Port Status And Control USB3 (PORTSCXUSB3)—Offset 540h

The USB3 Port Status and Control registers are available at the following offsets for applicable USB3 ports:
USB3 Port 1: 540h
USB3 port 2: 550h
USB3 port 3: 560h
USB3 port 4: 570h
USB3 port 5: 580h
USB3 port 6: 590h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2A0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/1S	**Warm Port Reset (WPR):** When software sets this bit to 1b, the Warm Reset sequence is enabled
30	0h RW/L	**Device Removable (DR):** This bit indicates if this port has a removable device. 0 = Device is removable. 1 = Device is non-removable.
29:28	0h RO	Reserved.
27	0h RW/P	**Wake on Over-current Enable (WOE):** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to overcurrent conditions as system wake-up events.
26	0h RW/P	**Wake on Disconnect Enable (WDE):** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device disconnects as system wake-up events.
25	0h RW/P	**Wake on Connect Enable (WCE):** 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device connects as system wake-up events.

Bit Range	Default and Access	Field Name (ID): Description
24	0h RO	**Cold Attach Status (CAS):** This bit indicates that far-end terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable to advance to the Enabled state. Software shall clear this bit by writing a 1b to the WPR bit or the xHC shall clear this bit if the CSS bit transitions to 1.
23	0h RW/1C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0h RW/1C	**Port Link State Change (PLC):** 0 = No change 1 = Link Status Change This flag is set to '1' due to the following Port Link State (PLS) transitions:
21	0h RW/1C	**Port Reset Change (PRC):** This flag is set to '1' due a '1' to '0' transition of Port Reset (PR), for example, when any reset processing on this port is complete. 0 = No change 1 = Reset Complete
20	0h RW/1C	**Over-current Change (OCC):** The functionality of this bit is not dependent upon the port owner. Software clears this bit by writing a 1 to it. 0 = No change. (Default) 1 = There is a change to Overcurrent Active.
19	0h RW/1C	**Warm Port Reset Change (WRC):** This bit is set when Warm Reset processing on this port completes. 0 = No change. (Default) 1 = Warm reset complete
18	0h RW/1C	**Port Enabled Disabled Change (PEC):** 0 = No change. (Default) 1 = There is a change to PED bit.
17	0h RW/1C	**Connect Status Change (CSC):** R/WC. This flag indicates a change has occurred in the port's Current Connect Status (CCS) or Cold Attach Status (CAS) bits. 0 = No change. (Default) 1 = There is a change to the CCS or CAS bit. The xHC sets this bit to 1b for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (that is, the bit will remain 1b).
16	0h RW	**Port Link State Write Strobe (LWS):** 0 = When 0b, write data in PLS field is ignored. (Default) 1 = When this bit is set to 1b on a write reference to this register, this flag enables writes to the PLS field. Reads to this bit return '0'.
15:14	0h RW/P	**Port Indicator Control (PIC):** Note: This register is sticky.
13:10	0h RW	**Port Speed (PORTSPEED):** A device attached to this port operates at a speed defined by the following codes: Value Speed 0100b SuperSpeed (5Gb/s) 0101b SuperSpeedPlus (10Gb/s) All other values reserved.
9	1h RW/P	**Port Power (PP):** This indicates that the port does have power.

Bit Range	Default and Access	Field Name (ID): Description
8:5	5h RW/P	**Port Link State (PLS):** This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U-state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. Write Value and Description: 0: The link shall transition to a U0 state from any of the U-states. 2: USB 2.0 ports only. The link should transition to the U2 State. 3: The link shall transition to a U3 state from any of the U-states. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub will respond to resume signaling from the port. 5: USB 3.0 ports only. If the port is in the Disabled state (PLS = Disabled, PP = 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored. 15: USB 2.0 ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3Exit substate, else ignored. All other values Ignored Note: The Port Link State Write Strobe (LWS) shall be set to 1b towrite this field. Read Value and Definition: 0: Link is in the U0 State 1: Link is in the U1 State 2: Link is in the U2 State 3: Link is in the U3 State (Device Suspended) 4: Link is in the Disabled State 5: Link is in the RxDetect State 6: Link is in the Inactive State 7: Link is in the Polling State 8: Link is in the Recovery State 9: Link is in the Hot Reset State 10: Link is in the Compliance Mode State 11: Link is in the Test Mode State 12–14: Reserved 15: Link is in the Resume State
4	0h RW/1S	**Port Reset (PR):** When software writes a 1 to this bit (from a 0), the bus reset sequence as defined in the USB Specification, Revision 2.0 is started. Software writes a 0 to this bit to terminate the bus reset sequence. Software must keep this bit at a 1 long enough to ensure the reset sequence completes as specified in the USB Specification, Revision 2.0. USB 3.0 ports shall execute the Hot Reset sequence as defined in the USB 3.0 Specification. PR remains set until reset signaling is completed by the root hub. 1 = Port is in Reset. 0 = Port is not in Reset.
3	0h RW	**Over-current Active (OCA):** 0 = This port does not have an overcurrent condition. (Default) 1 = This port currently has an overcurrent condition. This bit will automatically transition from 1 to 0 when the overcurrent condition is removed. The PCH automatically disables the port when the overcurrent active bit is 1.
2	0h RO	Reserved.
1	0h RW/1C	**Port Enabled Disabled (PED):** Ports can only be enabled by the host controller as a part of thereset and enable. Software cannot enable a port by writing a 1 to this bit. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. The bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. 0 = Disable. 1 = Enable. (Default)
0	0h RW	**Current Connect Status (CCS):** This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 0 = No device is present. (Default) 1 = Device is present on port.

18.2.21 Port Power Management Status And Control USB3 (PORTPMSCX)—Offset 544h

The USB3 Port Status and Control registers are available at the following offsets for applicable USB3 ports:
USB3 Port 1: 544h
USB3 port 2: 554h
USB3 port 3: 564h

USB3 port 4: 574h
USB3 port 5: 584h
USB3 port 6: 594h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW	**Force Link PM Accept (FLA):** Force Link PM Accept (FLA):
15:8	0h RW/P	**U2 Timeout (U2T):** U2 Timeout (U2T):
7:0	0h RW/P	**U1 Timeout (U1T):** U1 Timeout (U1T):

18.2.22 USB3 Port X Link Info (PORTLIX)—Offset 548h

Note that this USB3 Port Link Info register is available at the following offsets for all applicable USB3 ports:
USB3 Port 1: 548h
USB3 port 2: 558h
USB3 port 3: 568h
USB3 port 4: 578h
USB3 port 5: 588h
USB3 port 6: 598h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Link Error Count (LEC):** Displays the Link Error Count for the USB 3 port.

18.2.23 Microframe Index (RTMFINDEX)—Offset 2000h

Microframe Index

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:0	0h RO	**Microframe Index (IMAN0):** Microframe Index

18.2.24 Interrupter x Management (IMANx)—Offset 2020h

Note that there are a total of 8 IMAN registers at the following offsets:
IMAN0: at offset 2020h
IMAN1: at offset 2040h
IMAN2: at offset 2060h
.....
IMAN6: at offset 20E0h
IMAN7; at offset 2100h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RO	Reserved.
1	0h RW	**Interrupt Enable (IE):** This flag specifies whether the Interrupter is capable of generating an interrupt. 0 = The Interrupter is prohibited from generating interrupts. 1 = When this bit and the IP bit are set (1b), the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches '0'.
0	0h RW/1C	**Interrupt Pending (IP):** 0 = No interrupt is pending for the Interrupter. 1 = An interrupt is pending for this Interrupter. This bit is set to 1b when IE = 1, the IMODI Interrupt Moderation Counter field = 0b, the Event Ring associated with the Interrupter is not empty (or for the Primary Interrupter when the HCE flag is set to 1b), and EHB = 0. If MSI interrupts are enabled, this flag shall be cleared automatically when the PCI DWord write generated by the Interrupt assertion is complete. If PCI Pin Interrupts are enabled, this flag shall be cleared by software.

18.2.25 Interrupter x Moderation (IMODx)—Offset 2024h

Note that there are a total of 8 IMOD registers at the following offsets:
IMOD0 : at offset 2024h
IMOD1: at offset 2044h
IMOD2: at offset 2064h

.....
IMOD6: at offset 20E4h
IMOD7; at offset 2104h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: FA0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW	**Interrupt Moderation Counter (IMODC):** Down counter. Loaded with Interval Moderation value—value of bits 15:0, whenever the IP bit is cleared to 0b, counts down to '0', and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP bits = 1, and EHB = 0. This counter may be directly written by software at any time to alter the interrupt rate
15:0	FA0h RW	**Interrupt Moderation Interval (IMODI):** Minimum inter-interrupt interval. The interval is specified in 250 ns increments. A value of '0' disables interrupt throttling logic and interrupts shall be generated immediately if IP = 0, EHB = 0, and the Event Ring is not empty.

18.2.26 Event Ring Segment Table Size x (ERSTSZx)—Offset 2028h

There are 8 ERSTSZ registers available at the following address offsets:
ERSTSZ0: at offset 2028h
ERSTSZ1: at offset 2048h
ERSTSZ2: at offset 2068h
ERSTSZ3: at offset 2088h
ERSTSZ4: at offset 20A8h
ERSTSZ5: at offset 20C8h
ERSTSZ6: at offset 20E8h
ERSTSZ7: at offset 2108h
Address Offset: 2028-202Bh, 2048-204Bh, ..., 2028+(MaxInts-1)*20h-202B+(MaxInts-1)*20h

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register.

18.2.27 Event Ring Segment Table Base Address Low x (ERSTBA_LOx)—Offset 2030h

There are 8 ERSTBA_LO registers available at the following address offsets:
ERSTBA_LO0: at offset 2030h
ERSTBA_LO1: at offset 2050h
ERSTBA_LO2: at offset 2070h
ERSTBA_LO3: at offset 2090h
ERSTBA_LO4: at offset 20B0h
ERSTBA_LO5: at offset 20D0h
ERSTBA_LO6: at offset 20F0h
ERSTBA_LO7: at offset 2110h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:6	0h RW	**Event Ring Segment Table Base Address Register (ERSTBA):** This field defines the low order bits of the start address of the Event Ring Segment Table. This field shall not be modified if HCHalted (HCH) = 0.
5:0	0h RO	Reserved.

18.2.28 Event Ring Segment Table Base Address High x (ERSTBA_HIx)—Offset 2034h

There are 8 ERSTBA_HI registers available at the following address offsets:
ERSTBA_HI0: at offset 2034h
ERSTBA_HI1: at offset 2054h
ERSTBA_HI2: at offset 2074h
ERSTBA_HI3: at offset 2094h
ERSTBA_HI4: at offset 20B4h
ERSTBA_HI5: at offset 20D4h
ERSTBA_HI6: at offset 20F4h
ERSTBA_HI7: at offset 2114h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Segment Table Base Address (ERSTBA):** This field defines the low order bits of the start address of the Event Ring Segment Table. This field shall not be modified if HCHalted (HCH) = 0.

18.2.29 Event Ring Dequeue Pointer Low x (ERDP_LOx)—Offset 2038h

There are 8 ERDP_LO registers available at the following address offsets:
ERDP_LO0: at offset 2038h
ERDP_LO1: at offset 2058h
ERDP_LO2: at offset 2078h
ERDP_LO3: at offset 2098h
ERDP_LO4: at offset 20B8h
ERDP_LO5: at offset 20D8h
ERDP_LO6: at offset 20F8h
ERDP_LO7: at offset 2118h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RW	**Event Ring Dequeue Pointer (ERDP):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that Event Ring Dequeue Pointer resides in.
3	0h RW/1C	**Event Handler Busy (EHB):** This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written.
2:0	0h RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that Event Ring Dequeue Pointer resides in.

18.2.30 Event Ring Dequeue Pointer High x (ERDP_HIx)—Offset 203Ch

There are 8 ERDP_LO registers available at the following address offsets:
ERDP_HI0: at offset 203Ch
ERDP_HI1: at offset 205Ch
ERDP_HI2: at offset 207Ch
ERDP_HI3: at offset 209Ch
ERDP_HI4: at offset 20BCh
ERDP_HI5: at offset 20DCh
ERDP_HI6: at offset 20FCh
ERDP_HI7: at offset 211Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Event Ring Dequeue Pointer (ERDP):** This field defines the low order bits of the 64- bit address of the current Event Ring Dequeue Pointer.

18.2.31 Door Bell x (DBx)—Offset 3000h

Door Bell registers are an array of 32 registers.
The door bell registers are at the following offset:

Door Bell 0: 3000-3003h
Door Bell 1: 3004-3007h
.....
Door Bell 30: 3078-307Bh
Door Bell 31: 307C-307Fh

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW	**DB Stream ID (DSI):** DB Stream ID
15:8	0h RO	Reserved.
7:0	0h RW	**DB Target (DT):** This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Refer to the xHCI Specification for definitions of the values.

18.2.32 XECP SUPP USB2_0 (XECP_SUPP_USB2_0)—Offset 8000h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2000802h

Bit Range	Default and Access	Field Name (ID): Description
31:24	2h RO	**USB Major Revision: 2.0 (USB2_MAJ_REV):** Major Specification Release Number in Binary-Coded Decimal (i.e., version 3.x is 03h). This field identifies the major release number component of the specification with which the xHC is compliant.
23:16	0h RO	**USB Minor Revision (USB_MIN_REV):** Minor Specification Release Number in Binary-Coded Decimal (i.e., version x.10 is 10h). This field identifies the minor release number component of the specification with which the xHC is compliant.
15:8	8h RO	**Next Capability Pointer (NCP):** This field indicates the location of the next capability with respect to the effective address of this capability.
7:0	2h RO	**Supported Protocol ID (SPID):** This field identifies the xHCI Extended capability. Refer to Table 146 for a list of the valid xHCI extended capabilities.

18.2.33 XECP SUPP USB2_1 (XECP_SUPP_USB2_1)—Offset 8004h

XECP SUPP USB2_1

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 20425355h

Bit Range	Default and Access	Field Name (ID): Description
31:0	20425355h RO	**XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1):** This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters may be defined. Allowed characters are: alphanumeric, space, and underscore. Alpha characters are case sensitive.

18.2.34 XECP SUPP USB2_2 (XECP_SUPP_USB2_2)—Offset 8008h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 30180C01h

Bit Range	Default and Access	Field Name (ID): Description
31:28	3h RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT):** 3 USB 2.0 Speed (High, Full, Low)
27:21	0h RO	Reserved.
20	1h RW/L	**BESL LPM Capability (BLC):** Bit is set to 1 to indicate that the the ports described by this xHCI Supported Protocol Capability will apply BESL timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMCC registers.
19	1h RW/L	**Protocol Defined - Hardware LMP Capability (HLC):** This field can be modified and maintained by BIOS under Access Control

Bit Range	Default and Access	Field Name (ID): Description
18	0h RO	**Protocol Defined - Integrated Hub Implementation (IHI):** Protocol Defined - Integrated Hub Implementation
17	0h RO	**Protocol Defined - High SPeed Only (HSO):** This field indicates the number of Protocol Speed ID (PSI) Dwords that the xHCI Supported Protocol Capability data structure contains. If this field is non-zero, then all speeds supported by the protocol shall be defined using PSI Dwords, i.e. no implied Speed ID mappings apply.
16	0h RO	Reserved.
15:8	Ch RO	**Compatible Port Count (CPC):** This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are 1 to MaxPorts.
7:0	1h RO	**Compatible Port Offset (CPO):** This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are '1' to MaxPorts.

18.2.35 XECP SUPP USB3_3 (XECP_SUPP_USB2_3)—Offset 800Ch

XECP SUPP USB3_3

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:0	0h RO	**XECP_SUPP_USB3_3 (PROTOCOL_SLOT_TYPE):** Protocol Slot Type

18.2.36 XECP SUPP USB2_4 Full Speed (XECP_SUPP_USB2_4)—Offset 8010h

XECP SUPP USB2_4 Full Speed

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: C0021h

Bit Range	Default and Access	Field Name (ID): Description
31:16	Ch RO	**Protocol Speed ID Mantissa (PSIM):** This field defines the mantissa that shall be applied to the PSIE when calculating the maximum bit rate represented by this PSI Dword
15:9	0h RO	Reserved.
8	0h RO	**PSI Full Duplex (PFD):** If this bit is '1' the link is full-duplex (dual-simplex), and if '0' the link is half-duplex (simplex).
7:6	0h RO	**PSI Type (PLT):** This field identifies whether the PSI Dword defines a symmetric or asymmetric bit rate, and if asymmetric, then this field also indicates if this Dword defines the receive or transmit bit rate. Note that the Asymmetric PSI Dwords shall be paired, i.e. an Rx immediately followed by a Tx, and both Dwords shall define the same value for the PSIV. PLT Value Bit Rate Note 0 Symmetric Single PSI Dword 1 Reserved 2 Asymmetric Rx Paired with Asymmetric Tx PSI Dword 3 Asymmetric Tx Immediately follows Rx Asymmetric PSI Dword
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** This field defines the base 10 exponent times 3, that shall be applied to the Protocol Speed ID Mantissa when calculating the maximum bit rate represented by this PSI Dword. PSIE Value Bit Rate 0 Bits per second 1 Kb/s 2 Mb/s 3 Gb/s
3:0	1h RO	**Protocol Speed ID Value (PSIV):** If a device is attached that operates at the bit rate defined by this PSI Dword, then the value of this field shall be reported in the Port Speed field of PORTSC register (5.4.8) of a compatible port. Note, the PSIV value of '0' is reserved and shall not be defined by a PSI.

18.2.37 XECP_SUPP USB2_5 Low Speed (XECP_SUPP_USB2_5)—Offset 8014h

XECP_SUPP USB2_5 Low Speed

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 5DC0012h

Bit Range	Default and Access	Field Name (ID): Description
31:16	5DCh RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	Reserved.
8	0h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	1h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	2h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

18.2.38 XECP SUPP USB2_6 High Speed (XECP_SUPP_USB2_6)—Offset 8018h

XECP SUPP USB2_6 High Speed

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1E00023h

Bit Range	Default and Access	Field Name (ID): Description
31:16	1E0h RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	Reserved.
8	0h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	3h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

18.2.39 XECP SUPP USB3_0 (XECP_SUPP_USB3_0)—Offset 8020h

XECP SUPP USB3_0

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 3101402h

Bit Range	Default and Access	Field Name (ID): Description
31:24	3h RO	**USB Major Revision: 3.0 (USB3_MAJ_REV):** USB Major Revision: 3.0
23:16	10h RW/L	**USB Minor Revision (USB3_MIN_REV):** USB Minor Revision:0.1
15:8	14h RW/L	**Next Capability Pointer (NCP):** Next Capability Pointer
7:0	2h RO	**Supported Protocol ID (SPID):** Supported Protocol ID

18.2.40 XECP SUPP USB3_1 (XECP_SUPP_USB3_1)—Offset 8024h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 20425355h

Bit Range	Default and Access	Field Name (ID): Description
31:0	20425355h RO	**XECP_SUPP_USB3_1 (XECP_SUPP_USB3_1):** Namestring USB

18.2.41 XECP SUPP USB3_2 (XECP_SUPP_USB3_2)—Offset 8028h

XECP SUPP USB3_2

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 8000040Dh

Bit Range	Default and Access	Field Name (ID): Description
31:28	8h RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT):** 1 USB 3.0 Speed (Supper Speed)
27:16	0h RO	Reserved.
15:8	4h RO	**Compatible Port Count (CPC):** The compatible port count varies based on SKU - controlled by the USB3 Port config
7:0	Dh RO	**Compatible Port Offset (CPO):** Compatible Port Offset

18.2.42 XECP SUPP USB3_3 (XECP_SUPP_USB3_3)—Offset 802Ch

XECP SUPP USB3_3

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:0	0h RO	**XECP_SUPP_USB3_3 (PROTOCOL_SLOT_TYPE):** Protocol Slot Type

18.2.43 XECP SUPP USB3_4 (XECP_SUPP_USB3_4 Super Speed)—Offset 8030h

XECP SUPP USB3_4

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 50134h

Bit Range	Default and Access	Field Name (ID): Description
31:16	5h RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	3h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	4h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

18.2.44 XECP SUPP USB3_5 (XECP_SUPP_USB3_5 Super Speed Plus)—Offset 8034h

XECP SUPP USB3_5

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: A0135h

Bit Range	Default and Access	Field Name (ID): Description
31:16	Ah RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	3h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	5h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

18.2.45 XECP SUPP USB3_6 (XECP_SUPP_USB3_6)—Offset 8038h

XECP SUPP USB3_6

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 4E00126h

Bit Range	Default and Access	Field Name (ID): Description
31:16	4E0h RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	6h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

18.2.46 XECP SUPP USB3_7 (XECP_SUPP_USB3_7)—Offset 803Ch

XECP SUPP USB3_7

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 9C00127h

Bit Range	Default and Access	Field Name (ID): Description
31:16	9C0h RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	7h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

18.2.47 XECP SUPP USB3_8 (XECP_SUPP_USB3_8)—Offset 8040h

XECP SUPP USB3_8

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 13800128h

Bit Range	Default and Access	Field Name (ID): Description
31:16	1380h RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	8h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

18.2.48 XECP SUPP USB3_9 (XECP_SUPP_USB3_9)—Offset 8044h

XECP SUPP USB3_9

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 5B10129h

Bit Range	Default and Access	Field Name (ID): Description
31:16	5B1h RO	**Protocol Speed ID Mantissa (PSIM):** Protocol Speed ID Mantissa
15:9	0h RO	Reserved.
8	1h RO	**PSI Full Duplex (PFD):** PSI Full Duplex
7:6	0h RO	**PSI Type (PLT):** PSI Type
5:4	2h RO	**Protocol Speed ID Exponent (PSIE):** Protocol Speed ID Exponent
3:0	9h RO	**Protocol Speed ID Value (PSIV):** Protocol Speed ID Value

18.2.49 Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h

Host Control Scheduler

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 140h

Bit Range	Default and Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12:11	0h RW	**Cache Size Control Reg (CACHE_SZ_CTRL):** 0: 64 1: 32 2,3: 16
10:9	0h RO	Reserved.
8	1h RW	**Turn on scratch_pad_en (TO_SCRATCH_PAD_EN):** Cmd Mgr: Enables scratch pad function
7	0h RW	**Scheduler Host Control Reg (STOP_SCH_UNCON):** enable check to stop scheduling on port that are not connected
6	1h RW	**disable 1 pack scheduling limit when ISO pending in present microframe (DIS_SCH_LIMIT):** disable 1 pack scheduling limit when ISO pending in present microframe
5:4	0h RW	**scheduler sort pattern (SCH_SORT_PATTERN):** 00 (default) search ISO ahead of interrupt within each service interval 01 - search USB2-ISO, USB3-ISO, USB2-Interrupt, USB3-Interrupt within each service interval 10 - search strictly by interval 11 - search all ISO intervals ahead interrupt intervals and within each interval, USB2 ahead of USB3

Bit Range	Default and Access	Field Name (ID): Description
3	0h RW	**enable TTE overlap prevention on interrupt OUT EPs (at cost of possible service interval slip (EN_TTE_OVERLAP_PREV_OUT):** enable TTE overlap prevention on interrupt OUT EPs (at cost of possible service interval slip
2	0h RW	**enable TTE overlap prevention on interrupt IN EPs (at cost of possible service interval slip (EN_TTE_OVERLAP_PREV_IN):** enable TTE overlap prevention on interrupt IN EPs (at cost of possible service interval slip
1	0h RW	**Disable TRM active IN EP valid check function (DIS_TRM_ACT_IN_VALID):** Disable TRM active IN EP valid check function
0	0h RW	**Disable poll delay function (DIS_POLL_DELAY):** Scheduler: Disable poll delay function

18.2.50 Power Management Control (PMCTRL_REG)—Offset 80A4h

Power Management Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 492D5094h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**Async PME Source Enable (ASYNC_PME_SRC_EN):** This field allows the async PME source to be allowed to generate PME. This is specifically required for SoCs that do not allow for any clock other than RTC to be available during RTD3.
30	1h RW	**Legacy PME Source Enable (LEGACY_PME_SRC_EN):** This field allows the legacy PME source to be used in PME generation. The legacy source in in reference to the source prior to the RTD3 changes.
29	0h RW	**Reset Warn Power Gate Trigger Disable (RESET_WARN_PWR_GATE_TRIGGER_DISABLE):** This field controls the actions taken for due to reset warn. 0 - Reset Warn will trigger a HW autonomous Power Gate 1 - Reset Warn will not trigger a HW autonomous Power Gate
28	0h RW	**CLR_PME_FLAG_PULSE_AUX_CCLK (CLR_PME_FLAG_PULSE_AUX_CCLK):** Internal PME flag Clear This Write-Only bit can be used to clear the internal PME flag. SW write to '1' will clear the PME flag. SW write to '0' will have no effect and be ignored by the controller.
27	1h RW	**Disable RTD3 power gating when in D3 (DIS_D3_PG):** Disable RTD3 power gating when in D3 and context save operation is not performed
26	0h RW	**XLFPSCOUNTSRC (XLFPSCOUNTSRC):** XLFPSCOUNTSRC (Source for LFPS OFF Counter) 0: Central RTC Counter for LFPS detection 1: Local Counter for LFPS detection
25	0h RW	**XELFPSRTC (XELFPSRTC):** XELFPSRTC (Enable LFPS Filtering on RTC) 0: Use Oscillator clock for LFPS Filtering during P3 1: Use RTC Clock for LFPS Filtering during P3
24	1h RW	**XMPHYSPGDD0I2 (XMPHYSPGDD0I2):** XMPHYSPGDD0I2 (ModPhy Sus Well Power Gate Disable for D0I2) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
23	0h RW	**XMPHYSPGDD0I3 (XMPHYSPGDD0I3):** XMPHYSPGDD0I3 (ModPhy Sus Well Power Gate Disable for D0I3) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled
22	0h RW	**XMPHYSPGDRTD3 (XMPHYSPGDRTD3):** XMPHYSPGDRTD3 (ModPhy Sus Well Power Gate Disable for RTD3) 0 : Modphy sus well power gating enabled 1 : Modphy sus well power gating disabled

Bit Range	Default and Access	Field Name (ID): Description
21:18	Bh RW	**XD3RTCPTTM (XD3RTCPTTM):** XD3RTCPTTM (D3 RTC Port Timer Tick Multiplier) This register will be the multiplication factor for determining Wake Detection Frequency and RXDET based on the XD3RTCPTTC value. If XD3RTCPTTC is 9h and this register is Bh, frequency for RXDET and H8EXIT detection while MODPHY SUS Power gating is enabled would be 99ms.
17	0h RW	**U3 LFPS Periodic Sampling ON Time Control (U3_LFPS_PRDC_SAMPLING_ON_TIME_CTRL):** This field controls the ON time for the LFPS periodic sampling for USB3 ports. 0 ON time is 2 rtc clocks 1 ON time is 3 rtc clocks Note: This field is ignored if USB3 PHY SUS Well Power Gating is enabled.
16	1h RW	**AON LFPS Detector Enable Mode (AON_LFPS_DETECTOR_EN_MODE):** 1 - Allow the LFSP Detector in AON to own LFPS detection when the port is in PS3 for U2/U3 - not RxD regardless of port ownership. 0 - Allow the LFPS Detector in AON to own the LFPS detection only when the AON owns the port and in U2/U3 - not RxD
15:8	50h RW	**SS U3 LFPS Detection Threshold (SS_U3_LFPS_DETECTION_THRESHOLD):** This field controls the threshold used to determine when a valid U3 Wake is detected through when using the unfiltered LFPS source. The value on this field will reflect the binary count required to have been detected on the counter being clocked by the unfiltered lfps source to result in a valid U3 wake detection.
7:4	9h RW	**SS_U3_LFPS_PRDC_SAMPLING_OFFTIME_CTRL (SS_U3_LFPS_PRDC_SAMPLING_OFFTIME_CTRL):** This field controls the OFF time for the LFPS periodic sampling for USB3 Ports 0x0 periodic sampling is disabled. 0x1 OFF time is 1ms 0x2 OFF time is 2ms 0xF OFF time is 15ms The ON Time is determined by the amount of time required to reliably determine if there is a valid LFPS and is HW implementation specific. A speed up mode shall be implemented where this field is in units of us. i.e. 0x1 = 1 us OFF time, 0x2 = 2 us OFF time, etc.
3	0h RW	**PS3 LFPS Source Select (PS3_LFPS_SRC_SEL):** 0 LFPS Source is unfiltered 1 LFPS Source is filtered (Rx-Elec-Idle) LFPS Source is Rx-Elec-Idle for any non PS3 state.
2	1h RW	**XHCI Engine Autonomous Power Gate Exit Reset Policy (XHC_AUTO_PWRGATE_EXITRST_POLICY):** Controls when the xHCI engine is brought out of reset due to a power ungate. 0 Engine is brought out of reset when D3 to D0 is triggered. This allows for a quick power up sequence while leaving the virtual PCIe LTSSM in L23 is power ungate is not due to D3 to D0. 1 Engine is brought out of reset along with the rest of the IP. This is required for PMC save/restore flow.
1	0h RW	**USB2 Port Wake Unit Coupling Policy (USB2_PORT_WAKE_COUPLING_POLICY):** Controls the trigger for USB2 Port Wake Units to initiate Port Level Power Off Preparation. 0 RTD3 triggered 1 - Port Triggered when in L1, L2 or Disabled, Disconnected
0	0h RW	**USB3 Port Wake Unit Coupling Policy (USB3_PORT_WAKE_COUPLING_POLICY):** Controls the trigger for USB3 Port Wake Units to initiate Port Level Power Off Preparation. 0 - RTD3 Triggered 1 - Port Triggered when in PS3 due to RxDetect, U3, U2 or Disabled

18.2.51 Host Controller Misc Reg (HOST_CTRL_MISC_REG)—Offset 80B0h

Host Controller Misc Reg

Access Method

Type: MEM Register (Size: 32 bits)

Device:

Function:

Default: 37Fh

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**USB2_LTRUPDT_DIS (USB2_LTRUPDT_DIS):** This controls the inclusion of the USB2 LTR based on link state. Setting this bit will disable USB2 LTR and will expose a NO Requirement from USB2 thus not impacting the aggregated LTR vaule for the controller.
30	0h RW	**USB2 Line State Debounce During Port Reset Policy (USB2_LINE_STATE_DEBOUNCE_DURING_PORT_RESET_POLICY):** This register controls how the debounce is enforced during the Port Reset phase. 0 do not enable the line state debounce during port reset. 1 enable the line state debounce during port reset.
29	0h RW	**TTE PEXE Credit Fix Disable (TTE_PEXE_CREDIT_FIX_DISABLE):** When set, it disables a fix implemented to re-deem PEXE credits when a port is disconnected
28	0h RW	**TTE Scheduling policy (TTE_SCHEDULING_POLICY):** This register controls a fix made to prevent over-scheduling by not account for 188B in each uFrame. Setting this bit will disable the fix and allow for over-scheduling.
27	0h RW	**USB3 ITP Delta Timer Source Select (USB3_ITP_DELTA_TIMER_SOURCE_SELECT):** This register selects the source for the delta timer tracking used for ITP generation. 0 the source is a 16.666 ns tick generated from a crystal reference clock 1 - the source is a 16.666 ns tick generated from the aux_cclk. This field needs to remain in sync with Frame Timer Source Select to ensure the are both set or both cleared. There is no support for any other combination.
26	0h RW	**Frame Timer Source Select (FRAME_TIMER_SOURCE_SELECT):** This register controls the source for the frame timer. 0 the source for the frame timer is a crystal reference clock 1 the source for the frame timer is the aux_cclk.
25	0h RW	**uFrame Masking Enable (UFRAME_MASKING_ENABLE):** If set, enables the uFrame tick to be masked due to ports being in U3/NC. This controls a fix made to disable the auto masking of uFrame tick due to port state w/o any pipeline idle condition. When cleared, we rely on gating of frame timer due to proper port state and idleness tracking from the pipeline.
24	0h RW	**Late FID Check Disable (LATE_FID_CHECK_DISABLE):** This register disables the Late FID Check performed when starting an ISOCH stream.
23:20	0h RO	Reserved.
19	0h RW	**USB2 Resume Cx Inhibit Disable (USB2_RESUME_CX_INHIBIT_DISABLE):** Controls if USB2 L1 Resume is allowed to contribute to DMA Active which will inhibit Cx state. 0 USB2 L1 Resume is allowed to inhibit Cx via DMA Active 1 USB2 L1 Resume is NOT allowed to inhibit Cx via DMA Active When cleared, Cx will only be inhibited when the DMA traffic for the port begins.
18	0h RW	**LATE_FID_TTE_DIS:** Late FID TTE Disable 0: Late Frame ID Check is enabled for TTE Endpoints 1: Late Frame ID Check is disabled for TTE Endpoints
17	0h RW	**Late FID uframe Check Disable (LATE_FID_UFRAME_CHK_DIS):** 0 Frame ID Match only asserts in uframe 7 for non-TTE Endpoints Frame before match 1 Frame ID Match can assert in any uframe
16	0h RW	**Late FID Extra Interval (LATE_FID_EXTRA_INTER):** This register controls the extra number of intervals added onto the advancing of late FID check escentially a bias used to correct for possible errors in implementation
15:0	37Fh RW	**Valid Isoch Scheduling Range (VALID_ISOCH_SCHEDULING_RANGE):** This register defines the window in miliseconds from the current Frame that will be considered for scheduling in an upcoming Frame. Anything scheduled outside of this window will be considered as late and will trigger the Missed Service Error.

18.2.52 Host Controller Misc Reg2 (HOST_CTRL_MISC_REG2)—Offset 80B4h

Host Controller Misc Reg2

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:26	0h RO	Reserved.
25	0h RW	**ltm_belt_valid_clr (LTM_BELT_VALID_CLR):** ltm_belt_valid_clr
24	0h RW	**cfg_trm_drop_sch_req_dis (CFG_TRM_DROP_SCH_REQ_DIS):** cfg_trm_drop_sch_req_dis
23	0h RW	**cfg_trm_drop_tte_req_dis (CFG_TRM_DROP_TTE_REQ_DIS):** cfg_trm_drop_tte_req_dis
22	0h RW	**cfg_trm_edtla_clr_dis (CFG_TRM_EDTLA_CLR_DIS):** cfg_trm_edtla_clr_dis
21	0h RW	**cfg_xfer_is_serve_chk_en (CFG_XFER_IS_SERVE_CHK_EN):** Enable checking is_serve condition in XFER, mainly for undoing fix if needed
20	0h RW	**cfg_cpl_npkt0_fc_dis (CFG_CPL_NPKT0_FC_DIS):** Set low to allow receiving ACK with NUMP>0 to bring the TRM out of Remote Flow Control
19:18	0h RO	Reserved.
17	0h RW	**Disable IDT credit leak fix (CFG_DIS_ODMA_IDT_CRD_LEAK_FIX):** Disable the IDT credit leak fix in odma. 0 Fix is enabled 1 Fix is disabled
16	0h RW	**cfg_idma_ttype_chk_dis (CFG_IDMA_TTYPE_CHK_DIS):** Set to disable packet Transfer Type checking in IDMA
15	0h RW	**HC Reset Controller Isolation Disable (HCRST_CTRL_ISOL_DISABLE):** Setting this bit to 1 will disable the HC Reset based quiescing/isolation flow
14	0h RW	**cfg_dis_idma_perf_fix (DISABLE_IDMA_PERF_FIX):** Fix is enabled by default 0 - fix is enabled 1 - fix is disabled
13:0	0h RO	Reserved.

18.2.53 Super Speed Port Enable (SSPE_REG)—Offset 80B8h

Super Speed Port Enable

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW	**SSPE_REG (SSPE_REG):** USB3 Port Enable This field controls whether SuperSpeed capability is enabled for a given USB3 port. When set to 1, Enables SS termination Enables PORTSC to to see the connects on the ports. When set to 0, Disables SS termination Blocks PORTSC from reporting attach/connect. Places port in the lowest power state.

18.2.54 AUX Power Management Control (AUX_CTRL_REG1)—Offset 80E0h

AUX Power Management Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8080BCE0h

Bit Range	Default and Access	Field Name (ID): Description
31	1h RW	**D3 Hot function enable register (D3_HOT_FXN_EN):** This bit is from pin input which is set 1. But we allow software to alter it if it is needed. 1: D3 hot enabled 0: D3 hot not abled.
30	0h RW	**Allow L1 Core Clock Gating (ALL_L1_CORE_CG):** When set to 1 allows core clock being gated during L1 state.
29	0h RW	**Allow Engine PHY Status Extension (AL_EP_SEXT):** When set to 1 allows the engine to extend PHY status of PCIe PIPE for one more cycle. This is due to the fact that our rate change function has a potential of not being able to sample the phystatus signal.
28	0h RW	**Allow Engine PCIe Rate Change Passing (ALL_EP_RCP):** When set to 1 allows the engine to pass PCIe rate change signal as it is from PCIe core to PCIe PHY.
27	0h RW	**Allow Engine PERST Fundamental Reset (AL_PERST_FRST):** When set to 1 allow engine to treat PERST# as a fundamental reset
26	0h RW	**Overwrite PCIe P2 to P1 (OVR_PCIE_P2_P1):** When set to 1 will overwrite a PCIe powerdown state of P2 to P1.
25	0h RW	**Set Internal SSV 1 (SET_ISSV_1):** When set to 1 set the internal SSV to 1.
24	0h RW	**Clear Internal SSV 0 (CLR_ISSV_0):** When set to 1 clear the internal SSV to 0.
23	1h RW	**Enable save_restore_enable SW Loading (EN_SRE_SW_LD):** This is a bit that enables the save_restore_enable signal being loaded when a software command has set Save bit. This is a debug function.
22	0h RO	Reserved.
21	0h RW	**Force save_restore 1 (FORCE_SR1):** When set to 1, it will force the save_restore flag to 1. This flag is an bit to ensure that we have masked the update during low power state. If software write this bit to 1, it must write it to 0 in order to resume the normal save and restore function.
20	0h RO	Reserved.
19	0h RW	**cfg iob drivestrength[1] (CIDS1):** Controls the drive strength of the IO buffer
18	0h RW	**cfg iob drivestrength[0] (CIDS0):** Controls the drive strength of the IO buffer
17	0h RW	**cfg_dis_arc_RXDP3 (CFG_DIS_ARC_RXDP3):** When set to '1' DIsables arc to RXDET_p3 on disc from U2P3/U3
16	0h RW	**cfg clk gate dis (CCGD):** 1: Disable USB3 port clock gating 0: Enable USB3 port clock gating
15	1h RW	**Enable CFG RXDET P3 (EN_CFG_RDP3):** When set to '1' enable cfg rxdet p3

Bit Range	Default and Access	Field Name (ID): Description
14	0h RW	**Enable CFG PIPE Reset (EN_CFG_PIPE_RST):** When set to '1' enable cfg pipe rst
13	1h RW	**Enable Filter TX Idle (EN_FILT_TX_IDLE):** When set to 1 enables a filter function to TX electrical idle signal at PCie PIPE. We have a filter that will set TXelecidle signal of PCIe PIPE to 1 whenever we are in isolation state or power down transition states.
12	1h RW	**Enable Host Engine Generate PME (EN_HE_GEN_PME):** This is a global switch to whether or not eable this host engine to generate PME message.
11	1h RW	**Enable Isolation (EN_ISOL):** When set to '1' enable isolation
10	1h RW	**Enable L1 Caused P2 Overwrite (EN_L1_P2_OVR):** Set 1 to enable a new feature. This new feature is designed to use L1 as a state to identify whether we should do P2 Overwrite or not. We used to use P1 state to identify whether or not to invoke P2 overwrite function.
9	0h RW	**Enable Core Clock Gating (EN_CORE_CG):** When set to '1' disable core clock gating based on low power state entered
8	0h RW	**Enable PHY Status Timeout (EN_PHY_STS_TO):** When set to '1' enable PHY status timeout function which is designed to cover the PCIePHY issue that we may have not able to detect the PHY status toggle.
7	1h RW	**Ignore aux_pm_en PCIe Core (IGN_APE_PC):** When set to '1' ignore the aux_pm_en reg from PCIe core to continue the remote wake/clock switching support
6	1h RW	**Enable P2 Overwrite P1 (EN_P2_OVR_P1):** When set to '1' enable P2 overwrite P1 when PCIe core has indicated the transition from P0 to P1. This is to enable entering the even lower power state.
5	1h RW	**Enable P2 Remote Wake (EN_P2_REM_WAKE):** When set 1 '1' enable the remote wake function by allowing P2 clock/switching and P2 entering
4:1	0h RW	**Forced PM State (FORCED_PM_STATE):** Forced PM state
0	0h RW	**Initiate Force PM State (INIT_FPMS):** When set to '1' force PM state to go to the state indicated in bit 4:1

18.2.55 SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)—Offset 80ECh

SuperSpeed Port Link Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 18000C00h

Bit Range	Default and Access	Field Name (ID): Description
31:27	3h RW	**Force LTSSM State (FORCE_LTSSM_ST):** LTSSM state to be forced This value is for test purpose only.
26	0h RW	**Direct Link LTSSM State (DL_LTSSM_ST):** 0: Normal operation mode 1: Direct link to a specific state specified by bit 31:27 This bit is for test purpose only. It shall be written 0 in normal operation mode.
25	0h RW	**Direct Link To U0 (DL_U0):** 0: Normal operation mode 1: Direct link to U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.

Bit Range	Default and Access	Field Name (ID): Description
24:21	0h RW	**Forced Compliance Pattern (FORCED_CMP_PAT):** Compliance pattern to be forced to enter compliance mode This value is for test purpose only.
20:17	0h RO	Reserved.
16:15	0h RW	**PHY Low Power Latency (PHY_LP_LAT):** This field defines the latency to drive the PHY to enter low power mode 0: 4 cycles 1: 8 cycles 2: 16 cycles 3: 32 cycles
14:12	0h RW	**Link Recovery Minimum Time (LR_MIN_TM):** This value defines the minimum time for the link to stay in Recovery.Active other than from U3. The granuity is 128us.
11:9	6h RW	**Link Polling Minimum Time (LP_MIN_TM):** This value defines the minimum time for the link to stay in Polling.Active and Recovery.Active from U3. The granuity is 128us.
8	0h RW	**Force Link Accept PM Command (FORCE_LA_PMC):** 0: Normal operation mode 1: Force link to accept power management command
7	0h RW	**Direct Link Recovery U0 (DL_REC_U0):** 0: Normal operation mode 1: Direct link to Recovery from U0
6	0h RW	**Link Fast Training Mode (LINK_FTM):** 0: Normal operation mode 1: Link fast training mode This bit should be written 0 in normal operation.
5	0h RW	**Disable Link Scrambler (DIS_LINK_SCRAM):** 0: Enable link scrambler 1: Disable link scramber
4	0h RW	**Direct Link U3 From U0 (DL_U3_U0):** 0: Normal operation mode 1: Direct link to U3 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
3	0h RW	**Direct Link U3 From U0 (DL_U2_U0):** 0: Normal operation mode 1: Direct link to U2 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
2	0h RW	**Direct Link U3 From U0 (DL_U1_U0):** 0: Normal operation mode 1: Direct link to U1 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
1	0h RW	**Enable Link Loopback Master Mode (EN_LINK_LB_MAST):** 0: Disable link loopback master mode 1: Enable link loopback master mode
0	0h RW	**Disable Link Compliance Mode (DIS_LINK_CM):** 0: Enable link compliance mode 1: Disable link compliance mode

18.2.56 USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)—Offset 80F0h

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 314803A0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	31h RW	**FS/LS Mode SE0 Disconnect Delay[7:0] (FSLS_SE0_DIS_DEL_7_0):** # of microseconds of SE0 in FS/LS mode to register disconnect had occurred.
23	0h RW	**EN_SNPS_PHY_FIX (EN_SNPS_PHY_FIX):** Enable SNPS PHY Fix: 1: When set, termselect will assert at the start of EOR. Fslsserialmode will also deassert at the same clock as txenb. 0: Legacy behavior for Intel PHY.
22	1h RW	**EN_L1_DISC_IN_L0 (EN_L1_DISC_IN_L0):** Enable Pseudo L0 state when transition from L1 to L2 due to disconnect: 1: When set, {L1 suspendm, L2 suspendm} will go from 01->11->10 to allow the USB2 PHY to exit L1 and enter L2 for deeper PM 0: Legacy behavior (01->10)
21	0h RW	**DIS_PURGE_ON_SETUP_FIX (DIS_PURGE_ON_SETUP_FIX):** To disable the fix for SETUP purge that match for both device address and endpoint number: 0: Only allow purge for SETUP when both device address and endpoint number are matched. 1: Revert back to old behaviour that purge is allowed when either device address or endpoint number is matched.
20	0h RW	**L1_EXIT_RECOVERY_MODE (L1_EXIT_RECOVERY_MODE):** Mode for extended L1 Exit recovery delay: 0: 12us 1: 50us
19	1h RW	**L1_TO_INCR_MODE (L1_TO_INCR_MODE):** Mode select for L1 Timeout increments: 0: time out increments are in 125us 1: L1 Timeout increments are in 256us. Refer to USB2 PORTHLPMC.L1 Timeout in XHCI Spec for additional details
18	0h RO	Reserved.
17	0h RW	**EN_DETECT_NOMINAL_PKT_EOP (EN_DETECT_NOMINAL_PKT_EOP):** 0: Detect minimal packet EOP. 1: Detect nominal packet EOP.
16	0h RW	**Disable Chirp Response (DIS_CHIRP_RESPONSE):** 0: Normal 1: Force full speed on host ports (disable chirp response)
15	0h RW	**Disable 192 Byte Limit Check (DIS_192B_LIM):** 0: Enforce 192 byte limit on complete-split INs. Treat any packet) 192 as babble case. 1: Disable 192 byte limit check.
14	0h RW	**External Provided FS/LS Disconnect (EXT_FSLS_DIS):** 0: Internal FS/LS Disconnect from linestate(1:0) 1: External provided FS/LS Disconnect from hostdisconnect input
13:12	0h RW	**UTMI Reset Source Select (UTMI_RST_SEL):** Select UTMI Reset Source (FRD UTMI Reset Only) 00: HCReset or Force PHY Reset or internal reset after disconnect/suspend for restart (default) 01,11: UTMI reset = ~UTMI suspendm 10: UTMI reset = ~UTMI suspendm and synchronization to port clk.
11	0h RW	**Disable HS Disconnect Window (DIS_HS_DIS_WIN):** 0: Enable HS Disconnect Window Function 1: Disable HS Disconnect Window Function
10	0h RW	**Disable Port Error Detection (DIS_PERR_DET):** 0: Enable Port Error Detection (default) 1: Disable Port Error Detection
9	1h RW	**Disable Peek Function for ISO-OUT (DIS_PF_IOUT):** 0: Enable Peek function for ISO-OUT (default) 1: Disable Peek function for ISO-OUT
8	1h RW	**Drive Resume-K FS/LS Serial Interface (DRV_RESK_FSLS_SER):** 0: Drive Resume-K on parallel Interface 1: Drive Resume-K directly on FS/LS Serial Interface (default)
7	1h RW	**Enable USB2 Drop-Ping (EN_U2_DROP_PING):** 0: Disable Drop-Ping Function in USB2 Protocol (default) 1: Enable Drop-Ping Function in USB2 Protocol
6	0h RW	**Enable USB2 Force-Ping (EN_U2_FORCE_PING):** 0: Disable Force-Ping Function in USB2 Protocol (default) 1: Enable Force-Ping Function in USB2 Protocol
5	1h RW	**Enable USB2 Auto-Ping (EN_U2_AUTO_PING):** 0: Disable Auto-Ping Function 1: Enable Auto-Ping Function in USB2 Protocol (default)
4	0h RW	**Disable PHY SuspendM (DIS_PHY_SUSM):** 0: PHY is suspend=U3,U2,disconnect (default) 1: Disable PHY SuspendM in All States
3	0h RW	**UTMI Internal Clock Gate Disable (UTMI_INT_CG_DIS):** 0: Normal operation (internal clock gated in U2,U3,disconnect) 1: UTMI Internal Clock Gate Disable

Bit Range	Default and Access	Field Name (ID): Description
2	0h RW	**Disable PHY SuspendM in Disconnect State (DIS_PSUSM_DS):** 0: PHY is suspendM=0 in Disconnect State (default) 1: Disable PHY SuspendM in Disconnect State
1	0h RW	**Force PHY Reset (FORCE_PHY_RST):** 0: Normal Operation (default) 1: Force PHY Reset
0	0h RW	**USB2 Accelerated Simulation Timing (U2_ACC_SIM_TIM):** 0: Normal Operation (default - FPGA/ASIC) 1: USB2 Accelerated Simulation Timing (default - simulation)

18.2.57 USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)—Offset 80FCh

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 8003h

Bit Range	Default and Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21:9	40h RW	**U2 Detect Remote Wake Delay (U2D_RWAKE_DEL):** #of microseconds after detecting U2 remote wake condition to reflect K
8:0	3h RW	**U2 Entry Ignore Linestate Changes Duration[12:4] (U2_IGN_LS_DUR_12_4):** # of microseconds after entering U2, linestate changes are ignored as bus settles

18.2.58 Power Scheduler Control-0 (PWR_SCHED_CTRL0)—Offset 8140h

Power Scheduler Control-0

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: A019132h

Bit Range	Default and Access	Field Name (ID): Description
31:24	Ah RW	**Engine Idle Hysteresis (EIH):** This register controls the min. idle span that has to be observed from the engine idle indicators before the power state flags (xhc_*_idle) will indicate a 1.
23:12	19h RW	**Backbone PLL Shutdown Advance Wake (BPSAW):** This register controls the time before the next scheduled transaction where the Backbone PLL request will assert. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124)
11:0	132h RW	**Backbone PLL Shutdown Min. Idle Duration (BPSMID):** The sum of this register plus the Backbone PLL Shutdown Advance Wake form to a Total Idle time. When the next scheduled periodic transaction is after present time + Total Idle, the Backbone PLL request will de-assert, allowing the PLL to shutdwon. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124)

18.2.59 Power Scheduler Control-1 (PWR_SCHED_CTRL2)—Offset 8144h

These bit enable by EP type those EPs classes that are considered for determining next periodic active interval for pre-wake of the periodic_active signal. EP classes that are disabled may never be observed in setting of the periodic_active signal.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 23Fh

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9	1h RW	**HS Interrupt-OUT Alarm (HS_INT_OUT_ALRM):** HS Interrupt OUT Alarm
8	0h RW	**HS Interrupt-IN Alarm (HS_INT_IN_ALRM):** HS Interrupt IN Alarm (HSII):Note: This is required to be set to enable the functionality behind the PCICFG.HSCFG2.HSIIPAPC method of tracking HS Intr IN EPs for Periodic Active.
7	0h RW	**SS Interrupt-OUT FC Alarm (SS_INT_OUT_FC_ALRM):** SS Interrupt OUT Alarm
6	0h RW	**SS Interrupt-IN Alarm (SS_INT_IN_FC_ALRM):** SS Interrupt IN Alarm
5	1h RW	**SS Interrupt-OUT and not in FC Alarm (SS_INT_OUT_ALRM):** SS Interrupt OUT and not in FC Frame Alarm
4	1h RW	**SS Interrupt-IN & not in FC Alarm (SS_INT_IN_ALRM):** SS Interrupt IN and not in FC Frame Alarm
3	1h RW	**HS ISO-OUT Alarm (HS_ISO_OUT_ALRM):** HS ISO-OUT Alarm
2	1h RW	**HS ISO-IN Alarm (HS_ISO_IN_ALRM):** HS ISO-IN Alarm
1	1h RW	**SS ISO-OUT Alarm (SS_ISO_OUT_ALRM):** SS ISO-OUT Alarm
0	1h RW	**SS ISO-IN Alarm (SS_ISO_IN_ALRM):** SS ISO-IN Alarm

18.2.60 AUX Power Management Control (AUX_CTRL_REG2)—Offset 8154h

AUX Power Management Control Register2

Access Method

Type: MEM Register (Size: 32 bits)

Device:

Function:

Default: 1192206h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RO	Reserved.
30	0h RW	**CFG_FAST_TRAINING (CFG_FAST_TRAINING):** 0: Normal operation mode 1: Link fast training mode This bit should be written 0 in normal operation
29	0h RW	**snps_phystatus_done_l1_dis (SNPS_PHYSTATUS_DONE_L1_DIS):** snps_phystatus_done_l1_dis
28	0h RO	Reserved.
27	0h RW	**batt_charge_d3_en (BATT_CHARGE_D3_EN):** batt_charge_d3_en
26	0h RW	**cfg_debounce_en (CFG_DEBOUNCE_EN):** cfg_debounce_en
25	0h RO	Reserved.
24	1h RW	**Enable L1 exit notification to SNPS PCIe core (EN_L1_EXIT_NOTIF_PCIE):** This bit enables a L1 exit notification to SNPS PCIe core. There is a case where USB ports have waked up and AUX PM module has started the wakeup process. The AUX PM control state got into a wait for P0 state because it needs to wait until PCie core to signal powerdown state change. Due to the fact that the core is in D3Hot, there is no run_stop bit set such that no internal interrupt will be fired. This causes the LTSSM of PCIe stayed in L1 even though AUX PM has known that it needs an L1 exit. This bit works together with bit21 of this register. 1: enables this feature 0: disables this feature.
23	0h RW	**DISABLE PLC ON DISCONNECT (DIS_PLC_ON_DISCONNECT):** 1: do not assert PLC for disconnection 0: assert PLC for disconnection
22	0h RW	**TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2 (TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2):** This bit enables a feature in PCie core LTSSM to treat IDLE received as TS2 when LTSSM is in wait for TS2 receive state. This is a function requested from PHY where it is possible to not able to receive TS2 without error. 1: treat Logic IDLE as TS2 received when in some PCIe LTSSM state. 0: disable this feature.
21	0h RW	**Disable p2 overwrite due to the D3HOT where PCIe core enters the L1 (DIS_P2_OVERWRITE_DUE2_D3HOT):** We added a feature where if PCIe core LTSSM enters L1 due to the D3hot, the aux PM control will not start a P2 overwrite function in anticipating for the next L23 enter. 1: disables p2 overwrite due to the D3HOT where PCIe core enters the L1. 0: enables P2 overwrite even if we are in D3Hot.
20	1h RW	**Enable the port to enter U3 automatically when in U1/U2 (ENABLE_AUTO_U3_ENTRY_FROM_U2_U3):** 1: enables the port to enter U3 automatically when in U1/U2 0: disables the port to enter U3 automatically when in U1/U2
19	1h RW	**No linkdown reset is issue during low power state (DIS_LINKDOWN_RST_DURING_LOW_POWER):** No linkdown reset is issue during low power state
18	0h RW	**EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0 (EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0):** This bit enables a feature in AUX PM module where if PCIe core LTSSM is in P0 for a duration of time, we will exit the deep sleep state. This is for failure control in case. 1: enables this feature 0: disable this feature

Bit Range	Default and Access	Field Name (ID): Description
17	0h RW	**U2_EXIT_LFPS_TIMER_VALUE (U2_EXIT_LFPS_TIMER_VALUE):** This bit selects U2 exit LFPS timer value 0: 320ns 400ns in 25MHz domain 1: 240ns 320ns in 25MHz domain
16	1h RW	**EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP (EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP):** This bit enables a function that AUX PM module exits from the deep sleep state due to the USB ports wakeup level signal. We have added this feature where USB ports will generated a wakeup level signal to wakeup the AUX PM module if it is in deep sleep state and this level signal will be cleared if the change bits are updated by software. 1: enables this function 0: disables this function which means that a wakeup pulse generated from each USB PortSC event will wake up the AUX PM module from deep sleep if the D3 state is programmed.
15:14	0h RW	**P3_ENTRY_TIMEOUT (P3_ENTRY_TIMEOUT):** This field defines the timeout value to enter P3 mode in U2. 00: 7us 8us 01: 511us 512us 10: disables the timer (0us) 11: disables the timer (0us)
13	1h RW	**Enable U2 P3 Mode (EN_U2_P3):** 0: Disable U2 P3 mode 1: Enable U2 P3 mode
12:11	0h RW	**Fine Debug Mode Select (FINE_DM_SEL):** Fine Debug Mode Select
10	0h RW	**Enable Low Power State Based Core Clock Gating (EN_LP_CORE_CG):** When set to '1' enable core clock gating based on low power state entered
9	1h RW	**Disable USB3 Port Status Changed Event (DIS_U3_PORT_SCE):** 0: Enable USB3 port status change event generation if any change bit is not cleared 1: Disable USB3 port status change event generation if any change bit is not cleared Bit 12 default 0
8:4	0h RW	**Debug Mode Select Register (DEB_MODE_SEL):** Debug Mode Select Register
3	0h RW	**Enable Auto Wakeup Non-IDLE (EN_AWAK_NIDLE):** When set to 1 enables the auto wakeup function when engine has identified non IDLE condition.
2	1h RW	**Enable PM Control P1 Exit P2 (EN_PMC_P1_EXIT_P2):** When set 1 enables the PM control module to transition to P1 instead of P0 when exit P2.
1	1h RW	**Enable PCIe PIPE CLK Isolation (EN_PP_CLK_ISOL):** When set to 1 enables the PCIe PIPE CLK to be isolated when main power is removed.
0	0h RW	**Enable P2 Overwrite P1 Allowed Detect (EN_P2OVRP1_ADET):** When set to 1 enables a function that can detect whether or not enable P2 overwrite P1 function. The condition to get to P2 overwrite is when engine is in idle conditions. This means that there is no ISO EP pending.

18.2.61 USB2 PHY Power Management Control (USB2_PHY_PMC)—Offset 8164h

USB2 PHY Power Management Control

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: FCh

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	1h RW	**EN_CMDM_TXRXB (EN_CMDM_TXRXB):** Enable Command Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy
6	1h RW	**EN_TTE_TXRXB (EN_TTE_TXRXB):** Enable TTE Active indication for Tx/Rx Bias circuit HS Phy PM Policy
5	1h RW	**EN_IDMA_TXRXB (EN_IDMA_TXRXB):** Enable IDMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
4	1h RW	**EN_ODMA_TXRXB (EN_ODMA_TXRXB):** Enable ODMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
3	1h RW	**EN_TRM_TXRXB (EN_TRM_TXRXB):** Enable Transfer Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy
2	1h RW	**EN_SCH_TXRXB (EN_SCH_TXRXB):** Enable Scheduler Active indication for Tx/Rx Bias circuit HS Phy PM Policy
1	0h RW	**Enable Rx Bias ckt disable (EN_RXB_CD):** When set enables the Rx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits)
0	0h RW	**Enable Tx Bias ckt disable (EN_TXB_CD):** When set enables the Tx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits)

18.2.62 XHCI Aux Clock Control Register (XHCI_AUX_CCR)—Offset 816Ch

XHCI Aux Clock Control Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: F4038h

Bit Range	Default and Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19	1h RW	**USB3 Partition Engine/Link trunk gating Enable (PARUSB3_ENG_GEN):** When set to 1 enables gating of the SOSC trunk to the XHCI engine and link in the PARUSB3 partition.
18	1h RW	**USB3 Partition Frame Timer trunk gating Enable (PARUSB3_LINK_GEN):** When set to 1 enables gating of the SOSC trunk to the Frame timer in the PARUSB3 partition.
17	1h RW	**USB2 link partition clock gating enable (PARUSB2_CLK_GEN):** When set to 1 enables gating of the SOSC trunk to the USB2 link and Phy logic in the PARUSB2 partition.
16	1h RW	**USB2/USHIP 12.5 MHz partition clock gating enable (USHIP_PCGEN):** When set to 1 enables gating of the 12.5 MHz SOSC trunk to the USB2 and USHIP logic in the PARUSB2 partition.
15	0h RO	Reserved.
14	1h RW	**USB3 Port Aux/Core clock gating enable (USB3_AC_CGE):** When set, allows the aux_cclk clock into the USB3 port to be gated when conditions are met.

Bit Range	Default and Access	Field Name (ID): Description
13:12	0h RW	**Rx Detect Timer when port Aux Clock is Gated (RX_DT_ACG):** This field defines the value of the timer used to perform Rx Detect when port Aux Clock has been gated. 0x0: 100ms 0x1: 12ms Others: Reserved Note: This timer shall use the Fast Training Timer Tick (about 1us tick) for simulation purposes. For Fast Training mode, the above timeouts will become about 11us and about 100us, +/- implementation uncertainty, respectively.
11:10	0h RO	Reserved.
9	0h RW	**Aux Clock Gating Counter PipeStage Enable (AUXCLKGT_CNTEN_PIPE_STGEN):** Policy to enable pipe stage on cnten of aux_clk and frame_clk gating logic
8	0h RO	Reserved.
7	0h RW	**Frame Timer Clock Gating Ports in U2 Enable (FTCGPU2E):** This bit, when set, allows Host Controller to gate the clock to the Frame Timer when ports are in U2.
6	0h RW	**USB2 port clock throttle enable (USB2_PC_TE):** When set, allows the Aux clock into the USB2 ports to be throttled when conditions allow.
5	1h RW	**XHCI Engine Aux clock gating enable (XHCI_AC_GE):** When set, allows the aux clock into the XHCI engine to be gated when idle.
4	1h RW	**XHCI Aux PM block clock gating enable (XHCI_APMB_CGE):** When set, allows the aux clock into the Aux PM block to be gated when idle.
3	1h RW	**USB3 Aux Clock Trunk Gating Enable (USB3_AC_TGE):** When set, allows Aux Clock Trunk feeding to USB3.0 ports to be gated when port Aux clock is gated at all USB3.0 ports and all USB3.0 modPHY instances.
2	0h RO	Reserved.
1	0h RW	**ModPHY port Aux clock gating enable in U2 (MPP_AC_GEU2):** When set, allows the aux clock into the ModPhy to be gated when Link is in U2 and pipe has been in PS3 for at least the time defined by U2 Residency Before ModPHY Clock Gating field.
0	0h RW	**ModPHY port Aux clock gating enable in Disconnected, U3 or Disabled (MPP_AC_GE_DDU3):** When set, allows the aux clock into the ModPHY to be gated when Link is in Disconnected, U3 or Disabled state.

18.2.63 XHC Latency Tolerance Parameters LTV Control (XLTP_LTV1)—Offset 8174h

XHC Latency Tolerance Parameters LTV Control

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 1400C01h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW	**Disable scheduler direct transition from IDLE to NO requirement (DIS_SDT_IDL_NR):** 0: (default) allow scheduler direct transition from IDLE to NO requirement 1: Disable scheduler direct transition from IDLE to NO requirement
30:26	0h RO	Reserved.
25	0h RW	**XHCI LTR Transition Policy (XLTRTP):** When '0', LTR messaging state machine transitions from High, Medium, or Low LTR states to Active state upon the Alarm Timer timout and stays in Active until the next service boundary. When '1', the LTR messaging state machine transitions through High Med Low Active states assuming enough latency is available for each transition.
24	1h RW	**XHCI LTR Enable (XLTRE):** This bit must be set to enable LTV messaging from XHCI to the PMC.
23:12	400h RW	**Periodic Active LTV (PA_LTV):** 23:22 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 21:12 Latency Value (ns) Defaults to 0 micro seconds
11:0	C01h RW	**USB2 Port L0 LTV (USB2_PL0_LTV):** 11:10 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 9:0 Latency Value (ns) Defaults to 128 Micro Seconds

18.2.64 XHC Latency Tolerance Parameters High Idle Time Control (XLTP_HITC)—Offset 817Ch

XHC Latency Tolerance Parameters High Idle Time Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 50002h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:16	5h RW	**Minimum High Idle Time (MHIT):** This is the minimum schedule idle time that must be available before a "High" LTR value can be indicated. This value must be larger than HIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	0h RO	Reserved.
12:0	2h RW	**High Idle Wake Latency (HIWL):** This is the latency to access memory from the High Idle Latency state. This value must be larger than MIWL and LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

18.2.65 XHC Latency Tolerance Parameters Medium Idle Time Control (XLTP_MITC)—Offset 8180h

XHC Latency Tolerance Parameters Medium Idle Time Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 50002h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:16	5h RW	**Minimum Medium Idle Time (MMIT):** This is the minimum schedule idle time that must be available before a "Medium" LTR value can be indicated. This value must be larger than MIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	0h RO	Reserved.
12:0	2h RW	**Medium Idle Wake Latency (MIWL):** This is the latency to access memory from the Medium Idle Latency state. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

18.2.66 XHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)—Offset 8184h

XHC Latency Tolerance Parameters Low Idle Time Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 50002h

Bit Range	Default and Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:16	5h RW	**Minimum Low Idle Time (MLIT):** This is the minimum schedule idle time that must be available before a "Low" LTR value can be indicated. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15:13	0h RO	Reserved.
12:0	2h RW	**Low Idle Wake Latency (LIWL):** This is the latency to access memory from the Medium Idle Latency state. 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

18.2.67 LFPS On Count (LFPSONCOUNT_REG)—Offset 81B8h

LFPS On Count

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 20C8h

Bit Range	Default and Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17:16	0h RW	**U2P3 LFPS Periodic Sampling Control (XU2P3LPSC):** This field controls the OFF time for the LFPS periodic sampling for SS port in U2P3. If LFPSPM for a port is 1, it will override the OFF time and LFPS receiver will remain OFF permanently. For Fast Sim mode, 500us will be equivalent to 5us. 0x0 Polling Disable. (RXDET Polling will become 100ms.) 0x1 500us OFF Time 0x2 1ms OFF Time 0x3 1.5ms OFF Time
15:10	8h RW	**XLFPSONCNTSSIC (XLFPSONCNTSSIC):** This time would describe the number of clocks LFPS will remain ON. LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 8.
9:0	C8h RW	**XLFPSONCNTSS (XLFPSONCNTSS):** This time would describe the number of clocks LFPS will remain ON. LFPS detection operation may be carried out on using RTC clock or Oscillator clock. The value of this register should be adjusted accordingly. For RTC recommended value is 2. For Oscillator clock, recommended value is 200.

18.2.68 USB2 PM Control (USB2PMCTRL_REG)—Offset 81C4h

USB2 Power Management Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 908h

Bit Range	Default and Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h RW	**Bypass Suspend SM (BYPSUSSM):** 1: When set, Suspend SM is bypassed and L1/L2 suspendm from the controller goes directly to the PHY 0: When cleared, Suspend SM controls the L1/L2 suspendm to the PHY
12	0h RO	Reserved.
11	1h RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2PSPGPSCBP):** This controls the policy for blocking PORTSC Updates while the USB2 PHY SUS Well is power gated. When set, the controller will block any updates to the PORTSC caused by port status change if the USB2 PHY SUS is power gated.
10:8	1h RW	**USB2 PHY SUS Well Power Gate Entry Hysteresis Count (U2PSPGEHC):** This controls the amount of hysteresis time the controller will enforce after detecting the USB2 PHY SUS Power Gate entry condition. 0h 0 clocks 1h 32 clocks 2h 64 clocks 3h 128 clocks 4h 256 clocks 5h 512 clocks 6h 1024 clocks 7h 2048 clocks

Bit Range	Default and Access	Field Name (ID): Description
7:4	0h RW	**USB2 PHY SUS Power Gate PORTSC Block Policy (U2CLPGLAT):** This field represents the worst case latency for the USB2 Common Lane to enter and exit its power gate state. This fields is required to be compared to a ports HIRD/HIRD value for the ports that have allowed L1 to L2 mapping to determine if the Common Lane can be allowed to power off. If the power gate entry/exit latency is greater than the HIRD/HIRDD then the common lane should not be allowed to power gate as this will result in a L1 exit violation. 0h 100 us 1h 200 us 2h 300 us Eh 1500us Fh 1600 us
3:2	2h RW	**USB2 PHY SUS Well Power Gate Policy (U2PSUSPGP):** This field controls when to enable the USB2 PHY SUS Well Power Gating when the proper conditions are met. 00 USB2 PHY SUS Power Gating is Disabled. 01 USB2 PHY SUS Power Gating is Enabled in Only D0 and D0i2 (Excludes D0i3 and D3) 10 USB2 PHY SUS Power Gating is Eanabled in only in D0, D0i2 and D0i3 (Excludes D3) 11 USB2 PHY SUS Power Gating is Eanabled in D0/D0i2/D0i3/D3
1:0	0h RO	Reserved.

18.2.69 USB Legacy Support Capability (USBLEGSUP)—Offset 846Ch

This register is modified and maintained by BIOS

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2201h

Bit Range	Default and Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RW	**HC OS Owned Semaphore (HCOSOS):** Default = '0'. System software sets this bit to request ownership of the xHC. Ownership is obtained when this bit reads as '1' and the HC BIOS Owned Semaphore bit reads as '0'.
23:17	0h RO	Reserved.
16	0h RW	**HC BIOS Owned Semaphore (HCBIOSOS):** Default = '0'. The BIOS sets this bit to establish ownership of the xHC. System BIOS will set this bit to a '0' in response to a request for ownership of the xHC by system software.
15:8	22h RW/L	**Next Capability Pointer (NEXTCP):** This field indicates the location of the next capability with respect to the effective address of this capability. Refer to Table 145 for more information on this field.
7:0	1h RW/L	**Capability ID (CID):** This field identifies the extended capability. Refer to Table 146 for the value that identifies the capability as Legacy Support. This extended capability requires one additional 32-bit register for control/status information (USBLEGCTLSTS), and this register is located at offset xECP+04h.

18.2.70 Port Disable Override Capability Register (PDO_CAPABILITY)—Offset 84F4h

Port Disable Override Capability Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 3C6h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	3h RW/L	**Next Capability Pointer (NCP):** Next Capability Pointer
7:0	C6h RW/L	**Capability ID (CID):** Capability ID

18.2.71 Debug Capability ID Register (DCID)—Offset 8700h

This register is modified and maintained by BIOS

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 5100Ah

Bit Range	Default and Access	Field Name (ID): Description
31:21	0h RO	Reserved.
20:16	5h RW/L	**Debug Capability Event Ring Segment Table Max (DCERSTM):** Note: This register is sticky.
15:8	10h RW/L	**Next Capability Pointer (NCP):** Note: This register is sticky.
7:0	Ah RW/L	**Capability ID (CID):** Note: This register is sticky.

18.2.72 Global Time Sync Capability (GLOBAL_TIME_SYNC_CAP_REG)—Offset 8E10h

GLOBAL TIME SYNC CAP REG

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 12C9h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	12h RW/L	**Next Capability pointer (NCP):** Next Capability pointer
7:0	C9h RW/L	**Capability ID (CID):** Capability ID

18.2.73 Global Time Sync Control (GLOBAL_TIME_SYNC_CTRL_REG)—Offset 8E14h

GLOBAL TIME SYNC CTRL REG

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/1S	**Time Stamp Counter Capture Initiate (TIME_STAMP_CNTR_CAPTURE_INITIATE):** SW sets this bit to initiate a time capture. Once the time capture is complete and the time values are valid in the Local and Global time capture registers, HW clears the bit.

18.2.74 Microframe Time (Local Time) (MICROFRAME_TIME_REG)—Offset 8E18h

MICROFRAME TIME REG

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:30	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
29:16	0h RO	**Captured Frame List Current Index/Frame Number (CMFI):** The value in this register is updated in response to sample_now signal. Bits [29:16] reflect state of bits [13:0] of FRINDEX
15:13	0h RO	Reserved.
12:0	0h RO	**Captured Micro-frame BLIF (CMFB):** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done via Bus Interval Adjust (BIA).

18.2.75 Global Time Low REG (GLOBAL_TIME_LOW_REG)—Offset 8E20h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	**GLOBAL_TIME_LOW_REG (GLOBAL_TIME_LOW)**: Global Time Value (Low)

18.2.76 Global Time High REG (GLOBAL_TIME_High_REG)—Offset 8E24h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	**GLOBAL_TIME_HI_REG (GLOBAL_TIME_HI)**: Global Time Value (High)

18.2.77 XHCI USB2 Overcurrent Pin Mapping (U2OCM1)—Offset 90A4h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/L	**OC Mapping (OCM):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored.

18.2.78 XHCI USB2 Overcurrent Pin Mapping (U2OCM2)—Offset 90A8h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/L	**OC Mapping (OCM):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored.

18.2.79 XHCI USB2 Overcurrent Pin Mapping (U2OCM3)—Offset 90ACh

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/L	**OC Mapping (OCM):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored.

18.2.80 XHCI USB2 Overcurrent Pin Mapping (U2OCM4)—Offset 90B0h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/L	**OC Mapping (OCM):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored.

18.2.81 XHCI USB2 Overcurrent Pin Mapping (U2OCM5)—Offset 90B4h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/L	**OC Mapping (OCM):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored.

18.2.82 XHCI USB2 Overcurrent Pin Mapping (U2OCM6)—Offset 90B8h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/L	**OC Mapping (OCM):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored.

18.2.83 XHCI USB2 Overcurrent Pin Mapping (U2OCM7)—Offset 90BCh

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/L	**OC Mapping (OCM):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored.

18.2.84 XHCI USB2 Overcurrent Pin Mapping (U2OCM8)—Offset 90C0h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9:0	0h RW/L	**OC Mapping (OCM):** USB2 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB2 std. port 1 Bit 1 maps the OC pin N to USB2 std port 2 ... Bit (NumUSB2std-1) maps the OC pin N to USB2 Std port NumUSB2std Note: The USB-R port which is the most significant USB2 port does not have an OC pin. Thus the OC assignment for the USB-R port is ignored.

18.2.85 XHCI USB3 Overcurrent Pin Mapping (U3OCM1)—Offset 9124h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/L	**OC Mapping (OCM):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std. port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std

18.2.86 XHCI USB3 Overcurrent Pin Mapping (U3OCM2)—Offset 9128h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/L	**OC Mapping (OCM):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std. port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std

18.2.87 XHCI USB3 Overcurrent Pin Mapping (U3OCM3)—Offset 912Ch

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/L	**OC Mapping (OCM):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std. port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std

18.2.88 XHCI USB3 Overcurrent Pin Mapping (U3OCM4)—Offset 9130h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/L	**OC Mapping (OCM):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std. port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std

18.2.89 XHCI USB3 Overcurrent Pin Mapping (U3OCM5)—Offset 9134h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/L	**OC Mapping (OCM):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std. port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std

18.2.90 XHCI USB3 Overcurrent Pin Mapping (U3OCM6)—Offset 9138h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/L	**OC Mapping (OCM):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std. port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std

18.2.91 XHCI USB3 Overcurrent Pin Mapping (U3OCM7)—Offset 913Ch

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/L	**OC Mapping (OCM):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std. port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std

18.2.92 XHCI USB3 Overcurrent Pin Mapping (U3OCM8)—Offset 9140h

The RW/L property of this register is controlled by OCCFDONE bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/L	**OC Mapping (OCM):** USB3 Port assignment When Set to 1, Bit 0 maps the OC pin N to USB3 std. port 1 Bit 1 maps the OC pin N to USB3 std. port 2 ... Bit (NumUSB3std-1) maps the OC pin N to USB3 Std port NumUSB3std

18.3 USB Configuration Registers Summary

The USB Configuration Registers are distributed within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface using the following Target Port (Destination Port) Identification:

Target Port (Destination Port) Identification = 0xCA

For complete details on how to use the PCH Sideband Interface to access these PCH Private Configuration Registers reference the latest Platform Controller Hub BIOS Specification.

18.3.1 USB2 PER PORT 1 Electrical Control Register (USB2PP1)

Access Method

Type:
IOBP Index:
Port 0: CA004100h
Port 1: CA004200h
Port n: CA004n00h
(Size: 32 bits)

Device:
Function:

Default: See Below

Bit Range	Default and Access	Field Name (ID): Description
31:15	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
14	0h RW	**Per Port Half Bit Pre-emphasis (PERPORTTXPEHALF)** Configuration bit (per port) to select between half-bit or full-bit implementation 1 = select half-bit pre-emphasis 0 = select full-bit pre-emphasis Note: This bit is do not care when **Per Port HS TX Emphasis** is configured to "11"
13:11	0h RW	**Per Port HS Pre-emphasis bias (PERPORTPETXISET)**
10:8	0h RW	**Per Port HS TX Bias (PERPORTTXISET)**
7:0	0h RO	Reserved.

18.3.2 USB2 PER PORT 2 Electrical Control Register (USB2PP2)

Access Method

Type: IOBP Index: Port 0: CA004126h Port 1: CA004226h Port n: CA004n26h (Size: 32 bits)	**Device:** **Function:**

Default: See Below

Bit Range	Default and Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24:23	0h RW	**Per Port HS TX Emphasis (IUSBTXEMPHASISEN)** Enables the HS TX Emphasis for the respective port
22:0	0h RW	Reserved.

18.3.3 Global ADP VBUS COMP REG (GLB ADP VBUS COMP REG)

Access Method

Type: IOBP Index: CA00402Bh (Size: 32 bits)	**Device:** **Function:**

Default: See Below

Bit Range	Default and Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22	1h RW	**Differential Disconnect Enable** 0: Reserved. 1: Differential Disconnect - enabled
21:0	0h RW	Reserved.

18.3.4 USB2 COMPBG (USB2_COMPBG)

Access Method

Type: IOBP Index: CA007F04h (Size: 32 bits)	**Device:** **Function:**

Default: See Below

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	1h RW	**USB2 Disconnect Reference Select (UDRS)** Selects the reference voltage disconnect detector. 0: Reserved. 1: Differential Disconnect circuit.
14:13	0h RW	**USB2 AFE Squelch Reference Positive Voltage Programming (UASQRPVP)** These bits specify the programming options for USB2 AFE Squelch reference Positive voltage. 3h: 350mV 2h: 325mV 1h: 300mV 0h: 312.5mV
12:11	0h RW	**USB2 AFE Squelch Reference Negative Voltage Programming (UASQRNVP)** These bits specify the programming options for USB2 AFE Squelch reference Negative voltage. 3h: 250mV 2h: 225mV 1h: 175mV 0h: 200mV

Bit Range	Default and Access	Field Name (ID): Description
10:7	0h RW	**Differential Disconnect Reference Voltage Programming** Bit Value Vref (mV) 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: 562.5 0101: 687.5 0110: 437.5 0111: 312.5 1000: 625 1001: 750 1010: 500 1011: 375 1100: 687.5 1101: 812.5 1110: 562.5 1111: 437.5
7:0	0h RO	Reserved.

19 USB Dual Role

19.1 xDCI PCI Configuration Registers Summary

Table 19-1. Summary of xDCI PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID (DEVVENDID)—Offset 0h	AAA8086h
4h	7h	Status and Command (STATUSCOMMAND)—Offset 4h	100000h
10h	17h	Base Address Register (BAR)—Offset 10h	4h
18h	1Fh	Base Address Register1 (BAR1)—Offset 18h	4h
2Ch	2Fh	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	Interrupt Register (INTERRUPTREG)—Offset 3Ch	100h
80h	83h	Power Management Capability ID (POWERCAPID)—Offset 80h	48039001h
84h	87h	Power Management Control and Status (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
94h	97h	Device ID and Vendor Specific Register (DEVID_VEND_SPECIFIC_REG)—Offset 94h	1400010h
98h	9Bh	SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	10F8301h
A0h	A3h	(D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	80800h

19.1.1 Device ID and Vendor ID (DEVVENDID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: AAA8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	AAAh RO	**DEVICEID:** Device ID identifies the particular PCI device. Refer to the Device and Revision ID Table in Volume 1 for default value.
15:0	8086h RO	**Vendor Identification (VENDORID):** Vendor ID is a unique ID identifying the manufacturer of the device. 8086h = Intel

19.1.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**Received Master Abort (RMA):** If the completion status received from IOSF is UR, the Bridge sets this bit. Thesoftware writes a 1 to this bit to clear it.
28	0h RW/1C	**Received Target Abort (RTA):** If the completion status received from IOSF is CA, the Bridge sets this bit. Thesoftware writes a 1 to this bit to clear it.
27:21	0h RO	Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Indicates that the controller contains a capabilities pointer list. The firstitem is pointed to by looking at the configuration offset 34h.
19	0h RO	**Interrupt Status (INTR_STATUS):** This bit reflects state of interrupt in the device Only when theInterrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a1, is the device/function interrupt message sent. Setting the Interrupt Disable bit to a1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE):** Interrupt Disable: Setting this bit disables INTx assertion fromBridge. The interrupt disabled is legacy INTx# interrupt, which is the Bridge does notsend Interrupt Assert message through the IOSF Sideband Channel. Reset value ofthis bit is 0. This bit has no connection with the interrupt status bit.
9	0h RO	Reserved.
8	0h RW	**SERR Enable (SERR_ENABLE):** Not implemented
7:3	0h RO	Reserved.
2	0h RW	**Bus Master Enable (BME):** Bus Master Enable: If this bit is 0,the Bridge does not generate any newupstream transaction on IOSF as a master. Reset value of this bit is 0.
1	0h RW	**Memory Space Enable (MSE):** Memory Space Enable: This bit controls Bridge response to downstreammemory accesses. When set, accesses to memory space of the device is enabled.Reset value of this bit is 0.
0	0h RO	Reserved.

19.1.3 Base Address Register (BAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 64 bits)

Device: 20
Function: 1

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
63:21	0h RW	**Base Address Register Low (BASEADDR)**
20:12	0h RO	Reserved.
11:4	0h RO	**Size Indicator (SIZEINDICATOR):** Always returns 0. The size of this register depends on the size of the memory space.
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable
2:1	2h RO	**Type (TYPE):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range, If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0 indicates this BAR is present in the memory space.

19.1.4 Base Address Register1 (BAR1)—Offset 18h

Memory accesses to BAR1 region are aliased to the PCI configuration space. The BAR1region is always 4K. Software access through BAR1 can only access the regular PCIconfiguration space. BAR1 memory accesses, which do not access a defined PCIconfiguration register, are treated as access to reserved register. If this register isdisabled then this is RO and always returns 0.

Access Method

Type: CFG Register
(Size: 64 bits)

Device: 20
Function: 1

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RW	**Base Address high (BASEADDR1_HIGH)**
31:12	0h RW	**BASEADDR1:** This field is present if BAR1 is enabled through private configuration space.
11:4	0h RO	**Size Indicator (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not prefetchable.
2:1	2h RO	**Type (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0 Indicates this BAR is present in the memory space.

19.1.5 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SUBSYSTEMID):** This register is implemented for any function thatcan be instantiated more than once in a given system. The SID register, incombination with the Subsystem Vendor ID register make it possible for theoperating environment to distinguish one subsystem from the other. This register is aRead Write Once type register.
15:0	0h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register must be implemented for any function thatcan be instantiated more than once in a given system. The SVID register, incombination with the Subsystem ID register, enables the operating environment todistinguish one subsystem from the other. This register is a Read Write Once register

19.1.6 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 1

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is.

19.1.7 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: CFG Register (Size: 32 bits)
Device: 20
Function: 1

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Max Latency (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**Min Latency (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	Reserved.
11:8	1h RO	**Interrupt Pin (INTPIN):** Interrupt Pin Value in this register is reflected from the IPIN value in theprivate configuration space. For a single function device, this ideally is INTA.
7:0	0h RW	**Interrupt Line (INTLINE):** PCH does not use this field directly. It is used to communicate tosoftware, the interrupt line to which the interrupt pin is connected.

19.1.8 Power Management Capability ID (POWERCAPID)—Offset 80h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 48039001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	9h RO	**PMESUPPORT:**
26:19	0h RO	Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**Next Capability (NXTCAP):** Points to the next capability structure.
7:0	1h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

19.1.9 Power Management Control and Status (PMECTRLSTATUS)—Offset 84h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C	**PME Status (PMESTATUS):** 0 Software clears the bit by writing a 1 to it. 1 This bit is set when the PME# signal is asserted independent of the state of the PMEEnable bit (bit 8 in this register)
14:9	0h RO	Reserved.
8	0h RW	**PME Enable (PMEENABLE):** 1 Enables the function to assert PME#. 0 PME# message on Sideband is disabled
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state and toset a new power state.The values are: 00 D0 state 11 D3HOT state Others Reserved

19.1.10 PCI Device Idle Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP:** Vendor Specific Capability ID
27:24	0h RO	**REVID:** Revision ID of capability structure
23:16	14h RO	**CAP_LENGTH:** Vendor Specific Capability Length
15:8	0h RO	**NEXT_CAP:** Next Capability
7:0	9h RO	**CAPID:** Capability ID

19.1.11 Device ID and Vendor Specific Register (DEVID_VEND_SPECIFIC_REG)—Offset 94h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSEC_LENGTH:** Vendor Specific Extended Capability Length
19:16	0h RO	**VSEC_REV:** Vendor specific Extended Capability revision
15:0	10h RO	**VSECID:** Vendor Specific Extended Capability ID

19.1.12 SW LTR Update MMIO Location Register (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**SW_LAT_DWORD_OFFSET:** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW_LAT_BAR_NUM:** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**Valid (SW_LAT_VALID)**

19.1.13 Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 10F8301h

Bit Range	Default & Access	Field Name (ID): Description
31:4	10F830h RO	**DWORD_OFFSET:** Contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR
3:1	0h RO	**BAR Number (BAR_NUM):** Indicates that the D0i3 MMIO location is always at BAR0
0	1h RO	**Valid (VALID)**

19.1.14 (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 1

Default: 80800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW	**HAE:** Hardware Autonomous Enable
20	0h RO	Reserved.
19	1h RW	**SLEEP_EN:** Sleep Enable
18	0h RW	**D3HEN:** D3-Hot Enable (D3HEN): If 1, then the function will power gate when idle and the PMCSR[1:0] register in the function D3.
17	0h RW	**DEVIDLEN:** If 1, then the function will power gate when idle and the DevIdle register (DevIdleC[2]=1) is set.
16	0h RW	**D3_ENABLE:** D3-Hot Enable (D3HEN): If set to 1, then function will power gate when idle and the PMCSR[1:0] register in the function = 11 (D3).
15:13	0h RO	Reserved.
12:10	2h RW/O	**POW_LAT_SCALE:** Power On Latency Scale
9:0	0h RW/O	**POW_LAT_VALUE:** Power On Latency value

19.2 xDCI MMIO Device Registers Summary

Table 19-2. Summary of xDCI MMIO Device Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C700h	C703h	Device Configuration Register (DCFG)—Offset C700h	80004h
C704h	C707h	Device Control Register (DCTL)—Offset C704h	F00000h
C708h	C70Bh	Device Event Enable Register (DEVTEN)—Offset C708h	0h
C70Ch	C70Fh	Device Status Register (DSTS)—Offset C70Ch	520004h
C710h	C713h	Device Generic Command Parameter (DGCMDPAR)—Offset C710h	0h
C714h	C717h	Device Generic Command (DGCMD)—Offset C714h	0h
C720h	C723h	Device Active USB Endpoint Enable (DALEPENA)—Offset C720h	0h
C800h	C803h	Device Physical Endpoint-n Command Parameter 2 (DEPCMDPAR2)—Offset C800h	0h
C804h	C807h	Device Physical Endpoint-n Command Parameter 1 (DEPCMDPAR1)—Offset C804h	0h
C808h	C80Bh	Device Physical Endpoint-n Command Parameter 0 (DEPCMDPAR0)—Offset C808h	0h
C80Ch	C80Fh	Device Physical Endpoint-n Command (DEPCMD)—Offset C80Ch	0h

19.2.1 Device Configuration Register (DCFG)—Offset C700h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 80004h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	Reserved.
22	0h RW	**LPM Capable (LPMCAP):** The application uses this bit to control the LPM capabilities: 1'b0: LPM capability is not enabled. 1'b1: LPM capability is enabled.
21:17	4h RW	**Number of Receive Buffers (NUMP):** This bit indicates the number of receive buffers to be reported in the ACK TP.
16:12	0h RW	**Interrupt Number (INTRNUM):** Indicates interrupt number on which non-endpoint-specific device-related interrupts are generated.
11:10	0h RO	Reserved.
9:3	0h RW	**Device Address (DEVADDR)**
2:0	4h RW	**Device Speed (DEVSPD):** Indicates the speed at which the application requires the core to connect, or the maximum speed the application can support: 3’b100: SuperSpeed 3’b000: High-speed 3’b001: Full-speed

19.2.2 Device Control Register (DCTL)—Offset C704h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: F00000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Run/Stop (RUN_STOP):** The software writes 1 to this bit to start the device controller operation.To stop the device controller operation, the software must remove any active transfers and write 0 to this bit. When the controller is stopped, it sets the DSTS.DevCtrlHlt bit when the core is idle and the lower layer finishes the disconnect process. The Run/Stop bit must be used in following cases as specified: 1.After power-on reset and CSR initialization, the software must write 1 to this bit to start the device controller. The controller does not signal connect to the host until this bit is set. 2.The software uses this bit to control the device controller to perform a soft disconnect. When the software writes 0 to this bit, the host does not see that the device is connected. The device controller stays in the disconnected state until the software writes 1 to this bit. The minimum duration of keeping this bit cleared: SS: 30ms HS/FS/LS: 10ms If the software attempts a connect after the soft disconnect or detects adisconnect event, it must set DCTL[8:5] to 5 before reasserting the Run/Stopbit. 3.When the USB or Link is in a lower power state and the Two Power Rails configuration is selected, software writes 0 to this bit to indicate that it is going to turn off the Core Power Rail. After the software turns on the Core Power Rail again and re-initializes the device controller, it must set this bit to start the device controller.
30	0h RW	**Core Soft Reset (CSFTRST):** Resets the all clock domains
29	0h RO	Reserved.
28:24	0h RW	**HIRD Threshold (HIRDTHRES):** The core asserts output signals utmi_l1_suspend_n and utmi_sleep_n on the basis of this signal: The core asserts utmi_l1_suspend_n to put the PHY into Deep Low-Power mode in L1 when both of the following are true: -HIRD value is greater than or equal to the value in DCTL.HIRD_Thres[3:0] -HIRD_Thres[4] is set to 1'b1. The core asserts utmi_sleep_n on L1 when one of the following is true: -If the HIRD value is less than HIRD_Thres[3:0] or -HIRD_Thres[4] is set to 1'b0. Note: This field must be set to ‘0’ during SuperSpeed mode of operation.
23:20	Fh RW	**LPM NYET Response Threshold (LPM_NYET_thres):** Handshake response to LPM token specified by device application
19	0h RW	**Keep Connect (KeepConnect):** When '1', this bit enables the save and restore programming model by preventing the core from disconnecting from the host when DCTL.RunStop is set to '0'. It also enables the Hibernation Request Event to be generated when the link goes to U3 or L2. The device core disconnects from the host when DCTL.RunStop is set to '0'. This bit indicates whether to preserve this behavior ('0'), or if the core should not disconnect when RunStop is set to 0 ('1').This bit also prevents the LTSSM from automatically going to U0/L0 when the host requests resume from U3/L2.
18	0h RW	**L1 Hibernation Enable (L1HibernationEn):** When this bit is set along with KeepConnect, the device core generates a Hibernation Request Event if L1 is enabled and the HIRD value in the LPM token is larger than the threshold programmed in DCTL.HIRD_Thres. The core will not exit the LPM L1 state until software writes Recovery into the DCTL.ULStChngReq field. This prevents corner cases where the device is entering hibernation at the same time the host is attempting to exit L1.
17	0h RW	**Controller Restore State (CRS):** This command initiates the restore process. When software sets this bit to '1', the controller immediately sets DSTS.RSS to '1'. When the controller has finished the restore process, it sets DSTS.RSS to '0'. Note: When read, this field always returns '0'.
16	0h RW	**Controller Save State (CSS):** This command initiates the save process.When software sets this bit to '1', the controller immediately sets DSTS.SSS to '1'. When the controller has finished the save process, it sets DSTS.SSS to '0'. Note: When read, this field always returns '0'.

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h RW	**Initiate U2 Enable (INITU2ENA):** 1'b0: May not initiate U2 (default) 1'b1: May initiate U2 On USB reset, hardware clears this bit to ”0”. Software sets this bit after receiving SetFeature(U2_ENABLE), and clears this bit when ClearFeature(U2_ENABLE) is received.If DCTL[11] (AcceptU2Ena) is 0, the link immediately exits U2 state.
11	0h RW	**Accept U2 Enable (ACCEPTU2ENA):** 1'b0: Reject U2 except when Force_LinkPM_Accept bit is set (default) 1'b1: Core accepts transition to U2 state if nothing is pending on the application side.On USB reset, hardware clears this bit to ”0”. Software sets this bit after receiving a SetConfiguration command
10	0h RW	**Initiate U1 Enable (INITU1ENA):** 1'b0: May not initiate U1 1'b1: May initiate U1 On USB reset, hardware clears this bit to “0”. Software sets this bit after receiving SetFeature(U1_ENABLE), and clears this bit when ClearFeature(U1_ENABLE) is received. If DCTL[9] (AcceptU1Ena) is 0, the link immediately exits U1 state.
9	0h RW	**Accept U1 Enable (ACCEPTU1ENA):** 1'b0: Core rejects U1 except when Force_LinkPM_Accept bit is set (default) 1'b1: Core accepts transition to U1 state if nothing is pending on the application side. On USB reset, hardware clears this bit to “0”. Software sets this bit after receiving a SetConfiguration command.
8:5	0h WO	**USB / Link State Change Request (ULSTCHNGREQ):** Software writes this field to issue a USB/Link state change request. A change in this field indicates a new request to the core. If software wants to issue the same request back-to-back, it must write a 0 to this field between the two requests. The result of the state change request is reflected in the USB/Link State in DSTS. These bits are self-cleared on the MAC Layer exiting suspended state. If software is updating other fields of the DCTL register and not intending to force any link state change, then it must write a 0 to this field. SS Compliance mode is normally entered and controlled by the remote link partner. Alternatively, the local link can be forced directly into Compliance mode by resetting the SS link with the RUN/STOP bit set to zero. If then '10' is written to the USB/Link State Change field and '1' to RUN/STOP, the Link will go to Compliance. Once in Compliance, 'zero' and '10' may alternately be written to this field to advance the compliance pattern. In SS mode: ValueRequested Link State Transition: 0:No Action 4:SS.Disabled 5:Rx.Detect 6:SS.Inactive 8:Recovery 10:Compliance Others:Reserved In HS/FS/LS mode: ValueRequested USB state transition 8:Remote wakeup request Others:Reserved The Remote wakeup request should be issued 2µs after the device goes into suspend state. Note: After coming out of hibernation, software should write 8 (Recovery) into this field to confirm exit from the suspended state
4:0	0h RO	Reserved.

19.2.3 Device Event Enable Register (DEVTEN)—Offset C708h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RW	**Vendor Device Test LMP Received Event (VENDEVTSTRCVDEN)**
11:10	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Erratic Error Event Enable (ERRTICERREVTEN)**
8:7	0h RO	Reserved.
6	0h RW	**U3/L2-L1 Suspend Event Enable (U3L2L1SuspEn)**
5	0h RO	Reserved.
4	0h RW	**Resume/Remote Wakeup Detected Event Enable (WKUPEVTEN)**
3	0h RW	**USB/Link State Change Event Enable (ULSTCNGEN)**
2	0h RW	**Connection Done Enable (CONNECTDONEEVTEN)**
1	0h RW	**USB Reset Enable (USBRSTEVTEN)**
0	0h RW	**Disconnect Detected Event Enable (DISSCONNEVTEN)**

19.2.4 Device Status Register (DSTS)—Offset C70Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 520004h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RO	**Device Controller Not Ready (DCNRD):** The bit indicates that the core is in the process of completing the state transitions after exiting from hibernation. To complete the state transitions, it takes 256 bus clock cycles from the time DCTL[31].Run/Stop is set. During hibernation, if the UTMI/ULPI PHY is in suspended state, then the 256-bus clock cycle delay starts after the PHY exited suspended state. Software must set DCTL[31].Run/Stop to '1' and wait for this bit to be de-asserted to zero before processing DSTS.USBLnkSt. This bit is valid only when DWC_USB3_EN_PWROPT is set to two and GCTL[1].GblHibernationEn =1.
28:26	0h RO	Reserved.
25	0h RO	**Restore State Status (RSS):** When the controller has finished the restore process, it will complete the command by setting DSTS.RSS to '0'.
24	0h RO	**Save State Status (SSS):** When the controller has finished the save process, it will complete the command by setting DSTS.SSS to '0'.
23	0h RO	**Core Idle (COREIDLE):** The bit indicates that the core finished transferring all RxFIFO data to system memory, writing out all completed descriptors, and all Event Counts are zero.

Bit Range	Default & Access	Field Name (ID): Description
22	1h RO	**Device Controller Halted (DEVCTRLHLT):** This bit is set to 0 when the Run/Stop bit in the DCTL register is set to 1. The core sets this bit to 1 when, after SW sets Run/Stop to '0', the core is idle and the lower layer finishes the disconnect process. When Halted =1, the core does not generate Device events.
21:18	4h RO	**USB/Link State (USBLNKST):** In SS mode: 4'h0: U0 4'h1: U1 4'h2: U2 4'h3: U3 4'h4: SS_DIS 4'h5: RX_DET 4'h6: SS_INACT 4'h7: POLL 4'h8: RECOV 4'h9: HRESET 4'ha: CMPLY 4'hb: LPBK 4'hf: Resume/Reset In HS/FS/LS mode: 4'h0: On state 4'h2: Sleep (L1) state 4'h3: Suspend (L2) state 4'h4: Disconnected state 4'h5: Early Suspend state 4'he: Reset 4'hf: Resume
17	1h RO	**RxFIFO Empty (RXFIFOEMPTY)**
16:3	0h RO	**Frame/Microframe Number of the Received SOF (SOFFN):** When the core is operating at high-speed: [16:6] indicates the frame number [5:3] indicates the microframe number When the core is operating at full-speed: [16:14] is not used. Software can ignore these 3 bits [13:3] indicates the frame number
2:0	4h RO	**Connected Speed (CONNECTSPD):** Indicates the speed at which the core has come up after speed detection through a chirp sequence: 3'b100: SuperSpeed 3'b000: High-speed 3'b001: Full-speed 3'b010: Low-speed 3'b011: Full-speed

19.2.5 Device Generic Command Parameter (DGCMDPAR)—Offset C710h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Command Parameter (PARAMETER):** This register indicates the device command parameter. This must be programmed before or along with the device command (DGCMD).

19.2.6 Device Generic Command (DGCMD)—Offset C714h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:12	0h RO	**Command Status (CMDSTATUS):** 1: CmdErr – Indicates that the device controller encountered an error while processing the command. 0: Indicates command success
11	0h RO	Reserved.
10	0h NA	**Command Active (CMDACT):** The software sets this bit to 1 to enable the device controller to execute the generic command. The device controller sets this bit to 0 after executing the command.
9	0h RO	Reserved.
8	0h RW	**Command Interrupt on Complete (CMDIOC):** When this bit is set, the device controller issues a Generic Command Completion event after executing the command. Note that this interrupt is mapped to DCFG.IntrNum. Note: This field must not set to '1' if the DCTL.RunStop field is '0'.
7:0	0h RW	**Command Type (CMDTYP):** Specifies the type of command the software driver is requesting the core to perform: 02h: Set Periodic Parameters 04h: Set Scratchpad Buffer Array Address Lo 05h: Set Scratchpad Buffer Array Address Hi 07h:Transmit Device Notification 09h: Selected FIFO Flush 0Ah: All FIFO Flush 0Ch: Set Endpoint NRDY 10h: Run SoC Bus LoopBack Test

19.2.7 Device Active USB Endpoint Enable (DALEPENA)—Offset C720h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**USB Active Endpoints (USBACTEP):** This field indicates if a USB endpoint is active in the current configuration and interface. Bit[0]: USB EP0-OUT Bit[1]: USB EP0-IN Bit[2]: USB EP1-OUT Bit[3]: USB EP1-IN

19.2.8 Device Physical Endpoint-n Command Parameter 2 (DEPCMDPAR2)—Offset C800h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER):** This register indicates the physical endpoint command Parameter 2. It must be programmed before issuing the command.

19.2.9 Device Physical Endpoint-n Command Parameter 1 (DEPCMDPAR1)—Offset C804h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER):** This register indicates the physical endpoint command Parameter 1. It must be programmed before issuing the command

19.2.10 Device Physical Endpoint-n Command Parameter 0 (DEPCMDPAR0)—Offset C808h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**PARAMETER (PARAMETER):** This register indicates the physical endpoint command parameter 0. This must be programmed before or along with the command. For commands needing only one 32-bit parameter, this register must be programmed with the command register.

19.2.11 Device Physical Endpoint-n Command (DEPCMD)—Offset C80Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Command Parameters (COMMANDPARAM):** When this register is written: For Start Transfer command: -[31:16]: StreamID. The USB StreamID assigned to this transfer For Start Transfer command applied to an isochronous endpoint: -[31:16]: StartMicroFramNum: Indicates the (micro)frame number to which the first TRB applies For Update Transfer, End Transfer, and Start New Configuration commands: -[22:16]: Transfer Resource Index (XferRscIdx). The hardware-assigned transfer resource index for the transfer, which was returned in response to the Start Transfer command. The application software-assigned transfer resource index for a Start New Configuration command
15:12	0h RW	**Command Completion Status (CMDSTATUS):** Additional information about the completion of this command is available in this field.
11	0h RW	**HighPriority/ForceRM (HIPRI_FORCERM):** HighPriority: Only valid for Start Transfer command ForceRM: Only valid for End Transfer command ClearPendIN: Only valid for Clear Stall command – Software sets this bit to clear any pending IN transaction (on that endpoint) stuck at the lower layers when a Clear Stall command is issued.
10	0h RW	**Command Active (CMDACT):** Software sets this bit to 1 to enable the device endpoint controller to execute the generic command.The device controller sets this bit to 0 when the CmdStatus field is valid and the endpoint is ready to accept another command. This does not imply that all the effects of the previously-issued command have taken place.
9	0h RO	Reserved.
8	0h RW	**Command Interrupt on Complete (CMDIOC):** When this bit is set, the device controller issues a generic Endpoint Command Complete event after executing the command. Note that this interrupt is mapped to DEPCFG.IntrNum. When the DEPCFG command is executed, the command interrupt on completion goes to the interrupt pointed by the DEPCFG.IntrNum in the current command. Note: This field must not set to '1' if the DCTL.RunStop field is '0'.
7:4	0h RO	Reserved.
3:0	0h RW	**Command Type (CMDTYP):** Specifies the type of command the software driver is requesting the core to perform. 00h: Reserved 01h: Set Endpoint Configuration-64 or 96-bit Parameter 02h: Set Endpoint Transfer Resource Configuration-32-bit Parameter 03h: Get Endpoint State-No Parameter Needed 04h: Set Stall-No Parameter Needed 05h: Clear Stall (see Set Stall)-No Parameter Needed 06h: Start Transfer-64-bit Parameter 07h: Update Transfer-No Parameter Needed 08h: End Transfer-No Parameter Needed 09h: Start New Configuration-No Parameter Needed

19.3 xDCI MMIO Global Registers Summary

Table 19-3. Summary of xDCI MMIO Global Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C100h	C103h	Global SoC Bus Configuration 0 (GSBUSCFG0)—Offset C100h	6h
C104h	C107h	Global SoC Bus Configuration 1 (GSBUSCFG1)—Offset C104h	F00h
C108h	C10Bh	Global Tx Threshold Control (GTXTHRCFG)—Offset C108h	0h
C10Ch	C10Fh	Global Rx Threshold Control (GRXTHRCFG)—Offset C10Ch	24400000h
C110h	C113h	Global Core Control (GCTL)—Offset C110h	2000h
C114h	C117h	GPMSTS (GPMSTS)—Offset C114h	0h
C118h	C11Bh	Global Status (GSTS)—Offset C118h	0h
C130h	C133h	Bus Address Low (GBUSERRADDRLO)—Offset C130h	0h
C134h	C137h	Bus Address High (GBUSERRADDRHI)—Offset C134h	0h
C140h	C143h	GHWPARAMS0 (GHWPARAMS0)—Offset C140h	40204008h
C144h	C147h	GHWPARAMS1 (GHWPARAMS1)—Offset C144h	260C93Bh

Table 19-3. Summary of xDCI MMIO Global Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C148h	C14Bh	GHWPARAMS2 (GHWPARAMS2)—Offset C148h	8086A0h
C14Ch	C14Fh	GHWPARAMS3 (GHWPARAMS3)—Offset C14Ch	10420085h
C150h	C153h	GHWPARAMS4 (GHWPARAMS4)—Offset C150h	222004h
C154h	C157h	GHWPARAMS5 (GHWPARAMS5)—Offset C154h	4202088h
C158h	C15Bh	GHWPARAMS6 (GHWPARAMS6)—Offset C158h	2F60020h
C15Ch	C15Fh	GHWPARAMS7 (GHWPARAMS7)—Offset C15Ch	38507E6h
C160h	C163h	GDBGFIFOSPACE (GDBGFIFOSPACE)—Offset C160h	420000h
C164h	C167h	GDBGLTSSM (GDBGLTSSM)—Offset C164h	41010440h
C168h	C16Bh	GDBGLNMCC (GDBGLNMCC)—Offset C168h	0h
C16Ch	C16Fh	GDBGBMU (GDBGBMU)—Offset C16Ch	0h
C174h	C177h	GDBGLSP (GDBGLSP)—Offset C174h	0h
C178h	C17Bh	GDBGEPINFO0 (GDBGEPINFO0)—Offset C178h	0h
C17Ch	C17Fh	GDBGEPINFO1 (GDBGEPINFO1)—Offset C17Ch	800000h
C300h	C303h	Global Transmit FIFO Size Register N (GTXFIFOSIZ0_0)—Offset C300h	42h
C380h	C383h	GRXFIFOSIZ0_0 (GRXFIFOSIZ0_0)—Offset C380h	385h
C400h	C403h	GEVNTADRLO_0 (GEVNTADRLO_0)—Offset C400h	0h
C404h	C407h	GEVNTADRHI_0 (GEVNTADRHI_0)—Offset C404h	0h
C40Ch	C40Fh	GEVNTCOUNT_0 (GEVNTCOUNT_0)—Offset C40Ch	0h
C610h	C613h	GTXFIFOPRIDEV (GTXFIFOPRIDEV)—Offset C610h	0h

19.3.1 Global SoC Bus Configuration 0 (GSBUSCFG0)—Offset C100h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 6h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW	**Data Access is Big-Endian (DATBIGEND):** This bit controls the endian modefor data accesses. 0: Little-endian (default) 1: Big-endian In big-endian mode, DMAaccess (both read and write) for packet data will utilize a Byte Invariant Big-Endianmode. Note: Since AXI requires byteinvariant endianness, settingDescBigend and DatBigEnd to one causes an address invariant transform to be applied,which is not appropriate. Henceforth an AXI master (DWC_USB3_MBUS_TYPE=1), this bit must be set to zero.
10:8	0h RO	Reserved.
7	0h RW	**INCR256 Burst Type Enable (INCR256BRSTENA):** If software set this bit to "1", the master uses INCR to do the 256-beat burst.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**INCR128 Burst Type Enable (INCR128BRSTENA):** If software set this bit to “1”, the master uses INCR to do the 128-beat burst.
5	0h RW	**INCR64 Burst Type Enable (INCR64BRSTENA):** If software set this bit to “1”, the master uses INCR to do the 64-beat burst.
4	0h RW	**INCR32 Burst Type Enable (INCR32BRSTENA):** If software set this bit to “1”, the master uses INCR to do the 32-beat burst.
3	0h RW	**INCR16 Burst Type Enable (INCR16BRSTENA):** If software set this bit to "1", the master uses INCR to do the 16-beat burst.
2	1h RW	**INCR8 Burst Type Enable (INCR8BRSTENA):** if software set this bit to "1", the master uses INCR to do the 8-beat burst
1	1h RW	**INCR4 Burst Type Enable (INCR4BRSTENA):** When this bit is enabled the controller is allowed to do bursts of beat length 1, 2, 3, and 4
0	0h RW	**Undefined Length INCR Burst Type Enable (INCRBrstEna) Input to BUS-GM (INCRBRSTENA):** When enabled, this has higher priority than other burst types. For the AHBconfiguration. if this bit is set to 1, AHB master tries to do only one INCR burst for eachtransfer unless it has to break it at a 1Kbyte boundary. If this bit is set to 0, the AHBmaster may still use INCR burst type at the beginning and end bursts of transfers toalign the address. The middle bursts are INCR4/8/16, depending when the type isenabled.

19.3.2 Global SoC Bus Configuration 1 (GSBUSCFG1)—Offset C104h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: F00h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RW	**1k Page Boundary Enable (EN1KPAGE):** By default (this bit is disabled) the AXI breakstransfers at the 4k page boundary. When this bit is enabled, the AXI master (DMA data)breaks transfers at the 1k page boundary.
11:8	Fh RW	**AXI Pipelined Transfers Burst Request Limit (PipeTransLimit):** The fieldcontrols the number of outstanding pipelined transfers requests the AXI master willpush to the AXI slave. Once the AXI master reaches this limit, it will not make morerequests on the AXI ARADDR and AWADDR buses until the associated data phasescomplete. This field is encoded as follows: h0: 1 request h1: 2 requests h2: 3 requests h3: 4 requests ... hF: 16 requests
7:0	0h RO	Reserved.

19.3.3 Global Tx Threshold Control (GTXTHRCFG)—Offset C108h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RO	**USB Transmit Packet Count Enable (USBTxPktCntSel):** This fieldenables/ disables the USB transmission multi-packet thresholding: 0: USB transmissionmulti-packet thresholding is disabled, the core can only start transmission on the USBafter the entire packet has been fetched into the corresponding TXFIFO. 1: USBtransmission multi-packet thresholding is enabled. The core can only start transmissionon the USB after USB Transmit Packet Count amount of packets for the USB transaction(burst) are already in the corresponding TXFIFO This mode is only valid in the hostmode. It is only used for SuperSpeed.
28	0h RO	Reserved.
27:24	0h RO	**USB Transmit Packet Count (USBTxPktCnt):** This field specifies thenumber of packets that must be in the TXFIFO before the core can start transmission forthe corresponding USB transaction (burst). This field is only valid when the USBTransmit Packet Count Enable field is set to one. Valid values are from 1 to 15.
23:16	0h RW	**USB Maximum TX Burst Size (USBMaxTxBurstSize):** When USBTxPktCntSel is one,this field specifies the Maximum Bulk OUT burst the core should do. When the systembus is slower than the USB, TX FIFO can underrun during a long burst. User canprogram a smaller value to this field to limit the TX burst size that the core can do. Itonly applies to SS Bulk, Isochronous, and Interrupt OUT endpoints in the host mode.Valid values are from 1 to 16
15:0	0h RO	Reserved.

19.3.4 Global Rx Threshold Control (GRXTHRCFG)—Offset C10Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 24400000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	1h RW	**USB ReceivePacket Count Enable (USBRxPktCntSel):** This field enables/disables theUSB reception multi-packet thresholding: n 0: The core can only start reception on theUSB when the RX FIFO has space for at least one packet. n 1: The core can only startreception on the USB when the RX FIFO has space for at least USBRxPktCnt amount ofpackets. This mode is only valid in the host mode. It is only used for SuperSpeed.
28	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
27:24	4h RW	**USB Receive Packet Count (USBRxPktCnt):** This field specifies space (in number ofpackets) that must be available in the RX FIFO before the core can start thecorresponding USB RX transaction (burst). This field is only valid when the USB ReceivePacket Count Enable field is set to one. The valid values are from 1 to 15.
23:19	8h RW	**USB Maximum Rx Burst Size (USBMaxRxBurstSize):** This field is only validwhen USBRxPktCntSel is one. This field specifies the Maximum Bulk IN burst the coreshould do. When the system bus is slower than the USB, RX FIFO can overrun during along burst. User can program a smaller value to this field to limit the RX burst size thatthe core can do. It only applies to SS Bulk, Isochronous, and Interrupt IN endpoints inthe host mode. Valid values are from 1 to 16.
18:0	0h RO	Reserved.

19.3.5 Global Core Control (GCTL)—Offset C110h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:19	0h RO	Reserved.
18	0h RW	**Master Filter Bypass (MASTERFILTBYPASS):** When this bit is set to 1'b1, irrespective ofthe parameter DWC_USB3_EN_BUS_FILTERS chosen, all the filters in theDWC_usb3_filter module will be bypassed. The double synchronizers to mac_clkpreceding the filters will also be bypassed. For enabling the filters, this bit should be1'b0.
17	0h RO	Reserved.
16	0h RW	**U2RSTECN (U2RSTECN):** The super speed connection fails during POLL or LMP exchange, thedevice connects at non-SS mode. If this bit is set, then device attempts three moretimes to connect at SS, even if it previously failed to operate in SS mode.
15:14	0h RW	**FRMSCLDWN (FRMSCLDWN):** This field scales down device view of a SOF/USOF/ ITP duration. For SS/HS mode: 2'h3 implements interval to be 15. 625 us 2'h2 implementsinterval to be 31.25 us 2'h1 implements interval to be 62.5 us 2'h0implements interval to be125us For FS mode, the scale-down value is multiplied by 8.
13:12	2h RW	**Port Capability Direction (PRTCAPDIR):** 2’b01: Reserved 2’b10: for Device configurations 2’b11: Reserved
11	0h RW	**Core Soft Reset (CORESOFTRESET):** 1b0 - No soft reset 1b1 - Soft reset
10:4	0h RO	Reserved.
3	0h RW	**Disable Scrambling (DISSCRAMBLE):** Transmit request to Link Partner on next transition to Recovery or Polling.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	Reserved.
1	0h RW	**Global Hibernation Enable (GblHibernationEn):** This bit enables hibernation at the global level. If hibernation is not enabled via this bit, the PMU immediately accepts the D0->D3 and D3->D0 power state change requests, but does not save or restore any core state. In addition, the PMUs will never drive the PHY interfaces and let the core continue to drive the PHY interfaces.
0	0h RW	**Disable Clock Gating (DSBLCLKGTNG):** When this bit is set to 1 and the core is in Low Power mode, internal clock gating is disabled.You can set this bit to 1'b1 after Power On Reset.

19.3.6 GPMSTS (GPMSTS)—Offset C114h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h WO	**PortSel (PortSel)**
27:17	0h RO	Reserved.
16:12	0h RO	**U3Wakeup (U3Wakeup)**
11:10	0h RO	Reserved.
9:0	0h RO	**U2Wakeup (U2Wakeup)**

19.3.7 Global Status (GSTS)—Offset C118h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	Reserved.
6	0h RO	**Device Interrupt Pending (Device_IP):** This field indicates that there is a pendinginterrupt pertaining to peripheral (device) operation in the Device event queue
5	0h RO	**CSR Timeout (CSRTimeout):** When this bit is 1'b1, it indicates that software performeda write or read to a core register that could not be completed withinbus clock cycles (default: 65535).
4	0h RO	**Bus Error Address Valid (BUSERRADDRVLD):** Indicates that the GBUSERRADDR register is valid and reports the first bus address that encounters a bus error.
3:2	0h RO	Reserved.
1:0	0h RO	**Current Mode of Operation (CURMOD):** Indicates the current mode of operation. 2'b00: Device mode 2'b01: Reserved

19.3.8 Bus Address Low (GBUSERRADDRLO)—Offset C130h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Bus Address Low (BUSERRADDR):** This 64-bit register contains the lower 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1.It can only be cleared by resetting the core

19.3.9 Bus Address High (GBUSERRADDRHI)—Offset C134h

19.3.10 GHWPARAMS0 (GHWPARAMS0)—Offset C140h

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 40204008h

Bit Range	Default & Access	Field Name (ID): Description
31:24	40h RO	**DWC_USB3_ADWIDTH_31_24 (DWC_USB3_ADWIDTH_31_24)**
23:16	20h RO	**DWC_USB3_SDWIDTH_23_16 (DWC_USB3_SDWIDTH_23_16)**
15:8	40h RO	**DWC_USB3_MDWIDTH_15_8 (DWC_USB3_MDWIDTH_15_8)**
7:6	0h RO	**DWC_USB3_SBUS_TYPE_7_6 (DWC_USB3_SBUS_TYPE_7_6)**
5:3	1h RO	**DWC_USB3_MBUS_TYPE_5_3 (DWC_USB3_MBUS_TYPE_5_3)**
2:0	0h RO	**DWC_USB3_MODE_2_0 (DWC_USB3_MODE_2_0)**

19.3.11 GHWPARAMS1 (GHWPARAMS1)—Offset C144h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 260C93Bh

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	Reserved.
26	0h RO	**DWC_USB3_MAC_PHY_CLKS_SYNC_26 (DWC_USB3_MAC_PHY_CLKS_SYNC_26)**
25:24	2h RO	**DWC_USB3_EN_PWROPT_25_24 (DWC_USB3_EN_PWROPT_25_24)**
23	0h RO	**DWC_USB3_SPRAM_TYP_23 (DWC_USB3_SPRAM_TYP_23)**
22:21	3h RO	**DWC_USB3_NUM_RAMS_22_21 (DWC_USB3_NUM_RAMS_22_21)**
20:15	1h RO	**DWC_USB3_DEVICE_NUM_INT_20_15 (DWC_USB3_DEVICE_NUM_INT_20_15)**
14:12	4h RO	**DWC_USB3_ASPACEWIDTH_14_12 (DWC_USB3_ASPACEWIDTH_14_12)**
11:9	4h RO	**DWC_USB3_REQINFOWIDTH_11_9 (DWC_USB3_REQINFOWIDTH_11_9)**
8:6	4h RO	**DWC_USB3_DATAINFOWIDTH_8_6 (DWC_USB3_DATAINFOWIDTH_8_6)**
5:3	7h RO	**DWC_USB3_BURSTWIDTH_5_3 (DWC_USB3_BURSTWIDTH_5_3)**
2:0	3h RO	**DWC_USB3_IDWIDTH_2_0 (DWC_USB3_IDWIDTH_2_0)**

19.3.12 GHWPARAMS2 (GHWPARAMS2)—Offset C148h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8086A0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	8086A0h RO	**DWC_USB3_USERID_31_0 (DWC_USB3_USERID_31_0)**

19.3.13 GHWPARAMS3 (GHWPARAMS3)—Offset C14Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 10420085h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30:23	20h RO	**DWC_USB3_CACHE_TOTAL_XFER_RESOURCES_30_23 (DWC_USB3_CACHE_TOTAL_XFER_RESOURCES_30_23)**
22:18	10h RO	**DWC_USB3_NUM_IN_EPS_22_18 (DWC_USB3_NUM_IN_EPS_22_18)**
17:12	20h RO	**DWC_USB3_NUM_EPS_17_12 (DWC_USB3_NUM_EPS_17_12)**
11	0h RO	**DWC_USB3_ULPI_CARKIT_11 (DWC_USB3_ULPI_CARKIT_11)**
10	0h RO	**DWC_USB3_VENDOR_CTL_INTERFACE_10 (DWC_USB3_VENDOR_CTL_INTERFACE_10)**
9:8	0h RO	**ghwparams3_9_8 (ghwparams3_9_8)**
7:6	2h RO	**DWC_USB3_HSPHY_DWIDTH_7_6 (DWC_USB3_HSPHY_DWIDTH_7_6)**
5:4	0h RO	**DWC_USB3_FSPHY_INTERFACE_5_4 (DWC_USB3_FSPHY_INTERFACE_5_4)**
3:2	1h RO	**DWC_USB3_HSPHY_INTERFACE_3_2 (DWC_USB3_HSPHY_INTERFACE_3_2)**
1:0	1h RO	**DWC_USB3_SSPHY_INTERFACE_1_0 (DWC_USB3_SSPHY_INTERFACE_1_0)**

19.3.14 GHWPARAMS4 (GHWPARAMS4)—Offset C150h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 222004h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	1h RO	**DWC_USB3_EXT_BUFF_CONTROL_21 (DWC_USB3_EXT_BUFF_CONTROL_21)**
20:17	1h RO	**DWC_USB3_NUM_SS_USB_INSTANCES_20_17 (DWC_USB3_NUM_SS_USB_INSTANCES_20_17)**
16:13	1h RO	**DWC_USB3_HIBER_SCRATCHBUFS_16_13 (DWC_USB3_HIBER_SCRATCHBUFS_16_13):** Number of external scratchpad buffers the core requires to save its internal state in the device mode. Each buffer is assumed to be 4KB
12	0h RO	**ghwparams4_12 (ghwparams4_12)**
11	0h RO	**ghwparams4_11 (ghwparams4_11)**
10:9	0h RO	**ghwparams4_10_9 (ghwparams4_10_9)**
8:7	0h RO	**ghwparams4_8_7 (ghwparams4_8_7)**
6	0h RO	**ghwparams4_6 (ghwparams4_6)**
5:0	4h RO	**DWC_USB3_CACHE_TRBS_PER_TRANSFER_5_0 (DWC_USB3_CACHE_TRBS_PER_TRANSFER_5_0)**

19.3.15 GHWPARAMS5 (GHWPARAMS5)—Offset C154h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 4202088h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:22	10h RO	**DWC_USB3_DFQ_FIFO_DEPTH_27_22 (DWC_USB3_DFQ_FIFO_DEPTH_27_22)**
21:16	20h RO	**DWC_USB3_DWQ_FIFO_DEPTH_21_16 (DWC_USB3_DWQ_FIFO_DEPTH_21_16)**
15:10	8h RO	**DWC_USB3_TXQ_FIFO_DEPTH_15_10 (DWC_USB3_TXQ_FIFO_DEPTH_15_10)**
9:4	8h RO	**DWC_USB3_RXQ_FIFO_DEPTH_9_4 (DWC_USB3_RXQ_FIFO_DEPTH_9_4)**
3:0	8h RO	**DWC_USB3_BMU_BUSGM_DEPTH_3_0 (DWC_USB3_BMU_BUSGM_DEPTH_3_0)**

19.3.16 GHWPARAMS6 (GHWPARAMS6)—Offset C158h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 2F60020h

Bit Range	Default & Access	Field Name (ID): Description
31:16	2F6h RO	**DWC_USB3_RAM0_DEPTH_31_16 (DWC_USB3_RAM0_DEPTH_31_16)**
15	0h RO	**BusFltrsSupport (BusFltrsSupport)**
14	0h RO	**BCSupport (BCSupport)**
13	0h RO	**OTG_SS_Support (OTG_SS_Support):** 1'b0: No 3.0 support 1'b1: 3.0 support
12	0h RO	**ADPSupport (ADPSupport)**
11	0h RO	**HNPSupport (HNPSupport)**
10	0h RO	**SRPSupport (SRPSupport):** The application uses this bit to determine the DWC_usb3 core's SRP support. 1'b0: SRP support is not enabled 1'b1: SRP support is enabled
9:6	0h RO	Reserved.
5:0	20h RO	**DWC_USB3_PSQ_FIFO_DEPTH_5_0 (DWC_USB3_PSQ_FIFO_DEPTH_5_0)**

19.3.17 GHWPARAMS7 (GHWPARAMS7)—Offset C15Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 38507E6h

Bit Range	Default & Access	Field Name (ID): Description
31:16	385h RO	**DWC_USB3_RAM2_DEPTH_31_16 (DWC_USB3_RAM2_DEPTH_31_16)**
15:0	7E6h RO	**DWC_USB3_RAM1_DEPTH_15_0 (DWC_USB3_RAM1_DEPTH_15_0)**

19.3.18 GDBGFIFOSPACE (GDBGFIFOSPACE)—Offset C160h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 420000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	42h RO	**SPACE_AVAILABLE (SPACE_AVAILABLE)**
15:9	0h RO	Reserved.
8:0	0h RW	**FIFO_QUEUE_SELECT (FIFO_QUEUE_SELECT):** [8:5] indicates the FIFO/Queue Type [4:0] indicates the FIFO/Queue Number

19.3.19 GDBGLTSSM (GDBGLTSSM)—Offset C164h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 41010440h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	1h RO	**RxElecidle (RxElecidle)**
29	0h RO	**X3_XS_SWAPPING (X3_XS_SWAPPING)**

Bit Range	Default & Access	Field Name (ID): Description
28	0h RO	**X3_DS_HOST_SHUTDOWN (X3_DS_HOST_SHUTDOWN)**
27	0h RO	**PRTDIRECTION (PRTDIRECTION):** 1'b0: Upstream 1'b1: Downstream
26	0h RO	**LTDBTIMEOUT (LTDBTIMEOUT)**
25:22	4h RO	**LTDBLINKSTATE (LTDBLINKSTATE)**
21:18	0h RO	**LTDBSUBSTATE (LTDBSUBSTATE)**
17	0h RO	**ELASTICBUFFERMODE (ELASTICBUFFERMODE)**
16	1h RO	**TXELECLDLE (TXELECLDLE)**
15	0h RO	**RXPOLARITY (RXPOLARITY)**
14	0h RO	**TxDetRxLoopback (TxDetRxLoopback)**
13:11	0h RO	**LTDBPhyCmdState (LTDBPhyCmdState):** 000: PHY_IDLE 001: PHY_DET 010: PHY_DET_3 011: PHY_PWR_DLY 100: PHY_PWR_A 101: PHY_PWR_B
10:9	2h RO	**POWERDOWN (POWERDOWN)**
8	0h RO	**RXEQTRAIN (RXEQTRAIN)**
7:6	1h RO	**TXDEEMPHASIS (TXDEEMPHASIS)**
5:3	0h RO	**LTDBClkState (LTDBClkState):** 000: CLK_NORM 001: CLK_TO_P3 010: CLK_WAIT1 011: CLK_P3 100: CLK_TO_P0 101: CLK_WAIT2
2	0h RO	**TXSWING (TXSWING)**
1	0h RO	**RXTERMINATION (RXTERMINATION)**
0	0h RO	**TXONESZEROS (TXONESZEROS)**

19.3.20 GDBGLNMCC (GDBGLNMCC)—Offset C168h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8:0	0h RO	**LNMCC_BERC (LNMCC_BERC)**

19.3.21 GDBGBMU (GDBGBMU)—Offset C16Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**BMU_BCU (BMU_BCU)**
7:4	0h RO	**BMU_DCU (BMU_DCU)**
3:0	0h RO	**BMU_CCU (BMU_CCU)**

19.3.22 GDBGLSP (GDBGLSP)—Offset C174h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**LSPDEBUG (LSPDEBUG)**

19.3.23 GDBGEPINFO0 (GDBGEPINFO0)—Offset C178h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**EPDEBUG (EPDEBUG)**

19.3.24 GDBGEPINFO1 (GDBGEPINFO1)—Offset C17Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 800000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	800000h RO	**EPDEBUG (EPDEBUG)**

19.3.25 Global Transmit FIFO Size Register N (GTXFIFOSIZ0_0)—Offset C300h

FIFO_number: 0<= n <= 15 Offset: C300h + FIFO_number * 04h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 42h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**TXFSTADDR_N (TXFSTADDR_N)**
15:0	42h RW	**TXFDEP_N (TXFDEP_N)**

19.3.26 GRXFIFOSIZ0_0 (GRXFIFOSIZ0_0)—Offset C380h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 385h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**RXFSTADDR_N (RXFSTADDR_N)**
15:0	385h RW	**RXFDEP_N (RXFDEP_N)**

19.3.27 GEVNTADRLO_0 (GEVNTADRLO_0)—Offset C400h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**EVNTADRLO (EVNTADRLO)**

19.3.28 GEVNTADRHI_0 (GEVNTADRHI_0)—Offset C404h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**EVNTADRHI (EVNTADRHI)**

19.3.29 GEVNTCOUNT_0 (GEVNTCOUNT_0)—Offset C40Ch

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h NA	**EVNTCOUNT (EVNTCOUNT)**

19.3.30 GTXFIFOPRIDEV (GTXFIFOPRIDEV)—Offset C610h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**gtxfifopridev (gtxfifopridev)**

20 Shared SRAM (D20:F2)

20.1 PMC SSRAM PCI Configuration Space Registers Summary

Table 20-1. Summary of PMC SSRAM PCI Configuration Space Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device Vendor ID (DEVVENDID)—Offset 0h	8086h
4h	7h	STATUSCOMMAND Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	Revision ID and Class Code (REVCLASSCODE)—Offset 8h	0h
Ch	Fh	Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	0h
10h	13h	32-bit Base Address Register (BAR)—Offset 10h	4h
14h	17h	BAR HIGH (BAR_HIGH)—Offset 14h	0h
18h	1Bh	32-bit Base Address Register1 (BAR1)—Offset 18h	4h
1Ch	1Fh	BAR1 HIGH (BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	Subsystem Identifiers (SUBSYSTEMID)—Offset 2Ch	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	Interrupt Register (INTERRUPTREG)—Offset 3Ch	100h
80h	83h	POWER CAP ID PowerManagement Capability ID (POWERCAPID)—Offset 80h	48030001h
84h	87h	PME Control and Status (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI Device Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
98h	9Bh	D0I3 CONTROL SW LTR MMIO REG (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
9Ch	9Fh	Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch	0h
A0h	A3h	Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	800h
B0h	B3h	General Purpose Read Write Register1 (GEN_REGRW1)—Offset B0h	0h
B4h	B7h	General Purpose Read Write Register2 (GEN_REGRW2)—Offset B4h	0h
B8h	BBh	General Purpose Read Write Register3 (GEN_REGRW3)—Offset B8h	0h
BCh	BFh	General Purpose Read Write Register4 (GEN_REGRW4)—Offset BCh	0h
C0h	C3h	General Purpose Input Register (GEN_INPUT_REG)—Offset C0h	0h

20.1.1 Device Vendor ID (DEVVENDID)—Offset 0h

Device Vendor ID

Access Method

Type: CFG Register (Size: 32 bits)

Device: 20
Function: 2

Default: 8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	**Device Identification (DEVICEID):** Indicates the value assigned to the controller. Refer to Vol1 for default value.
15:0	8086h RO	**Vendor Identification (VENDORID):** Indicates Intel

20.1.2 STATUSCOMMAND Status and Command (STATUSCOMMAND)—Offset 4h

Status and Command

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 100000h

Bit Range	Default and Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**RMA (RMA):** Received Master Abort
28	0h RW/1C	**RTA (RTA):** Received Target Abort
27:21	0h RO	Reserved.
20	1h RO	**CAPLIST (CAPLIST):** Capabilities List
19	0h RO	**INTR_STATUS (INTR_STATUS):** Interrupt Status
18:11	0h RO	Reserved.
10	0h RW	**INTR_DISABLE (INTR_DISABLE):** Interrupt Disable
9	0h RO	Reserved.
8	0h RW/1C	**SERR_ENABLE (SERR_ENABLE):** System Error Enable
7:3	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
2	0h RW	**BME (BME):** Bus Master Enable
1	0h RW	**MSE (MSE):** Memory Space Enable
0	0h RO	Reserved.

20.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Revison Class Codes

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	**CLASS_CODES (CLASS_CODES):** The register is read-only and is used to identify the generic function of the device.
7:0	0h RO	**RID (RID):** Indicates stepping of the controller. Refer to Vol1 or specific value.

20.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Cache Line Latency Header And BIST

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RO	**MULFNDEV (MULFNDEV):** 0 = Single Function Device 1 = Multi Function device

Bit Range	Default and Access	Field Name (ID): Description
22:16	0h RO	**HEADERTYPE (HEADERTYPE):** Header Type
15:8	0h RO	**LATTIMER (LATTIMER):** Hard wired to 00h.
7:0	0h RW	**CACHELINE_SIZE (CACHELINE_SIZE):** Cacheline Size

20.1.5 32-bit Base Address Register (BAR)—Offset 10h

Base Address Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:13	0h RW	**BAR (BASEADDR):** Software programs this register with the base address of the device's memory region
12:4	0h RO	**Size Indicator (SIZEINDICATOR):** Hardwired to 0 to indicate 8KB of memory space
3	0h RO	**Prefetchable (PREFETCHABLE):** Hardwired to 0 to indicate the device's memory space as notprefetchable.
2:1	2h RO	**Type (TYPE):** Hardwired to 10 to indicate that Base register is 64 bits wide and mapping can be done anywhere in the 64-bit Memory Space.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** Hardwired to 0 to identify a Memory BAR.

20.1.6 BAR HIGH (BAR_HIGH)—Offset 14h

BAR -Base Address Register High

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address HIGH (BASEADDR_HIGH):** Base Address

20.1.7 32-bit Base Address Register1 (BAR1)—Offset 18h

Base Address Register1

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:12	0h RW	**BAR1 (BASEADDR1):** Software programs this register with the base address of the device's memory region
11:4	0h RO	**Size Indicator (SIZEINDICATOR1):** Hardwired to 0 to indicate 4KB of memory space
3	0h RO	**Prefetchable (PREFETCHABLE1):** Hardwired to 0 to indicate the device's memory space as notprefetchable.
2:1	2h RO	**Type (TYPE1):** Hardwired to 10 to indicate that Base register is 64 bits wide and mapping can be done anywhere in the 64-bit Memory Space.
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** Hardwired to 0 to identify a Memory BAR.

20.1.8 BAR1 HIGH (BAR1_HIGH)—Offset 1Ch

BAR1 -Base Address Register High

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Base Address HIGH (BASEADDR1_HIGH):** Base Address

20.1.9 Subsystem Identifiers (SUBSYSTEMID)—Offset 2Ch

Subsystem Identifiers

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SUBSYSTEMID):** Written by BIOS. Not used by hardware.
15:0	0h RW/O	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** Written by BIOS.Not used by hardware.

20.1.10 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**CAPPTR_POWER (CAPPTR_POWER):** Indicates what the next capability is. This capability points to the PM Capability (0x80) structure.

20.1.11 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Interrupt Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 100h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	**MAX_LAT (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**MIN_GNT (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers
15:12	0h RO	Reserved.
11:8	1h RO	**INTPIN (INTPIN):** Interrupt Pin
7:0	0h RW	**INTLINE (INTLINE):** Used to communicate to software the interrupt line that the interrupt pin is connected to.

20.1.12 POWER CAP ID PowerManagement Capability ID (POWERCAPID)—Offset 80h

PowerManagement Capability

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 48030001h

Bit Range	Default and Access	Field Name (ID): Description
31:27	9h RO	**PMESUPPORT (PMESUPPORT):** PME Support
26:19	0h RO	Reserved.
18:16	3h RW/1C	**VERSION (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	0h RO	**NXTCAP (NXTCAP):** Points to the next capability structure. This points to NULL.
7:0	1h RO	**POWER_CAP (POWER_CAP):** Indicates power management capability.

20.1.13 PME Control and Status (PMECTRLSTATUS)—Offset 84h

Power Management Control and Status Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C	**PMESTATUS (PMESTATUS):** PME Status
14:9	0h RO	Reserved.
8	0h RW	**PMEENABLE (PMEENABLE):** PME Enable
7:4	0h RO	Reserved.
3	1h RO	**NO_SOFT_RESET (NO_SOFT_RESET):** When set, this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved.
2	0h RO	Reserved.
1:0	0h RW	**POWERSTATE (POWERSTATE):** This field is used both to determine the current power state and to set a new power state.

20.1.14 PCI Device Capability Record (PCIDEVIDLE_CAP_RECORD)—Offset 90h

PCI DEVICE IDLE CAPABILITY RECORD

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: F0140009h

Bit Range	Default and Access	Field Name (ID): Description
31:28	Fh RO	**VEND_CAP (VEND_CAP):** Indicates this is Vendor Specific capability.
27:24	0h RO	**REVID (REVID):** Revision ID of capability structure
23:16	14h RO	**CAP_LENGTH (CAP_LENGTH):** Indicates the number of bytes in the capability structure.
15:8	0h RO	**NEXT_CAP (NEXT_CAP):** Points to the next capability structure. This points to NULL.
7:0	9h RO	**CAPID (CAPID):** Capability ID

20.1.15 D0I3 CONTROL SW LTR MMIO REG (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

SW LTR Update MMIO Location Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	**SW_LAT_DWORD_OFFSET (SW_LAT_DWORD_OFFSET):** This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR. The value of this register is a do not care, if the Valid bit is not set.
3:1	0h RO	**SW_LAT_BAR_NUM (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0.
0	0h RO	**SW_LAT_VALID (SW_LAT_VALID):** 0= not valid 1= valid

20.1.16 Device IDLE pointer register (DEVICE_IDLE_POINTER_REG)—Offset 9Ch

Device IDLE pointer register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	**DWORD_OFFSET (DWORD_OFFSET):** This register contains the location pointer to the DevIdle register in MMIO space, as an offset from the specified BAR. The value of this register is a do not care, if the Valid bit is not set.
3:1	0h RO	**BAR_NUM (BAR_NUM):** Indicates that the DevIdle update MMIO location is always at BAR0
0	0h RO	**VALID (VALID):** 0= not valid 1= valid

20.1.17 Device PG Config (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

DEVICE PG CONFIG

Access Method

Type: CFG Register (Size: 32 bits)

Device: 20
Function: 2

Default: 800h

Bit Range	Default and Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW	**HAE (HAE):** Hardware Autonomous Enable
20	0h RO	Reserved.
19	0h RW	**SLEEP_EN (SLEEP_EN):** Sleep Enable
18	0h RW	**PGE (PGE):** If clear, then the controller will never request a PG. If set, then the controller may request PG when proper conditions are met. Note: This Bit must be set by BIOs for PG to function
17	0h RW	**I3_ENABLE (I3_ENABLE):** If '1', then the function will power gate when idle and the DevIdle register (DevIdleC[2] = '1') is set.
16	0h RW	**PMCRE (PMCRE):** If this bit is set to '1', the function will power gate when idle.
15:13	0h RO	Reserved.
12:10	2h RW/O	**POW_LAT_SCALE (POW_LAT_SCALE):** Power On Latency Scale
9:0	0h RW/O	**POW_LAT_VALUE (POW_LAT_VALUE):** This value is written by BIOS to communicate to the Driver.

20.1.18 General Purpose Read Write Register1 (GEN_REGRW1)—Offset B0h

General Purpose Read Write Register1

Access Method

Type: CFG Register (Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW1 (GEN_REG_RW1):** General Purpose PCI Register

20.1.19 General Purpose Read Write Register2 (GEN_REGRW2)—Offset B4h

General Purpose Read Write Register2

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW2 (GEN_REG_RW2):** General Purpose PCI Register

20.1.20 General Purpose Read Write Register3 (GEN_REGRW3)—Offset B8h

General Purpose Read Write Register3

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW3 (GEN_REG_RW3):** General Purpose PCI Register

20.1.21 General Purpose Read Write Register4 (GEN_REGRW4)—Offset BCh

General Purpose Read Write Register4

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_RW4 (GEN_REG_RW4):** General Purpose PCI Register

20.1.22 General Purpose Input Register (GEN_INPUT_REG)—Offset C0h

General Purpose Input Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 20
Function: 2

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**GEN_REG_INPUT_RW (GEN_REG_INPUT_RW):** General Purpose Input Register

21 CNVi

21.1 CNVi PCI Configuration Registers Summary

Table 21-1. Summary of CNVi PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Vendor and Device ID (CNVI_WIFI_VEN_DEV_ID)—Offset 0h	XXXX8086h
4h	7h	Device Command and Status (CNVI_WIFI_PCI_COM_STAT)—Offset 4h	100000h
8h	Bh	Class Code and Revision ID (CNVI_WIFI_PCI_CLASS_CODE)—Offset 8h	28000XXh
10h	13h	Base Address Register BAR0 Low (CNVI_WIFI_BAR0)—Offset 10h	4h
14h	17h	Base Address Register BAR0 High (CNVI_WIFI_BAR1)—Offset 14h	0h
2Ch	2Fh	Subsystem ID (CNVI_WIFI_SUBSYS_ID)—Offset 2Ch	8086h
34h	37h	Capabilities Pointer (CNVI_WIFI_CAP_PTR)—Offset 34h	C8h
3Ch	3Fh	Interrupt (CNVI_WIFI_INTERRUPT)—Offset 3Ch	100h
40h	43h	PCI Express Capabilities (CNVI_WIFI_GIO_CAP)—Offset 40h	928010h
44h	47h	Device Capabilities (CNVI_WIFI_GIO_DEV_CAP)—Offset 44h	10000EC0h
48h	4Bh	Device Control Register (CNVI_WIFI_GIO_DEV)—Offset 48h	100C10h
64h	67h	Device Control 2 (CNVI_WIFI_GIO_DEV_CAP_2)—Offset 64h	80812h
68h	6Bh	Device Control (CNVI_WIFI_GIO_DEV_2)—Offset 68h	5h
80h	83h	MSIX Capability (CNVI_WIFI_MSIX_CAP_HEAD)—Offset 80h	F0011h
84h	87h	MSIX Capability Structure (CNVI_WIFI_MSIX_TABLE_OFFSET)—Offset 84h	2000h
88h	8Bh	MSIX Capability Structure (CNVI_WIFI_MSIX_PBA_OFFSET)—Offset 88h	3000h
C8h	CBh	Power Management Capabilities (CNVI_WIFI_PMC)—Offset C8h	C823D001h
CCh	CFh	Power Management Status and Control (CNVI_WIFI_PMCSR)—Offset CCh	D000008h
D0h	D3h	Capability ID and Message Control (CNVI_WIFI_MSI_MSG_CTRL)—Offset D0h	804005h
D4h	D7h	MSI Low Address (CNVI_WIFI_MSI_LOW_ADD)—Offset D4h	0h
D8h	DBh	MSI High Address (CNVI_WIFI_MSI_HIGH_ADD)—Offset D8h	0h
DCh	DFh	MSI Data (CNVI_WIFI_MSI_DATA)—Offset DCh	0h
104h	107h	Uncorrectable Error Status Register (CNVI_WIFI_UNCORRECT_ERR_STAT)—Offset 104h	0h
108h	10Bh	Uncorrectable Error mask Register (CNVI_WIFI_UNCORRECT_ERR_MASK)—Offset 108h	0h
10Ch	10Fh	Uncorrectable Error Severity (CNVI_WIFI_UNCORRECT_ERR_SEV)—Offset 10Ch	62031h
110h	113h	Error Status (CNVI_WIFI_CORRECT_ERR_STAT)—Offset 110h	0h
114h	117h	Error Mask (CNVI_WIFI_CORRECT_ERR_MASK)—Offset 114h	0h
118h	11Bh	Advanced Error Capabilities and Control (CNVI_WIFI_ADVANCED_ERR_CAP)—Offset 118h	0h
11Ch	11Fh	Header Log 1 (CNVI_WIFI_HEADER_LOG1)—Offset 11Ch	0h
120h	123h	Header Log 2 (CNVI_WIFI_HEADER_LOG2)—Offset 120h	0h

Table 21-1. Summary of CNVi PCI Configuration Registers (Continued)

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
124h	127h	Header Log 3 (CNVI_WIFI_HEADER_LOG3)—Offset 124h	0h
128h	12Bh	Header Log 4 (CNVI_WIFI_HEADER_LOG4)—Offset 128h	0h
140h	143h	Device Serial Number Capability (CNVI_WIFI_GIO_SERIAL_CAP)—Offset 140h	14C00000h
144h	147h	Serial Number Low (CNVI_WIFI_GIO_SERIAL_LOW)—Offset 144h	FF000000h
148h	14Bh	Serial Number Upper (CNVI_WIFI_GIO_SERIAL_UP)—Offset 148h	FFh
14Ch	14Fh	Header of LTR Extended Capability (CNVI_WIFI_LTR_EXTND_CAP_HEAD)—Offset 14Ch	16410018h
150h	153h	No Snoop Request (CNVI_WIFI_LTR_MAX_SNOOP_NOSNOOP_LAT)—Offset 150h	0h
154h	157h	L1 substates Extended Capability Header (CNVI_WIFI_L1PM_SUB_EXTND_CAP_HEAD)—Offset 154h	1001Eh
158h	15Bh	L1 Substates Capability (CNVI_WIFI_L1PM_SUB_CAP)—Offset 158h	481E1Fh
15Ch	15Fh	L1 Substates Control (CNVI_WIFI_L1PM_SUB_CNTRL)—Offset 15Ch	0h
160h	163h	L1 Substates Control 2 (CNVI_WIFI_L1PM_SUB_CNTRL2)—Offset 160h	28h
164h	167h	Vendor Specific Capability Header (CNVI_WIFI_VEN_SPEC_CAP)—Offset 164h	1000Bh
168h	16Bh	Vendor Specific Extended Capability (CNVI_WIFI_VEN_SPEC_EXTND_CAP)—Offset 168h	1400010h
16Ch	16Fh	SW LTR Pointer (CNVI_WIFI_LTP_PTR)—Offset 16Ch	0h
170h	173h	DevIdle Pointer (CNVI_WIFI_DEV_IDLE_PTR)—Offset 170h	31800001h
174h	177h	DevIdle Power on Latency (CNVI_WIFI_DEV_IDLE_PWR)—Offset 174h	800h

21.1.1 Vendor and Device ID (CNVI_WIFI_VEN_DEV_ID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 25
Function: 0

Default: XXXX8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	-- RO	**Device ID (DEV_ID):** Indicates the Device ID of the controller. Refer to the Device and Revision ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor ID (VEN_ID):** Indicates Intel.

21.1.2 Device Command and Status (CNVI_WIFI_PCI_COM_STAT)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 25
Function: 0

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1C	**Detected Parity Error (DET_PAR_ERR)**
30	0h RW/1C	**Signaled System Error (SIG_SYS_ERR)**
29	0h RW/1C	**Received Master Abort (REC_MAS_ABRT)**
28	0h RW/1C	**Received Target Abort (REC_TAR_ABRT)**
27	0h RW/1C	**Signaled Target Abort (SIG_TAR_ABRT)**
26:25	0h RO	**DEVSEL Timing (DEVSEL_TIMING):** Does not apply. Hardwired to 0.
24	0h RW/1C	**Master Data Parity Error (MAS_DATA_PAR_ER):** Master Data Parity Error
23	0h RO	**Fast Back to Back Transaction Capable (FAST_BTB_TCAP):** Does not apply. Hardwired to 0.
22	0h RO	Reserved.
21	0h RO	**66 MHz Capable (OLF_FREQ_CAP):** Does not apply. Hardwired to 0.
20	1h RO	**Capability List (CAP_LST):** Hardwired to 1.
19	0h RO	**Interrupt Status (INTRPT_STS):** Reflects the state of the interrupt in the device.
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTRPT_DIS):** Controls the ability of the device to generate legacy interrupt messages. 0 = Enable. 1 = Disable.
9	0h RO	**Fast Back to Back Enable (FAST_BTB_TNSCEN):** Does not apply. Hardwired to 0.
8	0h RW	**SERR Enable (SERR_EN):** Enable SERR# to be generated if this bit is set.
7	0h RO	**Wait Cycle Control (IDSEL_STEP_W_CY):** Does not apply. Hardwired to 0.
6	0h RW	**Parity Error Enable (PAR_ERR):** This bit is set to 1 to enable response to parity errorswhen detected.
5	0h RO	**VGA Palette Snoop (VGA_PALT_SNOOP):** Does not apply. Hardwired to 0.
4	0h RO	**Memory Write and Invalidate (MEM_WR_INVALD):** Does not apply. Hardwired to 0.
3	0h RO	**Special Cycle Enable (SPEC_CYC_ENB):** Does not apply. Hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Bus Master Enable (BUS_MAS):** 0 = Bus master is disabled. 1 = Bus master is enabled.
1	0h RW	**Memory Space Access Enable (MEM_SP_ACC):** 0 = Memory space access is disabled. 1 = Memory space access is enabled.
0	0h RO	**IO Space Access Enable (IO_SPC_AC_EN_0):** 0 = IO space access is disabled. 1 = IO space access is enabled.

21.1.3 Class Code and Revision ID (CNVI_WIFI_PCI_CLASS_CODE)—Offset 8h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: 28000XXh

Bit Range	Default & Access	Field Name (ID): Description
31:24	2h RO	**Base Class Code (SE_CLASS):** Classifies the type of function the device perform.
23:16	80h RO	**Sub-Class Code (SUB_CLASS):** Identifies more specifically the function of the device.
15:8	0h RO	**Interface (INTERFACE):** Identifies a specific register-level programming interface. Does not apply. Hardwired to 0.
7:0	-- RO	**Revision ID (REV_ID):** Identifies the revision of the device. Refer to Device and Revision ID Table in Vol1 for specific value.

21.1.4 Base Address Register BAR0 Low (CNVI_WIFI_BAR0)—Offset 10h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RW	**Base Address Field (BS_ADD_FLD_RW):** Provides system memory base address for thecontroller.
13:4	0h RO	**Base Address Field (BS_ADD_FLD_RO):** Hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**Prefetchable (PREFETCHBL):** Defines the block of memory as Prefetchable or not. 0 indicates that this BAR is not prefetchable.
2:1	2h RO	**Decoder Width Field (DECOD_WDTH_FLD):** Decoder Width Field (10b-64bit reg).
0	0h RO	**Memory Space Indicator (MEM_SPAC_INDIC):** Hardwired to 0.Indicates this BAR is present in the memory space.

21.1.5 Base Address Register BAR0 High (CNVI_WIFI_BAR1)—Offset 14h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Address High (BS_ADD_FLD)**

21.1.6 Subsystem ID (CNVI_WIFI_SUBSYS_ID)—Offset 2Ch

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: 8086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Subsystem Device ID (SB_DEV_ID)**
15:0	8086h RO	**Subsystem Vendor ID (SB_VEN_ID):** Indicates Intel.

21.1.7 Capabilities Pointer (CNVI_WIFI_CAP_PTR)—Offset 34h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: C8h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	C8h RO	**Capabilities Pointer (CARDB_PTR):** Indicates what the next capability is.

21.1.8 Interrupt (CNVI_WIFI_INTERRUPT)—Offset 3Ch

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: 100h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Max Latency (MAX_LATNC):** Does not apply. Hardwired to 0.
23:16	0h RO	**Min Latency (MIN_GNT):** Does not apply. Hardwired to 0.
15:8	1h RO	**Interrupt Pin (INT_PIN):** Identifies which interrupt pin the device uses.
7:0	0h RW	**Interrupt Line (INT_LINE):** Identifies which input interrupt request pin is routed to.

21.1.9 PCI Express Capabilities (CNVI_WIFI_GIO_CAP)—Offset 40h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: 928010h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:25	0h RO	**Interrupt Message Number (INTRPT_MSG_NUM)**
24	0h RO	**Slot Implemented (SLT_IMPLNT)**
23:20	9h RO	**Device Port Type (DEV_POR_TYP)**

Bit Range	Default & Access	Field Name (ID): Description
19:16	2h RO	**Capability Version (CAP_VER):** 2h = Gen 2.0.
15:8	80h RO	**Next Capability Pointer (GIO_CAP_NXT_OFS):** The offset to the next PCI capability structure.
7:0	10h RO	**Capability Structure (INCD_PCIE_CST):** Indicates PCI Express Capability Structure.

21.1.10 Device Capabilities (CNVI_WIFI_GIO_DEV_CAP)—Offset 44h

The Device Capabilities register identifies PCI Express device specific capabilities.(Offset 044 h)

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: 10000EC0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28	1h RO	**Function Level Reset Capability (FUNC_LVL_RES)**
27:26	0h RO	**Slot Power Limit Scale (SLT_PW_LSCL):** Captured Slot Power Limit Scale
25:18	0h RO	**Slot Power Limit Value (SLT_PW_LVAL):** Captured Slot Power Limit Value
17:16	0h RO	Reserved.
15	0h RO	**Error Reporting Support (ROLE_BASED_ERR):** This field indicates that the device supports Error reporting.
14:12	0h RO	Reserved.
11:9	7h RO	**Endpoint L1 Acceptable Latency (L1_ACC_LAT)**
8:6	3h RO	**Endpoint L0s Acceptable Latency (L0S_ACC_LAT)**
5	0h RO	**Extended Tag Field Supported (EX_TAG_FIELD)**
4:3	0h RO	Reserved.
2:0	0h RO	**Max Payload Size Supported (MAX_PL_SIZE)**

21.1.11 Device Control Register (CNVI_WIFI_GIO_DEV)—Offset 48h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 25
Function: 0

Default: 100C10h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RO	**TRANS_PEND (TRANS_PEND):** indicates that a device has Non-Posted Requests which have not been completed
20	1h RO	**Aux Power (AUX_P_DET):** device that requires AUX power reports this bit (asynch signal)
19	0h RW/1C	**Unsupported Request Detected (UNSOP_REQ_DET):** indicates that the device received Unsupported Request
18	0h RW/1C	**Fatal Error Detected (FAT_ERR_DET):** indicates status of fatal errors detected
17	0h RW/1C	**Non-Fatal Error Detected (NFAT_ER_DET):** indicates status of non-fatal errors detected
16	0h RW/1C	**Correctable Errors Detected (COR_ERR_DET):** indicates status of correctable errors detected
15	0h RO	**Initiate Function Level Reset (INIT_FNC_LV_RS):** A write of 1b initiates Function (init FLR)
14:12	0h RW	**Max Read Request Size (MAX_RDRQ_SIZE):** sets the maximum Read Request size
11	1h RW	**Enable No Snoop (EN_NO_SNOOP):** if set device is permitted to set No Snoop bit.
10	1h RW	**Auxiliary Power PM Enable (AUX_PM_EN):** Sticky value.
9	0h RO	Reserved.
8	0h RO	**IO Space access Enable (IO_SPC_AC_EN_8)**
7:5	0h RW	**Max Payload Size (MAX_PAY_SIZE):** sets maximum TLP payload size for the device functions
4	1h RW	**Relax Order Enable (EN_REL_ORD):** when set device permitted to set the Relaxed Ordering bit
3	0h RW	**Unsupported Request Reporting (UNSOP_REQ_REP):** enables reporting of Unsupported Request when set

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Fatal Error Reporting (FAT_ERR_REP):** controls reporting of fatal errors
1	0h RW	**Non-Fatal Error Reporting (NFAT_ER_REP):** controls reporting of non-fatal errors
0	0h RW	**Correctable Error Reporting (COR_ERR_REP):** controls reporting of correctable errors

21.1.12 Device Control 2 (CNVI_WIFI_GIO_DEV_CAP_2)—Offset 64h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 25
Function: 0

Default: 80812h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	Reserved.
19:18	2h RO	**OBFF Support (OBFF_MEC_SUP):** 0x00 = unsupported 0x01 = supported using message signaling A 0x10 = suported using signaling B 0x11 = supported using WAKE signaling
17:12	0h RO	Reserved.
11	1h RO	**LTR Mechanism Support (LTR_MEC_SUP):** A value of 1b indicates support for LTR.
10:5	0h RO	Reserved.
4	1h RO	**Complete Timeout Disable (CMP_TO_DIS_SUP):** 1 = support for the Completion Timeout Disable, 0 = not supported. Hardwired to 0x1.
3:0	2h RO	**Completion Timeout Ranges Supported (CMP_TO_RNG_SUP):** Hardwired to 0x2.

21.1.13 Device Control (CNVI_WIFI_GIO_DEV_2)—Offset 68h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 25
Function: 0

Default: 5h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:13	0h RW	**OBFF enable (OBFF_MEC_ENA):** OBFF enable: 0x00 -disable , 0x01 - enabled using message signaling A, 0x10 - message signaling B ,0x11-enabled using WAKE signaling
12:11	0h RO	Reserved.
10	0h RW	**LTR Mechanism Enable (LTR_MEC_EN):** When Set enables the LTR.
9:5	0h RO	Reserved.
4	0h RW	**CMP_TO_DIS (CMP_TO_DIS):** When Set, this bit disables the Completion Timeout mechanism
3:0	5h RW	**CMP_TO_VAL (CMP_TO_VAL):** this field allows system SW to modify the Completion Timeout value

21.1.14 MSIX Capability (CNVI_WIFI_MSIX_CAP_HEAD)—Offset 80h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 25

Function: 0

Default: F0011h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**MSIX_ENABLE (MSIX_ENABLE):** If set to 1, the function is permitted to use MSI-X to request service. System configuration software sets this bit to enable MSI-X. A device driver is prohibited from writing this bit to mask a function's service request. If 0, the function is prohibited from using MSI-X to request service.
30	0h RW	**FUN_MASK (FUN_MASK):** If set to 1, all of the vectors associated with the function are masked, regardless of their per-vector Mask bit states. If 0, each vector's Mask bit determines whether the vector is masked or not. Setting or clearing the MSI-X Function Mask bit has no effect on the state of the per-vector Mask bits
29:27	0h RO	Reserved.
26:16	Fh RO	**TABLE_SIZE (TABLE_SIZE):** System software reads this field to determine the MSI-X Table Size N, which is encoded as (N-1). Wifi Host supports Table Size of 16 and encodes a number of 15.
15:8	0h RO	**NEXT_PTR (NEXT_PTR):** Pointer to the next item in the capabilities list. NULL if last
7:0	11h RO	**MSIX_CAP_ID (MSIX_CAP_ID):** The value of 11h in this field identifies the function as being MSI-X capable.

21.1.15 MSIX Capability Structure (CNVI_WIFI_MSIX_TABLE_OFFSET)—Offset 84h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 25
Function: 0

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	400h RO	**TABLE_OFFSET (TABLE_OFFSET):** Used as an offset from the address contained by the Base Address register to point to the base of the MSI-X Table. The lower 3 bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. In Wifi Host the table is at 0x2000, so the value of this field in 0x400.
2:0	0h RO	**TABLE_BIR (TABLE_BIR):** Indicates which one of a function's Base Address registers, located beginning at 10h in configuration Space, and is used to map the function's MSI-X Table into Memory Space. Wifi Host cluster uses a single BAR to point to the MSI-X structures.

21.1.16 MSIX Capability Structure (CNVI_WIFI_MSIX_PBA_OFFSET)—Offset 88h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 25
Function: 0

Default: 3000h

Bit Range	Default & Access	Field Name (ID): Description
31:3	600h RO	**TABLE_OFFSET (TABLE_OFFSET):** Used as an offset from the address contained by the Base Address register to point to the base of the MSI-X PBA Table. The lower 3 bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. In Wifi Host the table is at 0x3000, so the value of this field in 0x600.
2:0	0h RO	**TABLE_BIR (TABLE_BIR):** Indicates which one of a function's Base Address registers, located beginning at 10h in configuration Space, and is used to map the function's MSI-X Table into Memory Space. Wifi Host cluster uses a single BAR to point to the MSI-X structures.

21.1.17 Power Management Capabilities (CNVI_WIFI_PMC)—Offset C8h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 25
Function: 0

Default: C823D001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	19h RO	**PME_SUPRT (PME_SUPRT):** PME Support,indicates the power states in which the device may assert PME
26	0h RO	**D2_PWR_MANG (D2_PWR_MANG):** D2 Power Management State support
25	0h RO	**D1_PWR_MANG (D1_PWR_MANG):** D1 Power Management State support
24:22	0h RO	**AUX_CUR (AUX_CUR):** AUX Current (Used data register instead)
21	1h RO	**DEV_SPC_INT (DEV_SPC_INT):** Device Specific Initialization
20	0h RO	Reserved.
19	0h RO	**PME_CLK (PME_CLK):** Does not apply. Hardwired to 0.
18:16	3h RO	**VERSION (VERSION):** value indicates that this function complies with the Revision 1.2
15:8	D0h RO	**PMC_NXT_PTR (PMC_NXT_PTR):** Next PTR, pointing to the location of next item in the functions capability list HARDWIRED
7:0	1h RO	**PMC_CAP_ID (PMC_CAP_ID):** Capability ID, Indicates the linked list item is the PCI Power Management Registers HARDWIRED

21.1.18 Power Management Status and Control (CNVI_WIFI_PMCSR)—Offset CCh

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 25
Function: 0

Default: D000008h

Bit Range	Default & Access	Field Name (ID): Description
31:24	Dh RO	**PWR_DIS_CON (PWR_DIS_CON):** used to report power consumption and heat dissipation (default for D3-0x1)
23	0h RO	**BUS_PWR_CLK_CEN (BUS_PWR_CLK_CEN):** Bus Power/Clock Control Enable. Does not apply. Hardwired to 0.
22	0h RO	**B2_B3_SUPRT (B2_B3_SUPRT):** B2/B3 Support. Does not apply. Hardwired to 0.
21:16	0h RO	Reserved.
15	0h RW/1C	**PME_STAT (PME_STAT):** This bit reflects whether the function has experienced a PME. sticky value.
14:13	0h RO	**DAT_SCALE (DAT_SCALE):** Data Scale
12:9	0h RW	**DAT_SEL (DAT_SEL):** Data Select, selects the data value to be viewed through the Data register

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**PME_ENA (PME_ENA):** PME Enable. sticky value.
7:4	0h RO	Reserved.
3	1h RO	**NO_SOFT_RESET (NO_SOFT_RESET):** No_Soft_Reset
2	0h RO	Reserved.
1:0	0h RW	**PWR_STATE (PWR_STATE):** Power State

21.1.19 Capability ID and Message Control (CNVI_WIFI_MSI_MSG_CTRL)—Offset D0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 25
Function: 0

Default: 804005h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**64 Bit Address Capable (BITA_CAP_64):** Hardwired to 1.
22:20	0h RO	**Multiple Message Enable (MUL_MSG_ENB):** Hardwired to 0.
19:17	0h RO	**Multiple Message Capable (MUL_MSG_CAP):** Hardwired to 0.
16	0h RW	**MSI Enable (MSI_ENA):** function is enabled to use MSI to request service and is forbidden to use its interrupt pin
15:8	40h RO	**Next Capability Pointer (MSI_MC_NXT_PTR)**
7:0	5h RO	**Capability ID (MSI_MC_CAP_ID):** Hardwired to 0x5.

21.1.20 MSI Low Address (CNVI_WIFI_MSI_LOW_ADD)—Offset D4h

Specifies the lower DWORD of the address for the MSI memory write transaction (Offset 0D4 h)

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**MSG_ADD_LOW (MSG_ADD_LOW):** Lower DWORD of the address
1:0	0h RO	**MSI_LOW_AD_1_0 (MSI_LOW_AD_1_0):** HARDWIRED

21.1.21 MSI High Address (CNVI_WIFI_MSI_HIGH_ADD)—Offset D8h

Specifies the upper DWORD of the address for the MSI memory write transaction

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**MSG_ADD_UP (MSG_ADD_UP):** upper DWORD of the address

21.1.22 MSI Data (CNVI_WIFI_MSI_DATA)—Offset DCh

Written by the system to indicate the lower 16 bits of the data written in the MSI memory write DWORD transaction (Offset 0DC h)

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**MSG_DATA (MSG_DATA):** data written in the MSI memory write DWORD transaction

21.1.23 Uncorrectable Error Status Register (CNVI_WIFI_UNCORRECT_ERR_STAT)—Offset 104h

Bits in this register are of type RW1CS. Software may clear an error status by writing a 1

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved.
20	0h RW/1C	**Unsupported Request Error Status (UNSPR_REQ_ERR_ST):** Sticky value
19	0h RO	**ECRC Error Status (ECRC_ERR_STS_19):** Not implemented
18	0h RW/1C	**Malformed TLP Status (MAL_TLP_ST):** if set indicates that the error occurred. Sticky value
17	0h RW/1C	**Receiver Overflow Status (REC_OVRF_ERR):** if set indicates that the error occurred. Sticky value
16	0h RW/1C	**Unexpected Completion Status (UNXPC_COM_ER):** if set indicates that the error occurred. Sticky value
15	0h RW/1C	**Completer Abort Status (COM_AB_ERR):** if set indicates that the error occurred. Sticky value
14	0h RW/1C	**Completion Timeout Status (COM_TO_ERR):** if set indicates that the error occurred. Sticky value
13	0h RW/1C	**Flow Control Protocol Error Status (FLWCNT_PR_ER):** if set indicates that the error occurred. Sticky value
12	0h RW/1C	**Poisoned TLP Status (POIS_TLP_ERR):** if set indicates that the error occurred. Sticky value
11:5	0h RO	Reserved.
4	0h RW/1C	**Data Link Protocol Error Status (DLNK_PRERR_ST):** if set indicates that the error occurred. sticky value
3:1	0h RO	Reserved.
0	0h RO	**Training Error Status (TRNG_ERR_STS_0):** Not implemented.

21.1.24 Uncorrectable Error mask Register (CNVI_WIFI_UNCORRECT_ERR_MASK)—Offset 108h

Bits in this register are of type RWS - if set to 1 the error is not logged in the Header Log register, or does not update the First Error Pointer and is not reported to PCI Express Root Complex.

Access Method

Type: CFG Register (Size: 32 bits)

Device: 25
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved.
20	0h RW	**Unsupported Request Error Mask (UNSPR_REQ_ERR_MSK):** Sticky value.
19	0h RO	**ECRC Error mask (ECRC_ERR_MSK_19):** Not implemented.
18	0h RW	**Malformed TLP Mask (MAL_TLP_MSK):** Sticky value.
17	0h RW	**Receiver Overflow Mask (REC_OVRF_MSK):** Sticky value.
16	0h RW	**Unexpected Completion Mask (UNXPL_COM_MSK):** Sticky value.
15	0h RW	**Completer Abort Mask (COM_AB_MSK):** Sticky value.
14	0h RW	**Completion Timeout Mask (COM_TO_MSK):** Sticky value.
13	0h RW	**Flow Control Protocol Error Mask (FLWCNT_PR_MSK):** Sticky value.
12	0h RW	**Poisoned TLP Mask (POIS_TLP_MSK):** Sticky value.
11:5	0h RO	Reserved.
4	0h RW	**Header Log (DLNK_PRERR_MSK):** Does not update the First Error Pointer and is not Data Link Protocol Error Mask, if set to 1 the error is not logged in the Header. Sticky value
3:1	0h RO	Reserved.
0	0h RO	**Training Error Mask (TRNG_ERR_MSK_0):** Not implemented.

21.1.25 Uncorrectable Error Severity (CNVI_WIFI_UNCORRECT_ERR_SEV)—Offset 10Ch

Bit value in this register are sticky - the error is reported as fatal when the field is set to 1; if it is cleared to 0, the error is considered non-fatal.

Access Method

Type: CFG Register (Size: 32 bits)

Device: 25
Function: 0

Default: 62031h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved.
20	0h RW	**Unsupported Request Error Severity (UNSPR_REQ_ERR_SVR)**
19	0h RO	Reserved.
18	1h RW	**Malformed TLP Severity (MAL_TLP_SVR)**
17	1h RW	**Receiver Overflow Severity (REC_OVRF_SVR)**
16	0h RW	**Unexpected Completion Severity (UNXPL_COM_SVR)**
15	0h RW	**Completer Abort Severity (COM_AB_SVR)**
14	0h RW	**Completion Timeout Severity (COM_TO_SVR)**
13	1h RW	**Flow Control Protocol Error Severity (FLWCNT_PR_SVR)**
12	0h RW	**Poisoned TLP Severity (POIS_TLP_SVR)**
11:6	0h RO	Reserved.
5	1h RW	**Surprise Down Error Severity (SURPRISE_DWN_SVR)**
4	1h RW	**Data Link Protocol Error Severity (DLNK_PRERR_SVR)**
3:1	0h RO	Reserved.
0	1h RO	**Training Error severity (TRNG_ERR_SVR_0)**

21.1.26 Error Status (CNVI_WIFI_CORRECT_ERR_STAT)—Offset 110h

Reg bits in this register are of type RW1CS - if set to 1 indicates that the error occurred. Software may clear the bit by writing a 1.

Access Method

Type: CFG Register (Size: 32 bits)

Device: 25
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RW/1C	**Replay Timer Timeout Error Status (REPL_TO_ST)**
11:9	0h RO	Reserved.
8	0h RW/1C	**REPLAY_NUM Rollover Status (REPL_ROLVR_ST)**
7	0h RW/1C	**Bad DLLP Status (BD_DLLP_ST)**
6	0h RW/1C	**Bad TLP Status (BD_TLP_ST)**
5:1	0h RO	Reserved.
0	0h RW/1C	**REV_ERR_ST (REV_ERR_ST)**

21.1.27 Error Mask (CNVI_WIFI_CORRECT_ERR_MASK)—Offset 114h

Bits in this register are of type RWS (Sticky) - if set to 1 the error is masked and not reported.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RW	**Replay Timer Timeout Error Mask (REPL_TO_MSK)**
11:9	0h RO	Reserved.
8	0h RW	**REPLAY_NUM Rollover Mask (REPL_ROLVR_MSK)**
7	0h RW	**Bad DLLP Mask (BD_DLLP_MSK)**

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Bad TLP Mask (BD_TLP_MSK)**
5:1	0h RO	Reserved.
0	0h RW	**Receiver Error Mask (REV_ERR_MSK)**

21.1.28 Advanced Error Capabilities and Control (CNVI_WIFI_ADVANCED_ERR_CAP)—Offset 118h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 25
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RO	**ECRC Check Enable (ECRC_CHK_EN):** if set enables ECRC checking.
7	0h RO	**ECRC Check Capable (ECRC_CHK_CP):** indicates the device is capable of checking ECRC.
6	0h RO	**ECRC Generation Enable (ECRC_GEN_EN):** if set enables ECRC generation.
5	0h RO	**ECRC Generation Capable (ECRC_GEN_CP):** indicates that the device is capable of generation ECRC.
4:0	0h RO	**First Error Pointer (FRST_ERR_PNT):** error reported in the Uncorrectable Error Status register First Error Pointer, identifies bit position of the first

21.1.29 Header Log 1 (CNVI_WIFI_HEADER_LOG1)—Offset 11Ch

Captures the header of TLP associated with error.

Access Method

Type: CFG Register (Size: 32 bits)

Device: 25
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**HEADER_LOG_1 (HEADER_LOG_1):** captures the header of TLP associated with error

21.1.30 Header Log 2 (CNVI_WIFI_HEADER_LOG2)—Offset 120h

Captures the header of TLP associated with error.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**HEADER_LOG_2 (HEADER_LOG_2):** captures the header of TLP associated with error

21.1.31 Header Log 3 (CNVI_WIFI_HEADER_LOG3)—Offset 124h

Captures the header of TLP associated with error.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**HEADER_LOG_3 (HEADER_LOG_3):** captures the header of TLP associated with error

21.1.32 Header Log 4 (CNVI_WIFI_HEADER_LOG4)—Offset 128h

Captures the header of TLP associated with error.

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**HEADER_LOG_4 (HEADER_LOG_4):** captures the header of TLP associated with error

21.1.33 Device Serial Number Capability (CNVI_WIFI_GIO_SERIAL_CAP)—Offset 140h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 25
Function: 0

Default: 14C00000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14Ch RO	**NXT_CAP_OFF (NXT_CAP_OFF):** Next Capability Offset, next is the LTR header
19:16	0h RO	**CAP_VER (CAP_VER):** Capability Version: Zero to skip Serial Number
15:0	0h RO	**EXT_CAP_ID (EXT_CAP_ID):** PCI Express Extended Capability ID: Zero to skip Serial Number

21.1.34 Serial Number Low (CNVI_WIFI_GIO_SERIAL_LOW)—Offset 144h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 25
Function: 0

Default: FF000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	FFh RO	**HARDWIRED_SR_LW (HARDWIRED_SR_LW):** hardwired to 0xFF
23:16	0h RO	**Byte 6 (BYTE_6)**
15:8	0h RO	**Byte 5 (BYTE_5)**
7:0	0h RO	**Byte 4 (BYTE_4)**

21.1.35 Serial Number Upper (CNVI_WIFI_GIO_SERIAL_UP)—Offset 148h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 25
Function: 0

Default: FFh

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Byte 1 (BYTE_1)**
23:16	0h RO	**Byte 2 (BYTE_2)**
15:8	0h RO	**Byte 3 (BYTE_3)**
7:0	FFh RO	**HARDWIRED_SR_UP (HARDWIRED_SR_UP):** hardwired to 0xFF

21.1.36 Header of LTR Extended Capability (CNVI_WIFI_LTR_EXTND_CAP_HEAD)—Offset 14Ch

Access Method

Type: CFG Register (Size: 32 bits)

Device: 25
Function: 0

Default: 16410018h

Bit Range	Default & Access	Field Name (ID): Description
31:20	164h RO	**Next Capability Offset (LTR_HD_NXT_PTR):** Next is the Vendor Specific Capability Header.
19:16	1h RO	**Capability Version (LTR_HD_CAP_VER):** Hardwired to 1.
15:0	18h RO	**Capability ID (LTR_HD_CAP_ID):** PCI Express Extended Capability ID for the LTR Extended Capability is 0018h

21.1.37 No Snoop Request (CNVI_WIFI_LTR_MAX_SNOOP_NOSNOOP_LAT)—Offset 150h

This register specifies the maximum no-snoop latency that a device is permitted to request.

Access Method

Type: CFG Register (Size: 32 bits)

Device: 25
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:26	0h RW	**NSNP_MX_LAT_SCL (NSNP_MX_LAT_SCL):** no-snoop max latency scale. set by SW
25:16	0h RW	**NSNP_MX_LAT_VAL (NSNP_MX_LAT_VAL):** no-snoop max latency value. set by SW
15:13	0h RO	Reserved.
12:10	0h RW	**SNP_MAX_LAT_SCL (SNP_MAX_LAT_SCL):** snoop max latency scale. set by SW
9:0	0h RW	**SNP_MAX_LAT_VAL (SNP_MAX_LAT_VAL):** snoop max latency value. set by SW

21.1.38 L1 substates Extended Capability Header (CNVI_WIFI_L1PM_SUB_EXTND_CAP_HEAD)—Offset 154h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 25
Function: 0

Default: 1001Eh

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Next Capability Offset (NXT_PTR):** 0x0 for last extended capability.
19:16	1h RO	**Capability Version (CAP_VER):** Hardwired to 1.
15:0	1Eh RO	**Capability ID (EXT_CAP_ID):** PCI Express Extended Capability ID for L1 PM

21.1.39 L1 Substates Capability (CNVI_WIFI_L1PM_SUB_CAP)—Offset 158h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 25
Function: 0

Default: 481E1Fh

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:19	9h RO	**L1SUB_PWRON_REQ (L1SUB_PWRON_REQ):** Port requirement for T_POWER_ON value
18	0h RO	Reserved.
17:16	0h RO	**T_PWRON_SCALE (T_PWRON_SCALE):** Portrequirement for T_POWER_ON scale
15:8	1Eh RO	**CMN_RESTORE_TM (CMN_RESTORE_TM):** Port common mode restore time
7:5	0h RO	Reserved.
4	1h RO	**L1SUB_PM_SUP (L1SUB_PM_SUP):** 1 = L1 PM substate supported.
3	1h RO	**L11_ASPM_SUP (L11_ASPM_SUP):** 1 = ASPM L1.1 is supported.
2	1h RO	**L12_ASPM_SUP (L12_ASPM_SUP):** 1 = ASPM L1.2 is supported.
1	1h RO	**L11_PM_SUP (L11_PM_SUP):** 1 = PM L1.1 is supported.
0	1h RO	**L12_PM_SUP (L12_PM_SUP):** 1 = PM L1.2 is supported.

21.1.40 L1 Substates Control (CNVI_WIFI_L1PM_SUB_CNTRL)—Offset 15Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 25
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW	**LTR_L1_THRS_SCL (LTR_L1_THRS_SCL):** LTR L1.2 threshold scale
28:26	0h RO	Reserved.
25:16	0h RW	**LTR_L1_THRS_VAL (LTR_L1_THRS_VAL):** LTR L1.1 threshold value, detemines if entry to L1 results in L1.1 or L1.2 (if they are enabled). scale of value set by: LTR L1.2 threshold scale
15:4	0h RO	Reserved.
3	0h RW	**L11_ASPM_EN (L11_ASPM_EN):** L1.1 ASPM is enabled

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**L12_ASPM_EN (L12_ASPM_EN):** L1.2 ASPM is enabled
1	0h RW	**L11_PM_EN (L11_PM_EN):** L1.1 PM is enabled
0	0h RW	**L12_PM_EN (L12_PM_EN):** L1.2 PM is enabled

21.1.41 L1 Substates Control 2 (CNVI_WIFI_L1PM_SUB_CNTRL2)—Offset 160h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: 28h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:3	5h RW	**T_POWER_ON_VAL (T_POWER_ON_VAL):** T power on value. Along with power on scale - sets min time in L1.2.exit
2	0h RO	Reserved.
1:0	0h RW	**L12_PWRON_SCALE (L12_PWRON_SCALE):** T power on scale. 0 =2us, 1=10us, 2=100us, 11 = reserved

21.1.42 Vendor Specific Capability Header (CNVI_WIFI_VEN_SPEC_CAP)—Offset 164h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 25
Function: 0

Default: 1000Bh

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Next Capability Offset (VSNEXT):** This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities.
19:16	1h RO	**Vendor Specific Extended Capability Revision (VSECREV):** The version of the PCIe capability structure present. Hardwired to 1h.
15:0	Bh RO	**Vendor Specific PCI Express Extended Capability ID (VSPCIECID):** The Extended Capability ID for the Vendor-Specific Capability is 000Bh.

21.1.43 Vendor Specific Extended Capability (CNVI_WIFI_VEN_SPEC_EXTND_CAP)—Offset 168h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 25
Function: 0

Default: 1400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	14h RO	**VSECLEN (VSECLEN):** Vendor Specific Extended Capability Length (VSECLEN): This field indicates the # of bytes of this Vendor Specific capability inclusive of the 1st DW which includes the capability ID and Next pointer. For DevIdle, this is 14h
19:16	0h RO	**VSECREV (VSECREV):** Vendor Specific Extended Capability Revision (VSECREV): For this revision of DevIdle, this field is 0h
15:0	10h RO	**VSECID (VSECID):** Vendor Specific Extended Capability ID (VSECID): DevIdle has been assigned the Intel VSEC ID of 10h

21.1.44 SW LTR Pointer (CNVI_WIFI_LTP_PTR)—Offset 16Ch

Access Method

Type: CFG Register (Size: 32 bits)

Device: 25
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**SWLTRLOC (SWLTRLOC):** SW LTR Update MMIO Offset Location This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR. The value of this register is a don't care, if the Valid bit is not set
19:4	0h RO	Reserved.
3:1	0h RO	**BARNUM (BARNUM):** Base Address Register Number. Contains the 0's based AR Number of the BAR which contains the location of the SW LTR MMIO register.
0	0h RO	**VALID (VALID):** Hardwired to '0' to indicate that the function has not implemented a SW LTR register that is compliant to the DevIdle definition. This could be because the function has not implemented SW LTR at all, or has a device specific version of SW LTR.

21.1.45 DevIdle Pointer (CNVI_WIFI_DEV_IDLE_PTR)—Offset 170h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 25
Function: 0

Default: 31800001h

Bit Range	Default & Access	Field Name (ID): Description
31:20	318h RO	**DEVIDLELOC (DEVIDLELOC):** DevIdle MMIO Offset Location.Contains the location pointer to the DevIdle register in MMIO space, as an offset from the specified BAR. The value of this register is a don't care, if the Valid bit is not set
19:4	0h RO	Reserved.
3:1	0h RO	**BARNUM (BARNUM):** Base Address Register Number. Contains the 0's based BAR Number of the BAR which contains the location of the DevIdle MMIO register. When counting BAR Numbers, all BARs, regardless of size and type, consume one BAR BAR Number. Bar 0 is the 1st BAR. The value of this register is a don't care, if the Valid bit is not set. Fixed to 3'b0
0	1h RO	**VALID (VALID):** Hardwired to '1' to indicate that the function has implemented a DevIdle register as specified in the DevIdle that can be located using the DEVIDLELOC register and BARNUM.

21.1.46 DevIdle Power on Latency (CNVI_WIFI_DEV_IDLE_PWR)—Offset 174h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 25
Function: 0

Default: 800h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12:10	2h RO	**POLS (POLS):** Power On Latency Scale. Latency Scale multiplier: 010: 1us 011: 32us All other settings are reserved. The value of this register is multiplied with the Power On Latency Value (POLV) to provide the DevIdle power on exit latency multiplier scale from 1us to 32ms.
9:0	0h RO	**POLV (POLV):** Power On Latency Value. 10-bit value that is multiplied by the Power On Latency Scale. A value of 0 indicates a power on latency of less than 1us.

22 Integrated Sensor Hub (ISH) (D19:F0)

22.1 ISH PCI Configuration Registers Summary

Table 22-1. Summary of ISH PCI Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID (DEVVENDID)—Offset 0h	22D88086h
4h	7h	Status and Command (STATUSCOMMAND)—Offset 4h	100000h
8h	Bh	Revision ID and Class Code (REVCLASSCODE)—Offset 8h	6h
Ch	Fh	Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch	800000h
10h	13h	Base Address Register (BAR)—Offset 10h	4h
14h	17h	Base Address Register High (BAR_HIGH)—Offset 14h	0h
18h	1Bh	Base Address Register1 (BAR1)—Offset 18h	0h
1Ch	1Fh	Base Address Register1 High (BAR1_HIGH)—Offset 1Ch	0h
2Ch	2Fh	Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch	0h
34h	37h	Capabilities Pointer (CAPABILITYPTR)—Offset 34h	80h
3Ch	3Fh	Interrupt Register (INTERRUPTREG)—Offset 3Ch	0h
80h	83h	PowerManagement Capability ID (POWERCAPID)—Offset 80h	48039001h
84h	87h	Power Management Control and Status (PMECTRLSTATUS)—Offset 84h	8h
90h	93h	PCI Device Idle Vendor Capability (PCIDEVIDLE_CAP_RECORD)—Offset 90h	F0140009h
98h	9Bh	Software LTR Update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h	0h
A0h	A3h	D0i3 And Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h	80800h

22.1.1 Device ID and Vendor ID (DEVVENDID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 18
Function: 0

Default: 22D88086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	22D8h RO/P	**Device Identification (DEVICEID):** This is a 16-bit value assigned to the PCH ISH.
15:0	8086h RO	**Vendor Identification (VENDORID):** This is a 16-bit value assigned to Intel. Intel VID = 8086h

22.1.2 Status and Command (STATUSCOMMAND)—Offset 4h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 18
Function: 0

Default: 100000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	0h RW/1C	**Received Master Abort (RMA)**
28	0h RW/1C	**Received Target Abort (RTA)**
27:21	0h RO	Reserved.
20	1h RO	**Capabilities List (CAPLIST):** Indicates that the controller contains a capabilities pointer list
19	0h RO	**Interrupt Status: (INTR_STATUS):** This bit reflects state of interrupt in the device
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTR_DISABLE)**
9	0h RO	Reserved.
8	0h RW	**SERR Enable (SERR_ENABLE):** Not implemented
7:3	0h RO	Reserved.
2	0h RW	**Bus Master Enable (BME)**
1	0h RW	**Memory Space Enable (MSE):** 0 = Disables memory mapped configuration space. 1 = Enables memory mapped configuration space
0	0h RO	Reserved.

22.1.3 Revision ID and Class Code (REVCLASSCODE)—Offset 8h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 18
Function: 0

Default: 6h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Class Code (CLASS_CODES):** Class Code register is read-only and is used to identify the generic function of the device and in some cases a specific register-level programming interface
7:0	6h RO/P	**Revision ID (RID):** Revision ID identifies the revision of particular PCI device.

22.1.4 Cache Line Latency Header and BIST (CLLATHEADERBIST)—Offset Ch

Cache Line size as RW with def 0 Latency timer RW with def 0 Header type with Type 0 configuration header and Reserved BIST register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 18
Function: 0

Default: 800000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO	**Multi-Function Device (MULFNDEV)**
22:16	0h RO	**Header Type (HEADERTYPE):** Implements Type 0 Configuration header
15:8	0h RO	**Latency Timer (LATTIMER)**
7:0	0h RW/P	**Cache Line Size (CACHELINE_SIZE)**

22.1.5 Base Address Register (BAR)—Offset 10h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 18
Function: 0

Default: 4h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Base Address (BASEADDR):** Provides system memory base address.
11:4	0h RO	**Size Indicator (SIZEINDICATOR):** Always returns. 0 The size of this register depends on the size of the memory space
3	0h RO	**Prefetchable (PREFETCHABLE):** Indicates that this BAR is not prefetchable
2:1	2h RO	**Type (TYPE):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE):** 0 indicates this BAR is present in the memory space.

22.1.6 Base Address Register High (BAR_HIGH)—Offset 14h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 18
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Address high (BASEADDR_HIGH)**

22.1.7 Base Address Register1 (BAR1)—Offset 18h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 18
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**Base Address 1 (BASEADDR1):** Base Address1 This field is present if BAR1 is enabled through private configuration space.
11:4	0h RO	**Size Indicator (SIZEINDICATOR1):** Always is 0 as minimum size is 4K
3	0h RO	**Prefetchable (PREFETCHABLE1):** Indicates that this BAR is not prefetchable.
2:1	0h RO	**Type (TYPE1):** If BAR_64b_EN is 0 then 00 indicates BAR lies in 32bit address range If BAR_64b_EN is 1 then 10 Indicates BAR lies in 64 bit address range
0	0h RO	**Memory Space Indicator (MESSAGE_SPACE1):** 0 Indicates this BAR is present in the memory space.

22.1.8 Base Address Register1 High (BAR1_HIGH)—Offset 1Ch

Base Address Register1 High enabled only if [2:1] of BAR1 register is 10

Access Method

Type: CFG Register (Size: 32 bits)
Device: 18
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Base Address 1 High (BASEADDR1_HIGH)**

22.1.9 Subsystem Vendor and Subsystem ID (SUBSYSTEMID)—Offset 2Ch

SVID register along with SID register is to distinguish subsystem from another

Access Method

Type: CFG Register (Size: 32 bits)
Device: 18
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/O/P	**Subsystem ID (SUBSYSTEMID):** This register is implemented for any function that can be instantiated more than once in a given system.
15:0	0h RW/O/P	**Subsystem Vendor ID (SUBSYSTEMVENDORID):** This register must be implemented for any function that can be instantiated more than once in a given system

22.1.10 Capabilities Pointer (CAPABILITYPTR)—Offset 34h

Access Method

Type: CFG Register (Size: 32 bits)
Device: 18
Function: 0

Default: 80h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	80h RO	**Capabilities Pointer (CAPPTR_POWER):** Indicates what the next capability is.

22.1.11 Interrupt Register (INTERRUPTREG)—Offset 3Ch

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 18
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Max Latency (MAX_LAT):** Value of 0 indicates device has no major requirements for the settings of latency timers
23:16	0h RO	**Min Latency (MIN_GNT):** Value of 0 indicates device has no major requirements for the settings of latency timers // Re-Check Desc Padma
15:12	0h RO	Reserved.
11:8	0h RO	**Interrupt Pin (INTPIN)**
7:0	0h RW/P	**Interrupt Line (INTLINE):** It is used to communicate to software, the interrupt line to which the interrupt pin is connected

22.1.12 PowerManagement Capability ID (POWERCAPID)—Offset 80h

PowerManagement Capability ID register points to next capability structure and power mgmnt capability with Power management capabilities register for PME support and version

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 18
Function: 0

Default: 48039001h

Bit Range	Default & Access	Field Name (ID): Description
31:27	9h RO	**PME Support (PMESUPPORT):** This 5-bit field indicates the power states in which the function can assert the PME#
26:19	0h RO	Reserved.
18:16	3h RO	**Version (VERSION):** Indicates support for Revision 1.2 of the PCI Power Management Specification
15:8	90h RO	**Next Capability (NXTCAP):** Points to the next capability structure.
7:0	1h RO	**Power Management Capability (POWER_CAP):** Indicates this is power management capability.

22.1.13 Power Management Control and Status (PMECTRLSTATUS)—Offset 84h

power management control and status register to set and read PME status PME enable No Soft reset and power state

Access Method

Type: CFG Register (Size: 32 bits)

Device: 18

Function: 0

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C/P	**PME Status (PMESTATUS)**
14:9	0h RO	Reserved.
8	0h RW/P	**PME Enable (PMEENABLE)**
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NO_SOFT_RESET):** This bit indicates that devices transitioning from D3hot to D0 because of Powerstate commands do not perform an internal reset
2	0h RO	Reserved.
1:0	0h RW	**Power State (POWERSTATE):** This field is used both to determine the current power state and to set a new power state.

22.1.14 PCI Device Idle Vendor Capability (PCIDEVIDLE_CAP_RECORD)—Offset 90h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 18
Function: 0

Default: F0140009h

Bit Range	Default & Access	Field Name (ID): Description
31:28	Fh RO	**Vendor Cap Field (VEND_CAP):** Vendor Specific Capability ID
27:24	0h RO	**Revision IDField (REVID):** Revision ID of capability structure
23:16	14h RO	**Cap Length Field (CAP_LENGTH):** Vendor Specific Capability Length
15:8	0h RO	**Next Capability Field (NEXT_CAP):** Next Capability
7:0	9h RO	**Capability ID Field (CAPID):** Capability ID

22.1.15 Software LTR Update MMIO Location (D0I3_CONTROL_SW_LTR_MMIO_REG)—Offset 98h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 18
Function: 0

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	**SW LTR Dword Offset Field (SW_LAT_DWORD_OFFSET):** SW LTR Update MMIO Offset Location (SWLTRLOC)
3:1	0h RO	**SW LTR BAR Number Field (SW_LAT_BAR_NUM):** Indicates that the SW LTR update MMIO location is always at BAR0
0	0h RO	**SW LTR Valid Field (SW_LAT_VALID):** This value is reflected from the SW LTR valid strap at the top level

22.1.16 D0i3 And Power Control Enable Register (D0I3_MAX_POW_LAT_PG_CONFIG)—Offset A0h

Access Method

Type: CFG Register (Size: 32 bits)

Device: 18
Function: 0

Default: 80800h

Bit Range	Default & Access	Field Name (ID): Description
31:22	0h RO	Reserved.
21	0h RW/P	**HAE Field (HAE):** Hardware Autonomous Enable
20	0h RO	Reserved.
19	1h RW/P	**Sleep Enable Field (SLEEP_EN):** Sleep Enable
18	0h RW/P	**D3 Hen Field (D3HEN):** DEVIDLE Enable (DEVIDLEN): If 1 then the function will power gate when idle and the DevIdle register (DevIdleC[2] = 1) is set.
17	0h RW/P	**Device Idle En Field (DEVIDLEN):** PMCRE: PMC Request Enable
16	0h RW/P	**PMC Request Enable Field (PMCRE):** D3-Hot Enable (D3HEN): If 1 then function will power gate when idle and the PMCSR[1:0] register in the function = 11 (D3).
15:13	0h RO	Reserved.
12:10	2h RW/O/P	**Power Latency Scale Field (POW_LAT_SCALE):** Power On Latency Scale
9:0	0h RW/O/P	**Power Latency Value Field (POW_LAT_VALUE):** Power On Latency value

22.2 ISH MMIO Registers Summary

Table 22-2. Summary of ISH MMIO Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
34h	37h	ISH Host Firmware Status (ISH_HOST_FWSTS)—Offset 34h	0h
38h	3Bh	Host Communication (HOST_COMM)—Offset 38h	0h
48h	4Bh	Inbound Doorbell Host To ISH (HOST2ISH_DOORBELL)—Offset 48h	0h
54h	57h	Outbound Doorbell ISH to Host (ISH2HOST_DOORBELL)—Offset 54h	0h
60h	63h	Outbound ISH to Host Message (ISH2HOST_MSG1)—Offset 60h	0h
E0h	E3h	Inbound Host to ISH Message (HOST2ISH_MSG1)—Offset E0h	0h
360h	363h	Remap 0 (REMAP0)—Offset 360h	0h
364h	367h	REMAP 1 (REMAP1)—Offset 364h	0h
368h	36Bh	REMAP 2 (REMAP2)—Offset 368h	0h
36Ch	36Fh	REMAP 3 (REMAP3)—Offset 36Ch	0h
6D0h	6D3h	D0I3 Control (IPC_d0i3C_reg)—Offset 6D0h	8h

22.2.1 ISH Host Firmware Status (ISH_HOST_FWSTS)—Offset 34h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**ISH_HOST_FWSTS:** This is a 32 bit register which is set to 0x0000 on a system reset or a wakeup from D3Cold. As the firmware comes up after the reset or power cycle it sets bits of this register to indicate its status.

22.2.2 Host Communication (HOST_COMM)—Offset 38h

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**HOST_COMM:** Host communication register.

22.2.3 Inbound Doorbell Host To ISH (HOST2ISH_DOORBELL)—Offset 48h

Inbound doorbell register, Host core to interrupt ISH. Data 30:0 is 31bits message payload used for backward compatibility. Software can use either this 31bit message payload or 256bit payload registers. When software writes the message in to respective message register, it should set bit 31(BUSY Bit) of doorbell register to indicate that new data is written. The ISH will assert a level sensitive interrupt to the IOAPIC as long as the BUSY bit is set. When the ISH reads the message code from this register it should write back to this register and clear the BUSY bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**BUSY:** When this bit is cleared, the ISH CPU is Ready to accept a new message.
30:0	0h RW	**PAYLOAD_31BIT:** 31bits message payload for backward compatibility.

22.2.4 Outbound Doorbell ISH to Host (ISH2HOST_DOORBELL)—Offset 54h

Outbound doorbell register for the ISH to interrupt the Host. Setting bit 31 of this register causes the Host to receive a IRQn interrupt. Data 30:0 is 31bits message payload used for backward compatibility. Software can use either this 31bit message payload or 256bit payload registers. The ISH will set bit 31 of this reg to ring the doorbell after it has completed programming the message to Host. When the Host reads the message code from this register it should write back to this register and clear the BUSY bit.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**BUSY:** When this bit is cleared, the HOST CPU is Ready to accept a new message.
30:0	0h RW	**PAYLOAD_31BIT:** 31bits message payload for backward compatibility.

22.2.5 Outbound ISH to Host Message (ISH2HOST_MSG1)—Offset 60h

Inter-process Message registers for ISH core to communicate to the HOST. These are eight 32bit registers that hold the message payload from the ISH to Host. These registers are meant to be written by the ISH and read by Host. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**MSG:** Message from ISH to HOST.

22.2.6 Inbound Host to ISH Message (HOST2ISH_MSG1)—Offset E0h

Inter-process Message registers for Host to communicate to the ISH. These are eight 32bit registers that hold the message payload from the Host to ISH. These registers are meant to be written by the Host and read by ISH. The format of the message bit 31:0 is defined in the ISH FW specification. When software writes the message in this registers, it should set bit 31(BUSY Bit) of the doorbell register.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**MSG:** Message from HOST to ISH.

22.2.7 Remap 0 (REMAP0)—Offset 360h

Remap register for Host to communicate addresses to ISH.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**REMAP0:** REMAP0.

22.2.8 REMAP 1 (REMAP1)—Offset 364h

Remap register for Host to communicate addresses to ISH.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**REMAP1:** REMAP1.

22.2.9 REMAP 2 (REMAP2)—Offset 368h

Remap register for Host to communicate addresses to ISH.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**REMAP2:** REMAP2.

22.2.10 REMAP 3 (REMAP3)—Offset 36Ch

Remap register for Host to communicate addresses to ISH.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**REMAP3:** REMAP3.

22.2.11 D0I3 Control (IPC_d0i3C_reg)—Offset 6D0h

This is a 32 bit register which is set to 0 on a system reset or a wakeup from D3Cold. When ME writes to any of these bits with 1, an interrupt is generated. The Interrupt is then cleared by writing 1`b1 to this register after the appropriate ISR is serviced.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved (RESERVED0):** D0i3 register for storing power related information.
4	0h RO	Reserved.
3	1h RW/1C	**Resetore Required (RR):** D0i3 register for storing power related information.
2	0h RW	**D0i3 (D0i3):** D0i3 register for storing power related information.
1	0h RW	**Interrupt Required (IR):** D0i3 register for storing power related information.
0	0h RW/1C	**Command In Progress (CIP):** D0i3 register for storing power related information.

23 Touch Host Controller (THC) Interface

23.1 Touch Host Controller (D16:F6 and D16:F7) Registers Summary

Table 23-1. Summary of Touch Host Controller (D16:F6 and D16:F7) Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Device ID and Vendor ID (THC_CFG_DID_VID)—Offset 0h	XXXX8086h
4h	7h	Status and Command (THC_CFG_STS_CMD)—Offset 4h	2900000h
8h	Bh	Revision ID and Class Code (THC_CFG_CC_RID)—Offset 8h	90100XXh
Ch	Fh	BIST_Header Type_Latency Timer_Cache Line Size (THC_CFG_BIST_HTYPE_LT_CLS)—Offset Ch	800000h
10h	13h	THC BAR0 MMIO Low (THC_CFG_BAR0_LOW)—Offset 10h	4h
14h	17h	THC BAR0 MMIO High (THC_CFG_BAR0_HI)—Offset 14h	0h
2Ch	2Fh	Subsystem and Vendor ID (THC_CFG_SID_SVID)—Offset 2Ch	0h
34h	37h	Capability List Pointer (THC_CFG_CAPP)—Offset 34h	50h
3Ch	3Fh	Interrupt Configuration (THC_CFG_INT)—Offset 3Ch	0h
40h	43h	THC Unsupported Request Status (THC_CFG_UR_STS_CTL)—Offset 40h	0h
50h	53h	MSI Message Control_ Next Pointer and Capability ID (THC_CFG_MSIMC_MSINP_MSICID)—Offset 50h	807005h
54h	57h	MSI Message Address (THC_CFG_MSIMA)—Offset 54h	0h
58h	5Bh	MSI Message Upper Address (THC_CFG_MSIMUA)—Offset 58h	0h
5Ch	5Fh	MSI Message Data (THC_CFG_MSIMD)—Offset 5Ch	0h
70h	73h	PCI Power Management Capability (THC_CFG_PMCAP_PMNP_PMCID)—Offset 70h	C0030001h
74h	77h	PCI Power Management Control and Status (THC_CFG_PMD_PMCSRBSE_PMCSR)—Offset 74h	8h
90h	93h	Device Idle Capability (THC_CFG_DEVIDLE)—Offset 90h	F0140009h
94h	97h	Vendor Specific Header (THC_CFG_VSHDR)—Offset 94h	1400010h
98h	9Bh	SW LTR Pointer Register (THC_CFG_SWLTRPTR)—Offset 98h	0h
9Ch	9Fh	Device Idle Pointer Register (THC_CFG_DEVIDLEPTR)—Offset 9Ch	101h
A0h	A3h	Device Idle Power On Latency (THC_CFG_DEVIDLEPOL)—Offset A0h	800h
A4h	A7h	Power Control Enables (THC_CFG_PCE)—Offset A4h	8h

23.1.1 Device ID and Vendor ID (THC_CFG_DID_VID)—Offset 0h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: XXXX8086h

Bit Range	Default and Access	Field Name (ID): Description
31:16	-- RO/V	**Device Identification (DID):** This is a 16-bit value assigned to the controller. Refer the Device and Revision ID Table in Volume 1 for the default value.
15:0	8086h RO	**Vendor Identification (VID):** This field identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. 0x8086 indicates Intel

23.1.2 Status and Command (THC_CFG_STS_CMD)—Offset 4h

This is a standard PCI config register. Refer the PCI spec for bit descriptions.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 2900000h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/1C/V	**Detected Parity Error (DPE):** Refer the PCI spec.
30	0h RW/1C/V	**Signaled System Error (SSE):** Refer the PCI spec.
29	0h RW/1C/V	**Received Master Abort (RMA):** Refer the PCI spec
28	0h RW/1C/V	**Received Target Abort (RTA):** Refer the PCI spec
27	0h RW/1C/V	**Signaled Target Abort (STA):** Refer the PCI spec
26:25	1h RO	**Devsel Timing (DEVT):** Refer the PCI spec
24	0h RW/1C/V	**Master Data Parity Error (MDPE):** Refer the PCI spec
23	1h RO	**Fast Back to Back Capable (FBTBC):** Has no meaning on the internalbackbone
22	0h RO	Reserved.
21	0h RO	**66 Mhz Capable (MCAP):** Not 66 MHz capable device. Has no meaning on the internal backbone.
20	1h RO	**Capablities List (CAPL):** Refer the PCI spec
19	0h RO/V	**Interrupt Status (INTS):** Refer the PCI spec
18:11	0h RO	Reserved.
10	0h RW	**Interrupt Disable (INTD):** Refer the PCI spec

Bit Range	Default and Access	Field Name (ID): Description
9	0h RO	**Fast Back to Back Enable (FBTBEN):** Refer the PCI spec
8	0h RW	**System Error Enable (SERREN):** Refer the PCI spec
7	0h RO	Reserved.
6	0h RW	**Parity Error Response (PERRR):** Refer the PCI spec
5	0h RO	**VGA Palette Snoop (VGAPS):** Refer the PCI spec
4	0h RO	**Memory Write and Invalidate Enable (MWRIEN):** Refer the PCI spec
3	0h RO	**Special Cycles (SPCYC):** Refer the PCI spec
2	0h RW	**Bus Master Enable (BME):** Refer the PCI spec
1	0h RW	**Memory Space Enable (MSE):** Refer the PCI spec
0	0h RO	**IO Space Enable (IOSE):** Refer the PCI spec

23.1.3 Revision ID and Class Code (THC_CFG_CC_RID)—Offset 8h

Revision ID and Class Code

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 90100XXh

Bit Range	Default and Access	Field Name (ID): Description
31:24	9h RW/O	**Base Class Code (BCC):** Input Device. It is a requirement that this can be programmed by BIOS following a Host reset.
23:16	1h RW/O	**Sub-Class Code (SCC):** 01h= Digitizer. It is a requirement that this can be programmed by BIOS following a Host reset.
15:8	0h RW/O	**Programming Interface (PI):** 00h = Touch Host Controller that conforms to this specification.
7:0	-- RO/V	**Revision ID (RID):** Indicates the part revision. This will reset to 0 but will overridden by the SetID IOSF-SB message during the power-up sequence.

23.1.4 BIST_Header Type_Latency Timer_Cache Line Size (THC_CFG_BIST_HTYPE_LT_CLS)—Offset Ch

BIST_Header Type, Latency Timer, Cache Line Size

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 800000h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	1h RO/V	**Multi-function Device (MFD):** See the PCI spec. The default value is from the top level parameter THC_PCI_MFD. (Note: Onesource does not support parameter for the reset value. SO the parameter need to be added to RTL/RDL directly.)
22:16	0h RO	**Header Type (HTYPE):** See the PCI spec.
15:8	0h RO	**Latency Timer (LT):** See the PCI spec.
7:0	0h RO	**Cacheline Size (CLSZ):** See the PCI spec.

23.1.5 THC BAR0 MMIO Low (THC_CFG_BAR0_LOW)—Offset 10h

Attributes and lower address bits of base address for MMIO registers.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
31:15	0h RW	**Memory BAR (MEMBAR):** Software programs this register with the lower 32 bit base address of the device's memory region. The MMIO registers in the touch controller are offset from this BAR.
14:4	0h RO	**Memory Size (MEMSIZE):** Hardwired to 0 to indicate 32KB of memory space.
3	0h RO	**Prefetchable (PREFETCH):** A device can mark a range as prefetchable if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables.
2:1	2h RO	**Type (TYP):** If this field is hardwired to 00 it indicates that this range can be mapped anywhere within 32-bit address space. If this field is hardwired to 10 it indicates that this range can be mapped anywhere within 64-bit address space.
0	0h RO	**Memory Space Indicator (MEMSPACE):** Hardwired to 0 to identify a Memory BAR.

23.1.6 THC BAR0 MMIO High (THC_CFG_BAR0_HI)—Offset 14h

Upper address bits of base address for MMIO registers.

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Memory BAR (MEMBAR):** Software programs this register with the high 32-bit base address of the device's memory region. The MMIO registers in the touch controller are offset from this BAR.

23.1.7 Subsystem and Vendor ID (THC_CFG_SID_SVID)—Offset 2Ch

Subsystem and Vendor ID

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RW/O	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value.
15:0	0h RW/O	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value.

23.1.8 Capability List Pointer (THC_CFG_CAPP)—Offset 34h

Capability List Pointer

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 50h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	50h RO	**Capability Pointer (CP):** This register points to the starting offset of the capabilities ranges.

23.1.9 Interrupt Configuration (THC_CFG_INT)—Offset 3Ch

Interrupt Configuration

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	0h RW/O	**Interrupt pin (IPIN):** reflect the Interrupt Pin assigned to the host controller by the platform (and are hardwired). 8'h01 = INTA 8'h02 = INTB 8'h03 = INTC 8'h04 = INTD others = INTA
7:0	0h RW	**Interrupt Line (ILINE):** This data is not used by the THC. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

23.1.10 THC Unsupported Request Status (THC_CFG_UR_STS_CTL)—Offset 40h

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.
2	0h RW/L	**Function Disable (FD):** If set to 1 by software, THC is disabled
1	0h RW/1C/V	**Unsupported Request Detected (URD):** Set to 1 by hardware upon detecting an Unspported Request that is not considered an Advisory Non-Fatal error. Cleared to 0 when software writes a 1 to this register.
0	0h RW	**Unsupported Request Reporting Enabled (URRE):** If set to 1 by software, the touch host controller generates a DoSERR sideband message when the URD bit transitions from 0 to 1.

23.1.11 MSI Message Control_ Next Pointer and Capability ID (THC_CFG_MSIMC_MSINP_MSICID)—Offset 50h

MSI Message Control, Next Pointer and Capability ID

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 807005h

Bit Range	Default and Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RO	**Per Vector Masking Capable (PVMC):** This function does not support MSI per vector masking
23	1h RO	**64 bit address capable (XAC):** This function is not capable of sending 64 bit message address
22:20	0h RO	**Multiple Message Enable (MMEN):** Encoded number of interrupt vectors allocated by SW. Value of zero indicates one vector.
19:17	0h RO	**Multiple Message Capable (MMC):** Encoded number of interrupt vectors supported. Value of zero indicates one vector.
16	0h RW	**MSI Enable (MSIE):** If set to '1' MSI interrupt delivery is enabled. When this bit is cleared, prior to returning the configuration write completion, the device must send any pending MSI(s).
15:8	70h RO	**Next Item Pointer (NXTP):** Indicates the pointer for the next entry in the capabilities list
7:0	5h RO	**Capability ID (CAPID):** Indicates the linked list item as being the MSI Capability registers

23.1.12 MSI Message Address (THC_CFG_MSIMA)—Offset 54h

Lower bits of the MSI Message Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:2	0h RW	**Message Address (MADDR):** DW aligned MSI message address.
1:0	0h RO	Reserved.

23.1.13 MSI Message Upper Address (THC_CFG_MSIMUA)—Offset 58h

Upper bits of the MSI Message Address

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**Message Address (MAUDDR):** Upper DW MSI message address.

23.1.14 MSI Message Data (THC_CFG_MSIMD)—Offset 5Ch

MSI Message Data

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	0h RW	**Message Data (MDAT):** MSI Message Data

23.1.15 PCI Power Management Capability (THC_CFG_PMCAP_PMNP_PMCID)—Offset 70h

PCI Power Management Capability

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: C0030001h

Bit Range	Default and Access	Field Name (ID): Description
31:27	18h RW/O	**PME Support (PMES):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(27) X XXX1b - PME# can be asserted from D0 bit(28) X XX1Xb - PME# can be asserted from D1 bit(29) X X1XXb - PME# can be asserted from D2 bit(30) X 1XXXb - PME# can be asserted from D3hot bit(31) 1 XXXXb - PME# can be asserted from D3cold
26	0h RO	**D2 Support (D2S):** This device does not support D2
25	0h RO	**D1 Support (D1S):** This device does not support D1
24:22	0h RO	**Aux Current (AUXC):** Not Applicable
21	0h RO	**Device Specific Initialization (DSI):** See PCI Power Management Interface specification.
20	0h RO	Reserved.
19	0h RO	**PME Clock (PMECLK):** Not Applicable
18:16	3h RO	**Version (VER):** Value of 011b indicates that this function complies with rev 1.2 of PCI Power Management Interface Spec
15:8	0h RW/O	**Next Item Pointer (NXTP):** Indicates the pointer for the next entry in the capabilities list
7:0	1h RO	**Capability ID (CAPP):** Indicates the linked list item as being the PCI Power Management registers

23.1.16 PCI Power Management Control and Status (THC_CFG_PMD_PMCSRBSE_PMCSR)—Offset 74h

PCI Power Management Control and Status

Access Method

Type: CFG Register (Size: 32 bits)

Device: 16
Function: 6

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	0h RW/1C/V	**PME Status (PMESTS):** See PCI Power Management Interface specification. This bit is set when the THC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). Writing a 0 has no effect. This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14:13	0h RO	**Data Scale (DS):** Not Applicable

Bit Range	Default and Access	Field Name (ID): Description
12:9	0h RO	**Data Select (DSEL):** Not Applicable
8	0h RW	**PME Enable (PMEEN):** See PCI Power Management Interface specification.
7:4	0h RO	Reserved.
3	1h RO	**No Soft Reset (NSR):** When set to 1, this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.
2	0h RO	Reserved.
1:0	0h RW/V	**Power State (PWRST):** This 2-bit field is used both to determine the current power state of THC function and to set a new power state. The definition of the field values are: 00b - D0 state 11b - D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally however, the data is discarded and no state change occurs. When in the D3hot state, the Intel PCH must not accept accesses to the THC memory range but the configuration space must still be accessible.

23.1.17 Device Idle Capability (THC_CFG_DEVIDLE)—Offset 90h

Device Idle Capability

Access Method

Type: CFG Register (Size: 32 bits)

Device: 16

Function: 6

Default: F0140009h

Bit Range	Default and Access	Field Name (ID): Description
31:28	Fh RO	**Vendor-Specific Capability ID (VID):** A value of Fh in this 4-bit field identifies this Vendor Specific Capability as an Extended Capability, which uses a VSEC 16-bit Extended Capability ID in the subsequent four bytes. This field allows software to differentiate this capability from other Vendor Specific capabilities.
27:24	0h RO	**Vendor-Specific Capability Revision (REV):** For a VID of Fh, this field is reserved 0h.
23:16	14h RO	**Length (LENGTH):** Indicates that this capability is 20 bytes long.
15:8	0h RO	**Next Capability Pointer (NCAPPP):** This field contains the offset to the next PCI Capability structure or 000h if no other items exist in the linked list of Capabilities.
7:0	9h RO	**Capability ID (CAPPID):** The value of 09h in this field indicates a Vendor Specific capability.

23.1.18 Vendor Specific Header (THC_CFG_VSHDR)—Offset 94h

Vendor Specific Header

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 1400010h

Bit Range	Default and Access	Field Name (ID): Description
31:20	14h RO	**VSEC Length (VSECL):** This field indicates the number of bytes in the entire VSEC structure, including the PCI Extended Capability header, the Vendor-Specific header, and the Vendor-Specific register
19:16	0h RO	**VSEC Rev (VSECR):** This field is a vendor-defined version number that indicates the version of the VSEC structure. Software must qualify the Vendor ID and VSEC ID before interpreting this field.
15:0	10h RO	**VSECID:** This field is a vendor-defined ID number that indicates the nature and format of the VSEC structure. Software must qualify the Vendor ID before interpreting this field.

23.1.19 SW LTR Pointer Register (THC_CFG_SWLTRPTR)—Offset 98h

SWLTRPTR Pointer Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	**SW LTR Update MMIO Offset Location (SWLTRLOC):** This register contains the location pointer to the SW LTR register in MMIO space, as an offset from the specified BAR. The value of this register is a do not care, if the Valid bit is not set
3:1	0h RO	**Base Address Register Number (BARNUM):** Contains the 0s based AR Number of the BAR which contains the location of the SW LTR MMIO register. When counting BAR Numbers, all BARs, regardless of size and type, consume one BAR Number. Bar 0 is the 1st BAR. The value of this register is a do not care, if the Valid bit is not set.
0	0h RO	**Valid (VALID):** Set to 1 to indicate that the function has implemented a SW LTR register as specified in the DevIdle that can be located using the SWLTRLOC register and BARNUM. Set to 0 to indicate that the function has not implemented a SW LTR register that is compliant to the DevIdle definition. This could be because the function has not implemented SW LTR at all, or has a device specific version of SW LTR.

23.1.20 Device Idle Pointer Register (THC_CFG_DEVIDLEPTR)—Offset 9Ch

Device Idle Pointer Register

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 101h

Bit Range	Default and Access	Field Name (ID): Description
31:4	10h RW/O	**DevIdle MMIO Offset Location (DEVIDLELOC):** This register contains the location pointer to the DevIdle register in MMIO space, as an offset from the specified BAR. The value of this register is a do not care, if the Valid bit is not set.
3:1	0h RO	**Base Address Register Number (BARNUM):** Contains the 0s based BAR Number of the BAR which contains the location of the DevIdle MMIO register. When counting BAR Numbers, all BARs, regardless of size and type, consume one BAR Number. Bar 0 is the 1st BAR. The value of this register is a do not care, if the Valid bit is not set.
0	1h RW/O	**Valid (VALID):** Set to 1 to indicate that the function has implemented a DevIdle register as specified in the DevIdle that can be located using the DEVIDLELOC register and BARNUM. Set to 0 to indicate that the function has not implemented a DevIdle register that is compliant to the DevIdle definition. This could be because the function has not implemented DevIdle at all, or has a device specific version of DevIdle.

23.1.21 Device Idle Power On Latency (THC_CFG_DEVIDLEPOL)—Offset A0h

Device Idle Power On Latency

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 800h

Bit Range	Default and Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12:10	2h RW/O	**Power On Latency Scale (POLS):** Latency Scale multiplier: 010: 1us 011: 32us All other settings are reserved. The value of this register is multiplied with the Power On Latency Value (POLV) to provide the DevIdle power on exit latency multiplier scale from 1us to 32ms. This register is defined to be RWO (read-write-once) to allow BIOS to set the initial value. This register is undefined if the DevIdle.Valid bit is 0.
9:0	0h RW/O	**Power On Latency Value (POLV):** 10-bit value that is multiplied by the Power On Latency Scale. A value of 0 indicates a power on latency of less than 1us. This register is defined to be RWO (read-write-once) to allow BIOS to set the initial value. This register is undefined if the DevIdle.Valid bit is 0.

23.1.22 Power Control Enables (THC_CFG_PCE)—Offset A4h

Power Control Enables

Access Method

Type: CFG Register
(Size: 32 bits)

Device: 16
Function: 6

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:6	0h RO	Reserved.
5	0h RW/V	**Hardware Autonomous Enable (HAE):** If set, then the PGCB may request a PG whenever it is idle. This bit is loaded with the value from the PowerGateEnable soft strap when the soft strap pull is complete.
4	0h RO	Reserved.
3	1h RW/V	**Sleep Enable (SE):** : if clear, then IP will never asset Sleep to the retention flops. If set, then IP may assert Sleep during PG'ing. Note that some platforms may default this bit to 0, others to 1.
2	0h RW	**D3-Hot Enable (D3HE):** if set, then IP will PG when idle and the PMCSR[1:0] register in the IP = 11.
1	0h RW	**I3 Enable (I3E):** if set, then IP will PG when idle and the D0i3 register (D0i3C[2] = 1) is set.
0	0h RW	**Software PowerGate Enable (SPE):** Software PowerGate Enable: If this bit is set, the IP will PG when pmc_sw_pg_req_b =0. NOTE: PMCSR[1:0] must not be used for this condition. It may be any value and the IP must PG if this bit is set and it sees pmc_sw_pg_req_b asserted and IP has met its IDLE requirements for Power Gating. This is not a force power gate mechanism, rather a PMC assisted Hardware Autonomous.

23.2 THC MMIO Space Common Register Map (IOSF Primary Access) Registers Summary

Table 23-2. Summary of THC MMIO Space Common Register Map (IOSF Primary Access) Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
10h	13h	Device Idle Control Register (THC_M_CMN_DEVIDLECTRL)—Offset 10h	8h
14h	17h	THC LTR Control Register (THC_M_CMN_LTR_CTRL)—Offset 14h	C0000000h

23.2.1 Device Idle Control Register (THC_M_CMN_DEVIDLECTRL)—Offset 10h

Device Idle Control Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RO	**Interrupt Request Capable (IRC):** Set to 1 by HW if it is capable of generating an interrupt on command completion, else 0.
3	1h RW/1C/V	**RestoreRequired (RR):** When set (by HW), SW must restore state to the IP. The state may have been lost due to a reset or full power lost. SW clears the bit by writing a 1. This bit will be set on initial power up.
2	0h RW	**DevIdle (DEVIDLE):** SW sets this bit to 1 to move the function into the DevIdle state. Writing this bit to 0 will return the function to the fully active D0 state (D0i0) THC currently does not support D0i3 and writing to this register has no effect.
1	0h RO	**Interrupt Request (IR):** SW sets this bit to 1 to ask for an interrupt to be generated on completion of the command. SW must clear or set this on each write to this register.
0	0h RO/V	**Command-In-Progress (CIP):** HW sets this bit on a 1-0 or 0-1 transition of bit [2]. While set, the other bits in this register are not valid and it is unsupported for SW to write to any bit in this register. When clear all the other bits in the register are valid and SW may write to any bit. If Interrupt Request bit [1] was set for the current command, HW may clear this bit before the interrupt has been made visible to SW, since when SW actually handles a particular interrupt is not visible to the HW. SW writes to this bit have no effect. THC currently does not support D0i3 and this bit will not ever read 1'b1.

23.2.2 THC LTR Control Register (THC_M_CMN_LTR_CTRL)—Offset 14h

THC LTR Control Register

Access Method

Type: MEM Register (Size: 32 bits)

Device:

Function:

Default: C0000000h

Bit Range	Default and Access	Field Name (ID): Description
31:30	3h RO/V	**Last LTR Message Sent (LAST_LTR_SENT):** This field reflects the last LTR message that was sent by the THC hardware. 00: infinite 01: active 10: low power 11: none
29:20	0h RW	**Active Latency Value (ACT_LTR_VAL):** The agent's latency tolerance is this value multiplied by ACT_LTR_SCALE.
19:17	0h RW	**Active Latency Scale (ACT_LTR_SCALE):** Specifies the scale for the value reported in the ACT_LTR_VAL field. Encodings: 000 - Value times 1 ns 001 - Value times 32 ns 010 - Value times 1,024 ns 011 - Value times 32,768 ns 100 - Value times 1,048,576 ns 101 - Value times 33,554,432 ns 110-111 - Not Permitted
16:7	0h RW	**Low Power Latency Value (LP_LTR_VAL):** The agent's latency tolerance is this value multiplied by LP_LTR_SCALE.

Bit Range	Default and Access	Field Name (ID): Description
6:4	0h RW	**Low Power Latency Scale (LP_LTR_SCALE):** Specifies the scale for the value reported in the LP_LTR_VAL field. Encodings: 000 - Value times 1 ns 001 - Value times 32 ns 010 - Value times 1,024 ns 011 - Value times 32,768 ns 100 - Value times 1,048,576 ns 101 - Value times 33,554,432 ns 110-111 - Not Permitted
3	0h RW	**Enable sending Low power LTR to PMC. (LP_LTR_EN):** If this bit is written to 1 then the THC will send a low power LTR message with value of LP_LTR_VAL multiplied by LP_LTR_SCALE if LP_LTR_REQ is 1, else will send an infinite LTR message. If this bit is written to 0 then the THC does not send low power LTR message. This is normally used by software to send LTR when it moves the THC devices to low power state like ARMed, Doze or Sleep. If multiple THC devices are supported, it's software responsibility to aggregate the latency across all the devices before setting this bit. Software must not set this bit simultaneously with ACTIVE_LTR_EN. Writing 1 to this field has no effect if the RXDMA start bit is 0. Software should enable the RXDMA before writing 1 to this bit.
2	0h RW	**Low Power LTR Requirement (LP_LTR_REQ):** If this bit is set to 1 then the agent's low power latency tolerance is LP_LTR_VAL multiplied by LP_LTR_SCALE. If this bit is 0 then the agent has no low power latency requirement (i.e. infinite latency).
1	0h RW	**Enable sending Active LTR to PMC (ACTIVE_LTR_EN):** If this bit is written to 1 then the THC will send a Active LTR message with value of ACT_LTR_VAL multiplied by ACT_LTR_SCALE if ACTIVE_LTR_REQ is 1, else will send an infinite LTR message. If this bit is written to 0 then the THC does not send Active LTR message. Software normally does not use this bit to send active LTR. THC will send active LTR in HW. Software must not set this bit simultaneously with LP_LTR_EN. Writing 1 to this field has no effect if the RXDMA start bit is 0. Software should enable the RXDMA before writing 1 to this bit.
0	0h RW	**Active LTR Requirement (ACTIVE_LTR_REQ):** If this bit is set to 1 then the agent's latency tolerance is ACT_LTR_VAL multiplied by ACT_LTR_SCALE. If this bit is 0 then the agent has no active latency requirement (i.e. infinite latency).

23.3 THC MMIO Space Port 0 Register Map Registers Summary

Table 9. Summary of THC MMIO Space Port 0 Register Map Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1008h	100Bh	Touch Host Controller Control Register (THC_M_PRT_CONTROL)—Offset 1008h	10000006h
1010h	1013h	THC SPI Bus Configuration Register (THC_M_PRT_SPI_CFG)—Offset 1010h	4700273h
1020h	1023h	THC Interrupt Enable Register (THC_M_PRT_INT_EN)—Offset 1020h	20003604h
1024h	1027h	THC Interrupt Status Register (THC_M_PRT_INT_STATUS)—Offset 1024h	0h
1028h	102Bh	THC Error Cause Register (THC_M_PRT_ERR_CAUSE)—Offset 1028h	0h
1040h	1043h	THC SW sequencing Control (THC_M_PRT_SW_SEQ_CNTRL)—Offset 1040h	0h
1044h	1047h	THC SW sequencing Status (THC_M_PRT_SW_SEQ_STS)—Offset 1044h	0h
1048h	104Bh	THC SW Sequencing Data DW0 or SPI Address Register (THC_M_PRT_SW_SEQ_DATA0_ADDR)—Offset 1048h	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
104Ch	104Fh	THC SW sequencing Data DW1 (THC_M_PRT_SW_SEQ_DATA1)—Offset 104Ch	0h
1050h	1053h	THC SW sequencing Data DW2 (THC_M_PRT_SW_SEQ_DATA2)—Offset 1050h	0h
1054h	1057h	THC SW sequencing Data DW3 (THC_M_PRT_SW_SEQ_DATA3)—Offset 1054h	0h
1058h	105Bh	THC SW sequencing Data DW4 (THC_M_PRT_SW_SEQ_DATA4)—Offset 1058h	0h
105Ch	105Fh	THC SW sequencing Data DW5 (THC_M_PRT_SW_SEQ_DATA5)—Offset 105Ch	0h
1060h	1063h	THC SW sequencing Data DW6 (THC_M_PRT_SW_SEQ_DATA6)—Offset 1060h	0h
1064h	1067h	THC SW sequencing Data DW7 (THC_M_PRT_SW_SEQ_DATA7)—Offset 1064h	0h
1068h	106Bh	THC SW sequencing Data DW8 (THC_M_PRT_SW_SEQ_DATA8)—Offset 1068h	0h
106Ch	106Fh	THC SW sequencing Data DW9 (THC_M_PRT_SW_SEQ_DATA9)—Offset 106Ch	0h
1070h	1073h	THC SW sequencing Data DW10 (THC_M_PRT_SW_SEQ_DATA10)—Offset 1070h	0h
1074h	1077h	THC SW sequencing Data DW11 (THC_M_PRT_SW_SEQ_DATA11)—Offset 1074h	0h
1078h	107Bh	THC SW sequencing Data DW12 (THC_M_PRT_SW_SEQ_DATA12)—Offset 1078h	0h
107Ch	107Fh	THC SW sequencing Data DW13 (THC_M_PRT_SW_SEQ_DATA13)—Offset 107Ch	0h
1080h	1083h	THC SW sequencing Data DW14 (THC_M_PRT_SW_SEQ_DATA14)—Offset 1080h	0h
1084h	1087h	THC SW sequencing Data DW15 (THC_M_PRT_SW_SEQ_DATA15)—Offset 1084h	0h
1088h	108Bh	THC SW sequencing Data DW16 (THC_M_PRT_SW_SEQ_DATA16)—Offset 1088h	0h
1090h	1093h	THC Write PRD Base Address Register Low (THC_M_PRT_WPRD_BA_LOW)—Offset 1090h	0h
1094h	1097h	THC Write PRD Base Address Register High (THC_M_PRT_WPRD_BA_HI)—Offset 1094h	0h
1098h	109Bh	THC Write DMA Control (THC_M_PRT_WRITE_DMA_CNTRL)—Offset 1098h	800000h
109Ch	109Fh	THC Write Interrupt Status (THC_M_PRT_WRITE_INT_STS)—Offset 109Ch	0h
10B4h	10B7h	THC device address for the bulk write (THC_M_PRT_WR_BULK_ADDR)—Offset 10B4h	1000h
10B8h	10BBh	THC Device Interrupt Cause Register Address (THC_M_PRT_DEV_INT_CAUSE_ADDR)—Offset 10B8h	0h
10BCh	10BFh	THC Device Interrupt Cause Register Value (THC_M_PRT_DEV_INT_CAUSE_REG_VAL)—Offset 10BCh	0h
10E0h	10E3h	THC TXDMA Frame Count (THC_M_PRT_TX_FRM_CNT)—Offset 10E0h	0h
10E4h	10E7h	THC TXDMA Packet Count (THC_M_PRT_TXDMA_PKT_CNT)—Offset 10E4h	0h
10E8h	10EBh	THC Device Interrupt Count on this port (THC_M_PRT_DEVINT_CNT)—Offset 10E8h	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1100h	1103h	THC Read PRD Base Address Low for the 1st RXDMA (THC_M_PRT_RPRD_BA_LOW_1)—Offset 1100h	0h
1104h	1107h	THC Read PRD Base Address High for the 1st RXDMA (THC_M_PRT_RPRD_BA_HI_1)—Offset 1104h	0h
1108h	110Bh	THC Read PRD Control for the 1st RXDMA (THC_M_PRT_RPRD_CNTRL_1)—Offset 1108h	0h
110Ch	110Fh	THC Read DMA Control for the 1st RXDMA (THC_M_PRT_READ_DMA_CNTRL_1)—Offset 110Ch	40000000h
1110h	1113h	THC Read Interrupt Status for the 1st RXDMA (THC_M_PRT_READ_DMA_INT_STS_1)—Offset 1110h	0h
1114h	1117h	THC Read DMA Error Register for the 1st RXDMA (THC_M_PRT_READ_DMA_ERR_1)—Offset 1114h	0h
1118h	111Bh	Touch Sequencer GuC Tail Offset Address Low for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_LOW_1)—Offset 1118h	0h
111Ch	111Fh	Touch Sequencer GuC Tail Offset Address High for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_HI_1)—Offset 111Ch	0h
1120h	1123h	Touch Host Controller GuC Work Queue Item Size for the 1st RXDMA (THC_M_PRT_GUC_WORKQ_ITEM_SZ_1)—Offset 1120h	0h
1124h	1127h	Touch Host Controller GuC Control register for the 1st RXDMA (THC_M_PRT_GUC_WORKQ_SZ_1)—Offset 1124h	0h
1128h	112Bh	Touch Sequencer Control for the 1st DMA (THC_M_PRT_TSEQ_CNTRL_1)—Offset 1128h	0h
1130h	1133h	Touch Sequencer GuC Doorbell Address Low for the 1st RXDMA (THC_M_PRT_GUC_DB_ADDR_LOW_1)—Offset 1130h	0h
1134h	1137h	Touch Sequencer GuC Doorbell Address High for the 1st RXDMA (THC_M_PRT_GUC_DB_ADDR_HI_1)—Offset 1134h	0h
1138h	113Bh	Touch Sequencer GuC Doorbell Data (THC_M_PRT_GUC_DB_DATA_1)—Offset 1138h	1h
1140h	1143h	Touch Sequencer GuC Tail Offset Initial Value for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_INITVAL_1)—Offset 1140h	0h
1170h	1173h	THC Device Address for the bulk/touch data read for the 1st RXDMA (THC_M_PRT_RD_BULK_ADDR_1)—Offset 1170h	1000h
11A0h	11A3h	THC Gfx/SW Doorbell Count from the 1st Stream RXDMA on this port (THC_M_PRT_DB_CNT_1)—Offset 11A0h	0h
11A4h	11A7h	THC Frame Count from the 1st Stream RXDMA on this port (THC_M_PRT_FRM_CNT_1)—Offset 11A4h	0h
11A8h	11ABh	THC Micro Frame Count from the 1st Stream RXDMA on this port (THC_M_PRT_UFRM_CNT_1)—Offset 11A8h	0h
11ACh	11AFh	THC Packet Count from the 1st Stream RXDMA on this port (THC_M_PRT_RXDMA_PKT_CNT_1)—Offset 11ACh	0h
11B0h	11B3h	THC Software Interrupt Count from the 1st Stream RXDMA on this port (THC_M_PRT_SWINT_CNT_1)—Offset 11B0h	0h
11B4h	11B7h	Touch Sequencer Frame Drop Counter for the 1st RXDMA (THC_M_PRT_FRAME_DROP_CNT_1)—Offset 11B4h	0h
1200h	1203h	THC Read PRD Base Address Low for the 2nd RXDMA (THC_M_PRT_RPRD_BA_LOW_2)—Offset 1200h	0h
1204h	1207h	THC Read PRD Base Address High for the 2nd RXDMA (THC_M_PRT_RPRD_BA_HI_2)—Offset 1204h	0h
1208h	120Bh	THC Read PRD Control for the 2nd RXDMA (THC_M_PRT_RPRD_CNTRL_2)—Offset 1208h	0h
120Ch	120Fh	THC Read DMA Control for the 2nd RXDMA (THC_M_PRT_READ_DMA_CNTRL_2)—Offset 120Ch	40000000h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1210h	1213h	THC Read Interrupt Status for the 2nd RXDMA (THC_M_PRT_READ_DMA_INT_STS_2)—Offset 1210h	0h
1214h	1217h	THC Read DMA Error Register for the 2nd RXDMA (THC_M_PRT_READ_DMA_ERR_2)—Offset 1214h	0h
1218h	121Bh	Touch Sequencer GuC Tail Offset Address Low for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_LOW_2)—Offset 1218h	0h
121Ch	121Fh	Touch Sequencer GuC Tail Offset Address High for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_HI_2)—Offset 121Ch	0h
1220h	1223h	Touch Host Controller GuC Work Queue Item Size for the 2nd RXDMA (THC_M_PRT_GUC_WORKQ_ITEM_SZ_2)—Offset 1220h	0h
1224h	1227h	Touch Host Controller GuC Control register for the 2nd RXDMA (THC_M_PRT_GUC_WORKQ_SZ_2)—Offset 1224h	0h
1228h	122Bh	Touch Sequencer Control for the 2nd DMA (THC_M_PRT_TSEQ_CNTRL_2)—Offset 1228h	0h
1230h	1233h	Touch Sequencer GuC Doorbell Address Low for the 2nd RXDMA (THC_M_PRT_GUC_DB_ADDR_LOW_2)—Offset 1230h	0h
1234h	1237h	Touch Sequencer GuC Doorbell Address High for the 2nd RXDMA (THC_M_PRT_GUC_DB_ADDR_HI_2)—Offset 1234h	0h
1238h	123Bh	Touch Sequencer GuC Doorbell Data for PRD2 (THC_M_PRT_GUC_DB_DATA_2)—Offset 1238h	1h
1240h	1243h	Touch Sequencer GuC Tail Offset Initial Value for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_INITVAL_2)—Offset 1240h	0h
1270h	1273h	THC Device Address for the bulk/touch data read for the 2nd RXDMA (THC_M_PRT_RD_BULK_ADDR_2)—Offset 1270h	1000h
12A0h	12A3h	THC Gfx/SW Doorbell Count from the 2nd Stream RXDMA on this port (THC_M_PRT_DB_CNT_2)—Offset 12A0h	0h
12A4h	12A7h	THC Frame Count from the 2nd Stream RXDMA on this port (THC_M_PRT_FRM_CNT_2)—Offset 12A4h	0h
12A8h	12ABh	THC Micro Frame Count from the 2nd Stream RXDMA on this port (THC_M_PRT_UFRM_CNT_2)—Offset 12A8h	0h
12ACh	12AFh	THC Packet Count from the 2nd Stream RXDMA on this port (THC_M_PRT_RXDMA_PKT_CNT_2)—Offset 12ACh	0h
12B0h	12B3h	THC Software Interrupt Count from the 2nd Stream RXDMA on this port (THC_M_PRT_SWINT_CNT_2)—Offset 12B0h	0h
12B4h	12B7h	Touch Sequencer Frame Drop Counter for the 2nd RXDMA (THC_M_PRT_FRAME_DROP_CNT_2)—Offset 12B4h	0h

23.3.1 Touch Host Controller Control Register (THC_M_PRT_CONTROL)—Offset 1008h

THC Control Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 10000006h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Port type for this port instance (PORT_TYPE):** 00: SPI port 01: thc port Others: reserved
29	0h RO/V	**Indication of SPI IO (SPI_IO_RDY):** 0: This SPI port IO is not ready for operation 1: This SPI port IO is ready for operation This bit is used by driver to decide whether the SPI port is ready to use, including rcomp done completion etc. SW needs to wait this bit to be 1 once on D0 entry (boot or D3 exit) before running any PIO/DMA cycles on SPI bus.
28	1h RW/L	**Whether this port is supported or not (PORT_SUPPORTED):** 0: This port is not supported 1: This port is supported This bit is used by driver to decide whether this port is supported or not. In the per port driver model, ii. BIOS will set the PORT_SUPPORTED bit to 1 only for the first port under each controller. Driver will not operate the other ports where the PORT_SUPPORTED bit is 0. In the multi-port shared driver model, BIOS may set this bit to 1 for multiple ports under the 1st THC. It will function disable the other THC. This bit is locked by THC_BIOS_LOCK_EN. For security reason, BIOS shall lock them after it completes the programming, before host software/OS is brought up.
27	0h RW/L	**Lock bit for several BIOS registers (THC_BIOS_LOCK_EN):** 0: The registers listed below are not locked 1: The registers listed below are locked. The registers locked by this bit includes: THC_M_PRT_GUC_VDM* For security reason, BIOS shall lock them after it completes the programming, before host software/OS is brought up.
26:23	0h RO	Reserved.
22:20	0h RO/V	**Port index under this THC (PORT_INDEX):** This field indicates the 0-based port index of this port in the THC.
19	0h RO	Reserved.
18:16	0h RO/V	**THC Instance index of this THC (THC_INSTANCE_INDEX):** This field indicates the 0-based instance index of this THC.
15:14	0h RO	Reserved.
13	0h RW/L	**THC Locking bit to lock driver registers (THC_DRV_LOCK_EN):** When set to 1 , prevents INT_SW_DMA_EN, INT_SW_DMA_EN2 from being changed. This bit can only be written from 0 to 1 once. Once set to 1, this bit can only be cleared by a hardware reset.
12:4	0h RO	Reserved.
3	0h RW	**Device GPIO Reset (DEVRST):** 1: Deassert Device reset/power on through GPIO. 0: Assert Device reset/power off through GPIO.
2	1h RO/V	**Hardware Status for Quiesce Status bit (THC_DEVINT_QUIESCE_HW_STS):** HW will set this bit once RX sequencer is IDLE, after completing processing of any microframe that started before the THC_DEVINT_QUIESCE_EN. SW cannot clear THC_DEVINT_QUIESCE_EN until it sees this bit set
1	1h RW	**Quiesce bit for the device interrupt (THC_DEVINT_QUIESCE_EN):** When this bit is set, THC shall complete servicing the current touch microframe or current device interrupt, and ignore the TIC's interrupt (including touch and non-touch interrupt) until the bit is cleared by SW. When SW writes 1 to this bit, THC is expected to complete processing the current microframe and then set THC_DEVINT_QUIESCE_HW_STS. THC shall not drop any outstanding interrupt asserted when THC_DEVINT_QUIESCE_EN is set. SW shall poll THC_DEVINT_QUIESCE_HW_STS to be 1 before it can clear THC_DEVINT_QUIESCE_EN. After the bit is cleared by SW, THC shall start service device interrupt as usual. This bit does not impact the activities on TXDMA and PIO operations.
0	0h RO	Reserved.

23.3.2 THC SPI Bus Configuration Register (THC_M_PRT_SPI_CFG)—Offset 1010h

THC SPI Port Configuration Register
Note: The THC_M_PRT_SPI_CFG register can't be written/updated when TX/RX DMAs is running or PIO is running cycles on the bus.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 4700273h

Bit Range	Default & Access	Field Name (ID): Description
31:24	4h RO	**SPI WRITE Max Packet Size (SPI_WR_MPS):** SPI Write Max Packet Size in 16 bytes. Software shall program this register after it negotiates with the device. This has to be programmed before it issues any other cycles to the device including the configuration, TX DMA and RX DMA.
23	0h RW	**Enable SPI Clock Divide by 8 to support low freq device. (SPI_LOW_FREQ_EN):** 1: All the SPI read/write clock frequency (defined in SPI_TCWF/SPI_TCRF) will be divided further by 8 0: No further divider is supported.
22:20	7h RW	**SPI Touch Cycle Write Frequency (SPI_TCWF):** The listed frequencies are approximate. 100 : 30MHz divide by 4 101 : 24MHz, divide by 5 110 : 20MHz, divide by 6 111 : 17MHz, divide by 7 Others: Reserved
19:18	0h RW	**SPI Touch IO Write mode (SPI_TWMODE):** Firmware programs this mode after discovering capabilities of Touch device.
17:16	0h RO	Reserved.
15:7	4h RO	**SPI READ Max Packet Size (SPI_RD_MPS):** SPI Read Max Packet Size in 16 bytes. Software shall program this register after it negotiates with the device. This has to be programmed before it issues any other cycles to the device including the configuration, TX DMA and RX DMA.
6:4	7h RW	**SPI Touch Cycle Read Frequency (SPI_TCRF):** The listed frequencies are approximate. 100 : 30MHz divide by 4 101 : 24MHz, divide by 5 110 : 20MHz, divide by 6 111 : 17MHz, divide by 7 Others: Reserved
3:2	0h RW	**SPI Touch IO Read mode (SPI_TRMODE):** Firmware programs this mode after discovering capabilities of Touch device. 00 : Single IO Read (1-1-1 0B) enabled 01: Dual IO Read (1-2-2 BBh) enabled (DIORE) 10: Quad IO Read (1-4-4/EBh) mode (QIORE) 11: Quad Parrellel IO Read (4-4-4/FBh) mode (QPIRE) enabled.
1:0	3h RW	**SPI Touch IO Read Dummy Clocks (SPI_TRDC):** Firmware programs this mode after discovering capabilities of Touch device.

23.3.3 THC Interrupt Enable Register (THC_M_PRT_INT_EN)—Offset 1020h

THC Port Interrupt Enable Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 20003604h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29	1h RW	**Enable THC Transaction Error Reporting with Interrupt (TXN_ERR_INT_EN):** b0: Disable THC Transaction Error Reporting Interrupt b1: Enable HCI Transaction Error Reporting Interrupt Note:The Interrupt enable is also qualified by the MSIE or Line Interrupt Enable. When all these enables are set and when THC_TXN_ERR_INT_STS is set, an interrupt will be sent to SW.
28:24	0h RO	Reserved.
23:16	0h RW	**Enable THC Fatal Error Reporting with Interrupt (FATAL_ERR_INT_EN):** b0: Disable THC Fatal Error Reporting Interrupt b1: Enable THC Fatal Error Reporting Interrupt Note:The Interrupt enable is also qualified by the MSIE or Line Interrupt Enable. When all these enables are set and when THC_FATAL_ERR_INT_STS is set, an interrupt will be sent to SW.
15:14	0h RO	Reserved.
13	1h RW	**Enable PRD Entry Error Reporting with Interrupt (PRD_ENTRY_ERR_INT_EN)**
12	1h RW	**Enable THC Buffer Overrun Error Reporting with Interrupt (BUF_OVRRUN_ERR_INT_EN)**
11	0h RO	Reserved.
10	1h RW	**Enable Frame Babble Error Reporting with Interrupt (FRAME_BABBLE_ERR_INT_EN)**
9	1h RW	**Enable Invalid Device Register Error Reporting with Interrupt (INVLD_DEV_ENTRY_INT_EN)**
8:4	0h RO	Reserved.
3	0h RW	**Stop on Frame Babble (SOFB):** When set, HW will clear the Start bit, upon detection of a frame babble, and stop read DMA operations.
2	1h RW	**Stop on Invalid Device Register (SIDR):** When set, HW will clear the Start bit, upon detection of a invalid device register, and stop read DMA operations.
1	0h RW	**Stop on THC buffer overrun (SBO):** When set, HW will clear the Start bit, upon detection of a buffer overrun, and stop read DMA operations.
0	0h RW	**Stop on Invalid PRD entry (SIPE):** When set, HW will clear the Start bit, upon detection of an invalid PRD entry, and stop read DMA operations.

23.3.4 THC Interrupt Status Register (THC_M_PRT_INT_STATUS)—Offset 1024h

THC Port Interrupt Status Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	Reserved.
30	0h RW/1C/V	**Interrupt Status of THC fatal error (FATAL_ERR_INT_STS):** Interrupt status when a THC fatal error occurs. If the THC_Fatal_Err_Intr_En bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit. 1 - A THC Fatal error occured. The error cause is captured in the FATAL_ERR_CAUSE register. 0 - No Connection status change.
29	0h RO	Reserved.
28	0h RW/1C/V	**Interrupt Status of THC transaction error (TXN_ERR_INT_STS):** Interrupt status when a THC transaction error occurs. If the THC_TXN_Err_Intr_En bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit. 1 - A THC transaction error occured. The error cause is captured in the TXN_ERR_CAUSE register. 0 - No Connection status change.
27:0	0h RO	Reserved.

23.3.5 THC Error Cause Register (THC_M_PRT_ERR_CAUSE)—Offset 1028h

THC Port Interrupt Status Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	0h RO/V	**THC Fatal Error Cause (FATAL_ERR_CAUSE):** There is no fatal error cause in SPI mode.
15:14	0h RO	Reserved.
13	0h RW/1C/V	**THC Transaction Error Cause - Invalid PRD Entry (PRD_ENTRY_ERR):** This error condition occurs when the THC detects an invalid PRD entry. A PRD entry is invalid when its length is 0.
12	0h RW/1C/V	**THC Transaction Error Cause - THC Buffer Overrun (BUF_OVRRUN_ERR):** This error condition occurs when the THC can't keep up with the incoming touch data due to IOSF or other internal bottleneck, and cause internal buffer overflow.
11	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/1C/V	**THC Transaction Error Cause - Frame Babble (FRAME_BABBLE_ERR):** This error condition occurs when the THC receives larger size of the touch data than the PRD table size for the current frame. This condition is detected when the micro-frame size is read from device register and the value exceeds the remaining buffer space for the current frame.
9	0h RW/1C/V	**THC Transaction Error Cause - Invalid Device Register Setting (INVLD_DEV_ENTRY):** This error condition occurs when the THC detects invalid settings in the touch device's register INT_CAUSE. The touch device's register settings are defined in Intel Precise Touch & Stylus Gen2. The device register setting is invalid if the microframe size field is 0.
8:0	0h RO	Reserved.

23.3.6 THC SW sequencing Control (THC_M_PRT_SW_SEQ_CNTRL)—Offset 1040h

THC SW sequencing Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/L	**THC SW Sequencing Bus Byte Count (THC_SS_BC):** This field specifies the SPI read/write byte count to send out during the SW sequencing cycle. For SPI, this is a 1-based byte count for read or write. i.e. value 1 is for 1 byte and 2 is for 2 bytes. Valid values are in the range of 1-64. Any other value will result in THC_SS_ERR being set.
15:8	0h RW/L	**THC SW Sequencing Bus Command (THC_SS_CMD):** In SPI port, the register read and touch data read commands are mapped to SPI read cycles. The register write and bulk write commands are mapped to SPI write cycles. The other commands are not used in SPI mode.
7:2	0h RO	Reserved.
1	0h RW/L	**THC SW Sequencing Cycle Done Interrupt Enable (THC_SS_CD_IE):** When set to 1, the THC asserts an interrupt request whenever the Touch Cycle Done bit is 1.
0	0h RW/1S/V/L	**THC SW Sequence Cycle Go (TSSGO):** A write to this register with THC Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the THC arbiter to run the cycle on the THC bus. When the cycle is complete, the TSSDONE bit is set. Software is forbidden to write to any register in the THC_SS_SEQ_CNTRL/DATA register between the TSSGO bit getting set and the TSSDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit remains set until the transaction is granted by the THC Controller's internal arbiter.

23.3.7 THC SW sequencing Status (THC_M_PRT_SW_SEQ_STS)—Offset 1044h

THC SW sequencing Status

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	0h RO/V	**THC SW Sequencing Cycle In Progress (THC_SS_CIP):** Hardware sets this bit when software sets the THC Cycle Go (TSSGO) bit. This bit remains set until the cycle completes on the bus interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.
2	0h RO	Reserved.
1	0h RW/1C/V	**THC SW Sequencing Error (THC_SS_ERR):** Hardware sets this bit to 1 when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or until a partition reset occurs. Software must clear this bit before setting the THC Cycle GO bit in this register.
0	0h RW/1C/V	**THC SW Sequence Cycle Done (TSSDONE):** The THC sets this bit to 1 when the SW Touch Cycle completes after software previously set the TSSGO bit. This bit remains asserted until cleared by software writing a 1 or host partition reset. When this bit is set and the THC_SS_CD_IE MSI Enable bit is set the THC controller sends MSI. Software must make sure this bit is cleared prior to enabling the TDONE MSI assertion for a new programmed access.

23.3.8 THC SW Sequencing Data DW0 or SPI Address Register (THC_M_PRT_SW_SEQ_DATA0_ADDR)—Offset 1048h

THC SW sequencing Data DW0/Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**THC SW sequencing Data/Address (THC_SW_SEQ_DATA0_ADDR):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc. In SPI mode, this DW are programmed with byte address field. The upper address bits [31:24] will be ignored by THC on the SPI bus.

23.3.9 THC SW sequencing Data DW1 (THC_M_PRT_SW_SEQ_DATA1)—Offset 104Ch

THC SW sequencing Data DW1

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data 1 (THC_SW_SEQ_DATA1):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

23.3.10 THC SW sequencing Data DW2 (THC_M_PRT_SW_SEQ_DATA2)—Offset 1050h

THC SW sequencing Data DW2

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW2 (THC_SW_SEQ_DATA2):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

23.3.11 THC SW sequencing Data DW3 (THC_M_PRT_SW_SEQ_DATA3)—Offset 1054h

THC SW sequencing Data DW3

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW3 (THC_SW_SEQ_DATA3):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

23.3.12 THC SW sequencing Data DW4 (THC_M_PRT_SW_SEQ_DATA4)—Offset 1058h

THC SW sequencing Data DW4

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW4 (THC_SW_SEQ_DATA4):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

23.3.13 THC SW sequencing Data DW5 (THC_M_PRT_SW_SEQ_DATA5)—Offset 105Ch

THC SW sequencing Data DW5

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW5 (THC_SW_SEQ_DATA5):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

23.3.14 THC SW sequencing Data DW6 (THC_M_PRT_SW_SEQ_DATA6)—Offset 1060h

THC SW sequencing Data DW6

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW Sequencing Data DW6 (THC_SW_SEQ_DATA6):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

23.3.15 THC SW sequencing Data DW7 (THC_M_PRT_SW_SEQ_DATA7)—Offset 1064h

THC SW sequencing Data DW7

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data 7 (THC_SW_SEQ_DATA7):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

23.3.16 THC SW sequencing Data DW8 (THC_M_PRT_SW_SEQ_DATA8)—Offset 1068h

THC SW sequencing Data DW8

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW8 (THC_SW_SEQ_DATA8):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

23.3.17 THC SW sequencing Data DW9 (THC_M_PRT_SW_SEQ_DATA9)—Offset 106Ch

THC SW sequencing Data DW9

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW9 (THC_SW_SEQ_DATA9):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

23.3.18 THC SW sequencing Data DW10 (THC_M_PRT_SW_SEQ_DATA10)—Offset 1070h

THC SW sequencing Data DW10

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data 10 (THC_SW_SEQ_DATA10):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

23.3.19 THC SW sequencing Data DW11 (THC_M_PRT_SW_SEQ_DATA11)—Offset 1074h

THC SW sequencing Data DW11

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW11 (THC_SW_SEQ_DATA11):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

23.3.20 THC SW sequencing Data DW12 (THC_M_PRT_SW_SEQ_DATA12)—Offset 1078h

THC SW sequencing Data DW12

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW12 (THC_SW_SEQ_DATA12):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

23.3.21 THC SW sequencing Data DW13 (THC_M_PRT_SW_SEQ_DATA13)—Offset 107Ch

THC SW sequencing Data DW13

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW13 (THC_SW_SEQ_DATA13):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

23.3.22 THC SW sequencing Data DW14 (THC_M_PRT_SW_SEQ_DATA14)—Offset 1080h

THC SW sequencing Data DW14

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW14 (THC_SW_SEQ_DATA14):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

23.3.23 THC SW sequencing Data DW15 (THC_M_PRT_SW_SEQ_DATA15)—Offset 1084h

THC SW sequencing Data DW15

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW15 (THC_SW_SEQ_DATA15):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

23.3.24 THC SW sequencing Data DW16 (THC_M_PRT_SW_SEQ_DATA16)—Offset 1088h

THC SW sequencing Data DW16

Access Method

Type: MEM Register (Size: 32 bits)
Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**THC SW sequencing Data DW16 (THC_SW_SEQ_DATA16):** This field is shifted in/out as the THC Data during the data portion of the THC cycle. The data is always shifted starting with the least significant byte, followed by the next least significant byte, etc.

23.3.25 THC Write PRD Base Address Register Low (THC_M_PRT_WPRD_BA_LOW)—Offset 1090h

THC Write PRD Base Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**THC Write PRD Base Address (THC_M_PRT_WPRD_BA_LOW):** This register initializes the lower 32 bits of the 64 bit write PRD table base address, 4K aligned, thus 20bits are allocated.
11:0	0h RO	Reserved.

23.3.26 THC Write PRD Base Address Register High (THC_M_PRT_WPRD_BA_HI)—Offset 1094h

THC Write PRD Base Address Register Hi

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**THC Write PRD Base Address Register Hi (THC_M_PRT_WPRD_BA_HI):** This register initializes the upper 32 bits of the 64 bit write PRD table base address.

23.3.27 THC Write DMA Control (THC_M_PRT_WRITE_DMA_CNTRL)—Offset 1098h

THC Write DMA Control

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 800000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW	**PRD Table Entry Count for WRDMA (THC_WRDMA_PTEC):** The number of PRD entries in the write PRD tables. 00h: 1 PRD entry for the write PRD Table 01h: 2 PRD entries for the write PRD Table :: FFh: 256 PRD entries for each PRD Table
23	1h RO	**Update HW Status for WRDMA (THC_WRDMA_UHS):** If set, the HwStatus field of each PRD entry (for each PRD table) bit is updated (successful or error).
22:4	0h RO	Reserved.
3	0h RW	**Interrupt Enable on WRDMA Completion (THC_WRDMA_IE_IOC_DMACPL):** When set, interrupt is generated upon completion of the Write DMA PRD table.
2	0h RW	**Interrupt Enable on IOC for WRDMA (THC_WRDMA_IE_IOC):** When set, interrupt is generated upon completion of the PRD block transfer, with IOC=1, or when an error is encountered with the Error=1 in the THC_WRITE_DMA_INT_STS register.
1	0h RW	**Interrupt Enable on Error for WRDMA (THC_WRDMA_IE_IOC_ERROR):** When set, interrupt is generated when an error is encountered with the Write DMA Error=1.
0	0h RW/V	**Start WRDMA (THC_WRDMA_START):** SW sets the Start bit to arm the Write DMA engine. HW clears the bit after the DMA completion as indicated by interrupt and/or Status bits. SW can also clear the Start bit to abort an on-going DMA operation. In this case, HW completes all the outstanding requests to system memory and then stops the PRD actions at a safe point. SW shall poll this bit after it writes 0 to the start bit until HW completes the stop and clears the bit.

23.3.28 THC Write Interrupt Status (THC_M_PRT_WRITE_INT_STS)—Offset 109Ch

THC Write Interrupt Status

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	0h RO/V	**Active status for Write DMA (THC_WRDMA_ACTIVE):** Write DMA is active. Set by HW when the Write DMA Start bit is set by SW and auto-cleared by HW in the following conditions: - The entire Write DMA operation has been completed successfully or - The Write DMA operation has been halted by software clearing the Write DMA Start bit (and no read completion pending).

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C/V	**Interrupt Status for IOC for Write DMA (THC_WRDMA_IOC_STS):** A PRD entry with IOC bit set has been completed during WRDMA operation. If the THC_WRDMA_IE_IOC bit is also 1, then an interrupt is generated. In polling mode, when THC_WRDMA_IE_IOC=0, SW clears the bit by writing 1 to the bit.
1	0h RW/1C/V	**Write DMA Error Status (THC_WRDMA_ERROR_STS):** Error encountered during write DMA operation. If the THC_WRDMA_IE_ERROR bit is also 1, then an interrupt is generated. In polling mode, when THC_WRDMA_IE_ERROR=0, SW clears the bit by writing 1 to the bit. Note: For SPI bus, there is no known error condition for this bit.
0	0h RW/1C/V	**Write DMA Completion Status bit (THC_WRDMA_CMPL_STATUS):** This bit is set upon successful completion of the Write DMA operation or by the rising edge of the Error bit. If the THC_WRDMA_IE_IOC_DMACPL bit is also 1, then an interrupt is generated. In polling mode, when THC_WRDMA_IE_IOC_DMACPL=0, SW clears the bit by writing 1 to the bit.

23.3.29 THC device address for the bulk write (THC_M_PRT_WR_BULK_ADDR)—Offset 10B4h

THC device address for the bulk write

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	1000h RW/O	**THC device address for the bulk write (THC_M_PRT_WR_BULK_ADDR):** THC Device Address for the bulk data write. The bulk write cycles addresses start from the bulk address defined in THC_M_PRT_WR_BULK_ADDR (default 0x1000) and increment on every packet until the end of the write frame. The bulk write address resumes using the address in THC_M_PRT_WR_BULK_ADDR at the beginning of every write frame. SW is responsible to program this register correctly, and make sure all resulting touch cycles will not exceed the touch device's bulk address space or roll over. Otherwise, THC's behavior is undefined. Note: For SPI devices, only 24bit addressing space is supported. Default to 0x1000.

23.3.30 THC Device Interrupt Cause Register Address (THC_M_PRT_DEV_INT_CAUSE_ADDR)—Offset 10B8h

THC Device Interrupt Cause Register Address

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/O	**THC Device Interrupt Cause Register Address (THC_M_PRT_DEV_INT_CAUSE_ADDR):** THC Device Interrupt Cause Register Address. This register defines the Device Interrupt Cause Register Address for RXDMA and SW operation. SW is responsible to program this register correctly based on the device register offset, and make sure all resulting touch cycles will not cause malfunction of the touch device. Otherwise, THC's behavior is undefined. Note: For SPI devices, only 24bit addressing space is supported. Default to 0x0.

23.3.31 THC Device Interrupt Cause Register Value (THC_M_PRT_DEV_INT_CAUSE_REG_VAL)—Offset 10BCh

THC Device Interrupt Cause Register Value

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**THC Device Interrupt Cause Register Value (THC_M_PRT_DEV_INT_CAUSE_REG_VAL):** THC Device Interrupt Cause Register Value. This register reflects the latest values of the Device Interrupt Cause Register when it read by the RXDMA sequencer.

23.3.32 THC TXDMA Frame Count (THC_M_PRT_TX_FRM_CNT)—Offset 10E0h

Touch TX Frame Counter

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch TX Frame Counter Reset (THC_M_PRT_TX_FRM_CNT_RST):** Reset the THC_M_PRT_TX_FRM_CNT counter. SW writing this bit to a 0x1, resets the THC_M_PRT_TX_FRM_CNT counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch TX Frame Counter (THC_M_PRT_TX_FRM_CNT):** Number of Touch Frames sent from this port. The counter shall roll over back to 0 after reaching the maximum value.

23.3.33 THC TXDMA Packet Count (THC_M_PRT_TXDMA_PKT_CNT)—Offset 10E4h

Touch TX DMA Packet Counter

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch TX DMA Packet Counter Reset (THC_M_PRT_TXDMA_PKT_CNT_RST):** Reset the THC_M_PRT_TXDMA_PKT_CNT counter. SW writing this bit to a 0x1, resets the THC_M_PRT_TXDMA_PKT_CNT clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch TX DMA Packet Counter (THC_M_PRT_TXDMA_PKT_CNT):** Number of TX DMA Packet sent on this port. The counter shall roll over back to 0 after reaching the maximum value.

23.3.34 THC Device Interrupt Count on this port (THC_M_PRT_DEVINT_CNT)—Offset 10E8h

Touch Device Interrupt Counter

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Device Interrupt Counter (THC_M_PRT_DEVINT_CNT_RST):** Reset the THC_M_PRT_DEVINT_CNT counter. SW writing this bit to a 0x1, resets the THC_M_PRT_DEVINT_CNT counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Device Interrupt Counter (THC_M_PRT_DEVINT_CNT):** Number of Device interrupts Received on this port. The counter shall roll over back to 0 after reaching the maximum value.

23.3.35 THC Read PRD Base Address Low for the 1st RXDMA (THC_M_PRT_RPRD_BA_LOW_1)—Offset 1100h

THC Read PRD Base Address for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**THC Read PRD Base Address for the 1st RXDMA (THC_M_PRT_RPRD_BA_LOW):** This register initializes the lower 32 bits of the 64 bit PRD table base address for the 1st RXDMA, 4K aligned, thus 20bits are allocated.
11:0	0h RO	Reserved.

23.3.36 THC Read PRD Base Address High for the 1st RXDMA (THC_M_PRT_RPRD_BA_HI_1)—Offset 1104h

THC Read PRD Base Address High for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**THC Read PRD Base Address High for the 1st RXDMA (THC_M_PRT_RPRD_BA_HI):** This register initializes the upper 32 bits of the 64 bit PRD table base address for the 1st RXDMA.

23.3.37 THC Read PRD Control for the 1st RXDMA (THC_M_PRT_RPRD_CNTRL_1)—Offset 1108h

THC Read PRD Control for the 1st RX DMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	0h RW	**PRD Table Entry Count for the 1st RX DMA (PTEC):** The number of PRD entries in each of the PRD tables held in the circular buffer. The PRD Entry Count must be large enough to contain the maximum raw data buffer size for any touch device. A fragmented data buffer could require a PRD entry for every 4KB of host memory allocated. In this case, for a 1MB raw data buffer, 128 PRD entries would be required. 00h: 1 PRD entry for each PRD Table 01h: 2 PRD entries for each PRD Table :: FFh: 256 PRD entries for each PRD Table
7	0h RO	Reserved.
6:0	0h RW	**PRD CB Depth for the 1st RX DMA (PCD):** This field indicates the number of PRD tables contained in the PRD address space. The filed directly corresponds to the number of raw data buffers used in the iTouch system. The raw data buffers are allocated by the host HID driver running in the OS. 00h: 1 PRD Table 01h: 2 PRD Table :: 7Fh: 128 PRD Tables

23.3.38 THC Read DMA Control for the 1st RXDMA (THC_M_PRT_READ_DMA_CNTRL_1)—Offset 110Ch

THC Read DMA Control for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 40000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**THC PRD CB Pointer Reset for the 1st RXDMA (TPCPR):** Setting this bit to a 1b resets DMA circular buffers read and write pointers to 00h. After the DMA CB pointers have been reset to 00h, hardware clears this bit to 0. SW can only reset tail offset when active and start are 0, i.e. DMA is idle.
30	1h RO	**Update HwStatus for the 1st RXDMA (UHS):** If set, the HwStatus field of each PRD entry (for each PRD table) bit is updated (successful or error).
29	0h RW	**Stop on Overflow for the 1st RXDMA (SOO):** When set, HW will clear the Start bit, upon detection of a DMA Buffer overflow, and stop read DMA operations.. An overflow condition occurs when the read and write pointers contain the same value.
28	0h RW/L	**Interrupt SW Enable on DMA Device Interrupt for the 1st RXDMA (INT_SW_DMA_EN):** When set to 1, an interrupt is generated to host SW even when a "touch data ready" interrupt cause is read from the touch IC INT_CAUSE register. The read DMA in the HW sequencer is not running to read the touch data in this case. The non-DMA device inband interrupt status bit is set. SW is expected to read the device interrupt cause register and if it sees the 01 (touch data ready) is set, it could potentially read the touch device using PIO.
27:24	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0h RW/V	**THC PRD CB Write Pointer for the 1st RXDMA (TPCWP):** The write pointer is updated by SW. The write pointer points to location in the DMA CB, where the next PRD table is going to be stored. SW needs to ensure that this pointer rolls over once the circular buffer's depth has been traversed with Bit[7] as the rollover bit. E.g. if the DMA CB depth is equal to 5 entries (0100b), then the write pointers will follow this pattern (SW is required to honor this behavior) 00h 01h 02h 03h 04h 80h 81h 82h 83h 84h 00h 01h ..
15:8	0h RO/V	**THC PRD CB Read Pointer for the 1st RXDMA (TPCRP):** DMA HW consumes the PRD tables in the CB, one PRD entry at a time until the EOP bit is found set in a PRD entry. At this point HW increments the PRD read pointer. Thus, the read pointer points to the PRD which the DMA engine is currently processing. This pointer rolls over once the circular buffer's depth has been traversed with bit[7] the Rollover bit. E.g. if the DMA CB depth is equal to 4 entries (0011b), then the read pointers will follow this pattern (HW is required to honor this behavior) 00h 01h 02h 03h 80h 81h 82h 83h 00h 01h ...
7	0h RW	**Interrupt Enable on DMA Completion for the 1st RXDMA (IE_DMACPL):** When set, interrupt is generated upon completion of DMA (DMACPL_STS=1).
6	0h RO	Reserved.
5	0h RW	**Interrupt Enable at EOF for the 1st RXDMA (IE_EOF):** When set, an interrupt will be generated when EOF is detected. For raw data mode, this occurs when all micro frames have been DMA'd. For HID mode, this occurs after each HID report is DMA'd.
4	0h RW	**Interrupt Enable on Non DMA Device Interrupt (IE_NDDI):** When set, an interrupt is generated to host SW when a non-DMA device inband interrupt is received.
3	0h RW	**Interrupt Enable on Stall for the 1st RXDMA (IE_STALL):** When set, an interrupt is generated to host SW when the CB read and write pointers are the same. This condition could be used to detect a stall of the GPU and subsequent buffer overrun internal to the Touch IC.
2	0h RW	**Interrupt Enable on Completion for the 1st RXDMA (IE_IOC):** When set, interrupt is generated upon completion of the PRD block transfer, with IOC=1, or when an error is encountered with the Error=1.
1	0h RW	**Interrupt Enable (IE) on Error for the 1st RXDMA (IE_ERROR):** When set, interrupt is generated upon an read DMA error is encountered.
0	0h RW/V	**Start for the 1st RXDMA (START):** SW sets the Start bit to arm the DMA engine. Once SW sets the Start bit it cannot modify entries in the PRD table. This gives HW the option of caching the PRD table for performance reasons. SW clears the bit after the DMA completion as indicated by interrupt and/or Status bits. SW can also clear the Start bit to abort an on-going DMA operation. DMA hardware completes all the outstanding requests to system memory and then stops the PRD actions at a safe point, e.g. at a microframe boundary so that it can resumed gracefully after SW set the start bit again. HW will clear this bit upon error conditions.

23.3.39 THC Read Interrupt Status for the 1st RXDMA (THC_M_PRT_READ_DMA_INT_STS_1)—Offset 1110h

THC Read DMA Interrupt Status Register

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RO/V	**Active status for the 1st RXDMA (ACTIVE):** DMA is active and not completed. Set by HW when the Start bit is set by SW and auto-cleared by HW in the following conditions: - The entire DMA operation has been completed or - The DMA operation has been halted by software clearing the Start bit (and no read completion pending).
7:6	0h RO	Reserved.
5	0h RW/1C/V	**Interrupt Status of EOF Interrupt for the 1st RXDMA (EOF_INT_STS):** Interrupt status when an EOF is encountered. If the IE_EOF bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.
4	0h RW/1C/V	**Interrupt Status of non DMA device interrupt (NONDMA_INT_STS):** Interrupt status when a non-DMA device inband interrupt is received. If the IE_NDDI bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.
3	0h RW/1C/V	**Interrupt Status of PRD table stalls for the 1st RXDMA (STALL_STS):** Interrupt status when the CB read and write pointers are the same and device sends moer touch data to THC. This condition could be used to detect a stall of the GPU and subsequent buffer overrun internal to the Touch IC. If the IE_STALL bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.
2	0h RW/1C/V	**Interrupt Status of PRD completion with IOC =1 for the 1st RXDMA (IOC_STS):** An PRD entry with IOC bit set has been completed during DMA operation. If the IE_IOC bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.
1	0h RW/1C/V	**Error status for the 1st RXDMA (ERROR_STS):** Error encountered during DMA operation. An interrupt is generated if the interrupt is enabled. SW clears the bit by writing 1 to the bit.
0	0h RW/1C/V	**DMA Complete for the 1st RXDMA (DMACPL_STS):** This bit is set upon successful completion of the DMA operation when the CB read and write pointers are the same. If the IE bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.

23.3.40 THC Read DMA Error Register for the 1st RXDMA (THC_M_PRT_READ_DMA_ERR_1)—Offset 1114h

THC Read DMA Error Register for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/1C/V	**DMA Length Error for the 1st RXDMA (DLERR):** Indicates the raw data transfer request from the Touch IC is longer than allocated PRD entries accounted for. This error condition does not apply to SPI touch device.

23.3.41 Touch Sequencer GuC Tail Offset Address Low for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_LOW_1)—Offset 1118h

Touch Sequencer GuC Tail Offset Address Low for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RW	**Touch Sequencer GuC Tail Offset Address Low for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_LOW):** This register initializes the lower 32 bits of the 64 bit GuC tail offset address, OW aligned. The GuC Tail Offset is a 32 bit value, updated by the THC Controller to set the GuC circular buffer to the correct value. The 64 bit memory address containing the tail offset is allocated by the graphics driver and passed to the THC Controller Driver.
2:0	0h RO	Reserved.

23.3.42 Touch Sequencer GuC Tail Offset Address High for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_HI_1)—Offset 111Ch

Touch Sequencer GuC Tail Offset Address HIGH for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Touch Sequencer GuC Tail Offset Address HIGH for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_HI):** This register initializes the upper 32 bits of the 64 bit GuC tail offset address. The GuC Tail Offset is a 32 bit value, updated by the THC Controller to set the GuC circular buffer to the correct value. The 64 bit memory address containing the tail offset is allocated by the graphics driver and passed to the THC Controller Driver.

23.3.43 Touch Host Controller GuC Work Queue Item Size for the 1st RXDMA (THC_M_PRT_GUC_WORKQ_ITEM_SZ_1)—Offset 1120h

Touch Host Controller GuC Work Queue Item Size for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**Touch Host Controller GuC Work Queue Item Size for the 1st RXDMA (WORKQ_ITEM_SZ):** This register initializes the WorkQueueItemSz for the GuC processing algorithm

23.3.44 Touch Host Controller GuC Control register for the 1st RXDMA (THC_M_PRT_GUC_WORKQ_SZ_1)—Offset 1124h

Touch Host Controller GuC Control register for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**Guc Work Queue Size for the 1st RXDMA (WORKQ_SZ):** This register initializes the WorkQueueSz for the GuC processing algorithm

23.3.45 Touch Sequencer Control for the 1st DMA (THC_M_PRT_TSEQ_CNTRL_1)—Offset 1128h

Touch Sequencer Control for the 1st DMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW/1S/V	**Reset Tail Offset for the 1st RXDMA (RTO):** SW writing this bit to a 0x1 resets the current TailOffset value (that is maintained as a result of the Tail Offset calculation) to 0x0. After HW has reset the tail offset to 0x0, HW resets RTO to 0x0.
3	0h RW	**Enable GuC Processing for the 1st RXDMA (EGP):** When this bit is set to 1b, the THC sequencer will execute the GuC processing flow when TOUCH_FRAME_CHAR.EOF=1 TOUCH_FRAME_CHAR.HDR=0.
2	0h RW/1S/V	**Reset GuC Doorbell for the 1st RXDMA (RGD):** SW Writing this bit to a 0x1, resets the GuC Doorbell to 0x1 (The doorbell can never be a value of 0x0). After HW has set the doorbell to 0x1, HW sets RGD to 0x0.
1:0	0h RO	Reserved.

23.3.46 Touch Sequencer GuC Doorbell Address Low for the 1st RXDMA (THC_M_PRT_GUC_DB_ADDR_LOW_1)—Offset 1130h

Touch Sequencer GuC Doorbell Address Low for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Touch Sequencer GuC Doorbell Address Low for the 1st RXDMA (GUC_DB_ADDR_LOW):** This register initializes the lower 32 bits of the 64 bit GuC doorbell address for the 1st RXDMA, which is required to be DW aligned.
1:0	0h RO	Reserved.

23.3.47 Touch Sequencer GuC Doorbell Address High for the 1st RXDMA (THC_M_PRT_GUC_DB_ADDR_HI_1)—Offset 1134h

Touch Sequencer GuC Doorbell Address High for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Touch Sequencer GuC Doorbell Address High for the 1st RXDMA (GUC_DB_ADDR_HI):** This register initializes the upper 32 bits of the 64 bit GuC doorbell address for the 1st RXDMA.

23.3.48 Touch Sequencer GuC Doorbell Data (THC_M_PRT_GUC_DB_DATA_1)—Offset 1138h

Touch Sequencer GuC Doorbell Data for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:0	1h RW/V	**Touch Sequencer GuC Doorbell Data for the 1st RXDMA (GUC_DB_DATA):** This register initializes the 32 bits of the GuC doorbell Data for the 1st RXDMA 1)This register is also changed when HW increments the value, AND 2)SW can only re-initialize it when RXDMA is stopped including during initialization.

23.3.49 Touch Sequencer GuC Tail Offset Initial Value for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_INITVAL_1)—Offset 1140h

Touch Sequencer GuC Tail Offset Initial Value for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Touch Sequencer GuC Tail Offset Initial Value for the 1st RXDMA (THC_M_PRT_GUC_OFFSET_INITVAL):** This register initializes the initial value of the GuC tail offset. The GuC Tail Offset is a 32 bit value, updated by the THC Controller to set the GuC circular buffer to the correct value.

23.3.50 THC Device Address for the bulk/touch data read for the 1st RXDMA (THC_M_PRT_RD_BULK_ADDR_1)—Offset 1170h

THC Device Address for the bulk/touch data read for the 1st RXDMA

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 1000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	1000h RW/O	**THC Device Address for the bulk/touch data read for the 1st RXDMA (THC_M_PRT_RD_BULK_ADDR):** THC Device Address for the bulk/touch data read. In SPI mode, the touch data read cycles addresses start from the bulk address specified in this register and increment every packet until the end of the microframe. The touch read address resumes using the address in this register at the beginning of every new microframe. SW is responsible to program this register correctly, and make sure all resulting touch cycles will not exceed the touch device's bulk address space or roll over. Otherwise, THC's behavior is undefined. Note: For SPI devices, only 24bit addressing space is supported. Default to 0x1000.

23.3.51 THC Gfx/SW Doorbell Count from the 1st Stream RXDMA on this port (THC_M_PRT_DB_CNT_1)—Offset 11A0h

Touch Host Controller Doorbell Counter for the 1st RXDMA

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Host Controller Doorbell Counter Reset for the 1st RXDMA (THC_M_PRT_DB_CNT_RST):** Reset the THC_M_PRT_DB_CNT counter. SW writing this bit to a 0x1, resets the THC_M_PRT_DB_CNT counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Host Controller Doorbell Counter for the 1st RXDMA (THC_M_PRT_DB_CNT):** Number of Touch Host Controller Doorbell sent on this port. The counter shall roll over back to 0 after reaching the maximum value.

23.3.52 THC Frame Count from the 1st Stream RXDMA on this port (THC_M_PRT_FRM_CNT_1)—Offset 11A4h

Touch Frame Counter

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Frame Counter Reset (THC_M_PRT_FRM_CNT_RST):** Reset the THC_M_PRT_FRM_CNT counter. SW writing this bit to a 0x1, resets the THC_M_PRT_FRM_CNT counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Frame Counter (THC_M_PRT_FRM_CNT):** Number of Touch Frames received on this DMA engine, including the dropped frames. The counter shall roll over back to 0 after reaching the maximum value.

23.3.53 THC Micro Frame Count from the 1st Stream RXDMA on this port (THC_M_PRT_UFRM_CNT_1)—Offset 11A8h

Touch Microframe Counter for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Microframe Counter Reset for the 1st RXDMA (THC_M_PRT_UFRM_CNT_RST):** Reset the THC_M_PRT_UFRM_CNT_1 counter. SW writing this bit to a 0x1, resets the THC_M_PRT_UFRM_CNT counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Microframe Counter for the 1st RXDMA (THC_M_PRT_UFRM_CNT):** Number of Touch Microframes received on this DMA stream. The counter shall roll over back to 0 after reaching the maximum value.

23.3.54 THC Packet Count from the 1st Stream RXDMA on this port (THC_M_PRT_RXDMA_PKT_CNT_1)—Offset 11ACh

Touch RX DMA Packet Counter for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch RX DMA Packet Counter Reset for the 1st RXDMA (THC_M_PRT_RXDMA_PKT_CNT_RST):** Reset the THC_M_PRT_RXDMA_PKT_CNT counter. SW writing this bit to a 0x1, resets the THC_M_PRT_RXDMA_PKT_CNT clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch RX DMA Packet Counter for the 1st RXDMA (THC_M_PRT_RXDMA_PKT_CNT):** Number of RX DMA Packet received on this DMA engine. The counter shall roll over back to 0 after reaching the maximum value.

23.3.55 THC Software Interrupt Count from the 1st Stream RXDMA on this port (THC_M_PRT_SWINT_CNT_1)—Offset 11B0h

Touch Host Controller Doorbell Counter for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Host Controller Software Interrupt Counter Reset for the 1st RXDMA (THC_M_PRT_SWINT_CNT_RST):** Reset the THC_M_PRT_SWINT_CNT_1 counter. SW writing this bit to a 0x1, resets the THC_M_PRT_SWINT_CNT_1 counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Host Controller Interrupt Counter for the 1st RXDMA (THC_M_PRT_SWINT_CNT):** Number of Touch Host Controller Doorbell sent on this DMA engine. The counter shall roll over back to 0 after reaching the maximum value.

23.3.56 Touch Sequencer Frame Drop Counter for the 1st RXDMA (THC_M_PRT_FRAME_DROP_CNT_1)—Offset 11B4h

Touch Sequencer Frame Drop Counter for the 1st RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Reset Frame Dropped Counter for the 1st RXDMA (RFDC):** SW writing this bit to a 0x1, resets the frame dropped counter, TSEQ_FRAME_DROP_CTR, to a 0x0. HW clears this bit to a 0x0 after the counter has been reset. SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Number of Frames Dropped for the 1st RXDMA (NOFD):** Number of Frames Dropped for the 1st RXDMA. When the counter reaches the maximum value, it shall be kept to the maximum value until the SW reset the counter using RFDC_1 bit.

23.3.57 THC Read PRD Base Address Low for the 2nd RXDMA (THC_M_PRT_RPRD_BA_LOW_2)—Offset 1200h

THC Read PRD Base Address for the 2nd RXDMA

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**THC Read PRD Base Address for the 2nd RXDMA (THC_M_PRT_RPRD_BA_LOW):** This register initializes the lower 32 bits of the 64 bit PRD table base address for the 2nd RXDMA, 4K aligned, thus 20bits are allocated.
11:0	0h RO	Reserved.

23.3.58 THC Read PRD Base Address High for the 2nd RXDMA (THC_M_PRT_RPRD_BA_HI_2)—Offset 1204h

THC Read 2nd RXDMA PRD Base Address

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**2nd RXDMA PRD Base Address Hi (THC_M_PRT_RPRD_BA_HI):** This register initializes the upper 32 bits of the 64 bit PRD table base address..

23.3.59 THC Read PRD Control for the 2nd RXDMA (THC_M_PRT_RPRD_CNTRL_2)—Offset 1208h

THC Read PRD Control for the 2nd RXDMA

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:8	0h RW	**Table Entry Count for the 2nd RXDMA (PTEC):** The number of PRD entries in each of the PRD tables held in the circular buffer. The PRD Entry Count must be large enough to contain the maximum raw data buffer size for any touch device. A fragmented data buffer could require a PRD entry for every 4KB of host memory allocated. In this case, for a 1MB raw data buffer, 128 PRD entries would be required. 00h: 1 PRD entry for each PRD Table 01h: 2 PRD entries for each PRD Table :: FFh: 256 PRD entries for each PRD Table
7	0h RO	Reserved.
6:0	0h RW	**CB Depth for the 2nd RXDMA (PCD):** This field indicates the number of PRD tables contained in the PRD address space. The filed directly corresponds to the number of raw data buffers used in the iTouch system. The raw data buffers are allocated by the host HID driver running in the OS. 00h: 1 PRD Table 01h: 2 PRD Table :: 7Fh: 128 PRD Tables For Example: iTouch allocates 16 PRD tables. Each PRD table need to address 1MB of address space, requiring 256 entries. 16 PRD Tables * 256 Entries/table * 16B per table == 64KB of PRD entries.

23.3.60 THC Read DMA Control for the 2nd RXDMA (THC_M_PRT_READ_DMA_CNTRL_2)—Offset 120Ch

THC Read DMA Control for the 2nd RXDMA

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 40000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**THC PRD CB Pointer Reset for the 2nd RXDMA (TPCPR):** Setting this bit to a 1b resets DMA circular buffers read and write pointers to 00h. After the DMA CB pointers have been reset to 00h, hardware clears this bit to 0. SW can only reset tail offset when active and start are 0, i.e. DMA is idle.
30	1h RO	**Update HwStatus for the 2nd RXDMA (UHS):** If set, the HwStatus field of each PRD entry (for each PRD table) bit is updated (successful or error).
29	0h RW	**Stop on Overflow for the 2nd RXDMA (SOO):** When set, HW will clear the Start bit, upon detection of a DMA Buffer overflow, and stop read DMA operations. An overflow condition occurs when the read and write pointers contain the same value.
28	0h RW/L	**Interrupt SW Enable on DMA Device Interrupt for the 2nd RXDMA (INT_SW_DMA_EN):** When set to 1, an interrupt is generated to host SW even when a "touch data ready" interrupt cause is read from the touch IC INT_CAUSE register. The read DMA in the HW sequencer is not running to read the touch data in this case. The non-DMA device inband interrupt status bit is set. SW is expected to read the device interrupt cause register and if it sees the 01 (touch data ready) is set, it could potentially read the touch device using PIO.
27:24	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
23:16	0h RW/V	**THC PRD CB Write Pointer for the 2nd RXDMA (TPCWP):** The write pointer is updated by SW. The write pointer points to location in the DMA CB, where the next PRD table is going to be stored. SW needs to ensure that this pointer rolls over once the circular buffer's depth has been traversed with Bit[7] as the rollover bit. E.g. if the DMA CB depth is equal to 5 entries (0100b), then the write pointers will follow this pattern (SW is required to honor this behavior) 00h 01h 02h 03h 04h 80h 81h 82h 83h 84h 00h 01h ..
15:8	0h RO/V	**THC PRD CB Read Pointer for the 2nd RXDMA (TPCRP):** DMA HW consumes the PRD tables in the CB, one PRD entry at a time until the EOP bit is found set in a PRD entry. At this point HW increments the PRD read pointer. Thus, the read pointer points to the PRD which the DMA engine is currently processing. This pointer rolls over once the circular buffer's depth has been traversed with bit[7] the Rollover bit. E.g. if the DMA CB depth is equal to 4 entries (0011b), then the read pointers will follow this pattern (HW is required to honor this behavior) 00h 01h 02h 03h 80h 81h 82h 83h 00h 01h ...
7	0h RW	**Interrupt Enable on DMA Completion for the 2nd RXDMA (IE_DMACPL):** When set, interrupt is generated upon completion of DMA (DMACPL_STS=1).
6	0h RO	Reserved.
5	0h RW	**Interrupt Enable at EOF for the 2nd RXDMA (IE_EOF):** When set, an interrupt will be generated when EOF is detected. For raw data mode, this occurs when all micro frames have been DMA'd. For HID mode, this occurs after each HID report is DMA'd. When EGP is set, the interrupt occurs after GuC processing is complete.
4	0h RO	Reserved.
3	0h RW	**Interrupt Enable on Stall for the 2nd RXDMA (IE_STALL):** When set, an interrupt is generated to host SW when the CB read and write pointers are the same. This condition could be used to detect a stall of the GPU and subsequent buffer overrun internal to the Touch IC.
2	0h RW	**Interrupt Enable on Completion for the 2nd RXDMA (IE_IOC):** When set, interrupt is generated upon completion of the PRD block transfer, with IOC=1, or when an error is encountered with the Error=1.
1	0h RW	**Interrupt Enable on Error for the 2nd RXDMA (IE_ERROR):** When set, interrupt is generated upon an read DMA error is encountered.
0	0h RW/V	**Start for the 2nd RXDMA (START):** SW sets the Start bit to arm the DMA engine. Once SW sets the Start bit it cannot modify entries in the PRD table. This gives HW the option of caching the PRD table for performance reasons. SW clears the bit after the DMA completion as indicated by interrupt and/or Status bits. SW can also clear the Start bit to abort an on-going DMA operation. DMA hardware completes all the outstanding requests to system memory and then stops the PRD actions at a safe point, e.g. at a microframe boundary so that it can resumed gracefully after SW set the start bit again. HW will clear this bit upon error conditions.

23.3.61 THC Read Interrupt Status for the 2nd RXDMA (THC_M_PRT_READ_DMA_INT_STS_2)—Offset 1210h

THC Read Interrupt Status for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RO/V	**Active status bit for the 2nd RXDMA (ACTIVE):** DMA is active and not completed. Set by HW when the Start bit is set by SW and auto-cleared by HW in the following conditions: - The entire DMA operation has been completed or - The DMA operation has been halted by software clearing the Start bit (and no read completion pending).
7:6	0h RO	Reserved.
5	0h RW/1C/V	**Interrupt Status of EOF for the 2nd RXDMA (EOF_INT_STS):** Interrupt status when an EOF is encountered. If the IE_EOF bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.
4	0h RO	Reserved.
3	0h RW/1C/V	**Interrupt Status of PRD table stalls bit for the 2nd RXDMA (STALL_STS):** Interrupt status when the CB read and write pointers are the same. This condition could be used to detect a stall of the GPU and subsequent buffer overrun internal to the Touch IC. If the IE_STALL bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.
2	0h RW/1C/V	**Interrupt Status of PRD completion with IOC =1 for the 2nd RXDMA (IOC_STS):** An PRD entry with IOC bit set has been completed during DMA operation. If the IE_IOC bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.
1	0h RW/1C/V	**Error status bit for the 2nd RXDMA (ERROR_STS):** Error encountered during DMA operation. An interrupt is generated if the interrupt is enabled. SW clears the bit by writing 1 to the bit.
0	0h RW/1C/V	**DMA Complete bit for the 2nd RXDMA (DMACPL_STS):** This bit is set upon successful completion of the DMA operation. If the IE bit is also 1, then an interrupt is generated. SW clears the bit by writing 1 to the bit.

23.3.62 THC Read DMA Error Register for the 2nd RXDMA (THC_M_PRT_READ_DMA_ERR_2)—Offset 1214h

THC Read DMA Error Register for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	Reserved.
0	0h RW/1C/V	**DMA Length Error for the 2nd RXDMA (DLERR):** Indicates the raw data transfer request from the Touch IC is longer than allocated PRD entries accounted for. This error condition does not apply to SPI touch device.

23.3.63 Touch Sequencer GuC Tail Offset Address Low for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_LOW_2)—Offset 1218h

Touch Sequencer GuC Tail Offset Address Low for the 2nd RXDMA

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:3	0h RW	**Touch Sequencer GuC Tail Offset Address Low for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_LOW):** This register initializes the lower 32 bits of the 64 bit GuC tail offset address, OW aligned. The GuC Tail Offset is a 32 bit value, updated by the THC Controller to set the GuC circular buffer to the correct value. The 64 bit memory address containing the tail offset is allocated by the graphics driver and passed to the THC Controller Driver.
2:0	0h RO	Reserved.

23.3.64 Touch Sequencer GuC Tail Offset Address High for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_HI_2)—Offset 121Ch

Touch Sequencer GuC Tail Offset Address High for the 2nd RXDMA

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Touch Sequencer GuC Tail Offset Address High for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_HI):** This register initializes the upper 32 bits of the 64 bit GuC tail offset address. The GuC Tail Offset is a 32 bit value, updated by the THC Controller to set the GuC circular buffer to the correct value. The 64 bit memory address containing the tail offset is allocated by the graphics driver and passed to the THC Controller Driver.

23.3.65 Touch Host Controller GuC Work Queue Item Size for the 2nd RXDMA (THC_M_PRT_GUC_WORKQ_ITEM_SZ_2)—Offset 1220h

Touch Host Controller GuC Work Queue Item Size for the 2nd RXDMA

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**WORKQ_ITEM_SZ for the 2nd RXDMA (WORKQ_ITEM_SZ):** This register initializes the WorkQueueItemSz for the GuC processing algorithm for the 2nd RXDMA

23.3.66 Touch Host Controller GuC Control register for the 2nd RXDMA (THC_M_PRT_GUC_WORKQ_SZ_2)—Offset 1224h

Touch Host Controller GuC Control register for the 2nd RXDMA

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**WORKQ_SZ for PRD2 (WORKQ_SZ):** This register initializes the WorkQueueSz for the GuC processing algorithm

23.3.67 Touch Sequencer Control for the 2nd DMA (THC_M_PRT_TSEQ_CNTRL_2)—Offset 1228h

Touch Sequencer Control for the 2nd DMA

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW/1S/V	**Reset Tail Offset for the 2nd RXDMA (RTO):** SW writing this bit to a 0x1 resets the current TailOffset value (that is maintained as a result of the Tail Offset calculation) to 0x0. After HW has reset the tail offset to 0x0, HW resets RTO to 0x0.
3	0h RW	**Enable GuC Processing for the 2nd RXDMA (EGP):** When this bit is set to 1b, the THC sequencer will execute the GuC processing flow when TOUCH_FRAME_CHAR.EOF=1 TOUCH_FRAME_CHAR.HDR=0.
2	0h RW/1S/V	**Reset GuC Doorbell for the 2nd RXDMA (RGD):** SW Writing this bit to a 0x1, resets the GuC Doorbell to 0x1 (The doorbell can never be a value of 0x0). After HW has set the doorbell to 0x1, HW sets RGD to 0x0.
1:0	0h RO	Reserved.

23.3.68 Touch Sequencer GuC Doorbell Address Low for the 2nd RXDMA (THC_M_PRT_GUC_DB_ADDR_LOW_2)—Offset 1230h

Touch Sequencer GuC Doorbell Address Low for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Touch Sequencer GuC Doorbell Address Low for the 2nd RXDMA (GUC_DB_ADDR_LOW):** This register initializes the lower 32 bits of the 64 bit GuC doorbell address for the 2nd RXDMA, which is required to be DW aligned.
1:0	0h RO	Reserved.

23.3.69 Touch Sequencer GuC Doorbell Address High for the 2nd RXDMA (THC_M_PRT_GUC_DB_ADDR_HI_2)—Offset 1234h

Touch Sequencer GuC Doorbell Address High for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Touch Sequencer GuC Doorbell Address High for the 2nd RXDMA (GUC_DB_ADDR_HI):** This register initializes the upper 32 bits of the 64 bit GuC doorbell address for the 2nd RXDMA

23.3.70 Touch Sequencer GuC Doorbell Data for PRD2 (THC_M_PRT_GUC_DB_DATA_2)—Offset 1238h

Touch Sequencer GuC Doorbell Data for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1h

Bit Range	Default & Access	Field Name (ID): Description
31:0	1h RW/V	**Touch Sequencer GuC Doorbell Data for the 2nd RXDMA (GUC_DB_DATA):** This register initializes the 32 bits of the GuC doorbell Data for the 2nd RXDMA. 1)This register is also changed when HW increments the value, AND 2)SW can only re-initialize it when RXDMA is stopped including during initialization.

23.3.71 Touch Sequencer GuC Tail Offset Initial Value for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_INITVAL_2)—Offset 1240h

Touch Sequencer GuC Tail Offset Initial Value for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Touch Sequencer GuC Tail Offset Initial Value for the 2nd RXDMA (THC_M_PRT_GUC_OFFSET_INITVAL):** This register initializes the initial value of the GuC tail offset. The GuC Tail Offset is a 32 bit value, updated by the THC Controller to set the GuC circular buffer to the correct value.

23.3.72 THC Device Address for the bulk/touch data read for the 2nd RXDMA (THC_M_PRT_RD_BULK_ADDR_2)—Offset 1270h

THC Device Address for the bulk/touch data read for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 1000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	1000h RW/O	**THC Device Address for the bulk/touch data read for the 2nd RXDMA (THC_M_PRT_RD_BULK_ADDR):** THC Device Address for the bulk/touch data read. In SPI mode, the touch data read cycles addresses start from the bulk address specified in this register and increment every packet until the end of the microframe. The touch read address resumes using the address in this register at the beginning of every new microframe. SW is responsible to program this register correctly, and make sure all resulting touch cycles will not exceed the touch device's bulk address space or roll over. Otherwise, THC's behavior is undefined. Note: For SPI devices, only 24bit addressing space is supported. Default to 0x1000.

23.3.73 THC Gfx/SW Doorbell Count from the 2nd Stream RXDMA on this port (THC_M_PRT_DB_CNT_2)—Offset 12A0h

Touch Host Controller Doorbell Counter for the 2nd DMA engine

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Host Controller Doorbell Counter Reset (THC_M_PRT_DB_CNT_RST):** Reset the THC_M_PRT_DB_CNT_2 counter. SW writing this bit to a 0x1, resets the THC_M_PRT_DB_CNT2 counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Host Controller Doorbell Counter (THC_M_PRT_DB_CNT):** Number of Touch Host Controller Doorbell sent on this port. The counter shall roll over back to 0 after reaching the maximum value.

23.3.74 THC Frame Count from the 2nd Stream RXDMA on this port (THC_M_PRT_FRM_CNT_2)—Offset 12A4h

Touch Frame Counter for the 2nd DMA engine

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Frame Counter Reset (THC_M_PRT_FRM_CNT_RST):** Reset the THC_M_PRT_FRM_CNT_2 counter. SW writing this bit to a 0x1, resets the THC_M_PRT_FRM_CNT2 counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Frame Counter (THC_M_PRT_FRM_CNT):** Number of Touch Frames received on this DMA engine, including the dropped frames. The counter shall roll over back to 0 after reaching the maximum value.

23.3.75 THC Micro Frame Count from the 2nd Stream RXDMA on this port (THC_M_PRT_UFRM_CNT_2)—Offset 12A8h

Touch Microframe Counter for the 2nd DMA engine

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Microframe Counter Reset for the 2nd DMA engine (THC_M_PRT_UFRM_CNT_RST):** Reset the THC_M_PRT_UFRM_CNT_2 counter. SW writing this bit to a 0x1, resets the THC_M_PRT_UFRM_CNT2 counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Microframe Counter for the 2nd DMA engine (THC_M_PRT_UFRM_CNT):** Number of Touch Microframes received on this DMA engine.The counter shall roll over back to 0 after reaching the maximum value.

23.3.76 THC Packet Count from the 2nd Stream RXDMA on this port (THC_M_PRT_RXDMA_PKT_CNT_2)—Offset 12ACh

Touch RX DMA Packet Counter for the 2nd DMA engine

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch RX DMA Packet Counter Reset (THC_M_PRT_RXDMA_PKT_CNT_RST):** Reset the THC_M_PRT_RXDMA_PKT_CNT2 counter. SW writing this bit to a 0x1, resets the THC_M_PRT_INT_CNTTHC_M_PRT_RXDMA_PKT_CNT2 clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch RX DMA Packet Counter (THC_M_PRT_RXDMA_PKT_CNT):** Number of RX DMA Packet received on this DMA engine. The counter shall roll over back to 0 after reaching the maximum value.

23.3.77 THC Software Interrupt Count from the 2nd Stream RXDMA on this port (THC_M_PRT_SWINT_CNT_2)—Offset 12B0h

Touch Host Controller Doorbell Counter for the 2nd DMA engine

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Touch Host Controller Software Interrupt Counter Reset (THC_M_PRT_SWINT_CNT_RST):** Reset the THC_M_PRT_SWINT_CNT2 counter. SW writing this bit to a 0x1, resets the THC_M_PRT_SWINT_CNT2 counter to a 0x0.HW clears this bit to a 0x0 after the counter has been reset.SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Touch Host Controller Interrupt Counter (THC_M_PRT_SWINT_CNT):** Number of Touch Host Controller Doorbell sent on this DMA engine. The counter shall roll over back to 0 after reaching the maximum value.

23.3.78 Touch Sequencer Frame Drop Counter for the 2nd RXDMA (THC_M_PRT_FRAME_DROP_CNT_2)—Offset 12B4h

Touch Sequencer Frame Drop Counter for the 2nd RXDMA

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**Reset Frame Dropped Counter for the 2nd RXDMA (RFDC):** SW writing this bit to a 0x1, resets the frame dropped counter, TSEQ_FRAME_DROP_CTR, to a 0x0. HW clears this bit to a 0x0 after the counter has been reset. SW writing this bit to a 0x0 has not effect.
30:0	0h RO/V	**Number of Frames Dropped for the 2nd RXDMA (NOFD):** Number of Frames Dropped for the 2nd RXDMA. Number of Frames Dropped for the 1st RXDMA. When the counter reaches the maximum value, it shall be kept to the maximum value until the SW reset the counter using RFDC_2 bit.

24 8254 Timer

24.1 8254 Timer Registers Summary

Table 24-1. Summary of 8254 Timer Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
40h	40h	Counter 0 - Counter Access Ports Register (C0_CAPR)—Offset 40h	0h
40h	40h	Counter 0 - Interval Timer Status Byte Format Register (C0_ITSBFR)—Offset 40h	C4h
42h	42h	Counter 2 - Counter Access Ports Register (C2_CAPR)—Offset 42h	0h
42h	42h	Counter 2 - Interval Timer Status Byte Format Register (C2_ITSBFR)—Offset 42h	0h
43h	43h	Timer Control Word Register (TCW)—Offset 43h	0h
43h	43h	Read Back Command (RBC)—Offset 43h	C0h
43h	43h	Counter Latch Command (CLC)—Offset 43h	0h

24.1.1 Counter 0 - Counter Access Ports Register (C0_CAPR)—Offset 40h

Access Method

Type: IO Register (Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW/V	**Counter Port (CP):** Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

24.1.2 Counter 0 - Interval Timer Status Byte Format Register (C0_ITSBFR)—Offset 40h

Each counter's status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for a given counter, the next read from the counter's Counter Access Ports Register (40h for counter 0 and 42h for counter 2) returns the status byte. The status byte returns the following:

Access Method

Type: IO Register (Size: 8 bits)

Device:
Function:

Default: C4h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RO	**Counter OUT Pin State (COPS):** When this bit is a 1, the OUT pin of the counter is also a 1. When this bit is a 0, the OUT pin of the counter is also a 0.
6	1h RO	**Count Register Status (CRSTS):** This bit indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the counter mode, but until the count is loaded into the counting element (CE), the count value will be incorrect. 0 Count has been transferred from CR to CE and is available for reading. 1 Null Count. Count has not been transferred from CR to CE and is not yet available for reading.
5:4	0h RO	**Read/Write Selection Status (RW_SLT_STS):** These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	2h RO	**Mode Selection Status (MD_SLT_STS):** These bits return the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	0h RO	**Countdown Type Status (CDT_STS):** This bit reflects the current countdown type, ether 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

24.1.3 Counter 2 - Counter Access Ports Register (C2_CAPR)—Offset 42h

Same definition as Counter 0 - Counter Access Ports Register.

24.1.4 Counter 2 - Interval Timer Status Byte Format Register (C2_ITSBFR)—Offset 42h

Same definition as counter 0.

24.1.5 Timer Control Word Register (TCW)—Offset 43h

This register is programmed prior to any counter being accessed to specify counter modes. Following reset, the control words for each register are undefined and each counter output is 0. Each timer must be programmed to bring it into a known state. There are two special commands that can be issued to the counters through this register, the Read Back Command and the Counter Latch Command. When these commands are chosen, several bits within this register are redefined.

Access Method

Type: IO Register (Size: 8 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:6	0h WO	**Counter Select (CNT_SLT):** The Counter Selection bits select the counter the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1 00 Counter 0 select 01 Reserved 10 Counter 2 select 11 Read Back Command

Bit Range	Default and Access	Field Name (ID): Description
5:4	0h WO	**Read/Write Select: (RW_SLT):** These bits are the read/ write control bits. The actual counter programming is done through the counter port (40h for counter 0 and 42h for counter 2) 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	0h WO	**Counter Mode Selection (CNT_MD_SLTN):** These bits select one of six possible modes of operation for the selected counter. 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	0h WO	**Binary/BCD Countdown Select (B_BCD_CNTDWN_SLT):** 0 Binary countdown is used. The largest possible binary count is 2^16 1 Binary coded decimal (BCD) count is used.The largest possible BCD count is 10^4

24.1.6 Read Back Command (RBC)—Offset 43h

The Read Back Command is used to determine the count value, programmed mode, and current states of the OUT pin and Null count flag of the selected counter or counters. Status and/or count may be latched in any or all of the counters by selecting the counter during the register write. The count and status remain latched until read, and further latch commands are ignored until the count is read.
Both count and status of the selected counters may be latched simultaneously by setting both bit 5 and bit 4 to 0. If both are latched, the first read operation from that counter returns the latched status. The next one or two reads, depending on whether the counter is programmed for one or two byte counts, returns the latched count. Subsequent reads return an unlatched count.

Access Method

Type: IO Register (Size: 8 bits)

Device:
Function:

Default: C0h

Bit Range	Default and Access	Field Name (ID): Description
7:6	3h WO	**Read Back Command (RBC):** Must be 11 to select the Read Back Command
5	0h WO	**Latch Count of Selected Counters (LCSC):** 0 Current count value of the selected counters will be latched 1 Current count will not be latched
4	0h WO	**Latch Status of Selected Counters (LSSC):** 0 Status of the selected counters will be latched 1 Status will not be latched
3	0h WO	**Counter 2 Select (CNT_2_SLT):** When set to 1, Counter 2 count and/or status will be latched
2	0h RO	Reserved.
1	0h WO	**Counter 0 Select (CNT_0_SLT):** When set to 1, Counter 0 count and/or status will be latched.
0	0h RO	Reserved.

24.1.7 Counter Latch Command (CLC)—Offset 43h

The Counter Latch Command latches the current count value. This command is used to insure that the count read from the counter is accurate. The count value is then read from each counter's count register through the Counter Ports Access Ports Register (40h for counter 0 and 42h for counter 2). The count must be read according to the programmed format, i.e. if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other (read, write, or programming operations for other counters may be inserted between the reads). If a counter is latched once and then latched again before the count is read, the second Counter Latch Command is ignored.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:6	0h WO	**Counter Selection (CNT_SLT):** These bits select the counter for latching. If 11 is written, then the write is interpreted as a read back command. 00 = Counter 0 01 = Reserved 10 = Counter 2
5:4	0h WO	**Counter Latch Command (CLC):** Write 00 to select the Counter Latch Command.
3:0	0h RO	Reserved.

25 Advanced Programmable Interrupt (APIC)

25.1 APIC Indirect Registers Summary

APIC Indirect Registers lists the registers that can be accessed within the APIC using the Index Register. When accessing these registers, accesses must be done one DWord at a time. For example, software should never access byte 2 from the Data register before accessing bytes 0 and 1. The hardware will not attempt to recover from a bad programming model in this case.

Index	Mnemonic	Register Name
10-11h	RTE0	Redirection Table Entry 0
12-13h	RTE1	Redirection Table Entry 1
14-15h	RTE2	Redirection Table Entry 2
...	...	...
3E-3Fh	RTE23	Redirection Table Entry 23
40-41h	RTE24	Redirection Table Entry 24
...	...	...
FE-FFh	RTE119	Redirection Table Entry 119

Table 25-1. Summary of APIC Indirect Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	3h	Identification Register (ID)—Offset 0h	0h
1h	4h	Version Register (VER)—Offset 1h	770020h
10h	17h	Redirection Table Entry 0 (RTE0)—Offset 10h	10000h
12h	19h	Redirection Table Entry 1 (RTE1)—Offset 12h	0h
14h	1Bh	Redirection Table Entry 2 (RTE2)—Offset 14h	0h
16h	1Dh	Redirection Table Entry 3 (RTE3)—Offset 16h	0h
18h	1Fh	Redirection Table Entry 4 (RTE4)—Offset 18h	0h
1Ah	21h	Redirection Table Entry 5 (RTE5)—Offset 1Ah	0h
1Ch	23h	Redirection Table Entry 6 (RTE6)—Offset 1Ch	0h
1Eh	25h	Redirection Table Entry 7 (RTE7)—Offset 1Eh	0h
20h	27h	Redirection Table Entry 8 (RTE8)—Offset 20h	0h
22h	29h	Redirection Table Entry 9 (RTE9)—Offset 22h	0h
24h	2Bh	Redirection Table Entry 10 (RTE10)—Offset 24h	0h
26h	2Dh	Redirection Table Entry 11 (RTE11)—Offset 26h	0h
28h	2Fh	Redirection Table Entry 12 (RTE12)—Offset 28h	0h
2Ah	31h	Redirection Table Entry 13 (RTE13)—Offset 2Ah	0h
2Ch	33h	Redirection Table Entry 14 (RTE14)—Offset 2Ch	0h
2Eh	35h	Redirection Table Entry 15 (RTE15)—Offset 2Eh	0h
30h	37h	Redirection Table Entry 16 (RTE16)—Offset 30h	0h
32h	39h	Redirection Table Entry 17 (RTE17)—Offset 32h	0h
34h	3Bh	Redirection Table Entry 18 (RTE18)—Offset 34h	0h

Table 25-1. Summary of APIC Indirect Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
36h	3Dh	Redirection Table Entry 19 (RTE19)—Offset 36h	0h
38h	3Fh	Redirection Table Entry 20 (RTE20)—Offset 38h	0h
3Ah	41h	Redirection Table Entry 21 (RTE21)—Offset 3Ah	0h
3Ch	43h	Redirection Table Entry 22 (RTE22)—Offset 3Ch	0h
3Eh	45h	Redirection Table Entry 23 (RTE23)—Offset 3Eh	0h
40h	47h	Redirection Table Entry 24 (RTE24)—Offset 40h	0h
42h	49h	Redirection Table Entry 25 (RTE25)—Offset 42h	0h
44h	4Bh	Redirection Table Entry 26 (RTE26)—Offset 44h	0h
46h	4Dh	Redirection Table Entry 27 (RTE27)—Offset 46h	0h
48h	4Fh	Redirection Table Entry 28 (RTE28)—Offset 48h	0h
4Ah	51h	Redirection Table Entry 29 (RTE29)—Offset 4Ah	0h
4Ch	53h	Redirection Table Entry 30 (RTE30)—Offset 4Ch	0h
4Eh	55h	Redirection Table Entry 31 (RTE31)—Offset 4Eh	0h
50h	57h	Redirection Table Entry 32 (RTE32)—Offset 50h	0h
52h	59h	Redirection Table Entry 33 (RTE33)—Offset 52h	0h
54h	5Bh	Redirection Table Entry 34 (RTE34)—Offset 54h	0h
56h	5Dh	Redirection Table Entry 35 (RTE35)—Offset 56h	0h
58h	5Fh	Redirection Table Entry 36 (RTE36)—Offset 58h	0h
5Ah	61h	Redirection Table Entry 37 (RTE37)—Offset 5Ah	0h
5Ch	63h	Redirection Table Entry 38 (RTE38)—Offset 5Ch	0h
5Eh	65h	Redirection Table Entry 39 (RTE39)—Offset 5Eh	0h
60h	67h	Redirection Table Entry 40 (RTE40)—Offset 60h	0h
62h	69h	Redirection Table Entry 41 (RTE41)—Offset 62h	0h
64h	6Bh	Redirection Table Entry 42 (RTE42)—Offset 64h	0h
66h	6Dh	Redirection Table Entry 43 (RTE43)—Offset 66h	0h
68h	6Fh	Redirection Table Entry 44 (RTE44)—Offset 68h	0h
6Ah	71h	Redirection Table Entry 45 (RTE45)—Offset 6Ah	0h
6Ch	73h	Redirection Table Entry 46 (RTE46)—Offset 6Ch	0h
6Eh	75h	Redirection Table Entry 47 (RTE47)—Offset 6Eh	0h
70h	77h	Redirection Table Entry 48 (RTE48)—Offset 70h	0h
72h	79h	Redirection Table Entry 49 (RTE49)—Offset 72h	0h
74h	7Bh	Redirection Table Entry 50 (RTE50)—Offset 74h	0h
76h	7Dh	Redirection Table Entry 51 (RTE51)—Offset 76h	0h
78h	7Fh	Redirection Table Entry 52 (RTE52)—Offset 78h	0h
7Ah	81h	Redirection Table Entry 53 (RTE53)—Offset 7Ah	0h
7Ch	83h	Redirection Table Entry 54 (RTE54)—Offset 7Ch	0h
7Eh	85h	Redirection Table Entry 55 (RTE55)—Offset 7Eh	0h
80h	87h	Redirection Table Entry 56 (RTE56)—Offset 80h	0h
82h	89h	Redirection Table Entry 57 (RTE57)—Offset 82h	0h
84h	8Bh	Redirection Table Entry 58 (RTE58)—Offset 84h	0h

Table 25-1. Summary of APIC Indirect Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
86h	8Dh	Redirection Table Entry 59 (RTE59)—Offset 86h	0h
88h	8Fh	Redirection Table Entry 60 (RTE60)—Offset 88h	0h
8Ah	91h	Redirection Table Entry 61 (RTE61)—Offset 8Ah	0h
8Ch	93h	Redirection Table Entry 62 (RTE62)—Offset 8Ch	0h
8Eh	95h	Redirection Table Entry 63 (RTE63)—Offset 8Eh	0h
90h	97h	Redirection Table Entry 64 (RTE64)—Offset 90h	0h
92h	99h	Redirection Table Entry 65 (RTE65)—Offset 92h	0h
94h	9Bh	Redirection Table Entry 66 (RTE66)—Offset 94h	0h
96h	9Dh	Redirection Table Entry 67 (RTE67)—Offset 96h	0h
98h	9Fh	Redirection Table Entry 68 (RTE68)—Offset 98h	0h
9Ah	A1h	Redirection Table Entry 69 (RTE69)—Offset 9Ah	0h
9Ch	A3h	Redirection Table Entry 70 (RTE70)—Offset 9Ch	0h
9Eh	A5h	Redirection Table Entry 71 (RTE71)—Offset 9Eh	0h
A0h	A7h	Redirection Table Entry 72 (RTE72)—Offset A0h	0h
A2h	A9h	Redirection Table Entry 73 (RTE73)—Offset A2h	0h
A4h	ABh	Redirection Table Entry 74 (RTE74)—Offset A4h	0h
A6h	ADh	Redirection Table Entry 75 (RTE75)—Offset A6h	0h
A8h	AFh	Redirection Table Entry 76 (RTE76)—Offset A8h	0h
AAh	B1h	Redirection Table Entry 77 (RTE77)—Offset AAh	0h
ACh	B3h	Redirection Table Entry 78 (RTE78)—Offset ACh	0h
AEh	B5h	Redirection Table Entry 79 (RTE79)—Offset AEh	0h
B0h	B7h	Redirection Table Entry 80 (RTE80)—Offset B0h	0h
B2h	B9h	Redirection Table Entry 81 (RTE81)—Offset B2h	0h
B4h	BBh	Redirection Table Entry 82 (RTE82)—Offset B4h	0h
B6h	BDh	Redirection Table Entry 83 (RTE83)—Offset B6h	0h
B8h	BFh	Redirection Table Entry 84 (RTE84)—Offset B8h	0h
BAh	C1h	Redirection Table Entry 85 (RTE85)—Offset BAh	0h
BCh	C3h	Redirection Table Entry 86 (RTE86)—Offset BCh	0h
BEh	C5h	Redirection Table Entry 87 (RTE87)—Offset BEh	0h
C0h	C7h	Redirection Table Entry 88 (RTE88)—Offset C0h	0h
C2h	C9h	Redirection Table Entry 89 (RTE89)—Offset C2h	0h
C4h	CBh	Redirection Table Entry 90 (RTE90)—Offset C4h	0h
C6h	CDh	Redirection Table Entry 91 (RTE91)—Offset C6h	0h
C8h	CFh	Redirection Table Entry 92 (RTE92)—Offset C8h	0h
CAh	D1h	Redirection Table Entry 93 (RTE93)—Offset CAh	0h
CCh	D3h	Redirection Table Entry 94 (RTE94)—Offset CCh	0h
CEh	D5h	Redirection Table Entry 95 (RTE95)—Offset CEh	0h
D0h	D7h	Redirection Table Entry 96 (RTE96)—Offset D0h	0h
D2h	D9h	Redirection Table Entry 97 (RTE97)—Offset D2h	0h
D4h	DBh	Redirection Table Entry 98 (RTE98)—Offset D4h	0h

Table 25-1. Summary of APIC Indirect Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
D6h	DDh	Redirection Table Entry 99 (RTE99)—Offset D6h	0h
D8h	DFh	Redirection Table Entry 100 (RTE100)—Offset D8h	0h
DAh	E1h	Redirection Table Entry 101 (RTE101)—Offset DAh	0h
DCh	E3h	Redirection Table Entry 102 (RTE102)—Offset DCh	0h
DEh	E5h	Redirection Table Entry 103 (RTE103)—Offset DEh	0h
E0h	E7h	Redirection Table Entry 104 (RTE104)—Offset E0h	0h
E2h	E9h	Redirection Table Entry 105 (RTE105)—Offset E2h	0h
E4h	EBh	Redirection Table Entry 106 (RTE106)—Offset E4h	0h
E6h	EDh	Redirection Table Entry 107 (RTE107)—Offset E6h	0h
E8h	EFh	Redirection Table Entry 108 (RTE108)—Offset E8h	0h
EAh	F1h	Redirection Table Entry 109 (RTE109)—Offset EAh	0h
ECh	F3h	Redirection Table Entry 110 (RTE110)—Offset ECh	0h
EEh	F5h	Redirection Table Entry 111 (RTE111)—Offset EEh	0h
F0h	F7h	Redirection Table Entry 112 (RTE112)—Offset F0h	0h
F2h	F9h	Redirection Table Entry 113 (RTE113)—Offset F2h	0h
F4h	FBh	Redirection Table Entry 114 (RTE114)—Offset F4h	0h
F6h	FDh	Redirection Table Entry 115 (RTE115)—Offset F6h	0h
F8h	FFh	Redirection Table Entry 116 (RTE116)—Offset F8h	0h
FAh	101h	Redirection Table Entry 117 (RTE117)—Offset FAh	0h
FCh	103h	Redirection Table Entry 118 (RTE118)—Offset FCh	0h
FEh	105h	Redirection Table Entry 119 (RTE119)—Offset FEh	0h

25.1.1 Identification Register (ID)—Offset 0h

This APIC ID serves as a physical name of the APIC. The APIC bus arbitration ID for the APIC is derived from its I/O APIC ID. This register is reset to 0 on power-up reset.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:24	0h RW	**APIC Identification (AID):** Software must program this value before using the APIC.

Bit Range	Default and Access	Field Name (ID): Description
23:16	0h RO	Reserved.
15	0h RW	**Scratchpad (SPD):** Scratchpad Field
14:0	0h RO	Reserved.

25.1.2 Version Register (VER)—Offset 1h

Each I/O APIC contains a hardwired Version Register that identifies different implementation of APIC and their versions. The maximum redirection entry information is also in this register to let software know how many interrupt are supported by this APIC.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 770020h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:16	77h RW/O	**Maximum Redirection Entries (MRE):** This is the entry number (0 being the lowest entry) of the highest entry in the redirection table. It is equal to the number of interrupt input pins minus one and is in the range of 0 through 239. In PCH this field is defaulted to 17h to indicate 24 interrupts. This field is Read-Write-Once. BIOS must write to this field after PLTRST# to lockdown the value. This allows BIOS to utilize some of the entries for its own purpose and thus advertising fewer IOxAPIC Redirection Entries to OS. BIOS may to program this field up to 78h (maximum 120 entries).
15	0h RO	**Pin Assertion Register Supported (PRQ):** Indicate that the IOxAPIC does not implement the Pin Assertion Register.
14:8	0h RO	Reserved.
7:0	20h RO	**Version (VS):** Identifies the implementation version as IOxAPIC.

25.1.3 Redirection Table Entry 0 (RTE0)—Offset 10h

The Redirection Table has a dedicated entry for each interrupt input pin. The information in the Redirection Table is used to translate the interrupt manifestation on the corresponding interrupt pin into an APIC message.
The APIC will respond to an edge triggered interrupt as long as the interrupt is held

until after the acknowledge cycle has begun. Once the interrupt is detected, a delivery status bit internally to the I/O APIC is set. The state machine will step ahead and wait for an acknowledgement from the APIC unit that the interrupt message was sent. Only then will the I/O APIC be able to recognize a new edge on that interrupt pin. That new edge will only result in a new invocation of the handler if its acceptance by the destination APIC causes the Interrupt Request register bit to go from 0 to 1. (In other words, if the interrupt was not already pending a the destination.)

Access Method

Type: MEM Register (Size: 64 bits)

Device:
Function:

Default: 10000h

Bit Range	Default and Access	Field Name (ID): Description
63:56	0h RW	**Destination ID (DID):** Destination ID of the local APIC
55:48	0h RW	**Extended Destination ID (EDID):** These bits are sent to a local APIC only when in Processor System Bus mode. They become bits 11:4 of the address.
47:17	0h RO	Reserved.
16	1h RW	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	0h RW	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	0h RO/V	**Remote IRR (RIRR):** This is used for level triggered interrupts; its meaning is undefined for edge triggered interrupts. 0 = Reset when an EOI message is received that matches the VCT field. 1 = Set when IOxAPIC sends the level interrupt message to the CPU. Note, this bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	0h RW	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	0h RO/V	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry

Bit Range	Default and Access	Field Name (ID): Description
11	0h RW	**Destination Mode (DSM):** This field is used by the local Apic to determine whether it is the destination of the message.
10:8	0h RW	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are: Val Name Notes 000 Fixed 001 Lowest Priority 010 SMI Not supported 011 Reserved 100 NMI Not supported 101 INIT Not supported 110 Reserved 111 ExtINT
7:0	0h RW	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

25.1.4 Redirection Table Entry 1 (RTE1)—Offset 12h

This register has the same bit definition as RTE0.

25.1.5 Redirection Table Entry 2 (RTE2)—Offset 14h

This register has the same bit definition as RTE0.

25.1.6 Redirection Table Entry 3 (RTE3)—Offset 16h

This register has the same bit definition as RTE0.

25.1.7 Redirection Table Entry 4 (RTE4)—Offset 18h

This register has the same bit definition as RTE0.

25.1.8 Redirection Table Entry 5 (RTE5)—Offset 1Ah

This register has the same bit definition as RTE0.

25.1.9 Redirection Table Entry 6 (RTE6)—Offset 1Ch

This register has the same bit definition as RTE0.

25.1.10 Redirection Table Entry 7 (RTE7)—Offset 1Eh

This register has the same bit definition as RTE0.

25.1.11 Redirection Table Entry 8 (RTE8)—Offset 20h

This register has the same bit definition as RTE0.

25.1.12 Redirection Table Entry 9 (RTE9)—Offset 22h

This register has the same bit definition as RTE0.

25.1.13 Redirection Table Entry 10 (RTE10)—Offset 24h

This register has the same bit definition as RTE0.

25.1.14 Redirection Table Entry 11 (RTE11)—Offset 26h

This register has the same bit definition as RTE0.

25.1.15 Redirection Table Entry 12 (RTE12)—Offset 28h

This register has the same bit definition as RTE0.

25.1.16 Redirection Table Entry 13 (RTE13)—Offset 2Ah

This register has the same bit definition as RTE0.

25.1.17 Redirection Table Entry 14 (RTE14)—Offset 2Ch

This register has the same bit definition as RTE0.

25.1.18 Redirection Table Entry 15 (RTE15)—Offset 2Eh

This register has the same bit definition as RTE0.

25.1.19 Redirection Table Entry 16 (RTE16)—Offset 30h

This register has the same bit definition as RTE0.

25.1.20 Redirection Table Entry 17 (RTE17)—Offset 32h

This register has the same bit definition as RTE0.

25.1.21 Redirection Table Entry 18 (RTE18)—Offset 34h

This register has the same bit definition as RTE0.

25.1.22 Redirection Table Entry 19 (RTE19)—Offset 36h

This register has the same bit definition as RTE0.

25.1.23 Redirection Table Entry 20 (RTE20)—Offset 38h

This register has the same bit definition as RTE0.

25.1.24 Redirection Table Entry 21 (RTE21)—Offset 3Ah

This register has the same bit definition as RTE0.

25.1.25 Redirection Table Entry 22 (RTE22)—Offset 3Ch

This register has the same bit definition as RTE0.

25.1.26 Redirection Table Entry 23 (RTE23)—Offset 3Eh

This register has the same bit definition as RTE0.

25.1.27 Redirection Table Entry 24 (RTE24)—Offset 40h

This register has the same bit definition as RTE0.

25.1.28 Redirection Table Entry 25 (RTE25)—Offset 42h

This register has the same bit definition as RTE0.

25.1.29 Redirection Table Entry 26 (RTE26)—Offset 44h

This register has the same bit definition as RTE0.

25.1.30 Redirection Table Entry 27 (RTE27)—Offset 46h

This register has the same bit definition as RTE0.

25.1.31 Redirection Table Entry 28 (RTE28)—Offset 48h

This register has the same bit definition as RTE0.

25.1.32 Redirection Table Entry 29 (RTE29)—Offset 4Ah

This register has the same bit definition as RTE0.

25.1.33 Redirection Table Entry 30 (RTE30)—Offset 4Ch

This register has the same bit definition as RTE0.

25.1.34 Redirection Table Entry 31 (RTE31)—Offset 4Eh

This register has the same bit definition as RTE0.

25.1.35 Redirection Table Entry 32 (RTE32)—Offset 50h

This register has the same bit definition as RTE0.

25.1.36 Redirection Table Entry 33 (RTE33)—Offset 52h

This register has the same bit definition as RTE0.

25.1.37 Redirection Table Entry 34 (RTE34)—Offset 54h

This register has the same bit definition as RTE0.

25.1.38 Redirection Table Entry 35 (RTE35)—Offset 56h

This register has the same bit definition as RTE0.

25.1.39 Redirection Table Entry 36 (RTE36)—Offset 58h

This register has the same bit definition as RTE0.

25.1.40 Redirection Table Entry 37 (RTE37)—Offset 5Ah

This register has the same bit definition as RTE0.

25.1.41 Redirection Table Entry 38 (RTE38)—Offset 5Ch

This register has the same bit definition as RTE0.

25.1.42 Redirection Table Entry 39 (RTE39)—Offset 5Eh

This register has the same bit definition as RTE0.

25.1.43 Redirection Table Entry 40 (RTE40)—Offset 60h

This register has the same bit definition as RTE0.

25.1.44 Redirection Table Entry 41 (RTE41)—Offset 62h

This register has the same bit definition as RTE0.

25.1.45 Redirection Table Entry 42 (RTE42)—Offset 64h

This register has the same bit definition as RTE0.

25.1.46 Redirection Table Entry 43 (RTE43)—Offset 66h

This register has the same bit definition as RTE0.

25.1.47 Redirection Table Entry 44 (RTE44)—Offset 68h

This register has the same bit definition as RTE0.

25.1.48 Redirection Table Entry 45 (RTE45)—Offset 6Ah

This register has the same bit definition as RTE0.

25.1.49 Redirection Table Entry 46 (RTE46)—Offset 6Ch

This register has the same bit definition as RTE0.

25.1.50 Redirection Table Entry 47 (RTE47)—Offset 6Eh

This register has the same bit definition as RTE0.

25.1.51 Redirection Table Entry 48 (RTE48)—Offset 70h

This register has the same bit definition as RTE0.

25.1.52 Redirection Table Entry 49 (RTE49)—Offset 72h

This register has the same bit definition as RTE0.

25.1.53 Redirection Table Entry 50 (RTE50)—Offset 74h

This register has the same bit definition as RTE0.

25.1.54 Redirection Table Entry 51 (RTE51)—Offset 76h

This register has the same bit definition as RTE0.

25.1.55 Redirection Table Entry 52 (RTE52)—Offset 78h

This register has the same bit definition as RTE0.

25.1.56 Redirection Table Entry 53 (RTE53)—Offset 7Ah

This register has the same bit definition as RTE0.

25.1.57 Redirection Table Entry 54 (RTE54)—Offset 7Ch

This register has the same bit definition as RTE0.

25.1.58 Redirection Table Entry 55 (RTE55)—Offset 7Eh

This register has the same bit definition as RTE0.

25.1.59 Redirection Table Entry 56 (RTE56)—Offset 80h

This register has the same bit definition as RTE0.

25.1.60 Redirection Table Entry 57 (RTE57)—Offset 82h

This register has the same bit definition as RTE0.

25.1.61 Redirection Table Entry 58 (RTE58)—Offset 84h

This register has the same bit definition as RTE0.

25.1.62 Redirection Table Entry 59 (RTE59)—Offset 86h

This register has the same bit definition as RTE0.

25.1.63 Redirection Table Entry 60 (RTE60)—Offset 88h

This register has the same bit definition as RTE0.

25.1.64 Redirection Table Entry 61 (RTE61)—Offset 8Ah

This register has the same bit definition as RTE0.

25.1.65 Redirection Table Entry 62 (RTE62)—Offset 8Ch

This register has the same bit definition as RTE0.

25.1.66 Redirection Table Entry 63 (RTE63)—Offset 8Eh

This register has the same bit definition as RTE0.

25.1.67 Redirection Table Entry 64 (RTE64)—Offset 90h

This register has the same bit definition as RTE0.

25.1.68 Redirection Table Entry 65 (RTE65)—Offset 92h

This register has the same bit definition as RTE0.

25.1.69 Redirection Table Entry 66 (RTE66)—Offset 94h

This register has the same bit definition as RTE0.

25.1.70 Redirection Table Entry 67 (RTE67)—Offset 96h

This register has the same bit definition as RTE0.

25.1.71 Redirection Table Entry 68 (RTE68)—Offset 98h

This register has the same bit definition as RTE0.

25.1.72 Redirection Table Entry 69 (RTE69)—Offset 9Ah

This register has the same bit definition as RTE0.

25.1.73 Redirection Table Entry 70 (RTE70)—Offset 9Ch

This register has the same bit definition as RTE0.

25.1.74 Redirection Table Entry 71 (RTE71)—Offset 9Eh

This register has the same bit definition as RTE0.

25.1.75 Redirection Table Entry 72 (RTE72)—Offset A0h

This register has the same bit definition as RTE0.

25.1.76 Redirection Table Entry 73 (RTE73)—Offset A2h

This register has the same bit definition as RTE0.

25.1.77 Redirection Table Entry 74 (RTE74)—Offset A4h

This register has the same bit definition as RTE0.

25.1.78 Redirection Table Entry 75 (RTE75)—Offset A6h

This register has the same bit definition as RTE0.

25.1.79 Redirection Table Entry 76 (RTE76)—Offset A8h

This register has the same bit definition as RTE0.

25.1.80 Redirection Table Entry 77 (RTE77)—Offset AAh

This register has the same bit definition as RTE0.

25.1.81 Redirection Table Entry 78 (RTE78)—Offset ACh

This register has the same bit definition as RTE0.

25.1.82 Redirection Table Entry 79 (RTE79)—Offset AEh

This register has the same bit definition as RTE0.

25.1.83 Redirection Table Entry 80 (RTE80)—Offset B0h

This register has the same bit definition as RTE0.

25.1.84 Redirection Table Entry 81 (RTE81)—Offset B2h

This register has the same bit definition as RTE0.

25.1.85 Redirection Table Entry 82 (RTE82)—Offset B4h

This register has the same bit definition as RTE0.

25.1.86 Redirection Table Entry 83 (RTE83)—Offset B6h

This register has the same bit definition as RTE0.

25.1.87 Redirection Table Entry 84 (RTE84)—Offset B8h

This register has the same bit definition as RTE0.

25.1.88 Redirection Table Entry 85 (RTE85)—Offset BAh

This register has the same bit definition as RTE0.

25.1.89 Redirection Table Entry 86 (RTE86)—Offset BCh

This register has the same bit definition as RTE0.

25.1.90 Redirection Table Entry 87 (RTE87)—Offset BEh

This register has the same bit definition as RTE0.

25.1.91 Redirection Table Entry 88 (RTE88)—Offset C0h

This register has the same bit definition as RTE0.

25.1.92 Redirection Table Entry 89 (RTE89)—Offset C2h

This register has the same bit definition as RTE0.

25.1.93 Redirection Table Entry 90 (RTE90)—Offset C4h

This register has the same bit definition as RTE0.

25.1.94 Redirection Table Entry 91 (RTE91)—Offset C6h

This register has the same bit definition as RTE0.

25.1.95 Redirection Table Entry 92 (RTE92)—Offset C8h

This register has the same bit definition as RTE0.

25.1.96 Redirection Table Entry 93 (RTE93)—Offset CAh

This register has the same bit definition as RTE0.

25.1.97 Redirection Table Entry 94 (RTE94)—Offset CCh

This register has the same bit definition as RTE0.

25.1.98 Redirection Table Entry 95 (RTE95)—Offset CEh

This register has the same bit definition as RTE0.

25.1.99 Redirection Table Entry 96 (RTE96)—Offset D0h

This register has the same bit definition as RTE0.

25.1.100 Redirection Table Entry 97 (RTE97)—Offset D2h

This register has the same bit definition as RTE0.

25.1.101 Redirection Table Entry 98 (RTE98)—Offset D4h

This register has the same bit definition as RTE0.

25.1.102 Redirection Table Entry 99 (RTE99)—Offset D6h

This register has the same bit definition as RTE0.

25.1.103 Redirection Table Entry 100 (RTE100)—Offset D8h

This register has the same bit definition as RTE0.

25.1.104 Redirection Table Entry 101 (RTE101)—Offset DAh

This register has the same bit definition as RTE0.

25.1.105 Redirection Table Entry 102 (RTE102)—Offset DCh

This register has the same bit definition as RTE0.

25.1.106 Redirection Table Entry 103 (RTE103)—Offset DEh

This register has the same bit definition as RTE0.

25.1.107 Redirection Table Entry 104 (RTE104)—Offset E0h

This register has the same bit definition as RTE0.

25.1.108 Redirection Table Entry 105 (RTE105)—Offset E2h

This register has the same bit definition as RTE0.

25.1.109 Redirection Table Entry 106 (RTE106)—Offset E4h

This register has the same bit definition as RTE0.

25.1.110 Redirection Table Entry 107 (RTE107)—Offset E6h

This register has the same bit definition as RTE0.

25.1.111 Redirection Table Entry 108 (RTE108)—Offset E8h

This register has the same bit definition as RTE0.

25.1.112 Redirection Table Entry 109 (RTE109)—Offset EAh

This register has the same bit definition as RTE0.

25.1.113 Redirection Table Entry 110 (RTE110)—Offset ECh

This register has the same bit definition as RTE0.

25.1.114 Redirection Table Entry 111 (RTE111)—Offset EEh

This register has the same bit definition as RTE0.

25.1.115 Redirection Table Entry 112 (RTE112)—Offset F0h

This register has the same bit definition as RTE0.

25.1.116 Redirection Table Entry 113 (RTE113)—Offset F2h

This register has the same bit definition as RTE0.

25.1.117 Redirection Table Entry 114 (RTE114)—Offset F4h

This register has the same bit definition as RTE0.

25.1.118 Redirection Table Entry 115 (RTE115)—Offset F6h

This register has the same bit definition as RTE0.

25.1.119 Redirection Table Entry 116 (RTE116)—Offset F8h

This register has the same bit definition as RTE0.

25.1.120 Redirection Table Entry 117 (RTE117)—Offset FAh

This register has the same bit definition as RTE0.

25.1.121 Redirection Table Entry 118 (RTE118)—Offset FCh

This register has the same bit definition as RTE0.

25.1.122 Redirection Table Entry 119 (RTE119)—Offset FEh

This register has the same bit definition as RTE0.

25.2 Advanced Programmable Interrupt Controller (APIC) Registers Summary

Table 25-2. Summary of Advanced Programmable Interrupt Controller (APIC) Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
FEC00000h	FEC00003h	Index Register (IDX)—Offset FEC00000h	0h
FEC00010h	FEC00013h	Data Register (DAT)—Offset FEC00010h	0h
FEC00040h	FEC00043h	EOI Register (EOI)—Offset FEC00040h	0h

25.2.1 Index Register (IDX)—Offset FEC00000h

The Index Register will select which APIC indirect register to be manipulated by software. Software will program this register to select the desired APIC internal register.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h RW	**Index Register (IDX):** This is an 8 bit pointer into the I/O APIC register table.

25.2.2 Data Register (DAT)—Offset FEC00010h

This 32-bit register specifies the data to be read or written to the register pointed to by the Index register. This register can be accessed only in DW quantities.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW/V	**Window Register (WDW):** This is a 32-bit register for the data to be read or written to the APIC indirect register pointed to by the Index register (Memory Address FEC0_0000h).

25.2.3 EOI Register (EOI)—Offset FEC00040h

When a write is issued to this register, the IOxAPIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, RTE.RIRR for that entry will be cleared. If multiple entries have the same vector, each of those entries will have RTE.RIRR cleared. Only bits 7:0 are used. Bits 31:8 are ignored.

Access Method

Type: MEM Register (Size: 32 bits)	**Device:** **Function:**

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7:0	0h WO	**EOI Register (EOI):** When a write is issued to this register, the I/O APIC will check this field and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the Remote_IRR bit for that I/O Redirection Entry will be cleared.

26 Processor Interface

26.1 Processor Interface Memory Registers Summary

Table 26-1. Summary of Processor Interface Memory Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
61h	61h	NMI Status and Control (NMI_STS_CNT)—Offset 61h	0h
70h	70h	NMI Enable (and Real Time Clock Index) (NMI_EN)—Offset 70h	80h
92h	92h	Init Register (PORT92)—Offset 92h	0h
CF9h	CF9h	Reset Control Register (RST_CNT)—Offset CF9h	0h

26.1.1 NMI Status and Control (NMI_STS_CNT)—Offset 61h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO	**SERR# NMI Source Status (SERR_NMI_STS):** This bit is set by any of the sources of the internal SERR on the PCH backbone, this includes SERR assertions forwarded from the secondary PCI bus,sssssss error from a PCIe port, Do_SERR or standard PCIe error message from DMI, or internal Bus 0 functions that generate SERR#. Bit 2 must be cleared in this register in order for this bit to be set. This interrupt source is enabled by setting bit 2 to 0. To reset the interrupt, set bit 2 to 1 and then set it to 0. This bit is read-only. When writing to port 61h, this bit must be 0.
6	0h RO	**IOCHK# NMI Source Status (IOCHK_NMI_STS):** This bit is set if an ISA agent (via SERIRQ) asserts IOCHK# and bit 3 is cleared in this register. This interrupt source is enabled by setting bit 3 to 0. To reset the interrupt, set bit 3 to 1 and then set it to 0. This bit is read-only. When writing to port 61h, this bit must be a 0.
5	0h RO	**Timer Counter 2 OUT Status (TMR2_OUT_STS):** This bit reflects the current state of the 8254 counter 2 output. Counter 2 must be programmed following any PCI reset for this bit to have a determinate value. When writing to port 61h, this bit must be a 0.
4	0h RO	Reserved.
3	0h RW	**IOCHK# NMI Enable (IOCHK_NMI_EN):** When this bit is a 1, IOCHK# NMIs are disabled and cleared. When this bit is a 0, IOCHK# NMIs are enabled.
2	0h RW	**PCI SERR# Enable (PCI_SERR_EN):** When this bit is a 1, the SERR# NMIs are disabled and cleared. When this bit is a 0, SERR# NMIs are enabled.
1	0h RW	**Speaker Data Enable (SPKR_DAT_EN):** When this bit is a 0, the SPKR output is a 0. When this bit is a 1, the SPKR output is equivalent to the Counter 2 OUT signal value.
0	0h RW	**Timer Counter 2 Enable (TIM_CNT2_EN):** When this bit is a 0, Counter 2 counting is disabled. Counting is enabled when this bit is 1.

26.1.2 NMI Enable (and Real Time Clock Index) (NMI_EN)—Offset 70h

This register is write-only for normal operation. In Alt-Access mode, this register can be read to find the NMI Enable status and the RTC index value.

Access Method

Type: IO Register (Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW/V	**NMI_EN# (NMI_EN):** When this bit is a 1, all NMI sources are disabled. When this bit is a 0, NMI sources are enabled.
6:0	0h RW/V	**Real Time Clock Index (Address) (RTC_INDX):** This data goes to the RTC to select which register or CMOS RAM address is being accessed.

26.1.3 Init Register (PORT92)—Offset 92h

Access Method

Type: IO Register (Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:1	0h RO	Reserved.
0	0h RW	**INIT NOW (INIT_NOW):** When this bit transitions from a 0 to a 1, the PCH will force INIT# active for 16 PCI clocks.

26.1.4 Reset Control Register (RST_CNT)—Offset CF9h

Access Method

Type: IO Register (Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:4	0h RO	Reserved.
3	0h RW	**Full Reset (FULL_RST):** When this bit is set to 1 and bit 1 is set to 1 (indicating Hard Reset, not Soft Reset), and the RST_CPU bit (bit 2) is written from 0 to 1, the PCH will do a full reset, including driving SLP_S3#, SLP_S4# and SLP_S5# active (low) for at least 3 (and no more than 5) seconds. When this bit is set, it also causes the full power cycle (SLP_S3/4/5# assertion) in response to SYSRESET#, PWROK#, and Watchdog timer reset sources.
2	0h RW	**Reset CPU (RST_CPU):** This bit will cause either a hard or soft reset to the CPU depending on the state of the SYS_RST bit (bit 1 in this same register). The software will cause the reset by setting bit 2 from a 0 to a 1.
1	0h RW	**System Reset (SYS_RST):** The bit determines the type of reset caused via RST_CPU (bit 2 of this register). If SYS_RST is 0 when RST_CPU goes from 0 to 1, then the PCH will force INIT# active for 16 PCI clocks. If SYS_RST is 1 when RST_CPU goes from 0 to 1, then the PCH will force PCI reset active for about 1 ms, however the SLP_S3#, SLP_S4# and SLP_S5# signals assertion is dependent on the value of the FULL_RST (bit3 of this register).
0	0h RO	Reserved.

27 General Purpose I/O (GPIO)

27.1 GPIO Community 0 Registers Summary

GPIO pins are grouped into different Community (e.g. Community 0, Community 1, etc.). Each Community consists of one or more GPIO groups.

This section covers registers for Community 0, which consists of GPP_A, GPP_B, and GPP_T groups.

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).
Note that each GPIO Community has a different PortID. See the Primary to Sideband Bridge Section in Vol1 for PortID info.

Table 10. Summary of GPIO Community 0 Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8h	Bh	Family Base Address (FAMBAR)—Offset 8h	300h
Ch	Fh	Pad Base Address (PADBAR)—Offset Ch	700h
10h	13h	Miscellaneous Configuration (MISCCFG)—Offset 10h	32043200h
20h	23h	Pad Ownership (PAD_OWN_GPP_B_0)—Offset 20h	0h
24h	27h	Pad Ownership (PAD_OWN_GPP_B_1)—Offset 24h	0h
28h	2Bh	Pad Ownership (PAD_OWN_GPP_B_2)—Offset 28h	0h
30h	33h	Pad Ownership (PAD_OWN_GPP_T_0)—Offset 30h	0h
38h	3Bh	Pad Ownership (PAD_OWN_GPP_A_0)—Offset 38h	0h
3Ch	3Fh	Pad Ownership (PAD_OWN_GPP_A_1)—Offset 3Ch	0h
40h	43h	Pad Ownership (PAD_OWN_GPP_A_2)—Offset 40h	0h
80h	83h	Pad Configuration Lock (PADCFGLOCK_GPP_B_0)—Offset 80h	0h
84h	87h	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_B_0)—Offset 84h	0h
88h	8Bh	Pad Configuration Lock (PADCFGLOCK_GPP_T_0)—Offset 88h	0h
8Ch	8Fh	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_T_0)—Offset 8Ch	0h
90h	93h	Pad Configuration Lock (PADCFGLOCK_GPP_A_0)—Offset 90h	0h
94h	97h	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_A_0)—Offset 94h	0h
B0h	B3h	Host Software Pad Ownership (HOSTSW_OWN_GPP_B_0)—Offset B0h	0h
B4h	B7h	Host Software Pad Ownership (HOSTSW_OWN_GPP_T_0)—Offset B4h	0h
B8h	BBh	Host Software Pad Ownership (HOSTSW_OWN_GPP_A_0)—Offset B8h	0h
100h	103h	GPI Interrupt Status (GPI_IS_GPP_B_0)—Offset 100h	0h
104h	107h	GPI Interrupt Status (GPI_IS_GPP_T_0)—Offset 104h	0h
108h	10Bh	GPI Interrupt Status (GPI_IS_GPP_A_0)—Offset 108h	0h
120h	123h	GPI Interrupt Enable (GPI_IE_GPP_B_0)—Offset 120h	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
124h	127h	GPI Interrupt Enable (GPI_IE_GPP_T_0)—Offset 124h	0h
128h	12Bh	GPI Interrupt Enable (GPI_IE_GPP_A_0)—Offset 128h	0h
140h	143h	GPI General Purpose Events Status (GPI_GPE_STS_GPP_B_0)—Offset 140h	0h
144h	147h	GPI General Purpose Events Status (GPI_GPE_STS_GPP_T_0)—Offset 144h	0h
148h	14Bh	GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_0)—Offset 148h	0h
160h	163h	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_B_0)—Offset 160h	0h
164h	167h	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_T_0)—Offset 164h	0h
168h	16Bh	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_0)—Offset 168h	0h
180h	183h	SMI Status (GPI_SMI_STS_GPP_B_0)—Offset 180h	0h
1A0h	1A3h	SMI Enable (GPI_SMI_EN_GPP_B_0)—Offset 1A0h	0h
1C0h	1C3h	NMI Status (GPI_NMI_STS_GPP_B_0)—Offset 1C0h	0h
1E0h	1E3h	NMI Enable (GPI_NMI_EN_GPP_B_0)—Offset 1E0h	0h
700h	703h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_0)—Offset 700h	4400XX00h See register for X value
704h	707h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_0)—Offset 704h	18h
710h	713h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_1)—Offset 710h	4400XX00h See register for X value
714h	717h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_1)—Offset 714h	19h
720h	723h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_2)—Offset 720h	4400XX00h See register for X value
724h	727h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_2)—Offset 724h	1Ah
730h	733h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_3)—Offset 730h	4400XX00h See register for X value
734h	737h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_3)—Offset 734h	1Bh
740h	743h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_4)—Offset 740h	4400XX00h See register for X value
744h	747h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_4)—Offset 744h	1Ch
750h	753h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_5)—Offset 750h	4400XX00h See register for X value
754h	757h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_5)—Offset 754h	1Dh
760h	763h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_6)—Offset 760h	4400XX00h See register for X value
764h	767h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_6)—Offset 764h	1Eh
770h	773h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_7)—Offset 770h	4400XX00h See register for X value
774h	777h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_7)—Offset 774h	1Fh

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
780h	783h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_8)—Offset 780h	4400XX00h See register for X value
784h	787h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_8)—Offset 784h	20h
790h	793h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_9)—Offset 790h	4400XX00h See register for X value
794h	797h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_9)—Offset 794h	21h
7A0h	7A3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_10)—Offset 7A0h	4400XX00h See register for X value
7A4h	7A7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_10)—Offset 7A4h	22h
7B0h	7B3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_11)—Offset 7B0h	4400XX00h See register for X value
7B4h	7B7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_11)—Offset 7B4h	23h
7C0h	7C3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_12)—Offset 7C0h	4400XX00h See register for X value
7C4h	7C7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_12)—Offset 7C4h	24h
7D0h	7D3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_13)—Offset 7D0h	4400XX00h See register for X value
7D4h	7D7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_13)—Offset 7D4h	25h
7E0h	7E3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_14)—Offset 7E0h	4400XX00h See register for X value
7E4h	7E7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_14)—Offset 7E4h	26h
7F0h	7F3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_15)—Offset 7F0h	4400XX00h See register for X value
7F4h	7F7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_15)—Offset 7F4h	27h
800h	803h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_16)—Offset 800h	4400XX00h See register for X value
804h	807h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_16)—Offset 804h	28h
810h	813h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_17)—Offset 810h	4400XX00h See register for X value
814h	817h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_17)—Offset 814h	29h
820h	823h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_18)—Offset 820h	4400XX00h See register for X value
824h	827h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_18)—Offset 824h	2Ah
830h	833h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_19)—Offset 830h	4400XX00h See register for X value
834h	837h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_19)—Offset 834h	2Bh
840h	843h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_20)—Offset 840h	4400XX00h See register for X value
844h	847h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_20)—Offset 844h	2Ch

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
850h	853h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_21)—Offset 850h	4400XX00h See register for X value
854h	857h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_21)—Offset 854h	2Dh
860h	863h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_22)—Offset 860h	4400XX00h See register for X value
864h	867h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_22)—Offset 864h	2Eh
870h	873h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_23)—Offset 870h	4400XX00h See register for X value
874h	877h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_23)—Offset 874h	2Fh
8C0h	8C3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_2)—Offset 8C0h	4400XX00h See register for X value
8C4h	8C7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_2)—Offset 8C4h	1032h
8D0h	8D3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_3)—Offset 8D0h	4400XX00h See register for X value
8D4h	8D7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_3)—Offset 8D4h	1033h
9A0h	9A3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_0)—Offset 9A0h	4400XX00h See register for X value
9A4h	9A7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_0)—Offset 9A4h	3040h
9B0h	9B3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_1)—Offset 9B0h	4400XX00h See register for X value
9B4h	9B7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_1)—Offset 9B4h	3041h
9C0h	9C3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_2)—Offset 9C0h	4400XX00h See register for X value
9C4h	9C7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_2)—Offset 9C4h	3042h
9D0h	9D3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_3)—Offset 9D0h	4400XX00h See register for X value
9D4h	9D7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_3)—Offset 9D4h	3043h
9E0h	9E3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_4)—Offset 9E0h	4400XX00h See register for X value
9E4h	9E7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_4)—Offset 9E4h	3044h
9F0h	9F3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_5)—Offset 9F0h	4400XX00h See register for X value
9F4h	9F7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_5)—Offset 9F4h	1045h
A00h	A03h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_6)—Offset A00h	4400XX00h See register for X value
A04h	A07h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_6)—Offset A04h	46h
A10h	A13h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_7)—Offset A10h	4400XX00h See register for X value
A14h	A17h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_7)—Offset A14h	47h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
A20h	A23h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_8)—Offset A20h	4400XX00h See register for X value
A24h	A27h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_8)—Offset A24h	48h
A30h	A33h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_9)—Offset A30h	4400XX00h See register for X value
A34h	A37h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_9)—Offset A34h	49h
A40h	A43h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_10)—Offset A40h	4400XX00h See register for X value
A44h	A47h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_10)—Offset A44h	4Ah
A50h	A53h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_11)—Offset A50h	4400XX00h See register for X value
A54h	A57h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_11)—Offset A54h	4Bh
A60h	A63h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_12)—Offset A60h	4400XX00h See register for X value
A64h	A67h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_12)—Offset A64h	4Ch
A70h	A73h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_13)—Offset A70h	4400XX00h See register for X value
A74h	A77h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_13)—Offset A74h	4Dh
A80h	A83h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_14)—Offset A80h	4400XX00h See register for X value
A84h	A87h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_14)—Offset A84h	4Eh
A90h	A93h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_15)—Offset A90h	4400XX00h See register for X value
A94h	A97h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_15)—Offset A94h	4Fh
AA0h	AA3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_16)—Offset AA0h	4400XX00h See register for X value
AA4h	AA7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_16)—Offset AA4h	50h
AB0h	AB3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_17)—Offset AB0h	4400XX00h See register for X value
AB4h	AB7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_17)—Offset AB4h	51h
AC0h	AC3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_18)—Offset AC0h	4400XX00h See register for X value
AC4h	AC7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_18)—Offset AC4h	52h
AD0h	AD3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_19)—Offset AD0h	4400XX00h See register for X value
AD4h	AD7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_19)—Offset AD4h	53h
AE0h	AE3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_20)—Offset AE0h	4400XX00h See register for X value
AE4h	AE7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_20)—Offset AE4h	54h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
AF0h	AF3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_21)—Offset AF0h	4400XX00h See register for X value
AF4h	AF7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_21)—Offset AF4h	55h
B00h	B03h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_22)—Offset B00h	4400XX00h See register for X value
B04h	B07h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_22)—Offset B04h	56h
B10h	B13h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_23)—Offset B10h	4400XX00h See register for X value
B14h	B17h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_23)—Offset B14h	57h

27.1.1 Family Base Address (FAMBAR)—Offset 8h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 300h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

27.1.2 Pad Base Address (PADBAR)—Offset Ch

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 700h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	700h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

27.1.3 Miscellaneous Configuration (MISCCFG)—Offset 10h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 32043200h

Bit Range	Default & Access	Field Name (ID): Description
31:24	32h RW	**GPIO Driver Mode Interrupt Select (GPDMINTSEL):** IRQ globally for all pads (GPI_IS with corresponding GPI_IE enable). 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255
23:20	0h RO	Reserved.
19:16	4h RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[87:64]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[67:66]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[87:64]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[71:64]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[75:64]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[71:64]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[87:64]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[83:64]; other GPE bits not used. 8h = GPP_U[5:4] mapped to GPE[69:68]; other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[87:64]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[87:64]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[87:64]; other GPE bits not used. Dh - Fh: Reserved
15:12	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[55:32]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[35:34]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[55:32]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[39:32]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[43:32]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[39:32]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[55:32]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[51:32]; other GPE bits not used. 8h = GPP_U[5:4] mapped to GPE[37:36]; other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[55:32]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[55:32]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[55:32]; other GPE bits not used. Dh - Fh: Reserved

Bit Range	Default & Access	Field Name (ID): Description
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[23:0]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[3:2]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[23:0]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[7:0]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[11:0]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[7:0]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[23:0]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[19:0]; other GPE bits not used. 8h = GPP_U[5:4] mapped to GPE[5:4];other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[23:0]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[23:0]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[23:0]; other GPE bits not used. Dh - Fh: Reserved
7:2	0h RO	Reserved.
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specify whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specifies whether the GPIO Community should perform local clock gating. 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating

27.1.4 Pad Ownership (PAD_OWN_GPP_B_0)—Offset 20h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_7):** Same description as bits[1:0].
27:26	0h RO	Reserved.
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_6):** Same description as bits[1:0].
23:22	0h RO	Reserved.
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_5):** Same description as bits[1:0].
19:18	0h RO	Reserved.
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_4):** Same description as bits[1:0].

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_3):** Same description as bits[1:0].
11:10	0h RO	Reserved.
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_2):** Same description as bits[1:0].
7:6	0h RO	Reserved.
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_1):** Same description as bits[1:0].
3:2	0h RO	Reserved.
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_B_0):** 00 = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership 01 = ME GPIO Mode. ME has ownership of the pad. 10 = ISH GPIO Mode. ME has ownership of the pad 11 = Reserved

27.1.5 Pad Ownership (PAD_OWN_GPP_B_1)—Offset 24h

Same description as PAD_OWN_GPP_B0, except that this register is for GPP_B[15:8]

27.1.6 Pad Ownership (PAD_OWN_GPP_B_2)—Offset 28h

Same description as PAD_OWN_GPP_B0, except that this register is for GPP_B[23:16]

27.1.7 Pad Ownership (PAD_OWN_GPP_T_0)—Offset 30h

Same description as PAD_OWN_GPP_B_0 register, except this register applies to GPP_T[3:2].
(Note: Bits corresponding to unimplemented GPP pins are reserved).

27.1.8 Pad Ownership (PAD_OWN_GPP_A_0)—Offset 38h

Same description as PAD_OWN_GPP_B0, except that this register is for GPP_A[7:0]

27.1.9 Pad Ownership (PAD_OWN_GPP_A_1)—Offset 3Ch

Same description as PAD_OWN_GPP_B0, except that this register is for GPP_A[15:8]

27.1.10 Pad Ownership (PAD_OWN_GPP_A_2)—Offset 40h

Same description as PAD_OWN_GPP_B0, except that this register is for GPP_A[23:16].

27.1.11 Pad Configuration Lock (PADCFGLOCK_GPP_B_0)—Offset 80h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_23):** Same description as bit 0.
22	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_22):** Same description as bit 0.
21	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_21):** Same description as bit 0.
20	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_20):** Same description as bit 0.
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_19):** Same description as bit 0.
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_18):** Same description as bit 0.
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_17):** Same description as bit 0.
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_16):** Same description as bit 0.
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_15):** Same description as bit 0.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_14):** Same description as bit 0.
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_13):** Same description as bit 0.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_12):** Same description as bit 0.
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_11):** Same description as bit 0.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_10):** Same description as bit 0.
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_9):** Same description as bit 0.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_8):** Same description as bit 0.
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_7):** Same description as bit 0.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_6):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_5):** Same description as bit 0.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_4):** Same description as bit 0.
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_3):** Same description as bit 0.
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_2):** Same description as bit 0.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_1):** Same description as bit 0.
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_B_0):** Pad Configuration Lock locks specific register fields in the GPP specific registers from being configured. The registers affected become Read-Only and software writes to these registers have no effect. 0 = Unlock 1 = Lock the following register fields as read-only (RO): - Pad Configuration registers (exclude GPIOTXState) - GPI_NMI_EN Register (if implemented) - GPI_SMI_EN Register (if implemented) - GPI_GPE_EN Register (if implemented) When PadCfgLock is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

27.1.12 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_B_0)—Offset 84h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_23):** Same description as bit 0.
22	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_22):** Same description as bit 0.
21	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_21):** Same description as bit 0.
20	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_20):** Same description as bit 0.
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_19):** Same description as bit 0.
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_18):** Same description as bit 0.
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_17):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_16):** Same description as bit 0.
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_15):** Same description as bit 0.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_14):** Same description as bit 0.
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_13):** Same description as bit 0.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_12):** Same description as bit 0.
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_11):** Same description as bit 0.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_10):** Same description as bit 0.
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_9):** Same description as bit 0.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_8):** Same description as bit 0.
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_7):** Same description as bit 0.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_6):** Same description as bit 0.
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_5):** Same description as bit 0.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_4):** Same description as bit 0.
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_3):** Same description as bit 0.
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_2):** Same description as bit 0.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_1):** Same description as bit 0.
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_B_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) When PadCfgLockTx is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

27.1.13 Pad Configuration Lock (PADCFGLOCK_GPP_T_0)—Offset 88h

Same description as PADCFGLOCK_GPP_B_0 register, except this register applies to GPP_T[3:2].
(Note: Bits corresponding to unimplemented GPP pins are reserved.)

27.1.14 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_T_0)—Offset 8Ch

Same description as PADCFGLOCKTX_GPP_B_0 register, except this register applies to GPP_T[3:2].
(Note: Bits corresponding to unimplemented GPP pins are reserved.)

27.1.15 Pad Configuration Lock (PADCFGLOCK_GPP_A_0)—Offset 90h

Same description as PADCFGLOCK_GPP_B_0 register, except this register applies to GPP_A[23:0].

27.1.16 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_A_0)—Offset 94h

Same description as PADCFGLOCKTX_GPP_B_0 register, except this register applies to GPP_A[23:0].

27.1.17 Host Software Pad Ownership (HOSTSW_OWN_GPP_B_0)—Offset B0h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_23):** Same description as bit 0.
22	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_22):** Same description as bit 0.
21	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_21):** Same description as bit 0.
20	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_20):** Same description as bit 0.
19	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_19):** Same description as bit 0.
18	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_18):** Same description as bit 0.
17	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_17):** Same description as bit 0.
16	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_16):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_15):** Same description as bit 0.
14	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_14):** Same description as bit 0.
13	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_13):** Same description as bit 0.
12	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_12):** Same description as bit 0.
11	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_11):** Same description as bit 0.
10	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_10):** Same description as bit 0.
9	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_9):** Same description as bit 0.
8	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_8):** Same description as bit 0.
7	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_7):** Same description as bit 0.
6	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_6):** Same description as bit 0.
5	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_5):** Same description as bit 0.
4	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_4):** Same description as bit 0.
3	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_3):** Same description as bit 0.
2	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_2):** Same description as bit 0.
1	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_1):** Same description as bit 0.
0	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_B_0):** This register determines the appropriate host status bit update when a pad is under host ownership. 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked.

27.1.18 Host Software Pad Ownership (HOSTSW_OWN_GPP_T_0)—Offset B4h

Same description as HOSTSW_OWN_GPP_B_0 register, except that this register applies to GPP_T[3:2]. (Note: bits corresponding to unimplemented GPP will be reserved.)

27.1.19 Host Software Pad Ownership (HOSTSW_OWN_GPP_A_0)—Offset B8h

Same description as HOSTSW_OWN_GPP_B_0 register, except that this register applies to GPP_A[23:0].

27.1.20 GPI Interrupt Status (GPI_IS_GPP_B_0)—Offset 100h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_23):** Same description as bit 0.
22	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_22):** Same description as bit 0.
21	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_21):** Same description as bit 0.
20	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_20):** Same description as bit 0.
19	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_19):** Same description as bit 0.
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_18):** Same description as bit 0.
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_17):** Same description as bit 0.
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_16):** Same description as bit 0.
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_15):** Same description as bit 0.
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_14):** Same description as bit 0.
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_13):** Same description as bit 0.
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_12):** Same description as bit 0.
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_11):** Same description as bit 0.
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_10):** Same description as bit 0.
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_9):** Same description as bit 0.
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_8):** Same description as bit 0.
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_7):** Same description as bit 0.
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_6):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_5):** Same description as bit 0.
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_4):** Same description as bit 0.
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_3):** Same description as bit 0.
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_2):** Same description as bit 0.
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_1):** Same description as bit 0.
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_B_0):** This bit is set to '1' by hardware when either an edge or a level event is detected on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode - HOSTSW_OWN = 1 (i.e. Host GPIO Driver Mode). Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x].

27.1.21 GPI Interrupt Status (GPI_IS_GPP_T_0)—Offset 104h

Same description GPI_IS_GPP_B_0 register, except this register applies to GPP_T[3:2]. (Note: bits corresponding to unimplemented GPP will be reserved.)

27.1.22 GPI Interrupt Status (GPI_IS_GPP_A_0)—Offset 108h

Same description GPI_IS_GPP_B_0 register, except this register applies to GPP_A[23:0].

27.1.23 GPI Interrupt Enable (GPI_IE_GPP_B_0)—Offset 120h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_23):** Same description as bit 0.
22	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_22):** Same description as bit 0.
21	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_21):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_20):** Same description as bit 0.
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_19):** Same description as bit 0.
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_18):** Same description as bit 0.
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_17):** Same description as bit 0.
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_16):** Same description as bit 0.
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_15):** Same description as bit 0.
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_14):** Same description as bit 0.
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_13):** Same description as bit 0.
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_12):** Same description as bit 0.
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_11):** Same description as bit 0.
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_10):** Same description as bit 0.
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_9):** Same description as bit 0.
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_8):** Same description as bit 0.
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_7):** Same description as bit 0.
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_6):** Same description as bit 0.
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_5):** Same description as bit 0.
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_4):** Same description as bit 0.
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_3):** Same description as bit 0.
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_2):** Same description as bit 0.
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_1):** Same description as bit 0.
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_B_0):** This bit is used to enable/ disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation

27.1.24 GPI Interrupt Enable (GPI_IE_GPP_T_0)—Offset 124h

Same description as GPI_IE_GPP_B_0 register, except that this register is for GPP_T[3:2]. (Note: bits corresponding to unimplemented GPP will be reserved.)

27.1.25 GPI Interrupt Enable (GPI_IE_GPP_A_0)—Offset 128h

Same description as GPI_IE_GPP_B_0 register, except that this register is for GPP_A[23:0].

27.1.26 GPI General Purpose Events Status (GPI_GPE_STS_GPP_B_0)—Offset 140h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_23):** Same description as bit 0.
22	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_22):** Same description as bit 0.
21	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_21):** Same description as bit 0.
20	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_20):** Same description as bit 0.
19	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_19):** Same description as bit 0.
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_18):** Same description as bit 0.
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_17):** Same description as bit 0.
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_16):** Same description as bit 0.
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_15):** Same description as bit 0.
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_14):** Same description as bit 0.
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_13):** Same description as bit 0.
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_12):** Same description as bit 0.
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_11):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_10):** Same description as bit 0.
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_9):** Same description as bit 0.
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_8):** Same description as bit 0.
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_7):** Same description as bit 0.
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_6):** Same description as bit 0.
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_5):** Same description as bit 0.
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_4):** Same description as bit 0.
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_3):** Same description as bit 0.
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_2):** Same description as bit 0.
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_1):** Same description as bit 0.
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_B_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: - If the system is in an S3-S5 state, the event will also wake the system. - If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be generated, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS.

27.1.27 GPI General Purpose Events Status (GPI_GPE_STS_GPP_T_0)—Offset 144h

Same description as PI_GPE_STS_GPP_B_0 register, except that this is for GPP_T[3:2]. (Note: Bits corresponding to unimplemented GPP pins are reserved.)

27.1.28 GPI General Purpose Events Status (GPI_GPE_STS_GPP_A_0)—Offset 148h

Same description as PI_GPE_STS_GPP_B_0 register, except that this is for GPP_A[23:0].

27.1.29 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_B_0)—Offset 160h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_23):** Same description as bit 0.
22	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_22):** Same description as bit 0.
21	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_21):** Same description as bit 0.
20	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_20):** Same description as bit 0.
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_19):** Same description as bit 0.
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_18):** Same description as bit 0.
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_17):** Same description as bit 0.
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_16):** Same description as bit 0.
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_15):** Same description as bit 0.
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_14):** Same description as bit 0.
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_13):** Same description as bit 0.
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_12):** Same description as bit 0.
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_11):** Same description as bit 0.
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_10):** Same description as bit 0.
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_9):** Same description as bit 0.
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_8):** Same description as bit 0.
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_7):** Same description as bit 0.
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_6):** Same description as bit 0.
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_5):** Same description as bit 0.
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_4):** Same description as bit 0.
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_3):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_2):** Same description as bit 0.
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_1):** Same description as bit 0.
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_B_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'.

27.1.30 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_T_0)—Offset 164h

Same description as GPI_GPE_EN_GPP_B_0, except that this is for GPP_T[3:2]. (Note: Bits corresponding to unimplemented GPP pins are reserved.)

27.1.31 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_A_0)—Offset 168h

Same description as GPI_GPE_EN_GPP_B_0, except that this is for GPP_A[23:0].

27.1.32 SMI Status (GPI_SMI_STS_GPP_B_0)—Offset 180h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_B_23):** Same description as bit 14.
22:21	0h RO	Reserved.
20	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_B_20):** Same description as bit 14.

Bit Range	Default & Access	Field Name (ID): Description
19:15	0h RO	Reserved.
14	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_B_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to 1. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is 1, bit0 of this bit is locked down to read-only.
13:0	0h RO	Reserved.

27.1.33 SMI Enable (GPI_SMI_EN_GPP_B_0)—Offset 1A0h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_23):** Same description as bit 14.
22:21	0h RO	Reserved.
20	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_20):** Same description as bit 14.
19:15	0h RO	Reserved.
14	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_B_14):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to 1. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is 1, bit0 of this bit is locked down to read-only.
13:0	0h RO	Reserved.

27.1.34 NMI Status (GPI_NMI_STS_GPP_B_0)—Offset 1C0h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_B_23):** Same description as bit 14.
22:21	0h RO	Reserved.
20	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_B_20):** Same description as bit 14.
19:15	0h RO	Reserved.
14	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_B_14):** This bit is set to 1 by hardware when an edge event is detected on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode (PMode) - The corresponding GPIONMIRout is set to 1, i.e. programmed to route as NMI - The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). - The corresponding GPI_NMI_EN is set Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = There is no NMI event 1 = There is an NMI event
13:0	0h RO	Reserved.

27.1.35 NMI Enable (GPI_NMI_EN_GPP_B_0)—Offset 1E0h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_23):** Same description as bit 14.
22:21	0h RO	Reserved.
20	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_20):** Same description as bit 14.

Bit Range	Default & Access	Field Name (ID): Description
19:15	0h RO	Reserved.
14	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_B_14):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only.
13:0	0h RO	Reserved.

27.1.36 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_0)—Offset 700h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 4400XX00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset GPIO pad register fields in various GPIO registers (PADCFGLOCK, PADCFGLOCKTX, GPI_IS, GPI_IE, GPI_GPE_STS, GPI_GPE_EN, GPI_SMI_STS, SPI_SMI_EN, GPI_NMI_STS, GPI_NMI_EN, PAD_CFG_DW0, and PAD_CFG_DW1). 00 = Global Reset or RSMRST# 01 = Host deep reset. This reset occurs when any of the following occur: Host reset (with or without power cycle) is initiated, Global reset is initiated, or Deep Sx entry. This reset does NOT occur as part of S3/S4/S5 entry. 10 = PLTRST# 11 = Global Reset
29	0h RW	**RX Pad State Select (RXPADSTSEL):** This bit determines how the RX pad state is used internally for native functions. This field is not applicable if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state 1 = RX pad state after applying RXINV, PreGfRXSel settings, or hardware debouncer (if applicable).
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field is only applicable when the pad is configured as an input in either GPIO Mode or native function mode. The override occurs before RXINV setting is applied. 0 = No Override 1 = Override to 1
27	0h RO	Reserved.
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** This bit determine if the raw RX pad state should be subjected to internal glitch filter or not. This field should only be used when the pad is configured as an input and the RX buffer is not disabled. 0 = Select non-filtered RX pad state 1 = Select filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the pad state is inverted. This field is only applicable when the RX buffer is configured as an input in either GPIO mode or native function mode. This bit does not affect GPIORXState. During host ownership GPIO mode, when this bit is set to '1', then the RX pad state is inverted before it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the native function selected by Pad Mode. This is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function defined in Pad Mode controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function defined in Pad Mode controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function defined in Pad Mode controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s). This bit only applies to a GPIO that has SMI capability. Otherwise, the bit is RO.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit. This bit only applies to a GPIO that has NMI capability. Otherwise, the bit is RO.
16:13	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
12:10	-- RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO controls the Pad 1h = Function 1, if applicable, controls the Pad ... 7h = Function 7, if applicable, controls the Pad Default value is determined by the default functionality of the pad.
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0'.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	Reserved.
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

27.1.37 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_0)—Offset 704h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 18h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved NOTES: 1.The 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily.
9:8	0h RW	Reserved.
7:0	18h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

27.1.38 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_1)—Offset 710h

This register applies to GPP_B1 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.39 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_1)—Offset 714h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 19h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	19h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.40 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_2)—Offset 720h

This register applies to GPP_B2 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.41 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_2)—Offset 724h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 1Ah

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	1Ah RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.42 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_3)—Offset 730h

This register applies to GPP_B3 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.43 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_3)—Offset 734h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 1Bh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	1Bh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.44 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_4)—Offset 740h

This register applies to GPP_B4 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.45 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_4)—Offset 744h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 1Ch

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	1Ch RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.46 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_5)—Offset 750h

This register applies to GPP_B5 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.47 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_5)—Offset 754h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 1Dh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	1Dh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.48 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_6)—Offset 760h

This register applies to GPP_B6 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.49 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_6)—Offset 764h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 1Eh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	1Eh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.50 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_7)—Offset 770h

This register applies to GPP_B7 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.51 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_7)—Offset 774h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 1Fh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	1Fh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.52 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_8)—Offset 780h

This register applies to GPP_B8 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.53 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_8)—Offset 784h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 20h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	20h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.54 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_9)—Offset 790h

This register applies to GPP_B9 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.55 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_9)—Offset 794h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 21h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	21h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.56 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_10)—Offset 7A0h

This register applies to GPP_B10 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.57 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_10)—Offset 7A4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 22h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	22h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.58 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_11)—Offset 7B0h

This register applies to GPP_B11 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.59 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_11)—Offset 7B4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 23h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	23h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.60 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_12)—Offset 7C0h

This register applies to GPP_B12 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.61 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_12)—Offset 7C4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 24h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	24h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.62 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_13)—Offset 7D0h

This register applies to GPP_B13 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.63 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_13)—Offset 7D4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 25h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	25h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.64 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_14)—Offset 7E0h

This register applies to GPP_B14 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.65 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_14)—Offset 7E4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 26h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	26h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.66 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_15)—Offset 7F0h

This register applies to GPP_B15 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.67 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_15)—Offset 7F4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 27h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	27h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.68 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_16)—Offset 800h

This register applies to GPP_B16 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.69 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_16)—Offset 804h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 28h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved
7:0	28h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.70 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_17)—Offset 810h

This register applies to GPP_B17 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.71 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_17)—Offset 814h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 29h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	29h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.72 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_18)—Offset 820h

This register applies to GPP_B18 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.73 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_18)—Offset 824h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 2Ah

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	2Ah RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.74 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_19)—Offset 830h

This register applies to GPP_B19 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.75 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_19)—Offset 834h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 2Bh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	2Bh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.76 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_20)—Offset 840h

This register applies to GPP_B20 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.77 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_20)—Offset 844h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 2Ch

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	2Ch RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.78 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_21)—Offset 850h

This register applies to GPP_B21 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.79 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_21)—Offset 854h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 2Dh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	2Dh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.80 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_22)—Offset 860h

This register applies to GPP_B22 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.81 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_22)—Offset 864h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 2Eh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	2Eh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.82 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_B_23)—Offset 870h

This register applies to GPP_B23 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.83 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_B_23)—Offset 874h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2Fh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_B_0.
9:8	0h RW	Reserved.
7:0	2Fh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_B_0.

27.1.84 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_2)—Offset 8C0h

This register applies to GPP_T2 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.85 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_2)—Offset 8C4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 1032h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	4h RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved NOTES: 1.The 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily.
9:8	0h RW	Reserved.
7:0	32h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

27.1.86 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_T_3)—Offset 8D0h

This register applies to GPP_T3 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.87 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_T_3)—Offset 8D4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 1033h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	4h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_T_2.
9:8	0h RW	Reserved.
7:0	33h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_T_2.

27.1.88 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_0)—Offset 9A0h

This register applies to GPP_A0 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.89 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_0)—Offset 9A4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 3040h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	Ch RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved NOTES: 1.The 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily.
9:8	0h RW	Reserved.
7:0	40h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

27.1.90 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_1)—Offset 9B0h

This register applies to GPP_A1 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.91 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_1)—Offset 9B4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 3041h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	Ch RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	41h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.92 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_2)—Offset 9C0h

This register applies to GPP_A2 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.93 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_2)—Offset 9C4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 3042h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	Ch RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	42h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.94 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_3)—Offset 9D0h

This register applies to GPP_A3 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.95 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_3)—Offset 9D4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 3043h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	Ch RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	43h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.96 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_4)—Offset 9E0h

This register applies to GPP_A4 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.97 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_4)—Offset 9E4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 3044h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	Ch RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	44h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.98 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_5)—Offset 9F0h

This register applies to GPP_A5 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.99 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_5)—Offset 9F4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 1045h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	4h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	45h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.100 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_6)—Offset A00h

This register applies to GPP_A6 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.101 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_6)—Offset A04h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 46h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	46h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.102 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_7)—Offset A10h

This register applies to GPP_A7 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.103 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_7)—Offset A14h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 47h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	47h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.104 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_8)—Offset A20h

This register applies to GPP_A8 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.105 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_8)—Offset A24h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 48h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	48h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.106 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_9)—Offset A30h

This register applies to GPP_A9 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.107 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_9)—Offset A34h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 49h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	49h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.108 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_10)—Offset A40h

This register applies to GPP_A10 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.109 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_10)—Offset A44h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 4Ah

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	4Ah RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.110 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_11)—Offset A50h

This register applies to GPP_A11 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.111 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_11)—Offset A54h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 4Bh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	4Bh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.112 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_12)—Offset A60h

This register applies to GPP_A12 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.113 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_12)—Offset A64h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 4Ch

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	4Ch RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.114 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_13)—Offset A70h

This register applies to GPP_A13 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.115 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_13)—Offset A74h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 4Dh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	4Dh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.116 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_14)—Offset A80h

This register applies to GPP_A14 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.117 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_14)—Offset A84h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 4Eh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	**IO Standby Termination (IOSTERM):** Same description as IOSTERM bits in PAD_CFG_DW1_GPPC_A_0.
7:0	4Eh RO	Reserved.

27.1.118 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_15)—Offset A90h

This register applies to GPP_A15 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.119 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_15)—Offset A94h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 4Fh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	4Fh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.120 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_16)—Offset AA0h

This register applies to GPP_A16 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.121 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_16)—Offset AA4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 50h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	50h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.122 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_17)—Offset AB0h

This register applies to GPP_A17 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.123 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_17)—Offset AB4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 51h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	51h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.124 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_18)—Offset AC0h

This register applies to GPP_A18 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.125 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_18)—Offset AC4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 52h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	52h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.126 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_19)—Offset AD0h

This register applies to GPP_A19 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.127 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_19)—Offset AD4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 53h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	53h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.128 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_20)—Offset AE0h

This register applies to GPP_A20 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.129 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_20)—Offset AE4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 54h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	54h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.130 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_21)—Offset AF0h

This register applies to GPP_A21 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.131 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_21)—Offset AF4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 55h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	55h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.132 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_22)—Offset B00h

This register applies to GPP_A22 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.133 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_22)—Offset B04h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 56h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	56h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.1.134 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_A_23)—Offset B10h

This register applies to GPP_A23 and has the same description as PAD_CFG_DW0_GPP_B_0

27.1.135 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_A_23)—Offset B14h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 57h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_A_0.
9:8	0h RW	Reserved.
7:0	57h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_A_0.

27.2 GPIO Community 1 Registers Summary

GPIO pins are grouped into different Community (e.g. Community 0, Community 1, etc.). Each Community consists of one or more GPIO groups.
This section covers registers for Community 1, which consists of GPP_D, GPP_H, GPP_S and GPP_U groups.

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID

+ Register Offset).
Note that each GPIO Community has a different PortID. See the Primary to Sideband Bridge Section in Vol1 for PortID info.

Table 11. Summary of GPIO Community 1 Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8h	Bh	Family Base Address (FAMBAR)—Offset 8h	300h
Ch	Fh	Pad Base Address (PADBAR)—Offset Ch	700h
10h	13h	Miscellaneous Configuration (MISCCFG)—Offset 10h	33043200h
20h	23h	Pad Ownership (PAD_OWN_GPP_S_0)—Offset 20h	0h
24h	27h	Pad Ownership (PAD_OWN_GPP_H_0)—Offset 24h	0h
28h	2Bh	Pad Ownership (PAD_OWN_GPP_H_1)—Offset 28h	0h
2Ch	2Fh	Pad Ownership (PAD_OWN_GPP_H_2)—Offset 2Ch	0h
30h	33h	Pad Ownership (PAD_OWN_GPP_D_0)—Offset 30h	0h
34h	37h	Pad Ownership (PAD_OWN_GPP_D_1)—Offset 34h	0h
38h	3Bh	Pad Ownership (PAD_OWN_GPP_D_2)—Offset 38h	0h
3Ch	3Fh	Pad Ownership (PAD_OWN_GPP_U_0)—Offset 3Ch	0h
80h	83h	Pad Configuration Lock (PADCFGLOCK_GPP_S_0)—Offset 80h	0h
84h	87h	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_S_0)—Offset 84h	0h
88h	8Bh	Pad Configuration Lock (PADCFGLOCK_GPP_H_0)—Offset 88h	0h
8Ch	8Fh	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_H_0)—Offset 8Ch	0h
90h	93h	Pad Configuration Lock (PADCFGLOCK_GPP_D_0)—Offset 90h	0h
94h	97h	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_D_0)—Offset 94h	0h
98h	9Bh	Pad Configuration Lock (PADCFGLOCK_GPP_U_0)—Offset 98h	0h
9Ch	9Fh	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_U_0)—Offset 9Ch	0h
B0h	B3h	Host Software Pad Ownership (HOSTSW_OWN_GPP_S_0)—Offset B0h	0h
B4h	B7h	Host Software Pad Ownership (HOSTSW_OWN_GPP_H_0)—Offset B4h	0h
B8h	BBh	Host Software Pad Ownership (HOSTSW_OWN_GPP_D_0)—Offset B8h	0h
BCh	BFh	Host Software Pad Ownership (HOSTSW_OWN_GPP_U_0)—Offset BCh	0h
100h	103h	GPI Interrupt Status (GPI_IS_GPP_S_0)—Offset 100h	0h
104h	107h	GPI Interrupt Status (GPI_IS_GPP_H_0)—Offset 104h	0h
108h	10Bh	GPI Interrupt Status (GPI_IS_GPP_D_0)—Offset 108h	0h
10Ch	10Fh	GPI Interrupt Status (GPI_IS_GPP_U_0)—Offset 10Ch	0h
120h	123h	GPI Interrupt Enable (GPI_IE_GPP_S_0)—Offset 120h	0h
124h	127h	GPI Interrupt Enable (GPI_IE_GPP_H_0)—Offset 124h	0h
128h	12Bh	GPI Interrupt Enable (GPI_IE_GPP_D_0)—Offset 128h	0h
12Ch	12Fh	GPI Interrupt Enable (GPI_IE_GPP_U_0)—Offset 12Ch	0h
140h	143h	GPI General Purpose Events Status (GPI_GPE_STS_GPP_S_0)—Offset 140h	0h
144h	147h	GPI General Purpose Events Status (GPI_GPE_STS_GPP_H_0)—Offset 144h	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
148h	14Bh	GPI General Purpose Events Status (GPI_GPE_STS_GPP_D_0)—Offset 148h	0h
14Ch	14Fh	GPI General Purpose Events Status (GPI_GPE_STS_GPP_U_0)—Offset 14Ch	0h
160h	163h	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_S_0)—Offset 160h	0h
164h	167h	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_H_0)—Offset 164h	0h
168h	16Bh	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_D_0)—Offset 168h	0h
16Ch	16Fh	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_U_0)—Offset 16Ch	0h
188h	18Bh	SMI Status (GPI_SMI_STS_GPP_D_0)—Offset 188h	0h
1A8h	1ABh	SMI Enable (GPI_SMI_EN_GPP_D_0)—Offset 1A8h	0h
1C8h	1CBh	NMI Status (GPI_NMI_STS_GPP_D_0)—Offset 1C8h	0h
1E8h	1EBh	NMI Enable (GPI_NMI_EN_GPP_D_0)—Offset 1E8h	0h
204h	207h	PWM Control (PWMC)—Offset 204h	0h
20Ch	20Fh	GPIO Serial Blink Enable (GP_SER_BLINK)—Offset 20Ch	0h
210h	213h	GPIO Serial Blink Command/Status (GP_SER_CMDSTS)—Offset 210h	80000h
214h	217h	GPIO Serial Blink Data (GP_SER_DATA)—Offset 214h	0h
700h	703h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_0)—Offset 700h	0h
704h	707h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_0)—Offset 704h	6Ch
710h	713h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_1)—Offset 710h	0h
714h	717h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_1)—Offset 714h	6Dh
720h	723h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_2)—Offset 720h	0h
724h	727h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_2)—Offset 724h	6Eh
730h	733h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_3)—Offset 730h	0h
734h	737h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_3)—Offset 734h	6Fh
740h	743h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_4)—Offset 740h	0h
744h	747h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_4)—Offset 744h	70h
750h	753h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_5)—Offset 750h	0h
754h	757h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_5)—Offset 754h	71h
760h	763h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_6)—Offset 760h	0h
764h	767h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_6)—Offset 764h	72h
770h	773h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_7)—Offset 770h	0h
774h	777h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_7)—Offset 774h	73h
780h	783h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_0)—Offset 780h	4400XX00h See register for X value
784h	787h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_0)—Offset 784h	74h
790h	793h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_1)—Offset 790h	4400XX00h See register for X value
794h	797h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_1)—Offset 794h	75h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
7A0h	7A3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_2)—Offset 7A0h	4400XX00h See register for X value
7A4h	7A7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_2)—Offset 7A4h	76h
7B0h	7B3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_3)—Offset 7B0h	4400XX00h See register for X value
7B4h	7B7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_3)—Offset 7B4h	77h
7C0h	7C3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_4)—Offset 7C0h	4400XX00h See register for X value
7C4h	7C7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_4)—Offset 7C4h	18h
7D0h	7D3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_5)—Offset 7D0h	4400XX00h See register for X value
7D4h	7D7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_5)—Offset 7D4h	19h
7E0h	7E3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_6)—Offset 7E0h	4400XX00h See register for X value
7E4h	7E7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_6)—Offset 7E4h	1Ah
7F0h	7F3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_7)—Offset 7F0h	4400XX00h See register for X value
7F4h	7F7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_7)—Offset 7F4h	1Bh
800h	803h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_8)—Offset 800h	4400XX00h See register for X value
804h	807h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_8)—Offset 804h	1Ch
810h	813h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_9)—Offset 810h	4400XX00h See register for X value
814h	817h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_9)—Offset 814h	1Dh
820h	823h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_10)—Offset 820h	4400XX00h See register for X value
824h	827h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_10)—Offset 824h	1Eh
830h	833h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_11)—Offset 830h	4400XX00h See register for X value
834h	837h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_11)—Offset 834h	1Fh
840h	843h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_12)—Offset 840h	4400XX00h See register for X value
844h	847h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_12)—Offset 844h	20h
850h	853h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_13)—Offset 850h	4400XX00h See register for X value
854h	857h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_13)—Offset 854h	21h
860h	863h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_14)—Offset 860h	4400XX00h See register for X value
864h	867h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_14)—Offset 864h	22h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
870h	873h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_15)—Offset 870h	4400XX00h See register for X value
874h	877h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_15)—Offset 874h	23h
880h	883h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_16)—Offset 880h	4400XX00h See register for X value
884h	887h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_16)—Offset 884h	24h
890h	893h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_17)—Offset 890h	4400XX00h See register for X value
894h	897h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_17)—Offset 894h	25h
8A0h	8A3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_18)—Offset 8A0h	4400XX00h See register for X value
8A4h	8A7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_18)—Offset 8A4h	26h
8B0h	8B3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_19)—Offset 8B0h	4400XX00h See register for X value
8B4h	8B7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_19)—Offset 8B4h	27h
8C0h	8C3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_20)—Offset 8C0h	4400XX00h See register for X value
8C4h	8C7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_20)—Offset 8C4h	28h
8D0h	8D3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_21)—Offset 8D0h	4400XX00h See register for X value
8D4h	8D7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_21)—Offset 8D4h	29h
8E0h	8E3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_22)—Offset 8E0h	4400XX00h See register for X value
8E4h	8E7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_22)—Offset 8E4h	2Ah
8F0h	8F3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_23)—Offset 8F0h	4400XX00h See register for X value
8F4h	8F7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_23)—Offset 8F4h	2Bh
900h	903h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_0)—Offset 900h	4400XX00h See register for X value
904h	907h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_0)—Offset 904h	2Ch
910h	913h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_1)—Offset 910h	4400XX00h See register for X value
914h	917h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_1)—Offset 914h	2Dh
920h	923h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_2)—Offset 920h	4400XX00h See register for X value
924h	927h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_2)—Offset 924h	2Eh
930h	933h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_3)—Offset 930h	4400XX00h See register for X value
934h	937h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_3)—Offset 934h	2Fh

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
940h	943h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_4)—Offset 940h	4400XX00h See register for X value
944h	947h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_4)—Offset 944h	30h
950h	953h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_5)—Offset 950h	4400XX00h See register for X value
954h	957h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_5)—Offset 954h	31h
960h	963h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_6)—Offset 960h	4400XX00h See register for X value
964h	967h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_6)—Offset 964h	32h
970h	973h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_7)—Offset 970h	4400XX00h See register for X value
974h	977h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_7)—Offset 974h	33h
980h	983h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_8)—Offset 980h	4400XX00h See register for X value
984h	987h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_8)—Offset 984h	34h
990h	993h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_9)—Offset 990h	4400XX00h See register for X value
994h	997h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_9)—Offset 994h	3C35h
9A0h	9A3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_10)—Offset 9A0h	4400XX00h See register for X value
9A4h	9A7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_10)—Offset 9A4h	3C36h
9B0h	9B3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_11)—Offset 9B0h	4400XX00h See register for X value
9B4h	9B7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_11)—Offset 9B4h	3C37h
9C0h	9C3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_12)—Offset 9C0h	4400XX00h See register for X value
9C4h	9C7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_12)—Offset 9C4h	3C38h
9D0h	9D3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_13)—Offset 9D0h	4400XX00h See register for X value
9D4h	9D7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_13)—Offset 9D4h	39h
9E0h	9E3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_14)—Offset 9E0h	4400XX00h See register for X value
9E4h	9E7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_14)—Offset 9E4h	3Ah
9F0h	9F3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_15)—Offset 9F0h	4400XX00h See register for X value
9F4h	9F7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_15)—Offset 9F4h	3Bh
A00h	A03h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_16)—Offset A00h	4400XX00h See register for X value
A04h	A07h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_16)—Offset A04h	3Ch

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
A10h	A13h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_17)—Offset A10h	4400XX00h See register for X value
A14h	A17h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_17)—Offset A14h	3Dh
A20h	A23h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_18)—Offset A20h	4400XX00h See register for X value
A24h	A27h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_18)—Offset A24h	3Eh
A30h	A33h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_19)—Offset A30h	4400XX00h See register for X value
A34h	A37h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_19)—Offset A34h	3Fh
A90h	A93h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_4)—Offset A90h	4400XX00h See register for X value
A94h	A97h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_4)—Offset A94h	44h
AA0h	AA3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_5)—Offset AA0h	4400XX00h See register for X value
AA4h	AA7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_5)—Offset AA4h	45h

27.2.1 Family Base Address (FAMBAR)—Offset 8h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 300h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

27.2.2 Pad Base Address (PADBAR)—Offset Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 700h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	700h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

27.2.3 Miscellaneous Configuration (MISCCFG)—Offset 10h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 33043200h

Bit Range	Default & Access	Field Name (ID): Description
31:24	33h RW	**GPIO Driver Mode Interrupt Select (GPDMINTSEL):** IRQ globally for all pads (GPI_IS with corresponding GPI_IE enable). 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255
23:20	0h RO	Reserved.
19:16	4h RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[87:64]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[67:66]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[87:64]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[71:64]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[75:64]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[71:64]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[87:64]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[83:64]; other GPE bits not used. 8h = GPP_U[5:4] mapped to GPE[69:68]; other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[87:64]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[87:64]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[87:64]; other GPE bits not used. Dh - Fh: Reserved
15:12	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[55:32]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[35:34]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[55:32]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[39:32]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[43:32]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[39:32]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[55:32]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[51:32]; other GPE bits not used. 8h = GPP_U[5:4] mapped to GPE[37:36]; other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[55:32]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[55:32]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[55:32]; other GPE bits not used. Dh - Fh: Reserved

Bit Range	Default & Access	Field Name (ID): Description
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[23:0]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[3:2]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[23:0]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[7:0]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[11:0]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[7:0]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[23:0]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[19:0]; other GPE bits not used. 8h = GPP_U[5:4] mapped to GPE[5:4];other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[23:0]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[23:0]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[23:0]; other GPE bits not used. Dh - Fh: Reserved
7:2	0h RO	Reserved.
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specify whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specifies whether the GPIO Community should perform local clock gating. 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating

27.2.4 Pad Ownership (PAD_OWN_GPP_S_0)—Offset 20h

Same description as PAD_OWN_GPP_H_0 at offset 24h, except that this register is for GPP_S[7:0].

27.2.5 Pad Ownership (PAD_OWN_GPP_H_0)—Offset 24h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_7):** Same description as bits[1:0].
27:26	0h RO	Reserved.
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_6):** Same description as bits[1:0].
23:22	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_5):** Same description as bits[1:0].
19:18	0h RO	Reserved.
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_4):** Same description as bits[1:0].
15:14	0h RO	Reserved.
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_3):** Same description as bits[1:0].
11:10	0h RO	Reserved.
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_2):** Same description as bits[1:0].
7:6	0h RO	Reserved.
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_1):** Same description as bits[1:0].
3:2	0h RO	Reserved.
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_H_0):** 00 = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership 01 = ME GPIO Mode. ME has ownership of the pad. 10 = ISH GPIO Mode. ME has ownership of the pad 11 = Reserved

27.2.6 Pad Ownership (PAD_OWN_GPP_H_1)—Offset 28h

Same description as PAD_OWN_GPP_H0 at offset 24h, except that this register is for GPP_H[15:8].

27.2.7 Pad Ownership (PAD_OWN_GPP_H_2)—Offset 2Ch

Same description as PAD_OWN_GPP_H_0 at offset 24h, except that this register is for GPP_H[23:16].

27.2.8 Pad Ownership (PAD_OWN_GPP_D_0)—Offset 30h

Same description as PAD_OWN_GPP_H_0 at offset 24h, except that this register is for GPP_D[7:0].

27.2.9 Pad Ownership (PAD_OWN_GPP_D_1)—Offset 34h

Same description as PAD_OWN_GPP_H_0 at offset 24h, except that this register is for GPP_D[15:8].

27.2.10 Pad Ownership (PAD_OWN_GPP_D_2)—Offset 38h

Same description as PAD_OWN_GPP_H_0 at offset 24h, except that this register is for GPP_D[19:16].
(Note: Bits corresponding to unimplemented GPP_D pins are reserved.)

27.2.11 Pad Ownership (PAD_OWN_GPP_U_0)—Offset 3Ch

Same description as PAD_OWN_GPP_H_0 at offset 24h, except that this register is for GPP_U[4:5].
(Note: bits corresponding to unimplemented GPP pins are reserved).

27.2.12 Pad Configuration Lock (PADCFGLOCK_GPP_S_0)—Offset 80h

Same description as PADCFGLOCK_GPP_H_0 register at offset 88h, except this register applies to GPP_S[7:0].
(Note: Bits corresponding to unimplemented GPP pins are reserved.)

27.2.13 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_S_0)—Offset 84h

Same description as PADCFGLOCKTX_GPP_H_0 register at offset 8Ch, except this register applies to GPP_S[7:0].
(Note: Bits corresponding to unimplemented GPP pins are reserved.)

27.2.14 Pad Configuration Lock (PADCFGLOCK_GPP_H_0)—Offset 88h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_23):** Same description as bit 0.
22	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_22):** Same description as bit 0.
21	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_21):** Same description as bit 0.
20	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_20):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_19):** Same description as bit 0.
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_18):** Same description as bit 0.
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_17):** Same description as bit 0.
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_16):** Same description as bit 0.
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_15):** Same description as bit 0.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_14):** Same description as bit 0.
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_13):** Same description as bit 0.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_12):** Same description as bit 0.
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_11):** Same description as bit 0.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_10):** Same description as bit 0.
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_9):** Same description as bit 0.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_8):** Same description as bit 0.
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_7):** Same description as bit 0.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_6):** Same description as bit 0.
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_5):** Same description as bit 0.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_4):** Same description as bit 0.
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_3):** Same description as bit 0.
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_2):** Same description as bit 0.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_1):** Same description as bit 0.
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_H_0):** Pad Configuration Lock locks specific register fields in the GPP specific registers from being configured. The registers affected become Read-Only and software writes to these registers have no effect. 0 = Unlock 1 = Lock the following register fields as read-only (RO): - Pad Configuration registers (exclude GPIOTXState) - GPI_NMI_EN Register (if implemented) - GPI_SMI_EN Register (if implemented) - GPI_GPE_EN Register (if implemented) When PadCfgLock is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

27.2.15 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_H_0)—Offset 8Ch

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_23):** Same description as bit 0.
22	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_22):** Same description as bit 0.
21	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_21):** Same description as bit 0.
20	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_20):** Same description as bit 0.
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_19):** Same description as bit 0.
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_18):** Same description as bit 0.
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_17):** Same description as bit 0.
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_16):** Same description as bit 0.
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_15):** Same description as bit 0.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_14):** Same description as bit 0.
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_13):** Same description as bit 0.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_12):** Same description as bit 0.
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_11):** Same description as bit 0.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_10):** Same description as bit 0.
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_9):** Same description as bit 0.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_8):** Same description as bit 0.
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_7):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_6):** Same description as bit 0.
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_5):** Same description as bit 0.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_4):** Same description as bit 0.
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_3):** Same description as bit 0.
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_2):** Same description as bit 0.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_1):** Same description as bit 0.
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_H_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) When PadCfgLockTx is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

27.2.16 Pad Configuration Lock (PADCFGLOCK_GPP_D_0)—Offset 90h

Same description as PADCFGLOCK_GPP_H_0 register at offset 88h, except this register applies to GPP_D[19:0].
(Note: Bits corresponding to unimplemented GPP pins are reserved.)

27.2.17 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_D_0)—Offset 94h

Same description as PADCFGLOCKTX_GPP_H_0 register at offset 8Ch, except this register applies to GPP_D[19:0].
(Note: Bits corresponding to unimplemented GPP pins are reserved.)

27.2.18 Pad Configuration Lock (PADCFGLOCK_GPP_U_0)—Offset 98h

Same description as PADCFGLOCK_GPP_H_0 register at offset 88h, except this register applies to GPP_U[5:4].
(Note: Bits corresponding to unimplemented GPP pins are reserved).

27.2.19 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_U_0)—Offset 9Ch

Same description as PADCFGLOCKTX_GPP_H_0 register at offset 8Ch, except this register applies to GPP_U[5:4].
(Note: Bits corresponding to unimplemented GPP pins are reserved).

27.2.20 Host Software Pad Ownership (HOSTSW_OWN_GPP_S_0)—Offset B0h

Same description as HOSTSW_OWN_GPP_H_0 register at offset B4h, except that this register applies to GPP_S[7:0].
(Note: bits corresponding to unimplemented GPP will be reserved.)

27.2.21 Host Software Pad Ownership (HOSTSW_OWN_GPP_H_0)—Offset B4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_23):** Same description as bit 0.
22	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_22):** Same description as bit 0.
21	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_21):** Same description as bit 0.
20	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_20):** Same description as bit 0.
19	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_19):** Same description as bit 0.
18	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_18):** Same description as bit 0.
17	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_17):** Same description as bit 0.
16	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_16):** Same description as bit 0.
15	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_15):** Same description as bit 0.
14	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_14):** Same description as bit 0.
13	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_13):** Same description as bit 0.
12	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_12):** Same description as bit 0.
11	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_11):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
10	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_10):** Same description as bit 0.
9	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_9):** Same description as bit 0.
8	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_8):** Same description as bit 0.
7	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_7):** Same description as bit 0.
6	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_6):** Same description as bit 0.
5	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_5):** Same description as bit 0.
4	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_4):** Same description as bit 0.
3	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_3):** Same description as bit 0.
2	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_2):** Same description as bit 0.
1	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_1):** Same description as bit 0.
0	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_H_0):** This register determines the appropriate host status bit update when a pad is under host ownership. 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked.

27.2.22 Host Software Pad Ownership (HOSTSW_OWN_GPP_D_0)—Offset B8h

Same description as HOSTSW_OWN_GPP_H_0 register at offset B4h, except that this register applies to GPP_D[19:0].
(Note: bits corresponding to unimplemented GPP will be reserved.)

27.2.23 Host Software Pad Ownership (HOSTSW_OWN_GPP_U_0)—Offset BCh

Same description as HOSTSW_OWN_GPP_H_0 register at offset B4h, except that this register applies to GPP_U[5:4].
(Note: bits corresponding to unimplemented GPP will be reserved).

27.2.24 GPI Interrupt Status (GPI_IS_GPP_S_0)—Offset 100h

Same description GPI_IS_GPP_H_0 register at offset 104h, except this register applies to GPP_S[7:0].
(Note: bits corresponding to unimplemented GPP will be reserved.)

27.2.25 GPI Interrupt Status (GPI_IS_GPP_H_0)—Offset 104h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_23):** Same description as bit 0.
22	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_22):** Same description as bit 0.
21	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_21):** Same description as bit 0.
20	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_20):** Same description as bit 0.
19	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_19):** Same description as bit 0.
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_18):** Same description as bit 0.
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_17):** Same description as bit 0.
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_16):** Same description as bit 0.
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_15):** Same description as bit 0.
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_14):** Same description as bit 0.
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_13):** Same description as bit 0.
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_12):** Same description as bit 0.
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_11):** Same description as bit 0.
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_10):** Same description as bit 0.
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_9):** Same description as bit 0.
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_8):** Same description as bit 0.
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_7):** Same description as bit 0.
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_6):** Same description as bit 0.
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_5):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_4):** Same description as bit 0.
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_3):** Same description as bit 0.
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_2):** Same description as bit 0.
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_1):** Same description as bit 0.
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_H_0):** This bit is set to '1' by hardware when either an edge or a level event is detected on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode - HOSTSW_OWN = 1 (i.e. Host GPIO Driver Mode). Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x].

27.2.26 GPI Interrupt Status (GPI_IS_GPP_D_0)—Offset 108h

Same description GPI_IS_GPP_H_0 register at offset 104h, except this register applies to GPP_D[19:0].
(Note: bits corresponding to unimplemented GPP will be reserved.)

27.2.27 GPI Interrupt Status (GPI_IS_GPP_U_0)—Offset 10Ch

Same description GPI_IS_GPP_H_0 register at offset 104h, except this register applies to GPP_U[5:4].
(Note: bits corresponding to unimplemented GPP will be reserved.)

27.2.28 GPI Interrupt Enable (GPI_IE_GPP_S_0)—Offset 120h

Same description GPI_IE_GPP_H_0 register at offset 124h, except this register applies to GPP_S[7:0].
(Note: bits corresponding to unimplemented GPP will be reserved.)

27.2.29 GPI Interrupt Enable (GPI_IE_GPP_H_0)—Offset 124h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_23):** Same description as bit 0.
22	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_22):** Same description as bit 0.
21	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_21):** Same description as bit 0.
20	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_20):** Same description as bit 0.
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_19):** Same description as bit 0.
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_18):** Same description as bit 0.
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_17):** Same description as bit 0.
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_16):** Same description as bit 0.
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_15):** Same description as bit 0.
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_14):** Same description as bit 0.
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_13):** Same description as bit 0.
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_12):** Same description as bit 0.
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_11):** Same description as bit 0.
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_10):** Same description as bit 0.
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_9):** Same description as bit 0.
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_8):** Same description as bit 0.
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_7):** Same description as bit 0.
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_6):** Same description as bit 0.
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_5):** Same description as bit 0.
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_4):** Same description as bit 0.
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_3):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_2):** Same description as bit 0.
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_1):** Same description as bit 0.
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_H_0):** This bit is used to enable/ disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation

27.2.30 GPI Interrupt Enable (GPI_IE_GPP_D_0)—Offset 128h

Same description GPI_IE_GPP_H_0 register at offset 124h, except this register applies to GPP_D[19:0].
(Note: bits corresponding to unimplemented GPP will be reserved.)

27.2.31 GPI Interrupt Enable (GPI_IE_GPP_U_0)—Offset 12Ch

Same description GPI_IE_GPP_H_0 register at offset 124h, except this register applies to GPP_U[5:4].
(Note: bits corresponding to unimplemented GPP will be reserved).

27.2.32 GPI General Purpose Events Status (GPI_GPE_STS_GPP_S_0)—Offset 140h

Same description GPI_GPE_STS_GPP_H_0 register at offset 144h, except this register applies to GPP_S[7:0].
(Note: bits corresponding to unimplemented GPP will be reserved.)

27.2.33 GPI General Purpose Events Status (GPI_GPE_STS_GPP_H_0)—Offset 144h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_23):** Same description as bit 0.
22	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_22):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
21	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_21):** Same description as bit 0.
20	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_20):** Same description as bit 0.
19	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_19):** Same description as bit 0.
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_18):** Same description as bit 0.
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_17):** Same description as bit 0.
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_16):** Same description as bit 0.
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_15):** Same description as bit 0.
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_14):** Same description as bit 0.
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_13):** Same description as bit 0.
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_12):** Same description as bit 0.
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_11):** Same description as bit 0.
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_10):** Same description as bit 0.
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_9):** Same description as bit 0.
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_8):** Same description as bit 0.
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_7):** Same description as bit 0.
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_6):** Same description as bit 0.
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_5):** Same description as bit 0.
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_4):** Same description as bit 0.
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_3):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_2):** Same description as bit 0.
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_1):** Same description as bit 0.
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_H_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: - If the system is in an S3-S5 state, the event will also wake the system. - If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be generated, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS.

27.2.34 GPI General Purpose Events Status (GPI_GPE_STS_GPP_D_0)—Offset 148h

Same description GPI_GPE_STS_GPP_H_0 register at offset 144h, except this register applies to GPP_D[19:0].
(Note: bits corresponding to unimplemented GPP will be reserved.)

27.2.35 GPI General Purpose Events Status (GPI_GPE_STS_GPP_U_0)—Offset 14Ch

Same description GPI_GPE_STS_GPP_H_0 register at offset 144h, except this register applies to GPP_U[5:4].
(Note: bits corresponding to unimplemented GPP will be reserved).

27.2.36 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_S_0)—Offset 160h

Same description GPI_GPE_EN_GPP_H_0 register, except this register applies to GPP_S[7:0].
(Note: bits corresponding to unimplemented GPP will be reserved.)

27.2.37 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_H_0)—Offset 164h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_23):** Same description as bit 0.
22	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_22):** Same description as bit 0.
21	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_21):** Same description as bit 0.
20	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_20):** Same description as bit 0.
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_19):** Same description as bit 0.
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_18):** Same description as bit 0.
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_17):** Same description as bit 0.
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_16):** Same description as bit 0.
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_15):** Same description as bit 0.
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_14):** Same description as bit 0.
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_13):** Same description as bit 0.
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_12):** Same description as bit 0.
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_11):** Same description as bit 0.
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_10):** Same description as bit 0.
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_9):** Same description as bit 0.
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_8):** Same description as bit 0.
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_7):** Same description as bit 0.
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_6):** Same description as bit 0.
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_5):** Same description as bit 0.
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_4):** Same description as bit 0.
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_3):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_2):** Same description as bit 0.
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_1):** Same description as bit 0.
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_H_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'.

27.2.38 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_D_0)—Offset 168h

Same description GPI_GPE_EN_GPP_H_0 register, except this register applies to GPP_D[19:0].
(Note: bits corresponding to unimplemented GPP will be reserved.)

27.2.39 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_U_0)—Offset 16Ch

Same description GPI_GPE_EN_GPP_H_0 register, except this register applies to GPP_U[5:4].
(Note: bits corresponding to unimplemented GPP will be reserved).

27.2.40 SMI Status (GPI_SMI_STS_GPP_D_0)—Offset 188h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_4):** Same description as bit 0.
3	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_3):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_2):** Same description as bit 0.
1	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_1):** Same description as bit 0.
0	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_D_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to 1. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is 1, bit0 of this bit is locked down to read-only.

27.2.41 SMI Enable (GPI_SMI_EN_GPP_D_0)—Offset 1A8h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_4):** Same description as bit 0.
3	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_3):** Same description as bit 0.
2	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_2):** Same description as bit 0.
1	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_1):** Same description as bit 0.
0	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_D_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to 1. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is 1, bit0 of this bit is locked down to read-only.

27.2.42 NMI Status (GPI_NMI_STS_GPP_D_0)—Offset 1C8h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_4):** Same description as bit 0.
3	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_3):** Same description as bit 0.
2	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_2):** Same description as bit 0.
1	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_1):** Same description as bit 0.
0	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_D_0):** This bit is set to 1 by hardware when an edge event is detected on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode (PMode) - The corresponding GPIONMIRout is set to 1, i.e. programmed to route as NMI - The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). - The corresponding GPI_NMI_EN is set Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = There is no NMI event 1 = There is an NMI event

27.2.43 NMI Enable (GPI_NMI_EN_GPP_D_0)—Offset 1E8h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_4):** Same description as bit 0.
3	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_3):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_2):** Same description as bit 0.
1	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_1):** Same description as bit 0.
0	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_D_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only.

27.2.44 PWM Control (PWMC)—Offset 204h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable (EN):** 0 = Disable PWM Output 1 = Enable PWM Output
30	0h RW/1S/V	**Software Update (SWUP):** Indication that there is an update to PWM settings pending. SW sets this bit to 1 when updating the PWM_base_unit or PWM_on_time_divisor fields. The PWM module will apply the new settings at the end of the current cycle and reset this bit. 0 = No updates pending 1 = Update pending
29:8	0h RW	**Base Unit (BASEUNIT):** Base unit register. Unsigned 8 integer bits, 14 fraction bits. Used to determine PWM output frequency.
7:0	0h RW	**On Time Divisor (ONTIMEDIV):** PWM duty cycle = PWM_on-time_divisor/256.

27.2.45 GPIO Serial Blink Enable (GP_SER_BLINK)—Offset 20Ch

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:0	0h RW	**GP SER BLINK (GP_SER_BLINK):** The setting of this bit has no effect if the corresponding GPIO is programmed as an input, if the corresponding GPIO has the PWM enabled, or if Serial Blink capability does not exist . This bit should be set to a 1 before output buffer is enabled. When set to a '0', the corresponding GPIO will function normally. This bit should be set to a 1 while the corresponding PMode bit is set to 0h (GPIO Mode). Setting the PMode bit to other value (non-GPIO Mode) after the GP_SER_BLINK bit ensures PCH will not drive a 1 on the pin as an output. When this corresponding bit is set to a 1 and the pin is configured to output mode, the serial blink capability is enabled and the programmed message is serialized out through an open-drain buffer configuration. The value of the corresponding GPIOTxState bit remains unchanged and does not impact the serial blink capability in any way. Writes to this register have no effect when the corresponding pin is configured in native mode and the read value returned is undefined. Bit0 = GPP_D0 Bit1 = GPP_D1 Bit2 = GPP_D2 Bit3 = GPP_D3. Bit4 = GPP_D4

27.2.46 GPIO Serial Blink Command/Status (GP_SER_CMDSTS)—Offset 210h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 80000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:22	0h RW	**Data Length Select (DLS):** This read/write field determines the number of bytes to serialize on GPIO 00: Serialize bits 7:0 of GP_GB_DATA (1 byte) 01: Serialize bits 15:0 of GP_GB_DATA (2 bytes) 10: Undefined - Software must not write this value 11: Serialize bits 31:0 of GP_GB_DATA (4 bytes) Software should not modify the value in this register unless the Busy bit is clear
21:16	8h RW	**Data Rate Select (DRS):** This read/write field selects the number of 166.64ns (4 clock periods GPIO clock - if GPIO clock is 24MHz) time intervals to count between Manchester data transitions. The default of 8h results in a 1333.33 ns minimum time between transitions. A value of 0h in this register produces undefined behavior. Software should not modify the value in this register unless the Busy bit is clear.
15:9	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO/V	**Busy (BUSY):** This read-only status bit is the hardware indication that a serialization is in progress. Hardware sets this bit to 1 based on the Go bit being set. Hardware clears this bit when the Go bit is cleared by the hardware.
7:1	0h RO	Reserved.
0	0h RW	**Go (GO):** This bit is set to 1 by software to start the serialization process. Hardware clears the bit after the serialized data is sent. Writes of 0 to this register have no effect. Software should not write this bit to 1 unless the Busy status bit is cleared.

27.2.47 GPIO Serial Blink Data (GP_SER_DATA)—Offset 214h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GP Serial Blink Data (GP_GB_DATA):** This read-write register contains the data serialized out. The number of bits shifted out is selected through the DLS field in the GP_GB_CMDSTS register. This register should not be modified by software when the Busy bit is set.

27.2.48 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_0)—Offset 700h

This register applies to GPP_S0 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.49 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_0)—Offset 704h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 6Ch

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved. NOTES: 1. The 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily.
9:8	0h RW	Reserved.
7:0	6Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

27.2.50 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_1)—Offset 710h

This register applies to GPP_S1 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.51 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_1)—Offset 714h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 6Dh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_S_0
9:8	0h RW	Reserved.
7:0	6Dh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPP_S_0.

27.2.52 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_2)—Offset 720h

This register applies to GPP_S2 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.53 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_2)—Offset 724h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 6Eh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_S_0
9:8	0h RW	Reserved.
7:0	6Eh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_S_0.

27.2.54 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_3)—Offset 730h

This register applies to GPP_S3 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.55 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_3)—Offset 734h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 6Fh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_S_0
9:8	0h RW	Reserved.
7:0	6Fh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_S_0.

27.2.56 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_4)—Offset 740h

This register applies to GPP_S4 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.57 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_4)—Offset 744h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 70h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_S_0
9:8	0h RW	Reserved.
7:0	70h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_S_0.

27.2.58 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_5)—Offset 750h

This register applies to GPP_S5 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.59 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_5)—Offset 754h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 71h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_S_0
9:8	0h RW	Reserved.
7:0	71h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_S_0.

27.2.60 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_6)—Offset 760h

This register applies to GPP_S6 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.61 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_6)—Offset 764h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 72h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_S_0
9:8	0h RW	Reserved.
7:0	72h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_S_0.

27.2.62 Pad Configuration DW0 (PAD_CFG_DW0_GPP_S_7)—Offset 770h

This register applies to GPP_S7 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.63 Pad Configuration DW1 (PAD_CFG_DW1_GPP_S_7)—Offset 774h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 73h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPP_S_0
9:8	0h RW	Reserved.
7:0	73h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_S_0.

27.2.64 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_0)—Offset 780h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 4400XX00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset GPIO pad register fields in various GPIO registers (PADCFGLOCK, PADCFGLOCKTX, GPI_IS, GPI_IE, GPI_GPE_STS, GPI_GPE_EN, GPI_SMI_STS, SPI_SMI_EN, GPI_NMI_STS, GPI_NMI_EN, PAD_CFG_DW0, and PAD_CFG_DW1). 00 = Global Reset or RSMRST# 01 = Host deep reset. This reset occurs when any of the following occur: Host reset (with or without power cycle) is initiated, Global reset is initiated, or Deep Sx entry. This reset does NOT occur as part of S3/S4/S5 entry. 10 = PLTRST# 11 = Global Reset
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	Reserved.
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	Reserved.
12:10	-- RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO controls the Pad 1h = Function 1, if applicable, controls the Pad ... 7h = Function 7, if applicable, controls the Pad Default value is determined by the default functionality of the pad.
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0'.
8	0h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	Reserved.
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

27.2.65 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_0)—Offset 784h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 74h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved. NOTES: 1. The 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily.
9:8	0h RW	Reserved.
7:0	74h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

27.2.66 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_1)—Offset 790h

This register applies to GPP_H1 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.67 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_1)—Offset 794h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 75h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	75h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.68 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_2)—Offset 7A0h

This register applies to GPP_H2 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.69 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_2)—Offset 7A4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 76h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	76h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.70 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_3)—Offset 7B0h

This register applies to GPP_H3 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.71 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_3)—Offset 7B4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 77h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	77h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.72 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_4)—Offset 7C0h

This register applies to GPP_H4 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.73 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_4)—Offset 7C4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 18h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	18h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.74 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_5)—Offset 7D0h

This register applies to GPP_H5 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.75 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_5)—Offset 7D4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 19h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	19h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.76 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_6)—Offset 7E0h

This register applies to GPP_H6 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.77 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_6)—Offset 7E4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 1Ah

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	1Ah RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.78 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_7)—Offset 7F0h

This register applies to GPP_H7 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.79 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_7)—Offset 7F4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 1Bh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	1Bh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.80 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_8)—Offset 800h

This register applies to GPP_H8 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.81 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_8)—Offset 804h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 1Ch

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	1Ch RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.82 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_9)—Offset 810h

This register applies to GPP_H9 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.83 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_9)—Offset 814h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 1Dh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	1Dh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.84 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_10)—Offset 820h

This register applies to GPP_H10 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.85 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_10)—Offset 824h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 1Eh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	1Eh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.86 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_11)—Offset 830h

This register applies to GPP_H11 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.87 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_11)—Offset 834h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 1Fh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	1Fh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.88 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_12)—Offset 840h

This register applies to GPP_H12 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.89 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_12)—Offset 844h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 20h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	20h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.90 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_13)—Offset 850h

This register applies to GPP_H13 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.91 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_13)—Offset 854h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 21h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	21h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.92 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_14)—Offset 860h

This register applies to GPP_H14 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.93 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_14)—Offset 864h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 22h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	22h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.94 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_15)—Offset 870h

This register applies to GPP_H15 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.95 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_15)—Offset 874h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 23h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	23h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.96 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_16)—Offset 880h

This register applies to GPP_H16 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.97 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_16)—Offset 884h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 24h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	24h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.98 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_17)—Offset 890h

This register applies to GPP_H17 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.99 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_17)—Offset 894h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 25h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	25h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.100 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_18)—Offset 8A0h

This register applies to GPP_H18 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.101 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_18)—Offset 8A4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 26h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	26h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.102 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_19)—Offset 8B0h

This register applies to GPP_H19 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.103 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_19)—Offset 8B4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 27h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	27h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.104 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_20)—Offset 8C0h

This register applies to GPP_H20 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.105 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_20)—Offset 8C4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 28h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	28h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.106 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_21)—Offset 8D0h

This register applies to GPP_H21 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.107 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_21)—Offset 8D4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 29h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	29h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.108 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_22)—Offset 8E0h

This register applies to GPP_H22 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.109 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_22)—Offset 8E4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 2Ah

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	2Ah RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.110 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_H_23)—Offset 8F0h

This register applies to GPP_H23 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.111 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_H_23)—Offset 8F4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 2Bh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_H_0.
9:8	0h RW	Reserved.
7:0	2Bh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_H_0.

27.2.112 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_0)—Offset 900h

This register applies to GPP_D0 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.113 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_0)—Offset 904h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2Ch

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved. NOTES: 1. The 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily.
9:8	0h RW	Reserved.
7:0	2Ch RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

27.2.114 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_1)—Offset 910h

This register applies to GPP_D1 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.115 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_1)—Offset 914h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2Dh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	2Dh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.116 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_2)—Offset 920h

This register applies to GPP_D2 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.117 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_2)—Offset 924h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2Eh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	2Eh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.118 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_3)—Offset 930h

This register applies to GPP_D3 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.119 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_3)—Offset 934h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 2Fh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	2Fh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.120 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_4)—Offset 940h

This register applies to GPP_D4 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.121 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_4)—Offset 944h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 30h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	30h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.122 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_5)—Offset 950h

This register applies to GPP_D5 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.123 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_5)—Offset 954h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 31h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	31h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.124 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_6)—Offset 960h

This register applies to GPP_D6 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.125 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_6)—Offset 964h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 32h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	32h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.126 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_7)—Offset 970h

This register applies to GPP_D7 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.127 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_7)—Offset 974h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 33h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	33h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.128 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_8)—Offset 980h

This register applies to GPP_D8 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.129 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_8)—Offset 984h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 34h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	34h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.130 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_9)—Offset 990h

This register applies to GPP_D9 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.131 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_9)—Offset 994h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 3C35h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	Fh RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	35h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.132 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_10)—Offset 9A0h

This register applies to GPP_D10 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.133 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_10)—Offset 9A4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 3C36h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	Fh RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	36h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.134 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_11)—Offset 9B0h

This register applies to GPP_D11 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.135 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_11)—Offset 9B4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 3C37h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	Fh RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	37h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.136 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_12)—Offset 9C0h

This register applies to GPP_D12 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.137 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_12)—Offset 9C4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 3C38h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	Fh RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	38h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.138 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_13)—Offset 9D0h

This register applies to GPP_D13 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.139 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_13)—Offset 9D4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 39h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	39h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.140 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_14)—Offset 9E0h

This register applies to GPP_D14 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.141 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_14)—Offset 9E4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 3Ah

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	3Ah RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.142 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_15)—Offset 9F0h

This register applies to GPP_D15 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.143 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_15)—Offset 9F4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 3Bh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	3Bh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.144 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_16)—Offset A00h

This register applies to GPP_D16 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.145 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_16)—Offset A04h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 3Ch

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	3Ch RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.146 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_17)—Offset A10h

This register applies to GPP_D17 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.147 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_17)—Offset A14h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 3Dh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	3Dh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.148 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_18)—Offset A20h

This register applies to GPP_D18 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.149 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_18)—Offset A24h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 3Eh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	3Eh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.150 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_D_19)—Offset A30h

This register applies to GPP_D19 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.151 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_D_19)—Offset A34h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 3Fh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_D_0.
9:8	0h RW	Reserved.
7:0	3Fh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_D_0.

27.2.152 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_4)—Offset A90h

This register applies to GPP_U4 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.153 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_4)—Offset A94h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 44h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved NOTES: 1.The 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily.
9:8	0h RW	Reserved.
7:0	44h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

27.2.154 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_U_5)—Offset AA0h

This register applies to GPP_U5 and has the same description as PAD_CFG_DW0_GPP_H_0

27.2.155 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_U_5)—Offset AA4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 45h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_U_4.
9:8	0h RW	Reserved.
7:0	45h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_U_4.

27.3 GPIO Community 2 Registers Summary

GPIO pins are grouped into different Community (e.g. Community 0, Community 1, etc.). Each Community consists of one or more GPIO groups.
This section covers registers for Community 2, which consists of GPD group.

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).
Note that each GPIO Community has a different PortID. See the Primary to Sideband Bridge Section in Vol1 for PortID info.

Table 12. Summary of GPIO Community 2 Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8h	Bh	Family Base Address (FAMBAR)—Offset 8h	300h
Ch	Fh	Pad Base Address (PADBAR)—Offset Ch	600h
10h	13h	Miscellaneous Configuration (MISCCFG)—Offset 10h	34043200h
20h	23h	Pad Ownership (PAD_OWN_DSW_0)—Offset 20h	0h
24h	27h	Pad Ownership (PAD_OWN_DSW_1)—Offset 24h	0h
80h	83h	Pad Configuration Lock (PADCFGLOCK_DSW_0)—Offset 80h	0h
84h	87h	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_DSW_0)—Offset 84h	0h
B0h	B3h	Host Software Pad Ownership (HOSTSW_OWN_DSW_0)—Offset B0h	0h
100h	103h	GPI Interrupt Status (GPI_IS_DSW_0)—Offset 100h	0h
120h	123h	GPI Interrupt Enable (GPI_IE_DSW_0)—Offset 120h	0h
140h	143h	GPI General Purpose Events Status (GPI_GPE_STS_DSW_0)—Offset 140h	0h
160h	163h	GPI General Purpose Events Enable (GPI_GPE_EN_DSW_0)—Offset 160h	0h
700h	703h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_0)—Offset 700h	4000X00h See register for X value
704h	707h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_0)—Offset 704h	3050h
710h	713h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_1)—Offset 710h	4000X00h See register for X value

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
714h	717h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_1)—Offset 714h	3C51h
720h	723h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_2)—Offset 720h	4000X00h See register for X value
724h	727h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_2)—Offset 724h	3C52h
730h	733h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_3)—Offset 730h	4000X00h See register for X value
734h	737h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_3)—Offset 734h	3053h
738h	73Bh	Pad Configuration DW2 (PAD_CFG_DW2_GPD_3)—Offset 738h	10h
740h	743h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_4)—Offset 740h	4000X00h See register for X value
744h	747h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_4)—Offset 744h	54h
750h	753h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_5)—Offset 750h	4000X00h See register for X value
754h	757h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_5)—Offset 754h	55h
760h	763h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_6)—Offset 760h	4000X00h See register for X value
764h	767h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_6)—Offset 764h	56h
770h	773h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_7)—Offset 770h	4000X00h See register for X value
774h	777h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_7)—Offset 774h	57h
780h	783h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_8)—Offset 780h	4000X00h See register for X value
784h	787h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_8)—Offset 784h	58h
790h	793h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_9)—Offset 790h	0h
794h	797h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_9)—Offset 794h	59h
7A0h	7A3h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_10)—Offset 7A0h	4000X00h See register for X value
7A4h	7A7h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_10)—Offset 7A4h	5Ah
7B0h	7B3h	Pad Configuration DW0 (PAD_CFG_DW0_GPD_11)—Offset 7B0h	4000X00h See register for X value
7B4h	7B7h	Pad Configuration DW1 (PAD_CFG_DW1_GPD_11)—Offset 7B4h	5Bh

27.3.1 Family Base Address (FAMBAR)—Offset 8h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 300h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

27.3.2 Pad Base Address (PADBAR)—Offset Ch

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 600h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	600h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

27.3.3 Miscellaneous Configuration (MISCCFG)—Offset 10h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 34043200h

Bit Range	Default & Access	Field Name (ID): Description
31:24	34h RW	**GPIO Driver Mode Interrupt Select (GPDMINTSEL):** IRQ globally for all pads (GPI_IS with corresponding GPI_IE enable). 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255
23:20	0h RO	Reserved.
19:16	4h RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[87:64]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[67:66]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[87:64]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[71:64]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[75:64]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[71:64]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[87:64]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[83:64]; other GPE bits not used. 8h = GPP_U[5:4] mapped to GPE[69:68]; other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[87:64]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[87:64]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[87:64]; other GPE bits not used. Dh - Fh: Reserved
15:12	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[55:32]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[35:34]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[55:32]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[39:32]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[43:32]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[39:32]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[55:32]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[51:32]; other GPE bits not used. 8h = GPP_U[5:4] mapped to GPE[37:36]; other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[55:32]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[55:32]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[55:32]; other GPE bits not used. Dh - Fh: Reserved
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[23:0]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[3:2]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[23:0]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[7:0]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[11:0]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[7:0]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[23:0]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[19:0]; other GPE bits not used. 8h = GPP_U[5:4] mapped to GPE[5:4];other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[23:0]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[23:0]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[23:0]; other GPE bits not used. Dh - Fh: Reserved
7:2	0h RO	Reserved.
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specify whether the GPIO Community should take part in partition clock gating. 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specifies whether the GPIO Community should perform local clock gating. 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating

27.3.4 Pad Ownership (PAD_OWN_DSW_0)—Offset 20h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:28	0h RW	**Pad Ownership (PAD_OWN_GPD_7):** Same description as bits[1:0].
27:26	0h RO	Reserved.
25:24	0h RW	**Pad Ownership (PAD_OWN_GPD_6):** Same description as bits[1:0].
23:22	0h RO	Reserved.
21:20	0h RW	**Pad Ownership (PAD_OWN_GPD_5):** Same description as bits[1:0].
19:18	0h RO	Reserved.
17:16	0h RW	**Pad Ownership (PAD_OWN_GPD_4):** Same description as bits[1:0].
15:14	0h RO	Reserved.
13:12	0h RW	**Pad Ownership (PAD_OWN_GPD_3):** Same description as bits[1:0].
11:10	0h RO	Reserved.
9:8	0h RW	**Pad Ownership (PAD_OWN_GPD_2):** Same description as bits[1:0].
7:6	0h RO	Reserved.
5:4	0h RW	**Pad Ownership (PAD_OWN_GPD_1):** Same description as bits[1:0].
3:2	0h RO	Reserved.
1:0	0h RW	**Pad Ownership (PAD_OWN_GPD_0):** 00 = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership 01 = ME GPIO Mode. ME has ownership of the pad. 10 = ISH GPIO Mode. ME has ownership of the pad 11 = Reserved

27.3.5 Pad Ownership (PAD_OWN_DSW_1)—Offset 24h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:12	0h RW	**Pad Ownership (PAD_OWN_GPD_11):** Same description as bits[1:0] in PAD_OWN_DSW_0 register.
11:10	0h RO	Reserved.
9:8	0h RW	**Pad Ownership (PAD_OWN_GPD_10):** Same description as bits[1:0] in PAD_OWN_DSW_0 register.
7:6	0h RO	Reserved.
5:4	0h RW	**Pad Ownership (PAD_OWN_GPD_9):** Same description as bits[1:0] in PAD_OWN_DSW_0 register.
3:2	0h RO	Reserved.
1:0	0h RW	**Pad Ownership (PAD_OWN_GPD_8):** Same description as bits[1:0] in PAD_OWN_DSW_0 register.

27.3.6 Pad Configuration Lock (PADCFGLOCK_DSW_0)—Offset 80h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_11):** Same description as bit 0.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_10):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_9):** Same description as bit 0.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_8):** Same description as bit 0.
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_7):** Same description as bit 0.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_6):** Same description as bit 0.
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_5):** Same description as bit 0.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_4):** Same description as bit 0.
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_3):** Same description as bit 0.
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_2):** Same description as bit 0.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_1):** Same description as bit 0.
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPD_0):** Pad Configuration Lock locks specific register fields in the GPP specific registers from being configured. The registers affected become Read-Only and software writes to these registers have no effect. 0 = Unlock 1 = Lock the following register fields as read-only (RO): - Pad Configuration registers (exclude GPIOTXState) - GPI_NMI_EN Register (if implemented) - GPI_SMI_EN Register (if implemented) - GPI_GPE_EN Register (if implemented) When PadCfgLock is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

27.3.7 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_DSW_0)—Offset 84h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_11):** Same description as bit 0.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_10):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_9):** Same description as bit 0.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_8):** Same description as bit 0.
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_7):** Same description as bit 0.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_6):** Same description as bit 0.
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_5):** Same description as bit 0.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_4):** Same description as bit 0.
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_3):** Same description as bit 0.
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_2):** Same description as bit 0.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_1):** Same description as bit 0.
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPD_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) When PadCfgLockTx is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

27.3.8 Host Software Pad Ownership (HOSTSW_OWN_DSW_0)—Offset B0h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_11):** Same description as bit 0.
10	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_10):** Same description as bit 0.
9	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_9):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_8):** Same description as bit 0.
7	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_7):** Same description as bit 0.
6	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_6):** Same description as bit 0.
5	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_5):** Same description as bit 0.
4	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_4):** Same description as bit 0.
3	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_3):** Same description as bit 0.
2	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_2):** Same description as bit 0.
1	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_1):** Same description as bit 0.
0	0h RW	**HostSW_Own (HOSTSW_OWN_GPD_0):** This register determines the appropriate host status bit update when a pad is under host ownership. 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked.

27.3.9 GPI Interrupt Status (GPI_IS_DSW_0)—Offset 100h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_11):** Same description as bit 0.
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_10):** Same description as bit 0.
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_9):** Same description as bit 0.
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_8):** Same description as bit 0.
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_7):** Same description as bit 0.
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_6):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_5):** Same description as bit 0.
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_4):** Same description as bit 0.
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_3):** Same description as bit 0.
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_2):** Same description as bit 0.
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_1):** Same description as bit 0.
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPD_0):** GPI Interrupt Status (GPI_INT_STS) This bit is set to '1' by hardware when either an edge or a level event is detected (See RxEdCfg RxInv) on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode - HOSTSW_OWN = 1 (i.e. Host GPIO Driver Mode). Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x].

27.3.10 GPI Interrupt Enable (GPI_IE_DSW_0)—Offset 120h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_11):** Same description as bit 0.
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_10):** Same description as bit 0.
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_9):** Same description as bit 0.
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_8):** Same description as bit 0.
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_7):** Same description as bit 0.
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_6):** Same description as bit 0.
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_5):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_4):** Same description as bit 0.
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_3):** Same description as bit 0.
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_2):** Same description as bit 0.
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_1):** Same description as bit 0.
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPD_0):** This bit is used to enable/disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation

27.3.11 GPI General Purpose Events Status (GPI_GPE_STS_DSW_0)—Offset 140h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_11):** Same description as bit 0.
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_10):** Same description as bit 0.
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_9):** Same description as bit 0.
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_8):** Same description as bit 0.
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_7):** Same description as bit 0.
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_6):** Same description as bit 0.
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_5):** Same description as bit 0.
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_4):** Same description as bit 0.
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_3):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_2):** Same description as bit 0.
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_1):** Same description as bit 0.
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPD_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: - If the system is in an S3-S5 state, the event will also wake the system. - If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be generated, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS.

27.3.12 GPI General Purpose Events Enable (GPI_GPE_EN_DSW_0)—Offset 160h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_11):** Same description as bit 0.
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_10):** Same description as bit 0.
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_9):** Same description as bit 0.
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_8):** Same description as bit 0.
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_7):** Same description as bit 0.
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_6):** Same description as bit 0.
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_5):** Same description as bit 0.
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_4):** Same description as bit 0.
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_3):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_2):** Same description as bit 0.
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_1):** Same description as bit 0.
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPD_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'.

27.3.13 Pad Configuration DW0 (PAD_CFG_DW0_GPD_0)—Offset 700h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 4000X00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset GPIO pad register fields in PAD_CFG_DW0 and PAD_CFG_DW1 registers. This register can be used for Sx isolation of the associated signal if needed. 00 = DSW_PWROK# 01 = Host deep reset. This reset occurs when any of the following occur: Host reset (with or without power cycle) is initiated, Global reset is initiated, or Deep Sx entry. This reset does NOT occur as part of S3/S4/S5 entry. 10 = PLTRST# 11 = RSMRST#
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	Reserved.
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge

Bit Range	Default & Access	Field Name (ID): Description
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:11	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
10	-- RO/V	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO controls the Pad 1h = Function 1, if applicable, controls the Pad Default value is determined by the default functionality of the pad.
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0'.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	Reserved.
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

27.3.14 Pad Configuration DW1 (PAD_CFG_DW1_GPD_0)—Offset 704h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 3050h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	Ch RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved. NOTES: 1. The 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily.
9:8	0h RO	Reserved.
7:0	50h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

27.3.15 Pad Configuration DW0 (PAD_CFG_DW0_GPD_1)—Offset 710h

This register applies to GPD1 and has the same description as PAD_CFG_DW0_GPD_0.

27.3.16 Pad Configuration DW1 (PAD_CFG_DW1_GPD_1)—Offset 714h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 3C51h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	Fh RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	0h RO	Reserved.
7:0	51h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

27.3.17 Pad Configuration DW0 (PAD_CFG_DW0_GPD_2)—Offset 720h

This register applies to GPD2 and has the same description as PAD_CFG_DW0_GPD_0.

27.3.18 Pad Configuration DW1 (PAD_CFG_DW1_GPD_2)—Offset 724h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 3C52h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	Fh RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	0h RO	Reserved.
7:0	52h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

27.3.19 Pad Configuration DW0 (PAD_CFG_DW0_GPD_3)—Offset 730h

This register applies to GPD3 and has the same description as PAD_CFG_DW0_GPD_0.

27.3.20 Pad Configuration DW1 (PAD_CFG_DW1_GPD_3)—Offset 734h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 3053h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	Ch RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	0h RO	Reserved.
7:0	53h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

27.3.21 Pad Configuration DW2 (PAD_CFG_DW2_GPD_3)—Offset 738h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 10h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4:1	8h RW	**Debounce duration (DEBOUNCE):** The debounce duration of value should be not less than 3. In other words, the value should not be any of 0, 1 and 2. The debounce time should be calculated as (2^debounce) * (glitch filter clock period) For example, when RTC clock (32 KHz) is used for glitch filter and debounce duration is set to 4b1011, the debounce time is (2 ^ 11) * (31.25 us) = 64ms
0	0h RW	**Debounce Enable (DEBEN):** This bit enables or disables the debouncer with the pad. 1 = Enable the debouncer of the pad 0 = Disable the debouncer of the pad

27.3.22 Pad Configuration DW0 (PAD_CFG_DW0_GPD_4)—Offset 740h

This register applies to GPD4 and has the same description as PAD_CFG_DW0_GPD_0.

27.3.23 Pad Configuration DW1 (PAD_CFG_DW1_GPD_4)—Offset 744h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 54h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	0h RO	Reserved.
7:0	54h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

27.3.24 Pad Configuration DW0 (PAD_CFG_DW0_GPD_5)—Offset 750h

This register applies to GPD5 and has the same description as PAD_CFG_DW0_GPD_0.

27.3.25 Pad Configuration DW1 (PAD_CFG_DW1_GPD_5)—Offset 754h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 55h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	0h RO	Reserved.
7:0	55h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

27.3.26 Pad Configuration DW0 (PAD_CFG_DW0_GPD_6)—Offset 760h

This register applies to GPD6 and has the same description as PAD_CFG_DW0_GPD_0.

27.3.27 Pad Configuration DW1 (PAD_CFG_DW1_GPD_6)—Offset 764h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)	**Device:** **Function:**

Default: 56h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	0h RO	Reserved.
7:0	56h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

27.3.28 Pad Configuration DW0 (PAD_CFG_DW0_GPD_7)—Offset 770h

This register applies to GPD7 and has the same description as PAD_CFG_DW0_GPD_0.

27.3.29 Pad Configuration DW1 (PAD_CFG_DW1_GPD_7)—Offset 774h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)	**Device:** **Function:**

Default: 57h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	0h RO	Reserved.
7:0	57h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

27.3.30 Pad Configuration DW0 (PAD_CFG_DW0_GPD_8)—Offset 780h

This register applies to GPD8 and has the same description as PAD_CFG_DW0_GPD_0.

27.3.31 Pad Configuration DW1 (PAD_CFG_DW1_GPD_8)—Offset 784h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 58h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	0h RO	Reserved.
7:0	58h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

27.3.32 Pad Configuration DW0 (PAD_CFG_DW0_GPD_9)—Offset 790h

This register applies to GPD9 and has the same description as PAD_CFG_DW0_GPD_0.

27.3.33 Pad Configuration DW1 (PAD_CFG_DW1_GPD_9)—Offset 794h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)	**Device:** **Function:**

Default: 59h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	0h RO	Reserved.
7:0	59h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

27.3.34 Pad Configuration DW0 (PAD_CFG_DW0_GPD_10)—Offset 7A0h

This register applies to GPD10 and has the same description as PAD_CFG_DW0_GPD_0.

27.3.35 Pad Configuration DW1 (PAD_CFG_DW1_GPD_10)—Offset 7A4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)	**Device:** **Function:**

Default: 5Ah

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	0h RO	Reserved.
7:0	5Ah RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

27.3.36 Pad Configuration DW0 (PAD_CFG_DW0_GPD_11)—Offset 7B0h

This register applies to GPD11 and has the same description as PAD_CFG_DW0_GPD_0.

27.3.37 Pad Configuration DW1 (PAD_CFG_DW1_GPD_11)—Offset 7B4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 5Bh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPD_0.
9:8	0h RO	Reserved.
7:0	5Bh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPD_0.

27.4 GPIO Community 4 Registers Summary

GPIO pins are grouped into different Community (e.g. Community 0, Community 1, etc.). Each Community consists of one or more GPIO groups.
This section covers registers for Community 4, which consists of GPP_C, GPP_E, and GPP_F groups.

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).
Note that each GPIO Community has a different PortID. See the Primary to Sideband Bridge Section in Vol1 for PortID info.

Table 13. Summary of GPIO Community 4 Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8h	Bh	Family Base Address (FAMBAR)—Offset 8h	300h
Ch	Fh	Pad Base Address (PADBAR)—Offset Ch	700h
10h	13h	Miscellaneous Configuration (MISCCFG)—Offset 10h	36043200h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
20h	23h	Pad Ownership (PAD_OWN_GPP_C_0)—Offset 20h	0h
24h	27h	Pad Ownership (PAD_OWN_GPP_C_1)—Offset 24h	0h
28h	2Bh	Pad Ownership (PAD_OWN_GPP_C_2)—Offset 28h	0h
2Ch	2Fh	Pad Ownership (PAD_OWN_GPP_F_0)—Offset 2Ch	0h
30h	33h	Pad Ownership (PAD_OWN_GPP_F_1)—Offset 30h	0h
34h	37h	Pad Ownership (PAD_OWN_GPP_F_2)—Offset 34h	0h
40h	43h	Pad Ownership (PAD_OWN_GPP_E_0)—Offset 40h	0h
44h	47h	Pad Ownership (PAD_OWN_GPP_E_1)—Offset 44h	0h
48h	4Bh	Pad Ownership (PAD_OWN_GPP_E_2)—Offset 48h	0h
80h	83h	Pad Configuration Lock (PADCFGLOCK_GPP_C_0)—Offset 80h	0h
84h	87h	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_C_0)—Offset 84h	0h
88h	8Bh	Pad Configuration Lock (PADCFGLOCK_GPP_F_0)—Offset 88h	0h
8Ch	8Fh	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_F_0)—Offset 8Ch	0h
98h	9Bh	Pad Configuration Lock (PADCFGLOCK_GPP_E_0)—Offset 98h	0h
9Ch	9Fh	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_E_0)—Offset 9Ch	0h
B0h	B3h	Host Software Pad Ownership (HOSTSW_OWN_GPP_C_0)—Offset B0h	0h
B4h	B7h	Host Software Pad Ownership (HOSTSW_OWN_GPP_F_0)—Offset B4h	0h
BCh	BFh	Host Software Pad Ownership (HOSTSW_OWN_GPP_E_0)—Offset BCh	0h
100h	103h	GPI Interrupt Status (GPI_IS_GPP_C_0)—Offset 100h	0h
104h	107h	GPI Interrupt Status (GPI_IS_GPP_F_0)—Offset 104h	0h
10Ch	10Fh	GPI Interrupt Status (GPI_IS_GPP_E_0)—Offset 10Ch	0h
120h	123h	GPI Interrupt Enable (GPI_IE_GPP_C_0)—Offset 120h	0h
124h	127h	GPI Interrupt Enable (GPI_IE_GPP_F_0)—Offset 124h	0h
12Ch	12Fh	GPI Interrupt Enable (GPI_IE_GPP_E_0)—Offset 12Ch	0h
140h	143h	GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_0)—Offset 140h	0h
144h	147h	GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_0)—Offset 144h	0h
14Ch	14Fh	GPI General Purpose Events Status (GPI_GPE_STS_GPP_E_0)—Offset 14Ch	0h
160h	163h	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_0)—Offset 160h	0h
164h	167h	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_0)—Offset 164h	0h
16Ch	16Fh	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_E_0)—Offset 16Ch	0h
180h	183h	SMI Status (GPI_SMI_STS_GPP_C_0)—Offset 180h	0h
18Ch	18Fh	SMI Status (GPI_SMI_STS_GPP_E_0)—Offset 18Ch	0h
1A0h	1A3h	SMI Enable (GPI_SMI_EN_GPP_C_0)—Offset 1A0h	0h
1ACh	1AFh	SMI Enable (GPI_SMI_EN_GPP_E_0)—Offset 1ACh	0h
1C0h	1C3h	NMI Status (GPI_NMI_STS_GPP_C_0)—Offset 1C0h	0h
1CCh	1CFh	NMI Status (GPI_NMI_STS_GPP_E_0)—Offset 1CCh	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1E0h	1E3h	NMI Enable (GPI_NMI_EN_GPP_C_0)—Offset 1E0h	0h
1ECh	1EFh	NMI Enable (GPI_NMI_EN_GPP_E_0)—Offset 1ECh	0h
700h	703h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_0)—Offset 700h	0h
704h	707h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_0)—Offset 704h	6Eh
710h	713h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_1)—Offset 710h	0h
714h	717h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_1)—Offset 714h	6Fh
720h	723h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_2)—Offset 720h	0h
724h	727h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_2)—Offset 724h	70h
730h	733h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_3)—Offset 730h	0h
734h	737h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_3)—Offset 734h	71h
740h	743h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_4)—Offset 740h	0h
744h	747h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_4)—Offset 744h	72h
750h	753h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_5)—Offset 750h	0h
754h	757h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_5)—Offset 754h	73h
760h	763h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_6)—Offset 760h	0h
764h	767h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_6)—Offset 764h	74h
770h	773h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_7)—Offset 770h	0h
774h	777h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_7)—Offset 774h	75h
780h	783h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_8)—Offset 780h	0h
784h	787h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_8)—Offset 784h	76h
790h	793h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_9)—Offset 790h	0h
794h	797h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_9)—Offset 794h	77h
7A0h	7A3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_10)—Offset 7A0h	0h
7A4h	7A7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_10)—Offset 7A4h	18h
7B0h	7B3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_11)—Offset 7B0h	0h
7B4h	7B7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_11)—Offset 7B4h	19h
7C0h	7C3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_12)—Offset 7C0h	0h
7C4h	7C7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_12)—Offset 7C4h	1Ah
7D0h	7D3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_13)—Offset 7D0h	0h
7D4h	7D7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_13)—Offset 7D4h	1Bh
7E0h	7E3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_14)—Offset 7E0h	0h
7E4h	7E7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_14)—Offset 7E4h	1Ch
7F0h	7F3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_15)—Offset 7F0h	0h
7F4h	7F7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_15)—Offset 7F4h	1Dh
800h	803h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_16)—Offset 800h	0h
804h	807h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_16)—Offset 804h	1Eh
810h	813h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_17)—Offset 810h	0h
814h	817h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_17)—Offset 814h	1Fh
820h	823h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_18)—Offset 820h	0h
824h	827h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_18)—Offset 824h	20h
830h	833h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_19)—Offset 830h	0h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
834h	837h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_19)—Offset 834h	21h
840h	843h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_20)—Offset 840h	0h
844h	847h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_20)—Offset 844h	22h
850h	853h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_21)—Offset 850h	0h
854h	857h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_21)—Offset 854h	23h
860h	863h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_22)—Offset 860h	0h
864h	867h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_22)—Offset 864h	24h
870h	873h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_23)—Offset 870h	0h
874h	877h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_23)—Offset 874h	25h
880h	883h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_0)—Offset 880h	4400XX00h See register for X value
884h	887h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_0)—Offset 884h	56h
890h	893h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_1)—Offset 890h	4400XX00h See register for X value
894h	897h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_1)—Offset 894h	3057h
8A0h	8A3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_2)—Offset 8A0h	4400XX00h See register for X value
8A4h	8A7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_2)—Offset 8A4h	58h
8B0h	8B3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_3)—Offset 8B0h	4400XX00h See register for X value
8B4h	8B7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_3)—Offset 8B4h	3059h
8C0h	8C3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_4)—Offset 8C0h	4400XX00h See register for X value
8C4h	8C7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_4)—Offset 8C4h	5Ah
8D0h	8D3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_5)—Offset 8D0h	4400XX00h See register for X value
8D4h	8D7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_5)—Offset 8D4h	5Bh
8E0h	8E3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_6)—Offset 8E0h	4400XX00h See register for X value
8E4h	8E7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_6)—Offset 8E4h	5Ch
8F0h	8F3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_7)—Offset 8F0h	4400XX00h See register for X value
8F4h	8F7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_7)—Offset 8F4h	5Dh
900h	903h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_8)—Offset 900h	4400XX00h See register for X value
904h	907h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_8)—Offset 904h	5Eh
910h	913h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_9)—Offset 910h	4400XX00h See register for X value
914h	917h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_9)—Offset 914h	5Fh

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
920h	923h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_10)—Offset 920h	4400XX00h See register for X value
924h	927h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_10)—Offset 924h	60h
930h	933h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_11)—Offset 930h	4400XX00h See register for X value
934h	937h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_11)—Offset 934h	61h
940h	943h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_12)—Offset 940h	4400XX00h See register for X value
944h	947h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_12)—Offset 944h	62h
950h	953h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_13)—Offset 950h	4400XX00h See register for X value
954h	957h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_13)—Offset 954h	63h
960h	963h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_14)—Offset 960h	4400XX00h See register for X value
964h	967h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_14)—Offset 964h	64h
970h	973h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_15)—Offset 970h	4400XX00h See register for X value
974h	977h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_15)—Offset 974h	65h
980h	983h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_16)—Offset 980h	4400XX00h See register for X value
984h	987h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_16)—Offset 984h	66h
990h	993h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_17)—Offset 990h	4400XX00h See register for X value
994h	997h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_17)—Offset 994h	67h
9A0h	9A3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_18)—Offset 9A0h	4400XX00h See register for X value
9A4h	9A7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_18)—Offset 9A4h	68h
9B0h	9B3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_19)—Offset 9B0h	4400XX00h See register for X value
9B4h	9B7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_19)—Offset 9B4h	69h
9C0h	9C3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_20)—Offset 9C0h	4400XX00h See register for X value
9C4h	9C7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_20)—Offset 9C4h	6Ah
9D0h	9D3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_21)—Offset 9D0h	4400XX00h See register for X value
9D4h	9D7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_21)—Offset 9D4h	6Bh
9E0h	9E3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_22)—Offset 9E0h	4400XX00h See register for X value
9E4h	9E7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_22)—Offset 9E4h	6Ch

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
9F0h	9F3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_23)—Offset 9F0h	4400XX00h See register for X value
9F4h	9F7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_23)—Offset 9F4h	6Dh
A70h	A73h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_0)—Offset A70h	4400XX00h See register for X value
A74h	A77h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_0)—Offset A74h	26h
A80h	A83h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_1)—Offset A80h	4400XX00h See register for X value
A84h	A87h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_1)—Offset A84h	27h
A90h	A93h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_2)—Offset A90h	4400XX00h See register for X value
A94h	A97h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_2)—Offset A94h	28h
AA0h	AA3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_3)—Offset AA0h	4400XX00h See register for X value
AA4h	AA7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_3)—Offset AA4h	29h
AB0h	AB3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_4)—Offset AB0h	4400XX00h See register for X value
AB4h	AB7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_4)—Offset AB4h	30h
AC0h	AC3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_5)—Offset AC0h	4400XX00h See register for X value
AC4h	AC7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_5)—Offset AC4h	31h
AD0h	AD3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_6)—Offset AD0h	4400XX00h See register for X value
AD4h	AD7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_6)—Offset AD4h	32h
AE0h	AE3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_7)—Offset AE0h	4400XX00h See register for X value
AE4h	AE7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_7)—Offset AE4h	33h
AF0h	AF3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_8)—Offset AF0h	4400XX00h See register for X value
AF4h	AF7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_8)—Offset AF4h	34h
B00h	B03h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_9)—Offset B00h	4400XX00h See register for X value
B04h	B07h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_9)—Offset B04h	35h
B10h	B13h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_10)—Offset B10h	4400XX00h See register for X value
B14h	B17h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_10)—Offset B14h	36h
B20h	B23h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_11)—Offset B20h	4400XX00h See register for X value
B24h	B27h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_11)—Offset B24h	37h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
B30h	B33h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_12)—Offset B30h	4400XX00h See register for X value
B34h	B37h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_12)—Offset B34h	38h
B40h	B43h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_13)—Offset B40h	4400XX00h See register for X value
B44h	B47h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_13)—Offset B44h	39h
B50h	B53h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_14)—Offset B50h	4400XX00h See register for X value
B54h	B57h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_14)—Offset B54h	3Ah
B60h	B63h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_15)—Offset B60h	4400XX00h See register for X value
B64h	B67h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_15)—Offset B64h	3Bh
B70h	B73h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_16)—Offset B70h	4400XX00h See register for X value
B74h	B77h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_16)—Offset B74h	3Ch
B80h	B83h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_17)—Offset B80h	4400XX00h See register for X value
B84h	B87h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_17)—Offset B84h	3Dh
B90h	B93h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_18)—Offset B90h	4400XX00h See register for X value
B94h	B97h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_18)—Offset B94h	3C3Eh
BA0h	BA3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_19)—Offset BA0h	4400XX00h See register for X value
BA4h	BA7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_19)—Offset BA4h	3C3Fh
BB0h	BB3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_20)—Offset BB0h	4400XX00h See register for X value
BB4h	BB7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_20)—Offset BB4h	3C40h
BC0h	BC3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_21)—Offset BC0h	4400XX00h See register for X value
BC4h	BC7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_21)—Offset BC4h	3C41h
BD0h	BD3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_22)—Offset BD0h	4400XX00h See register for X value
BD4h	BD7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_22)—Offset BD4h	1042h
BE0h	BE3h	Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_23)—Offset BE0h	4400XX00h See register for X value
BE4h	BE7h	Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_23)—Offset BE4h	43h

27.4.1 Family Base Address (FAMBAR)—Offset 8h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)	**Device:** **Function:**

Default: 300h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

27.4.2 Pad Base Address (PADBAR)—Offset Ch

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)	**Device:** **Function:**

Default: 700h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	700h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

27.4.3 Miscellaneous Configuration (MISCCFG)—Offset 10h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)	**Device:** **Function:**

Default: 36043200h

Bit Range	Default & Access	Field Name (ID): Description
31:24	36h RW	**GPIO Driver Mode Interrupt Select (GPDMINTSEL):** IRQ globally for all pads (GPI_IS with corresponding GPI_IE enable). 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255
23:20	0h RO	Reserved.
19:16	4h RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[87:64]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[67:66]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[87:64]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[71:64]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[75:64]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[71:64]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[87:64]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[83:64]; other GPE bits not used. 8h = GPP_U[5:4] mapped to GPE[69:68]; other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[87:64]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[87:64]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[87:64]; other GPE bits not used. Dh - Fh: Reserved
15:12	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[55:32]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[35:34]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[55:32]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[39:32]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[43:32]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[39:32]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[55:32]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[51:32]; other GPE bits not used. 8h = GPP_U[5:4] mapped to GPE[37:36]; other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[55:32]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[55:32]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[55:32]; other GPE bits not used. Dh - Fh: Reserved
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[23:0]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[3:2]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[23:0]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[7:0]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[11:0]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[7:0]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[23:0]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[19:0]; other GPE bits not used. 8h = GPP_U[5:4] mapped to GPE[5:4];other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[23:0]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[23:0]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[23:0]; other GPE bits not used. Dh - Fh: Reserved
7:2	0h RO	Reserved.
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specify whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specifies whether the GPIO Community should perform local clock gating. 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating

27.4.4 Pad Ownership (PAD_OWN_GPP_C_0)—Offset 20h

Same description as PAD_OWN_GPP_F_0, except that this register is for GPP_C[7:0].

27.4.5 Pad Ownership (PAD_OWN_GPP_C_1)—Offset 24h

Same description as PAD_OWN_GPP_F_0, except that this register is for GPP_C[15:8].

27.4.6 Pad Ownership (PAD_OWN_GPP_C_2)—Offset 28h

Same description as PAD_OWN_GPP_F_0, except that this register is for GPP_C[23:16].

27.4.7 Pad Ownership (PAD_OWN_GPP_F_0)—Offset 2Ch

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:28	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_7):** Same description as bits[1:0].
27:26	0h RO	Reserved.
25:24	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_6):** Same description as bits[1:0].
23:22	0h RO	Reserved.
21:20	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_5):** Same description as bits[1:0].
19:18	0h RO	Reserved.
17:16	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_4):** Same description as bits[1:0].
15:14	0h RO	Reserved.
13:12	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_3):** Same description as bits[1:0].
11:10	0h RO	Reserved.
9:8	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_2):** Same description as bits[1:0].

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	Reserved.
5:4	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_1):** Same description as bits[1:0].
3:2	0h RO	Reserved.
1:0	0h RW	**Pad Ownership (PAD_OWN_GPPC_F_0):** 00 = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIO Driver) has ownership of the pad. In Host GPIO Driver Mode (refer to HOSTSW_OWN), GPIO input event update is limited to GPI_STS update only. Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership 01 = ME GPIO Mode. ME has ownership of the pad. 10 = ISH GPIO Mode. ME has ownership of the pad 11 = Reserved

27.4.8 Pad Ownership (PAD_OWN_GPP_F_1)—Offset 30h

Same description as PAD_OWN_GPP_F_0, except that this register is for GPP_F[15:8]

27.4.9 Pad Ownership (PAD_OWN_GPP_F_2)—Offset 34h

Same description as PAD_OWN_GPP_F_0, except that this register is for GPP_F[23:16].

27.4.10 Pad Ownership (PAD_OWN_GPP_E_0)—Offset 40h

Same description as PAD_OWN_GPP_F_0, except that this register is for GPP_E[7:0].

27.4.11 Pad Ownership (PAD_OWN_GPP_E_1)—Offset 44h

Same description as PAD_OWN_GPP_F_0, except that this register is for GPP_E[15:8].

27.4.12 Pad Ownership (PAD_OWN_GPP_E_2)—Offset 48h

Same description as PAD_OWN_GPP_F_0, except that this register is for GPP_E[23:16].

27.4.13 Pad Configuration Lock (PADCFGLOCK_GPP_C_0)—Offset 80h

Same description as PADCFGLOCK_GPP_F_0 register, except this register applies to GPP_C[23:0]

27.4.14 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_C_0)—Offset 84h

Same description as PADCFGLOCKTX_GPP_F_0 register, except this register applies to GPP_C[23:0]

27.4.15 Pad Configuration Lock (PADCFGLOCK_GPP_F_0)—Offset 88h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_23):** Same description as bit 0.
22	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_22):** Same description as bit 0.
21	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_21):** Same description as bit 0.
20	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_20):** Same description as bit 0.
19	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_19):** Same description as bit 0.
18	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_18):** Same description as bit 0.
17	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_17):** Same description as bit 0.
16	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_16):** Same description as bit 0.
15	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_15):** Same description as bit 0.
14	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_14):** Same description as bit 0.
13	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_13):** Same description as bit 0.
12	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_12):** Same description as bit 0.
11	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_11):** Same description as bit 0.
10	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_10):** Same description as bit 0.
9	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_9):** Same description as bit 0.
8	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_8):** Same description as bit 0.
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_7):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_6):** Same description as bit 0.
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_5):** Same description as bit 0.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_4):** Same description as bit 0.
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_3):** Same description as bit 0.
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_2):** Same description as bit 0.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_1):** Same description as bit 0.
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPPC_F_0):** Pad Configuration Lock locks specific register fields in the GPP specific registers from being configured. The registers affected become Read-Only and software writes to these registers have no effect. 0 = Unlock 1 = Lock the following register fields as read-only (RO): - Pad Configuration registers (exclude GPIOTXState) - GPI_NMI_EN Register (if implemented) - GPI_SMI_EN Register (if implemented) - GPI_GPE_EN Register (if implemented) When PadCfgLock is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

27.4.16 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_F_0)—Offset 8Ch

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_23):** Same description as bit 0.
22	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_22):** Same description as bit 0.
21	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_21):** Same description as bit 0.
20	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_20):** Same description as bit 0.
19	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_19):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_18):** Same description as bit 0.
17	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_17):** Same description as bit 0.
16	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_16):** Same description as bit 0.
15	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_15):** Same description as bit 0.
14	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_14):** Same description as bit 0.
13	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_13):** Same description as bit 0.
12	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_12):** Same description as bit 0.
11	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_11):** Same description as bit 0.
10	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_10):** Same description as bit 0.
9	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_9):** Same description as bit 0.
8	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_8):** Same description as bit 0.
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_7):** Same description as bit 0.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_6):** Same description as bit 0.
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_5):** Same description as bit 0.
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_4):** Same description as bit 0.
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_3):** Same description as bit 0.
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_2):** Same description as bit 0.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_1):** Same description as bit 0.
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPPC_F_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) When PadCfgLockTx is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

27.4.17 Pad Configuration Lock (PADCFGLOCK_GPP_E_0)—Offset 98h

Same description as PADCFGLOCK_GPP_F_0 register, except this register applies to GPP_E[23:0]

27.4.18 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_E_0)—Offset 9Ch

Same description as PADCFGLOCKTX_GPP_F_0 register, except this register applies to GPP_E[23:0]

27.4.19 Host Software Pad Ownership (HOSTSW_OWN_GPP_C_0)—Offset B0h

Same description as HOSTSW_OWN_GPP_F_0 register, except that this register applies to GPP_C[23:0].

27.4.20 Host Software Pad Ownership (HOSTSW_OWN_GPP_F_0)—Offset B4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_23):** Same description as bit 0.
22	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_22):** Same description as bit 0.
21	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_21):** Same description as bit 0.
20	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_20):** Same description as bit 0.
19	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_19):** Same description as bit 0.
18	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_18):** Same description as bit 0.
17	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_17):** Same description as bit 0.
16	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_16):** Same description as bit 0.
15	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_15):** Same description as bit 0.
14	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_14):** Same description as bit 0.
13	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_13):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
12	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_12):** Same description as bit 0.
11	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_11):** Same description as bit 0.
10	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_10):** Same description as bit 0.
9	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_9):** Same description as bit 0.
8	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_8):** Same description as bit 0.
7	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_7):** Same description as bit 0.
6	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_6):** Same description as bit 0.
5	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_5):** Same description as bit 0.
4	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_4):** Same description as bit 0.
3	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_3):** Same description as bit 0.
2	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_2):** Same description as bit 0.
1	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_1):** Same description as bit 0.
0	0h RW	**HostSW_Own (HOSTSW_OWN_GPPC_F_0):** This register determines the appropriate host status bit update when a pad is under host ownership. 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited to GPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updates are masked.

27.4.21 Host Software Pad Ownership (HOSTSW_OWN_GPP_E_0)—Offset BCh

Same description as HOSTSW_OWN_GPP_F_0 register, except that this register applies to GPP_E[23:0].

27.4.22 GPI Interrupt Status (GPI_IS_GPP_C_0)—Offset 100h

Same description as GPI_IS_GPP_F_0 register, except that this register applies to GPP_C[23:0].

27.4.23 GPI Interrupt Status (GPI_IS_GPP_F_0)—Offset 104h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_23):** Same description as bit 0.
22	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_22):** Same description as bit 0.
21	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_21):** Same description as bit 0.
20	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_20):** Same description as bit 0.
19	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_19):** Same description as bit 0.
18	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_18):** Same description as bit 0.
17	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_17):** Same description as bit 0.
16	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_16):** Same description as bit 0.
15	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_15):** Same description as bit 0.
14	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_14):** Same description as bit 0.
13	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_13):** Same description as bit 0.
12	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_12):** Same description as bit 0.
11	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_11):** Same description as bit 0.
10	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_10):** Same description as bit 0.
9	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_9):** Same description as bit 0.
8	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_8):** Same description as bit 0.
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_7):** Same description as bit 0.
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_6):** Same description as bit 0.
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_5):** Same description as bit 0.
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_4):** Same description as bit 0.
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_3):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_2):** Same description as bit 0.
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_1):** Same description as bit 0.
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPPC_F_0):** GPI Interrupt Status (GPI_INT_STS) This bit is set to '1' by hardware when either an edge or a level event is detected on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode - HOSTSW_OWN = 1 (i.e. Host GPIO Driver Mode). Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x].

27.4.24 GPI Interrupt Status (GPI_IS_GPP_E_0)—Offset 10Ch

Same description as GPI_IS_GPP_F_0 register, except that this register applies to GPP_E[23:0].

27.4.25 GPI Interrupt Enable (GPI_IE_GPP_C_0)—Offset 120h

Same description as GPI_IE_GPP_F_0 register, except that this register applies to GPP_C[23:0].

27.4.26 GPI Interrupt Enable (GPI_IE_GPP_F_0)—Offset 124h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_23):** Same description as bit 0.
22	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_22):** Same description as bit 0.
21	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_21):** Same description as bit 0.
20	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_20):** Same description as bit 0.
19	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_19):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_18):** Same description as bit 0.
17	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_17):** Same description as bit 0.
16	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_16):** Same description as bit 0.
15	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_15):** Same description as bit 0.
14	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_14):** Same description as bit 0.
13	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_13):** Same description as bit 0.
12	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_12):** Same description as bit 0.
11	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_11):** Same description as bit 0.
10	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_10):** Same description as bit 0.
9	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_9):** Same description as bit 0.
8	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_8):** Same description as bit 0.
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_7):** Same description as bit 0.
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_6):** Same description as bit 0.
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_5):** Same description as bit 0.
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_4):** Same description as bit 0.
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_3):** Same description as bit 0.
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_2):** Same description as bit 0.
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_1):** Same description as bit 0.
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPPC_F_0):** This bit is used to enable/ disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation

27.4.27 GPI Interrupt Enable (GPI_IE_GPP_E_0)—Offset 12Ch

Same description as GPI_IE_GPP_F_0 register, except that this register applies to GPP_E[23:0].

27.4.28 GPI General Purpose Events Status (GPI_GPE_STS_GPP_C_0)—Offset 140h

Same description as PI_GPE_STS_GPP_F_0 register, except that this is for GPP_C[23:0].

27.4.29 GPI General Purpose Events Status (GPI_GPE_STS_GPP_F_0)—Offset 144h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_23):** Same description as bit 0.
22	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_22):** Same description as bit 0.
21	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_21):** Same description as bit 0.
20	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_20):** Same description as bit 0.
19	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_19):** Same description as bit 0.
18	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_18):** Same description as bit 0.
17	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_17):** Same description as bit 0.
16	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_16):** Same description as bit 0.
15	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_15):** Same description as bit 0.
14	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_14):** Same description as bit 0.
13	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_13):** Same description as bit 0.
12	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_12):** Same description as bit 0.
11	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_11):** Same description as bit 0.
10	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_10):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
9	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_9):** Same description as bit 0.
8	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_8):** Same description as bit 0.
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_7):** Same description as bit 0.
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_6):** Same description as bit 0.
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_5):** Same description as bit 0.
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_4):** Same description as bit 0.
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_3):** Same description as bit 0.
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_2):** Same description as bit 0.
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_1):** Same description as bit 0.
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPPC_F_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the corresponding enable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: - If the system is in an S3-S5 state, the event will also wake the system. - If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be generated, depending on the GPIRoutSCI bit for the corresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS.

27.4.30 GPI General Purpose Events Status (GPI_GPE_STS_GPP_E_0)—Offset 14Ch

Same description as PI_GPE_STS_GPP_F_0 register, except that this is for GPP_E[23:0].

27.4.31 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_C_0)—Offset 160h

Same description as GPI_GPE_EN_GPP_F_0 register, except that this is for GPP_C[23:0].

27.4.32 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_F_0)—Offset 164h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_23):** Same description as bit 0.
22	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_22):** Same description as bit 0.
21	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_21):** Same description as bit 0.
20	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_20):** Same description as bit 0.
19	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_19):** Same description as bit 0.
18	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_18):** Same description as bit 0.
17	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_17):** Same description as bit 0.
16	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_16):** Same description as bit 0.
15	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_15):** Same description as bit 0.
14	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_14):** Same description as bit 0.
13	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_13):** Same description as bit 0.
12	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_12):** Same description as bit 0.
11	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_11):** Same description as bit 0.
10	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_10):** Same description as bit 0.
9	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_9):** Same description as bit 0.
8	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_8):** Same description as bit 0.
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_7):** Same description as bit 0.
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_6):** Same description as bit 0.
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_5):** Same description as bit 0.
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_4):** Same description as bit 0.
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_3):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_2):** Same description as bit 0.
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_1):** Same description as bit 0.
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPPC_F_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note: The pad must also be routed for GPE functionality in order for GPE to be generated, i.e. the corresponding GPIRoutSCI must be set to '1'.

27.4.33 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_E_0)—Offset 16Ch

Same description as GPI_GPE_EN_GPP_F_0 register, except that this is for GPP_E[23:0].

27.4.34 SMI Status (GPI_SMI_STS_GPP_C_0)—Offset 180h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_C_23):** Same description as bit 22.
22	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_C_22):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to 1. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is 1, bit0 of this bit is locked down to read-only.
21:0	0h RO	Reserved.

27.4.35 SMI Status (GPI_SMI_STS_GPP_E_0)—Offset 18Ch

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_16):** Same description as bit 0.
15	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_15):** Same description as bit 0.
14	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_14):** Same description as bit 0.
13	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_13):** Same description as bit 0.
12:9	0h RO	Reserved.
8	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_8):** Same description as bit 0.
7	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_7):** Same description as bit 0.
6	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_6):** Same description as bit 0.
5	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_5):** Same description as bit 0.
4	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_4):** Same description as bit 0.
3	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_3):** Same description as bit 0.
2	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_2):** Same description as bit 0.
1	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_1):** Same description as bit 0.
0	0h RW/1C	**GPI SMI Status (GPI_SMI_STS_GPPC_E_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to 1. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is 1, bit0 of this bit is locked down to read-only.

27.4.36 SMI Enable (GPI_SMI_EN_GPP_C_0)—Offset 1A0h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_23):** Same description as bit 22.
22	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_C_22):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to 1. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is 1, bit0 of this bit is locked down to read-only.
21:0	0h RO	Reserved.

27.4.37 SMI Enable (GPI_SMI_EN_GPP_E_0)—Offset 1ACh

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_16):** Same description as bit 0.
15	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_15):** Same description as bit 0.
14	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_14):** Same description as bit 0.
13	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_13):** Same description as bit 0.
12:9	0h RO	Reserved.
8	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_8):** Same description as bit 0.
7	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_7):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_6):** Same description as bit 0.
5	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_5):** Same description as bit 0.
4	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_4):** Same description as bit 0.
3	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_3):** Same description as bit 0.
2	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_2):** Same description as bit 0.
1	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_1):** Same description as bit 0.
0	0h RW	**GPI SMI Enable (GPI_SMI_EN_GPPC_E_0):** This bit is used to enable/disable the generation of SMI when the corresponding GPI_SMI_STS bit is set. The pad must also be routed for SMI functionality in order for SMI to be generated, i.e. the corresponding GPIROUTSMI must be set to 1. 0 = disable SMI generation 1 = enable SMI generation Note: Each of the bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is 1, bit0 of this bit is locked down to read-only.

27.4.38 NMI Status (GPI_NMI_STS_GPP_C_0)—Offset 1C0h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_C_23):** Same description as bit 22.
22	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_C_22):** This bit is set to 1 by hardware when an edge event is detected on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode (PMode) - The corresponding GPIONMIRout is set to 1, i.e. programmed to route as NMI - The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). - The corresponding GPI_NMI_EN is set Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = There is no NMI event 1 = There is an NMI event
21:0	0h RO	Reserved.

27.4.39 NMI Status (GPI_NMI_STS_GPP_E_0)—Offset 1CCh

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_16):** Same description as bit 0.
15	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_15):** Same description as bit 0.
14	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_14):** Same description as bit 0.
13	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_13):** Same description as bit 0.
12:9	0h RO	Reserved.
8	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_8):** Same description as bit 0.
7	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_7):** Same description as bit 0.
6	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_6):** Same description as bit 0.
5	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_5):** Same description as bit 0.
4	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_4):** Same description as bit 0.
3	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_3):** Same description as bit 0.
2	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_2):** Same description as bit 0.
1	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_1):** Same description as bit 0.
0	0h RW/1C	**GPI NMI Status (GPI_NMI_STS_GPPC_E_0):** This bit is set to 1 by hardware when an edge event is detected on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode (PMode) - The corresponding GPIONMIRout is set to 1, i.e. programmed to route as NMI - The corresponding GPIOOwn[2:0] is '000' (i.e. ACPI GPIO Mode). - The corresponding GPI_NMI_EN is set Writing a value of 1 will clear the bit while writing a value of 0 has no effect. 0 = There is no NMI event 1 = There is an NMI event

27.4.40 NMI Enable (GPI_NMI_EN_GPP_C_0)—Offset 1E0h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_23):** Same description as bit 22.
22	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_C_22):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only.
21:0	0h RO	Reserved.

27.4.41 NMI Enable (GPI_NMI_EN_GPP_E_0)—Offset 1ECh

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:17	0h RO	Reserved.
16	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_16):** Same description as bit 0.
15	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_15):** Same description as bit 0.
14	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_14):** Same description as bit 0.
13	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_13):** Same description as bit 0.
12:9	0h RO	Reserved.
8	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_8):** Same description as bit 0.
7	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_7):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_6):** Same description as bit 0.
5	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_5):** Same description as bit 0.
4	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_4):** Same description as bit 0.
3	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_3):** Same description as bit 0.
2	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_2):** Same description as bit 0.
1	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_1):** Same description as bit 0.
0	0h RW	**GPI NMI Enable (GPI_NMI_EN_GPPC_E_0):** This bit is used to enable/disable the generation of NMI when the corresponding GPI_NMI_STS bit is set and its GPIROUTNMI is set. 0 = disable NMI generation 1 = enable NMI generation Each bit is lock-able dependent on the associated Pad Configuration register PadCfgLock setting. E.g. if the PadCfgLock of pad0 is '1', bit0 of this bit is locked down to read-only.

27.4.42 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_0)—Offset 700h

This register applies to GPP_C0 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.43 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_0)—Offset 704h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 6Eh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved. NOTES: 1. The 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily.
9:8	0h RW	Reserved.
7:0	6Eh RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

27.4.44 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_1)—Offset 710h

This register applies to GPP_C1 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.45 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_1)—Offset 714h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)	**Device:** **Function:**

Default: 6Fh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	6Fh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.46 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_2)—Offset 720h

This register applies to GPP_C2 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.47 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_2)—Offset 724h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 70h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	70h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.48 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_3)—Offset 730h

This register applies to GPP_C3 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.49 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_3)—Offset 734h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 71h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	71h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.50 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_4)—Offset 740h

This register applies to GPP_C4 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.51 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_4)—Offset 744h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 72h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	72h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.52 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_5)—Offset 750h

This register applies to GPP_C5 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.53 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_5)—Offset 754h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 73h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	73h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.54 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_6)—Offset 760h

This register applies to GPP_C6 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.55 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_6)—Offset 764h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 74h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	74h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.56 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_7)—Offset 770h

This register applies to GPP_C7 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.57 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_7)—Offset 774h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 75h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	75h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.58 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_8)—Offset 780h

This register applies to GPP_C8 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.59 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_8)—Offset 784h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 76h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	76h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.60 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_9)—Offset 790h

This register applies to GPP_C9 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.61 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_9)—Offset 794h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 77h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	77h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.62 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_10)—Offset 7A0h

This register applies to GPP_C10 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.63 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_10)—Offset 7A4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 18h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	18h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.64 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_11)—Offset 7B0h

This register applies to GPP_C11 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.65 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_11)—Offset 7B4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 19h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	19h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.66 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_12)—Offset 7C0h

This register applies to GPP_C12 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.67 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_12)—Offset 7C4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 1Ah

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	1Ah RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.68 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_13)—Offset 7D0h

This register applies to GPP_C13 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.69 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_13)—Offset 7D4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 1Bh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	1Bh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.70 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_14)—Offset 7E0h

This register applies to GPP_C14 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.71 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_14)—Offset 7E4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 1Ch

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	1Ch RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.72 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_15)—Offset 7F0h

This register applies to GPP_C15 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.73 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_15)—Offset 7F4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 1Dh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	1Dh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.74 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_16)—Offset 800h

This register applies to GPP_C16 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.75 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_16)—Offset 804h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 1Eh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	1Eh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.76 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_17)—Offset 810h

This register applies to GPP_C17 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.77 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_17)—Offset 814h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 1Fh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	1Fh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.78 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_18)—Offset 820h

This register applies to GPP_C18 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.79 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_18)—Offset 824h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 20h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	20h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.80 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_19)—Offset 830h

This register applies to GPP_C19 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.81 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_19)—Offset 834h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 21h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	21h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.82 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_20)—Offset 840h

This register applies to GPP_C20 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.83 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_20)—Offset 844h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 22h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	22h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.84 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_21)—Offset 850h

This register applies to GPP_C21 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.85 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_21)—Offset 854h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 23h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	23h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.86 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_22)—Offset 860h

This register applies to GPP_C22 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.87 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_22)—Offset 864h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 24h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	24h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.88 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_C_23)—Offset 870h

This register applies to GPP_C23 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.89 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_C_23)—Offset 874h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 25h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_C_0.
9:8	0h RW	Reserved.
7:0	25h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_C_0.

27.4.90 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_0)—Offset 880h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 4400XX00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset GPIO pad register fields in various GPIO registers (PADCFGLOCK, PADCFGLOCKTX, GPI_IS, GPI_IE, GPI_GPE_STS, GPI_GPE_EN, GPI_SMI_STS, SPI_SMI_EN, GPI_NMI_STS, GPI_NMI_EN, PAD_CFG_DW0, and PAD_CFG_DW1). 00 = Global Reset or RSMRST# 01 = Host deep reset. This reset occurs when any of the following occur: Host reset (with or without power cycle) is initiated, Global reset is initiated, or Deep Sx entry. This reset does NOT occur as part of S3/S4/S5 entry. 10 = PLTRST# 11 = Global Reset
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	Reserved.
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled

Bit Range	Default & Access	Field Name (ID): Description
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	Reserved.
12:10	-- RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO controls the Pad 1h = Function 1, if applicable, control the Pad ... 7h = Function 7, if applicable, controls the Pad. Default value is determined by the default functionality of the pad.
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0'.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	Reserved.
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

27.4.91 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_0)—Offset 884h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 56h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved. NOTES: 1. The 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily.
9:8	0h RW	Reserved.
7:0	56h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

27.4.92 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_1)—Offset 890h

This register applies to GPP_F1 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.93 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_1)—Offset 894h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 3057h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	Ch RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	57h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.94 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_2)—Offset 8A0h

This register applies to GPP_F2 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.95 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_2)—Offset 8A4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 58h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	58h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.96 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_3)—Offset 8B0h

This register applies to GPP_F3 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.97 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_3)—Offset 8B4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 3059h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	Ch RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	59h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.98 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_4)—Offset 8C0h

This register applies to GPP_F4 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.99 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_4)—Offset 8C4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 5Ah

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	5Ah RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.100 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_5)—Offset 8D0h

This register applies to GPP_F5 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.101 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_5)—Offset 8D4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 5Bh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	5Bh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.102 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_6)—Offset 8E0h

This register applies to GPP_F6 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.103 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_6)—Offset 8E4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 5Ch

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	5Ch RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.104 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_7)—Offset 8F0h

This register applies to GPP_F7 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.105 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_7)—Offset 8F4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 5Dh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	5Dh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.106 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_8)—Offset 900h

This register applies to GPP_F8 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.107 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_8)—Offset 904h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)	**Device:** **Function:**

Default: 5Eh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	5Eh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.108 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_9)—Offset 910h

This register applies to GPP_F9 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.109 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_9)—Offset 914h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)	**Device:** **Function:**

Default: 5Fh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	5Fh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.110 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_10)—Offset 920h

This register applies to GPP_F10 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.111 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_10)—Offset 924h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 60h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	60h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.112 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_11)—Offset 930h

This register applies to GPP_F11 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.113 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_11)—Offset 934h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 61h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	61h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.114 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_12)—Offset 940h

This register applies to GPP_F12 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.115 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_12)—Offset 944h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 62h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	62h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.116 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_13)—Offset 950h

This register applies to GPP_F13 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.117 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_13)—Offset 954h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 63h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	63h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.118 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_14)—Offset 960h

This register applies to GPP_F14 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.119 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_14)—Offset 964h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 64h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	64h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.120 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_15)—Offset 970h

This register applies to GPP_F15 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.121 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_15)—Offset 974h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 65h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	65h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.122 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_16)—Offset 980h

This register applies to GPP_F16 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.123 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_16)—Offset 984h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 66h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	66h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.124 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_17)—Offset 990h

This register applies to GPP_F17 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.125 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_17)—Offset 994h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 67h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	67h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.126 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_18)—Offset 9A0h

This register applies to GPP_F18 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.127 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_18)—Offset 9A4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 68h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	68h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.128 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_19)—Offset 9B0h

This register applies to GPP_F19 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.129 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_19)—Offset 9B4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 69h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	69h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.130 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_20)—Offset 9C0h

This register applies to GPP_F20 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.131 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_20)—Offset 9C4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 6Ah

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	6Ah RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.132 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_21)—Offset 9D0h

This register applies to GPP_F21 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.133 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_21)—Offset 9D4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 6Bh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	6Bh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.134 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_22)—Offset 9E0h

This register applies to GPP_F22 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.135 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_22)—Offset 9E4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 6Ch

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	6Ch RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.136 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_F_23)—Offset 9F0h

This register applies to GPP_F23 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.137 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_F_23)—Offset 9F4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 6Dh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.
9:8	0h RW	Reserved.
7:0	6Dh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_F_0.

27.4.138 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_0)—Offset A70h

This register applies to GPP_E0 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.139 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_0)—Offset A74h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 26h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved NOTES: 1.The 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily.
9:8	0h RW	Reserved.
7:0	26h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

27.4.140 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_1)—Offset A80h

This register applies to GPP_E1 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.141 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_1)—Offset A84h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 27h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	27h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.142 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_2)—Offset A90h

This register applies to GPP_E2 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.143 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_2)—Offset A94h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 28h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	28h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.144 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_3)—Offset AA0h

This register applies to GPP_E3 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.145 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_3)—Offset AA4h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 29h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	29h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.146 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_4)—Offset AB0h

This register applies to GPP_E4 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.147 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_4)—Offset AB4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 30h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	30h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.148 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_5)—Offset AC0h

This register applies to GPP_E5 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.149 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_5)—Offset AC4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 31h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	31h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.150 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_6)—Offset AD0h

This register applies to GPP_E6 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.151 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_6)—Offset AD4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 32h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	32h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.152 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_7)—Offset AE0h

This register applies to GPP_E7 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.153 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_7)—Offset AE4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 33h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	33h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.154 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_8)—Offset AF0h

This register applies to GPP_E8 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.155 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_8)—Offset AF4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 34h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	34h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.156 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_9)—Offset B00h

This register applies to GPP_E9 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.157 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_9)—Offset B04h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 35h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	35h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.158 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_10)—Offset B10h

This register applies to GPP_E10 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.159 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_10)—Offset B14h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 36h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	36h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.160 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_11)—Offset B20h

This register applies to GPP_E11 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.161 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_11)—Offset B24h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 37h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	37h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.162 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_12)—Offset B30h

This register applies to GPP_E12 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.163 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_12)—Offset B34h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 38h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	38h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.164 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_13)—Offset B40h

This register applies to GPP_E13 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.165 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_13)—Offset B44h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 39h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	39h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.166 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_14)—Offset B50h

This register applies to GPP_E14 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.167 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_14)—Offset B54h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 3Ah

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	3Ah RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.168 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_15)—Offset B60h

This register applies to GPP_E15 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.169 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_15)—Offset B64h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 3Bh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	3Bh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.170 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_16)—Offset B70h

This register applies to GPP_E16 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.171 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_16)—Offset B74h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 3Ch

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	3Ch RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.172 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_17)—Offset B80h

This register applies to GPP_E17 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.173 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_17)—Offset B84h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 3Dh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	3Dh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.174 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_18)—Offset B90h

This register applies to GPP_E18 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.175 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_18)—Offset B94h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 3C3Eh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	Fh RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	3Eh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.176 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_19)—Offset BA0h

This register applies to GPP_E19 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.177 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_19)—Offset BA4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 3C3Fh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	Fh RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	3Fh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.178 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_20)—Offset BB0h

This register applies to GPP_E20 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.179 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_20)—Offset BB4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 3C40h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	Fh RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	40h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.180 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_21)—Offset BC0h

This register applies to GPP_E21 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.181 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_21)—Offset BC4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 3C41h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	Fh RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	41h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.182 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_22)—Offset BD0h

This register applies to GPP_E22 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.183 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_22)—Offset BD4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 1042h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	4h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	42h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.4.184 Pad Configuration DW0 (PAD_CFG_DW0_GPPC_E_23)—Offset BE0h

This register applies to GPP_E23 and has the same description as PAD_CFG_DW0_GPPC_F_0.

27.4.185 Pad Configuration DW1 (PAD_CFG_DW1_GPPC_E_23)—Offset BE4h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 43h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPPC_E_0.
9:8	0h RW	Reserved.
7:0	43h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPPC_E_0.

27.5 GPIO Community 5 Registers Summary

GPIO pins are grouped into different Community (e.g. Community 0, Community 1, etc.). Each Community consists of one or more GPIO groups.
This section covers registers for Community 5, which consists of GPP_R group.

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).
Note that each GPIO Community has a different PortID. See the Primary to Sideband Bridge Section in Vol1 for PortID info.

Table 14. Summary of GPIO Community 5 Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
8h	Bh	Family Base Address (FAMBAR)—Offset 8h	300h
Ch	Fh	Pad Base Address (PADBAR)—Offset Ch	700h
10h	13h	Miscellaneous Configuration (MISCCFG)—Offset 10h	37043200h
20h	23h	Pad Ownership (PAD_OWN_GPP_R_0)—Offset 20h	0h
80h	83h	Pad Configuration Lock (PADCFGLOCK_GPP_R_0)—Offset 80h	0h
84h	87h	Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_R_0)—Offset 84h	0h
B0h	B3h	Host Software Pad Ownership (HOSTSW_OWN_GPP_R_0)—Offset B0h	0h
100h	103h	GPI Interrupt Status (GPI_IS_GPP_R_0)—Offset 100h	0h
120h	123h	GPI Interrupt Enable (GPI_IE_GPP_R_0)—Offset 120h	0h
140h	143h	GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_0)—Offset 140h	0h
160h	163h	GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_0)—Offset 160h	0h
700h	703h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_0)—Offset 700h	4400XX00h See register for X value
704h	707h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_0)—Offset 704h	58h
710h	713h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_1)—Offset 710h	4400XX00h See register for X value
714h	717h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_1)—Offset 714h	3C59h

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
720h	723h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_2)—Offset 720h	4400XX00h See register for X value
724h	727h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_2)—Offset 724h	3C5Ah
730h	733h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_3)—Offset 730h	4400XX00h See register for X value
734h	737h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_3)—Offset 734h	3C5Bh
740h	743h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_4)—Offset 740h	4400XX00h See register for X value
744h	747h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_4)—Offset 744h	5Ch
750h	753h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_5)—Offset 750h	4400XX00h See register for X value
754h	757h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_5)—Offset 754h	5Dh
760h	763h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_6)—Offset 760h	4400XX00h See register for X value
764h	767h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_6)—Offset 764h	5Eh
770h	773h	Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_7)—Offset 770h	4400XX00h See register for X value
774h	777h	Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_7)—Offset 774h	5Fh

27.5.1 Family Base Address (FAMBAR)—Offset 8h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 300h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	300h RO	**Family Base Address (FAMBAR):** This field provides the starting byte-align address of Family0 register sets within a Community. It is meant for software to discover from where the very first Family register (i.e. Family0 register) starts to compute the next Families address offsets.

27.5.2 Pad Base Address (PADBAR)—Offset Ch

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 700h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:0	700h RO	**Pad Base Address (PADBAR):** This field provides the starting byte-align address of Pad0 register sets within a Community. It is meant for software to discover from where the very first Pad register (i.e. Pad0 register) starts to compute the next Pad address offsets.

27.5.3 Miscellaneous Configuration (MISCCFG)—Offset 10h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 37043200h

Bit Range	Default & Access	Field Name (ID): Description
31:24	37h RW	**GPIO Driver Mode Interrupt Select (GPDMINTSEL):** IRQ globally for all pads (GPI_IS with corresponding GPI_IE enable). 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255
23:20	0h RO	Reserved.
19:16	4h RW	**GPIO Group to GPE_DW2 assignment encoding (GPE0_DW2):** This register assigns a specific GPIO Group to the ACPI GPE0[95:64]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[87:64]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[67:66]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[87:64]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[71:64]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[75:64]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[71:64]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[87:64]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[83:64]; other GPE bits not used. 8h = GPP_U[5:4] mapped to GPE[69:68]; other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[87:64]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[87:64]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[87:64]; other GPE bits not used. Dh - Fh: Reserved

Bit Range	Default & Access	Field Name (ID): Description
15:12	3h RW	**GPIO Group to GPE_DW1 assignment encoding (GPE0_DW1):** This register assigns a specific GPIO Group to the ACPI GPE0[63:32]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[55:32]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[35:34]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[55:32]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[39:32]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[43:32]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[39:32]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[55:32]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[51:32]; other GPE bits not used. 8h = GPP_U[5:4] mapped to GPE[37:36]; other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[55:32]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[55:32]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[55:32]; other GPE bits not used. Dh - Fh: Reserved
11:8	2h RW	**GPIO Group to GPE_DW0 assignment encoding (GPE0_DW0):** This register assigns a specific GPIO Group to the ACPI GPE0[31:0]. The selected GPIO group will be mapped to lower bits of the GPE register 0h = GPP_B[23:0] mapped to GPE[23:0]; other GPE bits not used. 1h = GPP_T[3:2] mapped to GPE[3:2]; other GPE bits not used. 2h = GPP_A[23:0] mapped to GPE[23:0]; other GPE bits not used. 3h = GPP_R[7:0] mapped to GPE[7:0]; other GPE bits not used. 4h = GPD[11:0] mapped to GPE[11:0]; other GPE bits not used. 5h = GPP_S[7:0] mapped to GPE[7:0]; other GPE bits not used. 6h = GPP_H[23:0] mapped to GPE[23:0]; other GPE bits not used. 7h = GPP_D[19:0] mapped to GPE[19:0]; other GPE bits not used. 8h = GPP_U[5:4] mapped to GPE[5:4];other GPE bits not used. 9h = Reserved Ah = GPP_F[23:0] mapped to GPE[23:0]; other GPE bits not used. Bh = GPP_C[23:0] mapped to GPE[23:0]; other GPE bits not used. Ch = GPP_E[23:0] mapped to GPE[23:0]; other GPE bits not used. Dh - Fh: Reserved
7:2	0h RO	Reserved.
1	0h RW	**GPIO Dynamic Partition Clock Gating Enable (GPDPCGEN):** Specify whether the GPIO Community should take part in partition clock gating 0 = Disable participation in dynamic partition clock gating 1 = Enable participation in dynamic partition clock gating
0	0h RW	**GPIO Dynamic Local Clock Gating Enable (GPDLCGEN):** Specifies whether the GPIO Community should perform local clock gating. 0 = Disable dynamic local clock gating 1 = Enable dynamic local clock gating

27.5.4 Pad Ownership (PAD_OWN_GPP_R_0)—Offset 20h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	Reserved.
29:28	0h RW	**Pad Ownership (PAD_OWN_GPP_R_7):** Same description as bits[1:0].
27:26	0h RO	Reserved.
25:24	0h RW	**Pad Ownership (PAD_OWN_GPP_R_6):** Same description as bits[1:0].
23:22	0h RO	Reserved.
21:20	0h RW	**Pad Ownership (PAD_OWN_GPP_R_5):** Same description as bits[1:0].
19:18	0h RO	Reserved.
17:16	0h RW	**Pad Ownership (PAD_OWN_GPP_R_4):** Same description as bits[1:0].
15:14	0h RO	Reserved.
13:12	0h RW	**Pad Ownership (PAD_OWN_GPP_R_3):** Same description as bits[1:0].
11:10	0h RO	Reserved.
9:8	0h RW	**Pad Ownership (PAD_OWN_GPP_R_2):** Same description as bits[1:0].
7:6	0h RO	Reserved.
5:4	0h RW	**Pad Ownership (PAD_OWN_GPP_R_1):** Same description as bits[1:0].
3:2	0h RO	Reserved.
1:0	0h RW	**Pad Ownership (PAD_OWN_GPP_R_0):** 00 = Host GPIO ACPI Mode or GPIO Driver Mode. Host software (ACPI or GPIODriver) has ownership of the pad. In Host GPIO Driver Mode (refer toHOSTSW_OWN), GPIO input event update is limited to GPI_STS update only.Otherwise in Host ACPI Mode, updates are limited to GPI_GPE_STS, GPI_NMI_STSand/or GPI_SMI_STS. No read/write restriction to the Pad Configuration register set during host ownership 01 = ME GPIO Mode. ME has ownership of the pad. 10 = ISH GPIO Mode. ME has ownership of the pad 11 = Reserved

27.5.5 Pad Configuration Lock (PADCFGLOCK_GPP_R_0)—Offset 80h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_7):** Same description as bit 0.
6	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_6):** Same description as bit 0.
5	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_5):** Same description as bit 0.
4	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_4):** Same description as bit 0.
3	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_3):** Same description as bit 0.
2	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_2):** Same description as bit 0.
1	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_1):** Same description as bit 0.
0	0h RW	**Pad Config Lock (PADCFGLOCK_GPP_R_0):** Pad Configuration Lock locks specific register fields in the GPP specific registers from being configured. The registers affected become Read-Only and software writes to these registers have no effect. 0 = Unlock 1 = Lock the following register fields as read-only (RO): - Pad Configuration registers (exclude GPIOTXState) - GPI_NMI_EN Register (if implemented) - GPI_SMI_EN Register (if implemented) - GPI_GPE_EN Register (if implemented) When PadCfgLock is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

27.5.6 Pad Configuration Lock GPIO TxState Register (PADCFGLOCKTX_GPP_R_0)—Offset 84h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_7):** Same description as bit 0.
6	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_6):** Same description as bit 0.
5	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_5):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_4):** Same description as bit 0.
3	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_3):** Same description as bit 0.
2	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_2):** Same description as bit 0.
1	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_1):** Same description as bit 0.
0	0h RW	**Pad Config Lock TXState (PADCFGLOCKTX_GPP_R_0):** PadCfgLockTx locks the GPIOTxState bit from being configured. The GPIOTxState register becomes Read-Only and software writes to the register have no effect. 0 = Unlock 1 = Locks the Pad Configuration GPIOTXState field as read-only (RO) When PadCfgLockTx is written from a '1' to a '0' (unlock), a synchronous SMI# is generated if enabled. This ensures that only SMM code can change the above GPIO registers after the lockdown.

27.5.7 Host Software Pad Ownership (HOSTSW_OWN_GPP_R_0)—Offset B0h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_R_7):** Same description as bit 0.
6	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_R_6):** Same description as bit 0.
5	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_R_5):** Same description as bit 0.
4	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_R_4):** Same description as bit 0.
3	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_R_3):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_R_2):** Same description as bit 0.
1	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_R_1):** Same description as bit 0.
0	0h RW	**HostSW_Own (HOSTSW_OWN_GPP_R_0):** This register determines the appropriate host status bit update when a pad is under host ownership. 0 = ACPI Mode. GPIO input event updates are limited to GPI_GPE_STS,GPI_NMI_STS and/or GPI_SMI_STS. GPI_STS update is masked. 1 = GPIO Driver Mode. GPIO input event updates are limited toGPI_STS. GPI_GPE_STS, GPI_NMI_STS and/or GPI_SMI_STS updatesare masked.

27.5.8 GPI Interrupt Status (GPI_IS_GPP_R_0)—Offset 100h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_7):** Same description as bit 0.
6	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_6):** Same description as bit 0.
5	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_5):** Same description as bit 0.
4	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_4):** Same description as bit 0.
3	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_3):** Same description as bit 0.
2	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_2):** Same description as bit 0.
1	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_1):** Same description as bit 0.
0	0h RW/1C	**GPI Interrupt Status (GPI_INT_STS_GPP_R_0):** This bit is set to '1' by hardware when either an edge or a level event isdetected on pad and all the following conditions are true: - The corresponding pad is used in GPIO input mode - HOSTSW_OWN = 1 (i.e. Host GPIO Driver Mode). Writing a value of 1 will clear the bit while writing a value of 0 has noeffect. 0 = No interrupt 1 = Interrupt asserts The state of GPI_INT_EN[x] does not prevent the setting of GPI_INT_STS[x].

27.5.9 GPI Interrupt Enable (GPI_IE_GPP_R_0)—Offset 120h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_7):** Same description as bit 0.
6	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_6):** Same description as bit 0.
5	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_5):** Same description as bit 0.
4	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_4):** Same description as bit 0.
3	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_3):** Same description as bit 0.
2	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_2):** Same description as bit 0.
1	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_1):** Same description as bit 0.
0	0h RW	**GPI Interrupt Enable (GPI_INT_EN_GPP_R_0):** This bit is used to enable/ disable the generation of APIC interrupt when the corresponding GPI_INT_STS bit is set. 0 = disable interrupt generation 1 = enable interrupt generation

27.5.10 GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_0)—Offset 140h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_7):** Same description as bit 0.
6	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_6):** Same description as bit 0.
5	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_5):** Same description as bit 0.
4	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_4):** Same description as bit 0.
3	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_3):** Same description as bit 0.
2	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_2):** Same description as bit 0.
1	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_1):** Same description as bit 0.
0	0h RW/1C	**GPI General Purpose Events Status (GPI_GPE_STS_GPP_R_0):** These bits are set any time the corresponding GPIO pad is set up as an input, under host ownership and the corresponding GPIO signal is high (or low if the corresponding RXINV bit is set). If the correspondingenable bit is set in the GPI_GPE_EN register, then when the GPI_GPE_STS bit is set: - If the system is in an S3-S5 state, the event will also wake the system. - If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be generated, depending on the GPIRoutSCI bit for thecorresponding pad. These bits are sticky bits and are cleared by writing a 1 back to this bit position. The state of GPI_GPE_EN does not prevent the setting of GPI_GPE_STS.

27.5.11 GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_0)—Offset 160h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	Reserved.
7	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_7):** Same description as bit 0.
6	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_6):** Same description as bit 0.
5	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_5):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_4):** Same description as bit 0.
3	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_3):** Same description as bit 0.
2	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_2):** Same description as bit 0.
1	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_1):** Same description as bit 0.
0	0h RW	**GPI General Purpose Events Enable (GPI_GPE_EN_GPP_R_0):** This bit is used to enable/disable the generation of GPE to cause SCI and/or wake when the corresponding GPI_GPE_STS bit is set. 0 = disable GPE generation 1 = enable GPE generation Note:The pad must also be routed for GPE functionality in order for GPE tobe generated, i.e. the corresponding GPIRoutSCI must be set to '1'.

27.5.12 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_0)—Offset 700h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 4400XX00h

Bit Range	Default & Access	Field Name (ID): Description
31:30	1h RW	**Pad Reset Config (PADRSTCFG):** This register controls which reset is used to reset GPIO pad register fields in various GPIO registers (PADCFGLOCK, PADCFGLOCKTX, GPI_IS, GPI_IE, GPI_GPE_STS, GPI_GPE_EN, PAD_CFG_DW0, and PAD_CFG_DW1). 00 = Global Reset or RSMRST# 01 = Host deep reset. This reset occurs when any of the following occur: Host reset (with or without power cycle) is initiated, Global reset is initiated, or Deep Sx entry. This reset does NOT occur as part of S3/S4/S5 entry. 10 = PLTRST# 11 = Global Reset
29	0h RW	**RX Pad State Select (RXPADSTSEL):** Determine from which node the RX pad state for native function should be source from. This field only affects the pad state value being fanned out to native function(s) and is not meaningful if the pad is in GPIO mode (i.e. Pad Mode = 0). 0 = Raw RX pad state directly from CFIO RX buffer 1 = Syncronized Internal RX pad state (subject to RXINV , hardware debouncer (if any) and PreGfRXSel settings)
28	0h RW	**RX Raw Override to '1' (RXRAW1):** This bit determines if the selected pad state is being overridden to '1'. This field only makes sense when the buffer is configured as an input in either GPIO Mode or native function mode. The override takes place at the internal pad state directly from buffer and before the RXINV. 0 = No Override 1 = RX drive 1 internally
27	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
26:25	2h RW	**RX Level/Edge Configuration (RXEVCFG):** Determine if the internal RX pad state (RXPadStSel=1) should be passed on to the next logic stage as is, as a pulse, or level signal. This field does not affect the received pad state (to GPIORXState or native functions) but how the interrupt or wake triggering events should be delivered to the GPIO Community Controller. 0h = Level 1h = Edge 2h = Disable 3h = Either rising edge or failing edge
24	0h RW	**Pre Glitch Filter Stage RX Pad State Select (PREGFRXSEL):** Determine if the synchronized version of the raw RX pad state should be subjected to glitch filter or not. This field only makes sense when the RX buffer is configured as an input and is not disabled. 0 = Select synchronized, non filtered RX pad state 1 = Select synchronized, filtered RX pad state The selected RX pad state can be further subjected to polarity inversion through RXINV
23	0h RW	**RX Invert (RXINV):** This bit determines if the selected pad state should go through the polarity inversion stage. This field only makes sense when the RX buffer is configured as an input in either GPIO Mode or native function mode. The polarity inversion takes place at the mux node of raw vs filtered or non-filtered RX pad state, as determined by PreGfRXsel and RXPadStSel This bit does not affect GPIORXState. During host ownership GPIO Mode, when this bit is set to '1', then the RX pad state is inverted as it is sent to the GPIO-to-IOxAPIC, GPE/SCI, SMI, NMI logic or GPI_IS[n] that is using it. This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. 0 = No inversion 1 = Inversion
22:21	0h RW	**RX/TX Enable Config (RXTXENCFG):** This controls the RX and TX buffer enables for the function selected by Pad Mode, but is not applicable when Pad Mode is 0 (i.e. GPIO mode). Hardware shall ensure GPIOTxDis and GPIORxDis are controlling the RX and TX buffers when this field is 0 and Pad Mode is 0. 0 = Function defined in Pad Mode controls TX and RX Enables 1 = Function controls TX Enable and RX Disabled with RX drive 0 internally 2 = Function controls TX Enable and RX Disabled with RX drive 1 internally 3 = Function controls TX Enabled and RX is always enabled
20	0h RW	**GPIO Input Route IOxAPIC (GPIROUTIOXAPIC):** Determine if the pad can be routed to cause peripheral IRQ when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause peripheral IRQ 1 = Routing can cause peripheral IRQ Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the peripheral IRQ indication to the intended recipient(s).
19	0h RW	**GPIO Input Route SCI (GPIROUTSCI):** Determine if the pad can be routed to cause SCI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SCI 1 = Routing can cause SCI Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the GPE indication to the intended recipient(s), e.g. PMU.
18	0h RO	**GPIO Input Route SMI (GPIROUTSMI):** Determine if the pad can be routed to cause SMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause SMI. 1 = Routing can cause SMI. Note: This bit does not affect any interrupt status bit within GPIO, but is used as the last qualifier for the SMI indication to the intended recipient(s).

Bit Range	Default & Access	Field Name (ID): Description
17	0h RO	**GPIO Input Route NMI (GPIROUTNMI):** Determine if the pad can be routed to cause NMI when configured in GPIO input mode. If the pad is not configured in GPIO input mode, this field has no effect. 0 = Routing does not cause NMI. 1 = Routing can cause NMI. Note: This bit also affects GPI_NMI_STS. If '0', GPI_NMI_STS is always clear. If '1', GPI_NMI_STS could be set (depending on GPIOOwn setting) when there is an event. Whether a NMI indication is generated and sent to the intended recipient(s) is also depending on the corresponding GPI_NMI_EN bit.
16:13	0h RO	Reserved.
12:10	-- RW	**Pad Mode (PMODE):** This field determines whether the Pad is controlled by GPIO controller logic or one of the native functions muxed onto the Pad. 0h = GPIO controls the Pad 1h = Function 1, if applicable, controls the Pad ... 7h = Function 7, if applicable, controls the Pad Default value is determined by the default functionality of the pad.
9	1h RW	**GPIO RX Disable (GPIORXDIS):** RX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the input buffer (active low enable) of the pad 1 = Disable the input buffer of the pad. Notes: When the input buffer is disabled, the internal pad state is always driven to '0'.
8	1h RW	**GPIO TX Disable (GPIOTXDIS):** TX buffer enable control when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Enable the output buffer (active low enable) of the pad 1 = Disable the output buffer of the pad; i.e. Hi-Z
7:2	0h RO	Reserved.
1	0h RO/V	**GPIO RX State (GPIORXSTATE):** This is the current internal RX pad state after Glitch Filter logic stage and is not affected by PMode and RXINV, hardware debouncer (if any) settings. When read, this bit returns a 0 if GPIORxDis is 1.
0	0h RW	**GPIO TX State (GPIOTXSTATE):** TX state in when PMode = 0 ONLY. No effect when the pad in native mode. 0 = Drive a level '0' to the TX output pad 1 = Drive a level '1' to the TX output pad

27.5.13 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_0)—Offset 704h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 58h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** The Pad Termination state defines the different weak pull-up and pull-down settings that are supported by the buffer. The settings for [13:10] correspond to: 0000: none 0100: 20k PD 1100: 20k PU 1111: Native controller selected by Pad Mode controls the Termination. This field should be set to 1111b for the selected native function that supports dynamic termination override. Refer to Vol1, GPIO chapter, for more info. Others: Reserved. NOTES: 1. The 20K pull-up/pull-down can only be enabled as long as the toggle rate on the signal is no more than 300KHz. 2. If a reserved value is programmed, pad may malfunction. 3. The setting of this field is applicable in all Pad Mode including GPIO. As each Pad Mode may require different termination and isolation, care must be taken in SW in the transition with appropriate register programming. The actual transition sequence requirement may vary on case by case basis depending on the native functions involved. For example, before changing the pad from output to input direction, PU/PD settings should be programmed first to ensure the input does not float momentarily.
9:8	0h RW	Reserved.
7:0	58h RO	**Interrupt Select (INTSEL):** The Interrupt Select defines which interrupt line driven from the GPIO Community Controller toggles when an interrupt is detected on this pad. 0 = Interrupt Line 0 1 = Interrupt Line 1 ... 255 = Interrupt Line 255

27.5.14 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_1)—Offset 710h

This register applies to GPP_R1 and has the same description as PAD_CFG_DW0_GPP_R_0.

27.5.15 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_1)—Offset 714h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 3C59h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
13:10	Fh RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPP_R_0.
9:8	0h RW	Reserved.
7:0	59h RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPP_R_0.

27.5.16 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_2)—Offset 720h

This register applies to GPP_R2 and has the same description as PAD_CFG_DW0_GPP_R_0.

27.5.17 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_2)—Offset 724h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 3C5Ah

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	Fh RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPP_R_0.
9:8	0h RW	Reserved.
7:0	5Ah RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPP_R_0.

27.5.18 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_3)—Offset 730h

This register applies to GPP_R3 and has the same description as PAD_CFG_DW0_GPP_R_0.

27.5.19 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_3)—Offset 734h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 3C5Bh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	Fh RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPP_R_0.
9:8	0h RW	Reserved.
7:0	5Bh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPP_R_0.

27.5.20 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_4)—Offset 740h

This register applies to GPP_R4 and has the same description as PAD_CFG_DW0_GPP_R_0.

27.5.21 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_4)—Offset 744h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 5Ch

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPP_R_0.
9:8	0h RW	Reserved.
7:0	5Ch RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPP_R_0.

27.5.22 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_5)—Offset 750h

This register applies to GPP_R5 and has the same description as PAD_CFG_DW0_GPP_R_0.

27.5.23 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_5)—Offset 754h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 5Dh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPP_R_0.
9:8	0h RW	Reserved.
7:0	5Dh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPP_R_0.

27.5.24 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_6)—Offset 760h

This register applies to GPP_R6 and has the same description as PAD_CFG_DW0_GPP_R_0.

27.5.25 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_6)—Offset 764h

Refer to Register Field for detail

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 5Eh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPP_R_0.
9:8	0h RW	Reserved.
7:0	5Eh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPP_R_0.

27.5.26 Pad Configuration DW0 (PAD_CFG_DW0_GPP_R_7)—Offset 770h

This register applies to GPP_R7 and has the same description as PAD_CFG_DW0_GPP_R_0.

27.5.27 Pad Configuration DW1 (PAD_CFG_DW1_GPP_R_7)—Offset 774h

Refer to Register Field for detail

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 5Fh

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13:10	0h RW	**Termination (TERM):** Same description as TERM bits in PAD_CFG_DW1_GPP_R_0.
9:8	0h RW	Reserved.
7:0	5Fh RO	**Interrupt Select (INTSEL):** Same description as INTSEL bits in PAD_CFG_DW1_GPP_R_0.

28 High Precision Event Timer (HPET)

28.1 HPET Memory Mapped Registers Summary

The timer registers are memory mapped directly (rather than indexed) to allow the CPU to access each register without having to use an index register. This ensures accesses are safe for multi-threaded environments. The timer register space is 1024 bytes. The registers are generally aligned on 64-bit boundaries to simplify implementation with IA64 processors. In the PCH, there are 4 possible memory address ranges beginning at 1) FED0_0000h, 2) FED0_1000h, 3) FED0_2000h, 4) FED0_3000h. The choice of address range should be selected by assigning the High Performance Event Timer Configuration (HPTC) register fields in the configuration space of the Primary to Sideband Bridge. All registers are implemented in the Primary power well, and all bits are reset by PLTRST#. Reads to reserved registers or bits will return a value of 0.
Behavorial Rules:
1. Software can read or write the various bytes in these registers using 32-bit or 64-bit accesses. Software must not attempt to read or write across register boundaries. For example, a 32-bit access should be to offset x0h, x4h, x8h, or xCh. 32-bit accesses should not be to 01h, 02h, 03h, 05h, 06h, 07h, 09h, 0Ah, 0Bh, 0Dh, 0Eh, or 0Fh. Any accesses to these offsets will result in an unexpected behavior, and may result in a master abort. However, these accesses should not result in system hangs. 64-bit accesses can only be to x0h and must not cross 64-bit boundaries.
2. Software should not write to read-only registers.
3. Software should not expect any particular or consistent value when reading reserved registers or bits.

Table 28-1. Summary of HPET Memory Mapped Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
FED000 00h	FED000 07h	General Capabilities and ID Register (GEN_CAP_ID)—Offset FED00000h	27BC86B8086A701h
FED000 10h	FED000 17h	General Config Register (GEN_CFG)—Offset FED00010h	0h
FED000 20h	FED000 27h	General Interrupt Status Register (GEN_INT_STS)—Offset FED00020h	0h
FED000F 0h	FED000F 7h	Main Counter Value (MAIN_CNTR)—Offset FED000F0h	0h
FED001 00h	FED001 07h	Timer n Config and Capabilities (TMRn_CNF_CAP)—Offset FED00100h	0h
FED001 08h	FED001 0Fh	Timer n Comparator Value (TMRn_CMP_VAL)—Offset FED00108h	FFFFFFFFFFFFFFFFh

28.1.1 General Capabilities and ID Register (GEN_CAP_ID)—Offset FED00000h

Access Method

Type: MEM Register
(Size: 64 bits)

Device:
Function:

Default: 27BC86B8086A701h

Bit Range	Default and Access	Field Name (ID): Description
63:32	27BC86Bh RO	**Main Counter Tick Period (COUNTER_CLK_PER_CAP):** This read-only field indicates the period at which the counter increments in femtoseconds (10^-15 seconds). The PCH HPET timers use a 24 MHz clock, which has a period of 41,666,667 femtoseconds. Therefore this register will always return 027BC86Bh when read.
31:16	8086h RO	**Vendor ID (VENDOR_ID_CAP):** These bits will return 8086h when read to reflect Intel as the vendor.
15	1h RO	**Legacy Rout Capable (LEG_RT_CAP):** This bit will always be 1 when read, indicating support for the Legacy Interrupt Rout.
14	0h RO	Reserved.
13	1h RO	**Counter Size (COUNT_SIZE_CAP):** This bit will return 1 when read to indicate support for 64-bit counters allowing 64 or 32-bit mode operation.
12:8	7h RO	**Number of Timers (NUM_TIM_CAP):** This value in this field will be 07h to indicate support for 8 timers in the timer block.
7:0	1h RO	**Revision ID (REV_ID):** This field indicates which revision of the function is implemented. Default value will be 01h.

28.1.2 General Config Register (GEN_CFG)—Offset FED00010h

Access Method

Type: MEM Register
(Size: 64 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
63:2	0h RO	Reserved.
1	0h RW	**Legacy Rout (LEG_RT_CNF):** If the ENABLE_CNF bit and the LEG_RT_CNF bit are both set, the interrupts will be routed as follows: • Timer 0 is routed to IRQ0 in 8259 or IRQ2 in the I/O APIC • Timer 1 is routed to IRQ8 in 8259 or IRQ8 in the I/O APIC • Timer 2-n is routed as per the routing in the timer n Configuration registers. • If the Legacy Replacement Rout bit is set, the individual routing bits for Timers 0 and 1 (APIC) will have no impact. • If the Legacy Replacement Rout bit is not set, the individual routing bits for each of the timers are used. • This bit will default to 0. BIOS can set it to 1 to enable the legacy replacement routing, or 0 to disable the legacy replacement routing.
0	0h RW	**Overall Enable (ENABLE_CNF):** This bit must be set to enable any of the timers to generate interrupts. If this bit is 0, then the main counter will halt (will not increment) and no interrupts will be caused by any of these timers. For level-triggered interrupts, if an interrupt is pending when the ENABLE_CNF bit is changed from 1 to 0, the interrupt status indications (in the various Txx_INT_STS bits) will not be cleared. Software must write to the Txx_INT_STS bits to clear the interrupts. NOTE: This bit will default to 0. BIOS can set it to 1 or 0.

28.1.3 General Interrupt Status Register (GEN_INT_STS)—Offset FED00020h

Access Method

Type: MEM Register (Size: 64 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
63:8	0h RO	Reserved.
7	0h RW/1C	**Timer 7 Interrupt Active (T07_INT_STS):** Same functionality as Timer 0.
6	0h RW/1C	**Timer 6 Interrupt Active (T06_INT_STS):** Same functionality as Timer 0.
5	0h RW/1C	**Timer 5 Interrupt Active (T05_INT_STS):** Same functionality as Timer 0.
4	0h RW/1C	**Timer 4 Interrupt Active (T04_INT_STS):** Same functionality as Timer 0.
3	0h RW/1C	**Timer 3 Interrupt Active (T03_INT_STS):** Same functionality as Timer 0.

Bit Range	Default and Access	Field Name (ID): Description
2	0h RW/1C	**Timer 2 Interrupt Active (T02_INT_STS):** Same functionality as Timer 0.
1	0h RW/1C	**Timer 1 Interrupt Active (T01_INT_STS):** Same functionality as Timer 0.
0	0h RW/1C	**Timer 0 Interrupt Active (T00_INT_STS):** The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer. (default = 0) If set to level-triggered mode: This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. Writes of 0 to this bit will have no effect. If set to edge-triggered mode: This bit should be ignored by software. Software should always write 0 to this bit. NOTE: Defaults to 0. In edge triggered mode, this bit will always read as 0 and writes will have no effect.

28.1.4 Main Counter Value (MAIN_CNTR)—Offset FED000F0h

Software can read the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 0F0h or 0F4h. 64-bit accesses may only be done to 0F0h. Writes to this register should only be done while the counter is halted. Reads to this register return the current value of the main counter. If 32-bit software attempts to read a 64-bit counter, it should first halt the counter. Since this will delay the interrupts for all of the timers, this should be done only if the consequences are understood. It is strongly recommended that 32-bit software only operate the timer in 32-bit mode. Reads to this register are monotonic. No two consecutive reads will return the same value. The second of two reads will always return a larger value (unless the timer has rolled over to 0)

Access Method

Type: MEM Register (Size: 64 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
63:0	0h RW/V	**Counter Value (COUNTER_VAL):** Reads return the current value of the counter. Writes load the new value to the counter. NOTES: 1. Writes to this register should only be done while the counter is halted. 2. Reads to this register return the current value of the main counter. 3. 32-bit counters will always return 0 for the upper 32-bits of this register. 4. If 32-bit software attempts to read a 64-bit counter, it should first halt the counter. Since this will delay the interrupts for all of the timers, this should be done only if the consequences are understood. It is strongly recommended that 32-bit software only operate the timer in 32-bit mode. 5. Reads to this register are monotonic. No two consecutive reads will return the same value. The second of two reads will always return a larger value (unless the timer has rolled over to 0)

28.1.5 Timer n Config and Capabilities (TMRn_CNF_CAP)—Offset FED00100h

Timer 0: 100–107h,
Timer 1: 120–127h,
Timer 2: 140–147h,
Timer 3: 160–167h,
Timer 4: 180–187h,
Timer 5: 1A0–1A7h,
Timer 6: 1C0–1C7h,
Timer 7: 1E0–1E7h,
The letter n can be 0, 1, 2, 3, 4, 5, 6, or 7 referring to Timer 0, 1, 2, 3, 4, 5, 6, or 7.

Access Method

Type: MEM Register (Size: 64 bits)
Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
63:4	0h RO	Reserved.
3	0h RW	**Timer 0 Type (TIMER0_TYPE_CNF):** Setting this bit to 1 enables the timer to generate a periodic interrupt if it is capable of doing so. If the TIMERn_PER_INT_CAP bit is 0, then this bit will always return 0 when read and writes will have no impact. For timer 0, this bit will be read/write, with default of 0. For timers 1-7, this bit will be read-only, with a fixed value of 0.
2:0	0h RO	Reserved.

28.1.6 Timer n Comparator Value (TMRn_CMP_VAL)—Offset FED00108h

Timer 0: 108h – 10Fh
Timer 1: 128h – 12Fh
Timer 2: 148h – 14Fh
Timer 3: 168h – 16Fh
Timer 4: 188h – 18Fh
Timer 5: 1A8h – 1AFh
Timer 6: 1C8h – 1CFh
Timer 7: 1E8h – 1EFh

Access Method

Type: MEM Register (Size: 64 bits)
Device:
Function:

Default: FFFFFFFFFFFFFFFFh

Bit Range	Default and Access	Field Name (ID): Description
63:0	FFFFFFFFFFFFFFFFh RW/V	**Timer 0 Comparator Value (TMR0_CMP_VAL):** If the timer is configured to non-periodic mode, when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). The value in this register does not change based on the interrupt being generated. If the timer is configured to periodic mode (supported only for Timer 0), when the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). When this time out occurs, the value in this register is increased by the value last written to the register. For example, in periodic mode if the value written to the register is 0000123h: 1. An interrupt will be generated when the main counter reaches 00000123h. 2. The value in this register will then be adjusted by the hardware to 00000246h. 3. Another interrupt will be generated when the main counter reaches 00000246h. 4. The value in this register will then be adjusted by the hardware to 00000369h. As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h The default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer will have a default value of 00000000FFFFFFFFh. A 64-bit timer will have a default value of FFFFFFFFFFFFFFFFh. Software can read or write the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses may only be done to offset 1x8h or 1xCh. 64-bit accesses may only be done to 1x8h. Comparator value. Timer 0 is 64-bits wide. Timers 1-7 are 32-bits wide.

29 Integrated Clock (ICC)

29.1 Integrated Clock (ICC) Configuration Registers Summary

Table 29-1. Summary of Integrated Clock (ICC) Configuration Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
22E4h	22E7h	SRCCLKREQ Config (src_muxsel1)—Offset 22E4h	6543210h

29.1.1 SRCCLKREQ Config (src_muxsel1)—Offset 22E4h

Access Method

Type:MSG Register
(Size: 32 bits)

Device:
Function:

Default:6543210h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO	Reserved.
27:24	6h RW	**SRCCLKREQ Select For CLKOUT_PCIE6 (muxsel_src6_cg_en_3_0):** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE6 0000: SRCCLKREQ0# controls CLKOUT_PCIE6 (default) 0001: SRCCLKREQ1# controls CLKOUT_PCIE6 0010: SRCCLKREQ2# controls CLKOUT_PCIE6 0011: SRCCLKREQ3# controls CLKOUT_PCIE6 0100: SRCCLKREQ4# controls CLKOUT_PCIE6 0101: SRCCLKREQ5# controls CLKOUT_PCIE6 0110: SRCCLKREQ6# controls CLKOUT_PCIE6 0111-1111: Reserved
23:20	5h RW	**SRCCLKREQ Select For CLKOUT_PCIE5 (muxsel_src5_cg_en_3_0):** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE5 0000: SRCCLKREQ0# controls CLKOUT_PCIE5 (default) 0001: SRCCLKREQ1# controls CLKOUT_PCIE5 0010: SRCCLKREQ2# controls CLKOUT_PCIE5 0011: SRCCLKREQ3# controls CLKOUT_PCIE5 0100: SRCCLKREQ4# controls CLKOUT_PCIE5 0101: SRCCLKREQ5# controls CLKOUT_PCIE5 0110: SRCCLKREQ6# controls CLKOUT_PCIE5 0111-1111: Reserved

Bit Range	Default & Access	Field Name (ID): Description
19:16	4h RW	**SRCCLKREQ Select For CLKOUT_PCIE4 (muxsel_src4_cg_en_3_0):** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE4 0000: SRCCLKREQ0# controls CLKOUT_PCIE4 (default) 0001: SRCCLKREQ1# controls CLKOUT_PCIE4 0010: SRCCLKREQ2# controls CLKOUT_PCIE4 0011: SRCCLKREQ3# controls CLKOUT_PCIE4 0100: SRCCLKREQ4# controls CLKOUT_PCIE4 0101: SRCCLKREQ5# controls CLKOUT_PCIE4 0110: SRCCLKREQ6# controls CLKOUT_PCIE4 0111-1111: Reserved
15:12	3h RW	**SRCCLKREQ Select For CLKOUT_PCIE3 (muxsel_src3_cg_en_3_0):** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE3 0000: SRCCLKREQ0# controls CLKOUT_PCIE3 (default) 0001: SRCCLKREQ1# controls CLKOUT_PCIE3 0010: SRCCLKREQ2# controls CLKOUT_PCIE3 0011: SRCCLKREQ3# controls CLKOUT_PCIE3 0100: SRCCLKREQ4# controls CLKOUT_PCIE3 0101: SRCCLKREQ5# controls CLKOUT_PCIE3 0110: SRCCLKREQ6# controls CLKOUT_PCIE3 0111-1111: Reserved
11:8	2h RW	**SRCCLKREQ Select For CLKOUT_PCIE2 (muxsel_src2_cg_en_3_0):** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE2 0000: SRCCLKREQ0# controls CLKOUT_PCIE2 (default) 0001: SRCCLKREQ1# controls CLKOUT_PCIE2 0010: SRCCLKREQ2# controls CLKOUT_PCIE2 0011: SRCCLKREQ3# controls CLKOUT_PCIE2 0100: SRCCLKREQ4# controls CLKOUT_PCIE2 0101: SRCCLKREQ5# controls CLKOUT_PCIE2 0110: SRCCLKREQ6# controls CLKOUT_PCIE2 0111-1111: Reserved
7:4	1h RW	**SRCCLKREQ Select For CLKOUT_PCIE1 (muxsel_src1_cg_en_3_0):** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE1 0000: SRCCLKREQ0# controls CLKOUT_PCIE1 (default) 0001: SRCCLKREQ1# controls CLKOUT_PCIE1 0010: SRCCLKREQ2# controls CLKOUT_PCIE1 0011: SRCCLKREQ3# controls CLKOUT_PCIE1 0100: SRCCLKREQ4# controls CLKOUT_PCIE1 0101: SRCCLKREQ5# controls CLKOUT_PCIE1 0110: SRCCLKREQ6# controls CLKOUT_PCIE1 0111-1111: Reserved
3:0	0h RW	**SRCCLKREQ Select For CLKOUT_PCIE0 (muxsel_src0_cg_en_3_0):** Select version of SRCCLKREQ# for dynamic control of the output CLKOUT_PCIE0 0000: SRCCLKREQ0# controls CLKOUT_PCIE0 (default) 0001: SRCCLKREQ1# controls CLKOUT_PCIE0 0010: SRCCLKREQ2# controls CLKOUT_PCIE0 0011: SRCCLKREQ3# controls CLKOUT_PCIE0 0100: SRCCLKREQ4# controls CLKOUT_PCIE0 0101: SRCCLKREQ5# controls CLKOUT_PCIE0 0110: SRCCLKREQ6# controls CLKOUT_PCIE0 0111-1111: Reserved

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30 Interrupt

30.1 Interrupt Registers Summary

Table 30-1. Summary of Interrupt Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
20h	20h	Master Initialization Command Word 1 (MICW1)—Offset 20h	11h
20h	20h	Master Operational Control Word 2 (MOCW2)—Offset 20h	0h
20h	20h	Master Operational Control Word 3 (MOCW3)—Offset 20h	8h
21h	21h	Master Initialization Command Word 2 (MICW2)—Offset 21h	0h
21h	21h	Master Initialization Command Word 3 (MICW3)—Offset 21h	7h
21h	21h	Master Initialization Command Word 4 (MICW4)—Offset 21h	0h
21h	21h	Master Operational Control Word 1 (MOCW1)—Offset 21h	0h
A0h	A0h	Slave Initialization Command Word 1 (SICW1)—Offset A0h	11h
A0h	A0h	Slave Operational Control Word 2 (SOCW2)—Offset A0h	0h
A0h	A0h	Slave Operational Control Word 3 (SOCW3)—Offset A0h	8h
A1h	A1h	Slave Initialization Command Word 2 (SICW2)—Offset A1h	0h
A1h	A1h	Slave Initialization Command Word 3 (SICW3)—Offset A1h	7h
A1h	A1h	Slave Initialization Command Word 4 (SICW4)—Offset A1h	0h
A1h	A1h	Slave Operational Control Word 1 (SOCW1)—Offset A1h	0h
4D0h	4D0h	Master Edge/Level Control (ELCR1)—Offset 4D0h	0h
4D1h	4D1h	Slave Edge/Level Control (ELCR2)—Offset 4D1h	0h

30.1.1 Master Initialization Command Word 1 (MICW1)—Offset 20h

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:
1. The Interrupt Mask register is cleared.
2. IRQ7 input is assigned priority 7.
3. The slave mode address is set to 7.
4. Special Mask Mode is cleared and Status Read is set to IRR.
Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Access Method

Type: IO Register (Size: 8 bits)

Device:
Function:

Default: 11h

Bit Range	Default and Access	Field Name (ID): Description
7:5	0h WO	**ICW/OCW select (ICW_OCW_SLT1):** These bits are MCS-85 specific, and not needed. Should be programmed to 000
4	1h WO	**ICW/OCW select (ICW_OCW_SLT2):** This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	0h WO	**Edge/Level Bank Select (LTIM):** Disabled. Replaced by the edge/level triggered control registers (ELCR).
2	0h WO	**ADI-IGNORED (ADI):** Ignored for PCH. Should be programmed to 0.
1	0h WO	**Single or Cascade (SNGL):** Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	1h WO	**ICW4 Write Required (IC4):** This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

30.1.2 Master Operational Control Word 2 (MOCW2)—Offset 20h

*address should be 20h
Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:5	0h WO	**Rotate and EOI Codes (REOI):** R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 Rotate in Auto EOI Mode (Clear) 001 Non-specific EOI command 010 No Operation 011 *Specific EOI Command 100 Rotate in Auto EOI Mode (Set) 101 Rotate on Non-Specific EOI Command 110 *Set Priority Command 111 *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	0h WO	**OCW2 Select (O2S):** When selecting OCW2, bits 4:3 = 00
2:0	0h WO	**Interrupt Level Select (L2, L1, L0) (ILSLT):** L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function, programming L2, L1 and L0 to 0 is sufficient in this case.

30.1.3 Master Operational Control Word 3 (MOCW3)—Offset 20h

*address should be 20h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO	Reserved.
6	0h WO	**Special Mask Mode (SMM):** If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.
5	0h WO	**Enable Special Mask Mode (ESMM):** When set, the SMM bit is enabled to set or reset the Special Mask Mode. When cleared, the SMM bit becomes a "do not care".
4:3	1h WO	**OCW3 Select (O3S):** When selecting OCW3, bits 4:3 = 01
2	0h WO	**Poll Mode Command (PMC):** When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	0h WO	**Register Read Command (RRC):** These bits provide control for reading the ISR and Interrupt IRR. When bit 1=0, bit 0 will not affect the register read selection. Following ICW initialization, the default OCW3 port address read will be "read IRR". To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. Value Command 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

30.1.4 Master Initialization Command Word 2 (MICW2)—Offset 21h

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h WO	**Interrupt Vector Base Address (IVBA):** Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.
2:0	0h WO	**Interrupt Request Level (IRL):** When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

30.1.5 Master Initialization Command Word 3 (MICW3)—Offset 21h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 7h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h WO	**MICW3 [7:3] (MICW3_7_3):** These bits must be programmed to zero.
2	1h WO	**Cascaded Controller Connection (CCC):** This bit must always be programmed to a 1 to indicate the slave controller for interrupts 8 - 15 is cascaded on IRQ2.
1:0	3h WO	**MICW [1:0] (MICW3_1_0):** These bits must be programmed to zero.

30.1.6 Master Initialization Command Word 4 (MICW4)—Offset 21h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:5	0h RO	Reserved.
4	0h WO	**Special Fully Nested Mode (SFNM):** Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0h WO	**Buffered Mode (BUF):** Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0h WO	**Master/Slave in Buffered Mode (MSBM):** Not used. Should always be programmed to 0.
1	0h WO	**Automatic End of Interrupt (AEOI):** This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.
0	0h WO	**Microprocessor Mode (MM):** This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.1

30.1.7 Master Operational Control Word 1 (MOCW1)—Offset 21h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Request Mask (IRM):** When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

30.1.8 Slave Initialization Command Word 1 (SICW1)—Offset A0h

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:
1. The Interrupt Mask register is cleared.
2. IRQ7 input is assigned priority 7.
3. The slave mode address is set to 7.
4. Special Mask Mode is cleared and Status Read is set to IRR.
Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 11h

Bit Range	Default and Access	Field Name (ID): Description
7:5	0h WO	**ICW/OCW select (ICW_OCW_SLT1):** These bits are MCS-85 specific, and not needed. Should be programmed to 000
4	1h WO	**ICW/OCW select (ICW_OCW_SLT2):** This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	0h WO	**Edge/Level Bank Select (LTIM):** Disabled. Replaced by the edge/level triggered control registers (ELCR).
2	0h WO	**ADI-IGNORED (ADI):** Ignored for PCH. Should be programmed to 0.
1	0h WO	**Single or Cascade (SNGL):** Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	1h WO	**ICW4 Write Required (IC4):** This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

30.1.9 Slave Operational Control Word 2 (SOCW2)—Offset A0h

*address should be A0h
Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:5	0h WO	**Rotate and EOI Codes (REOI):** R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 Rotate in Auto EOI Mode (Clear) 001 Non-specific EOI command 010 No Operation 011 *Specific EOI Command 100 Rotate in Auto EOI Mode (Set) 101 Rotate on Non-Specific EOI Command 110 *Set Priority Command 111 *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	0h WO	**OCW2 Select (O2S):** When selecting OCW2, bits 4:3 = 00
2:0	0h WO	**Interrupt Level Select (L2, L1, L0) (ILSLT):** L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function, programming L2, L1 and L0 to 0 is sufficient in this case.

30.1.10 Slave Operational Control Word 3 (SOCW3)—Offset A0h

*address should be A0h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO	Reserved.
6	0h WO	**Special Mask Mode (SMM):** If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.
5	0h WO	**Enable Special Mask Mode (ESMM):** When set, the SMM bit is enabled to set or reset the Special Mask Mode. When cleared, the SMM bit becomes a "do not care".
4:3	1h WO	**OCW3 Select (O3S):** When selecting OCW3, bits 4:3 = 01
2	0h WO	**Poll Mode Command (PMC):** When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	0h WO	**Register Read Command (RRC):** These bits provide control for reading the ISR and Interrupt IRR. When bit 1=0, bit 0 will not affect the register read selection. Following ICW initialization, the default OCW3 port address read will be "read IRR". To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. Value Command 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

30.1.11 Slave Initialization Command Word 2 (SICW2)—Offset A1h

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h WO	**Interrupt Vector Base Address (IVBA):** Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.
2:0	0h WO	**Interrupt Request Level (IRL):** When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

30.1.12 Slave Initialization Command Word 3 (SICW3)—Offset A1h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 7h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h RO	Reserved.
2:0	7h WO	**Slave Identification Code (SIC):** This field must be programmed to 02h to match the code broadcast by the master controller during the INTA# sequence.

30.1.13 Slave Initialization Command Word 4 (SICW4)—Offset A1h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:5	0h RO	Reserved.
4	0h WO	**Special Fully Nested Mode (SFNM):** Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0h WO	**Buffered Mode (BUF):** Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0h WO	**Master/Slave in Buffered Mode (MSBM):** Not used. Should always be programmed to 0.
1	0h WO	**Automatic End of Interrupt (AEOI):** This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.
0	0h WO	**Microprocessor Mode (MM):** This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.1

30.1.14 Slave Operational Control Word 1 (SOCW1)—Offset A1h

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Interrupt Request Mask (IRM):** When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

30.1.15 Master Edge/Level Control (ELCR1)—Offset 4D0h

Master Edge/Level Control Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:3	0h RW	**Edge Level Control (ELC_7_3):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level.
2:0	0h RO	Reserved.

30.1.16 Slave Edge/Level Control (ELCR2)—Offset 4D1h

Slave Edge/Level Control Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:6	0h RW	**Edge Level Control (ELC_15_14):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 7 applies to IRQ15, and bit 6 to IRQ14.
5	0h RW	**Edge Level Control (ELC_13):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. This bit applies to IRQ13.
4:1	0h RW	**Edge Level Control (ELC_12_9):** In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 4 applies to IRQ12, bit 3 to IRQ11, bit 2 to IRQ10, and bit 1 to IRQ9.
0	0h RO	Reserved.

30.2 Interrupt PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 30-2. Summary of Interrupt PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3100h	3100h	PIRQA Routing Control (PARC)—Offset 3100h	80h
3101h	3101h	PIRQB Routing Control (PBRC)—Offset 3101h	80h
3102h	3102h	PIRQC Routing Control (PCRC)—Offset 3102h	80h
3103h	3103h	PIRQD Routing Control (PDRC)—Offset 3103h	80h
3104h	3104h	PIRQE Routing Control (PERC)—Offset 3104h	80h
3105h	3105h	PIRQF Routing Control (PFRC)—Offset 3105h	80h

Table 30-2. Summary of Interrupt PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3106h	3106h	PIRQG Routing Control (PGRC)—Offset 3106h	80h
3107h	3107h	PIRQH Routing Control (PHRC)—Offset 3107h	80h
3140h	3141h	PCI Interrupt Route 0 (PIR0)—Offset 3140h	3210h
3142h	3143h	PCI Interrupt Route 1 (PIR1)—Offset 3142h	0h
3144h	3145h	PCI Interrupt Route 2 (PIR2)—Offset 3144h	0h
3146h	3147h	PCI Interrupt Route 3 (PIR3)—Offset 3146h	0h
3148h	3149h	PCI Interrupt Route 4 (PIR4)—Offset 3148h	0h
314Ah	314Bh	PCI Interrupt Route 5 (PIR5)—Offset 314Ah	0h
31FCh	31FFh	General Interrupt Control (GIC)—Offset 31FCh	0h
3200h	3203h	Interrupt Polarity Control 0 (IPC0)—Offset 3200h	FF0000h
3204h	3207h	Interrupt Polarity Control 1 (IPC1)—Offset 3204h	0h
3208h	320Bh	Interrupt Polarity Control 2 (IPC2)—Offset 3208h	0h
320Ch	320Fh	Interrupt Polarity Control 3 (IPC3)—Offset 320Ch	0h
3300h	3303h	ITSS Power Reduction Control (ITSSPRC)—Offset 3300h	0h
3334h	3335h	Master Message Control (MMC)—Offset 3334h	0h

30.2.1 PIRQA Routing Control (PARC)—Offset 3100h

PIRQA Routing Control Register

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

30.2.2 PIRQB Routing Control (PBRC)—Offset 3101h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

30.2.3 PIRQC Routing Control (PCRC)—Offset 3102h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

30.2.4 PIRQD Routing Control (PDRC)—Offset 3103h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

30.2.5 PIRQE Routing Control (PERC)—Offset 3104h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

30.2.6 PIRQF Routing Control (PFRC)—Offset 3105h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

30.2.7 PIRQG Routing Control (PGRC)—Offset 3106h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

30.2.8 PIRQH Routing Control (PHRC)—Offset 3107h

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Interrupt Routing Enable (REN):** When cleared, the corresponding PIRQ is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQ is not routed to the 8259.
6:4	0h RO	Reserved.
3:0	0h RW	**IRQ Routing (IR):** Bits Mapping: 1001: IRQ9 1010: IRQ10 0011: IRQ3 1011: IRQ11 0100: IRQ4 1100: IRQ12 0101: IRQ5 0110: IRQ6 1110: IRQ14 0111: IRQ7 1111: IRQ15 Others: Reserved

30.2.9 PCI Interrupt Route 0 (PIR0)—Offset 3140h

This register applies to Device 31 functions.

Access Method

Type: MSG Register
(Size: 16 bits)

Device:
Function:

Default: 3210h

Bit Range	Default and Access	Field Name (ID): Description
15	0h RO	Reserved.
14:12	3h RW	**Interrupt D Pin Route (IDR):** Indicates which PIRQ in PCH is connected to the INTD# pin reported for device 31 functions: Bits Pin Bits Pin 0h PIRQA# 4h PIRQE# 1h PIRQB# 5h PIRQF# 2h PIRQC# 6h PIRQG# 3h PIRQD# 7h PIRQH#
11	0h RO	Reserved.
10:8	2h RW	**Interrupt C Pin Route (ICR):** Refer the IDR description. This field applies to INTC#
7	0h RO	Reserved.
6:4	1h RW	**Interrupt B Pin Route (IBR):** Refer the IDR description. This field applies to INTB#.
3	0h RO	Reserved.
2:0	0h RW	**Interrupt A Pin Route (IAR):** Refer the IDR description. This field applies to INTA#.

30.2.10 PCI Interrupt Route 1 (PIR1)—Offset 3142h

Same definition as PIR0, except this register applies to Device 29 functions.

30.2.11 PCI Interrupt Route 2 (PIR2)—Offset 3144h

Same definition as PIR0, except this register applies to Device 28 functions.

30.2.12 PCI Interrupt Route 3 (PIR3)—Offset 3146h

Same definition as PIR0, except this register applies to Device 23 functions.

30.2.13 PCI Interrupt Route 4 (PIR4)—Offset 3148h

Same definition as PIR0, except this register applies to Device 22 functions.

30.2.14 PCI Interrupt Route 5 (PIR5)—Offset 314Ah

Same definition as PIR0, except this register applies to Device 20 and 18 functions.

30.2.15 General Interrupt Control (GIC)—Offset 31FCh

Note: FEC10000h - FEC3FFFFh is allocated to PCIe when Port I/OxApic Enable (PAE) bit is set.

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Alternate Access Mode Enable (AME):** When set, read only registers can be written, and write only registers can be read.
16	0h RW	**Shutdown Policy Select (SDPS):** When cleared (default) the PCH will update INIT# in response to the shutdown Vendor Defined Message (VDM). When set to 1, PCH will treat the shutdown VDM similar to receiving a CF9h I/O write, and will drive PLTRST# active. This register is reset any time PLTRST# asserts.
15:9	0h RW	**MAX_IRQ_ENTRY_SIZE (MAXIRQSIZE):** This field indicates the size of the IOAPIC entry. The default size is 120 entries. 0000000: 120 entry size 0000001: 24 entry size (Legacy mode) 0000010 - 1111111: Reserved
8:1	0h RO	Reserved.
0	0h RO/P	**CPU Shutdown Status (CPUSDSTS):** This bit is set to 1 if the CPU sends the Shutdown Special cycle message. The Shutdown Message is recognized as an INIT# event if the Shutdown Policy Select = 0, else PCH shall treat the Shutodwn Special cycle as a request for CF9 Hard Reset. This is a sticky Read Only bit that is only reset by a loss of core power.

30.2.16 Interrupt Polarity Control 0 (IPC0)—Offset 3200h

Interrupt Polarity Control 0 Register

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: FF0000h

Bit Range	Default and Access	Field Name (ID): Description
31:0	FF0000h RW	**IRQ 31-0 Active High Polarity Disable (IPC0_IRQxAHPOLDIS):** When set to 1, the interrupt polarity associated with IRQ31 down to IRQ0 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

30.2.17 Interrupt Polarity Control 1 (IPC1)—Offset 3204h

Interrupt Polarity Control 1 Register

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**IRQ 63-32 Active High Polarity Disable (IPC1_IRQAHPOLDIS):** When set to 1, the interrupt polarity associated with IRQ63 down to IRQ32 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

30.2.18 Interrupt Polarity Control 2 (IPC2)—Offset 3208h

Interrupt Polarity Control 2 Register

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RW	**IRQ 95-64 Active High Polarity Disable (IPC2_IRQAHPOLDIS):** When set to 1, the interrupt polarity associated with IRQ95 down to IRQ64 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

30.2.19 Interrupt Polarity Control 3 (IPC3)—Offset 320Ch

Interrupt Polarity Control 3 Register

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:0	0h RW	**IRQ 119-96 Active High Polarity Disable (IPC3_IRQAHPOLDIS):** When set to 1, the interrupt polarity associated with IRQ119 down to IRQ96 is inverted to appear as Active Low to IOAPIC. When set to 0, the interrupt is appears as Active High to IOAPIC.

30.2.20 ITSS Power Reduction Control (ITSSPRC)—Offset 3300h

Power controls for the entire interrupt and timer subsystem.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3	0h RW	**HPET Dynamic Clock Gating Enable (HPETDCGE):** When set, the HPET enables dynamic clock gating.
2	0h RW	**8254 Static Clock Gating Enable (CGE8254):** When set, the 8254 timer is disabled statically. This bit shall be set by BIOS if the 8254 feature is not needed in the system or before BIOS hands off the system that supports C11. Normal operation of 8254 requires this bit to 0.
1	0h RW	**Sideband Dynamic Clock Gating Enable (SBDCGE):** Setting this bit will enable all dynamic clock gating of the Sideband Clock domain.
0	0h RW	**PCI Dynamic Clock Gating Enable (PCIDCGE):** Setting this bit will enable dynamic clock gating for the Interrupt and Timer Sub System Core Logic.

30.2.21 Master Message Control (MMC)—Offset 3334h

Master Message Control Register

Access Method

Type: MSG Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:1	0h RO	Reserved.
0	0h RW/V	**Master Message Enable (MSTRMSG_EN):** When set, allows Interrupt and Timer Subsystem (ITSS) to release any pending/in progress IOAPIC memory write, HPET memory write, virtual wire event or error messages to the IO frabic. When cleared, ITSS prevents these messages from being issued to the IO frabic.

31 Real Time Clock (RTC)

31.1 FRTC IO INDEX REG Registers Summary

RTC IO Index Registers Port 70 and 71h

Table 31-1. Summary of RTC IO INDEX REG Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
70h	70h	RTC Index Register (INDEX)—Offset 70h	0h
71h	71h	RTC Target Register (TARGET)—Offset 71h	0h

31.1.1 RTC Index Register (INDEX)—Offset 70h

This 8-bit register selects which indirect register appears in the target register to be manipulated by software. Software will program this register to select the desired RTC indexed register.

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Index Register (INDEX):** Index Register for RTC

31.1.2 RTC Target Register (TARGET)—Offset 71h

This 32-bit register specifies the data to be read or written to the register pointed to by the INDEX register.

Access Method

Type: MSG Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW/V	**RTC Target Register (TARGET):** RTC Target Register for RTC

31.2 RTC Indexed Registers Summary

The RTC contains two sets of indexed registers that are accessed using the two separate Index and Target registers (70h/71h or 72h/73h), as shown in the following table:

RTC (Standard) RAM Bank
Index Name
00h Seconds
01h Seconds Alarm
02h Minutes
03h Minutes Alarm
04h Hours
05h Hours Alarm
06h Day of Week
07h Day of Month
08h Month
09h Year
0Ah Register A
0Bh Register Band
0Ch Register D
0Dh Register D
0Bh-7Fh 114 Bytes of User RAM

Table 31-2. Summary of RTC Indexed Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	0h	Seconds Value (Sec)—Offset 0h	0h
1h	1h	Seconds Alarm (Sec_Alarm)—Offset 1h	0h
2h	2h	Minutes Value (Minutes)—Offset 2h	0h
3h	3h	Minutes Alarm (Minutes_Alarm)—Offset 3h	0h
4h	4h	Hours Value (Hours)—Offset 4h	0h
5h	5h	Hours Alarm (Hours_Alarm)—Offset 5h	0h
6h	6h	Day Of Week (Day_of_Week)—Offset 6h	0h
7h	7h	Day Of Month (Day_of_Month)—Offset 7h	0h
8h	8h	Month Value (Month)—Offset 8h	0h
9h	9h	Year Value (Year)—Offset 9h	0h
Ah	Ah	Register A (RTC_REGA)—Offset Ah	0h
Bh	Bh	Register B General Configuration (Register_B)—Offset Bh	80h
Ch	Ch	Register C Flag Register (Register_C)—Offset Ch	0h

Table 31-2. Summary of RTC Indexed Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
Dh	Dh	Register D Flag Register (Register_D)—Offset Dh	80h
Eh	Eh	114 Bytes Of Lower User RAM (Register_E)—Offset Eh	0h
80h	80h	128 Bytes Of Upper User RAM (Register_80)—Offset 80h	0h

31.2.1 Seconds Value (Sec)—Offset 0h

RTC Index: 00h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current time second

31.2.2 Seconds Alarm (Sec_Alarm)—Offset 1h

RTC Index: 01h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores Seconds Alarm

31.2.3 Minutes Value (Minutes)—Offset 2h

RTC Index: 02h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current time Minutes

31.2.4 Minutes Alarm (Minutes_Alarm)—Offset 3h

RTC Index: 03h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores Alarm Minutes

31.2.5 Hours Value (Hours)—Offset 4h

RTC Index: 04h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current time Hours

31.2.6 Hours Alarm (Hours_Alarm)—Offset 5h

RTC Index: 05h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores Alarm Hours

31.2.7 Day Of Week (Day_of_Week)—Offset 6h

RTC Index: 06h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current Day of Week

31.2.8 Day Of Month (Day_of_Month)—Offset 7h

RTC Index: 07h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current Day of Month

31.2.9 Month Value (Month)—Offset 8h

RTC Index: 08h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current Month

31.2.10 Year Value (Year)—Offset 9h

RTC Index: 09h. Attribute: Read/Write. Default Value: Undefined. Size: 8-bit. This register stores current Year

31.2.11 Register A (RTC_REGA)—Offset Ah

This register is used for general configuration of the RTC functions. None of the bits are affected by RSMRST# or any other reset signal.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO/V	**UPDATE IN PROGRESS (UIP):** This bit may be monitored as a status flag. 0 = Update cycle will not start for at least 488 micro-seconds. The time, calendar, and alarm information in RAM is always available when the UIP bit is 0. 1 = The update is soon to occur or is in progress.
6:0	0h RO	Reserved.

31.2.12 Register B General Configuration (Register_B)—Offset Bh

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RW	**Update Cycle Inhibit (SET):** Enables/Inhibits the update cycles. 0 = Update cycle occurs normally once each second. 1 = A current update cycle will abort and subsequent update cycles will not occur until SET is returned to zero. When set is one, the BIOS may initialize time and calendar bytes safely. This bit is not affected by RSMRST# nor any other reset signal. Note: Software must ensure this bit is at least transitioned from '1' to '0' once whenever the RTC coin battery is inserted. This is to ensure that the internal RTC time updates occur properly.
6	0h RW	**Periodic Interrupt Enable (PIE):** 0 = Disabled. 1 = Enabled. Allows an interrupt to occur with a time base set with the RS bits of register A. This bit is cleared by RSMRST# assertion, but not on any other reset.
5	0h RW	**Alarm Interrupt Enable (AIE):** 0 = Disabled. 1 = Enabled. Allows an interrupt to occur when the AF is set from an alarm match from the update cycle. An alarm can occur once a second, one an hour, once a day, or once a month. This bit is cleared by RTCRST# assertion, but not on any other reset.
4	0h RW	**Update-ended Interrupt Enable: (UIE):** 0 = Disabled. 1 = Enabled. Allows an interrupt to occur when the update cycle ends. This bit is cleared by RSMRST# assertion, but not on any other reset.
3	0h RW	**Square Wave Enable (SQWE):** The Square Wave Enable bit serves no function in this device, yet is left in this register bank to provide compatibility with the Motorola 146818B. There is not SQW pin on this device. This bit is cleared by RSMRST# assertion, but not on any other reset.
2	0h RW	**Data Mode (DM):** This bit specifies either binary or BCD data representation. 0 = BCD. 1 = Binary. This bit is not affected by RSMRST# nor any other reset signal.
1	0h RW	**Hour Format (HOURFORM):** This bit indicates the hour byte format. 0 = Twelve-hour mode is selected.In twelve hour mode, the seventh bit represents AM as zero and PM as one. 1 = Twenty-four hour mode is selected. This bit is not affected by RSMRST# nor any other reset signal.
0	0h RW	**Daylight Savings Enable (DSE):** The Daylight Savings Enable bit triggers two special hour updates per year when set to one. One is on the first Sunday in April, where time increments from 1:59:59 AM to 3:00:00 AM. The other is the last Sunday in October when the time first reaches 1:59:59 AM, it is changed to 1:00:00 AM. The time mustincrement normally for at least two update cycles (seconds) previous to these conditions for the time change to occur properly. These special update conditions do not occur when the DSE bit is set to zero. The days for the hour adjustment are those specified in United States federal law as of 1987, which is different than previous years. If BUC.DSO bit is set, the DSE bit continues to be a R/W bit, but Daylight Saving is disabled regardless of the DSE bit. This bit is not affected by RSMRST# nor any other reset signal.

31.2.13 Register C Flag Register (Register_C)—Offset Ch

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7	0h RO/V	**Interrupt Request Flag (IRQF):** Interrupt Request Flag = (PF * PIE) + (AF * AIE) + (UF * UFE). This also causes the RTC Interrupt to be asserted. This bit is cleared upon RSMRST# assertion or a read of Register C.
6	0h RO/V	**Periodic Interrupt Flag (PF):** Periodic interrupt Flag will be one when the tap as specified by the RS bits of register A is one. If no taps are specified, this flag bit will remain at zero. This bit is cleared upon RSMRST# assertion or a read of Register C.
5	0h RO/V	**Alarm Flag (AF):** Alarm Flag will be high after all Alarm values match the current time. This bit is cleared upon RTCRST# assertion or a read of Register C.
4	0h RO/V	**Update-ended Flag (UF):** Updated-ended flag will be high immediately following an update cycle for each second. The bit is cleared upon RSMRST# assertion or a read of Register C.
3:0	0h RO	Reserved.

31.2.14 Register D Flag Register (Register_D)—Offset Dh

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 80h

Bit Range	Default and Access	Field Name (ID): Description
7	1h RO	**Valid RAM and Time Bit (VRT):** This bit is hard-wired to 1 in the RTC power well. This bit should always be written as a 0 for write cycle, however it will return a 1 for read cycles.
6	0h RO	Reserved.
5:0	0h RW	**Date Alarm (Date_Alarm):** These bits store the date of month alarm value. If set to 000000, then a dont care state is assumed. The host must configure the dates alarm for these bits to do anything, yet they can be written at any time. If the date alarm is not enabled, these bits will return zeros to mimic the functionality of the Motorola 146818B. These bits are not affected by any reset assertion.

31.2.15 114 Bytes Of Lower User RAM (Register_E)—Offset Eh

Remaining 114 Bytes of Lower User RAM. Each byte in this bank share the same description as shown below. RAM default values are undetermined and the last written value will be retained until RTC power is removed.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Lower User RAM (LOWER_USER_RAM):** RTC RAM lower unused range

31.2.16 128 Bytes Of Upper User RAM (Register_80)—Offset 80h

128 Bytes of Upper User RAM. Each byte in this bank share the same description as shown below. RAM default values are undetermined and the last written value will be retained until RTC power is removed.

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**Upper User RAM (UPPER_USER_RAM):** RTC RAM upper unused range

31.3 RTC PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 31-3. Summary of RTC PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
3400h	3403h	RTC Configuration (RC)—Offset 3400h	0h
3414h	3417h	Backed Up Control (BUC)—Offset 3414h	0h
3F04h	3F07h	RTC Update In Progress SMI Control (UIPSMI)—Offset 3F04h	0h

31.3.1 RTC Configuration (RC)—Offset 3400h

All bits in this register are in the Primary Well.

Access Method

Type: MEM Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31	0h RW/1L	**Bios Interface Lock-Down (BILD):** When set, prevents RTC version of TS (BUC.TS) from being changed. This bit can only be written from 0 to 1 once. This BILD bit has different function compared SPI and eSPI version but BIOS should set all the corresponding bits after reset in order to lock down the BIOS interface correctly.
30:7	0h RO	Reserved.
6	0h RW	**RTC High Power Mode HW Disable (HPM_HW_DIS):** When set to 1 the internal VRM that generates the rtc well supply voltage in SUS mode is disabled when SLP_S0# is asserted to '0'. (via irtcdswen pin to RTC EBB). When 0, HW control of the RTC internal VRM is disabled.
5	0h RW	**RTC High Power Mode SW Disable (HPM_SW_DIS):** When set to 1 the internal VRM that generates the rtc well supply voltage in SUS mode is disabled (via irtcdswen pin to RTC EBB). When 0 the internal VRM powers the rtc well when RSMRST# is '1'. (default)
4	0h RW/1L	**Partial Range Lock in Upper 128 Bytes (UL):** When set, bytes 38h-3Fh in the upper 128 byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any guaranteed data. Bit reset on system reset.
3	0h RW/1L	**Partial Range Lock in Lower 128 Bytes (LL):** When set, bytes 38h-3Fh in the lower 128 byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any guaranteed data. Bit reset on system reset.
2	0h RW	**Upper 128 Byte Enable (UE):** When set, the upper 128 byte bank of RTC RAM can be accessed.
1:0	0h RO	Reserved.

31.3.2 Backed Up Control (BUC)—Offset 3414h

All bits in this register are in the RTC well and only cleared by RTCRST#.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:5	0h RO	Reserved.
4	0h RW	**Daylight Savings Override (SDO):** When this bit is a '1', the DSE bit in the RTC Register B bit(0) is a RW bit but has no effect where daylight savings is hard-disabled internally. When this bit is a '0', the DSE bit in the RTC register B bit(0) is a RW bit that is configurable by software to enable the daylight savings. System BIOS shall configure this bit accordingly during the boot process before RTC time is initialized.
3:1	0h RO	Reserved.
0	0h RW/L	**Top Swap (TS):** This should be set by BIOS when the corresponding TS bit in the eSPI controller is set in order to properly restore the state of that field after reset since they are not preserved in an RTC well bit in those devices.*If PCH is strapped for Top-Swap (GNT(3)# is low at rising edge of PWROK), then this bit cannot be cleared by software. The strap jumper should be removed and the system rebooted.

31.3.3 RTC Update In Progress SMI Control (UIPSMI)—Offset 3F04h

This register exists in the Core well.

Access Method

Type: MEM Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW/1C/V	**RTC UIP Low-to-High (UIP_L2H):** This sticky status bit is set whenever the RTC Update-In-Progress signal transitions from low to high (i.e., at the start of an update).
16	0h RW/1C/V	**RTC UIP High-to-Low (UIP_H2L):** This sticky status bit is set whenever the RTC Update-In-Progress signal transitions from high to low (i.e., at the start of an update).
15:2	0h RO	Reserved.
1	0h RW	**RTC UIP Low-to-High SMI Enable (UIP_L2H_SMI_en):** When this bit is set, a '1' in bit 17 will assert the internal SMI signal to the Power Management SMI logic
0	0h RW	**RTC UIP High-to-Low SMI Enable (UIP_H2L_SMI_en):** When this BIOS is set, a '1' in bit 16 will assert the internal SMI signal to the Power Management SMI logic

32 System Management TCO

32.1 SMBus TCO I/O Registers Summary

The TCO I/O registers reside in a 32-byte range that starts from the IO Base Address described in the TCOBAR register in the SMBus PCI Configuration space.

Table 32-1. Summary of SMBus TCO I/O Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
0h	1h	TCO_RLD Register (TRLD)—Offset 0h	4h
2h	2h	TCO_DAT_IN Register (TDI)—Offset 2h	0h
3h	3h	TCO_DAT_OUT Register (TDO)—Offset 3h	0h
4h	5h	TCO1_STS Register (TSTS1)—Offset 4h	0h
6h	7h	TCO2_STS Register (TSTS2)—Offset 6h	0h
8h	9h	TCO1_CNT Register (TCTL1)—Offset 8h	0h
Ah	Bh	TCO2_CNT Register (TCTL2)—Offset Ah	8h
Ch	Dh	TCO Message Registers (TMSG)—Offset Ch	0h
Eh	Eh	TCO_WDSTATUS Register (TWDS)—Offset Eh	0h
10h	10h	LEGACY_ELIM Register (LE)—Offset 10h	3h
12h	13h	TCO_TMR Register (TTMR)—Offset 12h	4h

32.1.1 TCO_RLD Register (TRLD)—Offset 0h

TCO_RLD Register

Access Method

Type: IO Register
(Size: 16 bits)

Device:
Function:

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
15:10	0h RO	Reserved.
9:0	4h RW	**TCORLD (TCORLD):** Reading this register will return the current count of the TCO timer. Writing any value to this register will reload the timer to prevent the timeout.

32.1.2 TCO_DAT_IN Register (TDI)—Offset 2h

TCO_DAT_IN Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**TCO_DAT_IN (TDI):** Data Register for passing commands from the OS to the SMI handler. Writes to this register will cause an SMI and set the OS_TCO_SMI bit in the TCO_STS register.

32.1.3 TCO_DAT_OUT Register (TDO)—Offset 3h

TCO_DAT_OUT Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**TCO_DAT_OUT (TDO):** Data Register for passing commands from the SMI handler to the OS. Writes to this register will set the TCO_INT_STS bit in the TCO_STS register. It also causes an interrupt, as selected by the TCO_IRQ_SEL bits.

32.1.4 TCO1_STS Register (TSTS1)—Offset 4h

Unless otherwise indicated, these bits are sticky and are cleared by writing a 1 to the corresponding bit position.

Access Method

Type: IO Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:14	0h RO	Reserved.
13	0h RO	**TCO Slave Select (TCO_SLVSEL):** This register bit indicates the value of TCO Slave Select Soft Strap.
12	0h RW/1C	**CPUSERR_STS (CPUSERR_STS):** This bit is set to 1 if the CPU complex sends a DMI special cycle message indicating that it wants to cause an SERR#. The software must read the MCH to find out why it wanted the SERR#. Software must write a 1 back to this bit to clear it.

Bit Range	Default and Access	Field Name (ID): Description
11	0h RO	Reserved.
10	0h RW/1C	**CPUSMI_STS (CPUSMI_STS):** This bit is set to 1 if the CPU complex sends a DMI special cycle message indicating that it wants to cause an SMI. The software must read the CPU to find out why it wanted the SMI. Software must write a 1 back to this bit to clear it.
9	0h RW/1C	**CPUSCI_STS (CPUSCI_STS):** This bit is set to 1 if the CPU complex sends a DMI special cycle message indicating that it wants to cause an SCI. The software must read the CPU to find out why it wanted the SCI. Software must write a 1 back to this bit to clear it.
8	0h RW/1C	**BIOSWR_STS (BIOSWR_STS):** Intel PCH sets this bit to 1 and generates an SMI# to indicate an unsupported attempt to write to the BIOS located in the FWH. This occurs when either: a) The BIOSWP bit is changed from 0 to 1 and the LE bit is also set, or b) Any write is attempted to the BIOS and the BIOSWP bit is also set. This bit does not get set to 1 when: 1) a or b above occurs on eSPI controller. 2) a or b above occurs on SPI Flash controller. Note: On write cycles attempted to the 4MB lower alias to the BIOS space, the BIOSWR_STS bit will not be set.
7	0h RW/1C	**NEWCENTURY_STS (NEWCENTURY_STS):** This bit will be set when the year rolls over from 1999 to 2000. If the bit is already 1, it will remain 1. This bit can be cleared either by software writing a 1 back to the bit position, or by RTCRST# going active. When this bit is set, an SMI# will be generated. However, this will not be a wake event (i.e. if the system is in a sleeping state when the NEWCENTURY_STS bit is set, the system will not wake up). Note: This bit 7 is not valid when the RTC battery is first put in (or if the RTC battery does not provide sufficient power when the system is unplugged). Software can determine that the RTC well was not maintained by checking the RTC_PWR_STS bit (GEN_PMCON_3 register in the Power Management Controller, D31:F2:A4, bit 2) or by other means (such as doing a checksum on the RTC RAM array). If the RTC well is determined to not have been maintained, the BIOS should set the time to a legal value and then clear the NEWCENTURY_STS bit. Note: This bit may take up to 3 RTCCLKs for the bit to be cleared when a 1 is written to the bit to clear it. After writing a 1 to the NEWCENTURY_STS bit, software should also not exit the SMI handler until after the bit has been cleared. This is to make sure the SMI is not re-entered. BIOS Assumption: When booting, the BIOS checks the NEWCENTURY_STS bit. If set, the BIOS should increment the value in the RTC RAM register associated with the century. The BIOS should then clear the NEWCENTURY_STS bit. This scenario would occur if the system was asleep when the century rolls over. If the system is in an S0 state (not sleeping) and the SMI# occurs with the NEWCENTURY_STS bit sets, the SMI handler should increment the value in the RTC RAM register and clear the NEWCENTURY_STS bit.
6:4	0h RO	Reserved.
3	0h RW/1C	**TIMEOUT (TIMEOUT):** Bit set to 1 by Intel PCH to indicate that the SMI was caused by TCO timer reaching 0. Note: The SMI handler should clear this bit to prevent an immediate re-entry to the SMI handler.
2	0h RW/1C	**TCO_INT_STS (TCO_INT_STS):** Bit set to 1 when SMI handler caused the interrupt by writing to the TCO_DAT_OUT register.
1	0h RW/1C	**OS_TCO_SMI (OS_TCO_SMI):** Bit set to 1 when OS code caused an SMI# by writing to the TCO_DAT_IN register.
0	0h RO/V	**NMI2SMI_STS (NMI2SMI_STS):** The PCH sets this bit when an SMI# occurs because an event occurred that would otherwise have caused an NMI.

32.1.5 TCO2_STS Register (TSTS2)—Offset 6h

TCO2_STS Register

Access Method

Type: IO Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:5	0h RO	Reserved.
4	0h RW/1C	**SMLINK_SLAVE_SMI_STS (SMLINK_SLAVE_SMI_STS):** The PCH will set this bit to 1 when it receives the SMI message (encoding 08h in the command type) on the SMLinks Slave Interface. Software clears the bit by writing a 1 to this bit position. This bit is in the resume well. It is reset by RSMRST#, but not by the PCI Reset associated with exit from S3-S5 states. This allows the software (presumably BIOS) to get the interrupt, refer this new bit set, and decidedly go into the pre-determined (by local policy) sleep state.
3	0h RO	Reserved.
2	0h RO/V	**NO_REBOOT_PIN_STRAP_STATUS (NRSTRAP_STS):** This bit reflects the state of the No_Reboot strap that is sampled on PWROK rise.
1	0h RW/1C	**SECOND_TO_STS (SECOND_TO_STS):** Intel PCH sets this bit to 1 to indicate that the TIMEOUT bit had been (or is currently) set and a second timeout occurred before the TCO_RLD register was written. If this bit is set and the NO_REBOOT config bit is 0, then the Intel PCH will reboot the system after the second timeout. The reboot is done by asserting PLTRST#. This bit is only cleared by writing a 1 to this bit or by a RSMRST#.
0	0h RW/1C	**INTRD_DET (INTRD_DET):** The bit is set to 1 by the PCH to indicate that an intrusion was detected. This bit is cleared by writing a 1 to this bit or by RTCRST#. Note: This bit has a recovery time. After writing a 1 to this bit position (to clear it), the bit may be read back as a 1 for up 65 microseconds before it is read as a 0. Software must be aware of this recovery time when reading this bit after clearing it. Note: If the INTRUDER# signal is active when the software attempts to clear the INTRD_DET bit, the bit will remain as a 1, and the SMI# will be generated again immediately. The SMI handler can clear the INTRD_SEL bits to avoid further SMIs. However, if the INTRUDER# signals goes inactive and then active again, there will not be further SMIs. If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written as a 1, then the INTRD_DET signal will go to a 0 when INTRUDER# input signal goes inactive. Note that this is slightly different than a classic sticky bit, since most sticky bits would remain active indefinitely when the signal goes active and would immediately go inactive when a 1 is written to the bit.

32.1.6 TCO1_CNT Register (TCTL1)—Offset 8h

TCO1_CNT Register

Access Method

Type: IO Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:13	0h RO	Reserved.
12	0h RW	**TCO_LOCK (TCO_LOCK):** When set to 1, this bit prevents writes from changing the TCO_EN bit (in offset 30h of Power Management I/O space). Once this bit is set to 1, it can not be cleared by software writing a 0 to this bit location. A core-well reset is required to change this bit from 1 to 0. This bit defaults to 0.
11	0h RW	**TCO_TMR_HALT (TCO_TMR_HALT):** 1 = The TCO timer will halt. It will not count, and thus cannot reach a value that would cause an SMI# or to cause the SECOND_TO_STS bit to be set. This will also prevent rebooting. 0 = The TCO timer is enabled to count. This is the default.
10	0h RO	Reserved.
9	0h RW	**NMI2SMI_EN (NMI2SMI_EN):** Setting this bit 1 forces all NMIs to instead cause an SMI#, and will be reported in the TCO1_STS register. NMI2SMI_EN bit is set AND the NMI_EN# bit is set to 0, the NMI# will be routed to cause an SMI#. No NMI will be caused. However, if the GBL_SMI_EN bit is not set, then no SMI# will be generated, either. If NMI2SMI_EN is set but the NMI_EN# bit is set to 1, then no NMI or SMI# will be generated. The following table shows the possible combinations: NMI_EN#, GBL_SMI_EN 00: No SMI# based on NMI events (since no SMI# at all because SMI_EN = 0) 01: SMI# will be caused based on NMI events 10: No SMI# at all because SMI_EN is 0 11: No SMI# based on NMI events because NMI_EN#=1
8	0h RW	**NMI_NOW (NMI_NOW):** Writing a 1 to this bit causes an NMI. This allows the BIOS or SMI handler to force entry to the NMI handler. The NMI handler is expected to clear this bit. Another NMI will not be generated until the bit is cleared by writing a 1 back to the same bit position.
7:1	0h RO	Reserved.
0	0h RW	**NO_REBOOT_MSUS (NR_MSUS):** This bit reflects the No Reboot pin strap state. It is sampled high on PWROK. This bit may be set or cleared by software if the strap is sampled low but may not override the strap when the it indicates No Reboot. When set, the TCO timer will count down and generate the SMI# on the first timeout, but will not reboot on the second timeout.

32.1.7 TCO2_CNT Register (TCTL2)—Offset Ah

TCO2_CNT Register

Access Method

Type: IO Register
(Size: 16 bits)

Device:
Function:

Default: 8h

Bit Range	Default and Access	Field Name (ID): Description
15:6	0h RO	Reserved.
5:4	0h RW	**OS_POLICY (OS_POLICY):** OS-based software writes to these bits to select the policy that the BIOS will use after the platform resets due the WDT. The following convention is recommended for the BIOS and OS: 00 Boot normally 01 Shut down 10 Dont load OS. Hold in pre-boot state and use LAN to determine next step 11 Reserved Implementation note: These are just scratch pad bits. They should not be reset when the TCO logic resets the platform due to Watchdog Timer.
3	1h RW	**SMB_ALERT_DISABLE (SMB_ALERT_DISABLE):** Disables muxed GPIO/ SMBALERT# signal as an alert source for the heartbeats and the SMBus slave. At reset (RSMRST# pin assertion only), this bit is set and the muxed GPIO/SMBALERT# alerts are disabled.
2:1	0h RW	**INTRD_SEL (INTRD_SEL):** Selects the action to take if the INTRUDER# signal goes active. 11: Reserved 01: Interrupt (as selected by TCO_INT_SEL). 10: SMI# 00 INTRUDER# does not cause SMI# or interrupt
0	0h RO	Reserved.

32.1.8 TCO Message Registers (TMSG)—Offset Ch

TCOBASE+0Ch (MSG1) TCOBASE+0Dh (MSG2) BIOS can write into these registers to indicate its boot progress. The external microcontroller can read these registers to monitor the boot progress

Access Method

Type: IO Register
(Size: 16 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RW	**TCO Message2 (MSG2):** TCO Message2
7:0	0h RW	**TCO Message1 (MSG1):** TCO Message1

32.1.9 TCO_WDSTATUS Register (TWDS)—Offset Eh

TCO_WDSTATUS Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
7:0	0h RW	**TCO_WDSTATUS Register (TWDS):** The BIOS or system management software can write into this register to indicate more details on the boot progress. The register will rest to 00h based on a RSMRST# (but not PCI Reset). The external microcontroller can read this register to monitor boot progress.

32.1.10 LEGACY_ELIM Register (LE)—Offset 10h

LEGACY_ELIM Register

Access Method

Type: IO Register
(Size: 8 bits)

Device:
Function:

Default: 3h

Bit Range	Default and Access	Field Name (ID): Description
7:2	0h RO	Reserved.
1	1h RW	**IRQ12_CAUSE (IRQ12_CAUSE):** When software sets the bit to 1, IRQ12 will be high (asserted). When software sets the bit to 0, IRQ12 will be low (not asserted). Default for this bit is 1.
0	1h RW	**IRQ1_CAUSE (IRQ1_CAUSE):** When software sets the bit to 1, IRQ1 will be high (asserted). When software sets the bit to 0, IRQ1 will be low (not asserted). Default for this bit is 1.

32.1.11 TCO_TMR Register (TTMR)—Offset 12h

TCO_TMR Register

Access Method

Type: IO Register
(Size: 16 bits)

Device:
Function:

Default: 4h

Bit Range	Default and Access	Field Name (ID): Description
15:10	0h RO	Reserved.
9:0	4h RW	**TCOTMR (TCOTMR):** Value that is loaded into the timer each time the TCO_RLD register is written. Values of 0000h or 0001h will be ignored and should not be attempted. The timer is clocked at approximately 0.6 seconds, and thus allows timeouts ranging from 1.2 second to 613.8 seconds. Note: The timer has an error of +/- 1 tick (0.6s).

33 FIA Configuration

33.1 FIA Configuration PCR Registers Summary

Table 33-1. Summary of FIA Configuration PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
100h	103h	PCIe Device Reference Clock Request Enable 1 (PDRCRE1)—Offset 100h	0h
108h	10Bh	PCIe Device Reference Clock Request Mapping 1 (PDRCRM1)—Offset 108h	40C2040h
10Ch	10Fh	PCIe Device Reference Clock Request Mapping 2 (PDRCRM2)—Offset 10Ch	9207185h
110h	113h	PCIe Device Reference Clock Request Mapping 3 (PDRCRM3)—Offset 110h	2CAh
300h	303h	HSIO Lane Owner Status 1 (LOS1)—Offset 300h	0h
304h	307h	HSIO Lane Owner Status 2 (LOS2)—Offset 304h	0h

33.1.1 PCIe Device Reference Clock Request Enable 1 (PDRCRE1)—Offset 100h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	Reserved.
11	0h RW/L	**PCIe Root Port 12 CLKREQ Mapping Enable (P11CKRQME):** Same description as bit 0.
10	0h RW/L	**PCIe Root Port 11 CLKREQ Mapping Enable (P10CKRQME):** Same description as bit 0.
9	0h RW/L	**PCIe Root Port 10 CLKREQ Mapping Enable (P9CKRQME):** Same description as bit 0.
8	0h RW/L	**PCIe Root Port 9 CLKREQ Mapping Enable (P8CKRQME):** Same description as bit 0.
7	0h RW/L	**PCIe Root Port 7 CLKREQ Mapping Enable (P7CKRQME):** Same description as bit 0.
6	0h RW/L	**PCIe Root Port 7 CLKREQ Mapping Enable (P6CKRQME):** Same description as bit 0.
5	0h RW/L	**PCIe Root Port 6 CLKREQ Mapping Enable (P5CKRQME):** Same description as bit 0.
4	0h RW/L	**PCIe Root Port 5 CLKREQ Mapping Enable (P4CKRQME):** Same description as bit 0.

Bit Range	Default & Access	Field Name (ID): Description
3	0h RW/L	**PCIe Root Port 4 CLKREQ Mapping Enable (P3CKRQME):** Same description as bit 0.
2	0h RW/L	**PCIe Root Port 3 CLKREQ Mapping Enable (P2CKRQME):** Same description as bit 0.
1	0h RW/L	**PCIe Root Port 2 CLKREQ Mapping Enable (P1CKRQME):** Same description as bit 0.
0	0h RW/L	**PCIe Root Port 1 CLKREQ Mapping Enable (P0CKRQME):** The mapping of PCIe Root Port to the corresponding CLKREQ# pin is configured by this field. 1 = This PCIe Root Port has the CLKREQ pin presence and the corresponding register (PDRCRM) will indicate which CLKREQ# pin the PCIe Root Port is mapped to. 0 = no presence and will be masked to a de-asserted state.

33.1.2 PCIe Device Reference Clock Request Mapping 1 (PDRCRM1)—Offset 108h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 40C2040h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:24	4h RW/L	**PCIe Root Port 5 CLKREQ Mapping (P4CKRQM):** Same definition as bits[4:0].
23	0h RO	Reserved.
22:18	3h RW/L	**PCIe Root Port 4 CLKREQ Mapping (P3CKRQM):** Same definition as bits[4:0].
17	0h RO	Reserved.
16:12	2h RW/L	**PCIe Root Port 3 CLKREQ Mapping (P2CKRQM):** Same definition as bits[4:0].
11	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
10:6	1h RW/L	**PCIe Root Port 2 CLKREQ Mapping (P1CKRQM):** Same definition as bits[4:0].
5	0h RO	Reserved.
4:0	0h RW/L	**PCIe Root Port 1 CLKREQ Mapping (P0CKRQM):** The mapping of the PCIe* Root Port to the corresponding CLKREQ# pin is configured by this field. This register is only valid if the corresponding enable bit in PDRCRE register is set to 1. 00h: The PCIe* Root Port maps to CLKREQ0# pin 01h: The PCIe* Root Port maps to CLKREQ1# pin 02h: The PCIe* Root Port maps to CLKREQ2# pin ... 0Eh: The PCIe* Root Port maps to CLKREQ14# pin 0Fh: The PCIe* Root Port maps to CLKREQ15# pin Others: Reserved NOTE: If a CLKREQ# pin is not implemented in hardware, the corresponding encoding is reserved. Software must never map multiple PCIe* Root Ports to the same CLKREQ# pin. The hardware behavior is undefined if this ever happens. Configuring this field to map to any unsupported CLKREQ# pins may result in undefined hardware behavior.

33.1.3 PCIe Device Reference Clock Request Mapping 2 (PDRCRM2)—Offset 10Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 9207185h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	Reserved.
28:24	9h RW/L	**PCIe Root Port 10 CLKREQ Mapping (P9CKRQM):** Same description as bits[4:0].
23	0h RO	Reserved.
22:18	8h RW/L	**PCIe Root Port 9 CLKREQ Mapping (P8CKRQM):** Same description as bits[4:0].
17	0h RO	Reserved.
16:12	7h RW/L	**PCIe Root Port 8 CLKREQ Mapping (P7CKRQM):** Same description as bits[4:0].
11	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
10:6	6h RW/L	**PCIe Root Port 7 CLKREQ Mapping (P6CKRQM):** Same description as bits[4:0].
5	0h RO	Reserved.
4:0	5h RW/L	**PCIe Root Port 6 CLKREQ Mapping (P5CKRQM):** The mapping of the PCIe* Root Port to the corresponding CLKREQ# pin is configured by this field. This register is only valid if the corresponding enable bit in PDRCRE register is set to 1. 00h: The PCIe* Root Port maps to CLKREQ0# pin 01h: The PCIe* Root Port maps to CLKREQ1# pin 02h: The PCIe* Root Port maps to CLKREQ2# pin ... 0Eh: The PCIe* Root Port maps to CLKREQ14# pin 0Fh: The PCIe* Root Port maps to CLKREQ15# pin Others: Reserved NOTE: If a CLKREQ# pin is not implemented in hardware, the corresponding encoding is reserved. Software must never map multiple PCIe* Root Ports to the same CLKREQ# pin. The hardware behavior is undefined if this ever happens. Configuring this field to map to any unsupported CLKREQ# pins may result in undefined hardware behavior.

33.1.4 PCIe Device Reference Clock Request Mapping 3 (PDRCRM3)—Offset 110h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2CAh

Bit Range	Default & Access	Field Name (ID): Description
31:11	0h RO	Reserved.
10:6	Bh RW/L	**PCIe Root Port 12 CLKREQ Mapping (P11CKRQM):** Same description as bits[4:0].
5	0h RO	Reserved.
4:0	Ah RW/L	**PCIe Root Port 11 CLKREQ Mapping (P10CKRQM):** The mapping of the PCIe* Root Port to the corresponding CLKREQ# pin is configured by this field. This register is only valid if the corresponding enable bit in PDRCRE register is set to 1. 00h: The PCIe* Root Port maps to CLKREQ0# pin 01h: The PCIe* Root Port maps to CLKREQ1# pin 02h: The PCIe* Root Port maps to CLKREQ2# pin ... 0Eh: The PCIe* Root Port maps to CLKREQ14# pin 0Fh: The PCIe* Root Port maps to CLKREQ15# pin Others: Reserved NOTE: If a CLKREQ# pin is not implemented in hardware, the corresponding encoding is reserved. Software must never map multiple PCIe* Root Ports to the same CLKREQ# pin. The hardware behavior is undefined if this ever happens. Configuring this field to map to any unsupported CLKREQ# pins may result in undefined hardware behavior.

33.1.5 HSIO Lane Owner Status 1 (LOS1)—Offset 300h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RO/V	**Lane 7 Owner (L7O):** Same description as bits [3:0].
27:24	0h RO/V	**Lane 6 Owner (L6O):** Same description as bits [3:0].
23:20	0h RO/V	**Lane 5 Owner (L5O):** Same description as bits [3:0].
19:16	0h RO/V	**Lane 4 Owner (L4O):** Same description as bits [3:0].
15:12	0h RO/V	**Lane 3 Owner (L3O):** Same description as bits [3:0].
11:8	0h RO/V	**Lane 2 Owner (L2O):** Same description as bits [3:0].
7:4	0h RO/V	**Lane 1 Owner (L1O):** Same description as bits [3:0].
3:0	0h RO/V	**Lane 0 Owner (L0O):** This register indicates the lane owner for Lane 0. 0000: PCIe. 0001: USB3.2. 0010: SATA. 0011: GbE. 1111: No owner Others: Reserved.

33.1.6 HSIO Lane Owner Status 2 (LOS2)—Offset 304h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:12	0h RO/V	**Lane 11 Owner (L11O):** Same description as bits [3:0].

Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RO/V	**Lane 10 Owner (L10O):** Same description as bits [3:0].
7:4	0h RO/V	**Lane 9 Owner (L9O):** Same description as bits [3:0].
3:0	0h RO/V	**Lane 8 Owner (L8O):** This register indicates the lane owner for Lane 0. 0000: PCIe. 0001: USB3.2. 0010: SATA. 0011: GbE. 1111: No owner Others: Reserved.

34 On Package DMI (OPDMI)

34.1 OPI PCR Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 34-1. Summary of OPDMI PCR Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
2014h	2017h	Virtual Channel 0 Resource Control (V0CTL)—Offset 2014h	80000000h
2018h	201Bh	Virtual Channel 0 Resource Status (V0STS)—Offset 2018h	0h
2020h	2023h	Virtual Channel 1 Resource Control (V1CTL)—Offset 2020h	0h
2024h	2027h	Virtual Channel 1 Resource Status (V1STS)—Offset 2024h	0h
2044h	2043h	ME Virtual Channel (VCM) Resource Control (VMCTL)—Offset 2040h	0h
2046h	2047h	ME Virtual Channel Resource Status (VMSTS)—Offset 2046h	0h
2084h	2087h	Uncorrectable Error Status (UES)—Offset 2084h	0h
2088h	208Bh	Uncorrectable Error Mask (UEM)—Offset 2088h	0h
208Ch	208Fh	Uncorrectable Error Severity (UEV)—Offset 208Ch	0h
2090h	2093h	Correctable Error Status (CES)—Offset 2090h	0h
2094h	2097h	Correctable Error Mask (CEM)—Offset 2094h	2000h
20ACh	20AFh	Root Error Command (REC)—Offset 20ACh	0h
20B0h	20B3h	Root Error Status (RES)—Offset 20B0h	0h
20B4h	20B7h	Error Source Identification (ESID)—Offset 20B4h	0h
2234h	2237h	DMI Control Register (DMIC)—Offset 2234h	0h
223Ch	223Fh	IOSF Primary Control And Status (IPCS_IOSFSBCS)—Offset 223Ch	0h
2304h	2307h	DMI Port Link Control (DMILINKC)—Offset 2304h	0h
2320h	2323h	DMI PLL Shutdown (DMIPLLDOWN)—Offset 2320h	0h
2334h	2337h	DMI Power Management Control (DMIPMCTL)—Offset 2334h	0h
2608h	260Bh	Target Link Speed (TLS)—Offset 2608h	2h
2618h	261Bh	Link Configuration (LCFG)—Offset 2618h	0h
2730h	2733h	eSPI Generic I/O Range 1 (LPCLGIR1)—Offset 2730h	0h
2734h	2737h	eSPI Generic I/O Range 2 (LPCLGIR2)—Offset 2734h	0h
2738h	273Bh	eSPI Generic I/O Range 3 (LPCLGIR3)—Offset 2738h	0h
273Ch	273Fh	eSPI Generic I/O Range 4 (LPCLGIR4)—Offset 273Ch	0h
2740h	2743h	eSPI Generic Memory Range (LPCGMR)—Offset 2740h	0h
2744h	2747h	eSPI BIOS Decode Enable (LPCBDE)—Offset 2744h	FFCFh
274Ch	274Fh	General Control and Status (GCS)—Offset 274Ch	0h
2750h	2753h	I/O Trap Register 1 - Lower DW (IOT1_LOW)—Offset 2750h	0h
2754h	2757h	I/O Trap Register 1 - Upper DW (IOT1_HIGH)—Offset 2754h	0h
2770h	2773h	eSPI I/O Decode Range (LPCIOD)—Offset 2770h	0h
2774h	2777h	eSPI I/O Enable (LPCIOE)—Offset 2774h	0h
2778h	277Bh	TCO Base Address (TCOBASE)—Offset 2778h	0h
27ACh	27AFh	PM Base Address (PMBASEA)—Offset 27ACh	0h
27B0h	27B3h	PM Base Control (PMBASEC)—Offset 27B0h	0h
27B4h	27B7h	ACPI Base Address (ACPIBA)—Offset 27B4h	0h
27B8h	27BBh	ACPI Base Destination ID (ACPIBDID)—Offset 27B8h	0h

34.1.1 Virtual Channel 0 Resource Control (V0CTL)—Offset 2014h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 80000000h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**Virtual Channel Enable (EN):** Enables the VC when set. Disables the VC when cleared.
30:27	0h RO	Reserved.
26:24	0h RO	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel
23:16	0h RO	Reserved.
15:10	0h RW/L	**Extended TC/VC Map (ETVM):** Defines the upper 8-bits of the VC0 16-bit TC/VC mapping registers. These registers use the PCI Express reserved TC[3] traffic class bit.This register is locked down if the TCA1.TCLOCKDN register is Read-Only if DMIC.SRL field is set.
9:7	0h RO	Reserved.
6:1	0h RW/L	**Transaction Class / Virtual Channel Map (TVM):** Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. This register is Read-Only if DMIC.SRL field is set.
0	0h RO	Reserved.

34.1.2 Virtual Channel 0 Resource Status (V0STS)—Offset 2018h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RO/V	**VC Negotiation Pending (NP):** When set, indicates the virtual channel is still being negotiated with ingress ports.
16:0	0h RO	Reserved.

34.1.3 Virtual Channel 1 Resource Control (V1CTL)—Offset 2020h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Virtual Channel Enable (EN):** Enables the VC when set. Disables the VC when cleared.
30:28	0h RO	Reserved.
27:24	0h RW/L	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel. Note: BIOS is required to program VCID[3] to 0 when operating at DMI2.
23:16	0h RO	Reserved.
15:10	0h RW/L	**Extended TC/VC Map (ETVM):** Defines the upper 8-bits of the VC1 16-bit TC/VC mapping registers. These registers use the PCI Express reserved TC[3] traffic class bit. This register is Read-Only if the DMIC.SRL field is set. If VC1 is not enabled, the register output sent to the users of this register is forced to 0.
9:8	0h RO	Reserved.
7:1	0h RW/L	**Transaction Class / Virtual Channel Map (TVM):** Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. This register is Read-Only if the DMIC.SRL field is set. If VC1 is not enabled, the register output sent to the users of this register is forced to 0.
0	0h RO	Reserved.

34.1.4 Virtual Channel 1 Resource Status (V1STS)—Offset 2024h

Virtual Channel 1 Resource Status

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RO/V	**VC Negotiation Pending (NP):** When set, indicates the virtual channel is still being negotiated with ingress ports.
16:0	0h RO	Reserved.

34.1.5 ME Virtual Channel (VCM) Resource Control (VMCTL)—Offset 2040h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Virtual Channel Enable (EN):** Enables the VC when set. Disables the VC when cleared.
30:28	0h RO	Reserved.
27:24	0h RW/L	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel. Note: BIOS is required to program VCIC[3] to 0 when operating at DMI2.
23:16	0h RO	Reserved.
15:10	0h RW/L	**Extended TC/VC Map (ETVM):** Defines the upper 8-bits of the VCm 16-bit TC/VC mapping registers. These registers use the PCIe reserved TC[3] traffic class bit. This register is Read-Only if the DMIC.SRL field is set. If VCm is not enabled, the register output sent to the users of this register is forced to 0. This register is Read-Only if DMIC.SRL field is set
9:8	0h RO	Reserved.
7:1	0h RW/L	**Transaction Class / Virtual Channel Map (TVM):** Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. This register is Read-Only if the DMIC.SRL field is set. If VCm is not enabled, the register output sent to the users of this register is forced to 0. This register is Read-Only if DMIC.SRL field is set
0	0h RO	Reserved.

34.1.6 ME Virtual Channel Resource Status (VMSTS)—Offset 2046h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RO/V	**VC Negotiation Pending (NP):** When set, indicates the virtual channel is still being negotiated with ingress ports.
16:0	0h RO	Reserved.

34.1.7 Uncorrectable Error Status (UES)—Offset 2084h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved.
20	0h RW/1C/V/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0h RO	**ECRC Error Status (EE):** ECRC is not supported.
18	0h RW/1C/V/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0h RW/1C/V/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0h RO	**Unexpected Completion Status (UC):** Reserved, not supported.
15	0h RW/1C/V/P	**Completer Abort Status (CA):** Indicates a completer abort was received.
14	0h RO	**Completion Timeout Status (CT):** Reserved, not supported.
13	0h RO	**Flow Control Protocol Error Status (FCPE):** Reserved, not supported.
12	0h RW/1C/V/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.
11:5	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/1C/V/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	0h RO	Reserved.
0	0h RO	**Training Error Status (TE):** Not supported.

34.1.8 Uncorrectable Error Mask (UEM)—Offset 2088h

When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. These registers are reset by core PWROK.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved.
20	0h RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0h RO	**ECRC Error Mask (EE):** ECRC is not supported.
18	0h RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs.
17	0h RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.
16	0h RO	**Unexpected Completion Mask (UC):** Reserved, Not supported.
15	0h RW/P	**Completer Abort Mask (CM):** Mask for completer abort.
14	0h RO	**Completion Timeout Mask (CT):** Reserved, not supported.
13	0h RO	**Flow Control Protocol Error Mask (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:5	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	0h RO	Reserved.
0	0h RO	**Training Error Mask (TE):** Not supported.

34.1.9 Uncorrectable Error Severity (UEV)—Offset 208Ch

These registers are reset by core PWROK

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	Reserved.
20	0h RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0h RO	**ECRC Error Severity (EE):** Not Supported.
18	0h RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.
17	0h RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0h RO	**Unexpected Completion Severity (UC):** Not supported.
15	0h RW/P	**Completer Abort Severity (CA):** Severity for completer.
14	0h RO	**Completion Timeout Severity (CT):** Not supported.
13	0h RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0h RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.
11:5	0h RO	Reserved.
4	0h RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	0h RO	Reserved.
0	0h RW/P	**Training Error Severity (TE):** TE not supported. This bit is RW for ease of implementation.

34.1.10 Correctable Error Status (CES)—Offset 2090h

These registers are reset by core PWROK

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	0h RW/1C/V/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that a Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.
11:9	0h RO	Reserved.
8	0h RW/1C/V/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.
7	0h RW/1C/V/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.
6	0h RW/1C/V/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	0h RO	Reserved.
0	0h RW/1C/V/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

34.1.11 Correctable Error Mask (CEM)—Offset 2094h

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. These registers are reset by core PWROK.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	Reserved.
13	1h RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0h RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	0h RO	Reserved.
8	0h RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0h RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.
6	0h RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.
5:1	0h RO	Reserved.
0	0h RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

34.1.12 Root Error Command (REC)—Offset 20ACh

In an exposed AER capability, this register allows errors to generate interrupts. For this implementation, and for RCRBs in general, interrupts cannot be generated, so this register is reserved.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Drop Poisoned Downstream Packets (DPDP):** When set to a '1': if downstream packet on OPI is received with the EP bit set, this packet and all subsquent packets with data received on DMI for any VC will have their Unsupported Transaction (UT) field set causing them to be forwarded to the Error Handler. When cleared to a '0', downstream packets from OPI with the EP bit set are forwarded onto the downstream backbone normally.
30	0h RW	**Unsupported Transaction Policy Bit (UTPB):** When set to 1, the Unsupported Transactions detected on OPI will not set the UES.URE bit. This subsequently ensures that SERR will never be signaled in response to Unsupported Transactions regardless of UEV.URE. When set to 0, the Unsupported Transactions detected on OPI will set the UES.URE bit.
29:3	0h RO	Reserved.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RO	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device. Not implemented by PCH.
1	0h RO	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device. Not implemented in PCH.
0	0h RO	Reserved.

34.1.13 Root Error Status (RES)—Offset 20B0h

In an exposed AER capability, this register can track more than one error and set the "multiple" bits if a second or subsequent error occurs and the first has not been serviced. For this implementation, only one error will be captured.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Advanced Error Interrupt Message Number (AEMN):** There is only one error interrupt allocated.
26:4	0h RO	Reserved.
3	0h RO	**Multiple ERR_FATAL/NONFATAL Recvieved (MENR):** Set when either a fatal or a non-fatal error is received and the ENR bit is already set. This is not supported in PCH.
2	0h RW/1C/V	**ERR_FATAL/NONFATAL Received (ENR):** Set when either a fatal or a non-fatal error message is received or an internal fatal error is detected (all internal uncorrectable errors are fatal).
1	0h RO	**Multiple ERR_COR Received (MCR):** Set when a correctable error message is received and the CR bit is already set. This is not supported in PCH
0	0h RW/1C/V	**ERR_COR Received (CR):** Set when a correctable error message is received or an internal correctable error is detected.

34.1.14 Error Source Identification (ESID)—Offset 20B4h

Error Source Identification

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO/V	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the requester ID indicated in the received ERR_FATAL or ERR_NONFATAL message when RES.ENR is first set, or the internal requestor ID if an internally detected error.
15:0	0h RO/V	**ERR_COR Source Identification (ECSID):** Loaded with the requester ID indicated in the received ERR_COR message when RES.CR is first set, or the internal requester ID if an internally detected error

34.1.15 DMI Control Register (DMIC)—Offset 2234h

DMI Control Register (Common)

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**Secured Register Lock (SRL):** When this bit is set, all the secured registers will be locked and will be Read-Only.
30:5	0h RO	Reserved.
4	0h RW	**Partition/Trunk Oscillator Clock Gate Enable (PTOCGE):** When set, this bit allows the oscillator clock to be gated at the partition/trunk level when the conditions are met. When cleared, the oscillator clock gating at the partition/trunk level is disabled.
3	0h RW	**DMI Link CLKREQ Enable (DMILCLKREQEN):** When set, this bit enables DMI to de-assert the DMI link CLKREQ. When cleared, DMI link CLKREQ is not allowed to de-assert.
2	0h RW	**DMI Backbone CLKREQ Enable (DMIBBCLKREQEN):** When set, this bit enables DMI to de-assert the Primary backbone CLKREQ. When cleared, DMI Primary backbone CLKREQ is not allowed to de-assert.
1	0h RW	**DMI Link Dynamic Clock Gate Enable (DMILCGEN):** When set, this bit enables dynamic clock gating on the DMI Link clock domain logic. When cleared, dynamic clock gating on the DMI Link clock domain is disabled.
0	0h RW	**DMI Backbone Dynamic Clock Gate Enable (DMIBCGEN):** When set, this bit enables dynamic clock gating on the DMI backbone domain logic. When cleared, dynamic clock gating on the DMI backbone clock domain is disabled.

34.1.16 IOSF Primary Control And Status (IPCS_IOSFSBCS)—Offset 223Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	Reserved.
14:12	0h RW	**IOSF Primary ISM Idle Counter (PRIC):** BIOS may need to program this register field.
11:0	0h RO	Reserved.

34.1.17 DMI Port Link Control (DMILINKC)—Offset 2304h

BIOS may need to program this register.

34.1.18 DMI PLL Shutdown (DMIPLLDOWN)—Offset 2320h

BIOS may need to program this register.

34.1.19 DMI Power Management Control (DMIPMCTL)—Offset 2334h

BIOS may need to program this register.

34.1.20 Target Link Speed (TLS)—Offset 2608h

Target Link Speed

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 2h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	2h RO/V	**Target Link Speed (TLS):** Specifies the Target link speed that should be used if speed change is supported. Bit | Description 0000 | SPEED0: 100 Mb/s per-lane 0001 | SPEED1: 1 Gb/s per-lane 0010 | SPEED2: 2 Gb/s per-lane 0011 | SPEED3: 4 GT/s per-lane 0100-1111 | Reserved Note: The default value of bit[1:0] is defined by soft strap. This field is Read-only (RO) in with TLS value defined by soft-strap.

34.1.21 Link Configuration (LCFG)—Offset 2618h

Link Configuration

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	Reserved.
25	0h RW/L	**Secure Register Lock (SRL):** When set, the secured register will be locked.
24:0	0h RO	Reserved.

34.1.22 eSPI Generic I/O Range 1 (LPCLGIR1)—Offset 2730h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW/L	**Address[7:2] Mask (ADDRMASK):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
17:16	0h RO	Reserved.
15:2	0h RW/L	**Address[15:2] DWord-aligned address (ADDR):** Address[15:2]: DWord-aligned address. PCH does not provide decode down to the word or byte level. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
1	0h RW/L	**ISH Decode Enable (ISHDE):** When this bit is set to '1', then the range specified in this register is enabled for decoding to ISH. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
0	0h RW/L	Reserved.

34.1.23 eSPI Generic I/O Range 2 (LPCLGIR2)—Offset 2734h

Same description as LPCLGIR1 register.

34.1.24 eSPI Generic I/O Range 3 (LPCLGIR3)—Offset 2738h

Same description as LPCLGIR1 register.

34.1.25 eSPI Generic I/O Range 4 (LPCLGIR4)—Offset 273Ch

Same description as LPCLGIR1 register.

34.1.26 eSPI Generic Memory Range (LPCGMR)—Offset 2740h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/L	**Memory Address (MEMADDR):** This field specifies a 64KB memory block anywhere in the 4GB memory space that will be decoded to eSPI as standard eSPI Memory Cycle if enabled. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
15:1	0h RO	Reserved.
0	0h RW/L	Reserved.

34.1.27 eSPI BIOS Decode Enable (LPCBDE)—Offset 2744h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: FFCFh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15	1h RO	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS range: Data space: FFF80000h – FFFFFFFFh Feature space: FFB80000h – FFBFFFFFh Register Attribute: Static.
14	1h RW/L	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS range: Data space: FFF00000h – FFF7FFFFh Feature space: FFB00000h – FFB7FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.

Bit Range	Default & Access	Field Name (ID): Description
13	1h RW/L	**E8-EF Enable (EE8):** Enables decoding of 512K of the following BIOS range: Data space: FFE80000h – FFEFFFFFh Feature space: FFA80000h – FFAFFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
12	1h RW/L	**E0-E8 Enable (EE0):** Enables decoding of 512K of the following BIOS range: Data space: FFE00000h – FFE7FFFFh Feature Space: FFA00000h – FFA7FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
11	1h RW/L	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS range: Data space: FFD80000h – FFDFFFFFh Feature space: FF980000h – FF9FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
10	1h RW/L	**D0-D7 Enable (ED0):** Enables decoding of 512K of the following BIOS range: Data space: FFD00000h – FFD7FFFFh Feature space: FF900000h – FF97FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
9	1h RW/L	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS range: Data space: FFC80000h – FFCFFFFFh Feature space: FF880000h – FF8FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
8	1h RW/L	**C0-C7 Enable (EC0):** Enables decoding of 512K of the following BIOS range: Data space: FFC00000h – FFC7FFFFh Feature space: FF800000h – FF87FFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
7	1h RW/L	**Legacy F Segment Enable (LFE):** This enables the decoding of the legacy 64KB range at F0000h – FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
6	1h RW/L	**Legacy E Segment Enable (LEE):** This enables the decoding of the legacy 64KB range at E0000h – EFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
5:4	0h RO	Reserved.
3	1h RW/L	**70-7F Enable (E70):** Enables decoding of 1MB of the following BIOS range: Data space: FF700000h – FF7FFFFFh Feature space: FF300000h – FF3FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
2	1h RW/L	**60-6F Enable (E60):** Enables decoding of 1MB of the following BIOS range: Data space: FF600000h – FF6FFFFFh Feature Space: FF200000h – FF2FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
1	1h RW/L	**50-5F Enable (E50):** Enables decoding of 1MB of the following BIOS range: Data space: FF500000h – FF5FFFFFh Feature Space: FF100000h – FF1FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
0	1h RW/L	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS range: Data space: FF400000h – FF4FFFFFh Feature space: FF000000h – FF0FFFFFh This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.

34.1.28 General Control and Status (GCS)—Offset 274Ch

General Control and Status

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/L	**RPR Destination ID (RPRDID):** This field specifies the PCIe port Destination ID that is the target of the I/O ranges specified in the RPR field. Only one PCIe root port at a time can be enabled for Port 8xh support. This field is only valid when GCS.RPR field is set. BIOS must program the bits which are not used to zeros. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static. This register is Read-Only if DMIC.SRL field is set
15:12	0h RO	Reserved.
11	0h RW/L	**Reserved Page Route (RPR):** Determines where to send the reserved page registers. These addresses are sent to PCIe Root Port or eSPI for the purpose of generating POST codes. The I/O addresses modified by this field are: 80h - 8Fh.When cleared, DMI will not perform source decode on the I/O ranges specified above. The cycles hitting these ranges will end up in P2SB which will then forward the cycle to eSPI through IOSF Sideband. When set, access to the I/O ranges specified above will be forwarded to PCIe Root Port with the destination ID specified in GCS.RPRDID using DMI source decode.The aliases for these registers, at 90h, 94h, 95h, 96h, 98h, 9Ch, 9Dh, and 9Eh, are never source decoded by DMI. This register is Read-Only if the DMIC.SRL field is set. Register Attribute: Static.
10	0h RW/V/L	**Boot BIOS Strap (BBS):** This field determines the destination of accesses to the BIOS memory range. 0 = SPI 1 = eSPI When SPI or eSPI is selected, the range that is decoded is further qualified by other configuration bits described in the respective sections.The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down (bit 0) and DMIC.SRL are not set. Register Attribute: Static.
9:1	0h RO	Reserved.
0	0h RW/O	**BIOS Interface Lock-Down (BILD):** When set, prevents GCS.BBS from being changed. This bit can only be written from 0 to 1 once. Register Attribute: Static.

34.1.29 I/O Trap Register 1 - Lower DW (IOT1_LOW)—Offset 2750h

I/O Trap Register 1 Low

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address[7:2] Mask (ADDRMASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address[15:2] DWord-aligned address (ADDR):** DWord-aligned address.
1	0h RO	Reserved.
0	0h RW	**Trap and SMI# Enable (TNSMIEN):** When this bit is set to 1, then the trapping logic specified in this register is enabled.

34.1.30 I/O Trap Register 1 - Upper DW (IOT1_HIGH)—Offset 2754h

I/O Trap Register 1 High

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Read/Write Mask (RWMASK):** When this bit is 1, the trapping logic will operate on both read and write cycles. When this bit is 0, the cycle must match the type specified in bit 16.
16	0h RW	**Read/Write# (RW):** 1 = Read 0 = Write The value in this field does not matter if bit 17 is set.
15:8	0h RO	Reserved.
7:4	0h RW	**Byte Enable Mask (BEMASK):** A 1 in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enable (BE):** Active-high, DWord-aligned byte enables.

34.1.31 eSPI I/O Decode Range (LPCIOD)—Offset 2770h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	Reserved.
12	0h RW/L	**FDD Range (FDD):** The following table describes which range to decode for the FDD Port. Bits | Decode Range 0 | 3F0h 3F5h, 3F7h | (Primary) 1 | 370h 375h, 377h (Secondary) This register is Read-Only if DMIC.SRL field is set
11:10	0h RO	Reserved.
9:8	0h RW/L	**LPT Range (LPT):** The following table describes which range to decode for the LPT Port. Bits | Decode Range 00 | 378h 37Fh and 778h 77Fh 01 | 278h 27Fh (port 279h is read only) and 678h 67Fh 10 | 3BCh 3BEh and 7BCh 7BEh 11 | Reserved. This register is Read-Only if DMIC.SRL field is set
7	0h RO	Reserved.
6:4	0h RW/L	**ComB Range (CB):** The following table describes which range to decode for the COMB Port. Bits | Decode Range 000 | 3F8h 3FFh (COM1) 001 | 2F8h 2FFh (COM2) 010 | 220h 227h 011 | 228h 22Fh 100 | 238h 23Fh 101 | 2E8h 2EFh | (COM 4) 110 | 338h 33Fh 111 | 3E8h 3EFh (COM 3) This register is Read-Only if DMIC.SRL field is set
3	0h RO	Reserved.
2:0	0h RW/L	**ComA Range (CA):** The following table describes which range to decode for the COMA Port. Bits | Decode Range 000 | 3F8h 3FFh (COM1) 001 | 2F8h 2FFh (COM2) 010 | 220h 227h 011 | 228h 22Fh 100 | 238h 23Fh 101 | 2E8h 2EFh (COM 4) 110 | 338h 33Fh 111 | 3E8h 3EFh (COM 3) This register is Read-Only if DMIC.SRL field is set

34.1.32 eSPI I/O Enable (LPCIOE)—Offset 2774h

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	Reserved.
9	0h RW/L	**High Gameport Enable (HGE):** Enables decoding of the I/O locations 208h to 20Fh to eSPI. This register is Read-Only if the DMIC.SRL field is set.
8	0h RW/L	**Low Gameport Enable (LGE):** Enables decoding of the I/O locations 200h to 207h to eSPI.This register is Read-Only if the DMIC.SRL field is set.
7:4	0h RO	Reserved.
3	0h RW/L	**Floppy Drive Enable (FDE):** Enables decoding of the FDD range to eSPI. Range is selected by LIOD.FDE. This register is Read-Only if the DMIC.SRL field is set.
2	0h RW/L	**Parallel Port Enable (PPE):** Enables decoding of the LPT range to eSPI. Range is selected by LIOD.LPT. This register is Read-Only if the DMIC.SRL field is set.
1	0h RW/L	**Com Port B Enable (CBE):** Enables decoding of the COMB range to eSPI. Range is selected by LIOD.CB. This register is Read-Only if the DMIC.SRL field is set.
0	0h RW/L	**Com Port A Enable (CAE):** Enables decoding of the COMA range to eSPI. Range is selected by LIOD.CA. This register is Read-Only if the DMIC.SRL field is set.

34.1.33 TCO Base Address (TCOBASE)—Offset 2778h

TCO Base Address

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	Reserved.
15:5	0h RW/L	**TCO Base Address (TCOBA):** Provides the 32 bytes of I/O space for TCO logic, that can be map anywhere in the 64k I/O space on 32-byte boundaries. This register is Read-Only if the DMIC.SRL field is set.

Bit Range	Default & Access	Field Name (ID): Description
4:2	0h RO	Reserved.
1	0h RW/L	**TCO Enable (TCOEN):** When set, decode of the I/O range specified by the TCO base address. This register is Read-Only if the DMIC.SRL field is set.
0	0h RO	Reserved.

34.1.34 PM Base Address (PMBASEA)—Offset 27ACh

PM Base Address

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW/L	**PM Base Address Memory Range Limit (PMBAMRL):** This field specifies limit address bits[31:16] for the PM Base Address memory range. Bits [15:0] are assumed to be FFFFh. This register is Read-Only if the DMIC.SRL field is set.
15:0	0h RW/L	**PM Base Address Memory Range Base (PMBAMRB):** This field specifies base address bits[31:16] for the PM Base Address memory range. Bits [15:0] are assumed to be 0000h. This register is Read-Only if the DMIC.SRL field is set.

34.1.35 PM Base Control (PMBASEC)—Offset 27B0h

PM Base Control

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**PM Base Address Memory Range Decode Enable (PMBAMRDE):** When enabled, memory cycles that falls within the PMBASEADDR.PMBAMRB and PMBASEADDR.PMBAMRL range inclusive will be forwarded using source decode to the destination ID specified in PMBASEC.PMBDID field. This register is Read-Only if the DMIC.SRL field is set.
30:0	0h RW/L	**PM Base Destination ID (PMBDID):** The destination ID to be used to forward the cycle decoded to hit the PM Base Address range. BIOS must program the bits which are not used to zeros. Hardware will ignore the unused bits. This register is Read-Only if the DMIC.SRL field is set.

34.1.36 ACPI Base Address (ACPIBA)—Offset 27B4h

ACPI Base Address

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW/L	**Address[7:2] Mask (ADDR72MASK):** A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size. This register is Read-Only if the DMIC.SRL field is set.
17:16	0h RO	Reserved.
15:2	0h RW/L	**Address[15:2] DWord-aligned address (ADDR):** DWord-aligned address. Note that PCH does not provide decode down to the word or byte level. This register is Read-Only if the DMIC.SRL field is set.
1	0h RO	Reserved.
0	0h RW/L	**ACPI I/O Base Address Decode Enable (ACPIBADE):** When this bit is set to 1, then the range specified in this register is enabled for decoding to the destination ID specified in ACPIBDID register. This register is Read-Only if the DMIC.SRL field is set.

34.1.37 ACPI Base Destination ID (ACPIBDID)—Offset 27B8h

ACPI Base Destination ID

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/L	**ACPI Base Destination ID (ACPIBDID):** The destination ID to be used to forward the cycle decoded to hit the ACPI Base Address range. BIOS must program the bits which are not used to zeros. Hardware will ignore the unused bits. This register is Read-Only if the DMIC.SRL field is set.

35 IO Strap

35.1 IO Trap Registers Summary

These registers are within the PCH Private Configuration Space which is accessible through the PCH Sideband Interface. They can be accessed via (SBREG_BAR + PortID + Register Offset).

Table 35-1. Summary of IO Trap Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
1D00h	1D03h	PSTH Control Register (PSTHCTL)—Offset 1D00h	0h
1E00h	1E03h	Trap Status Register (TRPSTS)—Offset 1E00h	0h
1E10h	1E13h	Trapped Cycle Register (TRPCYC1)—Offset 1E10h	0h
1E18h	1E1Bh	Trapped Write Data Register (TRPWRDATA1)—Offset 1E18h	0h
1E80h	1E83h	I/O Trap Registers 1 (IOTRP1_1)—Offset 1E80h	0h
1E84h	1E87h	I/O Trap Registers 1 (IOTRP1_2)—Offset 1E84h	0h
1E88h	1E8Bh	I/O Trap Registers 2 (IOTRP2_1)—Offset 1E88h	0h
1E8Ch	1E8Fh	I/O Trap Registers 2 (IOTRP2_2)—Offset 1E8Ch	0h
1E90h	1E93h	I/O Trap Registers 3 (IOTRP3_1)—Offset 1E90h	0h
1E94h	1E97h	I/O Trap Registers 3 (IOTRP3_2)—Offset 1E94h	0h
1E98h	1E9Bh	I/O Trap Registers 4 (IOTRP4_1)—Offset 1E98h	0h
1E9Ch	1E9Fh	I/O Trap Registers 4 (IOTRP4_2)—Offset 1E9Ch	0h

35.1.1 PSTH Control Register (PSTHCTL)—Offset 1D00h

PSTH control register

Access Method

Type: MSG Register (Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:3	0h RO	Reserved.

Bit Range	Default and Access	Field Name (ID): Description
2	0h RW	**PSTH IOSF Primary Trunk Clock Gating Enable (PSTHIOSFPTCGE):** 0 = Disable 1 = Enable
1	0h RW	**PSTH IOSF Sideband Trunk Clock Gating Enable (PSTHIOSFSTCGE):** 0 = Disable 1 = Enable
0	0h RW	**PSTH Dynamic Clock Gating Enable (PSTHDCGE):** 0 = Disable 1 = Enable

35.1.2 Trap Status Register (TRPSTS)—Offset 1E00h

Trap status register

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:4	0h RO	Reserved.
3:0	0h RW/1C/V	**Cycle Trap SMI# Status (SMISTAT):** These bits are set by hardware when the corresponding Cycle Trap register is enabled and a matching cycle is received (and trapped). These bits are OR'ed together to create a single status bit in the Power Management register space.Note that the SMI# and trapping must be enabled in order to set these bits. This is because, in order to do the cycle comparison, packets must be delayed by several clocks from the DMI pins to the internal receiver. This delay is only enabled when at least one of the trap ranges is enabled. These bits are set before the completion is generated for the trapped cycle, thereby guaranteeing that the processor can enter the SMI# handler when the instruction completes. Each status bit is cleared by writing a '1' to the corresponding bit location in this register.

35.1.3 Trapped Cycle Register (TRPCYC1)—Offset 1E10h

This register saves information about the I/O Cycle that was trapped and generated the SMI# for software to read.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:25	0h RO	Reserved.
24	0h RO/V	**Read-Write (TRPRWR):** 1 = Read, 0 = Write
23:20	0h RO	Reserved.
19:16	0h RO/V	**Active-High Byte Enables (TRPBE):** This is the DWord-aligned byte enables associated with the trapped cycle. A 1 in any bit location indicates that the corresponding byte is enabled in the cycle.
15:2	0h RO/V	**IO Address (TRPADDR):** This is the DWord-aligned address of the trapped cycle.
1:0	0h RO	Reserved.

35.1.4 Trapped Write Data Register (TRPWRDATA1)—Offset 1E18h

This register saves the data from I/O write cycles that are trapped for software to read

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:0	0h RO/V	**Data (TRPDATA):** DWord of I/O write data. This field is undefined after trapping a read cycle.

35.1.5 I/O Trap Registers 1 (IOTRP1_1)—Offset 1E80h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address Mask (TRP1ADDRM):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address (TRP1ADDR):** DWord-aligned address
1	0h RO	Reserved.
0	0h RW	**Trap and SMI Enable (TRP1EN):** When this bit is set to 1, then the trapping logic specified in this register is enabled.

35.1.6 I/O Trap Registers 1 (IOTRP1_2)—Offset 1E84h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Read-Write Mask (TRP1RWM):** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0h RW	**Read/Write (TRP1RW):** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	0h RO	Reserved.
7:4	0h RW	**Byte Enable Mask (TRP1BEM):** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enables (TRP1BE):** Active-high, DWord-aligned byte enables

35.1.7 I/O Trap Registers 2 (IOTRP2_1)—Offset 1E88h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address Mask (TRP2ADDRM):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address (TRP2ADDR):** DWord-aligned address
1	0h RO	Reserved.
0	0h RW	**Trap and SMI Enable (TRP2EN):** When this bit is set to 1, then the trapping logic specified in this register is enabled.

35.1.8 I/O Trap Registers 2 (IOTRP2_2)—Offset 1E8Ch

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Read-Write Mask (TRP2RWM):** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0h RW	**Read/Write (TRP2RW):** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.

Bit Range	Default and Access	Field Name (ID): Description
15:8	0h RO	Reserved.
7:4	0h RW	**Byte Enable Mask (TRP2BEM):** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enables (TRP2BE):** Active-high, DWord-aligned byte enables

35.1.9 I/O Trap Registers 3 (IOTRP3_1)—Offset 1E90h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address Mask (TRP3ADDRM):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Address (TRP3ADDR):** DWord-aligned address
1	0h RO	Reserved.
0	0h RW	**Trap and SMI Enable (TRP3EN):** When this bit is set to 1, then the trapping logic specified in this register is enabled.

35.1.10 I/O Trap Registers 3 (IOTRP3_2)—Offset 1E94h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Read-Write Mask (TRP3RWM):** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0h RW	**Read/Write (TRP3RW):** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	0h RO	Reserved.
7:4	0h RW	**Byte Enable Mask (TRP3BEM):** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enables (TRP3BE):** Active-high, DWord-aligned byte enables

35.1.11 I/O Trap Registers 4 (IOTRP4_1)—Offset 1E98h

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:24	0h RO	Reserved.
23:18	0h RW	**Address Mask (TRP4ADDRM):** A '1' in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	0h RO	Reserved.
15:2	0h RW	**Reserved (TRP4ADDR):** DWord-aligned address
1	0h RO	Reserved.
0	0h RW	**Trap and SMI Enable (TRP4EN):** When this bit is set to 1, then the trapping logic specified in this register is enabled.

35.1.12 I/O Trap Registers 4 (IOTRP4_2)—Offset 1E9Ch

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default and Access	Field Name (ID): Description
31:18	0h RO	Reserved.
17	0h RW	**Read-Write Mask (TRP4RWM):** When this bit is '1', the trapping logic will operate on both read and write cycles. When this bit is '0', the cycle must match the type specified in bit 48.
16	0h RW	**Read/Write (TRP4RW):** 1 = Read, 0 = Write, the value in this field does not matter if bit 49 is set.
15:8	0h RO	Reserved.
7:4	0h RW	**Byte Enable Mask (TRP4BEM):** A '1' in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
3:0	0h RW	**Byte Enables (TRP4BE):** Active-high, DWord-aligned byte enables

36 PSF Registers

36.1 PSF1 Registers Summary

Table 36-1. Summary of PSF1 Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
19Ch	19Fh	D22:F0 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F0_OFFSET3)—Offset 19Ch	0h
21Ch	21Fh	D22:F1 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F1_OFFSET4)—Offset 21Ch	0h
29Ch	29Fh	D22:F4 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F4_OFFSET5)—Offset 29Ch	0h
31Ch	31Fh	D22:F5 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F5_OFFSET6)—Offset 31Ch	0h
61Ch	61Fh	D22:F2 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_PTIO_RS0_D22_F2_OFFSET12)—Offset 61Ch	0h
69Ch	69Fh	D22:F3 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_PTIO_RS0_D22_F3_OFFSET13)—Offset 69Ch	0h
79Ch	79Fh	D31:F7 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_NPK_RS0_D31_F7_OFFSET15)—Offset 79Ch	0h
81Ch	81Fh	D22:F0 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_XHCI_RS0_D20_F0_OFFSET16)—Offset 81Ch	0h
D9Ch	D9Fh	D31:F6 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_GBE_RS0_D31_F6_OFFSET27)—Offset D9Ch	0h
F1Ch	F1Fh	D31:F7 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_NPK_RS0_D31_F7_OFFSET30)—Offset F1Ch	0h
F9Ch	F9Fh	D20:F0 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_XHCI_RS0_D20_F0_OFFSET31)—Offset F9Ch	0h
109Ch	109Fh	D23:F0 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_VR_RS0_D23_F0_OFFSET33)—Offset 109Ch	0h
151Ch	151Fh	D23:F0 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_VR_RS0_D23_F0_OFFSET42)—Offset 151Ch	0h

36.1.1 D22:F0 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F0_OFFSET3)—Offset 19Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.1.2 D22:F1 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F1_OFFSET4)—Offset 21Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.1.3 D22:F4 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F4_OFFSET5)—Offset 29Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.1.4 D22:F5 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_CSE_RS0_D22_F5_OFFSET6)—Offset 31Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.1.5 D22:F2 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_PTIO_RS0_D22_F2_OFFSET12)—Offset 61Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.1.6 D22:F3 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_PTIO_RS0_D22_F3_OFFSET13)—Offset 69Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.1.7 D31:F7 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_NPK_RS0_D31_F7_OFFSET15)—Offset 79Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.1.8 D22:F0 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_XHCI_RS0_D20_F0_OFFSET16)—Offset 81Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.1.9 D31:F6 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_GBE_RS0_D31_F6_OFFSET27)—Offset D9Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.1.10 D31:F7 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_NPK_RS0_D31_F7_OFFSET30)—Offset F1Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.1.11 D20:F0 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_XHCI_RS0_D20_F0_OFFSET31)—Offset F9Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.1.12 D23:F0 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_VR_RS0_D23_F0_OFFSET33)—Offset 109Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.1.13 D23:F0 PCI Configuration Space Disable (PSF_1_AGNT_T0_SHDW_PCIEN_VR_RS0_D23_F0_OFFSET42)—Offset 151Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.2 PSF2 Registers Summary

Table 36-2. Summary of PSF2 Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
19Ch	19Fh	D16:F6 PCI Configuration Space Disable (PSF_2_AGNT_T0_SHDW_PCIEN_THC0_RS0_D16_F6_OFFSET3)—Offset 19Ch	0h
21Ch	21Fh	D16:F7 PCI Configuration Space Disable (PSF_2_AGNT_T0_SHDW_PCIEN_THC1_RS0_D16_F7_OFFSET4)—Offset 21Ch	0h
41Ch	41Fh	D20:F1 PCI Configuration Space Disable (PSF_2_AGNT_T0_SHDW_PCIEN_XDCI_RS0_D20_F1_OFFSET8)—Offset 41Ch	0h

36.2.1 D16:F6 PCI Configuration Space Disable (PSF_2_AGNT_T0_SHDW_PCIEN_THC0_RS0_D16_F6_OFFSET3)—Offset 19Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.2.2 D16:F7 PCI Configuration Space Disable (PSF_2_AGNT_T0_SHDW_PCIEN_THC1_RS0_D16_F7_OFFSET4)—Offset 21Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.2.3 D20:F1 PCI Configuration Space Disable (PSF_2_AGNT_T0_SHDW_PCIEN_XDCI_RS0_D20_F1_OFFSET8)—Offset 41Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3 PSF3 Registers Summary

Table 36-3. Summary of PSF3 Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
11Ch	11Fh	D31:F6 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_GBE_RS0_D31_F6_OFFSET2)—Offset 11Ch	0h
21Ch	21Fh	D18:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_ISH_RS0_D18_F0_OFFSET4)—Offset 21Ch	0h
21Ch	21Fh	D16:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_BTCORE_RS0_D16_F2_OFFSET4)—Offset 21Ch	0h
31Ch	31Fh	D18:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_ISH_RS0_D18_F0_OFFSET6)—Offset 31Ch	0h
39Ch	39Fh	D31:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPC_RS0_D31_F0_OFFSET7)—Offset 39Ch	0h
41Ch	41Fh	D21:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F0_OFFSET8)—Offset 41Ch	0h
49Ch	49Fh	D21:F1 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F1_OFFSET9)—Offset 49Ch	0h
51Ch	51Fh	D21:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F2_OFFSET10)—Offset 51Ch	0h
51Ch	51Fh	D21:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F0_OFFSET10)—Offset 51Ch	0h
59Ch	59Fh	D21:F1 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F1_OFFSET11)—Offset 59Ch	0h

Table 36-3. Summary of PSF3 Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
59Ch	59Fh	D21:F3 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F3_OFFSET11)—Offset 59Ch	0h
61Ch	61Fh	D25:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F0_OFFSET12)—Offset 61Ch	0h
61Ch	61Fh	D21:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F2_OFFSET12)—Offset 61Ch	0h
69Ch	69Fh	D25:F1 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F1_OFFSET13)—Offset 69Ch	0h
69Ch	69Fh	D21:F3 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F3_OFFSET13)—Offset 69Ch	0h
71Ch	71Fh	D25:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F0_OFFSET14)—Offset 71Ch	0h
79Ch	79Fh	D25:F1 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F1_OFFSET15)—Offset 79Ch	0h
81Ch	81Fh	D30:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F2_OFFSET16)—Offset 81Ch	0h
89Ch	89Fh	D30:F3 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F3_OFFSET17)—Offset 89Ch	0h
91Ch	91Fh	D18:F6 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D18_F6_OFFSET18)—Offset 91Ch	0h
91Ch	91Fh	D30:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F2_OFFSET18)—Offset 91Ch	0h
99Ch	99Fh	D19:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D19_F0_OFFSET19)—Offset 99Ch	0h
99Ch	99Fh	D30:F3 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F3_OFFSET19)—Offset 99Ch	0h
A1Ch	A1Fh	D18:F6 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D18_F6_OFFSET20)—Offset A1Ch	0h
A9Ch	A9Fh	D19:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D19_F0_OFFSET21)—Offset A9Ch	0h
B9Ch	B9Fh	D30:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F0_OFFSET23)—Offset B9Ch	0h
C1Ch	C1Fh	D30:F1 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F1_OFFSET24)—Offset C1Ch	0h
C9Ch	C9Fh	D25:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F2_OFFSET25)—Offset C9Ch	0h

Table 36-3. Summary of PSF3 Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
C9Ch	C9Fh	D30:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F0_OFFSET25)—Offset C9Ch	0h
D1Ch	D1Fh	D17:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D17_F0_OFFSET26)—Offset D1Ch	0h
D1Ch	D1Fh	D30:F1 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F1_OFFSET26)—Offset D1Ch	0h
D9Ch	D9Fh	D25:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F2_OFFSET27)—Offset D9Ch	0h
E1Ch	E1Fh	D17:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D17_F0_OFFSET28)—Offset E1Ch	0h
F9Ch	F9Fh	D31:F1 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_P2S_RS0_D31_F1_OFFSET31)—Offset F9Ch	0h
F9Ch	F9Fh	D17:F3 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D17_F3_OFFSET31)—Offset F9Ch	0h
101Ch	101Fh	D31:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_PMC_RS0_D31_F2_OFFSET32)—Offset 101Ch	0h
109Ch	109Fh	D20:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_PMC_RS0_D20_F2_OFFSET33)—Offset 109Ch	0h
109Ch	109Fh	D31:F1 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_P2S_RS0_D31_F1_OFFSET33)—Offset 109Ch	0h
111Ch	111Fh	D31:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_PMC_RS0_D31_F2_OFFSET34)—Offset 111Ch	0h
119Ch	119Fh	D31:F4 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_SMB_RS0_D31_F4_OFFSET35)—Offset 119Ch	0h
119Ch	119Fh	D20:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_PMC_RS0_D20_F2_OFFSET35)—Offset 119Ch	0h
121Ch	121Fh	D31:F5 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_SPI_RS0_D31_F5_OFFSET36)—Offset 121Ch	0h
129Ch	129Fh	D31:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_SPI_RS0_D31_F0_OFFSET37)—Offset 129Ch	0h
129Ch	129Fh	D31:F4 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_SMB_RS0_D31_F4_OFFSET37)—Offset 129Ch	0h

Table 36-3. Summary of PSF3 Registers

Offset Start	Offset End	Register Name (ID)—Offset	Default Value
131Ch	131Fh	D31:F5 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_SPI_RS0_D31_F5_OFFSET38)—Offset 131Ch	0h
139Ch	139Fh	D31:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_SPI_RS0_D31_F0_OFFSET39)—Offset 139Ch	0h
151Ch	151Fh	D20:F3 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_WIFI_RS0_D20_F3_OFFSET42)—Offset 151Ch	0h

36.3.1 D31:F6 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_GBE_RS0_D31_F6_OFFSET2)—Offset 11Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.2 D18:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_ISH_RS0_D18_F0_OFFSET4)—Offset 21Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.3 D16:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_BTCORE_RS0_D16_F2_OFFSET4)—Offset 21Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.4 D18:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_ISH_RS0_D18_F0_OFFSET6)—Offset 31Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.5 D31:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPC_RS0_D31_F0_OFFSET7)—Offset 39Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.6 D21:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F0_OFFSET8)—Offset 41Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.7 D21:F1 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F1_OFFSET9)—Offset 49Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.8 D21:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F2_OFFSET10)—Offset 51Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.9 D21:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F0_OFFSET10)—Offset 51Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.10 D21:F1 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F1_OFFSET11)—Offset 59Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.11 D21:F3 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F3_OFFSET11)—Offset 59Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.12 D25:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F0_OFFSET12)—Offset 61Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.13 D21:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F2_OFFSET12)—Offset 61Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.14 D25:F1 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F1_OFFSET13)—Offset 69Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.15 D21:F3 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D21_F3_OFFSET13)—Offset 69Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.16 D25:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F0_OFFSET14)—Offset 71Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.17 D25:F1 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F1_OFFSET15)—Offset 79Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.18 D30:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F2_OFFSET16)—Offset 81Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.19 D30:F3 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F3_OFFSET17)—Offset 89Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.20 D18:F6 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D18_F6_OFFSET18)—Offset 91Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.21 D30:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F2_OFFSET18)—Offset 91Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.22 D19:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D19_F0_OFFSET19)—Offset 99Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.23 D30:F3 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F3_OFFSET19)—Offset 99Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.24 D18:F6 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D18_F6_OFFSET20)—Offset A1Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.25 D19:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D19_F0_OFFSET21)—Offset A9Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.26 D30:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F0_OFFSET23)—Offset B9Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.27 D30:F1 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F1_OFFSET24)—Offset C1Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.28 D25:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F2_OFFSET25)—Offset C9Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.29 D30:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F0_OFFSET25)—Offset C9Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.30 D17:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D17_F0_OFFSET26)—Offset D1Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.31 D30:F1 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D30_F1_OFFSET26)—Offset D1Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.32 D25:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D25_F2_OFFSET27)—Offset D9Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.33 D17:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D17_F0_OFFSET28)—Offset E1Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.34 D31:F1 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_P2S_RS0_D31_F1_OFFSET31)—Offset F9Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.35 D17:F3 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_LPSS_RS0_D17_F3_OFFSET31)—Offset F9Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.36 D31:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_PMC_RS0_D31_F2_OFFSET32)—Offset 101Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.37 D20:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_PMC_RS0_D20_F2_OFFSET33)—Offset 109Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.38 D31:F1 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_P2S_RS0_D31_F1_OFFSET33)—Offset 109Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.39 D31:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_PMC_RS0_D31_F2_OFFSET34)—Offset 111Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.40 D31:F4 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_SMB_RS0_D31_F4_OFFSET35)—Offset 119Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.41 D20:F2 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_PMC_RS0_D20_F2_OFFSET35)—Offset 119Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.42 D31:F5 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_SPI_RS0_D31_F5_OFFSET36)—Offset 121Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.43 D31:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_SPI_RS0_D31_F0_OFFSET37)—Offset 129Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	Reserved.
-1:0	0h	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.

36.3.44 D31:F4 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_SMB_RS0_D31_F4_OFFSET37)—Offset 129Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.45 D31:F5 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_SPI_RS0_D31_F5_OFFSET38)—Offset 131Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.46 D31:F0 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_SPI_RS0_D31_F0_OFFSET39)—Offset 139Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.

36.3.47 D20:F3 PCI Configuration Space Disable (PSF_3_AGNT_T0_SHDW_PCIEN_WIFI_RS0_D20_F3_OFFSET42)—Offset 151Ch

Access Method

Type: MSG Register
(Size: 32 bits)

Device:
Function:

Default: 0h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	Reserved.
8	0h RW	**Function Disable. (FUNDIS):** Default value=0x0, When set, transactions targeting this PCI function will not be positively decoded, and cfgWr transactions to this function will not be shadowed. This bit is writable through SB interface only.
7:0	0h RO	Reserved.