11th Generation Intel® Core™ Processor

Specification Update

Supporting 11th Generation Intel® Core™ Processor, Intel® Pentium® Processor, and Intel® Celeron® Processor for UP3, UP3 IOT, UP4, H35, H81, UP3-Refresh, and H35-Refresh Processor Line Platforms, formerly known as Tiger Lake

Revision 027

November 2023

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Revision History

Revision Number	Description	Revision Date
001	• Initial Revision	September 2020
002	• Added Errata: TGL016, TGL017	September 2020
003	• Added IOT UP3 Processor Line • Added Errata: TGL018, TGL019, TGL020	October 2020
004	• Added Errata: TGL021, TGL022, TGL023, TGL024, TGL025 • Updated Erratum: TGL014 • Added UP3 IOT and UP4 support	November 2020
005	• Added Errata: TGL026, TGL027, TGL028, TGL029 • Removed Erratum: TGL026 • Updated Erratum: TGL003	January 2021
006	• Added Errata: TGL030, TGL031 • Added H35 Processor Line	February 2021
007	• Added Errata: TGL032, TGL033	March 2021
008	• Added Errata: TGL034, TGL035	April 2021
009	• Added Errata: TGL036, TGL037 • Removed Erratum: TGL018	May 2021
010	• Added Erratum: TGL038 • Added H81 Processor Line	June 2021
011	• Added Processor Lines: UP3-Refresh, H35-Refresh • Added Erratum TGL018 • Updated Affected Documents table	July 2021
012	• Added Errata: TGL039, TGL040, TGL042	August 2021
013	• Added Erratum: TGL043	September 2021
014	• Added Errata: TGL044, TGL045, TGL046, TGL047	October 2021
015	• Updated Specification Changes table	December 2021
016	• Added Errata: TGL048, TGL049, TGL050, TGL051	February 2022
017	• Added Erratum: TGL052	March 2022
018	• Added Errata: TGL053, TGL054	May 2022
019	• Added Errata: TGL055, TGL056 • Updated Erratum: TGL034	June 2022
020	• Added Errata: TGL057, TGL058	July 2022
021	• Added Errata: TGL059, TGL060, TGL061	September 2022
022	• Added Erratum: TGL062	January 2023
023	• Added Erratum: TGL063	April 2023

Revision Number	Description	Revision Date
024	• Added Erratum: TGL064	May 2023
025	• Added Erratum: TGL065	July 2023
026	• Added Erratum: TGL066	August 2023
027	• Added Erratum: TGL067	November 2023

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Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata, specification clarifications and changes. The document is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this updated document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents

Document Title	Document Number
11th Generation Intel® Core™ Processor Datasheet, Volume 1 of 2	631121
11th Generation Intel® Core™ Processor Datasheet, Volume 2a of 2	631122
11th Generation Intel® Core™ Processor Datasheet, Volume 2b of 2	643524

Related Documents

Document Title	Document Number/Location
AP-485, Intel® Processor Identification and the CPUID Instruction	http://www.intel.com/design/processor/applnots/241618.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference Manual A-M Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference Manual N-Z Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B: System Programming Guide Intel® 64 and IA-32 Intel® Architecture Optimization Reference Manual	http://www.intel.com/products/processor/manuals/index.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes	http://www.intel.com/content/www/us/en/processors/architectures-software-developer-manuals.html
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	D51397-001
ACPI Specifications	www.acpi.info

Nomenclature

Errata – These are design defects or errors. Errata may cause the processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes – These are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications – This describes a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes – This includes typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update, when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

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Identification Information

Component Identification via Programming Interface

The processor stepping is identified by the following register contents:

Table 1. Processor Lines Component Identification

Processor	CPUID	Reserved [31:28]	Extended Family [27:20]	Extended Model [19:16]	Reserved [15:14]	Processor Type [13:12]	Family Code [11:8]	Model Number [7:4]	Stepping ID [3:0]
UP3/UP4/H35	000806C1h	Reserved	0000000b	1000b	Reserved	00b	0110b	1100b	0001b
H81	000806D1h	Reserved	0000000b	1000b	Reserved	00b	0110b	1101b	0001b
UP3-Refresh/ H35-Refresh	000806C2h	Reserved	0000000b	1000b	Reserved	00b	0110b	1100b	0010b

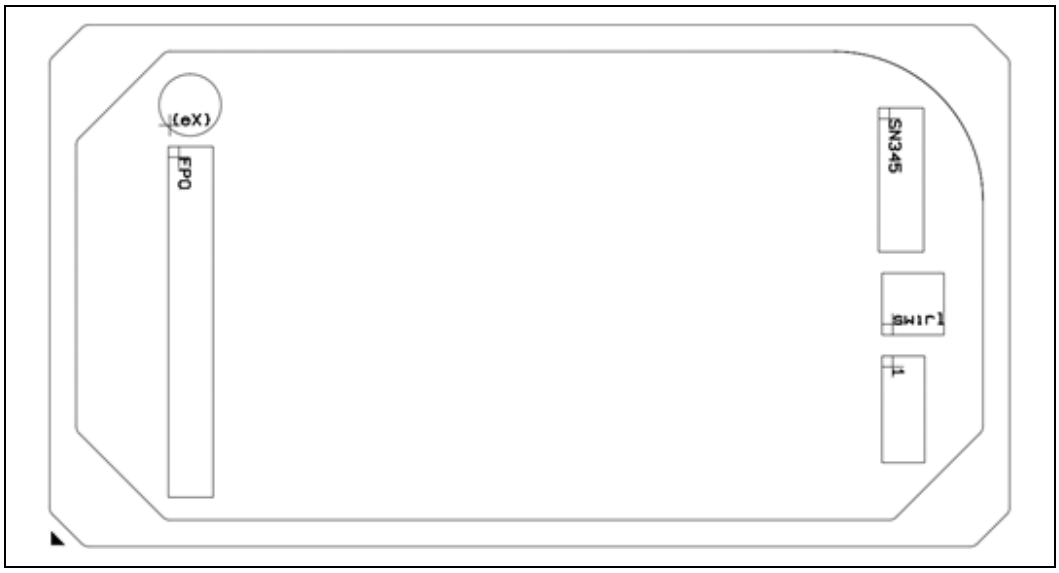
NOTES:

1. The Extended Family, Bits [27:20] are used in conjunction with the Family Code, specified in Bits[11:8], to indicate whether the processor belongs to the Celeron®, Pentium®, or Intel® Core™ processor family.
2. The Extended Model, Bits [19:16] in conjunction with the Model Number, specified in Bits [7:4], are used to identify the model of the processor within the processor's family.
3. The Family Code corresponds to Bits [11:8] of the EDX register after RESET, Bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
4. The Model Number corresponds to Bits [7:4] of the EDX register after RESET, Bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
5. The Stepping ID in Bits [3:0] indicates the revision number of that model. Refer table above for the processor stepping ID number in the CPUID information.
6. When EAX is initialized to a value of '1', the CPUID instruction returns the Extended Family, Extended Model, Processor Type, Family Code, Model Number and Stepping ID value in the EAX register. The EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX and EDX registers after the CPUID instruction is executed with a 2 in the EAX register.

Component Marking Information

Figure 1. Processor Based on UP3/H35/UP3-Refresh/H35-Refresh Processor Line Multi-Chip Package BGA Top-Side Markings



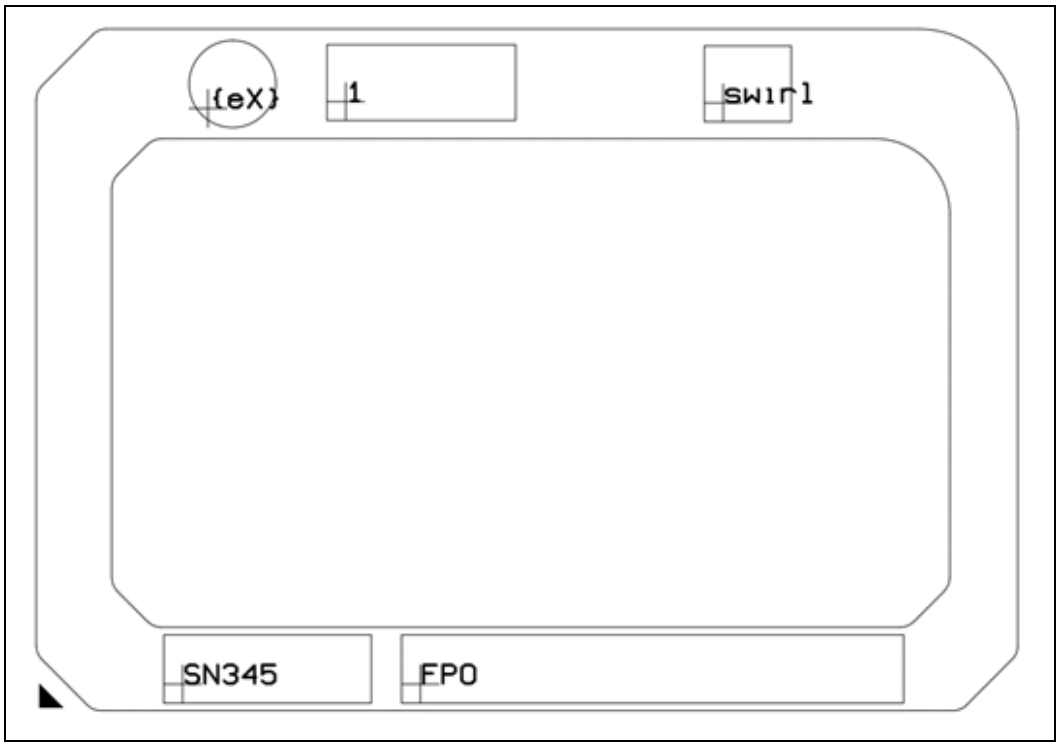
Pin Count: 1449 Package Size: 45.5 mm x 25 mm

Production (SSPEC):

- FPO: FPOxxxxx
- {eX}
- SWIR1: Intel® logo

Note: "1" is used to extract the unit visual ID (2D ID).

Figure 2. Processor Based on UP4 Processor Line Multi-Chip Package BGA Top-Side Markings



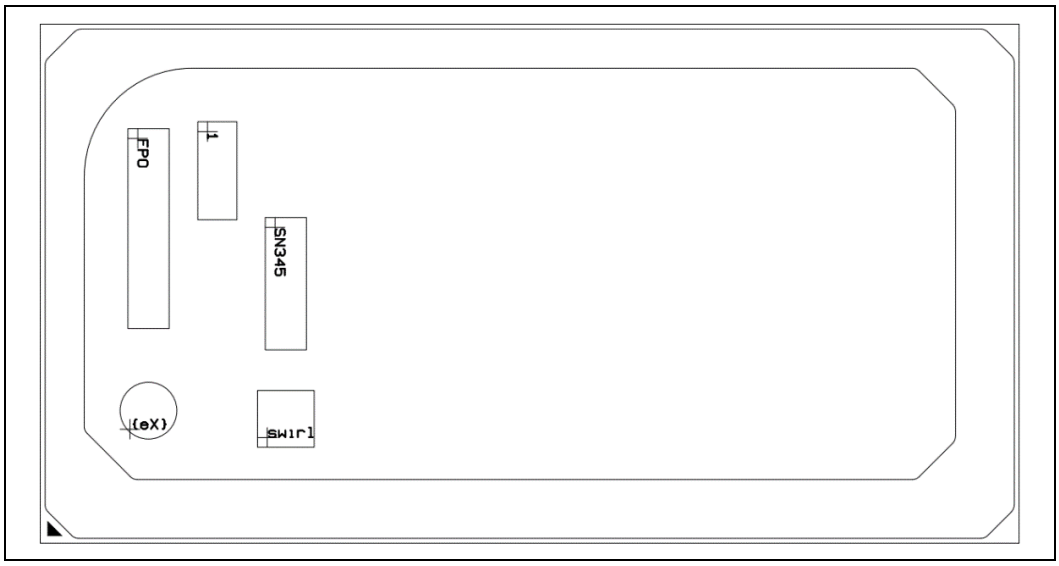
Pin Count: 1598 Package Size: 26.5 mm x 18.5 m

Production (SSPEC):

Intel logo
BRAND
PROC#
SPEC SPEED
{FPO} {eX}

Note: "1" is used to extract the unit visual ID (2D ID).

Figure 3. Processor Based on H81 Processor Line Multi-Chip Package BGA Top-Side Markings



Pin Count: 1787 Package Size (mm): Width x Height: 50 x 26.5

Production (SSPEC):

Intel logo
BRAND
PROC#
SPEC SPEED
{FPO} {eX}

Note: "1" is used to extract the unit visual ID (2D ID).

Note: Processor list can be found at:
https://ark.intel.com/content/www/us/en/ark/products/codename/88759/products-formerly-tiger-lake.html

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Summary Tables of Changes

The following tables indicate the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed processor stepping. Intel® intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. These tables use the following notations:

Codes Used in Summary Table

Stepping	Description
(No mark) or (Blank Box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status	Description
Doc	Document change or update that is implemented.
Planned Fix	This erratum may be fixed in a future stepping of the product.
Fixed	This erratum has been previously fixed in Intel® hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

Errata Summary Table

Erratum ID	Processor Line/Stepping							Title
	UP3	IOT UP3	UP4	H35	H81	UP3-Refresh	H35-Refresh	
TGL001	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	X87 FDP Value May be Saved Incorrectly In Real-Address Mode or Virtual-8086 Mode
TGL002	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Debug Exceptions May be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed by a Write to SP
TGL003	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	CPUID L2 Cache Information May be Inaccurate
TGL004	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Placing Posted-Interrupt Descriptors Within the PRMRR May Result In a Processor Hang
TGL005	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Intel® PT CBR Packet May be Delayed or Dropped

Erratum ID	Processor Line/Stepping							Title
	UP3	IOT UP3	UP4	H35	H81	UP3-Refresh	H35-Refresh	
TGL006	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Intel® PT TIP or FUP Packets May be Dropped Without OVF Packet
TGL007	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Overflow Flag in IA32_MC0_STATUS MSR May be Incorrectly Set
TGL008	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	An Exception During a 32-bit Mode Task Switch With CET Enabled May Lead to an Incorrect TSS Busy Flag Value
TGL009	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Exit Qualification For EPT Violations Incorrectly Indicate On Instruction Fetches That the Guest-Physical Address Was Writeable
TGL010	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Processor May Generate Spurious Page Faults On Shadow Stack Pages
TGL011	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	HDMI 1.4 Inter-Pair Skew Test May Fail
TGL012	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Intel® PT ToPA Tables Read From Non-Cacheable Memory During an Intel® TSX Transaction May Lead to Processor Hang
TGL013	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Performing an XACQUIRE to an Intel® PT ToPA Table May Lead to Processor Hang
TGL014	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	PECI Frequency Limited to 3.2Kbps-1Mbps
TGL015	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	PCIe Gen4 JTOL – Jitter Tolerance Compliance Test May Fail
TGL016	Fixed	Fixed	N/A	N/A	N/A	N/A	N/A	System May Fail To Exit Warm Reset or S3
TGL017	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Unable to Transmit Modified Compliance Test Pattern At 2.5 GT/S or 5.0 GT/s Link Speeds
TGL018	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	MSR IA32_THERM_STATUS CURRENT_LIMIT_STATUS May Report Incorrect Value
TGL019	Fixed	Fixed	N/A	N/A	N/A	N/A	N/A	System May Hang During Package-C10 Exit
TGL020	Fixed	Fixed	N/A	N/A	N/A	N/A	N/A	Processor May Hang When PROCHOT# is Active
TGL021	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Processor May Hang if Warm Reset Triggers During BIOS Initialization

Erratum ID	Processor Line/Stepping							Title
	UP3	IOT UP3	UP4	H35	H81	UP3-Refresh	H35-Refresh	
TGL022	Fixed	Fixed	Fixed	Fixed	N/A	N/A	N/A	PCIe Link Down May Occur After Exiting From Package C10 Cycle
TGL023	No Fix	No Fix	N/A	N/A	N/A	N/A	N/A	Reported Package Power May Not be Accurate
TGL024	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	USB TD.6.5 Polling.LFPS Duration Test Fail on Direct Port
TGL025	Fixed	Fixed	Fixed	N/A	N/A	N/A	N/A	Cache Configuration May be Incorrectly Initialized During Boot
TGL026	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A. Erratum has been removed.
TGL027	No Fix	No Fix	No Fix	N/A	N/A	N/A	N/A	Processor PCIe Reference Clock May be Unavailable if CLKREQ# is Asserted During L1.2 Entry
TGL028	Fixed	Fixed	Fixed	N/A	N/A	N/A	N/A	Processor PCIe May Hang Following PKG-C10
TGL029	N/A	N/A	N/A	N/A	No Fix	N/A	N/A	PCIe Width Change Transition May Fail
TGL030	Fixed	Fixed	N/A	Fixed	Fixed	Fixed	Fixed	DDR4 1Rx16 DIMMs Cannot Achieve Optimal Memory Configuration
TGL031	Fixed	Fixed	Fixed	Fixed	N/A	N/A	N/A	Incorrect Core Operating Voltage May Lead To Unpredictable System Behavior
TGL032	Fixed	Fixed	Fixed	Fixed	N/A	N/A	N/A	Processor May Hang on PKG C9 or Deeper Exit
TGL033	Fixed	Fixed	Fixed	Fixed	N/A	N/A	N/A	Processor May Hang on Pkg C10 Exit
TGL034	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Executing an XSAVE or VZEROALL Instruction After SYSENTER May Result in Unexpected SSE/AVX Register Values
TGL035	Fixed	Fixed	Fixed	Fixed	N/A	N/A	N/A	Processor May Fail to Resume From Package C10
TGL036	Fixed	Fixed	Fixed	Fixed	N/A	Fixed	Fixed	PkgC7 or Deeper Exits May Lead to Display Flicker
TGL037	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	VCVTPS2PH To Memory May Update MXCSR in The Case of a Fault on the Store
TGL038	Fixed	Fixed	Fixed	N/A	N/A	N/A	N/A	Memory Contents May Not be Accessible After a Warm Reset
TGL039	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Processor May Generate Malformed TLP

Erratum ID	Processor Line/Stepping							Title
	UP3	IOT UP3	UP4	H35	H81	UP3-Refresh	H35-Refresh	
TGL040	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	System May Experience an Internal Timeout Error When Directing Intel® PT to a Small, Uncacheable, Single-Range Output Buffer
TGL041	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A. Erratum has been removed.
TGL042	N/A	N/A	N/A	N/A	Fixed	N/A	N/A	Spurious FIVR OCP Event May Occur During Boot
TGL043	N/A	N/A	N/A	N/A	Fixed	N/A	N/A	Embedded Display Flicker May be Observed During Idle Scenarios
TGL044	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	False MC1 Error Reported in The Shadow of an Internal Timer Error
TGL045	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	PCIe Link May Fail to Train Upon Exit From L1.2
TGL046	N/A	N/A	N/A	N/A	Fixed	N/A	N/A	DMI Link Failure During L1 Exit
TGL047	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT Does Not Prevent The Three-strike Counter From Incrementing
TGL048	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Intel® PT TIP.PGD May Not Have Target IP Payload
TGL049	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Intel® Processor Trace PSB+ Packets May Contain Unexpected Packets
TGL050	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Intel® PT Trace May Drop Second Byte of CYC Packet
TGL051	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	VM Entry That Clears TraceEn May Generate a FUP
TGL052	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Intel® PT Trace May Contain Incorrect Data When Configured With Single Range Output Larger Than 4KB
TGL053	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	On Instructions Longer Than 15 Bytes, #GP Exception is Prioritized And Delivered Over #CP Exception
TGL054	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Mismatch on DR6 Value When Breakpoint Match is on Bitmap Address
TGL055	Fixed	Fixed	Fixed	Fixed	N/A	N/A	N/A	Unaligned CET-SS Stack Token Does Not Signal #GP

Erratum ID	Processor Line/Stepping							Title
	UP3	IOT UP3	UP4	H35	H81	UP3-Refresh	H35-Refresh	
TGL056	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	USB 3.0 Device May Not be Detected or May Down Train to USB 2.0 Speed
TGL057	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Call Instruction Wrapping Around The 32-bit Address Boundary May Return to Incorrect Address
TGL058	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
TGL059	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Incorrect MCACOD For L2 Prefetch MCE
TGL060	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Crashlog and Telemetry BAR May Not Function Correctly
TGL061	N/A	N/A	N/A	N/A	Fixed	Fixed	Fixed	LFENCE Instruction May Not Prevent FSFP Forwarding
TGL062	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	GPU Hang When Async Compute is Enabled
TGL063	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	Branch Predictor May Produce Incorrect Instruction Pointer
TGL064	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Processor May Encrypt TME Exclude Range if Mapped to Remap Range
TGL065	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	xHCI Force Header Command Incorrect Return Code
TGL066	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	USB Type-C Monitor Removal May Result In System Hang
TGL067	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	USB 3.2 DbC Sublink Speed Attribute ID (SSID) Value

Specification Changes

No.	Specification Changes
001	HDCP 2.2 not supported in certain modes for DP1.4a interface.
002	DP-in support of both LTTPR transparent and non-transparent modes.

Specification Clarifications

No.	Specification Clarifications
	None for this revision of this specification update.

Documentation Changes

No.	Documentation Changes
	None for this revision of this specification update.

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Errata Details

TGL001	X87 FDP Value May be Saved Incorrectly in Real-Address Mode or Virtual-8086 Mode
Problem	Execution of the FSAVE, FNSAVE, FSTENV, or FNSTENV instructions in real-address mode or virtual-8086 mode may save an incorrect value for the x87 FDP (FPU data pointer). This erratum does not apply if the last non-control x87 instruction had an unmasked exception.
Implication	Software operating in real-address mode or virtual-8086 mode that depends on the FDP value for non-control x87 instructions without unmasked exceptions may not operate properly. Intel® has not observed this erratum in any commercially available software.
Workaround	None identified. Software should use the FDP value saved by the listed instructions only when the most recent non-control x87 instruction incurred an unmasked exception.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL002	Debug Exceptions May be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed by a Write to SP
Problem	If a MOV SS or POP SS instruction generated a debug exception, and is not followed by an explicit write to the Stack Pointer (SP), the processor may fail to deliver the debug exception or, if it does, the DR6 register contents may not correctly reflect the causes of the debug exception.
Implication	Debugging software may fail to operate properly if a debug exception is lost or does not report complete information. Intel® has not observed this erratum with any commercially available software.
Workaround	Software should explicitly write to the stack pointer immediately after executing MOV SS or POP SS.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL003	CPUID L2 Cache Information May be Inaccurate
Problem	CPUID extended function 80000006H (EAX=80000006H) inaccurately reports information about the L2 cache in ECX. The function reports that the L2 cache size is 256K divided into 8 ways, while the actual L2 size and structure should be inferred from reading CPUID leaf 04H sub-leaf 02H.
Implication	Software that uses CPUID extended leaf 80000006H L2 cache information may operate incorrectly. Intel® has not observed this erratum to impact the operation of any commercially available software.
Workaround	None identified. Software should ignore the L2 cache size information reported by CPUID extended leaf 80000006H for the affected processors.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL004	Placing Posted-Interrupt Descriptors Within the PRMRR May Result in a Processor Hang
Problem	Posted-interrupt processing is a virtualization feature for interrupts which requires configuring addresses in the posted-interrupt descriptor fields in the Virtual Machine Control Structure (VMCS). Configuring posted-interrupt descriptors addresses that are within the PRMRR (Processor Reserved Memory Range Register, defined by MSR 1F4H and MSR 1F5H) may result in a logical processor hang.
Implication	This erratum may result in a processor hang. Intel® has not observed this erratum with any commercially available software.
Workaround	Virtual Machine Monitor (VMM) software should not use addresses within the PRMRR for posted-interrupt descriptors.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL005	Intel® PT CBR Packet May be Delayed or Dropped
Problem	Due to a complex set of microarchitectural conditions, the Intel® Processor Trace (Intel® PT) CBR (Core:Bus Ratio) packet generated on a frequency change may be dropped, without an OVF (Overflow) packet, or may be inserted into the trace late, after other packets (including possibly another CBR) that were generated after the frequency change completed.
Implication	An Intel® PT decoder may report an incorrect core; bus ratio to a portion of the trace, which may result in an incorrect wall clock time calculation.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL006	Intel® PT TIP or FUP Packets May be Dropped Without OVF Packet
Problem	The Intel® Processor Trace (Intel® PT) OVF (Overflow) packet may not be generated when only TIPs (Target IP Packets) and/or FUPs (Flow Update Packets) are lost due to internal buffer overflow.
Implication	A decoder error will result from the missing FUP and/or TIP packets.
Workaround	None identified. An Intel® PT decoder will be able to resume proper decode from the next FUP, TIP, or PSB (Packet Stream Boundary) packet. The incidence of error may be mitigated by setting IA32_RTIT_CTL. CYCEn[bit 1] (MSR 0570H) to 1, as an internal buffer overflow that loses a CYC packet will generate an OVF.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL007	Overflow Flag in IA32_MC0_STATUS MSR May be Incorrectly Set
Problem	Under complex microarchitectural conditions, a single internal parity error seen in IA32_MC0_STATUS MSR (401h) with MCACOD (bits 15:0) value of 5h and MSCOD (bits 31:16) value of 7h, may set the overflow flag (bit 62) in the same MSR.
Implication	Due to this erratum, the IA32_MC0_STATUS overflow flag may be set after a single parity error. Intel® has not observed this erratum with any commercially available software.
Workaround	None identified.

Status	For the steppings affected, refer to the Summary Table of Changes.

TGL008	**An Exception During a 32-bit Mode Task Switch with CET Enabled may Lead to an Incorrect TSS Busy Flag Value**
Problem	Under complex microarchitectural conditions, in 32Bit mode, the processor may reset the busy (B) flag in the Task State Segment (TSS) descriptor when handling a general protection exception (#GP), a control protection exception (#CP), or a page fault exception (#PF) that happens during a task switch when Control-flow Enforcement Technology (CET) is enabled, indicated by CR4. CET (bit 23).
Implication	Due to this erratum, the TSS descriptor busy flag might be incorrectly written as "not busy" in the TSS descriptor. Intel® has not observed this erratum with any commercially available software.
Workaround	Software should restore the busy flag in the TSS descriptor when handling #GP, #CP, or #PF exceptions, when CET is enabled.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL009	**Exit Qualification for EPT Violations Incorrectly Indicate On Instruction Fetches that the Guest-Physical Address Was Writeable**
Problem	On EPT violations, bit 4 of the Exit Qualification indicates whether the guest-physical address was writeable. When EPT is configured as supervisory shadow-stack (both bit 60 in EPT paging-structure leaf entry and bit 0 in EPT paging-structure entries are set), non-executable (bit 2 in EPT paging-structure entries is cleared), and non-writeable (bit 1 in EPT paging-structure entries is cleared) a VMExit due to a guest instruction fetch to a supervisory page will incorrectly set bit 4 of the Exit Qualification. Bits 3, 5, and 6 of the Exit Qualification is not impacted by this erratum.
Implication	Due to this erratum, bit 4 of the Exit Qualification may be incorrectly set. Intel® has not observed this erratum on any commercially available software.
Workaround	EPT handlers processing an EPT violation due to an instruction fetch access on a present page should ignore the value of bit 4 of the Exit Qualification.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL010	**Processor May Generate Spurious Page Faults on Shadow Stack Pages**
Problem	When operating in a virtualized environment, if shadow stack pages are mapped over an APIC page, the processor will generate spurious page faults on that shadow stack page whenever its linear to physical address translation is cached in the Translation Look-aside Buffer.
Implication	When this erratum occurs, the processor will generate a spurious page fault. Intel® is not aware of any software that maps shadow stack pages over an APIC page.
Workaround	Software should avoid mapping shadow stack pages over the APIC page.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL011	HDMI 1.4 Inter-Pair Skew Test May Fail
Problem	Type-C Port (TCP) PHY may fail the HDMI 1. 4 ID7-6 Inter-pair Skew Test for specific thermal corner cases.
Implication	Due to this erratum, the HDMI 1. 4 Inter-pair Skew Test may fail. Intel® has only observed this erratum in a synthetic test environment.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL012	Intel® PT ToPA Tables Read From Non-Cacheable Memory During an Intel® TSX Transaction May Lead to Processor Hang
Problem	If an Intel® Processor Trace (Intel® PT) ToPA (Table of Physical Addresses) table is placed in UC (Uncacheable) or USWC (Uncacheable Speculative Write Combining) memory, and a ToPA output region is filled during an Intel® TSX (Intel® Transaction Synchronization Extensions) transaction, the resulting ToPA table read may cause a processor hang.
Implication	Placing Intel® PT ToPA tables in non-cacheable memory when Intel® TSX is in use may lead to a processor hang.
Workaround	None identified. Intel® PT ToPA tables should be located in WB memory if Intel® TSX is in use.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL013	Performing an XACQUIRE to an Intel® PT ToPA Table May Lead to Processor Hang
Problem	If an XACQUIRE lock is performed to the address of an Intel® Processor Trace (Intel® PT) Table of Physical Addresses (ToPA) table, and that table is later read by the CPU during the HLE (Hardware Lock Elision) transaction, the processor may hang.
Implication	Accessing ToPA tables with XACQUIRE may result in a processor hang.
Workaround	None identified. Software should not access ToPA tables using XACQUIRE. An OS or hypervisor may wish to ensure all application or guest writes to ToPA tables to take page faults or EPT violations.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL014	PECI Frequency Limited to 3.2Kbps-1Mbps
Problem	The PECI (Platform Environmental Control Interface) 3.1 specification's operating frequency range is 2 Kbps to 2 Mbps. Due to this erratum, PECI may be unreliable when operated out of 3.2Kbps-1Mbps range.
Implication	Platforms attempting to run PECI out of 3.2Kbps-1Mbps range may not behave as expected.
Workaround	None identified. Platforms should limit PECI operating frequency to 3.2Kbps-1Mbps range.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL015	PCIe Gen4 JTOL – Jitter Tolerance Compliance Test May Fail
Problem	The processor may not meet the PCI Express M. 2 Specification Revision 4. 0, Version 0. 9 receiver Jitter Tolerance (JTol) Minimum Receiver Path Sensitivity requirements when operating at 16.0 GT/s under high temperature conditions.
Implication	Due to this erratum, the processor may exceed receiver jitter tolerance limits when tested at high temperature conditions. Intel® has not observed any impact to functional behavior or nominal PCIe compliance testing.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL016	System May Fail To Exit Warm Reset or S3
Problem	The processor may fail to access system memory if memory frequency changes between entry and exit of warm reset or S3.
Implication	When this erratum occurs the system may hang.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL017	Unable to Transmit Modified Compliance Test Pattern at 2.5 GT/S or 5.0 GT/s Link Speeds
Problem	The processor's PCIe port (Bus 0, Device 6, Function 0) does not transmit the Modified Compliance Test Pattern when in either 2. 5 GT/S or 5. 0 GT/s link speeds.
Implication	Due to this erratum, PCIe compliance testing may fail at 2. 5 GT/S or 5. 0 GT/s link speeds when enabling Modified Compliance Test Pattern.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL018	MSR IA32_THERM_STATUS CURRENT_LIMIT_STATUS May Report Incorrect Value
Problem	During a thermal event, MSR IA32_THERM_STATUS (19Ch) CURRENT_LIMIT_STATUS bit 12 may not reflect the proper value.
Implication	Due to this erratum, software may not be able to determine the cause of the frequency limitation.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL019	System May Hang During Package-C10 Exit
Problem	When exiting Package C10 the system may draw excessive current.
Implication	Due to this erratum, the system may hang.

Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL020	**Processor May Hang When PROCHOT# is Active**
Problem	When PROCHOT# is activated during BIOS initialization, the processor may hang with a machine check error reported in IA32_MCi_STATUS, with MCACOD (bits [15:0]) value of 0402H, and MSCOD (bits [31:16]) value of 0409H.
Implication	Due to this erratum, the processor may hang.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL021	**Processor May Hang if Warm Reset Triggers During BIOS Initialization**
Problem	Under complex microarchitectural conditions, when the processor receives a warm reset during BIOS initialization, the processor may hang with a machine check error reported in IA32_MCi_STATUS, with MCACOD (bits [15:0]) value of 0400H, and MSCOD (bits [31:16]) value of 0080H.
Implication	Due to this erratum, the processor may hang. Intel® has only observed this erratum in a synthetic test environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL022	**PCIe Link_Down May Occur After Exiting From Package C10 Cycle**
Problem	After a Package C10 Exit event, the processor's PCIe link may fail to retrain.
Implication	When, this erratum occurs, the PCIe link enters the Link Down state, which may lead to a system failure.
Workaround	It is possible for BIOS to include a workaround for this errata.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL023	**Reported Package Power May Not be Accurate**
Problem	MSR_PKG_ENERGY_STATUS (611H) bits[31:0] may not accurately reflect package power.
Implication	Due to this erratum, a higher than expected variation in the reported package power may be observed.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL024	USB TD65 Polling LFPS Duration Test Fail on Direct Port
Problem	The USB3 TD6.5 Compliance Polling LFPS Duration Test fails, because of Electrical Low Frequency Periodic Signalling (LFPS) common mode adjustment.
Implication	Due to this erratum, this compliance test will fail. Intel® has not observed a compliance test failure on ports with a platform-level retimer. Intel® has not observed any functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL025	Cache Configuration May be Incorrectly Initialized During Boot
Problem	The processor may fail to properly initialize internal cache configuration registers during boot.
Implication	Due to this erratum, the system may intermittently hang or exhibit unpredictable system behavior.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL026	N/A. Erratum has been removed.

TGL027	Processor PCIe Reference Clock May be Unavailable if CLKREQ# is Asserted During L1.2.Entry
Problem	Processor PCIe Reference Clock may be unavailable for up to Tpoweron after CLKREQ# is asserted by an end point device while root port is in L1.2.Entry.
Implication	End point devices that rely upon PCIe Refclk within Tpoweron may lead to PCIe Link instabilities; including link speed reduction and/or link drop.
Workaround	A BIOS code change has been identified and may be implemented as a mitigation for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL028	Processor PCIe May Hang Following PKG-C10
Problem	The DEKEL PHY may fail to resume following PKG-C10.
Implication	Due to this erratum, the CPU PCIe Link may hang resulting in an inaccessible PCIe device or a system hang.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL029	PCIe Width Change Transition May Fail
Problem	When a PCIe endpoint attempts to increase the PCIe link width after a previous link speed change, the upper lanes of the PCIe link may fail to train.
Implication	Due to this erratum, a PCIe link width change may fail and continue to operate at the previously configured link width.
Workaround	Endpoint devices need to perform link width change to maximum supported link width before performing any link speed change.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL030	DDR4 1Rx16 DIMMs Cannot Achieve Optimal Memory Configuration
Problem	DDR4 1Rx16 DIMMs cannot achieve optimal memory configuration, which may result in display artifacts.
Implication	Due to this erratum, visible display artifacts such as flickering or glitches may occur.
Workaround	It is possible for a BIOS code change to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL031	Incorrect Core Operating Voltage May Lead To Unpredictable System Behavior
Problem	Under complex microarchitectural conditions, it is possible for the processor to select an incorrect core operating voltage, which may lead to unpredictable system behavior.
Implication	Due to this erratum, the system may exhibit unpredictable system behavior.
Workaround	It is possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL032	Processor May Hang on PKG C9 or Deeper Exit
Problem	The processor may hang when exiting a Package (PKG) C9 or deeper state with a machine check exception (MCACOD=0402H, MSCOD=0471H).
Implication	Due to this erratum, the system may hang.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL033	Processor May Hang on Pkg C10 Exit
Problem	If the processor's Type C subsystem enters a TC7 state when the processor enters Package C10, the processor may hang upon Pkg C10 exit without reporting a machine check exception.
Implication	Due to this erratum, the system may hang.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL034	Executing an XSAVE or VZEROALL Instruction After SYSENTER May Result in Unexpected SSE/AVX Register Values
Problem	Under complex microarchitectural conditions, executing any of the XSAVE, XSAVEOPT, XSAVEC, XSAVES, or VZEROALL instructions shortly after the execution of SYSENTER may result in unexpected SSE/AVX register values.
Implication	Due to this erratum, software may observe unexpected values in the SSE/AVX registers. Intel® has only observed this erratum in a synthetic test environment.
Workaround	None identified. An operating system's SYSENTER handler should avoid using executing an XSAVE or VZEROALL instruction in its first ten instructions.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL035	Processor May Fail to Resume From Package C10
Problem	The processor may fail to resume from Package C10 and report an unexpected machine check exception.
Implication	Due to this erratum, the system may report a machine check exception (MSCOD 0403h, MCACOD 0402h, IP_READY_WAIT_TIMEOUT).
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL036	PkgC7 or Deeper Exits May Lead to Display Flicker
Problem	During Pkg C7 or deeper exit transitions, the processor may cause a display flicker.
Implication	Due to this erratum, a sporadic display flickering may be observed.
Workaround	It may be possible for BIOS to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL037	VCVTPS2PH To Memory May Update MXCSR in the Case of a Fault on Store
Problem	Execution of the VCVTPS2PH instruction with a memory destination may update the MXCSR exceptions flags (bits [5:0]) if the store to memory causes a fault (Example: #PF) or VM exit. The value written to the MXCSR exceptions flags is what would have been written if there were no fault.
Implication	Software may see exceptions flags set in MXCSR, although the instruction has not successfully completed due to a fault on the memory operation. Intel® has not observed this erratum to affect any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL038	Memory Contents May Not be Accessible After a Warm Reset
Problem	For platforms that have Intel® Trusted Execution Technology (Intel® TXT) (MSR IA32_FEATURE_CONTROL (3Ah)[2:1] = '11b') and Total Memory Encryption (TME) enabled (IA32_TME_ACTIVATE MSR (0982H), Bit 1 set to 1), software that performs a TXT launch (TXT.STS offset 000h bit 0 (SENTER.DONE.STS) = 1), intends to preserve memory across a warm reset, and performs a warm reset without first tearing down TXT ((TXT.STS offset 000h bit 1 (SEXIT.DONE.STS) = 1), may lead to the memory contents not being preserved.
Implication	Due to this erratum, software that relies on memory content but does not tear down TXT prior to a warm reset may not operate as expected. Intel® has observed BIOS Update Utilities to be susceptible to this erratum.
Workaround	It may be possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL039	Processor May Generate Malformed TLP
Problem	If the processor root port receives an FetchAdd, Swap, or CAS TLP (an atomic operation) that is erroneous, it should generate a UR completion to the downstream requestor. If the TLP has an operand size greater than 4 bytes, the generated UR completion will report an operand size of 4 bytes, which will be interpreted as a malformed transaction.
Implication	When this erratum occurs, the processor may respond with a malformed transaction.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL040	System May Experience an Internal Timeout Error When Directing Intel® PT to a Small, Uncacheable, Single-Range Output Buffer
Problem	A processor hang may result if Intel® Processor Trace (Intel®PT) is enabled with Mini Time Counter (MTC) packets and single range output mode (TraceEn[0]=1, MTCEn[9]=1 and ToPA[8]=0 in IA32_RTIT_CTL MSR (0570h)), while the output buffer is less than 1 KB in size (IA32_RTIT_OUTPUT_MASK_PTRS[31:0] MSR (0561h) < 0400h) and it is mapped as uncacheable (UC) or write protect (WP) memory type in the Memory Type Range Registers (MTRRs).
Implication	Due to this erratum, the system may experience an Internal Timer Error Machine Check (IA32_MCi_STATUS.MCACOD=400H; bits 15:0). Intel® has only observed this erratum in a synthetic test environment.
Workaround	Avoid directing Intel® PT output to an uncacheable buffer less than 1KB in size.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL041	N/A. Erratum has been removed.

TGL042	Spurious FIVR OCP Event May Occur During Boot
Problem	During system boot, a spurious Fully Integrated Voltage Regulator (FIVR) Over-Current Protection (OCP) machine check (IA32_MC6_STATUS MSR (419h) with MSCOD (bits[31:16]) value of 0810h and MCACOD (bits[15:0]) value of 0402h) may occur.
Implication	When this erratum occurs, the system may fail to boot.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL043	Embedded Display Flicker May be Observed During Idle Scenarios
Problem	During idle scenarios, the processor may cause the embedded display to flicker.
Implication	Due to this erratum, a sporadic display flickering may be observed.
Workaround	It may be possible to workaround this erratum with a combination of a graphics driver and a BIOS code change.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL044	False MC1 Error Reported in the Shadow of an Internal Timer Error
Problem	After an internal timer error has been reported in MC3_STATUS MSR (0x40d) with MCACOD (bits [15:0]) value of 0400H, and MSCOD (bits [31:16]) value of 0080H, under complex micro-architectural conditions, a false error may be reported in MC1_STATUS MSR (0x405) with MCACOD 0x174 or MCACOD 0x124.
Implication	Due to this erratum, a false MCE may be reported in MC1_STATUS MSR. Intel® has only observed this erratum in a synthetic test environment.
Workaround	Software should ignore the MC1_STATUS error when it appears with an internal timer error.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL045	PCIe Link May Fail to Train Upon Exit From L1.2
Problem	When the PCIe Link exits the L1.2 low-power link state, the link may fail to correctly train to L0.
Implication	Due to this erratum, a PCIe link may incur unexpected link recovery events or it may enter a Link_Down state.
Workaround	It may be possible for a BIOS code change to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL046	DMI Link Failure During L1 Exit
Problem	During S3/S4/S5 and/or S0ix cycles, DMI may fail to exit L1 in the time required.
Implication	The system may hang with a machine check exception (MCACOD=2AH).
Workaround	It is possible for a BIOS code change to workaround this erratum.

TGL046	DMI Link Failure During L1 Exit
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL047	Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT Does Not Prevent The Three-strike Counter From Incrementing
Problem	Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT (bit 11 in MSR 1A4h) does not prevent the three-strike counter from incrementing as documented; instead, it only prevents the signaling of the three-strike event once the counter has expired.
Implication	Due to this erratum, software may be able to see the three-strike logged in the MC3_STATUS (MSR 40Dh, MCACOD = 400h [bits 15:0]) even when MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT is set.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL048	Intel® PT TIP.PGD May Not Have Target IP Payload
Problem	When Intel® PT (Intel® Processor Trace) is enabled and a direct unconditional branch clears IA32_RTIT_STATUS.FilterEn (MSR 571H, bit 0), due to this erratum, the resulting TIP.PGD (Target IP Packet, Packet Generation Disable) may not have an IP payload with the target IP.
Implication	It may not be possible to tell which instruction in the flow caused the TIP.PGD using only the information in trace packets when this erratum occurs.
Workaround	The Intel® PT trace decoder can compare direct unconditional branch targets in the source with the FilterEn address range(s) to determine which branch cleared FilterEn.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL049	Intel® Processor Trace PSB+ Packets May Contain Unexpected Packets
Problem	Some Intel® Processor Trace packets should be issued only between TIP.PGE (Target IP Packet.Packet Generation Enable) and TIP.PGD (Target IP Packet.Packet Generation Disable) packets. Due to this erratum, when a TIP.PGE packet is generated it may be preceded by a PSB+ (Packet Stream Boundary) that incorrectly includes FUP (Flow Update Packet) and MODE.Exec packets.
Implication	Due to this erratum, FUP and MODE.Exec may be generated unexpectedly.
Workaround	Decoders should ignore FUP and MODE.Exec packets that are not between TIP.PGE and TIP.PGD packets.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL050	Intel® PT Trace May Drop Second Byte of CYC Packet
Problem	Due to a rare microarchitectural condition, the second byte of a 2-byte CYC (Cycle Count) packet may be dropped without an OVF (Overflow) packet.
Implication	A trace decoder may signal a decode error due to the lost trace byte.

TGL050	Intel® PT Trace May Drop Second Byte of CYC Packet
Workaround	None identified. A mitigation is available for this erratum. If a decoder encounters a multi-byte CYC packet where the second byte has bit 0 (Ext) set to 1, it should assume that 4095 cycles have passed since the prior CYC packet, and it should ignore the first byte of the CYC and treat the second byte as the start of a new packet.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL051	VM Entry That Clears TraceEn May Generate a FUP
Problem	If VM entry clears Intel® PT (Intel® Processor Trace) IA32_RTIT_CTL.TraceEn (MSR 570H, bit 0) while PacketEn is 1 then a FUP (Flow Update Packet) will precede the TIP.PGD (Target IP Packet, Packet Generation Disable). VM entry can clear TraceEn if the VM-entry MSR-load area includes an entry for the IA32_RTIT_CTL MSR.
Implication	When this erratum occurs, an unexpected FUP may be generated that creates the appearance of an asynchronous event taking place immediately before or during the VM entry.
Workaround	The Intel® PT trace decoder may opt to ignore any FUP whose IP matches that of a VM entry instruction.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL052	Intel® PT Trace May Contain Incorrect Data When Configured With Single Range Output Larger Than 4KB
Problem	Under complex micro-architectural conditions, when using Intel® Processor Trace (Intel® PT) with single range output larger than 4KB, disabling PT and then enabling PT using the TraceEn bit in IA32_RTIT_CTL MSR (MSR 570h, bit 0) may cause incorrect output values to be recorded.
Implication	Due to this erratum, a PT trace may contain incorrect values.
Workaround	None identified. Software should avoid using PT with single range output larger than 4KB.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL053	On Instructions Longer Than 15 Bytes, #GP Exception is Prioritized And Delivered Over #CP Exception
Problem	A #GP (global protection exception) that results from an instruction being longer than 15 bytes is prioritized and served before a #CP (Controlflow Protection exception) that was created due to a missing ENDBRx instruction at the target of an indirect branch.
Implication	Due to this erratum, during an indirect jump with ENDBRANCH tracking, if the processor lands on an illegal instruction with length longer than 15 bytes or that decodes to a CS limit, the processor will prioritize and deliver a #GP exception over the #CP exception.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL054	Mismatch on DR6 Value When Breakpoint Match is on Bitmap Address
Problem	Under complex microarchitectural conditions, on systems with Control-flow Enforcement Technology (CET) enabled, hitting a predefined data breakpoint may not be reported in B0-B3 (bits 3:0) in the DR6 register if that breakpoint was set on the legacy code page bitmap.
Implication	Due to this erratum, software may not know which breakpoint triggered when setting breakpoints on the legacy code page bitmap.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL055	Unaligned CET-SS Stack Token Does Not Signal #GP
Problem	On systems that enable Control-flow Enforcement Technology shadow-stack (CET-SS) in supervisor mode, an inter-privilege level far CALL or event delivery switches the shadow stack to a supervisor shadow stack. During this switch, the processor fails to signal a #GP exception if the 32-byte region comprised of 8 bytes containing the supervisor shadow stack token and the following 24-byte stack frame are not 32-byte aligned on the shadow stack.
Implication	Due to this erratum, on systems that enable CET-SS in supervisor mode, system software that fails to properly 32-byte align the supervisor shadow stack token may incorrectly mark the supervisor shadow stack token as busy, preventing re-entry into the supervisor thread by generating an unexpected #GP exception unrelated to stack token alignment.
Workaround	It may be possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL056	USB 3.0 Device May Not be Detected or May Down Train to USB 2.0 Speed
Problem	When hot-plugging a USB 3.0 Device that is connected through a Type A to Type C cable, the device may not be detected or may down train to USB 2.0 speed when connected to a Type-C port.
Implication	Due to this erratum, a USB 3.0 Device may not be detected or may down train to USB 2.0 speed.
Workaround	It may be possible for BIOS code changes to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL057	Call Instruction Wrapping Around The 32-bit Address Boundary May Return to Incorrect Address
Problem	In 32-bit mode, a call instruction wrapping around the 32-bit address should save a return address near the bottom of the address space (low address) around address zero. Under complex micro-architectural conditions, a return instruction following such a call may return to the next sequential address instead (high address).

Implication	Due to this erratum, In 32-bit mode a return following a call instruction that wraps around the 32-bit address boundary may return to the next sequential IP without wrapping around the address, possibly resulting in a #PF. Intel® has not observed this behavior on any commercially available software.
Workaround	Software should not place call instructions in addresses that wrap around the 32-bit address space in 32-bit mode.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL058	**USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst**
Problem	On USB 3.2 Gen 1x1 only capable ports, including ports configured as USB 3.2 Gen 1x1 by soft strap, the xHCI controller may send only 15 LFPS signals instead of a burst of 16 LFPS signals as specified by the USB 3.2 specification.
Implication	There are no known functional implications due to this erratum. LFPS handshake requires the receiver link partner to only detect 2 LFPS signals. This issue may impact the SuperSpeed compliance test case which checks for the 16 LFPS burst requirements: TD6.4, TD6.5, and TD7.31.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL059	**Incorrect MCACOD For L2 Prefetch MCE**
Problem	Under complex micro-architectural conditions, an L2 prefetch MCE that should be reported with MCACOD 165h in IA32_MC3_STATUS MSR (MSR 40dh, bits [15:0]) may be reported with an MCACOD of 101h.
Implication	Due to this erratum, the reported MCACOD for this MCE may be incorrect.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL060	**Crashlog and Telemetry BAR May Not Function Correctly**
Problem	The Crashlog and Telemetry PM_BAR register (Bus 0, Device 10, Function 0, Offset 10h) does not correctly implement the BAR sizing function. It reports a 32K BAR, but the BAR requires 64K memory alignment.
Implication	Due to this erratum, if PM_BAR is 32K aligned, but not 64K aligned, accesses to the BAR will fail.
Workaround	None identified. BIOS must ensure that this BAR is 64K aligned.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL061	**LFENCE Instruction May Not Prevent FSFP Forwarding**
Problem	When the Fast Store Forwarding Predictor (FSFP) is enabled, the LFENCE instruction may allow older stores to be predictively forwarded to younger loads.

Implication	Due to this erratum, software that relies on the LFENCE instruction to prevent FSFP forwarding may not behave as expected.
Workaround	It may be possible for BIOS to contain a workaround for this Erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL062	**GPU Hang When Async Compute is Enabled**
Problem	GPU may hang when Async Compute is enabled
Implication	Due to this erratum, the GPU may hang when running high bandwidth GFx application such as benchmarks and/or games.
Workaround	None identified. The Async Compute feature will be disabled in a graphics driver update. Please see GFx Driver Revenue SV2 PR5 (101.3616 or later) and release notes.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL063	**Branch Predictor May Produce Incorrect Instruction Pointer**
Problem	Under complex microarchitectural conditions, the branch predictor may produce an incorrect instruction pointer leading to unpredictable system behavior.
Implication	Due to this erratum, the system may exhibit unpredictable behavior.
Workaround	It may be possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL064	**Processor May Encrypt TME Exclude Range if Mapped to Remap Range**
Problem	The processor accesses to TME exclude range may be encrypted but not decrypted if mapped to remap range.
Implication	Due to this erratum, the processor exclude range it will be encrypted but will but not decrypted if mapped to remap range.
Workaround	It may be possible for BIOS to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL065	xHCI Force Header Command Incorrect Return Code
Problem	The xHCI controller does not return the correct completion code for the Force Header Command as defined in the Section 4.6.16 of the eXtensible Host Controller Interface for Universal Serial Bus (xHCI) Requirements Specification Rev 1.2.
Implication	xHCI CV TD4.12 - Force Header Command Test may report an error. Intel® has obtained a waiver for TD 4.12. The Force Header Command is only used by the USB-IF Command Verifier (xHCI CV) tool for device testing. There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL066	USB Type-C Monitor Removal May Result In System Hang
Problem	Platform designs with discrete graphics may hang upon removal of a USB Type-C monitor from the system.
Implication	Due to this erratum the system may hang.
Workaround	It is possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

TGL067	USB 3.2 DbC Sublink Speed Attribute ID (SSID) Value
Problem	The USB 3.2 Debug Class Device (DbC) reports an incorrect Sublink Speed Attribute ID (SSID) value in the SuperSpeedPlus USB Device Capability field.
Implication	Due to this erratum, the processor USB 3.2.DbC (Debug Capability) device may fail to enumerate when connected to a USB 3.2 Gen 2x1 port.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

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Specification Changes

ID	Affected Products/ Steps	Specification Change Title	Issue	Previous Text Reference	New Text	Affected Document
001	UP3 B1	HDCP 2.2 not supported in certain modes for DP1.4a interface.	While using DP1.4a output ports in MST (Multi transport mode) and Forward Error Correction (FEC) and utilizing HDCP2.2 for protected content, bitstream corruption can occur.	The processor supports both HDCP 2.3 and 1.4 content protection over wired displays (HDMI* and DisplayPort*).	The processor supports both HDCP 2.3 and 1.4 content protection over wired displays (HDMI* and DisplayPort*). HDCP 1.4 will be supported for DisplayPort wired displays while operated in multistream transports and FEC is enabled.	631121
002	TGL-H	DP-in support of both LTTPR transparent and non-transparent modes.	dGPU which are routed through DP-in may result in external panel not being enabled if dGPU does not support LTTPR non-transparent mode.	The processor supports DP1.4a LTTPR non-transparent mode.	The processor supports the below LTTPR modes of operation: Non-transparent mode Transparent mode for port which enables BBR re-timer	631121

NOTE: There are no Specification Clarifications or Document Changes for this revision of the specification update.

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