3rd Generation Intel® Xeon® Scalable Processors, Codename Cooper Lake

Specification Update

April 2023

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Revision History

Date	Revision	Description
April 2023	015US	Added erratum CPX25.
January 2023	014US	Added erratum CPX24.
September 2022	013US	Added erratum CPX23.
August 2022	012US	Added erratum CPX22.
July 2022	011US	Added erratum CPX21.
June 2022	010US	Added erratum CPX20. Updated Nomenclature.
March 2022	1.6/009US	Added errata CPX18., CPX19.
February 2022	1.5/008US	Added errata CPX15., CPX16., CPX17.
November 2021	005US	Added erratum CPX14.
May 2021	1.3	Added erratum CPX13.
April 2021	1.2	Product name updated to "3rd Generation Intel® Xeon® Scalable Processors, Codename Cooper Lake". Added errata CPX12.
February 2021	1.1	Renumbered CPX4. to CPX6. Renumbered CPX5. to CPX8. Renumbered CPX6. to CPX9. Added errata CPX4., CPX5., CPX7., CPX10. and CPX11.
January 2021	1.0	Initial Release.

Preface

This document is an update to the specifications contained in the Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Related Documents

Document Title	Document Number/ Location
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture	253665
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference, A-L	253666
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference, M-U	253667
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide, Part 1	253668
Intel® 64 and IA-32 Architectures Software Developer's Manual Volume 3B: System Programming Guide, Part 2	253669
Intel® Xeon® Processor Scalable Family (Cooper Lake) BIOS Writer's Guide (BWG)	607480
ACPI Specifications	www.acpi.info

Nomenclature

Errata are design defects or errors. These may cause the 3rd Generation Intel® Xeon® Scalable Processors, Codename Cooper Lake's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

S-Spec Number is a five-digit code used to identify products. Products are differentiated by their unique characteristics, such as, core speed, L2 cache size, all notes associated with each S-Spec number.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, and manuals).

Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the 3rd Generation Intel® Xeon® Scalable Processors, Codename Cooper Lake. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

	Change bar to the left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Number	Steppings			Status	ERRATA
	A0	A1	#		
CPX1.	X			No Fix	PCIe* Root Port Does Not Increment REPLAY_NUM on Multiple NAKs of The Same TLP.
CPX2.	X			No Fix	M2MEM Timeout With DRAM RAPL in Presence of CAP Errors.
CPX3.		X		No Fix	Memory Controller RAPL May Cause MESH2MEM Timeout on 3DS LRDIMMS.
CPX4.	X	X		No Fix	VERR Instruction Inside VM-entry May Cause DR6 to Contain Incorrect Values.
CPX5.	X	X		No Fix	A Fixed Interrupt May Be Lost When a Core Exits C6
CPX6.	X	X		No Fix	Memory Errors in a VLS Region on a Certain Device May not Be Properly Corrected.
CPX7.		X		No Fix	Retried PECI PCIConfigLocal Register Accesses May Not Operate Correctly.
CPX8.		X		No Fix	High Levels of Posted Interrupt Traffic on The PCIe* Port May Result in a Machine Check With a TOR Timeout.
CPX9.		X		No Fix	An Incorrect Instruction Pointer May Be Reported for a REP MOVS Instruction.
CPX10.	X			No Fix	When in CPGC Mode With Memory Refresh Disabled DDR Scheduler May be Blocked From Issuing CPGC Commands.
CPX11.	X	X		No Fix	A PMI That Freezes LBRs Can Cause a Duplicate Entry in TOS.
CPX12.	X			No Fix	Processor May Fail to Retry a Write to DDRT Memory.
CPX13.	X	X		No Fix	Overflow Flag in IA32_MC0_STATUS MSR May be Incorrectly Set.
CPX14.	X			No Fix	IA_PERF_LIMIT_REASONS MSR May Not Properly Report Frequency Clipping Cause.
CPX15.	X	X		No Fix	WBINVD/INVD Execution May Result in Unpredictable System Behavior
CPX16.	X	X		No Fix	Unexpected Code Breakpoint May Occur
CPX17.	X	X		No Fix	Writing Non-Zero Values to Read Only Fields in IA32_THERM_STATUS MSR May Cause a #GP
CPX18.	X	X		No Fix	Incorrect MCACOD For L2 MCE
CPX19.	X	X		No Fix	Poison Data Reported Instead of a CS Limit Violation
CPX20.	X	X		No Fix	HWPM Max Ratio May Not be Capped at P1
CPX21.	X	X		No Fix	Call Instruction Wrapping Around The 32-bit Address Boundary May Return to Incorrect Address
CPX22.	X	X		No Fix	During ADDDC Sparing Operation M2M MC Bank Counters May be Incorrect
CPX23.	X	X		No Fix	Accesses to CHA Configuration Space Beyond the CHA Logical Limit May Fail
CPX24.	X	X		No Fix	False Memory Error May Cause The System Hang.
CPX25.	X	X		No Fix	Branch Predictor May Produce Incorrect Instruction Pointer

Specification Changes

Number	SPECIFICATION CHANGES
1	None for this revision of this specification update.

Specification Clarifications

No.	SPECIFICATION CLARIFICATIONS
1	None for this revision of this specification update.

Documentation Changes

No.	DOCUMENTATION CHANGES
1	None for this revision of the specification update.

Identification Information

Component Identification via Programming Interface

The 3rd Generation Intel® Xeon® Scalable Processors, Codename Cooper Lake stepping can be identified by the following register contents:

3rd Generation Intel® Xeon® Scalable Processors, Codename Cooper Lake Stepping	Features	Vendor ID	Device ID	Revision Number
A-0			0x0005065A	
A-1			0x0005065B	

Component Marking Information

For 3rd Generation Intel® Xeon® Scalable Processors, codename Cooper Lake, SKUs, see https://ark.intel.com/content/www/us/en/ark/products/series/204098/3rd-generation-intel-xeon-scalable-processors.html

Errata

CPX1. PCIe* Root Port Does Not Increment REPLAY_NUM on Multiple NAKs of The Same TLP.

Problem: PCIe* Root Port does not increment REPLAY_NUM on a replay initiated by a duplicate Negative Acknowledgment (NAK) for the same Transaction Layer Packet (TLP) and does not retain the link.

Implication: If a non-compliant Endpoint NAKs the same TLP repeatedly, the lack of forward progress can lead to (PCIe* Completion, Table of Requests [TOR], Internal Timer Machine Check Error [MCE]) timeout.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX2. M2MEM Timeout With DRAM RAPL in Presence of CAP Errors.

Problem: If a Command/Address Parity (CAP) error occurs when DRAM Running Average Power Limit (RAPL) is enabled, the processor may hang.

Implication: Due to this erratum, the processor may hang with a mesh-to-mem timeout Machine Check Exception (MSCOD=20h, MCACOD=400h).

Workaround: It is possible for a BIOS to contain a workaround for this erratum.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX3. Memory Controller RAPL May Cause MESH2MEM Timeout on 3DS LRDIMMS.

Problem: On a system with at least one DRAM channel populated with 2DPC 3DS LRDIMMs running at 2933MHz or 3200MHz with RAPL enabled, the processor may hang when running high bandwidth workloads.

Implication: Due to this erratum, the processor may hang with a mesh-to-mem timeout Machine Check Exception (MSCOD=20h, MCACOD=400h).

Workaround: It is possible for a BIOS to contain a workaround for this erratum.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX4. VERR Instruction Inside VM-entry May Cause DR6 to Contain Incorrect Values.

Problem: Under complex micro-architectural conditions, a VERR instruction that follows a VM-entry with a guest-state area indicating MOV SS blocking (bit 1 in the Interruptibility state) and at least one of B3-B0 bits set (bits 3:0 in the pending debug exception) may lead to incorrect values in DR6.

Implication: Due to this erratum, DR6 may contain incorrect values. Intel has not observed this erratum with any commercially available software.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX5. A Fixed Interrupt May Be Lost When a Core Exits C6

Problem: Under Complex micro-architectural conditions, when performance throttling happens during a core C6 exit, a fixed interrupt may be lost.

Implication: Due to this erratum, a fixed interrupt may be lost when internal throttling happens during a core C6 exit. Intel has only observed this erratum in synthetic test conditions.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX6. Memory Errors in a VLS Region on a Certain Device May not Be Properly Corrected.

Problem: Under complex micro-architectural conditions, when Adaptive Data Correction (ADC) or Adaptive Double Device Data Correction (ADDDC) is enabled, and the system has spared out a DRAM device 0, 1, 3, 4, 5, 8, 13, 15 or 16, and the system is in VLS mode, then if a limited subset of multi-bit errors are detected on primary DRAM device 16 in the Virtual Lockstep (VLS) region, those errors may not be properly corrected.

Implication: The system may experience unpredictable system behavior. Intel has only observed this behavior under synthetic testing conditions.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX7. Retried PECI PCIConfigLocal Register Accesses May Not Operate Correctly.

Problem: When the processor Requests a PECI PCIConfigLocal Read or Write command to be retried, and the PECI host immediately retries the command (within 150 us), the processor may fail to correctly process the retried PECI command.

Implication: Due to this erratum, the PECI PCIConfigLocal Read command may return incorrect data, and the PECI PCIConfigLocal Write command may incorrectly update the target.

Workaround: It is possible for a BIOS to contain a workaround for this erratum.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX8. High Levels of Posted Interrupt Traffic on The PCIe* Port May Result in a Machine Check With a TOR Timeout.

Problem: High levels of posted interrupt traffic on the PCIe* port may lead to a TOR Timeout Machine Check Exception (MSCOD=000Ch, MCACOD="Cache Hierarchy Errors") in bank IA32_MC9_STATUS (MSR 425h), IA32_MC10_STATUS (MSR 429h), or IA32_MC11_STATUS (MSR 42Dh)"

Implication: Due to this erratum, the system may hang.

Workaround: It is possible for a BIOS to contain a workaround for this erratum.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX9. An Incorrect Instruction Pointer May Be Reported for a REP MOVS Instruction.

Problem: When a REP MOVS instruction reports a Software Recoverable Action Required (SRAR) error for memory that software did not intend to access, the instruction pointer is reported incorrectly on the thread where RIP/EIPV=1.

Implication: Due to this erratum, the processor may report SRAR error with an incorrect instruction pointer.

Workaround: It is possible for a BIOS to contain a workaround for this erratum.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX10. When in CPGC Mode With Memory Refresh Disabled DDR Scheduler May be Blocked From Issuing CPGC Commands.

Problem: When memory refresh is disabled during Converged Pattern Generation and Checking (CPGC) mode, the Integrated Memory Controller (iMC) scheduler may become blocked from issuing CPGC read and write commands.

Implication: Due to this erratum, a system hang or continuous restart may occur.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX11. A PMI That Freezes LBRs Can Cause a Duplicate Entry in TOS.

Problem: If a Performance Monitor Interrupt (PMI) is taken while Last Branch Records (LBRs) are enabled and IA32_DEBUGCTL.FREEZE_LBRS_ON_PMI[bit 11]=1 (MSR 01D9H), a taken branch that performs an LBR update near the time of the PMI may instead record a duplicate of the prior entry into the Top of Stack (TOS) entry.

Implication: Software may unexpectedly observe the appearance of back-to-back execution of the same branch.

Workaround: In general, software can ignore the TOS entry if it matches the TOS-1 entry. Note that certain code sequences with no intervening taken branches can legitimately insert a valid duplicate LRB record in the TOS entry.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX12. Processor May Fail to Retry a Write to DDRT Memory.

Problem: If a system DDR4 memory module asserts ALERT# to signify a transaction error, such as a Command Address Parity error or Write CRC error, the processor may fail to retry a write to DDRT memory. This erratum can only occur in memory configurations that have both DDR4 and DDRT memory in the same channel.

Implication: Due to this erratum, unexpected system behavior may occur.

Workaround: It is possible for a BIOS to contain a workaround for this erratum.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX13. Overflow Flag in IA32_MC0_STATUS MSR May be Incorrectly Set.

Problem: Under complex micro-architectural conditions, a single internal parity error seen in IA32_MC0_STATUS MSR (401h) with MCACOD (bits 15:0) value of 5h and MSCOD (bits 31:16) value of 7h, may set the overflow flag (bit 62) in the same Model Specific Register (MSR).

Implication: Due to this erratum, the IA32_MC0_STATUS overflow flag may be set after a single parity error. Intel has not observed this erratum with any commercially available software.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX14. IA_PERF_LIMIT_REASONS MSR May Not Properly Report Frequency Clipping Cause.

Problem: The VR_THERM_ALERT_LOG (bit 22) and VR_THERM_ALERT_STATUS (bit 6) fields in IA_PERF_LIMIT_REASONS MSR (64Fh) do not log a VR_HOT event. In addition, the associated PERFMON event VR_HOT_CYCLES (42h) does not increment upon VR_HOT events.

Implication: Due to this erratum, software may not be able to determine whether frequency clipping is due to VR_HOT events.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX15. WBINVD/INVD Execution May Result in Unpredictable System Behavior

Problem: Under complex micro-architectural conditions, the processor may hang or exhibit unpredictable system behavior during Writeback and Invalidate Cache (WBINVD) or Invalidate Internal Caches (INVD) cache instruction execution on a two-or-more socket system.

Implication: When this erratum occurs, the processor may hang, reporting an Internal Timer Error in MCi_STATUS MSRs (40Dh, 411h) with MSCOD (bits[31:16]) value of 0080h and MCACOD (bits[15:0]) value of 0400h, or reporting a Table Of Requests (TOR) Timeout in MCi_STATUS MSRs (425h, 429h, or 42Dh) with an MSCOD value of 000Ch, or it may exhibit unpredictable system behavior. Intel has only observed this erratum in a synthetic test environment.

Workaround: It is possible for a BIOS to contain a workaround for this erratum.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX16. Unexpected Code Breakpoint May Occur

Problem: An unexpected code breakpoint may occur in one logical thread on a physical core while another logical thread on the same physical core is performing a Branch Prediction Unit Flush (MSR 0x49, bit [0] set to 1).

Implication: Due to this erratum, the processor may take an unexpected code breakpoint exception. Software that is not configured to manage such an exception may not operate as expected.

Workaround: It is possible for a BIOS to contain a workaround for this erratum.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX17. Writing Non-Zero Values to Read Only Fields in IA32_THERM_STATUS MSR May Cause a #GP

Problem: IA32_THERM_STATUS MSR (19CH) includes read-only (RO) fields as well as writable fields. Writing a non-zero value to any of the read-only fields may cause a #GP.

Implication: Due to this erratum, software that reads the IA32_THERM_STATUS MSR, modifies some of the writable fields, and attempts to write the MSR back may cause a #GP.

Workaround: It is possible for a BIOS to contain a workaround for this erratum.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX18. Incorrect MCACOD For L2 MCE

Problem: Under complex micro-architectural conditions, an L2 poison MCE that should be reported with MCACOD 189h in IA32_MC3_STATUS MSR (MSR 40dh, bits [15:0]) may be reported with an MCACOD of 101h.

Implication: Due to this erratum, the reported MCACOD for this MCE may be incorrect.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX19. Poison Data Reported Instead of a CS Limit Violation

Problem: Under complex micro-architectural conditions, in case of poisoned data on an address that violates the CS (code segment) limit, a poison MCE may be signaled and logged in IA32_MC0_STATUS MSR (MSR 401H, MCACOD 150h) instead of CS limit violation.

Implication: Due to the erratum, the processor may signal an MCE, rather than a higher-priority CS limit violation.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX20. HWPM Max Ratio May Not be Capped at P1

Problem: The platform may be granted a ratio higher than the guaranteed ratio (P1) when the Energy Efficient Turbo Disable bit (19) in the POWER_CTL1 MSR is set to 1h if a ratio higher than P1 is requested in HWPM (Hardware Power Management) OOB (Out of Band) mode.

Implication: Due to this erratum, Turbo mode disable may not be enforced for HWPM. Intel has not observed any functional failures due to this erratum.

Workaround: None identified.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX21. Call Instruction Wrapping Around The 32-bit Address Boundary May Return to Incorrect Address

Problem: In 32-bit mode, a call instruction wrapping around the 32-bit address must save a return address near the bottom of the address space (low address) around address zero. Under complex micro-architectural conditions, a return instruction following such a call may return to the next sequential address instead (high address).

Implication: Due to this erratum, in 32-bit mode, a return following a call instruction that wraps around the 32-bit address boundary may return to the next sequential IP without wrapping around the address, possibly resulting in a #PF. Intel has not observed this behavior on any commercially available software.

Workaround: Software should not place call instructions in addresses that wrap around the 32-bit address space in 32-bit mode.

Status: For the steppings affected, refer to the Summary Tables of Changes.

CPX22. During ADDDC Sparing Operation M2M MC Bank Counters May be Incorrect

Problem: When an ADDDC sparing operation occurs under demand load, spurious corrected transient errors may be logged incorrectly in non-participating M2M MC Bank counters.

Implication: Due to this erratum, M2M MC Bank per rank counters may be incorrect.

Workaround: None identified.

Status: For the steppings affected, see the Summary Tables of Changes.

CPX23. Accesses to CHA Configuration Space Beyond the CHA Logical Limit May Fail

Problem: The processor may have more Caching and Home Agent (CHA) physically implemented than are logically available in the processor. CHA configuration registers are located in the PCIe* configuration space associated with the CHA bus, device, and function, with the first CHA being located at Bus1, Device 8, Function 0, and also BUS 1, Device 14, Function 0. There are 2 functions in PCI Configuration (CFG) space for each CHA. Accesses to CHA configuration space may not return valid results for BDFs beyond the number of logical CHAs supported in the processor as enumerated in CAPID6 (Bus 1, Device 30, Function 3, Offset 9Ch, bits [27:0]).

Implication: Due to this erratum, accesses to CHA configuration spaces, including Device ID, for CHAs beyond the CHA logical limit may not return valid results.

Workaround: None identified. Software must not rely upon CHA configuration space for CHAs beyond the logic limit of the processor.

Status: For the steppings affected, see the Summary Tables of Changes.

CPX24. False Memory Error May Cause The System Hang.

Problem: False memory error may be reported when DDR4 speed is 3200 and Advanced Memory Test (AMT) type15 is enabled.

Implication: Due to this erratum, false memory error may be reported leading to System hang.

Workaround: None Identified. Using BIOS Setup AdvMemTestCondition can set tWR to 22tck or changing DDR4 speed to DDR2993 to avoid False memory error, when AMT is enabled.

Status: For the steppings affected, see the Summary Tables of Changes.

CPX25. Branch Predictor May Produce Incorrect Instruction Pointer

Problem: Under complex microarchitectural conditions, the branch predictor may produce an incorrect instruction pointer leading to unpredictable system behavior.

Implication: Due to this erratum, the system may exhibit unpredictable behavior.

Workaround: It is possible for a BIOS to contain a workaround for this erratum.

Status: For the steppings affected, see the Summary Tables of Changes

Specification Changes

There are no Specification Clarifications in this Specification Update revision.

Specification Clarifications

There are no Specification Clarifications in this Specification Update revision.

Documentation Changes

There are no Documentation Changes in this Specification Update revision.