Intel Atom® x6000E Series, and Intel® Pentium® and Celeron® N and J Series Processors for IoT Applications

Datasheet, Volume 2 (Book 1 of 3)

Compute Die Registers Only

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Revision Date	Revision Number	Description
March 2024	002	Chapter 3, "Host Memory Mapped Configuration Space (MCHBAR) Registers" — Section 3.58 - Add new register
March 2021	001	Initial release.

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1 Introduction

The Intel Atom® x6000E series, Pentium® N and J series, and Celeron® N and J series processor is targeted towards various IoT segments, such as industrial, retail, and embedded. It features real time compute with technologies such as TSN, TCC, which are expected to drive the future of IoT.

Intel Atom® x6000E series, Pentium® N and J series, and Celeron® N and J series processor is an Intel Architecture (IA) Multi-Chip Processor (MCP) 2-Chip Package, built on a 10-nanometer Compute Die and a 14-nanometer Platform Controller Hub (PCH) into a single package. Both dies are connected via the On Package Interface (OPI).

Note: For Intel Atom® x6000E series, Pentium® N and J series, and Celeron® N and J series processor, DMI has been mentioned in this document are synonymous with OPI.

1.1 About this Manual

This document is intended for Original Equipment Manufacturers (OEMs), Original Design Manufacturers (ODM) and BIOS vendors creating products based on the Elkhart Lake family Multi Chip Package (MCP).

Throughout this document, the name "Processor" is used as a general term and refers to all Elkhart Lake family SKUs, unless specifically noted otherwise. The compute die may be referred to simply as "Compute Die" and the Platform Controller Hub may be referred to simply as "PCH".

This manual assumes a working knowledge of the vocabulary and principles of interfaces and architectures such as PCI express* (PCIe*), Universal Serial Bus (USB), Advanced Host Controller Interface (AHCI), eXtensible Host Controller Interface (xHCI), and so forth.

This manual abbreviates PCI buses as Bn, devices as Dn and functions as Fn. For example, Device 31 Function 0 is abbreviated as D31:F0, and Bus 1 Device 8 Function 0 is abbreviated as B1:D8:F0. Generally, the bus number will not be used, and can be considered to be Bus 0. These numbers are shown as decimal unless otherwise indicated.

This is the core reference document for external design specifications. Information provided here takes precedence, if there are any discrepancies found in related documents.

1.1.1 Terminology Usage

This document uses the terms 'initiator' and 'target' (formerly known as 'master' and 'slave').

1.2 References

Specification	Document #/Location
Intel Atom® x6000E Series, and Intel® Pentium® and Celeron® N and J Series Processors for IoT Applications Datasheet Volume 1	636112

Specification	Document #/Location
Intel Atom® x6000E Series, and Intel® Pentium® and Celeron® N and J Series Processors for Internet of Things (IoT) Applications, Datasheet, Volume 2 (Book 2 of 3)	636722
Intel Atom® x6000E Series, and Intel® Pentium® and Celeron® N and J Series Processors for Internet of Things (IoT) Applications, Datasheet, Volume 2 (Book 3 of 3)	636723

2 Host Bridge Registers (D0:F0)

This chapter documents the registers in Bus: 0, Device 0, Function 0.

Table 2-1. Summary of Bus: 0 Device: 0 Function: 0 Registers (Sheet 1 of 2)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	VID_0_0_0_PCI	8086h
2h	2	DID_0_0_0_PCI	9A00h
4h	2	PCICMD_0_0_0_PCI	0006h
6h	2	PCISTS_0_0_0_PCI	0090h
8h	1	RID_0_0_0_PCI	00h
9h	1	CC_PI_0_0_0_PCI	00h
Ah	2	CC_BCC_0_0_0_PCI	0600h
Eh	1	HDR_0_0_0_PCI	00h
2Ch	2	SVID_0_0_0_PCI	0000h
2Eh	2	SID_0_0_0_PCI	0000h
34h	1	CAPPTR_0_0_0_PCI	E0h
40h	8	PXPEPBAR_0_0_0_PCI	0000000000000000h
48h	8	MCHBAR_0_0_0_PCI	0000000000000000h
50h	2	GGC_0_0_0_PCI	0500h
54h	4	DEVEN_0_0_0_PCI	0000FFFFh
58h	4	PAVPC_0_0_0_PCI	00000001h
5Ch	4	DPR_0_0_0_PCI	00000000h
60h	8	PCIEXBAR_0_0_0_PCI	0000000000000000h
68h	8	DMIBAR_0_0_0_PCI	0000000000000000h
80h	1	PAM0_0_0_0_PCI	00h
81h	1	PAM1_0_0_0_PCI	00h
82h	1	PAM2_0_0_0_PCI	00h
83h	1	PAM3_0_0_0_PCI	00h
84h	1	PAM4_0_0_0_PCI	00h
85h	1	PAM5_0_0_0_PCI	00h
86h	1	PAM6_0_0_0_PCI	00h
87h	1	LAC_0_0_0_PCI	10h
A0h	8	TOM_0_0_0_PCI	0000007FFFF00000h
A8h	8	TOUUD_0_0_0_PCI	0000000000000000h
B0h	4	BDSM_0_0_0_PCI	00000000h
B4h	4	BGSM_0_0_0_PCI	00100000h
B8h	4	TSEGMB_0_0_0_PCI	00000000h
BCh	4	TOLUD_0_0_0_PCI	00100000h

Table 2-1. Summary of Bus: 0 Device: 0 Function: 0 Registers (Sheet 2 of 2)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
C8h	2	ERRSTS_0_0_0_PCI	0000h
CAh	2	ERRCMD_0_0_0_PCI	0000h
CCh	2	SMICMD_0_0_0_PCI	0000h
CEh	2	SCICMD_0_0_0_PCI	0000h
DCh	4	SKPD_0_0_0_PCI	00000000h
E4h	4	CAPID0_A_0_0_0_PCI	00000000h
ECh	4	CAPID0_C_0_0_0_PCI	00000000h

2.1 VID_0_0_0_PCI - Offset 0h

This register combined with the Device Identification register uniquely identifies any PCI device.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:0, F:0] + 0h	8086h

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**VID:** Vendor Identification Number: PCI standard identification for Intel.

2.2 DID_0_0_0_PCI - Offset 2h

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:0, F:0] + 2h	9A00h

Bit Range	Default & Access	Field Name (ID): Description
15:8	9Ah RW/Fuse	**DID_MSB:** Device Identification Number MSB: This is the upper part of device identification.
7:0	0h RW/Fuse	**DID_SKU:** Device Identification Number SKU: This is the lower part of device identification.

2.3 PCICMD_0_0_0_PCI - Offset 4h

Since Device #0 does not physically reside on PCI_A many of the bits are not implemented.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:0, F:0] + 4h	0006h

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	**Reserved**
9	0h RO	**FB2B:** Fast Back-to-Back Enable: This bit controls whether or not the initiator can do fast back-to-back write. Since device 0 is strictly a target this bit is not implemented and is hardwired to 0. Writes to this bit position have no effect.
8	0h RW	**SERRE:** SERR Enable: This bit is a global enable bit for Device 0 SERR messaging. The CPU communicates the SERR condition by sending an SERR message over DMI to the PCH. 1: The CPU is enabled to generate SERR messages over DMI for specific Device 0 error conditions that are individually enabled in the ERRCMD and DMIUEMSK registers. The error status is reported in the ERRSTS, PCISTS, and DMIUEST registers. 0: The SERR message is not generated by the Host for Device 0. This bit only controls SERR messaging for Device 0. Other integrated devices have their own SERRE bits to control error reporting for error conditions occurring in each device. The control bits are used in a logical OR manner to enable the SERR DMI message mechanism. OPI N/A
7	0h RO	**ADSTEP:** Address/Data Stepping Enable: Address/data stepping is not implemented in the CPU, and this bit is hardwired to 0. Writes to this bit position have no effect.
6	0h RW	**PERRE:** OPI - N/A Parity Error Enable: Controls whether or not the Master Data Parity Error bit in the PCI Status register can bet set. 0: Master Data Parity Error bit in PCI Status register can NOT be set. 1: Master Data Parity Error bit in PCI Status register CAN be set.
5	0h RO	**VGASNOOP:** VGA Palette Snoop Enable: The CPU does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
4	0h RO	**MWIE:** Memory Write and Invalidate Enable: The CPU will never issue memory write and invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect.
3	0h RO	**SCE:** Special Cycle Enable: The CPU does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
2	1h RO	**BME:** Bus Master Enable: The CPU is always enabled as a initiator on the backbone. This bit is hardwired to a 1. Writes to this bit position have no effect.
1	1h RO	**MAE:** Memory Access Enable: The CPU always allows access to main memory, except when such access would violate security principles. Such exceptions are outside the scope of PCI control. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect.
0	0h RO	**IOAE:** I/O Access Enable: This bit is not implemented in the CPU and is hardwired to a 0. Writes to this bit position have no effect.

2.4 PCISTS_0_0_0_PCI - Offset 6h

This status register reports the occurrence of error events on Device 0s PCI interface. Since Device 0 does not physically reside on PCI_A many of the bits are not implemented.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:0, F:0] + 6h	0090h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/1C/V	**DPE:** Detected Parity Error: This bit is set when this Device receives a Poisoned TLP.
14	0h RW/1C/V	**SSE:** Signaled System Error: This bit is set to 1 when Device 0 generates an SERR message over DMI for any enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD, ERRCMD, and DMIUEMSK registers. Device 0 error flags are read/reset from the PCISTS, ERRSTS, or DMIUEST registers. Software clears this bit by writing a 1 to it.
13	0h RW/1C/V	**RMAS:** Received Master Abort Status: This bit is set when the CPU generates a DMI request that receives an Unsupported Request completion packet. Software clears this bit by writing a 1 to it.
12	0h RW/1C/V	**RTAS:** Received Target Abort Status: This bit is set when the CPU generates a DMI request that receives a Completer Abort completion packet. Software clears this bit by writing a 1 to it.
11	0h RO	**STAS:** Signaled Target Abort Status: The CPU will not generate a Target Abort DMI completion packet or Special Cycle. This bit is not implemented and is hardwired to a 0. Writes to this bit position have no effect.
10:9	0h RO	**DEVT:** DEVSEL Timing: These bits are hardwired to 00. Writes to these bit positions have no affect. Device 0 does not physically connect to PCI_A. These bits are set to 00 (fast decode) so that optimum DEVSEL timing for PCI_A is not limited by the Host.
8	0h RW/1C/V	**DPD:** Master Data Parity Error Detected: This bit is set when DMI received a Poisoned completion from PCH. This bit can only be set when the Parity Error Enable bit in the PCI Command register is set.
7	1h RO	**FB2B:** Fast Back-to-Back: This bit is hardwired to 1. Writes to these bit positions have no effect. Device 0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the Host.
6	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**MC66:** 66 MHz Capable: Does not apply to PCI Express. Must be hardwired to 0.
4	1h RO	**CLIST:** Capability List: This bit is hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the Capability Identification register resides.
3:0	0h RO	**Reserved**

2.5 RID_0_0_0_PCI - Offset 8h

This register contains the revision number of Device #0.

These bits are read only and writes to this register have no effect.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:0, F:0] + 8h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:4	0h RW/L	**RID_MSB:** Revision Identification Number MSB: Four MSB of RID.
3:0	0h RW/Strap	**RID:** Revision Identification Number: Four LSB of RID.

2.6 CC_PI_0_0_0_PCI - Offset 9h

This register (split from original CC) identifies a register-specific programming interface.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:0, F:0] + 9h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**PI:** Programming Interface: This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

2.7 CC_BCC_0_0_0_PCI - Offset Ah

This register (split from original CC) identifies the basic function of the device and a more specific sub-class.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:0, F:0] + Ah	0600h

Bit Range	Default & Access	Field Name (ID): Description
15:8	6h RO	**BCC:** Base Class Code: This is an 8-bit value that indicates the base class code for the Host Bridge device. This code has the value 06h, indicating a Bridge device.
7:0	0h RO	**SUBCC:** Sub-Class Code: This is an 8-bit value that indicates the category of Bridge into which the Host Bridge device falls. The code is 00h indicating a Host Bridge.

2.8 HDR_0_0_0_PCI - Offset Eh

This register identifies the header layout of the configuration space. No physical register exists at this location.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:0, F:0] + Eh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**HDR:** PCI Header: This field always returns 0 to indicate that the Host Bridge is a single function device with standard header layout. Reads and writes to this location have no effect.

2.9 SVID_0_0_0_PCI - Offset 2Ch

This value is used to identify the vendor of the subsystem.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:0, F:0] + 2Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/L	**SUBVID:** Subsystem Vendor ID: This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only. **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.SUBVIDWOS

2.10 SID_0_0_0_PCI - Offset 2Eh

This value is used to identify a particular subsystem.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:0, F:0] + 2Eh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/L	**SUBID:** Subsystem ID: This field should be programmed during BIOS initialization. After it has been written once, it becomes read only. **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.SUBIDWOS

2.11 CAPPTR_0_0_0_PCI - Offset 34h

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:0, F:0] + 34h	E0h

Bit Range	Default & Access	Field Name (ID): Description
7:0	E0h RO	**CAPPTR:** Capabilities Pointer: Pointer to the offset of the first capability ID register block. In this case, the first capability is the product-specific Capability Identifier (CAPID0).

2.12 PXPEPBAR_0_0_0_PCI - Offset 40h

This is the base address for the PCI Express Egress Port MMIO Configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the EGRESS port MMIO configuration space is disabled and must be enabled by writing a 1 to PXPEPBAREN [Dev 0, offset 40h, bit 0].

Type	Size	Offset	Default
CFG	64 bit	[B:0, D:0, F:0] + 40h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RW	**PXPEPBAR:** This field corresponds to bits 38 to 12 of the base address PCI Express Egress Port MMIO configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the PCI Express Egress Port MMIO register set.
11:1	0h RO	**Reserved**
0	0h RW	**PXPEPBAREN:** 0: PXPEPBAR is disabled and does not claim any memory 1: PXPEPBAR memory mapped accesses are claimed and decoded appropriately

2.13 MCHBAR_0_0_0_PCI - Offset 48h

This is the base address for the Host Memory Mapped Configuration space. There is no physical memory within this 32KB window that can be addressed. The 32KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the Host MMIO Memory Mapped Configuration space is disabled and must be enabled by writing a 1 to MCHBAREN [Dev 0, offset48h, bit 0].

The register space contains memory control, initialization, timing, and buffer strength registers; clocking registers; and power and thermal management registers.

Type	Size	Offset	Default
CFG	64 bit	[B:0, D:0, F:0] + 48h	0000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:16	0h RW	**MCHBAR:** This field corresponds to bits 38 to 16 of the base address Host Memory Mapped configuration space. BIOS will program this register resulting in a base address for a 64KB block of contiguous memory address space. This register ensures that a naturally aligned 64KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the Host Memory Mapped register set.
15:1	0h RO	**Reserved**
0	0h RW	**MCHBAREN:** 0: MCHBAR is disabled and does not claim any memory 1: MCHBAR memory mapped accesses are claimed and decoded appropriately

2.14 GGC_0_0_0_PCI - Offset 50h

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:0, F:0] + 50h	0500h

Bit Range	Default & Access	Field Name (ID): Description
15:8	5h RW/L	**GMS:** This field is used to select the amount of Main Memory that is preallocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. BIOS ensures that memory is preallocated only when Internal graphic is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. **Locked by:** GGC_0_0_0_PCI.GGCLCK
7:6	0h RW/L	**GGMS:** This field is used to select the amount of Main Memory that is preallocated to support the Internal Graphics Translation Table. BIOS ensures that memory is preallocated only when Internal graphic is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed. **Locked by:** GGC_0_0_0_PCI.GGCLCK
5:3	0h RO	**Reserved**
2	0h RW/L	**VAMEN:** Enables the use of the iGFX engines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h. **Locked by:** GGC_0_0_0_PCI.GGCLCK
1	0h RW/L	**IVD:** 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Memory and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 7:3 of this register) preallocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0_A[IGD] = 1) or via a register (DEVEN[3] = 0). **Locked by:** GGC_0_0_0_PCI.GGCLCK
0	0h RW/L	**GGCLCK:** When set to 1b, this bit will lock all bits in this register. **Locked by:** GGC_0_0_0_PCI.GGCLCK

2.15 DEVEN_0_0_0_PCI - Offset 54h

Allows for enabling/disabling of PCI devices and functions that are within the CPU package. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:0, F:0] + 54h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	1h RW/L	**D8EN:** 0: Bus 0 Device 8 is disabled and not visible. 1: Bus 0 Device 8 is enabled and visible. This bit will be set to 0b and remain 0b if Device 8 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.GMM_DIS
14	1h RO	**Reserved**
13	1h RO	**Reserved**
12	1h RW/L	**D9EN:** 0: Bus 0 Device 9 is disabled and not visible. 1: Bus 0 Device 9 is enabled and visible. This bit will be set to 0b and remain 0b if Device 9 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.NPK_DIS
11	1h RO	**Reserved**
10	1h RO	**Reserved**
9	1h RO	**Reserved**
8	1h RO	**Reserved**
7	1h RW/L	**D4EN:** 0: Bus 0 Device 4 is disabled and not visible. 1: Bus 0 Device 4 is enabled and visible. This bit will be set to 0b and remain 0b if Device 4 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.CDD
6	1h RO	**Reserved**
5	1h RO	**Reserved**
4	1h RW/L	**D2EN:** 0: Bus 0 Device 2 is disabled and hidden 1: Bus 0 Device 2 is enabled and visible This bit will be set to 0b and remain 0b if Device 2 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.IGD
3	1h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
2	1h RO	**Reserved**
1	1h RO	**Reserved**
0	1h RO	**D0EN:** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

2.16 PAVPC_0_0_0_PCI - Offset 58h

When locked the R/W bits are RO.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:0, F:0] + 58h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/L	**PCMBASE:** **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK
19:7	0h RO	**Reserved**
6	0h RW/L	**ASMFEN:** ASMF method enabled 0b Disabled (default). 1b Enabled. This register is locked when PAVPLCK is set. **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK
5	0h RO	**Reserved**
4	0h RW/L	**OVTATTACK:** Override of Unsolicited Connection State Attack and Terminate. 0: Disable Override. Attack Terminate allowed. 1: Enable Override. Attack Terminate disallowed. This register bit is locked when PAVPE is set. **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK
3	0h RW/L	**HVYMODSEL:** This bit is applicable only for PAVP2 operation mode, or for PAVP3 mode only if the per-application memory configuration is disabled due to the clearing of an additional enable bit 9 in the Crypto Function Control_1 register (address 0x320F0). 0: Lite Mode (Non-Serpent mode) 1: Serpent Mode When the former enable-bit is set for PAVP3 mode, this one type boot time programming has been replaced by per-application programming (through the Media Crypto Copy command). Note that PAVP2 or PAVP3 mode selection is done by programming bit 8 of the MFX_MODE - Video Mode register. **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/L	**PAVPLCK:** This bit locks all writable contents in this register when set (including itself). Only a hardware reset can unlock the register again. This lock bit needs to be set only if PAVP is enabled (bit 1 of this register is asserted). **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK
1	0h RW/L	**PAVPE:** 0: PAVP functionality is disabled. 1: PAVP functionality is enabled. This register is locked when PAVPLCK is set. **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK
0	1h RW/L	**PCME:** This field enables Protected Content Memory within Graphics Stolen Memory. This memory is the same as the WOPCM area, whose size is defined by bit 5 of this register. This register is locked when PAVPLOCK is set. A value of 0 in this field indicates that Protected Content Memory is disabled, and cannot be programmed in this manner when PAVP is enabled. A value of 1 in this field indicates that Protected Content Memory is enabled, and is the only programming option available when PAVP is enabled. For non-PAVP3 Mode, even for Lite mode configuration, this bit should be programmed to 1 and HVYMODESEL = 0). This bit should always be programmed to 1 if bits 1 and 2 (PAVPE and PAVP lock bits) are both set. With per-application Memory configuration support, the range check for the WOPCM memory area should always happen when this bit is set, regardless of Lite mode, Serpent mode, PAVP2 or PAVP3 mode programming. **Locked by:** PAVPC_0_0_0_PCI.PAVPLCK

2.17 DPR_0_0_0_PCI - Offset 5Ch

DMA protected range register.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:0, F:0] + 5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/V/L	**TOPOFDPR:** Top address + 1 of DPR. This is the base of TSEG. Bits 19:0 of the BASE reported here are 0x0_0000.
19:12	0h RO	**Reserved**
11:4	0h RW/L	**DPRSIZE:** This is the size of memory, in MB, that will be protected from DMA accesses. A value of 0x00 in this field means no additional memory is protected. The maximum amount of memory that will be protected is 255 MB. The amount of memory reported in this field will be protected from all DMA accesses, including translated CPU accesses and graphics. The top of the protected range is the BASE of TSEG -1. ***Note:*** If TSEG is not enabled, then the top of this range becomes the base of stolen graphics, or CSE stolen space or TOLUD, whichever would have been the location of TSEG, assuming it had been enabled. The DPR range works independently of any other range, including the NoDMA.TABLE protection or the PMRC checks in VTd, and is done post any VTd translation. Therefore incoming cycles are checked against this range after the VTd translation and faulted if they hit this protected range, even if they passed the VTd translation or were clean in the NoDMA lookup. All the memory checks are ORed with respect to NOT being allowed to go to memory. So if either PMRC, DPR, NoDMA table lookup, NoDMA.TABLE.PROTECT OR a VTd translation disallows the cycle, then the cycle is not allowed to go to memory. Or in other words, all the above checks must pass before a cycle is allowed to DRAM. **Locked by:** DPR_0_0_0_PCI.LOCK
3	0h RO	**Reserved**
2	0h RW/L	**EPM:** This field controls DMA accesses to the DMA Protected Range (DPR) region. 0: DPR is disabled. 1: DPR is enabled. All DMA requests accessing DPR region is blocked. HW reports the status of DPR enable/disable through the PRS field in this register. When this bit changed, one must have to wait till the status (PRS) has updated before changing it again. **Locked by:** DPR_0_0_0_PCI.LOCK
1	0h RW/V/L	**PRS:** This field indicates the status of DPR. 0: DPR protection disabled. 1: DPR protection enabled.
0	0h RW/L	**LOCK:** All bits which may be updated by SW in this register are locked down when this bit is set. **Locked by:** DPR_0_0_0_PCI.LOCK

2.18 PCIEXBAR_0_0_0_PCI - Offset 60h

Define PCIEXBAR.

Type	Size	Offset	Default
CFG	64 bit	[B:0, D:0, F:0] + 60h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:31	0h RW	**PCIEXBAR:** This field corresponds to bits 38 to 32 of the base address for PCI Express enhanced configuration space including bus segments. BIOS will program this register resulting in a base address for a contiguous memory address space. The size of the range is defined by bits [3:1] of this register. This Base address shall be assigned on a boundary consistent with the number of buses (defined by the Length field in this register) above TOLUD and still within the 39-bit addressable memory space. The address bits decoded depend on the length of the region defined by this register. The address used to access the PCI Express configuration space for a specific device can be determined as follows: PCI Express Base Address +Segment Number*256MB+ Bus Number * 1MB + Device Number * 32KB + Function Number * 4KB. This address is the beginning of the 4KB space that contains both the PCI compatible configuration space and the PCI Express extended configuration space.
30	0h RW/V	**ADMSK1024:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits [3:1] in this register.
29	0h RW/V	**ADMSK512:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits [3:1] in this register.
28	0h RW/V	**ADMSK256:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits [3:1] in this register.
27	0h RW/V	**ADMSK128:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits [3:1] in this register.
26	0h RW/V	**ADMSK64:** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits [3:1] in this register.
25:4	0h RO	**Reserved**
3:1	0h RW	**LENGTH:** This field describes the length of this region. 000: 256MB (buses 0-255). Bits 38:28 are decoded in the PCI Express Base Address Field. 001: 128MB (buses 0-127). Bits 38:27 are decoded in the PCI Express Base Address Field. 010: 64MB (buses 0-63). Bits 38:26 are decoded in the PCI Express Base Address Field. 011: 512MB (buses 0-512). Bits 38:29 are decoded in the PCI Express Base Address Field. 100: 1024MB (buses 0-1024). Bits 38:30 are decoded in the PCI Express Base Address Field. 101: 2048MB (buses 0-2048). Bits 38:31 are decoded in the PCI Express Base Address Field. 110: 4096MB (buses 0-4096). Bits 38:32 are decoded in the PCI Express Base Address Field. 111:Rreserved.
0	0h RW	**PCIEXBAREN:** PCIEX BAR Enable.

2.19 DMIBAR_0_0_0_PCI - Offset 68h

This is the base address for the Root Complex configuration space. This window of addresses contains the Root Complex Register set for the PCI Express Hierarchy associated with the Host Bridge. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the Root Complex configuration space is disabled and must be enabled by writing a 1 to DMIBAREN [Dev 0, offset 68h, bit 0].

Type	Size	Offset	Default
CFG	64 bit	[B:0, D:0, F:0] + 68h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RW	**DMIBAR:** This field corresponds to bits 38 to 12 of the base address DMI configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the DMI register set.
11:1	0h RO	**Reserved**
0	0h RW	**DMIBAREN:** 0: DMIBAR is disabled and does not claim any memory. 1: DMIBAR memory mapped accesses are claimed and decoded appropriately.

2.20 PAM0_0_0_0_PCI - Offset 80h

This register controls the read, write and shadowing attributes of the BIOS range from F_0000h to F_FFFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cache-ability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host writes accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:0, F:0] + 80h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0F_0000h to 0F_FFFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** If this bit is set, all of the PAM* registers are locked (cannot be written). **Locked by:** PAM0_0_0_0_PCI.LOCK

2.21 PAM1_0_0_0_PCI - Offset 81h

This register controls the read, write and shadowing attributes of the BIOS range from C_0000h to C_7FFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cache-ability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host writes accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:0, F:0] + 81h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0C_4000h to 0C_7FFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:2	0h RO	**Reserved**
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0C0000h to 0C3FFFh. 00: DRAM Disabled. All reads are sent to DRAM. All writes are forwarded to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

2.22 PAM2_0_0_0_PCI - Offset 82h

This register controls the read, write and shadowing attributes of the BIOS range from C_8000h to C_FFFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cache-ability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host writes accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:0, F:0] + 82h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0CC000h to 0CFFFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:2	0h RO	**Reserved**
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0C8000h to 0CBFFFh. 00: DRAM Disabled. All reads are sent to DRAM. All writes are forwarded to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

2.23 PAM3_0_0_0_PCI - Offset 83h

This register controls the read, write and shadowing attributes of the BIOS range from D0000h to D7FFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cache-ability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host writes accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:0, F:0] + 83h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0D4000h to 0D7FFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:2	0h RO	**Reserved**
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0D0000h to 0D3FFFh. 00: DRAM Disabled. All reads are sent to DRAM. All writes are forwarded to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

2.24 PAM4_0_0_0_PCI - Offset 84h

This register controls the read, write and shadowing attributes of the BIOS range from D8000h to DFFFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cache-ability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host writes accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:0, F:0] + 84h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0DC000h to 0DFFFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:2	0h RO	**Reserved**
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0D8000h to 0DBFFFh. 00: DRAM Disabled. All reads are sent to DRAM. All writes are forwarded to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

2.25 PAM5_0_0_0_PCI - Offset 85h

This register controls the read, write and shadowing attributes of the BIOS range from E_0000h to E_7FFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cache-ability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host writes accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:0, F:0] + 85h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:2	0h RO	**Reserved**
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh. 00: DRAM Disabled. All reads are sent to DRAM. All writes are forwarded to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

2.26 PAM6_0_0_0_PCI - Offset 86h

This register controls the read, write and shadowing attributes of the BIOS range from E_8000h to E_FFFFh. The Uncore allows programmable memory attributes on 13 legacy memory segments of various sizes in the 768KB to 1MB address range. Seven Programmable Attribute Map (PAM) registers are used to support these features. Cache-ability of these areas is controlled via the MTRR register in the core.

Two bits are used to specify memory attributes for each memory segment. These bits apply to host accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE=1, the host read accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when RE=0, the host read accesses are directed to DMI.

WE - Write Enable. When WE=1, the host writes accesses to the corresponding memory segment are claimed by the Uncore and directed to main memory. Conversely, when WE=0, the host read accesses are directed to DMI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write or Disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:0, F:0] + 86h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:6	0h RO	**Reserved**
5:4	0h RW/L	**HIENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0EC000h to 0EFFFFh. 00: DRAM Disabled. All accesses are directed to DMI. 01: Read Only. All reads are sent to DRAM, all writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM, all reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK
3:2	0h RO	**Reserved**
1:0	0h RW/L	**LOENABLE:** This field controls the steering of read and write cycles that address the BIOS area from 0E8000h to 0EBFFFh. 00: DRAM Disabled. All reads are sent to DRAM. All writes are forwarded to DMI. 01: Read Only. All reads are sent to DRAM. All writes are forwarded to DMI. 10: Write Only. All writes are sent to DRAM. All reads are serviced by DMI. 11: Normal DRAM Operation. All reads and writes are serviced by DRAM. **Locked by:** PAM0_0_0_0_PCI.LOCK

2.27 LAC_0_0_0_PCI - Offset 87h

This 8-bit register controls steering of MDA cycles and a fixed DRAM hole from 15-16MB.

There can only be at most one MDA device in the system.

Note: Any configurations including Device 1 are invalid since the compute die does not implement a PCI Express port.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:0, F:0] + 87h	10h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RW	**HEN:** This field enables a memory hole in DRAM space. The DRAM that lies behind this space is not remapped. 0: No memory hole. 1: Memory hole from 15MB to 16MB.
6:5	0h RO	**Reserved**
4	1h RW	**MDAPCIE:** This bit works with the VGA Enable bits in the BCTRL register of Non PEG devices to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should be set to 1 by default. It is assumed that these devices will not need to support legacy MDA graphics. However this single bit is added just to support this rare case of using MDA over these devices. The behavior of this bit field is identical to bits [3:0].
3	0h RW	**MDAP60:** This bit works with the VGA Enable bits in the BCTRL register of Device 1 Function 2 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1 function 2 VGA Enable bit is not set. If device 1 function 2 VGA enable bit is not set, then accesses to IO address range x3BCh-x3BFh remain on the backbone. If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh-x3BFh are forwarded to PCI Express through device 1 function 2 if the address is within the corresponding IOBASE and IOLIMIT, otherwise they remain on the backbone. MDA resources are defined as the following: Memory: 0B0000h - 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will remain on the backbone even if the reference also includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: VGAEN MDAP Description 0 0 All References to MDA and VGA space are not claimed by Device 1 Function 2. 0 1 Illegal combination. 1 0 All VGA and MDA references are routed to PCI Express Graphics Attach device 1 function 2. 1 1 All VGA references are routed to PCI Express Graphics Attach device 1 function 2. MDA references are not claimed by device 1 function 2. VGA and MDA memory cycles can only be routed across PEG12 when MAE (PCICMD12[1]) is set. VGA and MDA I/O cycles can only be routed across PEG12 if IOAE (PCICMD12[0]) is set.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**MDAP12:** This bit works with the VGA Enable bits in the BCTRL register of Device 1 Function 2 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1 function 2 VGA Enable bit is not set. If device 1 function 2 VGA enable bit is not set, then accesses to IO address range x3BCh-x3BFh remain on the backbone. If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh-x3BFh are forwarded to PCI Express through device 1 function 2 if the address is within the corresponding IOBASE and IOLIMIT, otherwise they remain on the backbone. MDA resources are defined as the following: Memory: 0B0000h - 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will remain on the backbone even if the reference also includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: VGAEN MDAP Description 0 0 All References to MDA and VGA space are not claimed by Device 1 Function 2. 0 1 Illegal combination. 1 0 All VGA and MDA references are routed to PCI Express Graphics Attach device 1 function 2. 1 1 All VGA references are routed to PCI Express Graphics Attach device 1 function 2. MDA references are not claimed by device 1 function 2. VGA and MDA memory cycles can only be routed across PEG12 when MAE (PCICMD12[1]) is set. VGA and MDA I/O cycles can only be routed across PEG12 if IOAE (PCICMD12[0]) is set.
1	0h RW	**MDAP11:** This bit works with the VGA Enable bits in the BCTRL register of Device 1 Function 1 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1 function 1 VGA Enable bit is not set. If device 1 function 1 VGA enable bit is not set, then accesses to IO address range x3BCh-x3BFh remain on the backbone. If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh-x3BFh are forwarded to PCI Express through device 1 function 1 if the address is within the corresponding IOBASE and IOLIMIT, otherwise they remain on the backbone. MDA resources are defined as the following: Memory: 0B0000h - 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will remain on the backbone even if the reference also includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: VGAEN MDAP Description 0 0 All References to MDA and VGA space are not claimed by Device 1 Function 1. 0 1 Illegal combination. 1 0 All VGA and MDA references are routed to PCI Express Graphics Attach device 1 function 1. 1 1 All VGA references are routed to PCI Express Graphics Attach device 1 function 1. MDA references are not claimed by device 1 function 1. VGA and MDA memory cycles can only be routed across PEG11 when MAE (PCICMD11[1]) is set. VGA and MDA I/O cycles can only be routed across PEG11 if IOAE (PCICMD11[0]) is set.

Bit Range	Default & Access	Field Name (ID): Description
0	0h RW	**MDAP10:** This bit works with the VGA Enable bits in the BCTRL register of Device 1 Function 0 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1 function 0 VGA Enable bit is not set. If device 1 function 0 VGA enable bit is not set, then accesses to IO address range x3BCh-x3BFh remain on the backbone. If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh-x3BFh are forwarded to PCI Express through device 1 function 0 if the address is within the corresponding IOBASE and IOLIMIT, otherwise they remain on the backbone. MDA resources are defined as the following: Memory: 0B0000h - 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will remain on the backbone even if the reference also includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: VGAEN MDAP Description 0 0 All References to MDA and VGA space are not claimed by Device 1 Function 0. 0 1 Illegal combination. 1 0 All VGA and MDA references are routed to PCI Express Graphics Attach device 1 function 0. 1 1 All VGA references are routed to PCI Express Graphics Attach device 1 function 0. MDA references are not claimed by device 1 function 0. VGA and MDA memory cycles can only be routed across PEG10 when MAE (PCICMD10[1]) is set. VGA and MDA I/O cycles can only be routed across PEG10 if IOAE (PCICMD10[0]) is set.

2.28 TOM_0_0_0_PCI - Offset A0h

This Register contains the size of physical memory. BIOS determines the memory size reported to the OS using this Register.

Type	Size	Offset	Default
CFG	64 bit	[B:0, D:0, F:0] + A0h	0000007FFFF00000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
38:20	7FFFFh RW/L	**TOM:** This register reflects the total amount of populated physical memory. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory mapped IO). These bits correspond to address bits 38:20 (1MB granularity). Bits 19:0 are assumed to be 0. **Locked by:** TOM_0_0_0_PCI.LOCK
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writable settings in this register, including itself. **Locked by:** TOM_0_0_0_PCI.LOCK

2.29 TOUUD_0_0_0_PCI - Offset A8h

This 64 bit register defines the Top of Upper Usable DRAM.

Configuration software must set this value to TOM minus all CSE stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit + 1byte, 1MB aligned, since reclaim limit is 1MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4GB.

BIOS Restriction: Minimum value for TOUUD is 4GB.

Type	Size	Offset	Default
CFG	64 bit	[B:0, D:0, F:0] + A8h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:20	0h RW/L	**TOUUD:** This register contains bits 38 to 20 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system. Configuration software must set this value to TOM minus all CSE stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit 1MB aligned since reclaim limit + 1byte is 1MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4GB. **Locked by:** TOUUD_0_0_0_PCI.LOCK
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writable settings in this register, including itself. **Locked by:** TOUUD_0_0_0_PCI.LOCK

2.30 BDSM_0_0_0_PCI - Offset B0h

This register contains the base address of graphics data stolen DRAM memory. BIOS determines the base of graphics data stolen memory by subtracting the graphics data stolen memory size (PCI Device 0 offset 52 bits 7:4) from TOLUD (PCI Device 0 offset BC bits 31:20).

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:0, F:0] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/L	**BDSM:** This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0 offset 50 bits 15:8) from TOLUD (PCI Device 0 offset BC bits 31:20). **Locked by:** BDSM_0_0_0_PCI.LOCK
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writable settings in this register, including itself. **Locked by:** BDSM_0_0_0_PCI.LOCK

2.31 BGSM_0_0_0_PCI - Offset B4h

This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 9:8) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20).

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:0, F:0] + B4h	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	1h RW/L	**BGSM:** This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 50 bits 7:6) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20). **Locked by:** BGSM_0_0_0_PCI.LOCK
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writable settings in this register, including itself. **Locked by:** BGSM_0_0_0_PCI.LOCK

2.32 TSEGMB_0_0_0_PCI - Offset B8h

This register contains the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory which must be at or below Graphics Base of GTT Stolen Memory (PCI Device 0 Offset B4 bits 31:20).

***Note*:** BIOS must program TSEGMB to a 8MB naturally aligned boundary.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:0, F:0] + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW/L	**TSEGMB:** This register contains the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory which must be at or below Graphics Base of GTT Stolen Memory (PCI Device 0 Offset B4 bits 31:20). BIOS must program the value of TSEGMB to be the same as BGSM when TSEG is disabled. **Locked by:** TSEGMB_0_0_0_PCI.LOCK
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writable settings in this register, including itself. **Locked by:** TSEGMB_0_0_0_PCI.LOCK

2.33 TOLUD_0_0_0_PCI - Offset BCh

This 32 bit register defines the Top of Low Usable DRAM. TSEG, GTT Graphics memory and Graphics Stolen Memory are within the DRAM space defined. From the top, the Host optionally claims 1 to 64MBs of DRAM for internal graphics if enabled, 1or 2MB of DRAM for GTT Graphics Stolen Memory (if enabled) and 1, 2, or 8 MB of DRAM for TSEG if enabled.

Programming Example:

C1DRB3 is set to 4GB.

TSEG is enabled and TSEG size is set to 1MB.

Internal Graphics is enabled, and Graphics Mode Select is set to 32MB.

GTT Graphics Stolen Memory Size set to 2MB.

BIOS knows the OS requires 1G of PCI space.

BIOS also knows the range from 0_FEC0_0000h to 0_FFFF_FFFFh is not usable by the system. This 20MB range at the very top of addressable memory space is lost to APIC.

According to the above equation, TOLUD is originally calculated to: 4GB = 1_0000_0000h.

The system memory requirements are: 4GB (max addressable space) - 1GB PCI space) - 35MB (lost memory) = 3GB - 35MB (minimum granularity) = 0_ECB0_0000h.

Since 0_ECB0_0000h (PCI and other system requirements) is less than 1_0000_0000h, TOLUD should be programmed to ECBh.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:0, F:0] + BCh	00100000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	1h RW/L	**TOLUD:** This register contains bits 31 to 20 of an address one byte above the maximum DRAM memory below 4G that is usable by the operating system. Address bits 31 down to 20 programmed to 01h implies a minimum memory size of 1MB. Configuration software must set this value to the smaller of the following 2 choices: maximum amount memory in the system minus CSE stolen memory plus one byte or the minimum address allocated for PCI memory. Address bits 19:0 are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register. The Top of Low Usable DRAM is the lowest address above both Graphics Stolen memory and TSEG. BIOS determines the base of Graphics Stolen Memory by subtracting the Graphics Stolen Memory Size from TOLUD and further decrements by TSEG size to determine base of TSEG. This register must be 1MB aligned when reclaim is enabled. **Locked by:** TOLUD_0_0_0_PCI.LOCK
19:1	0h RO	**Reserved**
0	0h RW/L	**LOCK:** This bit will lock all writable settings in this register, including itself. **Locked by:** TOLUD_0_0_0_PCI.LOCK

2.34 ERRSTS_0_0_0_PCI - Offset C8h

This register is used to report various error conditions via the SERR DMI messaging mechanism. An SERR DMI message is generated on a zero to one transition of any of these flags (if enabled by the ERRCMD and PCICMD registers).

These bits are set regardless of whether or not the SERR is enabled and generated. After the error processing is complete, the error logging mechanism can be unlocked by clearing the appropriate status bit by software writing a 1 to it.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:0, F:0] + C8h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	0h RW/1C/V/P	**IBECC_UC:** When this bit is set to 1 it indicates an uncorrectable error occurred in IBECC.
6	0h RW/1C/V/P	**IBECC_COR:** When this bit is set to 1 it indicates a correctable error occurred in IBECC.
5	0h RW/1C/V/P	**FMUR:** When this bit is set to 1 it indicates an unsupported request event occurred in FMHC.
4	0h RW/1C/V/P	**FMCA:** When this bit is set to 1 it indicates a completer abort occurred in FMHC.
3	0h RW/1C/V/P	**FMIAN:** When this bit is set to 1 FMI Asynchronous Notification error event with Media dead or Health log critical notification has occurred in FMHC.
2	0h RW/1C/V/P	**FMITHERMERR:** When this bit is set to 1 it indicates a thermal event occurred in FMHC.
1	0h RW/1C/V/P	**Reserved**
0	0h RW/1C/V/P	**Reserved**

2.35 ERRCMD_0_0_0_PCI - Offset CAh

This register controls the Host Bridge responses to various system errors. Since the Host Bridge does not have an SERRB signal, SERR messages are passed from the CPU to the PCH over DMI.

When a bit in this register is set, a SERR message will be generated on DMI whenever the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device #0 via the PCI Command register.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:0, F:0] + CAh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	0h RW	**IBECC_UC:** SERR on IBECC Uncorrectable error event: 1: The Host Bridge generates an SERR special cycle over DMI when IBECC reports uncorrectable error. 0: Reporting of this condition via SERR messaging is disabled.
6	0h RW	**IBECC_COR:** SERR on IBECC correctable error event: 1: The Host Bridge generates an SERR special cycle over DMI when IBECC reports correctable error. 0: Reporting of this condition via SERR messaging is disabled.
5	0h RW	**FMUR:** SERR on FMHC unsupported request event: 1: The Host Bridge generates an SERR special cycle over DMI when FMHC reports an unsupported request event. 0: Reporting of this condition via SERR messaging is disabled.
4	0h RW	**FMCA:** SERR on FMHC CA event: 1: The Host Bridge generates an SERR special cycle over DMI when FMHC reports a CA event. 0: Reporting of this condition via SERR messaging is disabled.
3	0h RW	**FMIAN:** SERR on FMI Asynchronous Notification error event: 1: The Host Bridge generates an SERR special cycle over DMI when FMHC reports a Asynchronous Notification error event with Media dead or Health log critical notification. 0: Reporting of this condition via SERR messaging is disabled.
2	0h RW	**FMITHERMERR:** SERR on FMHC thermal event: 1: The Host Bridge generates an SERR special cycle over DMI when FMHC reports a thermal event. 0: Reporting of this condition via SERR messaging is disabled.
1	0h RW	**Reserved**
0	0h RW	**Reserved**

2.36 SMICMD_0_0_0_PCI - Offset CCh

This register enables various errors to generate an SMI DMI special cycle. When an error flag is set in the ERRSTS register, it can generate an SERR, SMI, or SCI DMI special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers, respectively. Note that one and only one message type can be enabled.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:0, F:0] + CCh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	0h RW	**IBECC_UC:** SMI on IBECC Uncorrectable error event: 1: The Host Bridge generates an SMI special cycle over DMI when IBECC reports uncorrectable error. 0: Reporting of this condition via SMI messaging is disabled.
6	0h RW	**IBECC_COR:** SMI on IBECC correctable error event: 1: The Host Bridge generates an SMI special cycle over DMI when IBECC reports correctable error. 0: Reporting of this condition via SMI messaging is disabled.
5	0h RW	**FMUR:** SMI on FMHC unsupported request event: 1: The Host Bridge generates an SMI special cycle over DMI when FMHC reports an unsupported request event. 0: Reporting of this condition via SMI messaging is disabled.
4	0h RW	**FMCA:** SMI on FMHC CA event: 1: The Host Bridge generates an SMI special cycle over DMI when FMHC reports a CA event. 0: Reporting of this condition via SMI messaging is disabled.
3	0h RW	**FMIAN:** SMI on FMI Asynchronous Notification error event: 1: The Host Bridge generates an SMI special cycle over DMI when FMHC reports a Asynchronous Notification error event with Media dead or Health log critical notification. 0: Reporting of this condition via SMI messaging is disabled.
2	0h RW	**FMITHERMERR:** SMI on FMHC thermal event: 1: The Host Bridge generates an SMI special cycle over DMI when FMHC reports a thermal event. 0: Reporting of this condition via SMI messaging is disabled.
1	0h RW	**Reserved**
0	0h RW	**Reserved**

2.37 SCICMD_0_0_0_PCI - Offset CEh

This register enables various errors to generate an SMI DMI special cycle. When an error flag is set in the ERRSTS register, it can generate an SERR, SMI, or SCI DMI special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers, respectively. Note that one and only one message type can be enabled.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:0, F:0] + CEh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**Reserved**
7	0h RW	**IBECC_UC:** SCI on IBECC Uncorrectable error event: 1: The Host Bridge generates an SCI special cycle over DMI when IBECC reports uncorrectable error. 0: Reporting of this condition via SCI messaging is disabled.
6	0h RW	**IBECC_COR:** SCI on IBECC correctable error event: 1: The Host Bridge generates an SCI special cycle over DMI when IBECC reports correctable error. 0: Reporting of this condition via SCI messaging is disabled.
5	0h RW	**FMUR:** SCI on FMHC unsupported request event: 1: The Host Bridge generates an SCI special cycle over DMI when FMHC reports an unsupported request event. 0: Reporting of this condition via SCI messaging is disabled.
4	0h RW	**FMCA:** SCI on FMHC CA event: 1: The Host Bridge generates an SCI special cycle over DMI when FMHC reports a CA event. 0: Reporting of this condition via SCI messaging is disabled.
3	0h RW	**FMIAN:** SCI on FMI Asynchronous Notification error event: 1: The Host Bridge generates an SCI special cycle over DMI when FMHC reports a Asynchronous Notification error event with Media dead or Health log critical notification. 0: Reporting of this condition via SCI messaging is disabled.
2	0h RW	**FMITHERMERR:** SCI on FMHC thermal event: 1: The Host Bridge generates an SCI special cycle over DMI when FMHC reports a thermal event. 0: Reporting of this condition via SCI messaging is disabled.
1	0h RW	**Reserved**
0	0h RW	**Reserved**

2.38 SKPD_0_0_0_PCI - Offset DCh

This register holds 32 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:0, F:0] + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**SKPD:** 1 DWORD of data storage.

2.39 CAPID0_A_0_0_0_PCI - Offset E4h

Control of bits in this register are only required for customer visible SKU differentiation.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:0, F:0] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RO	**Reserved**
29	0h RO	**Reserved**
28	0h RO	**Reserved**
27	0h RW/L	**PELWUD:** 0: Link width upconfig is supported. The CPU advertises upconfig capability using the data rate symbol in its TS2 training ordered sets during Configuration.Complete. The CPU responds to link width upconfigs initiated by the downstream device. 1: Link width upconfig is NOT supported. The CPU does not advertise upconfig capability using the data rate field in TS2 training ordered sets during Configuration.Complete. The CPU does not respond to link width upconfigs initiated by the downstream device.
26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/L	**VTDD:** 0: Enable VTd. 1: Disable VTd.
22	0h RO	**Reserved**
21	0h RO	**Reserved**
20:19	0h RW/L	**DDRSZ:** This field defines the maximum allowed memory size per channel. 00b Unlimited (64GB per channel). 01b Maximum 8GB per channel. 10b Maximum 4GB per channel. 11b Maximum 2GB per channel.

Bit Range	Default & Access	Field Name (ID): Description
18	0h RO	**Reserved**
17	0h RW/L	**D1NM:** 0: Part is capable of supporting 1n mode timings on the DDR interface. 1: Part is not capable of supporting 1n mode. Only supported timings are 2n or greater.
16	0h RO	**Reserved**
15	0h RW/L	**CDD:** 0: Camarillo Device enabled. 1: Camarillo Device disabled.
14	0h RO	**Reserved**
13	0h RW/L	**X2APIC_EN:** Extended Interrupt Mode. 0b: Hardware does not support Extended APIC mode. 1b: Hardware supports Extended APIC mode.
12	0h RW/L	**PDCD:** 0: Capable of Dual Channels. 1: Not Capable of Dual Channel - only single channel capable.
11	0h RW/L	**IGD:** 0: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the CPU. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2. A selected amount of Graphics Memory space is preallocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is preallocated above TSEG Memory. 1: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on to DMI. In addition, all clocks to internal graphics logic are turned off. DEVEN [4:3] (Device 0, offset 54h) have no meaning. Device 2 Functions 0 and 1 are disabled and hidden.
10	0h RW/L	**DID0OE:** 0b Disable ability to override DID0 - For production. 1b Enable ability to override DID - For debug and samples only.
9:8	0h RO	**Reserved**
7:4	0h RW/L	**CRID:** Compatibility Rev ID: PCODE will update this field with the value of FUSE_CRID.
3	0h RO	**Reserved**
2	0h RO	**Reserved**
1	0h RO	**Reserved**
0	0h RO	**Reserved**

2.40 CAPID0_C_0_0_0_PCI - Offset ECh

Control of bits in this register is only required for customer visible SKU differentiation.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:0, F:0] + ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW/L	**Reserved**
27:23	0h RW/L	**MAX_DATA_RATE_DDR4:** DDR4 Maximum Frequency Capability in 266Mhz units. This value is relevant only when CAPID0_A_0_0_0_PCI.DDR_OVERCLOCK is zero (DDR overclocking is not supported). 0: Unlimited. 1-31: multiples of 266MHz.
22	0h RW/L	**DDR4_EN:** DDR4 supported. 0: DDR4 is not supported. 1: DDR4 is supported.
21:17	0h RW/L	**MAX_DATA_RATE_LPDDR4:** DDR4 Maximum Frequency Capability in 266Mhz units. This value is relevant only when CAPID0_A_0_0_0_PCI.DDR_OVERCLOCK is zero (DDR overclocking is not supported). 0: Unlimited 1-31: multiples of 266MHz
16	0h RW/L	**LPDDR4_EN:** Allow LPDDR4 operation.
15	0h RW/L	**IBECC_EN:** IBECC1 on/off mode of work. 0 - IBECC1 is off. 1 - IBECC1 is on.
14	0h RW/L	**QCLK_GV_DIS:** 0: Qclk GV Enable. 1: Qclk GV Disable.
13:10	0h RW/L	**FDSKUFP:** Reserved.
9	0h RW/L	**SE_DIS:** 0: **Reserved** 1: Intel SGX is not supported.
8:7	0h RW/L	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
6	0h RW/L	**IDD:** Specifies whether the Internal Display is Disabled. 0 - Intel Display is enabled. 1 - Intel Display is disabled.
5	0h RW/L	**DISPLAY_PIPE3:** 0 - 3rd Display is disabled. 1 - 3rd Display is enabled.
4:0	0h RW/L	**MAX_DATA_RATE_AT_GEAR1:** This field reports the maximum Data Rate of the memory controller in GEAR 1 in 266Mhz units. This value is relevant only when CAPID0_A_0_0_0_PCI.DDR_OVERCLOCK is zero (DDR overclocking is not supported). 0: Unlimited. 1-31: Multiples of 266MHz.

3 Host Memory Mapped Configuration Space (MCHBAR) Registers

This chapter documents the MCHBAR registers. The MCHBAR consists of memory controller and power management registers.

Base address of these registers is defined in the MCHBAR_0_0_0_PCI register in Bus: 0, Device: 0, Function: 0.

The MCHBAR exposes 3 sets of memory controller registers channel 0, channel 1 as well broadcast.

- Channel 0 offset range: 4000h-43FFh
  (**Note**: Fields related to Ranks 3:2 should be ignored.)
- Channel 1 offset range: 4400h-47FFh
- Broadcast offset range: 4C00h-4FFFh

Memory Controller Broadcast register behavior is to write to all channels and read from channel 0.

Note: For brevity, only channel 0 is documented. For channel 1 registers add 0x0400, for broadcast add 0x0C00 to the channel 0 register offset

These registers apply to all processors.

Table 3-1. Summary of MCHBAR Registers (Sheet 1 of 4)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4000h	4	TC_PRE_0_0_0_MCHBAR	18863808h
4004h	4	TC_ACT_0_0_0_MCHBAR	01088410h
400Ch	4	TC_RDRD_0_0_0_MCHBAR	04040404h
4010h	4	TC_RDWR_0_0_0_MCHBAR	04040404h
4014h	4	TC_WRRD_0_0_0_MCHBAR	04040404h
4018h	4	TC_WRWR_0_0_0_MCHBAR	04040404h
4020h	8	SC_ROUNDTRIP_LATENCY_0_0_0_MCHBAR	1919191919191919h
4050h	8	TC_PWRDN_0_0_0_MCHBAR	0000000404440404h
4070h	8	TC_ODT_0_0_0_MCHBAR	0000000001850000h
4080h	4	SC_ODT_MATRIX_0_0_0_MCHBAR	00000000h
4088h	8	SC_GS_CFG_0_0_0_MCHBAR	0000000000001020h
4198h	4	SPID_LOW_POWER_CTL_0_0_0_MCHBAR	F8141442h
4224h	4	LPDDR_MR4_RANK_TEMPERATURE_0_0_0_MCHBAR	03030303h
4228h	4	DDR4_MPR_RANK_TEMPERATURE_0_0_0_MCHBAR	01010101h
4238h	4	TC_RFP_0_0_0_MCHBAR	4602980Fh
423Ch	4	TC_RFTP_0_0_0_MCHBAR	00B41004h

Table 3-1. Summary of MCHBAR Registers (Sheet 2 of 4)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
4240h	4	TC_SRFTP_0_0_0_MCHBAR	00000200h
4244h	4	MC_REFRESH_STAGGER_0_0_0_MCHBAR	00000000h
4248h	4	TC_ZQCAL_0_0_0_MCHBAR	32010000h
4254h	4	MC_INIT_STATE_0_0_0_MCHBAR	0000000Fh
4260h	4	PM_DIMM_IDLE_ENERGY_0_0_0_MCHBAR	00000000h
4264h	4	PM_DIMM_PD_ENERGY_0_0_0_MCHBAR	00000000h
4268h	4	PM_DIMM_ACT_ENERGY_0_0_0_MCHBAR	00000000h
426Ch	4	PM_DIMM_RD_ENERGY_0_0_0_MCHBAR	00000000h
4270h	4	PM_DIMM_WR_ENERGY_0_0_0_MCHBAR	00000000h
4278h	4	SC_WR_DELAY_0_0_0_MCHBAR	00000003h
4288h	4	SC_PBR_0_0_0_MCHBAR	0000F011h
4294h	4	TC_LPDDR4_MISC_0_0_0_MCHBAR	00000056h
42C4h	4	TC_SREXITTP_0_0_0_MCHBAR	00000000h
43FCh	4	MCMNTS_SPARE_0_0_0_MCHBAR	00000000h
5000h	4	MAD_INTER_CHANNEL_0_0_0_MCHBAR	00000000h
5004h	4	MAD_INTRA_CH0_0_0_0_MCHBAR	00000000h
5008h	4	MAD_INTRA_CH1_0_0_0_MCHBAR	00000000h
500Ch	4	MAD_DIMM_CH0_0_0_0_MCHBAR	00000000h
5010h	4	MAD_DIMM_CH1_0_0_0_MCHBAR	00000000h
5024h	4	CHANNEL_HASH_0_0_0_MCHBAR	00000000h
5028h	4	CHANNEL_EHASH_0_0_0_MCHBAR	00000000h
5040h	4	PWM_GT_REQCOUNT_0_0_0_MCHBAR	00000000h
5044h	4	PWM_IA_REQCOUNT_0_0_0_MCHBAR	00000000h
5048h	4	PWM_IO_REQCOUNT_0_0_0_MCHBAR	00000000h
5050h	4	PWM_RDDATA_COUNT_0_0_0_MCHBAR	00000000h
5054h	4	PWM_WRDATA_COUNT_0_0_0_MCHBAR	00000000h
5058h	4	PWM_COMMAND_COUNT_0_0_0_MCHBAR	00000000h
5060h	4	PM_SREF_CONFIG_0_0_0_MCHBAR	00000200h
5090h	8	REMAPBASE_0_0_0_MCHBAR	0000007FFFF00000h
5098h	8	REMAPLIMIT_0_0_0_MCHBAR	0000000000000000h
5400h	8	GFXVTBAR_0_0_0_MCHBAR_NCU	0000000000000000h
5410h	8	VTDPVC0BAR_0_0_0_MCHBAR_NCU	0000000000000000h
5824h	4	BIOS_POST_CODE_0_0_0_MCHBAR_PCU	00000000h
5920h	4	PRIP_TURBO_PLCY_0_0_0_MCHBAR_PCU	00000000h
5924h	4	SECP_TURBO_PLCY_0_0_0_MCHBAR_PCU	00000010h
5928h	4	PRIP_NRG_STTS_0_0_0_MCHBAR_PCU	00000000h
592Ch	4	SECP_NRG_STTS_0_0_0_MCHBAR_PCU	00000000h
5968h	4	PP0_EFFICIENT_CYCLES_0_0_0_MCHBAR_PCU	00000000h
596Ch	4	PP0_THREAD_ACTIVITY_0_0_0_MCHBAR_PCU	00000000h

Table 3-1. Summary of MCHBAR Registers (Sheet 3 of 4)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
597Ch	4	PP0_TEMPERATURE_0_0_0_MCHBAR_PCU	00000000h
599Ch	4	TEMPERATURE_TARGET_0_0_0_MCHBAR_PCU	00000000h
59A0	8	PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU	0000000000000000h
59C0h	4	THERM_STATUS_GT_0_0_0_MCHBAR_PCU	08000000h
59C4h	4	THERM_INTERRUPT_GT_0_0_0_MCHBAR_PCU	00000000h
5DA0h	4	BIOS_MAILBOX_DATA_0_0_0_MCHBAR_PCU	00000000h
5DA4h	4	BIOS_MAILBOX_INTERFACE_0_0_0_MCHBAR_PCU	00000000h
5E00h	4	MC_BIOS_REQ_0_0_0_MCHBAR_PCU	00000000h
5F58h	4	OC_STATUS_0_0_0_MCHBAR_PCU	00000000h
5F60h	4	PACKAGE_SW_PL4_OFFSET_0_0_0_MCHBAR_PCU	00000000h
5F68h	8	BCLK_FREQ_0_0_0_MCHBAR	0000000000000000h
7110h	8	REGBAR_0_0_0_MCHBAR_IMPH	0000000000000000h
DC00h	4	In-Band ECC Activate (IBECC_ACTIVATE)	00000000h
DC0Ch	4	IBECC Protected Address Range (IBECC_PROTECT_ADDR_RANGE_0)	00000000h
DC10h	4	IBECC Protected Address Range (IBECC_PROTECT_ADDR_RANGE_1)	00000000h
DC14h	4	IBECC Protected Address Range (IBECC_PROTECT_ADDR_RANGE_2)	00000000h
DC18h	4	IBECC Protected Address Range (IBECC_PROTECT_ADDR_RANGE_3)	00000000h
DC1Ch	4	IBECC Protected Address Range (IBECC_PROTECT_ADDR_RANGE_4)	00000000h
DC20h	4	IBECC Protected Address Range (IBECC_PROTECT_ADDR_RANGE_5)	00000000h
DC24h	4	IBECC Protected Address Range (IBECC_PROTECT_ADDR_RANGE_6)	00000000h
DC28h	4	IBECC Protected Address Range (IBECC_PROTECT_ADDR_RANGE_7)	00000000h
DC2Ch	4	ECC Data Storage Address (ECC_STORAGE_ADDR)	00000000h
DD20h	8	ECC Protected VC0 Read Data Request Count (ECC_VC0_RD_REQCOUNT)	0000000000000000h
DD28h	8	ECC Protected VC1 Read Data Request Count (ECC_VC1_RD_REQCOUNT)	0000000000000000h
DD30h	8	ECC Protected VC0 Write Data Request Count (ECC_VC0_WR_REQCOUNT)	0000000000000000h
DD38h	8	ECC Protected VC1 Write Data Request Count (ECC_VC1_WR_REQCOUNT)	0000000000000000h
DD40h	8	Unprotected VC0 Read Request Count (NOECC_VC0_RD_REQCOUNT)	0000000000000000h
DD48h	8	Unprotected VC1 Read Request Count (NOECC_VC1_RD_REQCOUNT)	0000000000000000h
DD50h	8	Unprotected VC0 Write Request Count (NOECC_VC0_WR_REQCOUNT)	0000000000000000h

Table 3-1. Summary of MCHBAR Registers (Sheet 4 of 4)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
DD58h	8	Unprotected VC1 Write Request Count (NOECC_VC1_WR_REQCOUNT)	0000000000000000h
DD70h	8	ECC Error Log (ECC_ERROR_LOG)	0000000000000000h
DD78h	8	Parity Error Log (PARITY_ERR_LOG)	0000000000000000h
DD80h	8	ECC Injection Address Mask (ECC_INJ_ADDR_MASK)	0000000000000000h
DD88h	8	ECC Error Injection Address Base (ECC_INJ_ADDR_BASE)	0000000000000000h
DD90h	4	Parity Error Injection (PARITY_ERR_INJ)	00000000h
DD98h	4	IBECC ECC Error Injection Control (ECC_INJ_CONTROL)	00000000h
DDC0h	8	Request Counter (ECC_VC0_SYND_RD_REQCOUNT)	0000000000000000h
DDC8h	8	Request Counter (ECC_VC1_SYND_RD_REQCOUNT)	0000000000000000h
DDD0h	8	Request Counter (ECC_VC0_SYND_WR_REQCOUNT)	0000000000000000h
DDD8h	8	Request Counter (ECC_VC1_SYND_WR_REQCOUNT)	0000000000000000h

3.1 TC_PRE_0_0_0_MCHBAR - Offset 4000h

DDR timing constraints related to PRE commands.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4000h	18863808h

Bit Range	Default & Access	Field Name (ID): Description
31:24	18h RW/L	**TWRPRE:** Holds DDR timing parameter tWRPRE. WR to PRE same bank minimum delay in tCK cycles. Supported range is 18-159. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
23:21	4h RW/L	**TPPD:** Holds DDR timing parameter tPPD (for LPDDR4 only). PRE/PREALL to PRE/PREALL (same rank) minimum delay in tCK cycles. This parameter is ignored for non LPDDR4 DRAM technology. Supported range is 4-7. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
20:16	6h RW/L	**TRDPRE:** Holds DDR timing parameter tRDPRE. RD to PRE same bank minimum delay in tCK cycles. Supported range is 6-15 **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

Bit Range	Default & Access	Field Name (ID): Description
15:9	1Ch RW/L	**TRAS:** Holds DDR timing parameter tRAS. ACT to PRE same bank minimum delay in tCK cycles. For DDR/LPDDR Supported, the range is 28-90 **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
8:6	0h RW/L	**TRPAB_EXT:** Holds the value of tRPab-tRPpb for LPDDR in tCK cycles. LPDDR technology requires a longer time from PREALL to ACT vs. PRE to ACT, the offset between the two should be programmed to this field. When using DDR4 this field should be programmed to 0. For LPDDR4 the following restrictions apply: For single/dual rank sub channels tRP-tRPab_ext > 6. For three/four ranks sub channels tRP-tRPab_ext > 8. Supported range is 0-6. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
5:0	8h RW/L	**TRP:** Holds DDR timing parameter tRP (and tRCD). PRE to ACT same bank minimum delay in tCK cycles. ACT to CAS (RD or WR) same bank minimum delay in tCK cycles. Supported range is 8-59. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.2 TC_ACT_0_0_0_MCHBAR - Offset 4004h

DDR timing constraints related to ACT commands.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4004h	01088410h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:21	8h RW/L	**TRCD_WR:** Holds DDR timing parameter tRCD_wr (for DDR4-E) in tCK cycles. In other DRAM technologies this field should be configured to be the same as TC_PRE_0_0_0_MCHBAR.tRP. Supported range is 8-59. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
20:18	2h RW/L	**DERATING_EXT:** Holds LPDDR timing parameters derating tRAS, tRRD, tRP and tRCD in tCK cycles. When LPDDR is hot, this value is added to the appropriate timing parameters. For non-LP devices program the field to 0. Supported range is 0-4. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
17:13	4h RW/L	**TRRD_DG:** Holds DDR timing parameter tRRD. ACT to ACT (different bank group in DDR4) minimum delay in tCK cycles. Supported range is 4-22. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

Bit Range	Default & Access	Field Name (ID): Description
12:8	4h RW/L	**TRRD_SG:** Holds DDR timing parameter tRRD/tRRD_L. For LPDDR4 program tRRD, for DDR4 program tRRD_L. ACT to ACT (same bank group in DDR4) minimum delay in tCK cycles. Supported range is 4-22. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
7	0h RO	**Reserved**
6:0	10h RW/L	**TFAW:** Holds DDR timing parameter tFAW (four activates window). In tCK cycles Supported range is 16-88. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.3 TC_RDRD_0_0_0_MCHBAR - Offset 400Ch

DDR timing constraints related to timing between read and read transactions.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 400Ch	04040404h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:24	4h RW/L	**TRDRD_DD:** Minimum delay from RD to RD to the other DIMM in tCK cycles. Supported range is 4-54. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
23:22	0h RO	**Reserved**
21:16	4h RW/L	**TRDRD_DR:** Minimum delay from RD to RD to the other rank in the same DIMM in tCK cycles. Supported range is 4-54. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
15:14	0h RO	**Reserved**
13:8	4h RW/L	**TRDRD_DG:** DDR4: Minimum delay from RD to RD to the different bank group in yCK cycles. Supported range is 4-54. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
7:6	0h RO	**Reserved**
5:0	4h RW/L	**TRDRD_SG:** DDR4: Minimum delay from RD to RD to the same bank group in tCK cycles. Supported range is 4-54. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.4 TC_RDWR_0_0_0_MCHBAR - Offset 4010h

DDR timing constraints related to timing between read and write transactions.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4010h	04040404h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:24	4h RW/L	**TRDWR_DD:** Minimum delay from RD to WR to the other DIMM in tCK cycles. Supported range is 4-54. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
23:22	0h RO	**Reserved**
21:16	4h RW/L	**TRDWR_DR:** Minimum delay from RD to WR to the other rank in the same DIMM in tCK cycles. Supported range is 4-54. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
15:14	0h RO	**Reserved**
13:8	4h RW/L	**TRDWR_DG:** DDR4: Minimum delay from RD to WR to the different bank group in tCK cycles. Supported range is 4-54. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
7:6	0h RO	**Reserved**
5:0	4h RW/L	**TRDWR_SG:** DDR4: Minimum delay from RD to WR to the same bank group in tCK cycles. Supported range is 4-54. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.5 TC_WRRD_0_0_0_MCHBAR - Offset 4014h

DDR timing constraints related to timing between write and read transactions.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4014h	04040404h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:24	4h RW/L	**TWRRD_DD:** Minimum delay from WR to RD to the other DIMM in tCK cycles. Supported range is 4-54. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
23:22	0h RO	**Reserved**
21:16	4h RW/L	**TWRRD_DR:** Minimum delay from WR to RD to the other rank in the same DIMM in tCK cycles. Supported range is 4-54. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
15	0h RO	**Reserved**
14:8	4h RW/L	**TWRRD_DG:** DDR4: Minimum delay from WR to RD to the different bank group in tCK cycles. Supported range is 4-65. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
7:0	4h RW/L	**TWRRD_SG:** DDR4: Minimum delay from WR to RD to the same bank group in tCK cycles. Supported range is 4-145. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.6 TC_WRWR_0_0_0_MCHBAR - Offset 4018h

DDR timing constraints related to timing between write and write transactions.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4018h	04040404h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29:24	4h RW/L	**TWRWR_DD:** Minimum delay from WR to WR to the other DIMM in tCK cycles. Supported range is 4-54. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
23:22	0h RO	**Reserved**
21:16	4h RW/L	**TWRWR_DR:** Minimum delay from WR to WR to the other rank in the same DIMM in tCK cycles. Supported range is 4-54. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:8	4h RW/L	**TWRWR_DG:** DDR4: Minimum delay from WR to WR to the different bank group in tCK cycles. Supported range is 4-54. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
7:6	0h RO	**Reserved**
5:0	4h RW/L	**TWRWR_SG:** DDR4: Minimum delay from WR to WR to the same bank group in tCK cycles. Supported range is 4-54. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.7 SC_ROUNDTRIP_LATENCY_0_0_0_MCHBAR - Offset 4020h

Read Round-trip latency per rank.

Type	Size	Offset	Default
MEM	64 bit	MCHBAR + 4020h	1919191919191919h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RO	**Reserved**
62:56	19h RW/L	**Reserved**
55	0h RO	**Reserved**
54:48	19h RW/L	**Reserved**
47	0h RO	**Reserved**
46:40	19h RW/L	**Reserved**
39	0h RO	**Reserved**
38:32	19h RW/L	**Reserved**
31	0h RO	**Reserved**
30:24	19h RW/L	**RANK_3_LATENCY:** Latency from read command to rank 3 until first data chunk return to MC in QCLK cycles. Supported range is 19-120. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

Bit Range	Default & Access	Field Name (ID): Description
23	0h RO	**Reserved**
22:16	19h RW/L	**RANK_2_LATENCY:** Latency from read command to rank 2 until first data chunk return to MC in QCLK cycles. Supported range is 19-120. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
15	0h RO	**Reserved**
14:8	19h RW/L	**RANK_1_LATENCY:** Latency from read command to rank 1 until first data chunk return to MC in QCLK cycles. Supported range is 19-120. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
7	0h RO	**Reserved**
6:0	19h RW/L	**RANK_0_LATENCY:** Latency from read command to rank 0 until first data chunk return to MC in QCLK cycles. Supported range is 19-120. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.8 TC_PWRDN_0_0_0_MCHBAR - Offset 4050h

DDR timing constraints related to power down.

Type	Size	Offset	Default
MEM	64 bit	MCHBAR + 4050h	0000000404440404h

Bit Range	Default & Access	Field Name (ID): Description
63:40	0h RO	**Reserved**
39:32	4h RW/L	**TWRPDEN:** Holds DDR timing parameter tWRPDEN. WR to power down minimum delay in tCK cycles. Supported range is 4-159. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
31	0h RO	**Reserved**
30:24	4h RW/L	**TRDPDEN:** Holds DDR timing parameter for tRDPDEN. RD to power down minimum delay in tCK cycles. Supported range is 4-95. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

Bit Range	Default & Access	Field Name (ID): Description
23:22	1h RW/L	**TPRPDEN:** Holds DDR timing parameter tPRPDEN. PRE to power down minimum delay in tCK cycles. Supported range is 1-3. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
21:16	4h RW/L	**TXPDLL:** Holds DDR timing parameter tXP. Power up to RD/WR minimum delay in tCK cycles. Applicable for DDR4 in case of exit from PPD when DRAM is configured to slow-exit mode. Supported range is 4-63. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
15:13	0h RO	**Reserved**
12:8	4h RW/L	**TXP:** Holds DDR timing parameter tXP. Power up to any command minimum delay in tCK cycles. Supported range is 4-16. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
7:5	0h RO	**Reserved**
4:0	4h RW/L	**TCKE:** Holds DDR timing parameter tCKE. Power down to power up (and vice versa) minimum delay in tCK cycles. Note that for LPDDR4 this value is also used for tCKCKEL and tCKELCMD. For LPDDR4 tSR (minimum self refresh time) is calculated to be tCKE*2. Supported range is 4-16. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.9 TC_ODT_0_0_0_MCHBAR - Offset 4070h

ODT timing-related parameters.

Type	Size	Offset	Default
MEM	64 bit	MCHBAR + 4070h	00000000018 50000h

Bit Range	Default & Access	Field Name (ID): Description
63:28	0h RO	**Reserved**
27:22	6h RW/L	**TCWL:** Holds DDR timing parameter tCWL (sometimes referred to as tWCL). Write command to data delay in tCK cycles. Supported range is 4-34 (maximum is for 1N mode) For LPDDR4 the minimum supported value is 4. For DDR4 the minimum supported value is 5. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
21:16	5h RW/L	**TCL:** Holds DDR timing parameter tCL. Read command to data delay in tCK cycles. Supported range is 4-36. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
15:0	0h RO	**Reserved**

3.10 SC_ODT_MATRIX_0_0_0_MCHBAR - Offset 4080h

ODT matrix (enabled using SC_GS_CFG_0_0_0_MCHBAR.enable_odt_matrix.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4080h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:28	0h RW/L	**Reserved**
27:24	0h RW/L	**Reserved**
23:20	0h RW/L	**WRITE_RANK_1:** Indicate which ranks should terminate when writing to rank 1 (bits 1:0 correspond to ODT pins 1:0). **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
19:16	0h RW/L	**WRITE_RANK_0:** Indicate which ranks should terminate when writing to rank 0 (bits 1:0 correspond to ODT pins 1:0). **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
15:12	0h RW/L	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
11:8	0h RW/L	**Reserved**
7:4	0h RW/L	**READ_RANK_1:** Indicate which ranks should terminate when reading from rank 1 (bits 1:0 correspond to ODT pins 1:0). Note that according to DRAM spec the target rank should not be terminated. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
3:0	0h RW/L	**READ_RANK_0:** Indicate which ranks should terminate when reading from rank 0 (bits 1:0 correspond to ODT pins 1:0). Note that according to DRAM spec the target rank should not be terminated. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.11 SC_GS_CFG_0_0_0_MCHBAR - Offset 4088h

Scheduler configuration.

Type	Size	Offset	Default
MEM	64 bit	MCHBAR + 4088h	0000000000001020h

Bit Range	Default & Access	Field Name (ID): Description
63:34	0h RO	**Reserved**
33:32	0h RW/L	**DDR4_1DPC:** Performance optimization for 1 DIMM Per Channel (1DPC) with dual rank. To be used only with Intel Memory reference Code as there are couple of low level configurations to enable it. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
31	0h RW/L	**GEAR2:** Indicate that MC is working in Gear-2 (Qclk is half the data transfer clock of the DRAM). **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
30	0h RW/L	**NO_GEAR2_PARAM_DIVIDE:** Don't do RU[param/2] for DRAM timing parameters when in gear-2, treat the value given in them in DCLKs instead of tCK clocks. For extending the existing ranges (mainly for Overclocking). **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
29:28	0h RW/L	**X8_DEVICE:** DIMM is made out of X8 devices. LSB is for DIMM 0, MSB is for DIMM 1. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
27:15	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
14:12	1h RW/L	**TCPDED:** Holds DDR timing parameter tCPDED. Power down to command bus tri-state delay in tCK cycles (for DDR4). Supported range is 1-7 in 1N mode. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
11:8	0h RW/L	**ADDRESS_MIRROR:** DIMM routing causes address mirroring. For DDR4: bit 0: DIMM 0 (rank 1 bus is mirrored). bit 1: **Reserved** For LPDDR4: **Reserved** **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
7:5	1h RW/L	**N_TO_1_RATIO:** When using N:1 command stretch mode, every how many B2B valid command cycles a bubble is required. Supported range is 1 to 7. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
4:3	0h RW/L	**CMD_STRETCH:** Command stretch mode: 00 - 1N 01 - 2N 10 - 3N 11 - N:1 Notice that in Gear2 MC uses only the low phase of Dclk for commands, effectively doing a 2N by default. Setting 2N in Gear2 will result in 4N at DDR interface. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
2:0	0h RO	**Reserved**

3.12 SPID_LOW_POWER_CTL_0_0_0_MCHBAR - Offset 4198h

This register holds DDRIO timing constraints regarding power modes latencies.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4198h	F8141442h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW/L	**SELFREFRESH_ENABLE:** Allow sending DDRIO self refresh mode indication. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
30	1h RW/L	**POWERDOWN_ENABLE:** Allow sending DDRIO CKE power down mode indication. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
29	1h RW/L	**IDLE_ENABLE:** Allow sending DDRIO idle mode indication. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
28	1h RW/L	**CKEVALID_ENABLE:** Allow deasserting cke_valid when not toggling CKE pins. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
27:24	8h RW/L	**CKEVALID_LENGTH:** cke_valid pulse length in DCLK cycles. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
23:20	1h RW/L	**SELFREFRESH_LENGTH:** Minimum time allowed in self refresh mode. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
19:16	4h RW/L	**SELFREFRESH_LATENCY:** Exit latency from self refresh mode till command can be sent in DCLK cycles. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
15:12	1h RW/L	**POWERDOWN_LENGTH:** Minimum time allowed in CKE power down mode. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
11:8	4h RW/L	**POWERDOWN_LATENCY:** Exit latency from CKE power down mode till command can be sent in DCLK cycles. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
7:4	4h RW/L	**IDLE_LENGTH:** Minimum time allowed in idle mode. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
3:1	1h RW/L	**IDLE_LATENCY:** Exit latency from idle mode till command can be sent in DCLK cycles. Note that a value larger than 2 will prevent sending requests in two cycle bypass when in IDLE mode. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
0	0h RW/L	**RAISE_CKE_AFTER_EXIT_LATENCY:** Delay raising of CKE on exit from powerdown and selfrefresh power modes until required latency has passed. If this bit is clear, then CKE exit (and tXP) happens in parallel of waking up the PHY. Otherwise they happen back to back. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.13 LPDDR_MR4_RANK_TEMPERATURE_0_0_0_MCHBAR - Offset 4224h

This register holds the latest MR4 read per rank and used to determine the required refresh rate and thermal conditions of the DRAMs.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4224h	03030303h

Bit Range	Default & Access	Field Name (ID): Description
31:27	0h RO	**Reserved**
26:24	3h RW/V/L	**Reserved**
23:19	0h RO	**Reserved**
18:16	3h RW/V/L	**Reserved**
15:11	0h RO	**Reserved**
10:8	3h RW/V/L	**RANK_1:** Rank 1 refresh rate. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT
7:3	0h RO	**Reserved**
2:0	3h RW/V/L	**RANK_0:** Rank 0 refresh rate. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT

3.14 DDR4_MPR_RANK_TEMPERATURE_0_0_0_MCHBAR Offset 4228h

This register holds the latest temperature read per rank and used to determine the required refresh rate and thermal conditions of the DRAMs.

Encodings are:

00 - Cold (below 45C), single refresh rate required, DRAM may drop refreshes if allowed

01 - Normal operating temperature (45C-85C), single refresh rate, DRAM may drop refreshes if double rate refreshes are given

10 - Hot (Above 85C), double refresh rate

11 - Reserved

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4228h	01010101h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:24	1h RW/V/L	**Reserved**
23:18	0h RO	**Reserved**
17:16	1h RW/V/L	**Reserved**
15:10	0h RO	**Reserved**
9:8	1h RW/V/L	**RANK_1:** Rank 1 refresh rate. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT
7:2	0h RO	**Reserved**
1:0	1h RW/V/L	**RANK_0:** Rank 0 refresh rate. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT

3.15 TC_RFP_0_0_0_MCHBAR - Offset 4238h

Refresh parameters.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4238h	4602980Fh

Bit Range	Default & Access	Field Name (ID): Description
31:25	23h RW/L	**TREFIX9:** Maximum time allowed between refreshes to a rank (in intervals of 1024 DCLK cycles). Should be programmed to 8.9*tREFI/1024 (to allow for possible delays from ZQ or isoc). **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
24:19	0h RO	**Reserved**
18	0h RW/L	**setting this bit will enable MRS refresh at the beginning of the flow, regardless of refresh debt (ALWAYSREFONMRS):** Since MRS can now send refreshes, adding a knob to do it. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
17	1h RW/L	**setting this bit will enable MRS refresh at the beginning of MRS flow if the rank reached HP refresh WM (HPREFONMRS):** Should be set by default, it's intended for SAGV as MC can enter SR while owing refreshes. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

Bit Range	Default & Access	Field Name (ID): Description
16	0h RW/L	**setting this bit will enable tREFI counter while MC refresh enable is not set. (COUNTTREFIWHILEREFENOFF):** Sometimes refresh enable bit is cleared in order to block maintenance operations. MC may want to accumulate refresh debt at that time, setting this bit enable it. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
15:12	9h RW/L	**REFRESH_PANIC_WM:** tREFI count level in which the refresh priority is panic (default is 9). The Maximum value for this field is 9. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
11:8	8h RW/L	**REFRESH_HP_WM:** tREFI count level that turns the refresh priority to high (default is 8). **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
7:0	Fh RW/L	**OREF_RI:** Rank idle period that defines an opportunity for refresh, in DCLK cycles. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.16 TC_RFTP_0_0_0_MCHBAR - Offset 423Ch

Refresh timing parameters.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 423Ch	00B41004h

Bit Range	Default & Access	Field Name (ID): Description
31:26	0h RO	**Reserved**
25:16	B4h RW/L	**TRFC:** Time of refresh - from beginning of refresh until next ACT or refresh is allowed (in tCK cycles, default is 180). **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
15:0	1004h RW/L	**TREFI:** Defines the average period between refreshes, and the rate that tREFI counter is incremented (in tCK cycles, default is 4100). **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.17 TC_SRFTP_0_0_0_MCHBAR - Offset 4240h

Self-refresh timing parameters.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4240h	00000200h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RO	**Reserved**
11:0	200h RW/L	**TXSDLL:** Delay between DDR SR exit and the first command that requires data RD/WR from DDR. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.18 MC_REFRESH_STAGGER_0_0_0_MCHBAR - Offset 4244h

Refresh stagger control.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4244h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14	0h RW/L	**EN_REF_TYPE_DISPLAY:** This bit when set displays refresh type on the BA address pins, 000 = Stolen Refresh 100 = Opportunistic Refresh 010 = Hi Priority Refresh 001 = Panic Refresh **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
13	0h RW/L	**DISABLE_STOLEN_REFRESH:** This bit when set disables stolen refreshes. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
12	0h RW/L	**REF_STAGGER_MODE:** This bit sets the refresh staggering mode, 0 = per DIMM refresh stagger 1 = per channel refresh stagger **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
11	0h RW/L	**REF_STAGGER_EN:** When set this bit enables refresh staggering. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
10:0	0h RW/L	**REF_INTERVAL:** Refresh Interval period in DCLKS. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.19 TC_ZQCAL_0_0_0_MCHBAR - Offset 4248h

ZQCAL control.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4248h	32010000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	320h RW/L	**TZQCAL:** LPDDR4 tZQCAL in tCK cycles. Should typically be set to 1usec. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
19:10	40h RW/L	**TZQCS:** For DDR4 holds tCK value in DCLK cycles. For LPDDR4 holds tZQLAT in DCLK cycles. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
9:0	0h RO	**Reserved**

3.20 MC_INIT_STATE_0_0_0_MCHBAR - Offset 4254h

Holds information on available ranks.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4254h	0000000Fh

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	Fh RW/L	**RANK_OCCUPANCY:** Indicates which ranks are occupied in the system. Non-enhanced channels: • Bit 0: Rank 0 • Bit 1: Rank 1 • Bit 2: **Reserved** • Bit 3: **Reserved** Enhanced channels: • Bit 0: Rank 0 = Sub channel 0 Rank 0 • Bit 1: Rank 1 = Sub channel 0 Rank 1 • Bit 2: Rank 2 = Sub channel 1 Rank 0 • Bit 3: Rank 3 = Sub channel 1 Rank 1 • Bit 4: **Reserved** • Bit 5: **Reserved** • Bit 6: **Reserved** • Bit 7: **Reserved** ***Note:*** Default on reset is all ranks enabled due to DDRIO requirements, BIOS MRC will write these bits to the proper values after reset based on the actual rank configuration. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.21 PM_DIMM_IDLE_ENERGY_0_0_0_MCHBAR - Offset 4260h

This register defines the energy of an idle DIMM with CKE on. Each 6-bit field corresponds to an integer multiple of the base DRAM command energy for that DIMM. There are 2 6-bit fields, one per DIMM.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4260h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:8	0h RW/L	**DIMM1_IDLE_ENERGY:** This register defines the energy consumed by DIMM1 for one clock cycle when the DIMM is idle with CKE on. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT
7:6	0h RO	**Reserved**
5:0	0h RW/L	**DIMM0_IDLE_ENERGY:** This register defines the energy consumed by DIMM0 for one clock cycle when the DIMM is idle with CKE on. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT

3.22 PM_DIMM_PD_ENERGY_0_0_0_MCHBAR - Offset 4264h

This register defines the energy of an idle DIMM with CKE off. Each 6-bit field corresponds to an integer multiple of the base DRAM command energy for that DIMM. There are 2 6-bit fields, one per DIMM.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4264h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:8	0h RW/L	**DIMM1_PD_ENERGY:** This register defines the energy consumed by DIMM1 for one clock cycle when the DIMM is idle with CKE off. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT
7:6	0h RO	**Reserved**
5:0	0h RW/L	**DIMM0_PD_ENERGY:** This register defines the energy consumed by DIMM0 for one clock cycle when the DIMM is idle with CKE off. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT

3.23 PM_DIMM_ACT_ENERGY_0_0_0_MCHBAR - Offset 4268h

This register defines the combined energy contribution of activate and precharge commands. Each 8-bit field corresponds to an integer multiple of the base DRAM command energy for that DIMM. There are 2 8-bit fields, one per DIMM.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4268h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	0h RW/L	**DIMM1_ACT_ENERGY:** This register defines the combined energy contribution of activate and precharge commands. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT
7:0	0h RW/L	**DIMM0_ACT_ENERGY:** This register defines the combined energy contribution of activate and precharge commands. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT

3.24 PM_DIMM_RD_ENERGY_0_0_0_MCHBAR - Offset 426Ch

This register defines the energy contribution of a read CAS command. Each 8-bit field corresponds to an integer multiple of the base DRAM command energy for that DIMM. There are 2 8-bit fields, one per DIMM.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 426Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	0h RW/L	**DIMM1_RD_ENERGY:** This register defines the energy contribution of a read CAS command. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT
7:0	0h RW/L	**DIMM0_RD_ENERGY:** This register defines the energy contribution of a read CAS command. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT

3.25 PM_DIMM_WR_ENERGY_0_0_0_MCHBAR - Offset 4270h

This register defines the energy contribution of a write CAS command. Each 8-bit field corresponds to an integer multiple of the base DRAM command energy for that DIMM. There are 2 8-bit fields, one per DIMM.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4270h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	0h RW/L	**DIMM1_WR_ENERGY:** This register defines the energy contribution of a write CAS command. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT
7:0	0h RW/L	**DIMM0_WR_ENERGY:** This register defines the energy contribution of a write CAS command. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT

3.26 SC_WR_DELAY_0_0_0_MCHBAR - Offset 4278h

This register defines the number of cycles decreased/increased from tCWL (TC_ODT_0_0_0_MCHBAR.tCWL) in Dclks.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4278h	00000003h

Bit Range	Default & Access	Field Name (ID): Description
31:13	0h RO	**Reserved**
12	0h RW/L	**ADD_1QCLK_DELAY:** In Gear2, MC Qclk is actually 1xclk of the DDR, the regular MC register can only set even number of cycles (working in Dclk == 2*1xclk), this bit gives an option to delay the write data by one 1xclk. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
11:6	0h RW/L	**ADD_TCWL:** The number of cycles (Dclk) increased to tCWL, make sure tCWL + Add_tCWL does not overflow. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
5:0	3h RW/L	**DEC_TCWL:** The number of cycles (Dclk) decreased from tCWL, configuring this number to be larger than tCWL is forbidden. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.27 SC_PBR_0_0_0_MCHBAR - Offset 4288h

Per Bank Refresh parameters.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4288h	0000F011h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:10	3Ch RW/L	**TRFCPB:** Refresh time in tCK for REFpb. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
9:4	1h RW/L	**PBR_EXIT_ON_IDLE_CNT:** Number of tREFI cycles to count before switching PBR off for better clock gating. Value of 0 means no Idle exit. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
3	0h RW/L	**PBR_DISABLE_ON_HOT:** Disable PBR when LP4 is at 0.25xtREFI condition. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
2	0h RO	**Reserved**
1	0h RW/L	**PBR_OOO_DIS:** Disable out of order scheduling of banks for LP4. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG
0	1h RW/L	**PBR_DISABLE:** Disable PBR (per bank refresh) for LP4 (DDR4 force PBR off). **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.28 TC_LPDDR4_MISC_0_0_0_MCHBAR - Offset 4294h

Miscellaneous timing constrains of LPDDR4.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 4294h	00000056h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:0	56h RW/L	**TOSCO:** Delay between DQS_OSC counter stop to MR18/19 read. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.29 TC_SREXITTP_0_0_0_MCHBAR - Offset 42C4h

Self-refresh exit timing parameters.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 42C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:10	0h RO	**Reserved**
9:0	0h RW/L	**TXSR:** Exit self refresh to valid commands delay. In LP4 configure this parameter for tXSR or tXSR abort if used. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_CONFIG

3.30 MCMNTS_SPARE_0_0_0_MCHBAR - Offset 43FCh

Spare control register.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 43FCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:12	0h RW/L	**DECODER_EBH:** Enable address decoder Extended bank hashing. Bit 0 - Enable XaB Bit 1 - Enable XbB **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_DFT
11	0h RO	**Reserved**
10	0h RW/L	**DISLOWREFRATE:** Don't allow refresh rate lower than 1X. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_DFT
9	0h RW/L	**FORCEX4REF:** Force accelerated refreshes, four times the refresh number. Should be mutexed with ForceX2Ref. Constant X4 refreshes may block channel from entering self refresh. In case of staggered refreshes and fully occupied channel it can cause performance degradation. Use with caution. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_DFT
8	0h RW/L	**FORCEX2REF:** Force accelerated refreshes, twice the refresh number. Should be mutexed with ForceX4Ref. Constant X2 refreshes may block channel from entering self refresh. In case of staggered refreshes and fully occupied channel it can cause a performance degradation. Use with caution. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_MC_DFT
7:0	0h RO	**Reserved**

3.31 MAD_INTER_CHANNEL_0_0_0_MCHBAR - Offset 5000h

This register holds parameters used by the channel decode stage. It defines virtual channel L mapping, as well as channel S size.

Also defined is the DDR type installed in the system (what DDR/LPDDR type is used).

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5000h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**Reserved**
19:12	0h RW/L	**CH_S_SIZE:** Channel S size in multiplies of 0.5GB. Supported range is 0GB - 64GB. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
11:5	0h RO	**Reserved**
4	0h RW/L	**CH_L_MAP:** Channel L mapping to physical channel. 0: Channel 0 1: Channel 1 **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
3	0h RW/L	**ECHM:** Enhanced channel mode for LPDDR4 indicates that the channel operates as two 32bit channels instead of one 64bit channel. In this mode DIMM 0 is mapped to DQ bits 31:0 and DIMM 1 is mapped to DQ bits 63:32. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
2:0	0h RW/L	**DDR_TYPE:** DDR_TYPE - defines the DDR type in system: 000: DDR4 011: LPDDR4 **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP

3.32 MAD_INTRA_CH0_0_0_0_MCHBAR - Offset 5004h

This register holds parameters used by the DRAM decode stage.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5004h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:12	0h RW/L	**Reserved**
11:9	0h RO	**Reserved**
8	0h RW/L	**EIM:** Enhanced interleaving mode enables bit: 0 - Disabled 1 - Enabled **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
7:5	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
4	0h RW/L	**RI:** Rank interleaving enable bit: 0 - Disabled 1 - Enabled **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
3:1	0h RO	**Reserved**
0	0h RW/L	**DIMM_L_MAP:** Virtual DIMM L mapping to physical DIMM: 0 - DIMM0 1 - DIMM1 **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP

3.33 MAD_INTRA_CH1_0_0_0_MCHBAR - Offset 5008h

This register holds parameters used by the DRAM decode stage.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5008h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13:12	0h RW/L	**Reserved**
11:9	0h RO	**Reserved**
8	0h RW/L	**EIM:** Enhanced interleaving mode enables bit: 0 - Disabled 1 - Enabled **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
7:5	0h RO	**Reserved**
4	0h RW/L	**RI:** Rank interleaving enable bit: 0 - Disabled 1 - Enabled **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
3:1	0h RO	**Reserved**
0	0h RW/L	**DIMM_L_MAP:** Virtual DIMM L mapping to physical DIMM. 0 - DIMM0 1 - DIMM1 **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP

3.34 MAD_DIMM_CH0_0_0_0_MCHBAR - Offset 500Ch

This register defines the channel DIMM characteristics - number of DIMMs, number of ranks, size and type.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 500Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW/L	**DLS_BG0_ON_BIT_11:** When set, BG[0] will be placed on bit 11 of the channel address instead of bit 6. CAS[7] will take zone address 6. 0- CAS[7] = zoneaddr[11], BG[0] = zoneaddr[6]; 1- CAS[7] = zoneaddr[6], BG[0] = zoneaddr[11]; **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
28	0h RO	**Reserved**
27:26	0h RW/L	**DSNOR:** DIMM S number of ranks: 0 - 1 Rank 1 - 2 Ranks **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
25:24	0h RW/L	**DSW:** DSW: DIMM S width of DDR chips: 00 - X8 chips 01 - X16 chips 10 - X32 chips 11 - Reserved **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
23	0h RO	**Reserved**
22:16	0h RW/L	**DIMM_S_SIZE:** Size of DIMM S in 0.5GB multiples. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
15:11	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
10:9	0h RW/L	**DLNOR:** DIMM L number of ranks: 00 - 1 Rank 01 - 2 Ranks In ERM (enhanced rank mode): 10 - 3 Ranks 11 - 4 Ranks **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
8:7	0h RW/L	**DLW:** DLW: DIMM L width of DDR chips: 00 - X8 chips 01 - X16 chips 10 - X32 chips 11 - Reserved **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
6:0	0h RW/L	**DIMM_L_SIZE:** Size of DIMM L in 0.5GB multiples: **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP

3.35 MAD_DIMM_CH1_0_0_0_MCHBAR - Offset 5010h

This register defines the channel DIMM characteristics - number of DIMMs, number of ranks, size and type.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5010h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:30	0h RO	**Reserved**
29	0h RW/L	**DLS_BG0_ON_BIT_11:** When set, BG[0] will be placed on bit 11 of the channel address instead of bit 6. CAS[7] will take zone address 6. 0- CAS[7] = zoneaddr[11], BG[0] = zoneaddr[6]; 1- CAS[7] = zoneaddr[6], BG[0] = zoneaddr[11]; **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
28	0h RO	**Reserved**
27:26	0h RW/L	**DSNOR:** DIMM S number of ranks: 0 - 1 Rank 1 - 2 Ranks **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP

Bit Range	Default & Access	Field Name (ID): Description
25:24	0h RW/L	**DSW:** DSW: DIMM S width of DDR chips: 00 - X8 chips 01 - X16 chips 10 - X32 chips 11 - Reserved **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
23	0h RO	**Reserved**
22:16	0h RW/L	**DIMM_S_SIZE:** Size of DIMM S in 0.5GB multiples. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
15:11	0h RO	**Reserved**
10:9	0h RW/L	**DLNOR:** DIMM L number of ranks: 00 - 1 Rank 01 - 2 Ranks In ERM (enhanced rank mode): 10 - 3 Ranks 11 - 4 Ranks **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
8:7	0h RW/L	**DLW:** DLW: DIMM L width of DDR chips: 00 - X8 chips 01 - X16 chips 10 - X32 chips 11 - Reserved **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
6:0	0h RW/L	**DIMM_L_SIZE:** Size of DIMM L in 0.5GB multiples. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP

3.36 CHANNEL_HASH_0_0_0_MCHBAR - Offset 5024h

This register defines the MC channel selection function.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5024h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW/L	**HASH_MODE:** Encoding: 0: Use address bit-6 for channel selection. 1: Use the channel hash function as defined in the other fields of this register. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
27	0h RO	**Reserved**
26:24	0h RW/L	**HASH_LSB_MASK_BIT:** This specifies the MC Channel interleave bit. The following encoding is used: 000 - Addr[6] 001 - Addr[7] 010 - Addr[8] 011 - Addr[9] 100 - Addr[10] 101 - Addr[11] 110 - Addr[12] 111 - Addr[13] For example, setting this field to 10b will interleave the channels at a 4 cacheline granularity. BIOS should set this field same as the lowest selected bit in the Mask field of this CR. Note that if the Mask field does not include the corresponding interleave bit, it will still be included in the XOR function by the MC decoding logic. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
23:20	0h RO	**Reserved**
19:6	0h RW/L	**HASH_MASK:** The 14-bit mask corresponds to memory request Addr[19:6]. Setting a mask bit to 1 will include that particular address bit in the channel XOR function. For example, if the mask is set to 14'h0C04, then Channel = Addr[17] Addr[16] Addr[8]. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
5:0	0h RO	**Reserved**

3.37 CHANNEL_EHASH_0_0_0_MCHBAR - Offset 5028h

This register defines the MC Enhanced channel selection function.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5028h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	0h RW/L	**EHASH_MODE:** Encoding: 0: Use address bit-6 for channel selection. 1: Use the channel Ehash function as defined in the other fields of this register. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
27	0h RO	**Reserved**
26:24	0h RW/L	**EHASH_LSB_MASK_BIT:** This specifies the MC Enhanced Channel interleave bit. The following encoding is used: • 000: Addr[6] • 001: Addr[7] • 010: Addr[8] • 011: Addr[9] • 100: Addr[10] • 101: Addr[11] • 110: Addr[12] • 111: Addr[13] For example, setting this field to 10b will interleave the sub channels at a 4 cache line granularity. BIOS should set this field same as the lowest selected bit in the Mask field of this register. Note that if the Mask field does not include the corresponding interleave bit, it will still be included in the XOR function by the MC decoding logic. The addresses above refer to channel addresses. When both channels are populated with sub-channels, addresses in this field that are higher than the HASH_LSB_MASK_BIT (defined in CHANNEL_HASH register) are one bit higher in physical address. Examples: • HASH_LSB_MASK_BIT = 0x2: physical Addr[8] • EHASH_LSB_MASK_BIT=0x2: channel address[8], physical address [9] **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
23:20	0h RO	**Reserved**
19:6	0h RW/L	**EHASH_MASK:** The 14 bit mask corresponds to memory request Addr[19:6]. Setting a mask bit to 1 will include that particular address bit in the channel XOR function. For example, if the mask is set to 14'h0C04, then Channel = Addr[17] Addr[16] Addr[8] The addresses above refer to channel addresses. When both channels are populated with sub-channels, addresses in this field that are higher than the HASH_LSB_MASK_BIT (defined in CHANNEL_HASH register) are one bit higher in physical address. Examples: • HASH_LSB_MASK_BIT = 0x2: physical Addr[8] • EHASH_LSB_MASK_BIT=0x2: channel address[8], physical address [9] **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_ADDR_MAP
5:0	0h RO	**Reserved**

3.38 PWM_GT_REQCOUNT_0_0_0_MCHBAR - Offset 5040h

Counts every read/write request entering the Memory Controller to DRAM (sum of all channels) from the GT engine. Each partial writes request counts as a request incrementing this counter. However same-cache-line partial write requests are combined to a single 64-byte data transfer from DRAM. Therefore multiplying the number of requests by 64-bytes will lead to inaccurate GT memory bandwidth. The inaccuracy is proportional to the number of same-cache-line partial writes combined.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5040h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**COUNT:** Number of accesses. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT

3.39 PWM_IA_REQCOUNT_0_0_0_MCHBAR - Offset 5044h

Counts every read/write request (demand and HW pre-fetch) entering the Memory Controller to DRAM (sum of all channels) from IA. Each partial writes request counts as a request incrementing this counter. However same-cache-line partial write requests are combined to a single 64-byte data transfer from DRAM. Therefore multiplying the number of requests by 64-bytes will lead to inaccurate IA memory bandwidth. The inaccuracy is proportional to the number of same-cache-line partial writes combined.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5044h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**COUNT:** Number of accesses. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT

3.40 PWM_IO_REQCOUNT_0_0_0_MCHBAR - Offset 5048h

Counts every read/write request entering the Memory Controller to DRAM (sum of all channels) from all IO sources (e.g. PCIe, Display Engine, USB audio, etc.). Each partial writes request counts as a request incrementing this counter. However same-cache-line partial write requests are combined to a single 64-byte data transfer from DRAM. Therefore multiplying the number of requests by 64-bytes will lead to inaccurate IO memory bandwidth. The inaccuracy is proportional to the number of same-cache-line partial writes combined.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5048h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**COUNT:** Number of accesses. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT

3.41 PWM_RDDATA_COUNT_0_0_0_MCHBAR - Offset 5050h

Counts every read (RdCAS) issued by the Memory Controller to DRAM (sum of all channels). All requests result in 64-byte data transfers from DRAM. Use for accurate memory bandwidth calculations.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5050h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**COUNT:** Number of accesses. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT

3.42 PWM_WRDATA_COUNT_0_0_0_MCHBAR - Offset 5054h

Counts every write (WrCAS) issued by the Memory Controller to DRAM (sum of all channels). All requests result in 64-byte data transfers from DRAM. Use for accurate memory bandwidth calculations.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5054h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**COUNT:** Number of accesses. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT

3.43 PWM_COMMAND_COUNT_0_0_0_MCHBAR - Offset 5058h

Request counter used by PCU for estimation of MC & MCIO power consumption and its sources. There are 3 registers for sources and three registers for MC Operations. Sources:

GT

IA

IO

MC Operations

RD data

WR data

Command

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5058h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V/L	**COUNT:** Number of accesses. **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT

3.44 PM_SREF_CONFIG_0_0_0_MCHBAR - Offset 5060h

Self refresh mode control register - defines if and when DDR can go into SR.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5060h	00000200h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	200h RW/V/L	**IDLE_TIMER:** This value is used when the SREF_enable field is set. It defines the number of cycles that there should not be any transaction in order to enter self-refresh. Supported range is 512 to 64K-1 **Locked by:** MC_LOCK_0_0_0_MCHBAR.LOCK_PWR_MNGMENT

3.45 REMAPBASE_0_0_0_MCHBAR - Offset 5090h

MMIO copy of REMAPBASE_0_0_0_PCI.

Type	Size	Offset	Default
MEM	64 bit	MCHBAR + 5090h	0000007FFF00000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:20	7FFFFh RW	**REMAPBASE:** The value in this register defines the lower boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[19:0] of the Remap Base Address are assumed to be 0's. Thus the bottom of the defined memory range will be aligned to a 1MB boundary. When the value in this register is greater than the value programmed into the Remap Limit register, the Remap window is disabled.
19:0	0h RO	**Reserved**

3.46 REMAPLIMIT_0_0_0_MCHBAR - Offset 5098h

MMIO copy of REMAPLIMIT_0_0_0_PCI.

Type	Size	Offset	Default
MEM	64 bit	MCHBAR + 5098h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:20	0h RW	**REMAPLMT:** The value in this register defines the upper boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[19:0] of the remap limit address are assumed to be F's. Thus the top of the defined range will be one byte less than a 1MB boundary. When the value in this register is less than the value programmed into the Remap Base register, the Remap window is disabled.
19:0	0h RO	**Reserved**

3.47 GFXVTBAR_0_0_0_MCHBAR_NCU - Offset 5400h

This is the base address for the Graphics VT configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the GFX-VT configuration space is disabled and must be enabled by writing a 1 to GFX-VTBAREN.

All the bits in this register are locked in LT mode.

BIOS programs this register after which the register cannot be altered.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5400h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RW/V	**GFXVTBAR:** This field corresponds to bits 38 to 12 of the base address GFX-VT configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the GFX-VT register set. All the Bits in this register are locked in LT mode.
11:1	0h RO	**Reserved**
0	0h RW/V/L	**GFXVTBAREN:** 0: GFX-VTBAR is disabled and does not claim any memory 1: GFX-VTBAR memory mapped accesses are claimed and decoded appropriately This bit will remain 0 if VTd capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.VTDD

3.48 VTDPVC0BAR_0_0_0_MCHBAR_NCU - Offset 5410h

This is the base address for the DMI VC0 configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the DMI VC0 configuration space is disabled and must be enabled by writing a 1 to VC0BAREN.

All the bits in this register are locked in LT mode.

BIOS programs this register after which the register cannot be altered.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + 5410h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0000000h RW/V	**VTVC0BAR:** This field corresponds to bits 38 to 12 of the base address DMI VC0 configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the DMI VC0 register set. All the Bits in this register are locked in LT mode.
11:1	0h RO	**Reserved**
0	0h RW/V/L	**VTVC0BAREN:** 0: VC0BAR is disabled and does not claim any memory 1: VC0BAR memory mapped accesses are claimed and decoded appropriately This bit will remain 0 if VTd capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.VTDD

3.49 BIOS_POST_CODE_0_0_0_MCHBAR_PCU - Offset 5824h

This register holds 32 writable bits with no functionality behind them. BIOS will write here the current POST code (port 80).

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5824h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**POSTCODE:** BIOS will write the current POST code in this field.

3.50 PRIP_TURBO_PLCY_0_0_0_MCHBAR_PCU - Offset 5920h

The PRIMARY_PLANE_TURBO_POWER_POLICY and SECONDARY_PLANE_TURBO_POWER_POLICY are used together to balance the power budget between the two power planes.

The power plane with the higher policy will get a higher priority. The default value will aim to maintain same ratio for IA and GT.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5920h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	0h RW	**PRIPTP:** Priority Level. A higher number implies a higher priority.

3.51 SECP_TURBO_PLCY_0_0_0_MCHBAR_PCU - Offset 5924h

The PRIMARY_PLANE_TURBO_POWER_POLICY and SECONDARY_PLANE_TURBO_POWER_POLICY are used together to balance the power budget between the two power planes.

The power plane with the higher policy will get a higher priority. The default value will aim to maintain same ratio for IA and GT.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5924h	00000010h

Bit Range	Default & Access	Field Name (ID): Description
31:5	0h RO	**Reserved**
4:0	10h RW	**SECPTP:** Priority Level. A higher number implies a higher priority.

3.52 PRIP_NRG_STTS_0_0_0_MCHBAR_PCU - Offset 5928h

Reports total energy consumed. The counter will wrap around and continue counting when it reaches its limit.

The energy status is reported in units which are defined in PACKAGE_POWER_SKU_UNIT_MSR[ENERGY_UNIT].

Software will read this value and subtract the difference from last value read. The value of this register is updated every 1mSec.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5928h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**DATA:** Energy Value.

3.53 SECP_NRG_STTS_0_0_0_MCHBAR_PCU - Offset 592Ch

Reports total energy consumed. The counter will wrap around and continue counting when it reaches its limit.

The energy status is reported in units which are defined in PACKAGE_POWER_SKU_UNIT_MSR[ENERGY_UNIT].

Software will read this value and subtract the difference from last value read. The value of this register is updated every 1mSec.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 592Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**DATA:** Energy Value.

3.54 PP0_EFFICIENT_CYCLES_0_0_0_MCHBAR_PCU - Offset 5968h

This register will store a value equal to the product of the number of BCLK cycles in which at least one of the IA cores was active and the efficiency score calculated by the PCODE. The efficiency score is a number between 0 and 1 that indicates the IAs efficiency.

This is a 32 bit accumulation done by P-code to this register out of the PUSH-BUS. Values exceeding 32b will wrap around.

This value is used in conjunction with PP0_ANY_THREAD_ACTIVITY to generate statistics for software.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5968h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**DATA:** Number of Cycles

3.55 PP0_THREAD_ACTIVITY_0_0_0_MCHBAR_PCU - Offset 596Ch

This register will store a value equal to the product of the number of BCLK cycles and the number of IA threads that are running. This is a 32 bit accumulation done by PCU HW. Values exceeding 32b will wrap around.

This value is used in conjunction with PP0_ANY_THREAD_ACTIVITY to generate statistics for software.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 596Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**DATA:** Number of Cycles.

3.56 PP0_TEMPERATURE_0_0_0_MCHBAR_PCU - Offset 597Ch

PP0 (IA) temperature in degrees (C). This field is updated by FW.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 597Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	0h RO/V	**DATA:** Temperature in degrees (C).

3.57 TEMPERATURE_TARGET_0_0_0_MCHBAR_PCU - Offset 599Ch

Legacy register holding temperature related constants for Platform use.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 599Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/L	**LOCKED:** When set, this entire register becomes read-only. **Locked by:** TEMPERATURE_TARGET.LOCKED

Bit Range	Default & Access	Field Name (ID): Description
30:24	0h RO	**Reserved**
23:16	0h RO/V	**REF_TEMP:** This field indicates the maximum junction temperature, also referred to as the Throttle Temperature, TCC Activation Temperature or Prochot Temperature. This is the temperature at which the Adaptive Thermal Monitor is activated.
15:0	0h RO	**Reserved**

3.58 PACKAGE_RAPL_LIMIT_0_0_0_MCHBAR_PCU – Offset 59A0h

Package RAPL Power Limit allows a software agent to define power limitation for the package domain. Power limitation is defined in terms of average power usage (Watts) over a time window specified.

Two power limits and associated time windows can be specified. These power limits are commonly referred to as PL1 (long time window) and PL2 (short time window). Each power limit provides independent clamping control that would permit the processor cores to go below OS-requested state to meet the power limits. A lock mechanism allows the software agent to enforce power limit settings. Once the lock bit is set, the power limit settings are static and un-modifiable until next RESET.

Type	Size	Offset	Default
MEM	64 bit	MCHBAR + 59A0h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW_L	**PKG_PWR_LIM_LOCK:** When set all settings in this register are locked and are treated as Read Only. This lock control is persistent until the next reset. This bit will typically set by BIOS during boot time or resume from Sx.
62:56	0h RO	**Reserved**
55:49	00h RW_L	**PKG_PWR_LIM_2_TIME:** Time window for Power Limit 1 (PL2). This describes the control window of the power limit. This time window is described in an RC time constant format, which means that if 1s is programmed, the power limit constraint really applies at more like 5s. The maximal time window is bounded by PACKAGE_POWER_SKU_MSR.PKG_MAX_WIN. There is no constraint on the minimum programmable time window, however at very short time windows the control algorithms may not be effective. The bits of this field describe parameters for a mathematical equation for time window configuration. This field is split into two sub-fields: • x = bits[6:5] • y = bits[4:0] Time window equation: time_window = PACKAGE_POWER_SKU_UNIT.TIME_UNIT * ((1+x/4)^y)

Bit Range	Default & Access	Field Name (ID): Description
48	00h RW_L	**PKG_CLMP_LIM_2:** Clamp mode control for PL2. • 0 = PL2 power control is prevented from forcing P-states below the base frequency / P1 for any domain in the SOC. • 1 = PL2 power control will take all actions necessary to meet the power target, even if that involves running at clock frequencies below the base frequency / P1 level. In order to ensure proper SOC cooling, it is generally recommended that the clamp mode is always enabled.
47	00h RW_L	**PKG_PWR_LIM_2_EN:** Enable for Power Limit 2 (PL2). Setting this bit activates the power limit and time window defined for PL2.
46:32	0000h RW_L	**PKG_PWR_LIM_2:** Sets the average power usage limit of the package domain corresponding to the PL2 time window. The power units of this field are specified by the PACKAGE_POWER_SKU_UNIT_MSR.PWR_UNIT. This power limit must be configured by software before it will engage. The PL2 limit is most commonly associated with long time windows (1s and longer), although there are no explicit constraints on what software configures.
31:24	0h RO	**Reserved**
23:17	00h RW_L	**PKG_PWR_LIM_1_TIME:** Time window for Power Limit 1 (PL1). This describes the control window of the power limit. This time window is described in an RC time constant format, which means that if 1s is programmed, the power limit constraint really applies at more like 5s. The maximal time window is bounded by PACKAGE_POWER_SKU_MSR.PKG_MAX_WIN. There is no constraint on the minimum programmable time window, however at very short time windows the control algorithms may not be effective. The bits of this field describe parameters for a mathematical equation for time window configuration. This field is split into two sub-fields: • x = bits[6:5] • y = bits[4:0] Time window equation: time_window = PACKAGE_POWER_SKU_UNIT.TIME_UNIT * ((1+x/4)^y)
16	0h RW_L	**PKG_CLMP_LIM_1:** Clamp mode control for PL1. • 0 = PL1 power control is prevented from forcing P-states below the base frequency / P1 for any domain in the SOC. • 1 = PL1 power control will take all actions necessary to meet the power target, even if that involves running at clock frequencies below the base frequency / P1 level. In order to ensure proper SOC cooling, it is generally recommended that the clamp mode is always enabled.
15	0h RW_L	**PKG_PWR_LIM_1_EN:** Enable for Power Limit 1 (PL1). Setting this bit activates the power limit and time window defined for PL1.
14:0	0000h RW_L	**PKG_PWR_LIM_1:** Sets the average power usage limit of the package domain corresponding to the PL1 time window. The power units of this field are specified by the PACKAGE_POWER_SKU_UNIT_MSR.PWR_UNIT. This power limit must be configured by software before it will engage. The PL1 limit is most commonly associated with long time windows (1s and longer), although there are no explicit constraints on what software configures.

3.59 THERM_STATUS_GT_0_0_0_MCHBAR_PCU - Offset 59C0h

Contains status information about the processors thermal sensor and automatic thermal monitoring facilities.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 59C0h	08000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**VALID:** This bit indicates that the TEMPERATURE field is valid. It is set by PCODE if the temperature is within valid thermal sensor range.
30:27	1h RO	**RESOLUTION:** Supported resolution in degrees C.
26:23	0h RO	**Reserved**
22:16	0h RO/V	**TEMPERATURE:** This is a temperature offset in degrees C below theTJ Max temperature. This number is meaningful only if VALID bit in this register is set.
15	0h RW/0C/V	**CROSS_DOMAIN_LIMIT_LOG:** R/WC0 - If set (1), indicates another hardware domain (e.g. processor graphics) has limited energy efficiency optimizations in the processor core domain since the last clearing of this bit or a reset. This bit is sticky, software may clear this bit by writing a zero (0).
14	0h RO/V	**CROSS_DOMAIN_LIMIT_STATUS:** RO - If set (1), indicates another hardware domain (e.g. processor graphics) is currently limiting energy efficiency optimizations in the processor core domain.
13	0h RW/0C/V	**CURRENT_LIMIT_LOG:** R/WC0 - If set (1), an electrical current limit has been exceeded that has adversely impacted energy efficiency optimizations since the last clearing of this bit or a reset. This bit is sticky, software may clear this bit by writing a zero (0).
12	0h RO/V	**CURRENT_LIMIT_STATUS:** RO - If set (1), indicates an electrical current limit (e.g. Electrical Design Point/ IccMax) is being exceeded and is adversely impacting energy efficiency optimizations.
11	0h RW/0C/V	**POWER_LIMITATION_LOG:** R/WC0 - Sticky bit which indicates whether the current P-state is limited by power limitation since the last clearing of this bit or a reset. Software may clear this bit by writing a zero (0). For legacy P state method, this bit will be set only if the P-state is limit below the guaranty level.
10	0h RO/V	**POWER_LIMITATION_STATUS:** RO - Indicates whether the current P-state is limited by power limitation. For legacy P state method, this bit will be set only if the P-state is limit below the guaranty level.
9	0h RW/0C/V	**THRESHOLD2_LOG:** Sticky log bit that asserts on a 0 to 1 or a 1 to 0 transition of the THRESHOLD2_STATUS bit. This bit is set by HW and cleared by software.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO/V	**THRESHOLD2_STATUS:** Indicates that the current temperature is higher than or equal to Threshold 2 temperature.
7	0h RW/0C/V	**THRESHOLD1_LOG:** Sticky log bit that asserts on a 0 to 1 or a 1 to 0 transition of the THRESHOLD1_STATUS bit. This bit is set by HW and cleared by software.
6	0h RO/V	**THRESHOLD1_STATUS:** Indicates that the current temperature is higher than or equal to Threshold 1 temperature.
5	0h RW/0C/V	**OUT_OF_SPEC_LOG:** Sticky log bit indicating that the processor operating out of its thermal specification since the last time this bit was cleared. This bit is set by HW on a 0 to 1 transition of OUT_OF_SPEC_STATUS.
4	0h RO/V	**OUT_OF_SPEC_STATUS:** Status bit indicating that the processor is operating out of its thermal specification. Once set, this bit should only clear on a reset.
3	0h RW/0C/V	**PROCHOT_LOG:** Sticky log bit indicating that xxPROCHOT# has been asserted since the last time this bit was cleared by software. This bit is set by HW on a 0 to 1 transition of PROCHOT_STATUS.
2	0h RO/V	**PROCHOT_STATUS:** Status bit indicating that xxPROCHOT# is currently being asserted.
1	0h RW/0C/V	**THERMAL_MONITOR_LOG:** Sticky log bit indicating that the core has seen a thermal monitor event since the last time software cleared this bit. This bit is set by HW on a 0 to 1 transition of THERMAL_MONITOR_STATUS.
0	0h RO/V	**THERMAL_MONITOR_STATUS:** Status bit indicating that the Thermal Monitor has tripped and is currently thermally throttling.

3.60 THERM_INTERRUPT_GT_0_0_0_MCHBAR_PCU - Offset 59C4h

Enables and disables the generation of an interrupt on temperature transitions detected with the processors thermal sensors and thermal monitor.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 59C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:25	0h RO	**Reserved**
24	0h RW	**POWER_INT_ENABLE:** When this bit is set, a thermal interrupt will be sent upon throttling due to power limitations.
23	0h RW	**THRESHOLD_2_INT_ENABLE:** Controls the generation of a thermal interrupt whenever the Thermal Threshold 2 Temperature is crossed.
22:16	0h RW	**THRESHOLD_2_REL_TEMP:** This value indicates the offset in degrees below TJ Max Temperature that should trigger a Thermal Threshold 2 trip.
15	0h RW	**THRESHOLD_1_INT_ENABLE:** Controls the generation of a thermal interrupt whenever the Thermal Threshold 1 Temperature is crossed.
14:8	0h RW	**THRESHOLD_1_REL_TEMP:** This value indicates the offset in degrees below TJ Max Temperature that should trigger a Thermal Threshold 1 trip.
7:5	0h RO	**Reserved**
4	0h RW	**OUT_OF_SPEC_INT_ENABLE:** Thermal interrupt enable for the critical temperature condition which is stored in the Critical Temperature Status bit in IA32_THERM_STATUS.
3	0h RO	**Reserved**
2	0h RW	**PROCHOT_INT_ENABLE:** Bidirectional PROCHOT# assertion interrupt enable. If set, a thermal interrupt is delivered on the rising edge of xxPROCHOT#.
1	0h RW	**LOW_TEMP_INT_ENABLE:** Enables a thermal interrupt to be generated on the transition from a high-temperature to a low-temperature when set, where high temperature is dictated by the thermal monitor trip temperature.
0	0h RW	**HIGH_TEMP_INT_ENABLE:** Enables a thermal interrupt to be generated on the transition from a low-temperature to a high-temperature when set, where high temperature is dictated by the thermal monitor trip temperature.

3.61 BIOS_MAILBOX_DATA_0_0_0_MCHBAR_PCU - Offset 5DA0h

Data register for the BIOS-to-Firmware mailbox.

This register is used in conjunction with BIOS_MAILBOX_INTERFACE.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5DA0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**DATA:** This field contains the data associated with specific commands.

3.62 BIOS_MAILBOX_INTERFACE_0_0_0_MCHBAR_PCU Offset 5DA4h

Control and Status register for the BIOS-to-Firmware mailbox.

This register is used in conjunction with BIOS_MAILBOX_DATA.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5DA4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/1S/V	**RUN_BUSY:** Software may write to the two mailboxes registers only when RUN_BUSY is cleared (0b). After setting this bit, software will poll this bit until it is cleared. Firmware will clear RUN_BUSY after updating the mailbox registers with the result and error code.
30:29	0h RO	**Reserved**
28:8	0h RW/V	**ADDR:** This field contains additional parameters associated with specific commands.
7:0	0h RW/V	**COMMAND:** On RUN_BUSY assertion this field should contain the software request command, on RUN_BUSY deassertion this field will contain the Firmware response code.

3.63 MC_BIOS_REQ_0_0_0_MCHBAR_PCU - Offset 5E00h

This register allows BIOS to request Memory Controller clock frequency.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5E00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**RUN_BUSY:** This bit indicates that the BIOS request is pending. BIOS sets this bit together with a command in the lower bits of this register. Firmware may only clear this bit after the BIOS request has been served or observed.
30:25	0h RO	**Reserved**
24:17	0h RW	**VDDQ_TX_VOLTAGE:** These bits are used for LP4 DDR Tx Voltage. BIOS will WRITE and PUNIT READ this field.
16	0h RW	GEAR_TYPE: 0h - Gear1 (Default) 1h - Gear2
15:12	0h RO	**Reserved**
11:8	0h RW	**REQ_TYPE:** 0h - MC frequency request for 133MHz Qclk granularity. 1h - MC frequency request for 100MHz Qclk granularity. All other values are reserved.
0:7	0h RW	**REQ_DATA:** These 8 bits are the data for the Qclk ratio request. The only possible request type is MC frequency request. ***Note***: In case of MC frequency request, the LSB contains the legacy REQ_QCLK_ODD_RATIO bit, so the requested Qclk granularity is 133/100MHz. Binary Dec DCLK Equation DCLK Freq QCLK Equation QCLK Freq 0000b 0d ----------MC PLL - shutdown ---------- ... 0011b 3d 3 * 66.66 200.00 MHz 3 * 133.33 400.00 MHz 0100b 4d 4 * 66.66 266.66 MHz 4 * 133.33 533.33 MHz 0101b 5d 5 * 66.66 333.33 MHz 5 * 133.33 666.67 MHz 0110b 6d 6 * 66.66 400.00 MHz 6 * 133.33 800.00 MHz 0111b 7d 7 * 66.66 466.66 MHz 7 * 133.33 933.33 MHz 1000b 8d 8 * 66.66 533.33 MHz 8 * 133.33 1066.67 MHz ...

3.64 OC_STATUS_0_0_0_MCHBAR_PCU - Offset 5F58h

This MMIO register will be written by pcode to report the BCLK frequency.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5F58h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/L	**MC_TIMING_RUNTIME_OC_ENABLED:**

3.65 PACKAGE_SW_PL4_OFFSET_0_0_0_MCHBAR_PCU - Offset 5F60h

Software PL4 OFFSET Data register written by the platform software.

Type	Size	Offset	Default
MEM	32 bit	MCHBAR + 5F60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:12	0h RW/V	**SW_PL4_UNIT:** Exponent of the PL4 Offset. (2^PL4_unit)*(PL4_Offset)*1mw.
11:8	0h RW/V	**SW_PL4_RSVD1:** Reserved.
7:0	0h RW/V	**SW_PL4_OFFSET:** Mantissa of software PL4 OFFSET.

3.66 BCLK_FREQ_0_0_0_MCHBAR - Offset 5F68h

This MMIO register will be written by pcode to report the BCLK frequency.

Type	Size	Offset	Default
MEM	64 bit	MCHBAR + 5F68h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:32	0h RW/L	**PCIECLK_FREQ:** Reported PCIE BCLK Frequency in kHz.
31:0	0h RW/L	**BCLK_FREQ:** Reported BCLK Frequency in kHz.

3.67 REGBAR_0_0_0_MCHBAR_IMPH - Offset 7110h

Type	Size	Offset	Default
MEM	64 bit	MCHBAR + 7110h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:24	0h RW	**REGFBAR:** This field corresponds to bits 38 to 24 of the base address MMIO space. BIOS will program this register resulting in a base address for a 16MB block of contiguous memory address space.
23:1	0h RO	**Reserved**
0	0h RW	**REGBAREN:** 0: REGBAR is disabled and does not claim any memory. 1: REGBAR memory mapped accesses are claimed and decoded appropriately. **Locked by:** CAPID0_A_0_0_0_PCI.VTDD

3.68 In-Band ECC Activate (IBECC_ACTIVATE) — Offset DC00h

BIOS programmed register that enables or disables In-Band ECC; should be the last IBECC register programmed.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + DC00h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW	**IBECC Enable Control (IBECC_EN):** When set, enables In-Band ECC and initiates credit handshakes on CMI.

3.69 IBECC Protected Address Range (IBECC_PROTECT_ADDR_RANGE_0) — Offset DC0Ch

Address/Enable control register for ADDR_RANGE X of ECC Protected Space. If (ADDRESS & MASK_X == BASE_X), then ADDRESS is part of RANGE_X.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + DC0Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ECC Protect Address Range Enable (RANGE_EN):** When set, enables use of the address range specified in this register for ECC Protection.
30	0h RO	**Reserved**
29:16	0000h RW	**ECC Protect Address Range Mask (MASK):** Mask address for this address range of ECC protected space.
15:14	0h RO	**Reserved**
13:0	0000h RW	**ECC Protect Address Range Base (BASE):** Base address for this address range of ECC protected space.

3.70 IBECC Protected Address Range (IBECC_PROTECT_ADDR_RANGE_1) — Offset DC10h

Address/Enable control register for ADDR_RANGE X of ECC Protected Space. If (ADDRESS & MASK_X == BASE_X), then ADDRESS is part of RANGE_X.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + DC10h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ECC Protect Address Range Enable (RANGE_EN):** When set, enables use of the address range specified in this register for ECC Protection.
30	0h RO	**Reserved**
29:16	0000h RW	**ECC Protect Address Range Mask (MASK):** Mask address for this address range of ECC protected space.
15:14	0h RO	**Reserved**
13:0	0000h RW	**ECC Protect Address Range Base (BASE):** Base address for this address range of ECC protected space.

3.71 IBECC Protected Address Range (IBECC_PROTECT_ADDR_RANGE_2) — Offset DC14h

Address/Enable control register for ADDR_RANGE X of ECC Protected Space. If (ADDRESS & MASK_X == BASE_X), then ADDRESS is part of RANGE_X.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + DC14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ECC Protect Address Range Enable (RANGE_EN):** When set, enables use of the address range specified in this register for ECC Protection.
30	0h RO	**Reserved**
29:16	0000h RW	**ECC Protect Address Range Mask (MASK):** Mask address for this address range of ECC protected space.
15:14	0h RO	**Reserved**
13:0	0000h RW	**ECC Protect Address Range Base (BASE):** Base address for this address range of ECC protected space.

3.72 IBECC Protected Address Range (IBECC_PROTECT_ADDR_RANGE_3) — Offset DC18h

Address/Enable control register for ADDR_RANGE X of ECC Protected Space. If (ADDRESS & MASK_X == BASE_X), then ADDRESS is part of RANGE_X.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + DC18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ECC Protect Address Range Enable (RANGE_EN):** When set, enables use of the address range specified in this register for ECC Protection.
30	0h RO	**Reserved**
29:16	0000h RW	**ECC Protect Address Range Mask (MASK):** Mask address for this address range of ECC protected space.
15:14	0h RO	**Reserved**
13:0	0000h RW	**ECC Protect Address Range Base (BASE):** Base address for this address range of ECC protected space.

3.73 IBECC Protected Address Range (IBECC_PROTECT_ADDR_RANGE_4) — Offset DC1Ch

Address/Enable control register for ADDR_RANGE X of ECC Protected Space. If (ADDRESS & MASK_X == BASE_X), then ADDRESS is part of RANGE_X.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + DC1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ECC Protect Address Range Enable (RANGE_EN):** When set, enables use of the address range specified in this register for ECC Protection.
30	0h RO	**Reserved**
29:16	0000h RW	**ECC Protect Address Range Mask (MASK):** Mask address for this address range of ECC protected space.
15:14	0h RO	**Reserved**
13:0	0000h RW	**ECC Protect Address Range Base (BASE):** Base address for this address range of ECC protected space.

3.74 IBECC Protected Address Range (IBECC_PROTECT_ADDR_RANGE_5) — Offset DC20h

Address/Enable control register for ADDR_RANGE X of ECC Protected Space. If (ADDRESS & MASK_X == BASE_X), then ADDRESS is part of RANGE_X.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + DC20h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ECC Protect Address Range Enable (RANGE_EN):** When set, enables use of the address range specified in this register for ECC Protection.
30	0h RO	**Reserved**
29:16	0000h RW	**ECC Protect Address Range Mask (MASK):** Mask address for this address range of ECC protected space.
15:14	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
13:0	0000h RW	**ECC Protect Address Range Base (BASE):** Base address for this address range of ECC protected space.

3.75 IBECC Protected Address Range (IBECC_PROTECT_ADDR_RANGE_6) — Offset DC24h

Address/Enable control register for ADDR_RANGE X of ECC Protected Space. If (ADDRESS & MASK_X == BASE_X), then ADDRESS is part of RANGE_X.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + DC24h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ECC Protect Address Range Enable (RANGE_EN):** When set, enables use of the address range specified in this register for ECC Protection.
30	0h RO	**Reserved**
29:16	0000h RW	**ECC Protect Address Range Mask (MASK):** Mask address for this address range of ECC protected space.
15:14	0h RO	**Reserved**
13:0	0000h RW	**ECC Protect Address Range Base (BASE):** Base address for this address range of ECC protected space.

3.76 IBECC Protected Address Range (IBECC_PROTECT_ADDR_RANGE_7) — Offset DC28h

Address/Enable control register for ADDR_RANGE X of ECC Protected Space. If (ADDRESS & MASK_X == BASE_X), then ADDRESS is part of RANGE_X.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + DC28h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**ECC Protect Address Range Enable (RANGE_EN):** When set, enables use of the address range specified in this register for ECC Protection.
30	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
29:16	0000h RW	**ECC Protect Address Range Mask (MASK):** Mask address for this address range of ECC protected space.
15:14	0h RO	**Reserved**
13:0	0000h RW	**ECC Protect Address Range Base (BASE):** Base address for this address range of ECC protected space.

3.77 ECC Data Storage Address (ECC_STORAGE_ADDR) — Offset DC2Ch

Specifies the address space that is reserved to store ECC data for all protected ranges. The address must be at least 32MB in size and aligned to the size as well.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + DC2Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:15	0h RO	**Reserved**
14:0	0000h RW	**Storage Address (ADDRESS):** Specifies the start Address of ECC data storage. Corresponds to CMI address [38:24] at the input of IBECC

3.78 ECC Protected VC0 Read Data Request Count (ECC_VC0_RD_REQCOUNT) — Offset DD20h

Register to count outgoing IBECC requests on each VC. Each request is a 64B cacheline request. Partial Writes are considered as a full write.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + DD20h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RW/V	**Counter Value (COUNT):** Number of requests issued to this vc.

3.79 ECC Protected VC1 Read Data Request Count (ECC_VC1_RD_REQCOUNT) — Offset DD28h

Register to count outgoing IBECC requests on each VC. Each request is a 64B cacheline request. Partial Writes are considered as a full write.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + DD28h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0000000000000000h RW/V	**Counter Value (COUNT):** Number of requests issued to this vc.

3.80 ECC Protected VC0 Write Data Request Count (ECC_VC0_WR_REQCOUNT) — Offset DD30h

Register to count outgoing IBECC requests on each VC. Each request is a 64B cacheline request. Partial Writes are considered as a full write.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + DD30h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:0	0000000000000000h RW/V	**Counter Value (COUNT):** Number of requests issued to this vc.

3.81 ECC Protected VC1 Write Data Request Count (ECC_VC1_WR_REQCOUNT) — Offset DD38h

Register to count outgoing IBECC requests on each VC. Each request is a 64B cacheline request. Partial Writes are considered as a full write.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + DD38h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000h RW/V	**Counter Value (COUNT):** Number of requests issued to this vc.

3.82 Unprotected VC0 Read Request Count (NOECC_VC0_RD_REQCOUNT) — Offset DD40h

Register to count outgoing IBECC requests on each VC. Each request is a 64B cacheline request. Partial Writes are considered as a full write.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + DD40h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000h RW/V	**Counter Value (COUNT):** Number of requests issued to this vc.

3.83 Unprotected VC1 Read Request Count (NOECC_VC1_RD_REQCOUNT) — Offset DD48h

Register to count outgoing IBECC requests on each VC. Each request is a 64B cacheline request. Partial Writes are considered as a full write.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + DD48h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000h RW/V	**Counter Value (COUNT):** Number of requests issued to this vc.

3.84 Unprotected VC0 Write Request Count (NOECC_VC0_WR_REQCOUNT) — Offset DD50h

Register to count outgoing IBECC requests on each VC. Each request is a 64B cacheline request. Partial Writes are considered as a full write.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + DD50h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000h RW/V	**Counter Value (COUNT):** Number of requests issued to this vc.

3.85 Unprotected VC1 Write Request Count (NOECC_VC1_WR_REQCOUNT) — Offset DD58h

Register to count outgoing IBECC requests on each VC. Each request is a 64B cacheline request. Partial Writes are considered as a full write.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + DD58h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000h RW/V	**Counter Value (COUNT):** Number of requests issued to this vc.

3.86 ECC Error Log (ECC_ERROR_LOG) — Offset DD70h

This register is used to store the CMI address information of the address block of main memory of which an error (single bit or multi-bit error) has occurred. Note that the address fields represent the address of the first single or the first multiple bit error occurrence after the error flag bits in the ERRSTS register have been cleared by software. An uncorrectable error will overwrite a correctable error. Once the error flag bits are set as a result of an error. This bit field is locked and doesn't change as a result of a new similar error until the error flag is cleared by software

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + DD70h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/1C/V/P	**Uncorrectable (Multiple-bit) Error Status (MERRSTS):** This bit is set when an uncorrectable multiple-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked until this bit is cleared. This field can be cleared by writing 1.

Bit Range	Default & Access	Field Name (ID): Description
62	0h RW/1C/V/P	**Correctable Error Status (CERRSTS):** This bit is set when a correctable single-bit error occurs on a memory read data transfer. When this bit is set, the address that caused the error and the error syndrome are also logged and they are locked to further single bit errors, until this bit is cleared. But, a multiple bit error that occurs after this bit is set will over-write the address/error syndrome info. Writing 1 to this field by software will clear this field.
61:46	0000h RO/V/P	**ECC Error Syndrome (ERRSYND):** Error Syndrome that is associated with the failing Cache Line
45:39	0h RO	**Reserved**
38:5	00000000 0h RO/V/P	**Error Address (ERRADD):** CMI address of the address block of main memory of which an error (single bit or multi-bit error) has occurred.
4:0	0h RO	**Reserved**

3.87 Parity Error Log (PARITY_ERR_LOG) — Offset DD78h

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + DD78h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/1C/V/P	**Error Status (ERR_STS):** Set by hardware, cleared by software when written to 1.
62:61	0h RO/V/P	**Error Type (ERR_TYPE):** Indicates the type of parity error (0x0 RSVD , 0x1 = write byte enable, 0x2 = write data, 0x3 = read data)
60	0h RO/V/P	**Transaction Type (TRANS_TYPE):** Indicates the transaction in which the parity error occurred (0x0 = Partial Write, 0x1 = Read)
59:39	0h RO	**Reserved**
38:5	00000000 0h RO/V/P	**Error Address (ERR_ADDRESS):** CMI address of the address block of main memory of which a parity error has occurred.
4:0	0h RO	**Reserved**

3.88 ECC Injection Address Mask (ECC_INJ_ADDR_MASK) — Offset DD80h

Address compares for ECC error injection is issued when ECC_Inj_Addr_Base[38:6] = ADDR[38:6] AND ECC_Inj_Addr_Mask[38:6].

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + DD80h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:6	00000000 0h RW	**ADDRESS:** Address Mask
5:0	0h RO	**Reserved**

3.89 ECC Error Injection Address Base (ECC_INJ_ADDR_BASE) — Offset DD88h

Address compares for ECC error injection is issued when ECC_Inj_Addr_Base[38:6] = ADDR[38:6] AND ECC_Inj_Addr_Mask[38:6].

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + DD88h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:6	00000000 0h RW	**ADDRESS:** Address Base
5:0	0h RO	**Reserved**

3.90 Parity Error Injection (PARITY_ERR_INJ) — Offset DD90h

The errors are injected by flipping the parity bits before they are checked by the parity checker. This allows it to check the parity checking and error reporting mechanism inside the IBECC.

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + DD90h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**Reserved**
17:16	0h RW	**Data Parity Injection Mask (ERR_INJ_MASK):** Specifies the checker that the data errors are injected on. 0x0: data parity injection is disabled (DATA_ERR_EN is ignored), 0x1: partial write data checker injection enable, 0x2: read data checker injection enable, 0x3: enable injection on both partial write data checker and read data checker
15:11	0h RO	**Reserved**
10:9	0h RW/V	**Byte Enable Parity Flip Enable (BE_ERR_EN):** 1 control bit per wbe parity bit received. Bit 0 is for lower 32B and bit 1 is for upper 32B. If set to 1, the byte enable parity bit received for the next partial write transaction will be inverted; This bit will be cleared to 1'b0 by HW after a transaction has been received with a parity error injected.
8	0h RO	**Reserved**
7:0	00h RW/V	**Data Parity Flip Enables (DATA_ERR_EN):** 1 control bit per data parity bit being generated; If set to 1, the corresponding data parity bit received for the next transaction will be inverted; This bit will be cleared to 1'b0 by HW after a transaction has been received with a parity error.

3.91 IBECC ECC Error Injection Control (ECC_INJ_CONTROL) — Offset DD98h

Type	Size	Offset	Default
MMIO	32 bit	MCHBAR + DD98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	00h RW	**Injection Count (COUNT):** When ECC_INJECT mode is set to 0x2 or 0x4, inject an ECC error every time this counter expires. The ECC_Inject_Count is incremented every time that a cache line is issued by IBECC
7:3	0h RO	**Reserved**
2:0	0h RW	**ECC Error Injection Mode (ECC_INJECT):** Configures the error injection mechanism; 000b: No ECC error injection, 001b: Inject a correctable ECC error on the ECC_INJ_ADDR_COMPARE register match, 011b: Inject a correctable ECC error on the ECC error insertion counter, 101b: Inject a non-recoverable ECC error on the ECC_INJ_ADDR_COMPARE register match, 111b: Inject a non-recoverable ECC error on the ECC error insertion counter

3.92 Request Counter (ECC_VC0_SYND_RD_REQCOUNT) — Offset DDC0h

Register to count outgoing IBECC requests on each VC. Each request is a 64B cacheline request. Partial Writes are considered as a full write.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + DDC0h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RW/V	**Counter Value (COUNT):** Number of requests issued to this vc.

3.93 Request Counter (ECC_VC1_SYND_RD_REQCOUNT) — Offset DDC8h

Register to count outgoing IBECC requests on each VC. Each request is a 64B cacheline request. Partial Writes are considered as a full write.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + DDC8h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000 h RW/V	**Counter Value (COUNT):** Number of requests issued to this vc.

3.94 Request Counter (ECC_VC0_SYND_WR_REQCOUNT) — Offset DDD0h

Register to count outgoing IBECC requests on each VC. Each request is a 64B cacheline request. Partial Writes are considered as a full write.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + DDD0h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000h RW/V	**Counter Value (COUNT):** Number of requests issued to this vc.

3.95 Request Counter (ECC_VC1_SYND_WR_REQCOUNT) — Offset DDD8h

Register to count outgoing IBECC requests on each VC. Each request is a 64B cacheline request. Partial Writes are considered as a full write.

Type	Size	Offset	Default
MMIO	64 bit	MCHBAR + DDD8h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:0	00000000 00000000h RW/V	**Counter Value (COUNT):** Number of requests issued to this vc.

4 Direct Media Interface BAR (DMIBAR) Registers

This chapter documents the DMIBAR registers. Base address of these registers is defined in the DMIBAR_0_0_0_PCI register in Bus: 0, Device: 0, Function: 0.

Table 4-1. Summary of DMIBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	DMIVCECH_0_0_0_DMIBAR	04010002h
4h	4	DMIPVCCAP1_0_0_0_DMIBAR	00000000h
8h	4	DMIPVCCAP2_0_0_0_DMIBAR	00000000h
Ch	2	DMIPVCCTL_0_0_0_DMIBAR	0000h
10h	4	DMIVC0RCAP_0_0_0_DMIBAR	00000001h
1Ch	4	DMIVC1RCAP_0_0_0_DMIBAR	00000001h
26h	2	DMIVC1RSTS_0_0_0_DMIBAR	0002h
34h	4	DMIVCMRCAP_0_0_0_DMIBAR	00008000h
38h	4	DMIVCMRCTL_0_0_0_DMIBAR	07000180h
3Eh	2	DMIVCMRSTS_0_0_0_DMIBAR	0002h
40h	4	DMIRCLDECH_0_0_0_DMIBAR	08010005h
44h	4	DMIESD_0_0_0_DMIBAR	01000202h
50h	4	DMILE1D_0_0_0_DMIBAR	00000000h
5Ch	4	DMILUE1A_0_0_0_DMIBAR	00000000h
60h	4	DMILE2D_0_0_0_DMIBAR	00000000h
68h	4	DMILE2A_0_0_0_DMIBAR	00000000h
88h	2	LCTL_0_0_0_DMIBAR	0000h
1C4h	4	DMIUESTS_0_0_0_DMIBAR	00000000h
1C8h	4	DMIUEMSK_0_0_0_DMIBAR	00000000h
1CCh	4	DMIUESEV_0_0_0_DMIBAR	00060010h
1D0h	4	DMICESTS_0_0_0_DMIBAR	00000000h
1D4h	4	DMICEMSK_0_0_0_DMIBAR	00002000h

4.1 DMIVCECH_0_0_0_DMIBAR - Offset 0h

Indicates DMI Virtual Channel capabilities.

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 0h	04010002h

Bit Range	Default & Access	Field Name (ID): Description
31:20	40h RO	**PNC:** Pointer to Next Capability: This field contains the offset to the next PCI Express capability structure in the linked list of capabilities (Link Declaration Capability).
19:16	1h RO	**PCIEVCCV:** PCI Express Virtual Channel Capability Version: Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification. ***Note:*** This version does not change for 2.0 compliance.
15:0	2h RO	**ECID:** Extended Capability ID: Value of 0002h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

4.2 DMIPVCCAP1_0_0_0_DMIBAR - Offset 4h

Describes the configuration of PCI Express Virtual Channels associated with this port.

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0h RO	**Reserved**
6:4	0h RO	**LPEVCC:** Low Priority Extended VC Count: Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	0h RO	**Reserved**
2:0	0h RW/L	**EVCC:** Extended VC Count: Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. The Private Virtual Channel, VC1 and the Manageability Virtual Channel are not included in this count. **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.EVCCDWOS

4.3 DMIPVCCAP2_0_0_0_DMIBAR - Offset 8h

Describes the configuration of PCI Express Virtual Channels associated with this port.

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**VCATO:** Reserved.
23:8	0h RO	**Reserved**
7:0	0h RO	**VCAC:** Reserved.

4.4 DMIPVCCTL_0_0_0_DMIBAR - Offset Ch

Type	Size	Offset	Default
MEM	16 bit	DMIBAR + Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:4	0h RO	**Reserved**
3:1	0h RW	**VCAS:** VC Arbitration Select: This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. The value 000b when written to this field indicates the VC arbitration scheme is hardware fixed (in the root complex). This field cannot be modified when more than one VC in the LPVC group is enabled. 000: Hardware fixed arbitration scheme. E.G. Round Robin Others: Reserved.
0	0h RO	**LVCAT:** Reserved.

4.5 DMIVC0RCAP_0_0_0_DMIBAR - Offset 10h

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 10h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**PATO:** Reserved.
23	0h RO	**Reserved**
22:16	0h RO	**MTS:** Reserved.

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**REJSNPT:** Reject Snoop Transactions: 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction for which the No Snoop attribute is applicable but is not set within the TLP Header will be rejected as an Unsupported Request.
14:8	0h RO	**Reserved**
7:0	1h RO	**PAC:** Port Arbitration Capability: Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

4.6 DMIVC1RCAP_0_0_0_DMIBAR - Offset 1Ch

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 1Ch	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**PATO:** Reserved.
23	0h RO	**Reserved**
22:16	0h RO	**MTS:** Reserved.
15	0h RO	**REJSNPT:** Reject Snoop Transactions: 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP Header will be rejected as an Unsupported Request.
14:8	0h RO	**Reserved**
7:0	1h RO	**PAC:** Port Arbitration Capability: Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

4.7 DMIVC1RSTS_0_0_0_DMIBAR - Offset 26h

Reports the Virtual Channel specific status.

Type	Size	Offset	Default
MEM	16 bit	DMIBAR + 26h	0002h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	1h RO/V	**VC1NP:** Virtual Channel 1 Negotiation Pending: 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). Software may use this bit when enabling or disabling the VC. This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	0h RO	**Reserved**

4.8 DMIVCMRCAP_0_0_0_DMIBAR - Offset 34h

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 34h	00008000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	1h RO	**REJSNPT:** Reject Snoop Transactions: 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on the VC. 1: When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP Header will be rejected as an Unsupported Request.
14:0	0h RO	**Reserved**

4.9 DMIVCMRCTL_0_0_0_DMIBAR - Offset 38h

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 38h	07000180h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**VCMEN:** Virtual Channel enable: 0: Virtual Channel is disabled. 1: Virtual Channel is enabled. See exceptions below. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. When VC Negotiation Pending bit is cleared, a 1 read from this VC Enable bit indicates that the VC is enabled (Flow Control Initialization is completed for the PCI Express port). A 0 read from this bit indicates that the Virtual Channel is currently disabled. BIOS Requirement: 1. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be set in both Components on a Link. 2. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both Components on a Link. 3. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 4. Software must fully disable a Virtual Channel in both Components on a Link before re-enabling the Virtual Channel.
30:27	0h RO	**Reserved**
26:24	7h RW	**VCID:** Virtual Channel ID: Assigns a VC ID to the VC resource. Assigned value must be non-zero. This field cannot be modified when the VC is already enabled.
23:13	0h RO	**Reserved**
12:8	1h RW/V/L	**FC_FSM_STATE:** This register is for Save Restore to restore the FC fsm.
7:0	80h RO	**TCVCMMAP:** Traffic Class/Virtual Channel Map: Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.

4.10 DMIVCMRSTS_0_0_0_DMIBAR - Offset 3Eh

Type	Size	Offset	Default
MEM	16 bit	DMIBAR + 3Eh	0002h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	1h RO/V	**VCNEGPND:** Virtual Channel Negotiation Pending: 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). Software may use this bit when enabling or disabling the VC. This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	0h RO	**Reserved**

4.11 DMIRCLDECH_0_0_0_DMIBAR - Offset 40h

This capability declares links from the respective element to other elements of the root complex component to which it belongs and to an element in another root complex component. See PCI Express specification for link/topology declaration requirements.

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 40h	08010005h

Bit Range	Default & Access	Field Name (ID): Description
31:20	80h RO	**PNC:** Pointer to Next Capability: This field contains the offset to the next PCI Express capability structure in the linked list of capabilities (Internal Link Control Capability).
19:16	1h RO	**LDCV:** Link Declaration Capability Version: Hardwired to 1 to indicate compliancies with the 1.1 version of the PCI Express specification. ***Note:*** This version does not change for 2.0 compliance.
15:0	5h RO	**ECID:** Extended Capability ID: Value of 0005h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability.

4.12 DMIESD_0_0_0_DMIBAR - Offset 44h

Provides information about the root complex element containing this Link Declaration Capability.

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 44h	01000202h

Bit Range	Default & Access	Field Name (ID): Description
31:24	1h RO	**PORTNUM:** Port Number: Specifies the port number associated with this element with respect to the component that contains this element. This port number value is utilized by the egress port of the component to provide arbitration to this Root Complex Element.
23:16	0h RW/L	**CID:** Component ID: Identifies the physical component that contains this Root Complex Element. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS). **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.CIDDWOS
15:8	2h RO	**NLE:** Number of Link Entries: Indicates the number of link entries following the Element Self Description. This field reports 2 (one for MCH egress port to main memory and one to egress port belonging to ICH on other side of internal link).
7:4	0h RO	**Reserved**
3:0	2h RO	**ETYP:** Element Type: Indicates the type of the Root Complex Element. Value of 2h represents an Internal Root Complex Link (DMI).

4.13 DMILE1D_0_0_0_DMIBAR - Offset 50h

First part of a Link Entry which declares an internal link to another Root Complex Element.

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 50h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/L	**TPN:** Target Port Number: Specifies the port number associated with the element targeted by this link entry (egress port of PCH). The target port number is with respect to the component that contains this element as specified by the target component ID. This can be programmed by BIOS, but the default value will likely be correct because the DMI RCRB in the PCH will likely be associated with the default egress port for the PCH meaning it will be assigned port number 0. **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.TPNWOS
23:16	0h RW/L	**TCID:** Target Component ID: Identifies the physical component that is targeted by this link entry. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS). **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.TCIDE1DWOS

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RO	**LTYP:** Link Type: Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	0h RW/L	**LV:** Link Valid: 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link. **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.LVE1DWOS

4.14 DMILUE1A_0_0_0_DMIBAR - Offset 5Ch

Second part of a Link Entry which declares an internal link to another Root Complex Element.

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 5Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	0h RW/L	**ULA:** Upper Link Address: Memory mapped base address of the RCRB that is the target element (egress port of PCH) for this link entry. **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.ULAE1DWOS

4.15 DMILE2D_0_0_0_DMIBAR - Offset 60h

First part of a Link Entry which declares an internal link to another Root Complex Element.

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 60h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**TPN:** Target Port Number: Specifies the port number associated with the element targeted by this link entry (Egress Port). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	0h RW/L	**TCID:** Target Component ID: Identifies the physical or logical component that is targeted by this link entry. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS). **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.TCIDE2DWOS
15:2	0h RO	**Reserved**
1	0h RO	**LTYP:** Link Type: Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	0h RW/L	**LV:** Link Valid: 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link. **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.LVE2DWOS

4.16 DMILE2A_0_0_0_DMIBAR - Offset 68h

Second part of a Link Entry which declares an internal link to another Root Complex Element.

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW/L	**LA:** Link Address: Memory mapped base address of the RCRB that is the target element (Egress Port) for this link entry. **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.LAE2DWOS
11:0	0h RO	**Reserved**

4.17 LCTL_0_0_0_DMIBAR - Offset 88h

Allows control of PCI Express link.

Type	Size	Offset	Default
MEM	16 bit	DMIBAR + 88h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	**Reserved**
9	0h RO	**HAWD:** OPI - N/A Hardware Autonomous Width Disable: Hardware Autonomous Width Disable - When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Devices that do not implement the ability autonomously to change Link width are permitted to hardwire this bit to 0b.
8	0h RO	**Reserved**
7	0h RW	**ES:** OPI - N/A Extended Synch: Extended synch. 0: Standard Fast Training Sequence (FTS). 1: Forces the transmission of additional ordered sets when exiting the L0s state and when in the Recovery state. This mode provides external devices (e.g., logic analyzers) monitoring the Link time to achieve bit and symbol lock before the link enters L0 and resumes communication. This is a test mode only and may cause other undesired side effects such as buffer overflows or underruns.
6	0h RO	**Reserved**
5	0h RO	**RL:** Retrain Link: 0: Normal operation. 1: Full Link retraining is initiated by directing the Physical Layer LTSSM from L0, L0s, or L1 states to the Recovery state. This bit always returns 0 when read. This bit is cleared automatically (no need to write a 0).
4:2	0h RO	**Reserved**
1:0	0h RO	**ASPM:** Active State PM: Controls the level of active state power management supported on the given link. 00: Disabled. 01: L0s Entry Supported. 10: L1 Entry Supported. 11: L0s and L1 Entry Supported.

4.18 DMIUESTS_0_0_0_DMIBAR - Offset 1C4h

DMI Uncorrectable Error Status register. This register is for test and debug purposes only.

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 1C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RW/1C/V/P	**URES:** Unsupported Request Error Status.
19	0h RO	**Reserved**
18	0h RW/1C/V/P	**MTLPS:** Malformed TLP Status.
17	0h RW/1C/V/P	**ROS:** Receiver Overflow Status.
16	0h RW/1C/V/P	**UCS:** Unexpected Completion Status.
15	0h RO	**Reserved**
14	0h RW/1C/V/P	**CTS:** Completion Timeout Status.
13	0h RO	**Reserved**
12	0h RW/1C/V/P	**PTLPS:** Poisoned TLP Status.
11:5	0h RO	**Reserved**
4	0h RW/1C/V/P	**DLPES:** Data Link Protocol Error Status.
3:0	0h RO	**Reserved**

4.19 DMIUEMSK_0_0_0_DMIBAR - Offset 1C8h

DMI Uncorrectable Error Mask register. This register is for test and debug purposes only.

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 1C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22	0h RW/P	**ECCERRM:** 2 Bit Error Mask.
21	0h RO	**Reserved**
20	0h RW/P	**UREM:** Unsupported Request Error Mask.
19	0h RO	**Reserved**
18	0h RW/P	**MTLPM:** Malformed TLP Mask.
17	0h RW/P	**ROM:** Receiver Overflow Mask.
16	0h RW/P	**UCM:** Unexpected Completion Mask.
15	0h RO	**Reserved**
14	0h RW/P	**CPLTM:** Completion Timeout Mask.
13	0h RO	**Reserved**
12	0h RW/P	**PTLPM:** Poisoned TLP Mask.
11:5	0h RO	**Reserved**
4	0h RW/P	**DLPEM:** Data Link Protocol Error Mask.
3:0	0h RO	**Reserved**

4.20 DMIUESEV_0_0_0_DMIBAR - Offset 1CCh

DMI Uncorrectable Error Severity register. This register controls whether an individual error is reported as a non-fatal or fatal error. An error is reported as fatal when the corresponding error bit in the severity register is set. If the bit is cleared, the corresponding error is considered nonfatal. It is for test and debug purposes only.

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 1CCh	00060010h

Bit Range	Default & Access	Field Name (ID): Description
31:23	0h RO	**Reserved**
22	0h RW/P	**ECCERRS:** 2 Bit Error Mask.
21	0h RO	**Reserved**
20	0h RW/P	**URES:** Unsupported Request Error Severity.
19	0h RO	**ECRCES:** Reserved.
18	1h RW/P	**MTLPES:** Malformed TLP Error Severity.
17	1h RW/P	**ROEV:** Receiver Overflow Error Severity.
16	0h RW/P	**UCES:** Unexpected Completion Error Severity.
15	0h RO	**CAES:** Reserved.
14	0h RW/P	**CTES:** Completion Timeout Error Severity.
13	0h RO	**FCPES:** Reserved.
12	0h RW/P	**PTLPES:** Poisoned TLP Error Severity.
11:5	0h RO	**Reserved**
4	1h RW/P	**DLPES:** Data Link Protocol Error Severity.
3:0	0h RO	**Reserved**

4.21 DMICESTS_0_0_0_DMIBAR - Offset 1D0h

DMI Correctable Error Status Register. This register is for test and debug purposes only.

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 1D0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	0h RW/1C/V/P	**ANFES:** Advisory Non-Fatal Error Status: When set, indicates that an Advisory Non-Fatal Error occurred.
12	0h RW/1C/V/P	**RTTS:** Replay Timer Timeout Status.
11:9	0h RO	**Reserved**
8	0h RW/1C/V/P	**RNRS:** REPLAY_NUM Rollover Status.
7	0h RW/1C/V/P	**BDLLPS:** Bad DLLP Status.
6	0h RW/1C/V/P	**BTLPS:** Bad TLP Status.
5:1	0h RO	**Reserved**
0	0h RW/1C/V/P	**RES:** Receiver Error Status: Physical layer receiver Error occurred. These errors include: elastic Buffer Collision, 8b/10b error, De-skew Timeout Error.

4.22 DMICEMSK_0_0_0_DMIBAR - Offset 1D4h

DMI Correctable Error Mask register. This register is for test and debug purposes only.

Type	Size	Offset	Default
MEM	32 bit	DMIBAR + 1D4h	00002000h

Bit Range	Default & Access	Field Name (ID): Description
31:14	0h RO	**Reserved**
13	1h RW/P	**ANFEM:** Advisory Non-Fatal Error Mask: When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register, and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12:0	0h RO	**Reserved**

5 PXPEPBAR Registers

This chapter documents the PXPEPBAR registers. Base address of these registers is defined in the PXPEPBAR_0_0_0_PCI register in Bus: 0, Device: 0, Function: 0.

Table 5-1. Summary of PXPEPBAR Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
Ch	2	EPPVCCTL_0_0_0_PXPEPBAR	0000h
44h	4	EPESD_0_0_0_PXPEPBAR	00000501h

5.1 EPPVCCTL_0_0_0_PXPEPBAR - Offset Ch

Type	Size	Offset	Default
MEM	16 bit	PXPEPBAR + Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:4	0h RO	**Reserved**
3:1	0h RW	**VCAS:** VC Arbitration Select: This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. The value 000b when written to this field will indicate the VC arbitration scheme is hardware fixed (in the root complex). This field cannot be modified when more than one VC in the LPVC group is enabled.
0	0h RO	**LVCAT:** Reserved

5.2 EPESD_0_0_0_PXPEPBAR - Offset 44h

Provides information about the root complex element containing this Link Declaration Capability.

Type	Size	Offset	Default
MEM	32 bit	PXPEPBAR + 44h	00000501h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**PN:** Port Number: This field specifies the port number associated with this element with respect to the component that contains this element. Value of 00 h indicates to configuration software that this is the default egress port.
23:16	0h RW/L	**CID:** Component ID: Identifies the physical component that contains this Root Complex Element. BIOS Requirement: Must be initialized according to guidelines in the PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS). **Locked by:** TLDMIREGS.WO_STATUS0_0_0_0_DMIBAR.CIDPWOS
15:8	5h RO	**NLE:** Number of Link Entries: Indicates the number of link entries following the Element Self Description. This field reports 5 (one each for PEG0, PEG11 PEG12, PEG1 and DMI).
7:4	0h RO	**Reserved**
3:0	1h RO	**ET:** Element Type: Indicates the type of the Root Complex Element. Value of 1h represents a port to system memory.

6 VTDPVC0BAR Registers

This chapter documents the VC0PREMAP BAR registers. Base address of these registers is defined in the VTDPVC0BAR_0_0_0_MCHBAR_NCU register which resides in the MCHBAR register collection.

Table 6-1. Summary of VTDPVC0BAR Registers (Sheet 1 of 2)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Version Register (VER_REG_0_0_0_VTDBAR)	00000010h
8h	8	Capability Register (CAP_REG_0_0_0_VTDBAR)	00D2008C40660462h
10h	8	Extended Capability Register (ECAP_REG_0_0_0_VTDBAR)	0000000000F050DAh
18h	4	Global Command Register (GCMD_REG_0_0_0_VTDBAR)	00000000h
1Ch	4	Global Status Register (GSTS_REG_0_0_0_VTDBAR)	00000000h
20h	8	Root Table Address Register (RTADDR_REG_0_0_0_VTDBAR)	0000000000000000h
28h	8	Context Command Register (CCMD_REG_0_0_0_VTDBAR)	0800000000000000h
34h	4	Fault Status Register (FSTS_REG_0_0_0_VTDBAR)	00000000h
38h	4	Fault Event Control Register (FECTL_REG_0_0_0_VTDBAR)	80000000h
3Ch	4	Fault Event Data Register (FEDATA_REG_0_0_0_VTDBAR)	00000000h
40h	4	Fault Event Address Register (FEADDR_REG_0_0_0_VTDBAR)	00000000h
44h	4	Fault Event Upper Address Register (FEUADDR_REG_0_0_0_VTDBAR)	00000000h
58h	8	Advanced Fault Log Register (AFLOG_REG_0_0_0_VTDBAR)	0000000000000000h
64h	4	Protected Memory Enable Register (PMEN_REG_0_0_0_VTDBAR)	00000000h
68h	4	Protected Low Memory Base Register (PLMBASE_REG_0_0_0_VTDBAR)	00000000h
6Ch	4	Protected Low-Memory Limit Register (PLMLIMIT_REG_0_0_0_VTDBAR)	00000000h
70h	8	Protected High-Memory Base Register (PHMBASE_REG_0_0_0_VTDBAR)	0000000000000000h
78h	8	Protected High-Memory Limit Register (PHMLIMIT_REG_0_0_0_VTDBAR)	0000000000000000h
80h	8	Invalidation Queue Head Register (IQH_REG_0_0_0_VTDBAR)	0000000000000000h
88h	8	Invalidation Queue Tail Register (IQT_REG_0_0_0_VTDBAR)	0000000000000000h
90h	8	Invalidation Queue Address Register (IQA_REG_0_0_0_VTDBAR)	0000000000000000h
9Ch	4	Invalidation Completion Status Register (ICS_REG_0_0_0_VTDBAR)	00000000h
A0h	4	Invalidation Event Control Register (IECTL_REG_0_0_0_VTDBAR)	80000000h
A4h	4	Invalidation Event Data Register (IEDATA_REG_0_0_0_VTDBAR)	00000000h

Table 6-1. Summary of VTDPVC0BAR Registers (Sheet 2 of 2)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
A8h	4	Invalidation Event Address Register (IEADDR_REG_0_0_0_VTDBAR)	00000000h
ACh	4	Invalidation Event Upper Address Register (IEUADDR_REG_0_0_0_VTDBAR)	00000000h
B8h	8	Interrupt Remapping Table Address Register (IRTA_REG_0_0_0_VTDBAR)	0000000000000000h
DCh	4	Page Request Status Register (PRESTS_REG_0_0_0_VTDBAR)	00000000h
E0h	4	Page Request Event Control Register (PRECTL_REG_0_0_0_VTDBAR)	80000000h
E4h	4	Page Request Event Data Register (PREDATA_REG_0_0_0_VTDBAR)	00000000h
E8h	4	Page Request Event Address Register (PREADDR_REG_0_0_0_VTDBAR)	00000000h
ECh	4	Page Request Event Upper Address Register (PREUADDR_REG_0_0_0_VTDBAR)	00000000h
400h	8	Fault Recording Register Low [0] (FRCDL_REG_0_0_0_VTDBAR)	0000000000000000h
408h	8	Fault Recording Register High [0] (FRCDH_REG_0_0_0_VTDBAR)	0000000000000000h
500h	8	Invalidate Address Register (IVA_REG_0_0_0_VTDBAR)	0000000000000000h
508h	8	IOTLB Invalidate Register (IOTLB_REG_0_0_0_VTDBAR)	0200000000000000h

6.1 Version Register (VER_REG_0_0_0_VTDBAR) - Offset 0h

Register to report the architecture version supported. Backward compatibility for the architecture is maintained with new revision numbers, allowing software to load remapping hardware drivers written for prior architecture versions.

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + 0h	00000010h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:4	1h RO	**Major Version Number (MAJOR):** Indicates supported architecture version.
3:0	0h RO	**Minor Version Number (MINOR):** Indicates supported architecture minor version.

6.2 Capability Register (CAP_REG_0_0_0_VTDBAR) - Offset 8h

Register to report general remapping hardware capabilities.

Type	Size	Offset	Default
MEM	64 bit	VTDPVC0BAR + 8h	00D2008C40660462h

Bit Range	Default & Access	Field Name (ID): Description
63:57	0h RO	**Reserved**
56	0h RO	**First Level 64-KByte Page SupportP (FL1GP):** A value of 1 in this field indicates 1-GByte page size is supported for first-level translation.
55	1h RO	**Read Draining (DRD):** • 0 = Hardware does not support draining of DMA read requests. • 1 = Hardware supports draining of DMA read requests.
54	1h RO	**Write Draining (DWD):** • 0 = Hardware does not support draining of DMA write requests. • 1 = Hardware supports draining of DMA write requests.
53:48	12h RO	**Maximum Address Mask Value (MAMV):** The value in this field indicates the maximum supported value for the Address Mask (AM) field in the Invalidation Address register (IVA_REG) and IOTLB Invalidation Descriptor (iotlb_inv_dsc) used for invalidations of second-level translation. This field is valid only when the PSI field in Capability register is reported as Set.
47:40	0h RO	**Number of Fault-Recording Registers (NFR):** Number of fault recording registers is computed as N+1, where N is the value reported in this field. Implementations must support at least one fault recording register (NFR = 0) for each remapping hardware unit in the platform. The maximum number of fault recording registers per remapping hardware unit is 256.
39	1h RO	**Page Selective Invalidation (PSI):** • 0 = Hardware supports only domain and global invalidates for IOTLB. • 1 = Hardware supports page selective, domain and global invalidates for IOTLB. Hardware implementations reporting this field as set are recommended to support a Maximum Address Mask Value (MAMV) value of at least 9 (or 18 if supporting 1GB pages with second level translation).
38	0h RO	**Reserved**
37:34	3h RO	**Second Level Large Page Support (SLLPS):** This field indicates the super page sizes supported by hardware.A value of 1 in any of these bits indicates the corresponding super-page size is supported. The super-page sizes corresponding to various bit positions within this field are: • 0 = 21-bit offset to page frame (2MB) • 1 = 30-bit offset to page frame (1GB) • 2 = 39-bit offset to page frame (512GB) • 3 = 48-bit offset to page frame (1TB) Hardware implementations supporting a specific super-page size must support all smaller super-page sizes, i.e. only valid values for this field are 0000b, 0001b, 0011b, 0111b, 1111b.

Bit Range	Default & Access	Field Name (ID): Description
33:24	40h RO	**Fault-Recording Register Offset (FRO):** This field specifies the location to the first fault recording register relative to the register base address of this remapping hardware unit. If the register base address is X, and the value reported in this field is Y, the address for the first fault recording register is calculated as X+(16*Y).
23	0h RO	**Reserved**
22	1h RO	**Zero Length Read (ZLR):** • 0 = Indicates the remapping hardware unit blocks (and treats as fault) zero length DMA read requests to write-only pages. • 1 = Indicates the remapping hardware unit supports zero length DMA read requests to write-only pages. DMA remapping hardware implementations are recommended to report ZLR field as Set.
21:16	26h RO	**Maximum Guest Address Width (MGAW):** This field indicates the maximum DMA virtual addressability supported by remapping hardware. The Maximum Guest Address Width (MGAW) is computed as (N+1), where N is the value reported in this field. For example, a hardware implementation supporting 48-bit MGAW reports a value of 47 (101111b) in this field. If the value in this field is X, untranslated and translated DMA requests to addresses above 2(x+1)-1 are always blocked by hardware. Translations request to address above 2(x+1)-1 from allowed devices return a null Translation Completion Data Entry with R=W=0.Guest addressability for a given DMA request is limited to the minimum of the value reported through this field and the adjusted guest address width of the corresponding page-table structure. (Adjusted guest address widths supported by hardware are reported through the SAGAW field). Implementations are recommended to support MGAW at least equal to the physical addressability (host address width) of the platform.
15:13	0h RO	**Reserved**
12:8	4h RO	**Supported Adjusted Guest Address Widths (SAGAW):** This 5-bit field indicates the supported adjusted guest address widths (which in turn represents the levels of page-table walks for the 4KB base page size) supported by the hardware implementation.A value of 1 in any of these bits indicates the corresponding adjusted guest address width is supported. The adjusted guest address widths corresponding to various bit positions within this field are: • 0 = 30-bit AGAW (2-level page table) • 1 = 39-bit AGAW (3-level page table) • 2 = 48-bit AGAW (4-level page table) • 3 = 57-bit AGAW (5-level page table) • 4 = 64-bit AGAW (6-level page table) Software must ensure that the adjusted guest address width used to setup the page tables is one of the supported guest address widths reported in this field.
7	0h RO	**Caching Mode (CM):** • 0 = Not-present and erroneous entries are not cached in any of the remapping caches. Invalidations are not required for modifications to individual not present or invalid entries. However, any modifications that result in decreasing the effective permissions or partial permission increases require invalidations for them to be effective. • 1 = Not-present and erroneous mappings may be cached in the remapping caches. Any software updates to the remapping structures (including updates to not-present or erroneous entries) require explicit invalidation. Hardware implementations of this architecture must support a value of 0 in this field.
6	1h RO	**Protected High-Memory Region (PHMR):** • 0 = Indicates protected high-memory region is not supported. • 1 = Indicates protected high-memory region is supported.

Bit Range	Default & Access	Field Name (ID): Description
5	1h RO	**Protected Low-Memory Region (PLMR):** • 0 = Indicates protected low-memory region is not supported. • 1 = Indicates protected low-memory region is supported.
4	0h RO	**Required Write-Buffer Flushing (RWBF):** • 0 = Indicates no write-buffer flushing is needed to ensure changes to memory-resident structures are visible to hardware. • 1 = Indicates software must explicitly flush the write buffers to ensure updates made to memory-resident remapping structures are visible to hardware.
3	0h RO	**Advanced Fault Logging (AFL):** • 0 = Indicates advanced fault logging is not supported. Only primary fault logging is supported. • 1 = Indicates advanced fault logging is supported.
2:0	2h RO	**Number of Domains Supported (ND):** • 000b = Hardware supports 4-bit domain-ids with support for up to 16 domains. • 001b = Hardware supports 6-bit domain-ids with support for up to 64 domains. • 010b = Hardware supports 8-bit domain-ids with support for up to 256 domains. • 011b = Hardware supports 10-bit domain-ids with support for up to 1024 domains. • 100b = Hardware supports 12-bit domain-ids with support for up to 4K domains. • 100b = Hardware supports 14-bit domain-ids with support for up to 16K domains. • 110b = Hardware supports 16-bit domain-ids with support for up to 64K domains. • 111b = Reserved.

6.3 Extended Capability Register (ECAP_REG_0_0_0_VTDBAR) - Offset 10h

Register to report remapping hardware extended capabilities.

Type	Size	Offset	Default
MEM	64 bit	VTDPVC0BAR + 10h	0000000000F050DAh

Bit Range	Default & Access	Field Name (ID): Description
63:41	0h RO	**Reserved**
40	0h RO	**Process Address Space ID Support (PASID):** • 0 = Hardware does not support requests tagged with Process Address Space IDs. • 1 = Hardware supports requests tagged with Process Address Space IDs.
39:35	0h RO	**PASID Size Supported (PSS):** This field reports the PASID size supported by the remapping hardware for requests-with-PASID. A value of N in this field indicates hardware supports PASID field of N+1 bits (For example, value of 7 in this field, indicates 8-bit PASIDs are supported).Requests-with-PASID with PASID value beyond the limit specified by this field are treated as error by the remapping hardware. This field is valid only when PASID field is reported as Set.

Bit Range	Default & Access	Field Name (ID): Description
34	0h RO	**Extended Accessed Flag Support (EAFS):** • 0 = Hardware does not support the extended-accessed (EA) bit in first-level paging-structure entries. • 1 = Hardware supports the extended accessed (EA) bit in first-level paging-structure entries. This field is valid only when PASID field is reported as Set.
33	0h RO	**No Write Flag Support (NWFS):** • 0 = Hardware ignores the No Write (NW) flag in Device-TLB translation requests, and behaves as if NW is always 0. • 1 = Hardware supports the No Write (NW) flag in Device-TLB translation requests. This field is valid only when Device-TLB support (DT) field is reported as Set.
32	0h RO	**PASID-Only Translations (POT):** • 0 = Hardware does not support PASID-only Translation Type in extended-context-entries. • 1 = Hardware supports PASID-only Translation Type in extended-context-entries. This field is valid only when PASID field is reported as Set.
31	0h RO	**Supervisor Request Support (SRS):** • 0 = H/W does not support requests-with-PASID seeking supervisor privilege. • 1 = H/W supports requests-with-PASID seeking supervisor privilege. The field is valid only when PASID field is reported as Set.
30	0h RO	**Execute Request Support (ERS):** • 0 = H/W does not support requests-with-PASID seeking execute permission. • 1 = H/W supports requests-with-PASID seeking execute permission. This field is valid only when PASID field is reported as Set.
29	0h RO	**Page Request Support (PRS):** • 0 = Hardware does not support Page Requests. • 1 = Hardware supports Page Requests This field is valid only when Device-TLB (DT) field is reported as Set.
28	0h RO	**IGN:** Ignore this field
27	0h RO	**Deferred Invalidate Support (DIS):** • 0 = Hardware does not support deferred invalidations of IOTLB and Device-TLB. • 1 = Hardware supports deferred invalidations of IOTLB and Device-TLB. This field is valid only when PASID field is reported as Set.
26	0h RO	**Nested Translation Support (NEST):** • 0 = Hardware does not support nested translations. • 1 = Hardware supports nested translations. This field is valid only when PASID field is reported as Set.
25	0h RO	**Memory Type Support (MTS):** • 0 = Hardware does not support Memory Type in first-level translation and Extended Memory type in second-level translation. • 1 = Hardware supports Memory Type in first-level translation and Extended Memory type in second-level translation. This field is valid only when PASID and ECS fields are reported as Set. Remapping hardware units with, one or more devices that operate in processor coherency domain, under its scope must report this field as Set.
24	0h RO	**Extended Context Support (ECS):** • 0 = Hardware does not support extended-root-entries and extended-context-entries. • 1 = Hardware supports extended-root-entries and extended-context-entries. Implementations reporting PASID or PRS fields as Set, must report this field as Set.

Bit Range	Default & Access	Field Name (ID): Description
23:20	Fh RO	**Maximum Handle Mask Value (MHMV):** The value in this field indicates the maximum supported value for the Handle Mask (HM) field in the interrupt entry cache invalidation descriptor (iec_inv_dsc).This field is valid only when the IR field in Extended Capability register is reported as Set.
19:18	0h RO	**Reserved**
17:8	50h RO	**IOTLB Register Offset (IRO):** This field specifies the offset to the IOTLB registers relative to the register base address of this remapping hardware unit. If the register base address is X, and the value reported in this field is Y, the address for the first IOTLB invalidation register is calculated as X+(16*Y).
7	1h RO	**Snoop Control (SC):** • 0 = Hardware does not support 1-setting of the SNP field in the page-table entries. • 1 = Hardware supports the 1-setting of the SNP field in the page-table entries.
6	1h RO	**Pass Through (PT):** • 0 = Hardware does not support pass-through translation type in context entries and extended-context-entries. • 1 = Hardware supports pass-through translation type in context entries and extended-context-entries. Pass-through translation is specified through Translation-Type (T) field value of 10b in context-entries, or T field value of 010b in extended-context-entries.Hardware implementations supporting PASID must report a value of 1b in this field.
5	0h RO	**Reserved**
4	1h RO	**Extended Interrupt Mode (EIM):** • 0 = On Intel64 platforms, hardware supports only 8-bit APIC-IDs (xAPIC mode). • 1 = On Intel64 platforms, hardware supports 32-bit APIC-IDs (x2APIC mode). This field is valid only on Intel64 platforms reporting Interrupt Remapping support (IR field Set).
3	1h RO	**Interrupt Remapping Support (IR):** • 0 = Hardware does not support interrupt remapping. • 1 = Hardware supports interrupt remapping. Implementations reporting this field as Set must also support Queued Invalidation (QI).
2	0h RO	**Device-TLB Support (DT):** • 0 = Hardware does not support device-IOTLBs. • 1 = Hardware supports Device-IOTLBs. Implementations reporting this field as Set must also support Queued Invalidation (QI).Hardware implementations supporting I/O Page Requests (PRS field Set in Extended Capability register) must report a value of 1b in this field.
1	1h RO	**Queued Invalidation Support (QI):** • 0 = Hardware does not support queued invalidations. • 1 = Hardware supports queued invalidations.
0	0h RO	**Page-Walk Coherency (C):** This field indicates if hardware access to the root, context, extended-context and interrupt-remap tables, and second-level paging structures for requests-without-PASID, are coherent (snooped) or not. • 0 = Indicates hardware accesses to remapping structures are non-coherent. • 1 = Indicates hardware accesses to remapping structures are coherent. Hardware access to advanced fault log, invalidation queue, invalidation semaphore, page-request queue, PASID-table, PASID-state table, and first-level page-tables are always coherent.

6.4 Global Command Register (GCMD_REG_0_0_0_VTDBAR) - Offset 18h

Register to control remapping hardware. If multiple control fields in this register need to be modified, software must serialize the modifications through multiple writes to this register.

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Translation Enable (TE):** Software writes to this field to request hardware to enable/disable DMA-remapping: • 0 = Disable DMA remapping. • 1 = Enable DMA remapping. Hardware reports the status of the translation enable operation through the TES field in the Global Status register. There may be active DMA requests in the platform when software updates this field. Hardware must enable or disable remapping logic only at deterministic transaction boundaries, so that any in-flight transaction is either subject to remapping or not at all. Hardware implementations supporting DMA draining must drain any in-flight DMA read/write requests queued within the Root-Complex before completing the translation enable command and reflecting the status of the command through the TES field in the Global Status register. The value returned on a read of this field is undefined.
30	0h WO	**Set Root Table Pointer (SRTP):** Software sets this field to set/update the root-entry table pointer used by hardware. The root-entry table pointer is specified through the Root-entry Table Address (RTA_REG) register. Hardware reports the status of the Set Root Table Pointer operation through the RTPS field in the Global Status register. The Set Root Table Pointer operation must be performed before enabling or re-enabling (after disabling) DMA remapping through the TE field..After a Set Root Table Pointer operation, software must globally invalidate the context cache and then globally invalidate of IOTLB. This is required to ensure hardware uses only the remapping structures referenced by the new root table pointer, and not stale cached entries. While DMA remapping hardware is active, software may update the root table pointer through this field. However, to ensure valid in-flight DMA requests are deterministically remapped, software must ensure that the structures referenced by the new root table pointer are programmed to provide the same remapping results as the structures referenced by the previous root-table pointer. Clearing this bit has no effect. The value returned on read of this field is undefined.
29	0h RO	**Set Fault Log (SFL):** This field is valid only for implementations supporting advanced fault logging. Software sets this field to request hardware to set/update the fault-log pointer used by hardware. The fault-log pointer is specified through Advanced Fault Log register. Hardware reports the status of the Set Fault Log operation through the FLS field in the Global Status register. The fault log pointer must be set before enabling advanced fault logging (through EAFL field). Once advanced fault logging is enabled, the fault log pointer may be updated through this field while DMA remapping is active. Clearing this bit has no effect. The value returned on read of this field is undefined.

Bit Range	Default & Access	Field Name (ID): Description
28	0h RO	**Enable Advanced Fault Logging (EAFL):** This field is valid only for implementations supporting advanced fault logging. Software writes to this field to request hardware to enable or disable advanced fault logging: • 0 = Disable advanced fault logging. In this case, translation faults are reported through the Fault Recording registers. • 1 = Enable use of memory-resident fault log. When enabled, translation faults are recorded in the memory-resident log. The fault log pointer must be set in hardware (through the SFL field) before enabling advanced fault logging. Hardware reports the status of the advanced fault logging enable operation through the AFLS field in the Global Status register. The value returned on read of this field is undefined.
27	0h RO	**Write Buffer Flush (WBF):** This bit is valid only for implementations requiring write buffer flushing. Software sets this field to request that hardware flush the Root-Complex internal write buffers. This is done to ensure any updates to the memory-resident remapping structures are not held in any internal write posting buffers. Hardware reports the status of the write buffer flushing operation through the WBFS field in the Global Status register. Clearing this bit has no effect. The value returned on a read of this field is undefined.
26	0h RW	**Queued Invalidation Enable (QIE):** This field is valid only for implementations supporting queued invalidations. Software writes to this field to enable or disable queued invalidations. • 0 = Disable queued invalidations. • 1 = Enable use of queued invalidations. Hardware reports the status of queued invalidation enable operation through QIES field in the Global Status register. The value returned on a read of this field is undefined.
25	0h RW	**Interrupt Remapping Enable (IRE):** This field is valid only for implementations supporting interrupt remapping. • 0 = Disable interrupt-remapping hardware. • 1 = Enable interrupt-remapping hardware. Hardware reports the status of the interrupt remapping enable operation through the IRES field in the Global Status register. There may be active interrupt requests in the platform when software updates this field. Hardware must enable or disable interrupt-remapping logic only at deterministic transaction boundaries, so that any in-flight interrupts are either subject to remapping or not at all. Hardware implementations must drain any in-flight interrupts requests queued in the Root-Complex before completing the interrupt-remapping enable command and reflecting the status of the command through the IRES field in the Global Status register. The value returned on a read of this field is undefined.

Bit Range	Default & Access	Field Name (ID): Description
24	0h WO	**Set Interrupt Remap Table Pointer (SIRTP):** This field is valid only for implementations supporting interrupt-remapping. Software sets this field to set/update the interrupt remapping table pointer used by hardware. The interrupt remapping table pointer is specified through the Interrupt Remapping Table Address (IRTA_REG) register. Hardware reports the status of the Set Interrupt Remap Table Pointer operation through the IRTPS field in the Global Status register. The Set Interrupt Remap Table Pointer operation must be performed before enabling or re-enabling (after disabling) interrupt-remapping hardware through the IRE field. After a Set Interrupt Remap Table Pointer operation, software must globally invalidate the interrupt entry cache. This is required to ensure hardware uses only the interrupt-remapping entries referenced by the new interrupt remap table pointer, and not any stale cached entries. While interrupt remapping is active, software may update the interrupt remapping table pointer through this field. However, to ensure valid in-flight interrupt requests are deterministically remapped, software must ensure that the structures referenced by the new interrupt remap table pointer are programmed to provide the same remapping results as the structures referenced by the previous interrupt remap table pointer. Clearing this bit has no effect. The value returned on a read of this field is undefined.
23	0h RW	**Compatibility Format Interrupt (CFI):** This field is valid only for Intel64 implementations supporting interrupt-remapping. Software writes to this field to enable or disable Compatibility Format interrupts on Intel64 platforms. The value in this field is effective only when interrupt-remapping is enabled and Extended Interrupt Mode (x2APIC mode) is not enabled. • 0 = Block Compatibility format interrupts. • 1 = Process Compatibility format interrupts as pass-through (bypass interrupt remapping). Hardware reports the status of updating this field through the CFIS field in the Global Status register. The value returned on a read of this field is undefined.
22:0	0h RO	**Reserved**

6.5 Global Status Register (GSTS_REG_0_0_0_VTDBAR) - Offset 1Ch

Register to report general remapping hardware status.

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Translation Enable Status (TES):** This field indicates the status of DMA-remapping hardware. • 0 = DMA-remapping hardware is not enabled. • 1 = DMA-remapping hardware is enabled
30	0h RO/V	**Root Table Pointer Status (RTPS):** This field indicates the status of the root-table pointer in hardware. This field is cleared by hardware when software sets the SRTP field in the Global Command register. This field is set by hardware when hardware completes the Set Root Table Pointer operation using the value provided in the Root-Entry Table Address register.
29	0h RO	**Fault Log Status (FLS):** This field: • Is cleared by hardware when software Sets the SFL field in the Global Command register. • Is Set by hardware when hardware completes the Set Fault Log Pointer operation using the value provided in the Advanced Fault Log register.
28	0h RO	**Advanced Fault Logging Status (AFLS):** This field is valid only for implementations supporting advanced fault logging. It indicates the advanced fault logging status: • 0 = Advanced Fault Logging is not enabled. • 1 = Advanced Fault Logging is enabled.
27	0h RO	**Write Buffer Flush Status (WBFS):** This field is valid only for implementations requiring write buffer flushing. This field indicates the status of the write buffer flush command. It is: • Set by hardware when software sets the WBF field in the Global Command register. • Cleared by hardware when hardware completes the write buffer flushing operation.
26	0h RO/V	**Queued Invalidation Enable Status (QIES):** This field indicates queued invalidation enable status. • 0 = queued invalidation is not enabled. • 1 = queued invalidation is enabled
25	0h RO/V	**Interrupt Remapping Enable Status (IRES):** This field indicates the status of Interrupt-remapping hardware. • 0 = Interrupt-remapping hardware is not enabled. • 1 = Interrupt-remapping hardware is enabled
24	0h RO/V	**Interrupt Remapping Pointer Status (IRTPS):** This field indicates the status of the interrupt remapping table pointer in hardware. This field is cleared by hardware when software sets the SIRTP field in the Global Command register. This field is Set by hardware when hardware completes the set interrupt remap table pointer operation using the value provided in the Interrupt Remapping Table Address register.
23	0h RO/V	**Compatibility Format Interrupt Status (CFIS):** This field indicates the status of Compatibility format interrupts on Intel64 implementations supporting interrupt-remapping. The value reported in this field is applicable only when interrupt-remapping is enabled and Extended Interrupt Mode (x2APIC mode) is not enabled. • 0 = Compatibility format interrupts are blocked. • 1 = Compatibility format interrupts are processed as pass-through (bypassing interrupt remapping).
22:0	0h RO	**Reserved**

6.6 Root Table Address Register (RTADDR_REG_0_0_0_VTDBAR) - Offset 20h

Register providing the base address of root-entry table.

Type	Size	Offset	Default
MEM	64 bit	VTDPVC0BAR + 20h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:12	0h RW	**Root Table Address (RTA):** This register points to base of page aligned, 4KB-sized root-entry table in system memory. Hardware ignores and not implements bits 63:HAW, where HAW is the host address width. Software specifies the base address of the root-entry table through this register, and programs it in hardware through the SRTP field in the Global Command register. Reads of this register returns value that was last programmed to it.
11	0h RW	**Root Table Type (RTT):** This field specifies the type of root-table referenced by the Root Table Address (RTA) field: • 0 = Root Table. • 1 = Extended Root Table
10:0	0h RO	**Reserved**

6.7 Context Command Register (CCMD_REG_0_0_0_VTDBAR) - Offset 28h

Register to manage context cache. The act of writing the uppermost byte of the CCMD_REG with the ICC field Set causes the hardware to perform the context-cache invalidation.

Type	Size	Offset	Default
MEM	64 bit	VTDPVC0BAR + 28h	0800000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/V	**Invalidate Context Cache (ICC):** Software requests invalidation of context-cache by setting this field. Software must also set the requested invalidation granularity by programming the CIRG field. Software must read back and check the ICC field is Clear to confirm the invalidation is complete. Software must not update this register when this field is set. Hardware clears the ICC field to indicate the invalidation request is complete. Hardware also indicates the granularity at which the invalidation operation was performed through the CAIG field. Software must submit a context-cache invalidation request through this field only when there are no invalidation requests pending at this remapping hardware unit. Since information from the context-cache may be used by hardware to tag IOTLB entries, software must perform domain-selective (or global) invalidation of IOTLB after the context cache invalidation has completed. Hardware implementations reporting write-buffer flushing requirement (RWBF=1 in Capability register) must implicitly perform a write buffer flush before invalidating the context cache.
62:61	0h RW	**Context Invalidation Request Granularity (CIRG):** Software provides the requested invalidation granularity through this field when setting the ICC field: • 00: Reserved. • 01: Global Invalidation request. • 10: Domain-selective invalidation request. The target domain-id must be specified in the DID field. • 11: Device-selective invalidation request. The target source-id(s) must be specified through the SID and FM fields, and the domain-id (that was programmed in the context-entry for these device(s)) must be provided in the DID field. Hardware implementations may process an invalidation request by performing invalidation at a coarser granularity than requested. Hardware indicates completion of the invalidation request by clearing the ICC field. At this time, hardware also indicates the granularity at which the actual invalidation was performed through the CAIG field.
60:59	1h RO/V	**Context Actual Invalidation Granularity (CAIG):** Hardware reports the granularity at which an invalidation request was processed through the CAIG field at the time of reporting invalidation completion (by clearing the ICC field).The following are the encodings for this field: • 00: Reserved. • 01: Global Invalidation performed. This could be in response to a global, domain-selective or device-selective invalidation request. • 10: Domain-selective invalidation performed using the domain-id specified by software in the DID field. This could be in response to a domain-selective or device-selective invalidation request. • 11: Device-selective invalidation performed using the source-id and domain-id specified by software in the SID and FM fields. This can only be in response to a device-selective invalidation request.
58:34	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
33:32	0h RW	**Function Mask (FM):** Software may use the Function Mask to perform device-selective invalidations on behalf of devices supporting PCI Express Phantom Functions...This field specifies which bits of the function number portion (least significant three bits) of the SID field to mask when performing device-selective invalidations. The following encodings are defined for this field: • 00: No bits in the SID field masked. • 01: Mask most significant bit of function number in the SID field. • 10: Mask two most significant bit of function number in the SID field. • 11: Mask all three bits of function number in the SID field. The context-entries corresponding to all the source-ids specified through the FM and SID fields must have to the domain-id specified in the DID field.
31:16	0h RW	**SID:** Indicates the source-id of the device whose corresponding context-entry needs to be selectively invalidated. This field along with the FM field must be programmed by software for device-selective invalidation requests.
15:0	0h RW	**DID:** Indicates the id of the domain whose context-entries need to be selectively invalidated. This field must be programmed by software for both domain-selective and device-selective invalidation requests. The Capability register reports the domain-id width supported by hardware. Software must ensure that the value written to this field is within this limit. Hardware may ignore and not implement bits15:N, where N is the supported domain-id width reported in the Capability register.

6.8 Fault Status Register (FSTS_REG_0_0_0_VTDBAR) - Offset 34h

Register indicating the various error statuses.

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + 34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	0h RO	**Fault Record Index (FRI):** This field is valid only when the PPF field is Set. The FRI field indicates the index (from base) of the fault recording register to which the first pending fault was recorded when the PPF field was Set by hardware. The value read from this field is undefined when the PPF field is clear.
7	0h RW/1C	**Page Request Overflow (PRO):** Hardware detected a Page Request Overflow error. Hardware implementations not supporting the Page Request Queue implement this bit as RsvdZ.
6	0h RO	**Invalidation Time-out Error (ITE):** Hardware detected a Device-IOTLB invalidation completion time-out. At this time, a fault event may be generated based on the programming of the Fault Event Control register. Hardware implementations not supporting device Device-IOTLBs implement this bit as RsvdZ.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RO	**Invalidation Completion Error (ICE):** Hardware received an unexpected or invalid Device-IOTLB invalidation completion. This could be due to either an invalid ITag or invalid source-id in an invalidation completion response. At this time, a fault event may be generated based on the programming of hte Fault Event Control register. Hardware implementations not supporting Device-IOTLBs implement this bit as RsvdZ.
4	0h RW/1C	**Invalidation Queue Error (IQE):** Hardware detected an error associated with the invalidation queue. This could be due to either a hardware error while fetching a descriptor from the invalidation queue, or hardware detecting an erroneous or invalid descriptor in the invalidation queue. At this time, a fault event may be generated based on the programming of the Fault Event Control register. Hardware implementations not supporting queued invalidations implement this bit as RsvdZ.
3	0h RO	**Advanced Pending Fault (APF):** When this field is Clear, hardware sets this field when the first fault record (at index 0) is written to a fault log. At this time, a fault event is generated based on the programming of the Fault Event Control register. Software writing 1 to this field clears it. Hardware implementations not supporting advanced fault logging implement this bit as RsvdZ.
2	0h RO	**Advanced Fault Overflow (AFO):** Hardware sets this field to indicate advanced fault log overflow condition. At this time, a fault event is generated based on the programming of the Fault Event Control register. Software writing 1 to this field clears it. Hardware implementations not supporting advanced fault logging implement this bit as RsvdZ.
1	0h RO/V	**Primary Pending Fault (PPF):** This field indicates if there are one or more pending faults logged in the fault recording registers. Hardware computes this field as the logical OR of Fault (F) fields across all the fault recording registers of this remapping hardware unit. • 0 = No pending faults in any of the fault recording registers. • 1 = One or more fault recording registers has pending faults. The FRI field is updated by hardware whenever the PPF field is set by hardware. Also, depending on the programming of Fault Event Control register, a fault event is generated when hardware sets this field.
0	0h RW/1C	**Primary Fault Overflow (PFO):** Hardware sets this field to indicate overflow of fault recording registers. Software writing 1 clears this field. When this field is Set, hardware does not record any new faults until software clears this field.

6.9 Fault Event Control Register (FECTL_REG_0_0_0_VTDBAR) - Offset 38h

Register specifying the fault event interrupt message control bits.

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + 38h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Interrupt Mask (IM):** • 0 = No masking of interrupt. When an interrupt condition is detected, hardware issues an interrupt message (using the Fault Event Data and Fault Event Address register values). • 1 = This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is set.
30	0h RO/V	**Interrupt Pending (IP):** Hardware sets the IP field whenever it detects an interrupt condition, which is defined as: • When primary fault logging is active, an interrupt condition occurs when hardware records a fault through one of the Fault Recording registers and sets the PPF field in Fault Status register. • When advanced fault logging is active, an interrupt condition occurs when hardware records a fault in the first fault record (at index 0) of the current fault log and sets the APF field in the Fault Status register. • Hardware detected error associated with the Invalidation Queue, setting the IQE field in the Fault Status register. • Hardware detected invalid Device-IOTLB invalidation completion, setting the ICE field in the Fault Status register. • Hardware detected Device-IOTLB invalidation completion time-out, setting the ITE field in the Fault Status register. If any of the status fields in the Fault Status register were already Set at the time of setting any of these fields, it is not treated as a new interrupt condition. The IP field is kept set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set or other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending, or due to software clearing the IM field. • Software servicing all the pending interrupt status fields in the Fault Status register as follows: - When primary fault logging is active, software clearing the Fault (F) field in all the Fault Recording registers with faults, causing the PPF field in Fault Status register to be evaluated as clear. - Software clearing other status fields in the Fault Status register by writing back the value read from the respective fields.
29:0	0h RO	**Reserved**

6.10 Fault Event Data Register (FEDATA_REG_0_0_0_VTDBAR) - Offset 3Ch

Register specifying the interrupt message data

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Extended Interrupt Message Data (EIMD):** This field is valid only for implementations supporting 32-bit interrupt data fields. Hardware implementations supporting only 16-bit interrupt data may treat this field as RsvdZ.
15:0	0h RW	**Interrupt Message Data (IMD):** Data value in the interrupt request.

6.11 Fault Event Address Register (FEADDR_REG_0_0_0_VTDBAR) - Offset 40h

Register specifying the interrupt message address.

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + 40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Message Address (MA):** When fault events are enabled, the contents of this register specify the DWORD-aligned address (bits 31:2) for the interrupt request.
1:0	0h RO	**Reserved**

6.12 Fault Event Upper Address Register (FEUADDR_REG_0_0_0_VTDBAR) - Offset 44h

Register specifying the interrupt message upper address.

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + 44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Message Upper Address (MUA):** Hardware implementations supporting Extended Interrupt Mode are required to implement this register.Hardware implementations not supporting Extended Interrupt Mode may treat this field as RsvdZ.

6.13 Advanced Fault Log Register (AFLOG_REG_0_0_0_VTDBAR) - Offset 58h

Register to specify the base address of the memory-resident fault-log region. This register is treated as RsvdZ for implementations not supporting advanced translation fault logging (AFL field reported as 0 in the Capability register).

Type	Size	Offset	Default
MEM	64 bit	VTDPVC0BAR + 58h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:12	0h RO	**Fault Log Address (FLA):** This field specifies the base of 4KB aligned fault-log region in system memory. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width. Software specifies the base address and size of the fault log region through this register, and programs it in hardware through the SFL field in the Global Command register. When implemented, reads of this field return the value that was last programmed to it.
11:9	0h RO	**Fault Log Size (FLS):** This field specifies the size of the fault log region pointed by the FLA field. The size of the fault log region is 2X * 4KB, where X is the value programmed in this register. When implemented, reads of this field return the value that was last programmed to it.
8:0	0h RO	**Reserved**

6.14 Protected Memory Enable Register (PMEN_REG_0_0_0_VTDBAR) - Offset 64h

Register to enable the DMA-protected memory regions setup through the PLMBASE,..., PLMLIMT, PHMBASE, PHMLIMIT registers. This register is always treated as RO for implementations not supporting protected memory regions (PLMR and PHMR fields reported as Clear in the Capability register).Protected memory regions may be used by software to securely initialize remapping structures in memory. To avoid impact to legacy BIOS usage of memory, software is recommended to not overlap protected memory regions with any reserved memory regions of the platform reported through the Reserved Memory Region Reporting (RMRR) structures.

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Protected Memory (EPM):** This field controls DMA accesses to the protected low-memory and protected high-memory regions. • 0 = Protected memory regions are disabled. • 1 = Protected memory regions are enabled. DMA requests accessing protected memory regions are handled as follows: - When DMA remapping is not enabled, all DMA requests accessing protected memory regions are blocked. - When DMA remapping is enabled: • DMA requests processed as pass-through (Translation Type value of 10b in Context-Entry) and accessing the protected memory regions are blocked. • DMA requests with translated address (AT=10b) and accessing the protected memory regions are blocked. • DMA requests that are subject to address remapping, and accessing the protected memory regions may or may not be blocked by hardware. For such requests, software must not depend on hardware protection of the protected memory regions, and instead program the DMA-remapping page-tables to not allow DMA to protected memory regions. Remapping hardware access to the remapping structures are not subject to protected memory region checks. DMA requests blocked due to protected memory region violation are not recorded or reported as remapping faults. Hardware reports the status of the protected memory enable/disable operation through the PRS field in this register.Hardware implementations supporting DMA draining must drain any in-flight translated DMA requests queued within the Root-Complex before indicating the protected memory region as enabled through the PRS field.
30:1	0h RO	**Reserved**
0	0h RO/V	**Protected Region Status (PRS):** This field indicates the status of protected memory region(s): • 0 = Protected memory region(s) disabled. • 1 = Protected memory region(s) enabled.

6.15 Protected Low Memory Base Register (PLMBASE_REG_0_0_0_VTDBAR) - Offset 68h

Register to set up the base address of DMA-protected low-memory region below 4GB. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled. This register is always treated as RO for implementations not supporting protected low memory region (PLMR field reported as Clear in the Capability register).The alignment of the protected low memory region base depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding the most significant zero bit position with 0 in the value read back from the register. Bits N:0 of this register is decoded by hardware as all 0s...Software must setup the protected low memory region below 4GB. Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Protected Low-Memory Base (PLMB):** This register specifies the base of protected low-memory region in system memory.
19:0	0h RO	**Reserved**

6.16 Protected Low-Memory Limit Register (PLMLIMIT_REG_0_0_0_VTDBAR) - Offset 6Ch

Register to set up the limit address of DMA-protected low-memory region below 4GB. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled. This register is always treated as RO for implementations not supporting protected low memory region (PLMR field reported as Clear in the Capability register). The alignment of the protected low memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding most significant zero bit position with 0 in the value read back from the register. Bits N:0 of the limit register is decoded by hardware as all 1s. The Protected low-memory base and limit registers functions as follows:

- Programming the protected low-memory base and limit registers with the same value in bits 31: (N+1) specifies a protected low-memory region of size 2(N+1) bytes
- Programming the protected low-memory limit register with a value less than the protected low-memory base register disables the protected low-memory region

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + 6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Protected Low-Memory Limit (PLML):** This register specifies the last host physical address of the DMA-protected low-memory region in system memory.
19:0	0h RO	**Reserved**

6.17 Protected High-Memory Base Register (PHMBASE_REG_0_0_0_VTDBAR) - Offset 70h

Register to set up the base address of DMA-protected high-memory region. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled. This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as Clear in the Capability register). The alignment of the protected high memory region base depends on the number of reserved bits (N:0) of

this register. Software may determine N by writing all 1s to this register, and finding most significant zero bit position below host address width (HAW) in the value read back from the register. Bits N:0 of this register are decoded by hardware as all 0s. Software may setup the protected high memory region either above or below 4GB. Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MEM	64 bit	VTDPVC0BAR + 70h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:20	0h RW	**Protected High-Memory Base (PHMB):** This register specifies the base of protected (high) memory region in system memory Hardware ignores, and does not implement, bits 63:HAW, where HAW is the host address width.
19:0	0h RO	**Reserved**

6.18 Protected High-Memory Limit Register (PHMLIMIT_REG_0_0_0_VTDBAR) - Offset 78h

Register to set up the limit address of DMA-protected high-memory region. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled. This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as Clear in the Capability register). The alignment of the protected high memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine the value of N by writing all 1s to this register, and finding most significant zero bit position below host address width (HAW) in the value read back from the register. Bits N:0 of the limit register is decoded by hardware as all 1sThe protected high-memory base & limit registers functions as follows.

- Programming the protected low-memory base and limit registers with the same value in bits HAW:(N+1) specifies a protected low-memory region of size 2(N+1) bytes
- Programming the protected high-memory limit register with a value less than the protected high-memory base register disables the protected high-memory region

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MEM	64 bit	VTDPVC0BAR + 78h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:20	0h RW	**Protected High-Memory Limit (PHML):** This register specifies the last host physical address of the DMA-protected high-memory region in system memory Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width.
19:0	0h RO	**Reserved**

6.19 Invalidation Queue Head Register (IQH_REG_0_0_0_VTDBAR) - Offset 80h

Register indicating the invalidation queue head. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	64 bit	VTDPVC0BAR + 80h	00000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0h RO/V	**Queue Head (QH):** Specifies the offset (128-bit aligned) to the invalidation queue for the command that will be fetched next by hardware. Hardware resets this field to 0 whenever the queued invalidation is disabled (QIES field Clear in the Global Status register).
3:0	0h RO	**Reserved**

6.20 Invalidation Queue Tail Register (IQT_REG_0_0_0_VTDBAR) - Offset 88h

Register indicating the invalidation tail head. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	64 bit	VTDPVC0BAR + 88h	00000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0h RW	**Queue Tail (QT):** Specifies the offset (128-bit aligned) to the invalidation queue for the command that will be written next by software.
3:0	0h RO	**Reserved**

6.21 Invalidation Queue Address Register (IQA_REG_0_0_0_VTDBAR) - Offset 90h

Register to configure the base address and size of the invalidation queue. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	64 bit	VTDPVC0BAR + 90h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RW	**Invalidation Queue Base Address (IQA):** This field points to the base of 4KB aligned invalidation request queue. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width. Reads of this field return the value that was last programmed to it.
11:3	0h RO	**Reserved**
2:0	0h RW	**Queue Size (QS):** This field specifies the size of the invalidation request queue. A value of X in this field indicates an invalidation request queue of (2X) 4KB pages. The number of entries in the invalidation queue is 2(X + 8).

6.22 Invalidation Completion Status Register (ICS_REG_0_0_0_VTDBAR) - Offset 9Ch

Register to report completion status of invalidation wait descriptor with Interrupt Flag (IF) Set. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/1C	**Invalidation Wait Descriptor Complete (IWC):** Indicates completion of Invalidation Wait Descriptor with Interrupt Flag (IF) field Set. Hardware implementations not supporting queued invalidations implement this field as RsvdZ.

6.23 Invalidation Event Control Register (IECTL_REG_0_0_0_VTDBAR) - Offset A0h

Register specifying the invalidation event interrupt control bits. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + A0h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Interrupt Mask (IM):** • 0= No masking of interrupt. When an invalidation event condition is detected, hardware issues an interrupt message (using the Invalidation Event Data & Invalidation Event Address register values) • 1= This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is Set.
30	0h RO/V	**Interrupt Pending (IP):** Hardware sets the IP field whenever it detects an interrupt condition. Interrupt condition is defined as: • An Invalidation Wait Descriptor with Interrupt Flag (IF) field Set completed, setting the IWC field in the Invalidation Completion Status register • If the IWC field in the Invalidation Completion Status register was already Set at the time of setting this field, it is not treated as a new interrupt condition The IP field is kept Set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set, or due to other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • 0= Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending or due to software clearing the IM field • 1= Software servicing the IWC field in the Invalidation Completion Status register.
29:0	0h RO	**Reserved**

6.24 Invalidation Event Data Register (IEDATA_REG_0_0_0_VTDBAR) - Offset A4h

Register specifying the Invalidation Event interrupt message data. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Extended Interrupt Message Data (EIMD):** This field is valid only for implementations supporting 32-bit interrupt data fields. Hardware implementations supporting only 16-bit interrupt data treat this field as Rsvd.
15:0	0h RW	**Interrupt Message Data (IMD):** Data value in the interrupt request.

6.25 Invalidation Event Address Register (IEADDR_REG_0_0_0_VTDBAR) - Offset A8h

Register specifying the Invalidation Event Interrupt message address. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Message Address (MA):** When fault events are enabled, the contents of this register specify the DWORD-aligned address (bits 31:2) for the interrupt request.
1:0	0h RO	**Reserved**

6.26 Invalidation Event Upper Address Register (IEUADDR_REG_0_0_0_VTDBAR) - Offset ACh

Register specifying the Invalidation Event interrupt message upper address.

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Message Upper Address (MUA):** Hardware implementations supporting Queued Invalidations and Extended Interrupt Mode are required to implement this register. Hardware implementations not supporting Queued Invalidations or Extended Interrupt Mode may treat this field as RsvdZ.

6.27 Interrupt Remapping Table Address Register (IRTA_REG_0_0_0_VTDBAR) - Offset B8h

Register providing the base address of Interrupt remapping table. This register is treated as RsvdZ by implementations reporting Interrupt Remapping (IR) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	64 bit	VTDPVC0BAR + B8h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:12	0h RW	**Interrupt Remapping Table Address (IRTA):** This field points to the base of 4KB aligned interrupt remapping table. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width. Reads of this field returns value that was last programmed to it.
11	0h RW	**Extended Interrupt Mode Enable (EIME):** This field is used by hardware on Intel64 platforms as follows: • 0=xAPIC mode is active. Hardware interprets only low 8-bits of Destination-ID field in the IRTEs. The high 24-bits of the Destination-ID field are treated as reserved • 1= x2APIC mode is active. Hardware interprets all 32-bits of Destination-ID field in the IRTEs This field is implemented as RsvdZ on implementations reporting Extended Interrupt Mode (EIM) field as Clear in Extended Capability register.
10:4	0h RO	**Reserved**
3:0	0h RW	**S:** This field specifies the size of the interrupt remapping table. The number of entries in the interrupt remapping table is 2(X+1), where X is the value programmed in this field.

6.28 Page Request Status Register (PRESTS_REG_0_0_0_VTDBAR) - Offset DCh

Register to report pending page request in page request queue. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO	**Pending Page Request (PPR):** Pending Page Request: Indicates pending page requests to be serviced by software in the page request queue. This field is Set by hardware when a streaming page request entry (page_stream_reg_dsc) or a page group request (page_grp_req_dsc) with Last Page in Group (LPG) field Set, is added to the page request queue.

6.29 Page Request Event Control Register (PRECTL_REG_0_0_0_VTDBAR) - Offset E0h

Register specifying the page request event interrupt control bits. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + E0h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RO	**Interrupt Mask (IM):** Interrupt Mask • 0=No masking of interrupt. When a page request event condition is detected, hardware issues an interrupt message (using the Page Request Event Data and Page Request Event Address register values) • 1=This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is Set.
30	0h RO	**Interrupt Pending (IP):** Interrupt Pending: Hardware sets the IP field whenever it detects an interrupt condition. Interrupt condition is defined as: • A streaming page request entry (page_stream_req_dsc) or a page group request (page_grp_req_dsc) with Last Page in Group (LPG) field Set, was added to page request queue, resulting in hardware setting the Pending Page Request (PPR) field in Page Request Status register • If the PPR field in the Page Request Event Status register was already Set at the time of setting this field, it is not treated as a new interrupt condition The IP field is kept Set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set, or due to other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending or due to software clearing the IM field • Software servicing the PPR field in the Page Request Event Status register.
29:0	0h RO	**Reserved**

6.30 Page Request Event Data Register (PREDATA_REG_0_0_0_VTDBAR) - Offset E4h

Register specifying the Page Request Event interrupt message data. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Extended Interrupt Message Data (EIMD):** Extended Interrupt Message Data
15:0	0h RO	**Interrupt Message Data (IMD):** Interrupt Message Data: Data value in the interrupt request. Software requirements for programming this register are described in VTd Spec

6.31 Page Request Event Address Register (PREADDR_REG_0_0_0_VTDBAR) - Offset E8h

Register specifying the Page Request Event Interrupt message address. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RO	**Message Address (MA):** Message Address: When fault events are enabled, the contents of this register specify the DWORD-aligned address (bits 31:2) for the interrupt request.
1:0	0h RO	**Reserved**

6.32 Page Request Event Upper Address Register (PREUADDR_REG_0_0_0_VTDBAR) - Offset ECh

Register specifying the Page Request Event interrupt message upper address.

Type	Size	Offset	Default
MEM	32 bit	VTDPVC0BAR + ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Message Upper Address (MUA):** Message Upper Address: This field specifies the upper address (bits.. 63:32) for the page request event interrupt.

6.33 Fault Recording Register Low [0] (FRCDL_REG_0_0_0_VTDBAR) - Offset 400h

Register to record fault information when primary fault logging is active. Hardware reports the number and location of fault recording registers through the Capability register. This register is relevant only for primary fault logging. This register is sticky and can be cleared only through power good reset or by software clearing the RW1C fields by writing a 1.

Type	Size	Offset	Default
MEM	64 bit	VTDPVC0BAR + 400h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:12	0h RO/V	**Fault Info (FI):** When the Fault Reason (FR) field indicates one of the DMA-remapping fault conditions, bits 63:12 of this field contain the page address in the faulted DMA request. Hardware treats bits 63:N as reserved (0), where N is the maximum guest address width (MGAW) supported. When the Fault Reason (FR) field indicates one of the interrupt-remapping fault conditions, bits 63:48 of this field indicate the interrupt_index computed for the faulted interrupt request, and bits 47:12 are cleared. This field is relevant only when the F field is Set.
11:0	0h RO	**Reserved**

6.34 Fault Recording Register High [0] (FRCDH_REG_0_0_0_VTDBAR) - Offset 408h

Register to record fault information when primary fault logging is active. Hardware reports the number and location of fault recording registers through the Capability register. This register is relevant only for primary fault logging. This register is sticky and can be cleared only through power good reset or by software clearing the RW1C fields by writing a 1.

Type	Size	Offset	Default
MEM	64 bit	VTDPVC0BAR + 408h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/1C	**F:** Hardware sets this field to indicate a fault is logged in this Fault Recording register. The F field is set by hardware after the details of the fault is recorded in other fields. When this field is Set, hardware may collapse additional faults from the same source-id (SID)
62	0h RO/V	**T:** Type of the faulted request: • 0=0: Write request • 1=1: Read request or Atom icOp request This field is relevant only when the F field is Set, and when the fault reason (FR) indicates one of the DMA-remapping fault conditions.
61:60	0h RO/V	**Address Type (AT):** This field captures the AT field from the faulted DMA request. Hardware implementations not supporting Device-IOTLBs (DI field Clear in Extended Capability register) treat this field as RsvdZ. When supported, this field is valid only when the F field is Set, and when the fault reason (FR) indicates one of the DMA-remapping fault conditions.
59:40	0h RO/V	**PASID Value (PN):** PASID value in the faulted request. This field is relevant only when the PP field is set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
39:32	0h RO/V	**Fault Reason (FR):** Reason for the fault This field is relevant only when the F field is set.
31	0h RO/V	**PASID Present (PP):** When set, indicates the faulted request has a PASID tag. The value of the PASID field is reported in the PASID Value (PV) field. This field is relevant only when the F field is Set, and when the fault reason (FR) indicates one of the non-recoverable address translation fault conditions. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
30	0h RO/V	**Execute Permission Requested (EXE):** When set, indicates Execute permission was requested by the faulted read request. This field is relevant only when the PP field and T field are both Set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
29	0h RO/V	**Privilege Mode Requested (PRIV):** When set, indicates Supervisor privilege was requested by the faulted request. This field is relevant only when the PP field is Set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
28:16	0h RO	**Reserved**
15:0	0h RO/V	**Source Identifier (SID):** Requester-id associated with the fault condition This field is relevant only when the F field is set.

6.35 Invalidate Address Register (IVA_REG_0_0_0_VTDBAR) - Offset 500h

Register to provide the DMA address whose corresponding IOTLB entry needs to be invalidated through the corresponding IOTLB Invalidate register. This register is a write-only register.

Type	Size	Offset	Default
MEM	64 bit	VTDPVC0BAR + 500h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:12	0h RW	**ADDR:** Software provides the DMA address that needs to be page-selectively invalidated. To make a page-selective invalidation request to hardware, software must first write the appropriate fields in this register, and then issue the appropriate page-selective invalidate command through the IOTLB_REG. Hardware ignores bits 63:N, where N is the maximum guest address width (MGAW) supported.A value returned on a read of this field is undefined. A value returned on a read of this field is undefined.
11:7	0h RO	**Reserved**
6	0h RW	**Invalidation Hint (IH):** The field provides hint to hardware about preserving or flushing the non-leaf (page-directory) entries that may be cached in hardware: • 0 = Software may have modified both leaf and non-leaf page-table entries corresponding to mappings specified in the ADDR and AM fields. On a page-selective invalidation request, hardware must flush both the cached leaf and non-leaf page-table entries corresponding to the mappings specified by ADDR and AM fields. • 1 = Software has not modified any non-leaf page-table entries corresponding to mappings specified in the ADDR and AM fields. On a page-selective invalidation request, hardware may preserve the cached non-leaf page-table entries corresponding to mappings specified by ADDR and AM fields. A value returned on a read of this field is undefined.
5:0	0h RW	**Address Mask (AM):** The value in this field specifies the number of low order bits of the ADDR field that must be masked for the invalidation operation. This field enables software to request invalidation of contiguous mappings for size-aligned regions. For example:..Mask ADDR bits Pages..Value masked invalidated.. 0 None 1.. 1 12 2.. 2 13:12 4.. 3 14:12 8.. 4 15:12 16 When invalidating mappings for super-pages, software must specify the appropriate mask value. For example, when invalidating mapping for a 2MB page, software must specify an address mask value of at least 9...Hardware implementations report the maximum supported mask value through the Capability register.

6.36 IOTLB Invalidate Register (IOTLB_REG_0_0_0_VTDBAR) - Offset 508h

Register to invalidate IOTLB. The act of writing the upper byte of the IOTLB_REG with IVT field Set causes the hardware to perform the IOTLB invalidation.

Type	Size	Offset	Default
MEM	64 bit	VTDPVC0BAR + 508h	0200000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/V	**Invalidate IOTLB (IVT):** Software requests IOTLB invalidation by setting this field. Software must also set the requested invalidation granularity by programming the IIRG field. Hardware clears the IVT field to indicate the invalidation request is complete. Hardware also indicates the granularity at which the invalidation operation was performed through the IAIG field. Software must not submit another invalidation request through this register while the IVT field is Set, nor update the associated Invalidate Address register. Software must not submit IOTLB invalidation requests when there is a context-cache invalidation request pending at this remapping hardware unit. Hardware implementations reporting write-buffer flushing requirement (RWBF=1 in Capability register) must implicitly perform a write buffer flushing before invalidating the IOTLB.
62	0h RO	**Reserved**
61:60	0h RW	**IOTLB Invalidation Request Granularity (IIRG):** When requesting hardware to invalidate the IOTLB (by setting the IVT field), software writes the requested invalidation granularity through this field. The following are the encodings for the field • 00 = Reserved • 01 = Global invalidation request • 10 = Domain-selective invalidation request. The target domain-id must be specified in the DID field • 11 = Page-selective invalidation request. The target address, mask and invalidation hint must be specified in the Invalidate Address register, and the domain-id must be provided in the DID field Hardware implementations may process an invalidation request by performing invalidation at a coarser granularity than requested. Hardware indicates completion of the invalidation request by clearing the IVT field. At this time, the granularity at which actual invalidation was performed is reported through the IAIG field
59	0h RO	**Reserved**
58:57	1h RO/V	**IOTLB Actual Invalidation Granularity (IAIG):** Hardware reports the granularity at which an invalidation request was processed through this field when reporting invalidation completion (by clearing the IVT field). The following are the encodings for this field • 00 = Reserved. This indicates hardware detected an incorrect invalidation request and ignored the request. Examples of incorrect invalidation requests include detecting an unsupported address mask value in Invalidate Address register for page-selective invalidation requests • 01 = Global Invalidation performed. This could be in response to a global, domain-selective, or page-selective invalidation request • 10 = Domain-selective invalidation performed using the domain-id specified by software in the DID field. This could be in response to a domain-selective or a page-selective invalidation request • 11 = Domain-page-selective invalidation performed using the address, mask and hint specified by software in the Invalidate Address register and domain-id specified in DID field. This can be in response to a page-selective invalidation request.
56:50	0h RO	**Reserved**
49	0h RW	**Drain Reads (DR):** This field is ignored by hardware if the DRD field is reported as clear in the Capability register. When the DRD field is reported as Set in the Capability register, the following encodings are supported for this field: • 0 = Hardware may complete the IOTLB invalidation without draining any translated DMA read requests • 1 = Hardware must drain DMA read requests.

Bit Range	Default & Access	Field Name (ID): Description
48	0h RW	**Drain Writes (DW):** This field is ignored by hardware if the DWD field is reported as Clear in the Capability register. When the DWD field is reported as Set in the Capability register, the following encodings are supported for this field: • 0 = Hardware may complete the IOTLB invalidation without draining DMA write requests • 1 = Hardware must drain relevant translated DMA write requests.
47:32	0h RW	**DID:** Indicates the ID of the domain whose IOTLB entries need to be selectively invalidated. This field must be programmed by software for domain-selective and page-selective invalidation requests. The Capability register reports the domain-id width supported by hardware. Software must ensure that the value written to this field is within this limit. Hardware ignores and not implements bits 47:(32+N), where N is the supported domain-id width reported in the Capability register.
31:0	0h RO	**Reserved**

7 Processor Graphics Registers (D2:F0)

This chapter documents the registers in Bus: 0, Device 2, Function 0.

Table 7-1. Summary of Bus: 0 Device: 2 Function: 0 Registers (Sheet 1 of 3)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	VID2_0_2_0_PCI	8086h
2h	2	DID2_0_2_0_PCI	0A80h
4h	2	PCICMD_0_2_0_PCI	0000h
6h	2	PCISTS2_0_2_0_PCI	0010h
8h	4	RID2_CC_0_2_0_PCI	03000000h
Ch	1	CLS_0_2_0_PCI	00h
Dh	1	MLT2_0_2_0_PCI	00h
Eh	1	HDR2_0_2_0_PCI	00h
Fh	1	BIST_0_2_0_PCI	00h
10h	4	GTTMMADR0_0_2_0_PCI	00000004h
14h	4	GTTMMADR1_0_2_0_PCI	00000000h
18h	4	GMADR0_0_2_0_PCI	0000000Ch
1Ch	4	GMADR1_0_2_0_PCI	00000000h
20h	4	IOBAR_0_2_0_PCI	00000001h
2Ch	2	SVID2_0_2_0_PCI	0000h
2Eh	2	SID2_0_2_0_PCI	0000h
30h	4	ROMADR_0_2_0_PCI	00000000h
34h	1	CAPPOINT_0_2_0_PCI	40h
3Ch	1	INTRLINE_0_2_0_PCI	00h
3Dh	1	INTRPIN_0_2_0_PCI	01h
3Eh	1	MINGNT_0_2_0_PCI	00h
3Fh	1	MAXLAT_0_2_0_PCI	00h
40h	2	CAPID0_0_2_0_PCI	7009h
42h	2	CAPCTRL0_0_2_0_PCI	010Ch
44h	4	CAPID0_A_0_2_0_PCI	00000000h
48h	4	CAPID0_B_0_2_0_PCI	00000000h
50h	2	MGGC0_0_2_0_PCI	0500h
54h	2	DEVEN_0_2_0_PCI	00BFh
58h	1	DEV2CTL_0_2_0_PCI	00h
60h	4	MSAC_0_2_0_PCI	00010000h

Table 7-1. Summary of Bus: 0 Device: 2 Function: 0 Registers (Sheet 2 of 3)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
68h	4	PUSHAP_0_2_0_PCI	00000000h
6Ch	1	VTD_STATUS_0_2_0_PCI	00h
70h	2	PCIECAPHDR_0_2_0_PCI	AC10h
72h	2	PCIECAP_0_2_0_PCI	0092h
74h	4	DEVICECAP_0_2_0_PCI	10008000h
78h	2	DEVICECTL_0_2_0_PCI	0000h
7Ah	2	DEVICESTS_0_2_0_PCI	0000h
ACh	2	MSI_CAPID_0_2_0_PCI	D005h
AEh	2	MC_0_2_0_PCI	0100h
B0h	4	MA_0_2_0_PCI	00000000h
B4h	2	MD_0_2_0_PCI	0000h
B8h	4	MSI_MASK_0_2_0_PCI	00000000h
BCh	4	MSI_PEND_0_2_0_PCI	00000000h
C0h	4	BDSM0_0_2_0_PCI	00000000h
C4h	4	BDSM1_0_2_0_PCI	00000000h
C8h	4	GFXVTDBAR_LSB_0_2_0_PCI	00000000h
CCh	4	GFXVTDBAR_MSB_0_2_0_PCI	00000000h
D0h	2	PMCAPID_0_2_0_PCI	0001h
D2h	2	PMCAP_0_2_0_PCI	0022h
D4h	2	PMCS_0_2_0_PCI	0000h
E0h	2	SWSMI_0_2_0_PCI	0000h
E4h	4	GSE_0_2_0_PCI	00000000h
E8h	2	SWSCI_0_2_0_PCI	0000h
F0h	4	PAVPC0_0_2_0_PCI	00000000h
F4h	4	PAVPC1_0_2_0_PCI	00000000h
F8h	4	SRID_0_2_0_PCI	00000000h
FCh	4	ASLS_0_2_0_PCI	00000000h
100h	4	PASID_EXTCAP_0_2_0_PCI	2001001Bh
104h	2	PASID_CAP_0_2_0_PCI	1400h
106h	2	PASID_CTRL_0_2_0_PCI	0000h
200h	4	ATS_EXTCAP_0_2_0_PCI	3001000Fh
204h	2	ATS_CAP_0_2_0_PCI	0060h
206h	2	ATS_CTRL_0_2_0_PCI	0000h
300h	4	PR_EXTCAP_0_2_0_PCI	00010013h
304h	2	PR_CTRL_0_2_0_PCI	0000h
306h	2	PR_STATUS_0_2_0_PCI	8100h
308h	4	OPRC_0_2_0_PCI	00008000h
30Ch	4	OPRA_0_2_0_PCI	00000000h

Table 7-1. Summary of Bus: 0 Device: 2 Function: 0 Registers (Sheet 3 of 3)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
320h	4	SRIOV_ECAPHDR_0_2_0_PCI	00010010h
324h	4	SRIOV_CAP_0_2_0_PCI	00000000h
328h	2	SRIOV_CTRL_0_2_0_PCI	0000h
32Ah	2	SRIOV_STS_0_2_0_PCI	0000h
32Ch	2	SRIOV_INITVFS_0_2_0_PCI	0007h
32Eh	2	SRIOV_TOTVFS_0_2_0_PCI	0007h
330h	4	SRIOV_NUMOFVFS_0_2_0_PCI	00000000h
334h	2	FIRST_VF_OFFSET_0_2_0_PCI	0001h
336h	2	VF_STRIDE_0_2_0_PCI	0001h
33Ah	2	VF_DEVICEID_0_2_0_PCI	0A80h
33Ch	4	SUPPORTED_PAGE_SIZES_0_2_0_PCI	00000513h
340h	4	SYSTEM_PAGE_SIZES_0_2_0_PCI	00000001h
344h	4	VF_BAR0_LDW_0_2_0_PCI	00000004h
348h	4	VF_BAR0_UDW_0_2_0_PCI	00000000h
34Ch	4	VF_BAR1_LDW_0_2_0_PCI	0000000Ch
350h	4	VF_BAR1_UDW_0_2_0_PCI	00000000h
354h	4	VF_BAR2_LDW_0_2_0_PCI	00000000h
358h	4	VF_BAR2_UDW_0_2_0_PCI	00000000h
35Ch	4	VF_MIGST_OFFSET_0_2_0_PCI	00000000h

7.1 VID2_0_2_0_PCI - Offset 0h

This register combined with the Device Identification register uniquely identifies any PCI device.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 0h	8086h

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**VID:** PCI standard identification for Intel.

7.2 DID2_0_2_0_PCI - Offset 2h

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 2h	0A80h

Bit Range	Default & Access	Field Name (ID): Description
15:7	15h RW	**DID_MSB:** This is the upper part of a 16 bit value assigned to the device.
6:0	0h RO/V	**DID_SKU:** This is the lower part of a 16 bit value assigned to the device. Fuses will populate this register. Reference EDS Volume 1, Chapter 31 for product DID values.

7.3 PCICMD_0_2_0_PCI - Offset 4h

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**Reserved**
10	0h RW/V	**INTDIS:** This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to DMI.
9	0h RO	**FB2B:** Not Implemented. Hardwired to 0.
8	0h RO	**SEN:** Not Implemented. Hardwired to 0.
7	0h RO	**WCC:** Not Implemented. Hardwired to 0.
6	0h RO	**PER:** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	0h RO	**VPS:** This bit is hardwired to 0 to disable snooping.
4	0h RO	**MWIE:** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	0h RO	**SCE:** This bit is hardwired to 0. The IGD ignores Special cycles.

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW/V	**BME:** 0: Disable IGD bus mastering. 1: Enable the IGD to function as a PCI compliant master.
1	0h RW/V	**MAE:** This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.
0	0h RW/V/L	**IOAE:** This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable. This field is RO 1'b0 if DEV2CTL[0] IOBARDIS at offset 0x58 is 1b. **Locked by:** DEV2CTL_0_2_0_PCI.IOBARDIS

7.4 PCISTS2_0_2_0_PCI - Offset 6h

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 6h	0010h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**DPE:** Since the IGD does not detect parity, this bit is always hardwired to 0.
14	0h RO	**SSE:** The IGD never asserts SERR#, therefore this bit is hardwired to 0.
13	0h RO	**RMAS:** The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
12	0h RO	**RTAS:** The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	0h RO	**STAS:** Hardwired to 0. The IGD does not use target abort semantics.
10:9	0h RO	**DEVT:** Hardwired to 00.
8	0h RO	**DPD:** Since Parity Error Response is hardwired to disabled, and the IGD does not do any parity detection, this bit is hardwired to 0.
7	0h RO	**FB2B:** Hardwired to 0 to be compliant to PCI Express Base Spec (rev 3.0).
6	0h RO	**UDF:** Hardwired to 0.
5	0h RO	**C66:** Hardwired to 0.

Bit Range	Default & Access	Field Name (ID): Description
4	1h RO	**CLIST:** This bit is hardwired to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3	0h RO/V	**INTSTS:** This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted.
2:0	0h RO	**Reserved**

7.5 RID2_CC_0_2_0_PCI - Offset 8h

This register contains the revision number for Device #2 Functions 0 and contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 8h	03000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	3h RO/V	**BCC:** This is an 8-bit value that indicates the base class code. When MGGC0[VAMEN] is 0 this code has the value 03h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this code has the value 03h, indicating a Display Controller Device.
23:16	0h RO/V	**SUBCC:** When MGGC0[VAMEN] is 0, this value is 00h.When MGGC0[VAMEN] is 1, this value is 80h, indicating other display device.
15:8	0h RO	**PI:** When MGGC0[VAMEN] is 0 this value is 00h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this value is 00h, indicating a NOP.
7:4	0h RW	**RID_MSB:** Four MSB of RID
3:0	0h RW	**RID:** Four LSB of RID

7.6 CLS_0_2_0_PCI - Offset Ch

The register 'Cache_Line_Size'.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:2, F:0] + Ch	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**CLS:** This field is implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no effect on any PCI Express device behavior.

7.7 MLT2_0_2_0_PCI - Offset Dh

The IGD does not support the programmability of the initiator latency timer because it does not perform bursts.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:2, F:0] + Dh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**MLTCV:** Hardwired to 0s.

7.8 HDR2_0_2_0_PCI - Offset Eh

This register contains the Header Type of the IGD.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:2, F:0] + Eh	00h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**MFUNC:** Indicates if the device is a Multi-Function Device. The Value of this register is hardwired to 0, internal graphics is a single function.
6:0	0h RO	**H:** This is a 7-bit value that indicates the Header Code for the IGD. This code is hardwired to the value 00h, indicating a type 0 configuration space format.

7.9 BIST_0_2_0_PCI - Offset Fh

This register is used for control and status of Built In Self Test (BIST).

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:2, F:0] + Fh	00h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**BISTS:** BIST is not supported. This bit is hardwired to 0.
6:0	0h RO	**Reserved**

7.10 GTTMMADR0_0_2_0_PCI - Offset 10h

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 16 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO, 6MB reserved, and 8MB used by GTT. GTTADR will begin at (GTTMMADR + 8 MB) while the MMIO base address will be the same as GTTMMADR. The region between (GTTMMADR + 2MB) - (GTTMMADR + 8MB) is reserved. For the Global GTT, this range is defined as a memory BAR in graphics device configuration space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area. The device snoops writes to this region in order to invalidate any cached translations within the various TLB's implemented on-chip. The allocation is for 16MB and the base address is defined by bits [38:24].

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 10h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V	**MBA_0:** Set by the OS, these bits correspond to address signals [63:24].
23:4	0h RO	**ADM:** Hardwired to 0s to indicate at least 16MB address range.
3	0h RO	**PREFMEM:** Hardwired to 0 to prevent prefetching.
2:1	2h RO	**MEMTYP:** Hardwired to 2h to indicate 64 bit base address.
0	0h RO	**MIOS:** Hardwired to 0 to indicate memory space.

7.11 GTTMMADR1_0_2_0_PCI - Offset 14h

This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 16 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO, 6MB reserved, and 8MB used by GTT. GTTADR will begin at (GTTMMADR + 8 MB) while the MMIO base address will be the same as GTTMMADR. The region between (GTTMMADR + 2MB) - (GTTMMADR + 8MB) is reserved. For the Global GTT, this range is defined as a memory BAR in graphics device configuration space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT

memory area. The device snoops writes to this region in order to invalidate any cached translations within the various TLB's implemented on-chip. The allocation is for 16MB and the base address is defined by bits [38:24].

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**MBA_1:** Set by the OS, these bits correspond to address signals [63:24].

7.12 GMADR0_0_2_0_PCI - Offset 18h

GMADR is the PCI aperture used by S/W to access tiled GFX surfaces in a linear fashion.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 18h	0000000Ch

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW/V/L	**ADMSK4096:** This bit is either part of the Memory Base Address (R/W) or part of Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 4096MB. (i.e. MSAC.APSZ[4]=1) **Locked by:** MSAC_0_2_0_PCI.APSZ4
30	0h RW/V/L	**ADMSK2048:** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 2048MB. (i.e. MSAC.APSZ[3]=1) **Locked by:** MSAC_0_2_0_PCI.APSZ3
29	0h RW/V/L	**ADMSK1024:** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 1024MB. (i.e. MSAC.APSZ[2]=1) **Locked by:** MSAC_0_2_0_PCI.APSZ2
28	0h RW/V/L	**ADMSK512:** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 512MB. (i.e. MSAC.APSZ[1]=1) **Locked by:** MSAC_0_2_0_PCI.APSZ1
27	0h RW/V/L	**ADMSK256:** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ.RO and forced to 0 when MSAC.APSZ >= 256MB. (i.e. MSAC.APSZ[0]=1) **Locked by:** MSAC_0_2_0_PCI.APSZ0
26:4	0h RO	**ADM:** Hardwired to 0s to indicate at least 128MB address range.

Bit Range	Default & Access	Field Name (ID): Description
3	1h RO	**PREFMEM:** Hardwired to 1 to enable prefetching.
2:1	2h RO	**MEMTYP:** Hardwired to 2h to indicate 64 bit base address.
0	0h RO	**MIOS:** Hardwired to 0 to indicate memory space.

7.13 GMADR1_0_2_0_PCI - Offset 1Ch

GMADR is the PCI aperture used by S/W to access tiled GFX surfaces in a linear fashion.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**MBA:** Set by the OS, these bits correspond to address signals [63:32].

7.14 IOBAR_0_2_0_PCI - Offset 20h

This register provides the Base offset of the I/O registers within Device #2. Bits 15:6 are programmable allowing the I/O Base to be located anywhere in 16bit I/O Address Space. Bits 2:1 are fixed and return zero; bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded. Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device #2 is turned off or if Internal graphic is disabled through the fuse or fuse override mechanisms. Note that access to this IO BAR is independent of VGA functionality within Device #2. If accesses to this IO bar is allowed, then all 8, 16 or 32 bit IO cycles from IA cores that fall within the 8B are claimed. This IO BAR can be disabled and hidden from system software via DEV2CTL[0] IOBARDIS at offset 0x58.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 20h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:6	0h RW/V/L	**IOBASE:** Set by the OS, these bits correspond to address signals [15:6]. ***Note:*** This field is RO 0's if DEV2CTL[0] IOBARDIS is 1b. **Locked by:** DEV2CTL_0_2_0_PCI.IOBARDIS

Bit Range	Default & Access	Field Name (ID): Description
5:3	0h RO	**Reserved**
2:1	0h RO	**MEMTYPE:** Hardwired to 0s to indicate 32-bit address.
0	1h RO	**MIOS:** Hardwired to '1' to indicate IO space. ***Note:*** This field is RO 0's if DEV2CTL[0] IOBARDIS is 1b.

7.15 SVID2_0_2_0_PCI - Offset 2Ch

This register is used to uniquely identify the subsystem where the PCI device resides.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 2Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**SUBVID:** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

7.16 SID2_0_2_0_PCI - Offset 2Eh

This register is used to uniquely identify the subsystem where the PCI device resides.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 2Eh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW	**SUBID:** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

7.17 ROMADR_0_2_0_PCI - Offset 30h

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0s.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 30h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:18	0h RO	**RBA:** Hardwired to 0's.
17:11	0h RO	**ADMSK:** Hardwired to 0s to indicate 256 KB address range.
10:1	0h RO	**Reserved**
0	0h RO	**RBE:** Hardwired to 0 to indicate ROM not accessible.

7.18 CAPPOINT_0_2_0_PCI - Offset 34h

This register points to a linked list of capabilities implemented by this device.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:2, F:0] + 34h	40h

Bit Range	Default & Access	Field Name (ID): Description
7:0	40h RO	**CPV:** This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the CAPID0 register at offset 40h.

7.19 INTRLINE_0_2_0_PCI - Offset 3Ch

This register is used to communicate interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:2, F:0] + 3Ch	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RW	**INTCON:** Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates to which input of the system interrupt controller the device's interrupt pin is connected.

7.20 INTRPIN_0_2_0_PCI - Offset 3Dh

This register tells which interrupt pin the device uses.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:2, F:0] + 3Dh	01h

Bit Range	Default & Access	Field Name (ID): Description
7:0	1h RO	**INTPIN:** As a single function device, the IGD specifies INTA# as its interrupt pin. Hardwired to 01h = INTA#.

7.21 MINGNT_0_2_0_PCI - Offset 3Eh

The Integrated Graphics Device has no requirement for the settings of Latency Timers.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:2, F:0] + 3Eh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**MGV:** Hardwired to 0s because the IGD does not burst as a PCI compliant master.

7.22 MAXLAT_0_2_0_PCI - Offset 3Fh

The Integrated Graphics Device has no requirement for the settings of Latency Timers.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:2, F:0] + 3Fh	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	0h RO	**MLV:** Hardwired to 0s because the IGD has no specific requirements for how often it needs to access the PCI bus.

7.23 CAPID0_0_2_0_PCI - Offset 40h

The register 'Capability_Identifier'.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 40h	7009h

Bit Range	Default & Access	Field Name (ID): Description
15:8	70h RO	**NEXT_CAP:** This field is hardwired to point to the next PCI Capability structure, the PCIe Capabilities structure at 70h.
7:0	9h RO	**CAP_ID:** This field is hardwired to the value 09h to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

7.24 CAPCTRL0_0_2_0_PCI - Offset 42h

The register 'Capabilities_Control'.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 42h	010Ch

Bit Range	Default & Access	Field Name (ID): Description
15:12	0h RO	**Reserved**
11:8	1h RO	**CAPID_VER:** This field is hardwired to the value 1h to identify the first revision of the CAPID register definition.
7:0	Ch RO	**CAPIDLEN:** This field is hardwired to the value 0Ch to indicate the structure length (12 bytes).

7.25 CAPID0_A_0_2_0_PCI - Offset 44h

Populated by pulling relevant fuses.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO	**Reserved**

7.26 CAPID0_B_0_2_0_PCI - Offset 48h

Populated by pulling relevant fuses.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 48h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Reserved**

7.27 MGGC0_0_2_0_PCI - Offset 50h

Mirror of GGC register from GTTMMADR Space at offset 0x108040.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 50h	0500h

Bit Range	Default & Access	Field Name (ID): Description
15:8	5h RO/V	**GMS:** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. It corresponds to DSM (Data Stolen Memory region) region. The BIOS ensures that memory is pre-allocated only when Internal graphic is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/ enabled.BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0.BIOS Requirement: Given new sizes allow down to 8MB allocation, BIOS has to ensure there is sufficient space for WOPCM and basic GFX Stolen functions.00h:0 MB 01h:32 MB 02h:64 MB 03h:96 MB 04h:128 MB 05h:160 MB 06h:192 MB 07h:224 MB 08h:256 MB 09h:288 MB 0Ah:320 MB 0Bh:352 MB 0Ch:384 MB 0Dh:416 MB 0Eh:448 MB 0Fh:480 MB 10h:512 MB 11h - 1Fh: Reserved 20h:1024 MB 21h - 2Fh: Reserved 30h:1536 MB 31h - 3Fh: Reserved 40h: 2048 MB 41h - EFh: Reserved F0h: 4 MB F1h: 8MB F2h: 12 MB F3h: 16 MB F4h: 20 MB F5h: 24 MB F6h: 28 MB F7h: 32 MB F8h: 36 MB F9h: 40 MB FAh: 44 MB FBh: 48 MB FCh: 52 MB FDh: 56 MB FEh: 60 MB FFh: Reserved Hardware functionality in case of programming this value to Reserved is not guaranteed.
7:6	0h RO/V	**GGMS:** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphic is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register.Hardware functionality in case of programming this value to Reserved is not guaranteed.0x0:No Preallocated Memory0x1:2MB of Preallocated Memory0x2:4MB of Preallocated Memory0x3:8MB of Preallocated Memory
5:3	0h RO	**Reserved**
2	0h RO/V	**VAMEN:** Enables the use of the iGFX engines for Versatile Acceleration.0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 038000h.
1	0h RO/V	**IVD:** 0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00.1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80.BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 7:3 of this register) pre-allocates no memory.
0	0h RO	**Reserved**

7.28 DEVEN_0_2_0_PCI - Offset 54h

Mirror of DEVEN_0_0_0_PCI.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 54h	00BFh

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RO	**Reserved**
13	0h RO	**Reserved**
12:11	0h RO	**Reserved**
10	0h RO	**Reserved**
9:8	0h RO	**Reserved**
7	1h RO/V	**D4EN:** 0: Bus 0 Device 4 is disabled and not visible. 1: Bus 0 Device 4 is enabled and visible. This bit will be set to 0b and remain 0b if Device 4 capability is disabled.
6	0h RO	**Reserved**
5	1h RO	**Reserved**
4	1h RO/V	**D2EN:** 0: Bus 0 Device 2 is disabled and hidden 1: Bus 0 Device 2 is enabled and visible. This bit will be set to 0b and remain 0b if Device 2 capability is disabled.
3	1h RO	**Reserved**
2	1h RO	**Reserved**
1	1h RO	**Reserved**
0	1h RO	**D0EN:** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

7.29 DEV2CTL_0_2_0_PCI - Offset 58h

This register implements a control bit to disable and hide the IOBAR register in systems that do not require legacy IOBAR access to Gfx MMIO registers.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:2, F:0] + 58h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved**
0	0h RW	**IOBARDIS:** System BIOS can choose to disable and hide the IOBAR for systems that do not require legacy IOBAR access to Gfx MMIO registers. 0b: IOBAR is enabled and exposed at offset 0x20 in Device 2 Configuration space. (Default) 1b: IOBAR is disabled and not visible in PCI Configuration Space. Behaves as if hardwired to zeros.

7.30 MSAC_0_2_0_PCI - Offset 60h

This register contains MSAC register which determines the size of the graphics memory aperture (GMADR) in function 0 and in the trusted space, and affects certain bits of the GMADR register. Bits [20:16] 00000b: 128MB, GMADR[26:4] is hardwired to all 0Bits [20:16] 00001b: 256MB, GMADR[27:4] overridden to all 0Bits [20:16] 00010b: illegal (hardware will treat this as 00011b) Bits [20:16] 00011b: 512MB, GMADR[28:27] overridden to all 0Bits [20:16] 00100-00110b: illegal (hardware will treat this as 00111b) Bits [20:16] 00111b: 1024MB, GMADR[29:27] overridden to all 0Bits [20:16] 01000-01110b: illegal (hardware will treat this as 01111b) Bits [20:16] 01111b: 2048MB, GMADR[30:27] overridden to all 0Bits [20:16] 10000-11110b: illegal (hardware will treat this as 11111b) Bits [20:16] 11111b: 4096MB, GMADR[31:27] overridden to all 0.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 60h	00010000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**Reserved**
20	0h RW/V	**APSZ4:** The field 'Untrusted_Aperture_Size_Bit_4' in register 'Multi_Size_Aperture_Control'.
19	0h RW/V	**APSZ3:** The field 'Untrusted_Aperture_Size_Bit_3' in register 'Multi_Size_Aperture_Control'.
18	0h RW/V	**APSZ2:** The field 'Untrusted_Aperture_Size_Bit_2' in register 'Multi_Size_Aperture_Control'.
17	0h RW/V	**APSZ1:** The field 'Untrusted_Aperture_Size_Bit_1' in register 'Multi_Size_Aperture_Control'.
16	1h RW/V	**APSZ0:** The field 'Untrusted_Aperture_Size_Bit_0' in register 'Multi_Size_Aperture_Control'.
15:0	0h RO	**Reserved**

7.31 PUSHAP_0_2_0_PCI - Offset 68h

GT writes this Push Aperture register to ensure aperture writes have been pushed to DRAM.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**TOKEN_VALUE:** 32 bit Token Value. GT (GuC) writes a Dword Token value to this field. A write to this register triggers a write response to GT. The response write will use the value written into this register.

7.32 VTD_STATUS_0_2_0_PCI - Offset 6Ch

This register contains indicator bits for Graphics VTd mode.

Type	Size	Offset	Default
CFG	8 bit	[B:0, D:2, F:0] + 6Ch	00h

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved**
0	0h RW/V	**VTACT:** Reflects GFX VTd Mode is active. 1 - if active. 0 if inactive. Acts as R/W register only during Punit restore - when iommu freeze bit is set. RO otherwise

7.33 PCIECAPHDR_0_2_0_PCI - Offset 70h

PCI Express Capability Header.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 70h	AC10h

Bit Range	Default & Access	Field Name (ID): Description
15:8	ACh RO	**NEXT_PTR:** This field is hardwired to point to the next PCI Capability structure, the MSI Capabilities at ACh.
7:0	10h RO	**CAP_ID:** This field is hardwired to 10h to indicate that this is a PCI Express Capability structure.

7.34 PCIECAP_0_2_0_PCI - Offset 72h

PCI Express Capability.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 72h	0092h

Bit Range	Default & Access	Field Name (ID): Description
15:14	0h RO	**Reserved**
13:9	0h RO	**INTRMSG:** This field indicates which MSI vector is used for the interrupt message generated in association with any of the status bits of this Capability structure. Since this device only supports one MSI vector, this field is hardwired to 0.
8	0h RO	**SLOTIMP:** This field is hardwired to 0 for an endpoint device.
7:4	9h RO	**DEV_TYPE:** This field is hardwired to 9h to indicate a Root Complex Integrated Endpoint.
3:0	2h RO	**CAP_VER:** This field is hardwired to 2h to indicate Functions compliant to PCI Express 3.0 Base Specification.

7.35 DEVICECAP_0_2_0_PCI - Offset 74h

PCI Express Device Capabilities.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 74h	10008000h

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RO	**Reserved**
28	1h RO	**FLRCAP:** Hardwired to 1b to indicate the Function supports the optional Function Level Reset mechanism.
27:26	0h RO	**PWR_LIM_SCALE:** Not applicable for a Root Complex Integrated Endpoint with no Link or Slot. Hardwired to 00b
25:18	0h RO	**CSPLS:** Not applicable for a Root Complex Integrated Endpoint with no Link or Slot. Hardwired to 00h
17:16	0h RO	**Reserved**
15	1h RO	**RBER:** When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1.Hardwired to 1b as this bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions.
14:12	0h RO	**Reserved**
11:9	0h RO	**EPL1AL:** This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L1 state to the L0 state. This does not apply to the integrated graphics device, so it is hardwired to 000b (Maximum of 1 us).
8:6	0h RO	**EPL0AL:** This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L0s state to the L0 state. This does not apply to the integrated graphics device, so it is hardwired to 000b (Maximum of 64 ns).
5	0h RO	**ETFS:** This bit indicates the maximum supported size of the Tag field as a Requester. This does not apply to the integrated graphics device, so it is hardwired to 0b (5-bit Tag field supported).
4:3	0h RO	**PFS:** This field indicates the support for use of unclaimed Function Numbers to extend the number of outstanding transactions for PCIe devices. This does not apply to the integrated graphics device, so it is hardwired to 00b to indicate no Function Number bits are used for Phantom Functions.
2:0	0h RO	**MPSS:** This field indicates the maximum payload size that the Function can support for TLPs. Hardwired to 000b to represents 128 bytes, the minimum allowed value.

7.36 DEVICECTL_0_2_0_PCI - Offset 78h

PCI Express Device Control.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 78h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW/V	**INIT_FLR:** A write of 1b initiates Function Level Reset to the Function.During FLR, a read will return 1b since device 2 reads abort. If a local panel is powered on and configured to power down on reset, the FLR will typically take several hundred milliseconds to complete. The worst possible, although unrealistic, delay is 5 seconds.
14:12	0h RO	**MRRS:** Functions that do not generate Read Requests larger than 128 bytes and Functions that do not generate Read Requests on their own behalf are permitted to implement this field as Read Only (RO) with a value of 000b.
11	0h RO	**ENS:** This bit is permitted to be hardwired to 0b if a Function would never Set the No Snoop attribute in transactions it initiates. The graphics device never generates a PCI Express TLP.
10	0h RO	**APPME:** Functions that do not implement this capability hardwire this bit to 0b.
9	0h RO	**PFE:** Functions that do not implement this capability hardwire this bit to 0b.
8	0h RO	**ETFE:** Functions that do not implement this capability hardwire this bit to 0b.
7:5	0h RO	**MPS:** Functions that support only the 128-byte max payload size are permitted to hardwire this field to 000b.
4	0h RO	**ERO:** A Function is permitted to hardwire this bit to 0b if it never sets the Relaxed Ordering attribute in transactions it initiates as a Requester. The graphics device never generates a PCI Express TLP.
3	0h RO	**URRE:** A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.
2	0h RO	**FEE:** A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.
1	0h RO	**NFEE:** A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.
0	0h RO	**CEE:** A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.

7.37 DEVICESTS_0_2_0_PCI - Offset 7Ah

PCI Express Capability Structure.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 7Ah	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	0h RO	**TP:** When Set, this bit indicates that the Function has issued Non-Posted Requests that have not been completed.A Function reports this bit is cleared only when all outstanding Non-Posted Requests have completed or have been terminated by the Completion Timeout mechanism. This bit must also be cleared upon the completion of an FLR.
4	0h RO	**APD:** Functions that require Aux power report this bit as Set if Aux power is detected by the Function. Hardwired to 0b, the integrated graphics device does not require Aux power.
3	0h RO	**URD:** This bit indicates the Function received an Unsupported Request. Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.
2	0h RO	**FED:** This bit indicates the status of Fatal errors detected. Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.
1	0h RO	**NFED:** This bit indicates the status of Non-Fatal errors detected. Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.
0	0h RO	**CED:** This bit indicates the status of Correctable errors detected. Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.

7.38 MSI_CAPID_0_2_0_PCI - Offset ACh

When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + ACh	D005h

Bit Range	Default & Access	Field Name (ID): Description
15:8	D0h RO	**POINTNEXT:** This is a hardwired pointer to the next item in the capabilities list.
7:0	5h RO	**CAPID:** This field is hardwired to the value 05h to identify the CAP_ID as being for MSI registers.

7.39 MC_0_2_0_PCI - Offset AEh

Message Signaled Interrupt control register. System software can modify bits in this register, but the device is prohibited from doing so. If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + AEh	0100h

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	**Reserved**
8	1h RO	**PVMASKCAP:** SR-IOV requires this capability.
7	0h RO	**CAP64B:** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message address register and is incapable of generating a 64-bit memory address.
6:4	0h RW/V	**MME:** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested.Value: Number of requests 000: 1001: 2010: 4011: 8100: 16101: 32110: Reserved111: Reserved
3:1	0h RO	**MMC:** System Software reads this field to determine the number of messages being requested by this device. Hardwired to 000b to indicate number of requests is 1.
0	0h RW/V	**MSIEN:** Controls the ability of this device to generate MSIs.

7.40 MA_0_2_0_PCI - Offset B0h

This register contains the Message Address for MSIs sent by the device.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + B0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW/V	**MESSADD:** Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	0h RO	**FDWORD:** Hardwired to 0 so that addresses assigned by system software are always aligned on a DWORD address boundary.

7.41 MD_0_2_0_PCI - Offset B4h

This register contains the Message Data for MSIs sent by the device.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + B4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0h RW/V	**MESSDATA:** Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

7.42 MSI_MASK_0_2_0_PCI - Offset B8h

This register contains the MSI Mask Bits.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + B8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/V	**MASKBIT:** For each Mask bit that is set, the function is prohibited from sending the associated message.

7.43 MSI_PEND_0_2_0_PCI - Offset BCh

This register contains the MSI Pending Bits.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + BCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RO/V	**PENDBIT:** For each Pending bit that is set, the function has a pending associated message. If this bit is set when the corresponding vector's Mask bit is cleared, the function will send an MSI and then clear the Pending bit.

7.44 BDSM0_0_2_0_PCI - Offset C0h

Mirror of BSDM from GTTMMADR space. This register contains the base address of graphics data stolen DRAM memory.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + C0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO/V	**BDSM_LSB:** This register contains bits 63 to 20 of the base address of stolen DRAM memory. BIOS is now able to allocate GDSM above 4GB.
19:0	0h RO	**Reserved**

7.45 BDSM1_0_2_0_PCI - Offset C4h

Mirror of BSDM from GTTMMADR space. This register contains the base address of graphics data stolen DRAM memory.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + C4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**BDSM_MSB:** This register contains bits 63 to 20 of the base address of stolen DRAM memory. BIOS is now able to allocate GDSM above 4GB.

7.46 GFXVTDBAR_LSB_0_2_0_PCI - Offset C8h

This is the base address for the Graphics VTD configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the GFX-VTD configuration space is disabled and must be enabled by writing a 1 to GFXVTDBAREN.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + C8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:12	0h RW	**GFXVTDBAR:** This field corresponds to bits 31 to 12 of the base address GFX-VTD configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the GFX-VTD register set.
11:1	0h RO	**Reserved**
0	0h RW/V	**GFXVTDBAREN:** 0: GFX-VTBAR is disabled and does not claim any memory. 1: GFX-VTBAR memory mapped accesses are claimed and decoded appropriately. This bit will remain 0 if VTd capability is disabled.

7.47 GFXVTDBAR_MSB_0_2_0_PCI - Offset CCh

This is the base address for the Graphics VTD configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the GFX-VTD configuration space is disabled and must be enabled by writing a 1 to GFXVTDBAREN. BIOS programs this register, after which the register cannot be altered.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + CCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**GFXVTDBAR:** This field corresponds to bits 63 to 32 of the base address GFX-VTD configuration space. BIOS will program this register, resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the GFX-VTD register set.

7.48 PMCAPID_0_2_0_PCI - Offset D0h

This register contains the PCI Power Management Capability ID and the next capability pointer.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + D0h	0001h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RO	**NEXT_PTR:** This is a hardwired pointer to the next item in the capabilities list.
7:0	1h RO	**CAP_ID:** Hardwired to 01h for power management.

7.49 PMCAP_0_2_0_PCI - Offset D2h

This register provides information on the capabilities of the function related to power management.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + D2h	0022h

Bit Range	Default & Access	Field Name (ID): Description
15:11	0h RO	**PMES:** This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	0h RO	**D2:** Hardwired to 0 to indicate the D2 power management state is not supported.
9	0h RO	**D1:** Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6	0h RO	**Reserved**
5	1h RO	**DSI:** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	0h RO	**Reserved**
3	0h RO	**PMECLK:** Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	2h RO	**VER:** Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification.

7.50 PMCS_0_2_0_PCI - Offset D4h

The register 'Power_Management_Control_and_Status'.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + D4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**PMESTS:** This bit is hardwired to 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:13	0h RO	**DSCALE:** This field is hardwired to 00 to indicate IGD does not support data register.
12:9	0h RO	**DSEL:** This field is hardwired to 0h to indicate IGD does not support data register.

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**PMEEN:** This bit is hardwired to 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2	0h RO	**Reserved**
1:0	0h RW/V	**PWRSTAT:** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. Bits[1:0]Power state00:D0Default01:D1Not Supported10:D2Not Supported11:D3

7.51 SWSMI_0_2_0_PCI - Offset E0h

As long as there is the potential that DVO port legacy drivers exist which expect this register at this address, Dev#2F0 address E0h-E1h must be reserved for this register.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + E0h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	0h RW	**SWSB:** The field 'Software_Scratch_Bits' in register 'Software_SMI'.
7:1	0h RW	**SWF:** Used to indicate caller and SMI function desired, as well as return result.
0	0h RW	**GSSMIE:** When Set this bit will trigger an SMI. Software must write a '0' to clear this bit.SMI will be triggered only if SWSCI[SMISCISEL] is set to select SMI.

7.52 GSE_0_2_0_PCI - Offset E4h

This register can be accessed by either Byte, Word, or Dword PCI configuration cycles. A write to this register will cause the Graphics System Event display interrupt if it is enabled and unmasked in the display interrupt registers.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Reserved**

7.53 SWSCI_0_2_0_PCI - Offset E8h

This register serves 2 purposes:1) Support selection of SMI or SCI event source (SMISCISEL - bit15) 2) SCI Event trigger (GSSCIE - bit 0). To generate a SW SCI event, software should program bit 15 (SMISCISEL) to 1. This is typically programmed once (assuming SMIs are never triggered). On a '0' to '1' subsequent transition in bit 0 of this register (caused by a software write operation), a SCI message will be sent to cause the TCOSCI_STS bit in GPE0 register to be set to 1. The corresponding SCI event handler in BIOS is to be defined as a _Lxx method, indicating level trigger to the operating system. Once written as 1, software must write a '0' to this bit to clear it, and all other write transitions (1-0, 0-0, 1-1) will not cause a SCI message to be sent. To generate a SW SMI event, software should program bit 15 to 0 and trigger SMI via writes to SWSMI register (See SWSMI register for programming details).

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + E8h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**SMISCISEL:** 0 = SMI (default) 1 = SCI If selected event source is SMI, SMI trigger and associated scratch bits accesses are performed via SWSMI register. If SCI event source is selected, the rest of the bits in this register provide SCI trigger capability and associated SW scratch pad area.
14:1	0h RW	**SCISB:** Read/write bits not used by hardware.
0	0h RW	**GSSCIE:** If SCI event is selected (SMISCISEL = 1), on a 0 to 1 transition of GSSCIE bit, a SCI message will be sent to cause the TCOSCI_STS bit in GPE0 register to be set to 1. Software must write a 0 to clear this bit.

7.54 PAVPC0_0_2_0_PCI - Offset F0h

Device 2 Mirror of Protected Audio Video Control.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + F0h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO/V	**WOPCMBASE_LSB:** Base value programmed (from Top of Stolen Memory). The programmed value must be consistent with the WOPCM Size programming.
19:9	0h RO	**Reserved**
8:7	0h RO/V	**WOPCMSIZE:** This register determines the WOPCM size. The programmed value must be consistent with the WOPCM base programming. 00b: 1MB (default) 01b: 2MB 10b: 4MB 11b: 8MB
6	0h RO/V	**ASMFEN:** 0: Disable ASMF 1: Enable ASMF
5	0h RO	**Reserved**
4	0h RO/V	**OVTATTACK:** Override of unsolicited connection state attack and terminate. 0: Disable override; attack terminate allowed 1: Enable override; attack terminate disallowed
3	0h RO/V	**HVYMODSEL:** Heavy/light encryption mode select. 0: Surface encryption is disabled - Light mode 1: Surface encryption is enabled
2	0h RO/V	**LOCK:** BIOS will set this bit with bit 0 and/or bit 1.
1	0h RO/V	**PAVPE:** 0: PAVP functionality disabled 1: PAVP functionality enabled
0	0h RO/V	**PCME:** Protected content memory enable.

7.55 PAVPC1_0_2_0_PCI - Offset F4h

Device 2 Mirror of Protected Audio Video Control.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + F4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RO/V	**WOPCMBASE_MSB:** Base value programmed (from Top of Stolen Memory). The programmed value must be consistent with the WOPCM Size programming.

7.56 SRID_0_2_0_PCI - Offset F8h

Debug

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + F8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**SRID_MSB:** The four MSB of the stepping revision ID
19:16	0h RW	**SRID_LSB:** Those are the four LSB of SRID as set by fuses
15:0	0h RO	**Reserved**

7.57 ASLS_0_2_0_PCI - Offset FCh

This is a software scratch register. The exact bit register usage must be worked out in common between System BIOS and driver software. For each device, the ASL control method requires two bits for DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for DGS (enable/disable requested), and two bits for DCS (enabled now/disabled now, connected or not).

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + FCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**DSS:** Software controlled usage to support device switching.

7.58 PASID_EXTCAP_0_2_0_PCI - Offset 100h

PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 100h	2001001Bh

Bit Range	Default & Access	Field Name (ID): Description
31:20	200h RO	**NCO:** This is a hardwired pointer to the next item in the capabilities list.
19:16	1h RO	**V:** Hardwired to capability version 1.
15:0	1Bh RO	**CAPID:** Hardwired to the PASID Extended Capability ID.

7.59 PASID_CAP_0_2_0_PCI - Offset 104h

PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 104h	1400h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12:8	14h RO	**MPW:** Indicates the width of the PASID field supported by the Endpoint. Hardwired to 14h to indicate support for all PASID values (20 bits).
7:3	0h RO	**Reserved**
2	0h RO	**PMS:** Hardwired to 0, the Endpoint supports operating in Non-privileged mode only, and will never request privileged mode in requests-with-PASID.
1	0h RO	**EPS:** Hardwired to 0, the Endpoint supports requests-with-PASID that requests execute permission.
0	0h RO	**Reserved**

7.60 PASID_CTRL_0_2_0_PCI - Offset 106h

Process Address Space ID (PASID) control for Device-2.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 106h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:3	0h RO	**Reserved**
2	0h RO	**PME:** Hardwired to 0, the Endpoint is not permitted to request privileged mode in requests-with-PASID.
1	0h RW	**EPE:** If Set, the Endpoint is permitted to request execute permission in requests-with-PASID. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if this bit changes value when ATS Enable field in ATS Capability is Set. Processor graphics does not use this field. Software is expected to Set this field before configuring extended-context-entry for Device-2 with the Execute Request Enable field Set.
0	0h RW	**PE:** If Set, the Endpoint is permitted to generate requests-with-PASID. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if this bit changes value when ATS Enable field in ATS Capability is Set. If Privileged Mode Supported field in PASID Capability register is Clear, then this field is treated as Reserved(0).Processor graphic does not use this field. Software is expected to Set this field before configuring extended-context-entry for Device-2 with Supervisor Request Enable field Set. For compatibility reasons, this field is implemented as RW.

7.61 ATS_EXTCAP_0_2_0_PCI - Offset 200h

ATS Capability reports support for Device-TLBs on Device-2, compliant to PCI Express ATS specification.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 200h	3001000Fh

Bit Range	Default & Access	Field Name (ID): Description
31:20	300h RO	**NCO:** This is a hardwired pointer to the next item in the capabilities list. Value 300h in this field provides the offset for Page-Request Capability.
19:16	1h RO	**V:** Hardwired to capability version 1.
15:0	Fh RO	**CAPID:** Hardwired to the ATS Extended Capability ID.

7.62 ATS_CAP_0_2_0_PCI - Offset 204h

ATS Capability reports support for Device-TLBs on Device-2, compliant to PCI Express ATS specification.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 204h	0060h

Bit Range	Default & Access	Field Name (ID): Description
15:7	0h RO	**Reserved**
6	1h RO	**GIS:** If Set, the Function supports Invalidation Requests that have the Global Invalidate bit Set. If Clear, the Function ignores the Global Invalidate bit in all Invalidate requests. Reserved.
5	1h RO	**PAR:** Hardwired to 1, the Untranslated Address is always aligned to a 4096 byte boundary. Processor Graphics reports value of 1b indicating all VT-d and SVM translations are page-aligned.
4:0	0h RO	**IQE:** The number of Invalidate Requests that the endpoint can accept before putting back pressure on the upstream connection. Hardwired to 0h, the function can accept 32 Invalidate Requests.

7.63 ATS_CTRL_0_2_0_PCI - Offset 206h

The register 'ATS_Control'.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 206h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RW	**AE:** When Set, the function is enabled to cache translations. Processor graphic ignores this field, as GT uses GTLB as IOTLB and only pretends to software that it has a Device-TLB. Software is expected to Set this field before configuring extended context-entry for Device2 with Page Request Enable field Set. For compatibility, this field is implemented as RW as software can read it to determine ATS enable status.
14:5	0h RO	**Reserved**
4:0	0h RW	**STU:** This value indicates to the Endpoint the minimum number of 4096-byte blocks that is indicated in a Translation Completion or Invalidate Request. This is a power of 2 multiple and the number of blocks is 2^STU. A value of 0 indicates one block and value 1F indicates 2^31 blocks. For IGD this must be programmed to 0h for 4KB as smallest translation unit.

7.64 PR_EXTCAP_0_2_0_PCI - Offset 300h

Page Request Extended Capability reports support for page-faults on Device-2, compliant to PCI-Express ATS 1.1 Specification.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 300h	00010013h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO/V	**NCO:** This is a hardwired pointer to the next item in the capabilities list. Value 000h (Default) indicates that this is the end of the PCI-Express Extended capability Linked List. When Graphics Virtualization is enabled, this field is hardwired to point to the next PCI Capability structure, the SRIOV Extended Capability Header at 320h. When Graphics Virtualization is disabled, this field will be hardwired to 000h to indicate the end of PCI-Express Extended capability Linked List.
19:16	1h RO	**V:** Hardwired to capability version 1.
15:0	13h RO	**CAPID:** Hardwired to the Page Request Extended Capability ID.

7.65 PR_CTRL_0_2_0_PCI - Offset 304h

The register 'Page_Request_Control'.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 304h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:2	0h RO	**Reserved**
1	0h RO	**RST:** When the Enable field is clear, or is being cleared in the same register update that sets this field, writing a 1b to this field, clears the associated implementation dependent page request credit Counter and pending request state for the associated Page Request Interface. No action is initiated if this field is written to 0b or if this field is written with any value when the PRE field is set. Processor graphic does not use this field, and hardwires it as read-only (0).
0	0h RW	**PRE:** When Set, indicates that the page request interface on the endpoint is allowed to make page requests. If both this field and the Stopped field in Page Request Status register are Clear, then the Page request interface will not issue new page requests, but has outstanding page requests for which page response is not yet received. When this field transitions from 0 to 1, all the status fields in the Page-Request Status register are cleared. Enabling a page request interface that has not successfully stopped has indeterminate results.

7.66 PR_STATUS_0_2_0_PCI - Offset 306h

The register 'Page_Request_Status'.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 306h	8100h

Bit Range	Default & Access	Field Name (ID): Description
15	1h RO	**PRPR:** If set, the Function expects a PASID TLP Prefix on PRG Response Messages when the corresponding page requests had a PASID TLP Prefix. If Clear, the function does not expect PASID TLP Prefixes on any PRG Response Message. Function behavior is undefined if this bit is Clear and the Function receives a PRG Response Message with a PASID TLP Prefix. Function behavior is undefined if this bit is Set and the Function receives a PRG Response Message with no PASID TLP Prefix when the corresponding Page Requests had a PASID TLP Prefix. This bit is RsvdZ if the Function does not support the PASID TLP Prefix.
14:9	0h RO	**Reserved**
8	1h RO	**S:** When this field is Set, the associated page request interface has stopped issuing additional Page requests and that all previously issued Page requests have completed. When this field is clear the associate Page request interface either has not stopped or has stopped issuing new Page requests but has outstanding Page requests.
7:2	0h RO	**Reserved**
1	0h RW/V	**UPGRI:** When Set, indicates the function received a PRG response message containing a PRG index that has no matching request, a response failure. This field is Set by the Function and cleared when a 1b is written to the field.
0	0h RW/V	**RF:** When Set, indicates the function received a PRG response message indicating a response failure. The function expects no further response from the host (any received are ignored). This field is Set by the Function and cleared when a 1b is written to this field.

7.67 OPRC_0_2_0_PCI - Offset 308h

The register 'Outstanding_Page_Request_Capacity'.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 308h	00008000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	8000h RO	**OPRC:** This register contains the number of outstanding page request messages the associated Page Request Interface physically supports. This is the upper limit on the number of pages that can be usefully allocated to the Page Request Interface. Hardwired to 32,768 requests.

7.68 OPRA_0_2_0_PCI - Offset 30Ch

The register 'Outstanding_Page_Request_Allocation'.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 30Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**OPRA:** This register contains the number of outstanding page request messages the associated Page Request Interface is allowed to issue.

7.69 SRIOV_ECAPHDR_0_2_0_PCI - Offset 320h

SR-IOV Extended Capability Header.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 320h	00010010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RO	**NEXT:** Next capability Offset. Value = 0x000 to indicate the end of the Extended Capability List.
19:16	1h RO	**CAP_VER:** Capability Version.
15:0	10h RO	**PCIE_ECAP_ID:** PCIE Extended Capability ID.

7.70 SRIOV_CAP_0_2_0_PCI - Offset 324h

Defines SR-IOV Capabilities.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 324h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:21	0h RO	**VF_MIG_INTR_MSG_NUM:** Value: 0. VF Migration is not supported.
20:2	0h RO	**Reserved**
1	0h RO	**ARI_CAP_HIER_PRESERVED:** Value: 0. ARI not supported.
0	0h RO	**VF_MIG_CAP:** Value: 0. VF Migration not supported.

7.71 SRIOV_CTRL_0_2_0_PCI - Offset 328h

SR-IOV Control Register.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 328h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:5	0h RO	**Reserved**
4	0h RO	**ARI_CAPHIER:** Hardwired to 0. ARI capability is not supported.
3	0h RW/V	**VF_MSE:** SW shall set this bit before setting VF Enable. (to allow VF memory space response)
2	0h RO	**VF_MIG_INTR_EN:** VF migration is not supported.
1	0h RO	**VF_MIG_EN:** VF migration is not supported.
0	0h RW/V	**VF_EN:** System SW shall set this bit to enable VFs. Setting/Clearing this bit shall result in an interrupt to GUC. This allows the GuC and subsequently the PF to take appropriate action to comprehend virtualization.

7.72 SRIOV_STS_0_2_0_PCI - Offset 32Ah

SR-IOV Status Register.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 32Ah	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:1	0h RO	**Reserved**
0	0h RO	**VF_MIG_STS:** VF Migration Status.

7.73 SRIOV_INITVFS_0_2_0_PCI - Offset 32Ch

Defines Initial number of VFs available to the VMM.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 32Ch	0007h

Bit Range	Default & Access	Field Name (ID): Description
15:0	7h RO/V	**INITIAL_VFS:** For SR-IOV implementation, this value must exactly match the Total VFs.

7.74 SRIOV_TOTVFS_0_2_0_PCI - Offset 32Eh

Defines the Total number of VFs available to the VMM.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 32Eh	0007h

Bit Range	Default & Access	Field Name (ID): Description
15:0	7h RO	**TOTAL_VFS:** Indicates the maximum number of VFs that could be associated with the PF.

7.75 SRIOV_NUMOFVFS_0_2_0_PCI - Offset 330h

Number of VFs enabled by the VMM.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 330h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RO	**Reserved**
23:16	0h RO	**FUN_DPNDNCY_LINK:** Same value as the Physical function number, indicating no Dependency.
15:0	0h RW/V	**NUMOF_VFS:** System SW shall set this field to control the number of VFs that are visible. This field must be programmed before setting VF Enable. Changing this field when VF Enable is set will produced undefined behavior as per the SR-IOV specification. HW will ignore the new value programmed.

7.76 FIRST_VF_OFFSET_0_2_0_PCI - Offset 334h

Defines the offset of the function number from the PF to the first VF.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 334h	0001h

Bit Range	Default & Access	Field Name (ID): Description
15:0	1h RO	**FIRST_VF_OFFSET:** Defines the routing ID offset of the first VF that is associated with the PF that contains this Capability structure. The first VFs 16-bit Routing ID is calculated by adding the contents of this field to the Routing ID of the PF containing this field ignoring any carry, using unsigned, 16-bit arithmetic. The value of this field is hardwired to 0001h.

7.77 VF_STRIDE_0_2_0_PCI - Offset 336h

Defines the stride of the function number from one VF to the next.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 336h	0001h

Bit Range	Default & Access	Field Name (ID): Description
15:0	1h RO	**VF_STRIDE:** Defines the Routing ID offset from one VF to the next one for all VFs associated with the PF that contains this Capability structure. The next VFs 16-bit Routing ID is calculated by adding the contents of this field to the Routing ID of the current VF, ignoring any carry, using unsigned 16-bit arithmetic. The value of this field is hardwired to 0001h.

7.78 VF_DEVICEID_0_2_0_PCI - Offset 33Ah

Defines the Device ID to be used by all Virtual Functions.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:2, F:0] + 33Ah	0A80h

Bit Range	Default & Access	Field Name (ID): Description
15:0	A80h RO/V	**VF_DEVICEID:** Mirror the same device ID as the PF.

7.79 SUPPORTED_PAGE_SIZES_0_2_0_PCI - Offset 33Ch

Defines the System Page Sizes supported by this SR-IOV implementation.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 33Ch	00000513h

Bit Range	Default & Access	Field Name (ID): Description
31:0	513h RO	**PAGE_SIZES:** This field indicates the page sizes supported by the PF. This PF supports a page size of 2^(n+12) if bit n is Set. For example, if bit 0 is Set, the PF supports 4-KB page sizes. PFs are required to support 4-KB, 8-KB, 64-KB, 256-KB, 1-MB, and 4-MB page sizes. All other page sizes are optional, and not supported in this implementation.

7.80 SYSTEM_PAGE_SIZES_0_2_0_PCI - Offset 340h

Defines the System Page Size chosen by the VMM.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 340h	00000001h

Bit Range	Default & Access	Field Name (ID): Description
31:0	1h RO	**SYS_PAGE_SIZES:** This field defines the page size the system will use to map the VFs memory addresses. Software must set the value of the System Page Size to one of the page sizes set in the Supported Page Sizes field. As with Supported Page Sizes, if bit n is Set in System Page Size, the VFs associated with this PF are required to support a page size of 2^(n+12). For example, if bit 1 is Set, the system is using an 8-KB page size. The results are undefined if System Page Size is zero. The results are undefined if more than one bit is set in System Page Size. The results are undefined if a bit is Set in System Page Size that is not Set in Supported Page Sizes. When System Page Size is set, the VF associated with this PF is required to align all BAR resources 20 on a System Page Size boundary. Each VF BARn or VF BARn pair shall be aligned on a System Page Size boundary. Each VF BARn or VF BARn pair defining a non-zero address space shall be sized to consume an integer multiple of System Page Size bytes. All data structures requiring page size alignment within a VF shall be aligned on a System Page Size boundary. VF Enable must be zero when System Page Size is written. The results are undefined if System Page Size is written when VF Enable is Set. Default value is 1h (i.e., 4 KB), and that is the only value allowed for this implementation.

7.81 VF_BAR0_LDW_0_2_0_PCI - Offset 344h

Lower DW of the BAR that defines the base address of GTTMMADR for all VFs.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 344h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:24	0h RW/V	**VF_GTTMMADDR_LDW:** VF GTTMMADDR Lower DW
23:4	0h RO	**VF_GTTMMADDR_LDW_MASK:** VF GTTMMADDR Lower DW Mask

Bit Range	Default & Access	Field Name (ID): Description
3	0h RO	**PREFETCHABLE:** Prefetchable
2:1	2h RO	**BAR_TYPE:** Type. Value 10 indicates 64 bit BAR
0	0h RO	**MEM_SPACE_IND:** Memory space Indicator. Value 0 indicates memory space

7.82 VF_BAR0_UDW_0_2_0_PCI - Offset 348h

Upper DW of the BAR that defines the base address of GTTMMADR for all VFs.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 348h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**VF_GTTMMADDR_UDW:** VF GTTMMADDR Upper DW

7.83 VF_BAR1_LDW_0_2_0_PCI - Offset 34Ch

Lower DW of the BAR that defines the base address of GMADR for all VFs.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 34Ch	0000000Ch

Bit Range	Default & Access	Field Name (ID): Description
31:29	0h RW/V	**VF_GMADDR_LDW:** VF GMADDR Lower DW
28:4	0h RO	**VF_GMADDR_LDW_MASK:** VF GMADDR Lower DW Mask
3	1h RO	**PREFETCHABLE:** Prefetchable
2:1	2h RO	**BAR_TYPE:** Type. Value 10 indicates 64 bit BAR
0	0h RO	**MEM_SPACE_IND:** Memory space Indicator. Value 0 indicates memory space

7.84 VF_BAR1_UDW_0_2_0_PCI - Offset 350h

Upper DW of the BAR that defines the base address of GMADR for all VFs.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 350h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW/V	**VF_GMADDR_UDW:** VF GMADDR Upper DW

7.85 VF_BAR2_LDW_0_2_0_PCI - Offset 354h

Lower DW of Unused BAR.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 354h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Reserved**

7.86 VF_BAR2_UDW_0_2_0_PCI - Offset 358h

Upper DW of Unused BAR.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 358h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Reserved**

7.87 VF_MIGST_OFFSET_0_2_0_PCI - Offset 35Ch

Defines offset from a PF BAR to the VF Migration State Array. VF Migration not supported in this implementation.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:2, F:0] + 35Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Reserved**

8 Graphics VT BAR (GFXVTBAR) Registers

This chapter documents the GFXVTBAR registers. Base address of these registers is defined in the GFXVTBAR_0_0_0_MCHBAR_NCU register which resides in the MCHBAR register collection.

Table 8-1. Summary of GFXVTBAR Registers (Sheet 1 of 3)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	Version Register (VER_REG_0_0_0_VTDBAR)	00000040h
8h	8	Capability Register (CAP_REG_0_0_0_VTDBAR)	01C0000C40660462h
10h	8	Extended Capability Register (ECAP_REG_0_0_0_VTDBAR)	0000049E2FF0505Eh
18h	4	Global Command Register (GCMD_REG_0_0_0_VTDBAR)	00000000h
1Ch	4	Global Status Register (GSTS_REG_0_0_0_VTDBAR)	00000000h
20h	8	Root Table Address Register (RTADDR_REG_0_0_0_VTDBAR)	0000000000000000h
28h	8	Context Command Register (CCMD_REG_0_0_0_VTDBAR)	0800000000000000h
34h	4	Fault Status Register (FSTS_REG_0_0_0_VTDBAR)	00000000h
38h	4	Fault Event Control Register (FECTL_REG_0_0_0_VTDBAR)	80000000h
3Ch	4	Fault Event Data Register (FEDATA_REG_0_0_0_VTDBAR)	00000000h
40h	4	Fault Event Address Register (FEADDR_REG_0_0_0_VTDBAR)	00000000h
44h	4	Fault Event Upper Address Register (FEUADDR_REG_0_0_0_VTDBAR)	00000000h
58h	8	Advanced Fault Log Register (AFLOG_REG_0_0_0_VTDBAR)	0000000000000000h
64h	4	Protected Memory Enable Register (PMEN_REG_0_0_0_VTDBAR)	00000000h
68h	4	Protected Low Memory Base Register (PLMBASE_REG_0_0_0_VTDBAR)	00000000h
6Ch	4	Protected Low-Memory Limit Register (PLMLIMIT_REG_0_0_0_VTDBAR)	00000000h
70h	8	Protected High-Memory Base Register (PHMBASE_REG_0_0_0_VTDBAR)	0000000000000000h
78h	8	Protected High-Memory Limit Register (PHMLIMIT_REG_0_0_0_VTDBAR)	0000000000000000h
80h	8	Invalidation Queue Head Register (IQH_REG_0_0_0_VTDBAR)	0000000000000000h
88h	8	Invalidation Queue Tail Register (IQT_REG_0_0_0_VTDBAR)	0000000000000000h
90h	8	Invalidation Queue Address Register (IQA_REG_0_0_0_VTDBAR)	0000000000000000h
9Ch	4	Invalidation Completion Status Register (ICS_REG_0_0_0_VTDBAR)	00000000h

Table 8-1. Summary of GFXVTBAR Registers (Sheet 2 of 3)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
A0h	4	Invalidation Event Control Register (IECTL_REG_0_0_0_VTDBAR)	80000000h
A4h	4	Invalidation Event Data Register (IEDATA_REG_0_0_0_VTDBAR)	00000000h
A8h	4	Invalidation Event Address Register (IEADDR_REG_0_0_0_VTDBAR)	00000000h
ACh	4	Invalidation Event Upper Address Register (IEUADDR_REG_0_0_0_VTDBAR)	00000000h
B8h	8	Interrupt Remapping Table Address Register (IRTA_REG_0_0_0_VTDBAR)	0000000000000000h
C0h	8	Page Request Queue Head Register (PQH_REG_0_0_0_VTDBAR)	0000000000000000h
C8h	8	Page Request Queue Tail Register (PQT_REG_0_0_0_VTDBAR)	0000000000000000h
D0h	8	Page Request Queue Address Register (PQA_REG_0_0_0_VTDBAR)	0000000000000000h
DCh	4	Page Request Status Register (PRS_REG_0_0_0_VTDBAR)	00000000h
E0h	4	Page Request Event Control Register (PECTL_REG_0_0_0_VTDBAR)	80000000h
E4h	4	Page Request Event Data Register (PEDATA_REG_0_0_0_VTDBAR)	00000000h
E8h	4	Page Request Event Address Register (PEADDR_REG_0_0_0_VTDBAR)	00000000h
ECh	4	Page Request Event Upper Address Register (PEUADDR_REG_0_0_0_VTDBAR)	00000000h
100h	8	MTRR Capability Register (MTRRCAP_0_0_0_VTDBAR)	0000000000000000h
108h	8	MTRR Default Type Register (MTRRDEFAULT_0_0_0_VTDBAR)	0000000000000000h
120h	8	Fixed-Range MTRR Format 64K-00000 (MTRR_FIX64K_00000_REG_0_0_0_VTDBAR)	0000000000000000h
128h	8	Fixed-Range MTRR Format 16K-80000 (MTRR_FIX16K_80000_REG_0_0_0_VTDBAR)	0000000000000000h
130h	8	Fixed-Range MTRR Format 16K-A0000 (MTRR_FIX16K_A0000_REG_0_0_0_VTDBAR)	0000000000000000h
138h	8	Fixed-Range MTRR Format 4K-C0000 (MTRR_FIX4K_C0000_REG_0_0_0_VTDBAR)	0000000000000000h
140h	8	Fixed-Range MTRR Format 4K-C8000 (MTRR_FIX4K_C8000_REG_0_0_0_VTDBAR)	0000000000000000h
148h	8	Fixed-Range MTRR Format 4K-D0000 (MTRR_FIX4K_D0000_REG_0_0_0_VTDBAR)	0000000000000000h
150h	8	Fixed-Range MTRR Format 4K-D8000 (MTRR_FIX4K_D8000_REG_0_0_0_VTDBAR)	0000000000000000h
158h	8	Fixed-Range MTRR Format 4K-E0000 (MTRR_FIX4K_E0000_REG_0_0_0_VTDBAR)	0000000000000000h
160h	8	Fixed-Range MTRR Format 4K-E8000 (MTRR_FIX4K_E8000_REG_0_0_0_VTDBAR)	0000000000000000h
168h	8	Fixed-Range MTRR Format 4K-F0000 (MTRR_FIX4K_F0000_REG_0_0_0_VTDBAR)	0000000000000000h

Table 8-1. Summary of GFXVTBAR Registers (Sheet 3 of 3)

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
170h	8	Fixed-Range MTRR Format 4K-F8000 (MTRR_FIX4K_F8000_REG_0_0_0_VTDBAR)	0000000000000000h
180h	8	Variable-Range MTRR Format Physical Base 0 (MTRR_PHYSBASE0_REG_0_0_0_VTDBAR)	0000000000000000h
188h	8	Variable-Range MTRR Format Physical Mask 0 (MTRR_PHYSMASK0_REG_0_0_0_VTDBAR)	0000000000000000h
190h	8	Variable-Range MTRR Format Physical Base 1 (MTRR_PHYSBASE1_REG_0_0_0_VTDBAR)	0000000000000000h
198h	8	Variable-Range MTRR Format Physical Mask 1 (MTRR_PHYSMASK1_REG_0_0_0_VTDBAR)	0000000000000000h
1A0h	8	Variable-Range MTRR Format Physical Base 2 (MTRR_PHYSBASE2_REG_0_0_0_VTDBAR)	0000000000000000h
1A8h	8	Variable-Range MTRR Format Physical Mask 2 (MTRR_PHYSMASK2_REG_0_0_0_VTDBAR)	0000000000000000h
1B0h	8	Variable-Range MTRR Format Physical Base 3 (MTRR_PHYSBASE3_REG_0_0_0_VTDBAR)	0000000000000000h
1B8h	8	Variable-Range MTRR Format Physical Mask 3 (MTRR_PHYSMASK3_REG_0_0_0_VTDBAR)	0000000000000000h
1C0h	8	Variable-Range MTRR Format Physical Base 4 (MTRR_PHYSBASE4_REG_0_0_0_VTDBAR)	0000000000000000h
1C8h	8	Variable-Range MTRR Format Physical Mask 4 (MTRR_PHYSMASK4_REG_0_0_0_VTDBAR)	0000000000000000h
1D0h	8	Variable-Range MTRR Format Physical Base 5 (MTRR_PHYSBASE5_REG_0_0_0_VTDBAR)	0000000000000000h
1D8h	8	Variable-Range MTRR Format Physical Mask 5 (MTRR_PHYSMASK5_REG_0_0_0_VTDBAR)	0000000000000000h
1E0h	8	Variable-Range MTRR Format Physical Base 6 (MTRR_PHYSBASE6_REG_0_0_0_VTDBAR)	0000000000000000h
1E8h	8	Variable-Range MTRR Format Physical Mask 6 (MTRR_PHYSMASK6_REG_0_0_0_VTDBAR)	0000000000000000h
1F0h	8	Variable-Range MTRR Format Physical Base 7 (MTRR_PHYSBASE7_REG_0_0_0_VTDBAR)	0000000000000000h
1F8h	8	Variable-Range MTRR Format Physical Mask 7 (MTRR_PHYSMASK7_REG_0_0_0_VTDBAR)	0000000000000000h
200h	8	Variable-Range MTRR Format Physical Base 8 (MTRR_PHYSBASE8_REG_0_0_0_VTDBAR)	0000000000000000h
208h	8	Variable-Range MTRR Format Physical Mask 8 (MTRR_PHYSMASK8_REG_0_0_0_VTDBAR)	0000000000000000h
210h	8	Variable-Range MTRR Format Physical Base 9 (MTRR_PHYSBASE9_REG_0_0_0_VTDBAR)	0000000000000000h
218h	8	Variable-Range MTRR Format Physical Mask 9 (MTRR_PHYSMASK9_REG_0_0_0_VTDBAR)	0000000000000000h
400h	8	Fault Recording Register Low [0] (FRCDL_REG_0_0_0_VTDBAR)	0000000000000000h
408h	8	Fault Recording Register High [0] (FRCDH_REG_0_0_0_VTDBAR)	0000000000000000h
500h	8	Invalidate Address Register (IVA_REG_0_0_0_VTDBAR)	0000000000000000h
508h	8	IOTLB Invalidate Register (IOTLB_REG_0_0_0_VTDBAR)	0200000000000000h

8.1 Version Register (VER_REG_0_0_0_VTDBAR) - Offset 0h

Register to report the architecture version supported. Backward compatibility for the architecture is maintained with new revision numbers, allowing software to load remapping hardware drivers written for prior architecture versions.

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + 0h	00000040h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:4	4h RO	**Major Version Number (MAJOR):** Indicates supported architecture version.
3:0	0h RO	**Minor Version Number (MINOR):** Indicates supported architecture minor version.

8.2 Capability Register (CAP_REG_0_0_0_VTDBAR) - Offset 8h

Register to report general remapping hardware capabilities.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 8h	01C0000C406 60462h

Bit Range	Default & Access	Field Name (ID): Description
63:60	0h RO	**Reserved**
59	0h RO	**Posted Interrupt Support (PI):** • 0 = Hardware does not support Posting of Interrupts. • 1 = Hardware supports Posting of Interrupts. Hardware implementations reporting this field as Set must also report Interrupt Remapping support (IR field in Extended Capability Register)
58:57	0h RO	**Reserved**
56	1h RO	**First Level 1-GByte Page Support (FL1GP):** A value of 1 in this field indicates 1-GByte page size is supported for first-level translation.
55	1h RO	**Read Draining (DRD):** • 0 = Hardware does not support draining of DMA read requests. • 1 = Hardware supports draining of DMA read requests.

Bit Range	Default & Access	Field Name (ID): Description
54	1h RO	**Write Draining (DWD):** • 0 = Hardware does not support draining of DMA write requests. • 1 = Hardware supports draining of DMA write requests.
53:48	0h RO	**Maximum Address Mask Value (MAMV):** The value in this field indicates the maximum supported value for the Address Mask (AM) field in the Invalidation Address register (IVA_REG) and IOTLB Invalidation Descriptor (iotlb_inv_dsc) used for invalidations of second-level translation. This field is valid only when the PSI field in Capability register is reported as Set.
47:40	0h RO	**Number of Fault-Recording Registers (NFR):** Number of fault recording registers is computed as N+1, where N is the value reported in this field. Implementations must support at least one fault recording register (NFR = 0) for each remapping hardware unit in the platform. The maximum number of fault recording registers per remapping hardware unit is 256.
39	0h RO	**Page Selective Invalidation (PSI):** • 0 = Hardware supports only domain and global invalidates for IOTLB. • 1 = Hardware supports page selective, domain and global invalidates for IOTLB. Hardware implementations reporting this field as set are recommended to support a Maximum Address Mask Value (MAMV) value of at least 9 (or 18 if supporting 1GB pages with second level translation).
38	0h RO	**Reserved**
37:34	3h RO	**Second Level Large Page Support (SLLPS):** This field indicates the super page sizes supported by hardware. A value of 1 in any of these bits indicates the corresponding super-page size is supported. The super-page sizes corresponding to various bit positions within this field are: • 0 = 21-bit offset to page frame (2MB) • 1 = 30-bit offset to page frame (1GB) • 2 = 39-bit offset to page frame (512GB) • 3 = 48-bit offset to page frame (1TB) Hardware implementations supporting a specific super-page size must support all smaller super-page sizes, i.e. only valid values for this field are 0000b, 0001b, 0011b, 0111b, 1111b.
33:24	40h RO	**Fault-Recording Register Offset (FRO):** This field specifies the location to the first fault recording register relative to the register base address of this remapping hardware unit. If the register base address is X, and the value reported in this field is Y, the address for the first fault recording register is calculated as X+(16*Y).
23	0h RO	**Reserved**
22	1h RO	**Zero Length Read (ZLR):** • 0 = Indicates the remapping hardware unit blocks (and treats as fault) zero length DMA read requests to write-only pages. • 1 = Indicates the remapping hardware unit supports zero length DMA read requests to write-only pages. DMA remapping hardware implementations are recommended to report ZLR field as Set.

Bit Range	Default & Access	Field Name (ID): Description
21:16	26h RO	**Maximum Guest Address Width (MGAW):** This field indicates the maximum DMA virtual addressability supported by remapping hardware. The Maximum Guest Address Width (MGAW) is computed as (N+1), where N is the value reported in this field. For example, a hardware implementation supporting 48-bit MGAW reports a value of 47 (101111b) in this field. If the value in this field is X, untranslated and translated DMA requests to addresses above 2(x+1)-1 are always blocked by hardware. Translations request to address above 2(x+1)-1 from allowed devices return a null Translation Completion Data Entry with R=W=0. Guest addressability for a given DMA request is limited to the minimum of the value reported through this field and the adjusted guest address width of the corresponding page-table structure. (Adjusted guest address widths supported by hardware are reported through the SAGAW field). Implementations are recommended to support MGAW at least equal to the physical addressability (host address width) of the platform.
15:13	0h RO	**Reserved**
12:8	4h RO	**Supported Adjusted Guest Address Widths (SAGAW):** This 5-bit field indicates the supported adjusted guest address widths (which in turn represents the levels of page-table walks for the 4KB base page size) supported by the hardware implementation. A value of 1 in any of these bits indicates the corresponding adjusted guest address width is supported. The adjusted guest address widths corresponding to various bit positions within this field are: • 0 = 30-bit AGAW (2-level page table) • 1 = 39-bit AGAW (3-level page table) • 2 = 48-bit AGAW (4-level page table) • 3 = 57-bit AGAW (5-level page table) • 4 = 64-bit AGAW (6-level page table) Software must ensure that the adjusted guest address width used to setup the page tables is one of the supported guest address widths reported in this field.
7	0h RO	**Caching Mode (CM):** • 0 = Not-present and erroneous entries are not cached in any of the remapping caches. Invalidations are not required for modifications to individual not present or invalid entries. However, any modifications that result in decreasing the effective permissions or partial permission increases require invalidations for them to be effective. • 1 = Not-present and erroneous mappings may be cached in the remapping caches. Any software updates to the remapping structures (including updates to not-present or erroneous entries) require explicit invalidation. Hardware implementations of this architecture must support a value of 0 in this field.
6	1h RO	**Protected High-Memory Region (PHMR):** • 0 = Indicates protected high-memory region is not supported. • 1 = Indicates protected high-memory region is supported.
5	1h RO	**Protected Low-Memory Region (PLMR):** • 0 = Indicates protected low-memory region is not supported. • 1 = Indicates protected low-memory region is supported.

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Required Write-Buffer Flushing (RWBF):** • 0 = Indicates no write-buffer flushing is needed to ensure changes to memory-resident structures are visible to hardware. • 1 = Indicates software must explicitly flush the write buffers to ensure updates made to memory-resident remapping structures are visible to hardware.
3	0h RO	**Advanced Fault Logging (AFL):** • 0 = Indicates advanced fault logging is not supported. Only primary fault logging is supported. • 1 = Indicates advanced fault logging is supported.
2:0	2h RO	**Number of Domains Supported (ND):** • 000b = Hardware supports 4-bit domain-ids with support for up to 16 domains. • 001b = Hardware supports 6-bit domain-ids with support for up to 64 domains. • 010b = Hardware supports 8-bit domain-ids with support for up to 256 domains. • 011b = Hardware supports 10-bit domain-ids with support for up to 1024 domains. • 100b = Hardware supports 12-bit domain-ids with support for up to 4K domains. • 100b = Hardware supports 14-bit domain-ids with support for up to 16K domains. • 110b = Hardware supports 16-bit domain-ids with support for up to 64K domains. • 111b = Reserved.

8.3 Extended Capability Register (ECAP_REG_0_0_0_VTDBAR) - Offset 10h

Register to report remapping hardware extended capabilities.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 10h	0000049E2FF0505Eh

Bit Range	Default & Access	Field Name (ID): Description
63:43	0h RO	**Reserved**
42	1h RO	**Page Request Draining Support (PDS):** • 0 = Hardware does not support Page-Request Drain (PD) flag in Inv_wait_dsc. • 1 = Hardware supports Page-Request Drain (PD) flag in Inv_wait_dsc. This field is valid only when Device-TLB support field is reported as Set.
41	0h RO	**Reserved**
40	0h RO	**Process Address Space ID Support (PASID):** • 0 = Hardware does not support requests tagged with Process Address Space IDs. • 1 = Hardware supports requests tagged with Process Address Space IDs.
39:35	13h RO	**PASID Size Supported (PSS):** This field reports the PASID size supported by the remapping hardware for requests-with-PASID. A value of N in this field indicates hardware supports PASID field of N+1 bits (For example, value of 7 in this field, indicates 8-bit PASIDs are supported). Requests-with-PASID with PASID value beyond the limit specified by this field are treated as error by the remapping hardware. This field is valid only when PASID field is reported as Set.

Bit Range	Default & Access	Field Name (ID): Description
34	1h RO	**Extended Accessed Flag Support (EAFS):** • 0 = Hardware does not support the extended-accessed (EA) bit in first-level paging-structure entries. • 1 = Hardware supports the extended accessed (EA) bit in first-level paging-structure entries. This field is valid only when PASID field is reported as Set.
33	1h RO	**No Write Flag Support (NWFS):** • 0 = Hardware ignores the No Write (NW) flag in Device-TLB translation requests, and behaves as if NW is always 0. • 1 = Hardware supports the No Write (NW) flag in Device-TLB translation requests. This field is valid only when Device-TLB support (DT) field is reported as Set.
32	0h RO	**Reserved**
31	0h RO	**Supervisor Request Support (SRS):** • 0 = H/W does not support requests-with-PASID seeking supervisor privilege. • 1 = H/W supports requests-with-PASID seeking supervisor privilege. The field is valid only when PASID field is reported as Set.
30	0h RO	**Execute Request Support (ERS):** • 0 = H/W does not support requests-with-PASID seeking execute permission. • 1 = H/W supports requests-with-PASID seeking execute permission. This field is valid only when PASID field is reported as Set.
29	1h RO	**Page Request Support (PRS):** • 0 = Hardware does not support Page Requests. • 1 = Hardware supports Page Requests This field is valid only when Device-TLB (DT) field is reported as Set.
28	0h RO	**IGN:** Ignore this field
27	1h RO	**Deferred Invalidate Support (DIS):** • 0 = Hardware does not support deferred invalidations of IOTLB and Device-TLB. • 1 = Hardware supports deferred invalidations of IOTLB and Device-TLB. This field is valid only when PASID field is reported as Set.
26	1h RO	**Nested Translation Support (NEST):** • 0 = Hardware does not support nested translations. • 1 = Hardware supports nested translations. This field is valid only when PASID field is reported as Set.
25	1h RO	**Memory Type Support (MTS):** • 0 = Hardware does not support Memory Type in first-level translation and Extended Memory type in second-level translation. • 1 = Hardware supports Memory Type in first-level translation and Extended Memory type in second-level translation. This field is valid only when PASID and ECS fields are reported as Set. Remapping hardware units with, one or more devices that operate in processor coherency domain, under its scope must report this field as Set.
24	1h RO	**Extended Context Support (ECS):** • 0 = Hardware does not support extended-root-entries and extended-context-entries. • 1 = Hardware supports extended-root-entries and extended-context-entries. Implementations reporting PASID or PRS fields as Set, must report this field as Set.

Bit Range	Default & Access	Field Name (ID): Description
23:20	Fh RO	**Maximum Handle Mask Value (MHMV):** The value in this field indicates the maximum supported value for the Handle Mask (HM) field in the interrupt entry cache invalidation descriptor (iec_inv_dsc). This field is valid only when the IR field in Extended Capability register is reported as Set.
19:18	0h RO	**Reserved**
17:8	50h RO	**IOTLB Register Offset (IRO):** This field specifies the offset to the IOTLB registers relative to the register base address of this remapping hardware unit. If the register base address is X, and the value reported in this field is Y, the address for the first IOTLB invalidation register is calculated as X+(16*Y).
7	0h RO	**Snoop Control (SC):** • 0 = Hardware does not support 1-setting of the SNP field in the page-table entries. • 1 = Hardware supports the 1-setting of the SNP field in the page-table entries.
6	1h RO	**Pass Through (PT):** • 0 = Hardware does not support pass-through translation type in context entries and extended-context-entries. • 1 = Hardware supports pass-through translation type in context entries and extended-context-entries. Pass-through translation is specified through Translation-Type (T) field value of 10b in context-entries, or T field value of 010b in extended-context-entries. Hardware implementations supporting PASID must report a value of 1b in this field.
5	0h RO	**Reserved**
4	1h RO	**Extended Interrupt Mode (EIM):** • 0 = On Intel® 64 platforms, hardware supports only 8-bit APIC-IDs (xAPIC mode). • 1 = On Intel®64 platforms, hardware supports 32-bit APIC-IDs (x2APIC mode). This field is valid only on Intel®64 platforms reporting Interrupt Remapping support (IR field Set).
3	1h RO	**Interrupt Remapping Support (IR):** • 0 = Hardware does not support interrupt remapping. • 1 = Hardware supports interrupt remapping. Implementations reporting this field as Set must also support Queued Invalidation (QI).
2	1h RO	**Device-TLB Support (DT):** • 0 = Hardware does not support device-IOTLBs. • 1 = Hardware supports Device-IOTLBs. Implementations reporting this field as Set must also support Queued Invalidation (QI). Hardware implementations supporting I/O Page Requests (PRS field Set in Extended Capability register) must report a value of 1b in this field.
1	1h RO	**Queued Invalidation Support (QI):** • 0 = Hardware does not support queued invalidations. • 1 = Hardware supports queued invalidations.
0	0h RO	**Page-Walk Coherency (C):** This field indicates if hardware access to the root, context, extended-context and interrupt-remap tables, and second-level paging structures for requests-without-PASID, are coherent (snooped) or not. • 0 = Indicates hardware accesses to remapping structures are non-coherent. • 1 = Indicates hardware accesses to remapping structures are coherent. Hardware access to advanced fault log, invalidation queue, invalidation semaphore, page-request queue, PASID-table, PASID-state table, and first-level page-tables are always coherent.

8.4 Global Command Register (GCMD_REG_0_0_0_VTDBAR) - Offset 18h

Register to control remapping hardware. If multiple control fields in this register need to be modified, software must serialize the modifications through multiple writes to this register.

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + 18h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Translation Enable (TE):** Software writes to this field to request hardware to enable/disable DMA-remapping: • 0 = Disable DMA remapping. • 1 = Enable DMA remapping. Hardware reports the status of the translation enable operation through the TES field in the Global Status register. There may be active DMA requests in the platform when software updates this field. Hardware must enable or disable remapping logic only at deterministic transaction boundaries, so that any in-flight transaction is either subject to remapping or not at all. Hardware implementations supporting DMA draining must drain any in-flight DMA read/write requests queued within the Root-Complex before completing the translation enable command and reflecting the status of the command through the TES field in the Global Status register. The value returned on a read of this field is undefined.
30	0h WO	**Set Root Table Pointer (SRTP):** Software sets this field to set/update the root-entry table pointer used by hardware. The root-entry table pointer is specified through the Root-entry Table Address (RTA_REG) register. Hardware reports the status of the Set Root Table Pointer operation through the RTPS field in the Global Status register. The Set Root Table Pointer operation must be performed before enabling or re-enabling (after disabling) DMA remapping through the TE field. After a Set Root Table Pointer operation, software must globally invalidate the context cache and then globally invalidate of IOTLB. This is required to ensure hardware uses only the remapping structures referenced by the new root table pointer, and not stale cached entries. While DMA remapping hardware is active, software may update the root table pointer through this field. However, to ensure valid in-flight DMA requests are deterministically remapped, software must ensure that the structures referenced by the new root table pointer are programmed to provide the same remapping results as the structures referenced by the previous root-table pointer. Clearing this bit has no effect. The value returned on read of this field is undefined.
29	0h RO	**Set Fault Log (SFL):** This field is valid only for implementations supporting advanced fault logging. Software sets this field to request hardware to set/update the fault-log pointer used by hardware. The fault-log pointer is specified through Advanced Fault Log register. Hardware reports the status of the Set Fault Log operation through the FLS field in the Global Status register. The fault log pointer must be set before enabling advanced fault logging (through EAFL field). Once advanced fault logging is enabled, the fault log pointer may be updated through this field while DMA remapping is active. Clearing this bit has no effect. The value returned on read of this field is undefined.

Bit Range	Default & Access	Field Name (ID): Description
28	0h RO	**Enable Advanced Fault Logging (EAFL):** This field is valid only for implementations supporting advanced fault logging. Software writes to this field to request hardware to enable or disable advanced fault logging: • 0 = Disable advanced fault logging. In this case, translation faults are reported through the Fault Recording registers. • 1 = Enable use of memory-resident fault log. When enabled, translation faults are recorded in the memory-resident log. The fault log pointer must be set in hardware (through the SFL field) before enabling advanced fault logging. Hardware reports the status of the advanced fault logging enable operation through the AFLS field in the Global Status register. The value returned on read of this field is undefined.
27	0h RO	**Write Buffer Flush (WBF):** This bit is valid only for implementations requiring write buffer flushing. Software sets this field to request that hardware flush the Root-Complex internal write buffers. This is done to ensure any updates to the memory-resident remapping structures are not held in any internal write posting buffers. Hardware reports the status of the write buffer flushing operation through the WBFS field in the Global Status register. Clearing this bit has no effect. The value returned on a read of this field is undefined.
26	0h RW	**Queued Invalidation Enable (QIE):** This field is valid only for implementations supporting queued invalidations. Software writes to this field to enable or disable queued invalidations. • 0 = Disable queued invalidations. • 1 = Enable use of queued invalidations. Hardware reports the status of queued invalidation enable operation through QIES field in the Global Status register. The value returned on a read of this field is undefined.
25	0h RW	**Interrupt Remapping Enable (IRE):** This field is valid only for implementations supporting interrupt remapping. • 0 = Disable interrupt-remapping hardware. • 1 = Enable interrupt-remapping hardware. Hardware reports the status of the interrupt remapping enable operation through the IRES field in the Global Status register. There may be active interrupt requests in the platform when software updates this field. Hardware must enable or disable interrupt-remapping logic only at deterministic transaction boundaries, so that any in-flight interrupts are either subject to remapping or not at all. Hardware implementations must drain any in-flight interrupts requests queued in the Root-Complex before completing the interrupt-remapping enable command and reflecting the status of the command through the IRES field in the Global Status register. The value returned on a read of this field is undefined.

Bit Range	Default & Access	Field Name (ID): Description
24	0h WO	**Set Interrupt Remap Table Pointer (SIRTP):** This field is valid only for implementations supporting interrupt-remapping. Software sets this field to set/update the interrupt remapping table pointer used by hardware. The interrupt remapping table pointer is specified through the Interrupt Remapping Table Address (IRTA_REG) register. Hardware reports the status of the Set Interrupt Remap Table Pointer operation through the IRTPS field in the Global Status register. The Set Interrupt Remap Table Pointer operation must be performed before enabling or re-enabling (after disabling) interrupt-remapping hardware through the IRE field. After a Set Interrupt Remap Table Pointer operation, software must globally invalidate the interrupt entry cache. This is required to ensure hardware uses only the interrupt-remapping entries referenced by the new interrupt remap table pointer, and not any stale cached entries. While interrupt remapping is active, software may update the interrupt remapping table pointer through this field. However, to ensure valid in-flight interrupt requests are deterministically remapped, software must ensure that the structures referenced by the new interrupt remap table pointer are programmed to provide the same remapping results as the structures referenced by the previous interrupt remap table pointer. Clearing this bit has no effect. The value returned on a read of this field is undefined.
23	0h RW	**Compatibility Format Interrupt (CFI):** This field is valid only for Intel®64 implementations supporting interrupt-remapping. Software writes to this field to enable or disable Compatibility Format interrupts on Intel®64 platforms. The value in this field is effective only when interrupt-remapping is enabled and Extended Interrupt Mode (x2APIC mode) is not enabled. • 0 = Block Compatibility format interrupts. • 1 = Process Compatibility format interrupts as pass-through (bypass interrupt remapping). Hardware reports the status of updating this field through the CFIS field in the Global Status register. The value returned on a read of this field is undefined.
22:0	0h RO	**Reserved**

8.5 Global Status Register (GSTS_REG_0_0_0_VTDBAR) - Offset 1Ch

Register to report general remapping hardware status.

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + 1Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO/V	**Translation Enable Status (TES):** This field indicates the status of DMA-remapping hardware. • 0 = DMA-remapping hardware is not enabled. • 1 = DMA-remapping hardware is enabled
30	0h RO/V	**Root Table Pointer Status (RTPS):** This field indicates the status of the root- table pointer in hardware. This field is cleared by hardware when software sets the SRTP field in the Global Command register. This field is set by hardware when hardware completes the Set Root Table Pointer operation using the value provided in the Root-Entry Table Address register.
29	0h RO	**Fault Log Status (FLS):** This field: • Is cleared by hardware when software Sets the SFL field in the Global Command register. • Is Set by hardware when hardware completes the Set Fault Log Pointer operation using the value provided in the Advanced Fault Log register.
28	0h RO	**Advanced Fault Logging Status (AFLS):** This field is valid only for implementations supporting advanced fault logging. It indicates the advanced fault logging status: • 0 = Advanced Fault Logging is not enabled. • 1 = Advanced Fault Logging is enabled.
27	0h RO	**Write Buffer Flush Status (WBFS):** This field is valid only for implementations requiring write buffer flushing. This field indicates the status of the write buffer flush command. It is: • Set by hardware when software sets the WBF field in the Global Command register. • Cleared by hardware when hardware completes the write buffer flushing operation.
26	0h RO/V	**Queued Invalidation Enable Status (QIES):** This field indicates queued invalidation enable status. • 0 = queued invalidation is not enabled. • 1 = queued invalidation is enabled
25	0h RO/V	**Interrupt Remapping Enable Status (IRES):** This field indicates the status of Interrupt-remapping hardware. • 0 = Interrupt-remapping hardware is not enabled. • 1 = Interrupt-remapping hardware is enabled
24	0h RO/V	**Interrupt Remapping Pointer Status (IRTPS):** This field indicates the status of the interrupt remapping table pointer in hardware. This field is cleared by hardware when software sets the SIRTP field in the Global Command register. This field is Set by hardware when hardware completes the set interrupt remap table pointer operation using the value provided in the Interrupt Remapping Table Address register.
23	0h RO/V	**Compatibility Format Interrupt Status (CFIS):** This field indicates the status of Compatibility format interrupts on Intel®64 implementations supporting interrupt-remapping. The value reported in this field is applicable only when interrupt-remapping is enabled and Extended Interrupt Mode (x2APIC mode) is not enabled. • 0 = Compatibility format interrupts are blocked. • 1 = Compatibility format interrupts are processed as pass-through (bypassing interrupt remapping).
22:0	0h RO	**Reserved**

8.6 Root Table Address Register (RTADDR_REG_0_0_0_VTDBAR) - Offset 20h

Register providing the base address of root-entry table.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 20h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:52	0h RO	**Reserved**
51:12	0h RW	**Root Table Address (RTA):** This register points to base of page aligned, 4KB-sized root-entry table in system memory. Hardware ignores and not implements bits 63:HAW, where HAW is the host address width. Software specifies the base address of the root-entry table through this register, and programs it in hardware through the SRTP field in the Global Command register. Reads of this register returns value that was last programmed to it.
11	0h RW	**Root Table Type (RTT):** This field specifies the type of root-table referenced by the Root Table Address (RTA) field: • 0 = Root Table. • 1 = Extended Root Table
10:0	0h RO	**Reserved**

8.7 Context Command Register (CCMD_REG_0_0_0_VTDBAR) - Offset 28h

Register to manage context cache. The act of writing the uppermost byte of the CCMD_REG with the ICC field Set causes the hardware to perform the context-cache invalidation.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 28h	0800000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/V	**Invalidate Context Cache (ICC):** Software requests invalidation of context-cache by setting this field. Software must also set the requested invalidation granularity by programming the CIRG field. Software must read back and check the ICC field is Clear to confirm the invalidation is complete. Software must not update this register when this field is set. Hardware clears the ICC field to indicate the invalidation request is complete. Hardware also indicates the granularity at which the invalidation operation was performed through the CAIG field. Software must submit a context-cache invalidation request through this field only when there are no invalidation requests pending at this remapping hardware unit. Since information from the context-cache may be used by hardware to tag IOTLB entries, software must perform domain-selective (or global) invalidation of IOTLB after the context cache invalidation has completed. Hardware implementations reporting write-buffer flushing requirement (RWBF=1 in Capability register) must implicitly perform a write buffer flush before invalidating the context cache.
62:61	0h RW	**Context Invalidation Request Granularity (CIRG):** Software provides the requested invalidation granularity through this field when setting the ICC field: • 00: Reserved. • 01: Global Invalidation request. • 10: Domain-selective invalidation request. The target domain-id must be specified in the DID field. • 11: Device-selective invalidation request. The target source-id(s) must be specified through the SID and FM fields, and the domain-id (that was programmed in the context-entry for these device(s)) must be provided in the DID field. Hardware implementations may process an invalidation request by performing invalidation at a coarser granularity than requested. Hardware indicates completion of the invalidation request by clearing the ICC field. At this time, hardware also indicates the granularity at which the actual invalidation was performed through the CAIG field.
60:59	1h RO/V	**Context Actual Invalidation Granularity (CAIG):** Hardware reports the granularity at which an invalidation request was processed through the CAIG field at the time of reporting invalidation completion (by clearing the ICC field). The following are the encodings for this field: • 00: Reserved. • 01: Global Invalidation performed. This could be in response to a global, domain-selective or device-selective invalidation request. • 10: Domain-selective invalidation performed using the domain-id specified by software in the DID field. This could be in response to a domain-selective or device-selective invalidation request. • 11: Device-selective invalidation performed using the source-id and domain-id specified by software in the SID and FM fields. This can only be in response to a device-selective invalidation request.
58:34	0h RO	**Reserved**

Bit Range	Default & Access	Field Name (ID): Description
33:32	0h RW	**Function Mask (FM):** Software may use the Function Mask to perform device-selective invalidations on behalf of devices supporting PCI Express Phantom Functions. This field specifies which bits of the function number portion (least significant three bits) of the SID field to mask when performing device-selective invalidations. The following encodings are defined for this field: • 00: No bits in the SID field masked. • 01: Mask most significant bit of function number in the SID field. • 10: Mask two most significant bit of function number in the SID field. • 11: Mask all three bits of function number in the SID field. The context-entries corresponding to all the source-ids specified through the FM and SID fields must have to the domain-id specified in the DID field.
31:16	0h RW	**SID:** Indicates the source-id of the device whose corresponding context-entry needs to be selectively invalidated. This field along with the FM field must be programmed by software for device-selective invalidation requests.
15:0	0h RW	**DID:** Indicates the id of the domain whose context-entries need to be selectively invalidated. This field must be programmed by software for both domain-selective and device-selective invalidation requests. The Capability register reports the domain-id width supported by hardware. Software must ensure that the value written to this field is within this limit. Hardware may ignore and not implement bits15:N, where N is the supported domain-id width reported in the Capability register.

8.8 Fault Status Register (FSTS_REG_0_0_0_VTDBAR) - Offset 34h

Register indicating the various error statuses.

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + 34h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:8	0h RO	**Fault Record Index (FRI):** This field is valid only when the PPF field is Set. The FRI field indicates the index (from base) of the fault recording register to which the first pending fault was recorded when the PPF field was Set by hardware. The value read from this field is undefined when the PPF field is clear.
7	0h RW/1C	**Page Request Overflow (PRO):** Hardware detected a Page Request Overflow error. Hardware implementations not supporting the Page Request Queue implement this bit as RsvdZ.
6	0h RW/1C	**Invalidation Time-out Error (ITE):** Hardware detected a Device-IOTLB invalidation completion time-out. At this time, a fault event may be generated based on the programming of the Fault Event Control register. Hardware implementations not supporting device Device-IOTLBs implement this bit as RsvdZ.

Bit Range	Default & Access	Field Name (ID): Description
5	0h RW/1C	**Invalidation Completion Error (ICE):** Hardware received an unexpected or invalid Device-IOTLB invalidation completion. This could be due to either an invalid ITag or invalid source-id in an invalidation completion response. At this time, a fault event may be generated based on the programming of the Fault Event Control register. Hardware implementations not supporting Device-IOTLBs implement this bit as RsvdZ.
4	0h RW/1C	**Invalidation Queue Error (IQE):** Hardware detected an error associated with the invalidation queue. This could be due to either a hardware error while fetching a descriptor from the invalidation queue, or hardware detecting an erroneous or invalid descriptor in the invalidation queue. At this time, a fault event may be generated based on the programming of the Fault Event Control register. Hardware implementations not supporting queued invalidations implement this bit as RsvdZ.
3	0h RO	**Advanced Pending Fault (APF):** When this field is Clear, hardware sets this field when the first fault record (at index 0) is written to a fault log. At this time, a fault event is generated based on the programming of the Fault Event Control register. Software writing 1 to this field clears it. Hardware implementations not supporting advanced fault logging implement this bit as RsvdZ.
2	0h RO	**Advanced Fault Overflow (AFO):** Hardware sets this field to indicate advanced fault log overflow condition. At this time, a fault event is generated based on the programming of the Fault Event Control register. Software writing 1 to this field clears it. Hardware implementations not supporting advanced fault logging implement this bit as RsvdZ.
1	0h RO/V	**Primary Pending Fault (PPF):** This field indicates if there are one or more pending faults logged in the fault recording registers. Hardware computes this field as the logical OR of Fault (F) fields across all the fault recording registers of this remapping hardware unit. • 0 = No pending faults in any of the fault recording registers. • 1 = One or more fault recording registers has pending faults. The FRI field is updated by hardware whenever the PPF field is set by hardware. Also, depending on the programming of Fault Event Control register, a fault event is generated when hardware sets this field.
0	0h RW/1C	**Primary Fault Overflow (PFO):** Hardware sets this field to indicate overflow of fault recording registers. Software writing 1 clears this field. When this field is Set, hardware does not record any new faults until software clears this field.

8.9 Fault Event Control Register (FECTL_REG_0_0_0_VTDBAR) - Offset 38h

Register specifying the fault event interrupt message control bits.

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + 38h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Interrupt Mask (IM):** • 0 = No masking of interrupt. When an interrupt condition is detected, hardware issues an interrupt message (using the Fault Event Data and Fault Event Address register values). • 1 = This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is set.
30	0h RO/V	**Interrupt Pending (IP):** Hardware sets the IP field whenever it detects an interrupt condition, which is defined as: • When primary fault logging is active, an interrupt condition occurs when hardware records a fault through one of the Fault Recording registers and sets the PPF field in Fault Status register. • When advanced fault logging is active, an interrupt condition occurs when hardware records a fault in the first fault record (at index 0) of the current fault log and sets the APF field in the Fault Status register. • Hardware detected error associated with the Invalidation Queue, setting the IQE field in the Fault Status register. • Hardware detected invalid Device-IOTLB invalidation completion, setting the ICE field in the Fault Status register. • Hardware detected Device-IOTLB invalidation completion time-out, setting the ITE field in the Fault Status register. If any of the status fields in the Fault Status register were already Set at the time of setting any of these fields, it is not treated as a new interrupt condition. The IP field is kept set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set or other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending, or due to software clearing the IM field. • Software servicing all the pending interrupt status fields in the Fault Status register as follows: - When primary fault logging is active, software clearing the Fault (F) field in all the Fault Recording registers with faults, causing the PPF field in Fault Status register to be evaluated as clear. - Software clearing other status fields in the Fault Status register by writing back the value read from the respective fields.
29:0	0h RO	**Reserved**

8.10 Fault Event Data Register (FEDATA_REG_0_0_0_VTDBAR) - Offset 3Ch

Register specifying the interrupt message data

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + 3Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Extended Interrupt Message Data (EIMD):** This field is valid only for implementations supporting 32-bit interrupt data fields. Hardware implementations supporting only 16-bit interrupt data may treat this field as RsvdZ.
15:0	0h RW	**Interrupt Message Data (IMD):** Data value in the interrupt request.

8.11 Fault Event Address Register (FEADDR_REG_0_0_0_VTDBAR) - Offset 40h

Register specifying the interrupt message address.

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + 40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Message Address (MA):** When fault events are enabled, the contents of this register specify the DWORD-aligned address (bits 31:2) for the interrupt request.
1:0	0h RO	**Reserved**

8.12 Fault Event Upper Address Register (FEUADDR_REG_0_0_0_VTDBAR) - Offset 44h

Register specifying the interrupt message upper address.

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + 44h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Message Upper Address (MUA):** Hardware implementations supporting Extended Interrupt Mode are required to implement this register.Hardware implementations not supporting Extended Interrupt Mode may treat this field as RsvdZ.

8.13 Advanced Fault Log Register (AFLOG_REG_0_0_0_VTDBAR) - Offset 58h

Register to specify the base address of the memory-resident fault-log region. This register is treated as RsvdZ for implementations not supporting advanced translation fault logging (AFL field reported as 0 in the Capability register).

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 58h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:12	0h RO	**Fault Log Address (FLA):** This field specifies the base of 4KB aligned fault-log region in system memory. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width. Software specifies the base address and size of the fault log region through this register, and programs it in hardware through the SFL field in the Global Command register. When implemented, reads of this field return the value that was last programmed to it.
11:9	0h RO	**Fault Log Size (FLS):** This field specifies the size of the fault log region pointed by the FLA field. The size of the fault log region is 2X * 4KB, where X is the value programmed in this register. When implemented, reads of this field return the value that was last programmed to it.
8:0	0h RO	**Reserved**

8.14 Protected Memory Enable Register (PMEN_REG_0_0_0_VTDBAR) - Offset 64h

Register to enable the DMA-protected memory regions setup through the PLMBASE,..., PLMLIMT, PHMBASE, PHMLIMIT registers. This register is always treated as RO for implementations not supporting protected memory regions (PLMR and PHMR fields reported as Clear in the Capability register).Protected memory regions may be used by software to securely initialize remapping structures in memory. To avoid impact to legacy BIOS usage of memory, software is recommended to not overlap protected memory regions with any reserved memory regions of the platform reported through the Reserved Memory Region Reporting (RMRR) structures.

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + 64h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RW	**Enable Protected Memory (EPM):** This field controls DMA accesses to the protected low-memory and protected high-memory regions. • 0 = Protected memory regions are disabled. • 1 = Protected memory regions are enabled. DMA requests accessing protected memory regions are handled as follows: - When DMA remapping is not enabled, all DMA requests accessing protected memory regions are blocked. - When DMA remapping is enabled: • DMA requests processed as pass-through (Translation Type value of 10b in Context-Entry) and accessing the protected memory regions are blocked. • DMA requests with translated address (AT=10b) and accessing the protected memory regions are blocked. • DMA requests that are subject to address remapping, and accessing the protected memory regions may or may not be blocked by hardware. For such requests, software must not depend on hardware protection of the protected memory regions, and instead program the DMA-remapping page-tables to not allow DMA to protected memory regions. Remapping hardware access to the remapping structures are not subject to protected memory region checks. DMA requests blocked due to protected memory region violation are not recorded or reported as remapping faults. Hardware reports the status of the protected memory enable/disable operation through the PRS field in this register.Hardware implementations supporting DMA draining must drain any in-flight translated DMA requests queued within the Root-Complex before indicating the protected memory region as enabled through the PRS field.
30:1	0h RO	**Reserved**
0	0h RO/V	**Protected Region Status (PRS):** This field indicates the status of protected memory region(s): • 0 = Protected memory region(s) disabled. • 1 = Protected memory region(s) enabled.

8.15 Protected Low Memory Base Register (PLMBASE_REG_0_0_0_VTDBAR) - Offset 68h

Register to set up the base address of DMA-protected low-memory region below 4GB. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled. This register is always treated as RO for implementations not supporting protected low memory region (PLMR field reported as Clear in the Capability register).The alignment of the protected low memory region base depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding the most significant zero bit position with 0 in the value read back from the register. Bits N:0 of this register is decoded by hardware as all 0s...Software must setup the protected low memory region below 4GB.Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + 68h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Protected Low-Memory Base (PLMB):** This register specifies the base of protected low-memory region in system memory.
19:0	0h RO	**Reserved**

8.16 Protected Low-Memory Limit Register (PLMLIMIT_REG_0_0_0_VTDBAR) - Offset 6Ch

Register to set up the limit address of DMA-protected low-memory region below 4GB. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled. This register is always treated as RO for implementations not supporting protected low memory region (PLMR field reported as Clear in the Capability register) The alignment of the protected low memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine N by writing all 1s to this register, and finding most significant zero bit position with 0 in the value read back from the register. Bits N:0 of the limit register is decoded by hardware as all 1sThe Protected low-memory base and limit registers functions as follows:

- Programming the protected low-memory base and limit registers with the same value in bits 31: (N+1) specifies a protected low-memory region of size 2(N+1) bytes
- Programming the protected low-memory limit register with a value less than the protected low-memory base register disables the protected low-memory region

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + 6Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:20	0h RW	**Protected Low-Memory Limit (PLML):** This register specifies the last host physical address of the DMA-protected low-memory region in system memory.
19:0	0h RO	**Reserved**

8.17 Protected High-Memory Base Register (PHMBASE_REG_0_0_0_VTDBAR) - Offset 70h

Register to set up the base address of DMA-protected high-memory region. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled. This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as Clear in the Capability register) The alignment of the protected high memory region base depends on the number of reserved bits (N:0) of

this register. Software may determine N by writing all 1s to this register, and finding most significant zero bit position below host address width (HAW) in the value read back from the register. Bits N:0 of this register are decoded by hardware as all 0sSoftware may setup the protected high memory region either above or below 4GBSoftware must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 70h	00000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:20	0h RW	**Protected High-Memory Base (PHMB):** This register specifies the base of protected (high) memory region in system memory Hardware ignores, and does not implement, bits 63:HAW, where HAW is the host address width.
19:0	0h RO	**Reserved**

8.18 Protected High-Memory Limit Register (PHMLIMIT_REG_0_0_0_VTDBAR) - Offset 78h

Register to set up the limit address of DMA-protected high-memory region. This register must be set up before enabling protected memory through PMEN_REG, and must not be updated when protected memory regions are enabled. This register is always treated as RO for implementations not supporting protected high memory region (PHMR field reported as Clear in the Capability register). The alignment of the protected high memory region limit depends on the number of reserved bits (N:0) of this register. Software may determine the value of N by writing all 1s to this register, and finding most significant zero bit position below host address width (HAW) in the value read back from the register. Bits N:0 of the limit register is decoded by hardware as all 1sThe protected high-memory base & limit registers functions as follows:

- Programming the protected low-memory base and limit registers with the same value in bits HAW:(N+1) specifies a protected low-memory region of size 2(N+1) bytes
- Programming the protected high-memory limit register with a value less than the protected high-memory base register disables the protected high-memory region

Software must not modify this register when protected memory regions are enabled (PRS field Set in PMEN_REG).

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 78h	00000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:20	0h RW	**Protected High-Memory Limit (PHML):** This register specifies the last host physical address of the DMA-protected high-memory region in system memory Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width.
19:0	0h RO	**Reserved**

8.19 Invalidation Queue Head Register (IQH_REG_0_0_0_VTDBAR) - Offset 80h

Register indicating the invalidation queue head. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 80h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0h RO/V	**Queue Head (QH):** Specifies the offset (128-bit aligned) to the invalidation queue for the command that will be fetched next by hardware. Hardware resets this field to 0 whenever the queued invalidation is disabled (QIES field Clear in the Global Status register).
3:0	0h RO	**Reserved**

8.20 Invalidation Queue Tail Register (IQT_REG_0_0_0_VTDBAR) - Offset 88h

Register indicating the invalidation tail head. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 88h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0h RW	**Queue Tail (QT):** Specifies the offset (128-bit aligned) to the invalidation queue for the command that will be written next by software.
3:0	0h RO	**Reserved**

8.21 Invalidation Queue Address Register (IQA_REG_0_0_0_VTDBAR) - Offset 90h

Register to configure the base address and size of the invalidation queue. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 90h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RW	**Invalidation Queue Base Address (IQA):** This field points to the base of 4KB aligned invalidation request queue. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width. Reads of this field return the value that was last programmed to it.
11:3	0h RO	**Reserved**
2:0	0h RW	**Queue Size (QS):** This field specifies the size of the invalidation request queue. A value of X in this field indicates an invalidation request queue of (2^X) 4KB pages. The number of entries in the invalidation queue is 2^(X + 8).

8.22 Invalidation Completion Status Register (ICS_REG_0_0_0_VTDBAR) - Offset 9Ch

Register to report completion status of invalidation wait descriptor with Interrupt Flag (IF) Set This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + 9Ch	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/1C	**Invalidation Wait Descriptor Complete (IWC):** Indicates completion of Invalidation Wait Descriptor with Interrupt Flag (IF) field Set. Hardware implementations not supporting queued invalidations implement this field as RsvdZ.

8.23 Invalidation Event Control Register (IECTL_REG_0_0_0_VTDBAR) - Offset A0h

Register specifying the invalidation event interrupt control bits. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + A0h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Interrupt Mask (IM):** • 0= No masking of interrupt. When an invalidation event condition is detected, hardware issues an interrupt message (using the Invalidation Event Data & Invalidation Event Address register values) • 1= This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is Set.
30	0h RO/V	**Interrupt Pending (IP):** Hardware sets the IP field whenever it detects an interrupt condition. Interrupt condition is defined as: • An Invalidation Wait Descriptor with Interrupt Flag (IF) field Set completed, setting the IWC field in the Invalidation Completion Status register • If the IWC field in the Invalidation Completion Status register was already Set at the time of setting this field, it is not treated as a new interrupt condition The IP field is kept Set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set, or due to other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • 0= Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending or due to software clearing the IM field • 1= Software servicing the IWC field in the Invalidation Completion Status register.
29:0	0h RO	**Reserved**

8.24 Invalidation Event Data Register (IEDATA_REG_0_0_0_VTDBAR) - Offset A4h

Register specifying the Invalidation Event interrupt message data. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + A4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Extended Interrupt Message Data (EIMD):** This field is valid only for implementations supporting 32-bit interrupt data fields. Hardware implementations supporting only 16-bit interrupt data treat this field as Rsvd.
15:0	0h RW	**Interrupt Message Data (IMD):** Data value in the interrupt request.

8.25 Invalidation Event Address Register (IEADDR_REG_0_0_0_VTDBAR) - Offset A8h

Register specifying the Invalidation Event Interrupt message address. This register is treated as RsvdZ by implementations reporting Queued Invalidation (QI) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Message Address (MA):** When fault events are enabled, the contents of this register specify the DWORD-aligned address (bits 31:2) for the interrupt request.
1:0	0h RO	**Reserved**

8.26 Invalidation Event Upper Address Register (IEUADDR_REG_0_0_0_VTDBAR) - Offset ACh

Register specifying the Invalidation Event interrupt message upper address.

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + ACh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Message Upper Address (MUA):** Hardware implementations supporting Queued Invalidations and Extended Interrupt Mode are required to implement this register. Hardware implementations not supporting Queued Invalidations or Extended Interrupt Mode may treat this field as RsvdZ.

8.27 Interrupt Remapping Table Address Register (IRTA_REG_0_0_0_VTDBAR) - Offset B8h

Register providing the base address of Interrupt remapping table. This register is treated as RsvdZ by implementations reporting Interrupt Remapping (IR) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + B8h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:12	0h RW	**Interrupt Remapping Table Address (IRTA):** This field points to the base of 4KB aligned interrupt remapping table. Hardware ignores and does not implement bits 63:HAW, where HAW is the host address width Reads of this field returns value that was last programmed to it.
11	0h RW	**Extended Interrupt Mode Enable (EIME):** This field is used by hardware on Intel®64 platforms as follows: • 0=xAPIC mode is active. Hardware interprets only low 8-bits of Destination-ID field in the IRTEs. The high 24-bits of the Destination-ID field are treated as reserved • 1= x2APIC mode is active. Hardware interprets all 32-bits of Destination-ID field in the IRTEs This field is implemented as RsvdZ on implementations reporting Extended Interrupt Mode (EIM) field as Clear in Extended Capability register.
10:4	0h RO	**Reserved**
3:0	0h RW	**S:** This field specifies the size of the interrupt remapping table. The number of entries in the interrupt remapping table is 2(X+1), where X is the value programmed in this field.

8.28 Page Request Queue Head Register (PQH_REG_0_0_0_VTDBAR) - Offset C0h

Register indicating the page request queue head. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + C0h	00000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0h RW	**Page Queue Head (PQH):** Specifies the offset (16-bytes aligned) to the page request queue for the request that will be processed next by software.
3:0	0h RO	**Reserved**

8.29 Page Request Queue Tail Register (PQT_REG_0_0_0_VTDBAR) - Offset C8h

Register indicating the page request queue tail. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + C8h	00000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:19	0h RO	**Reserved**
18:4	0h RW/V	**Page Queue Tail (PQT):** Specifies the offset (16-bytes aligned) to the page request queue for the request that will be written next by hardware.
3:0	0h RO	**Reserved**

8.30 Page Request Queue Address Register (PQA_REG_0_0_0_VTDBAR) - Offset D0h

Register to configure the base address and size of the page request queue. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + D0h	00000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:46	0h RO	**Reserved**
45:12	0h RW	**Page Request Queue Base Address (PQA):** This field points to the base of 4KB aligned page request queue. Hardware may ignore and not implement bits 63:HAW, where HAW is the host address width. Software must configure this register before enabling page requests in any extended-context-entries.
11:3	0h RO	**Reserved**
2:0	0h RW	**Page Request Queue Size (PQS):** This field specifies the size of the page request queue. A value of X in this field indicates an invalidation request queue of (2^X) 4KB pages. The number of entries in the page request queue is 2^(X + 8)

8.31 Page Request Status Register (PRS_REG_0_0_0_VTDBAR) - Offset DCh

Register to report pending page request in page request queue. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + DCh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:1	0h RO	**Reserved**
0	0h RW/1C	**Pending Page Request (PPR):** Pending Page Request: Indicates pending page requests to be serviced by software in the page request queue. This field is Set by hardware when a streaming page request entry (page_stream_reg_dsc) or a page group request (page_grp_req_dsc) with Last Page in Group (LPG) field Set, is added to the page request queue.

8.32 Page Request Event Control Register (PECTL_REG_0_0_0_VTDBAR) - Offset E0h

Register specifying the page request event interrupt control bits. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + E0h	80000000h

Bit Range	Default & Access	Field Name (ID): Description
31	1h RW	**Interrupt Mask (IM):** Interrupt Mask • 0=No masking of interrupt. When a page request event condition is detected, hardware issues an interrupt message (using the Page Request Event Data and Page Request Event Address register values) • 1=This is the value on reset. Software may mask interrupt message generation by setting this field. Hardware is prohibited from sending the interrupt message when this field is Set.
30	0h RO/V	**Interrupt Pending (IP):** Interrupt Pending: Hardware sets the IP field whenever it detects an interrupt condition. Interrupt condition is defined as: • A streaming page request entry (page_stream_req_dsc) or a page group request (page_grp_req_dsc) with Last Page in Group (LPG) field Set, was added to page request queue, resulting in hardware setting the Pending Page Request (PPR) field in Page Request Status register • If the PPR field in the Page Request Event Status register was already Set at the time of setting this field, it is not treated as a new interrupt condition The IP field is kept Set by hardware while the interrupt message is held pending. The interrupt message could be held pending due to interrupt mask (IM field) being Set, or due to other transient hardware conditions. The IP field is cleared by hardware as soon as the interrupt message pending condition is serviced. This could be due to either: • Hardware issuing the interrupt message due to either change in the transient hardware condition that caused interrupt message to be held pending or due to software clearing the IM field • Software servicing the PPR field in the Page Request Event Status register.
29:0	0h RO	**Reserved**

8.33 Page Request Event Data Register (PEDATA_REG_0_0_0_VTDBAR) - Offset E4h

Register specifying the Page Request Event interrupt message data. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RW	**Extended Interrupt Message Data (EIMD):** Extended Interrupt Message Data
15:0	0h RW	**Interrupt Message Data (IMD):** Interrupt Message Data: Data value in the interrupt request. Software requirements for programming this register are described in VTd Spec

8.34 Page Request Event Address Register (PEADDR_REG_0_0_0_VTDBAR) - Offset E8h

Register specifying the Page Request Event Interrupt message address. This register is treated as RsvdZ by implementations reporting Page Request Support (PRS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + E8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	0h RW	**Message Address (MA):** Message Address: When fault events are enabled, the contents of this register specify the DWORD-aligned address (bits 31:2) for the interrupt request.
1:0	0h RO	**Reserved**

8.35 Page Request Event Upper Address Register (PEUADDR_REG_0_0_0_VTDBAR) - Offset ECh

Register specifying the Page Request Event interrupt message upper address.

Type	Size	Offset	Default
MEM	32 bit	GFXVTBAR + ECh	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:0	0h RW	**Message Upper Address (MUA):** Message Upper Address: This field specifies the upper address (bits... 63:32) for the page request event interrupt.

8.36 MTRR Capability Register (MTRRCAP_0_0_0_VTDBAR) - Offset 100h

Register reporting the Memory Type Range Register Capability. This register is treated as RsvdZ by implementations reporting Memory Type Support (MTS) as not supported in the Extended Capability register. When implemented, value reported in this register must match IA32_MTRRCAP Model Specific Register (MSR) value reported by the host IA-32 processor(s).

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 100h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:11	0h RO	**Reserved**
10	0h RO	**Write Combining (WC):** • 0 = Write-combining (WC) memory type is not supported. • 1 = Write-combining (WC) memory type is supported. Indicates whether the Write Combining memory type is supported.
9	0h RO	**Reserved**
8	0h RO	**Fixed Range MTRRs Supported (FIX):** • 0 = No fixed range MTRRs are supported • 1 = Fixed range MTRRs (MTRR_FIX64K_00000 through MTRR_FIX4K_0F8000) are supported
7:0	0h RO	**Variable MTRR Count (VCNT):** Indicates number of variable range MTRRs are supported.

8.37 MTRR Default Type Register (MTRRDEFAULT_0_0_0_VTDBAR) - Offset 108h

Register for enabling/configuring Memory Type Range Registers. This register is treated as RsvdZ by implementations reporting Memory Type Support (MTS) as not supported in the Extended Capability register.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 108h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:12	0h RO	**Reserved**
11	0h RO	**MTRR Enable (E):** • 0 = Disable MTRRs; UC memory type is applied. FE field has no effect. • 1 = Enable MTRRs. FE field can disable the fixed-range MTRRs. Type specified in the default memory type field is used for areas of memory not already mapped by either fixed or variable MTRR
10	0h RO	**Fixed Range MTRR Enable (FE):** • 0 = Disable fixed range MTRRs. • 1 = Enable fixed range MTRRs. When fixed range MTRRs are enabled, they take priority over the variable range MTRRs when overlaps in ranges occur. If the fixed-range MTRRs are disabled, the variable range MTRRs can still be used and can map the range ordinarily covered by the fixed range MTRRs.
9:8	0h RO	**Reserved**
7:0	0h RO	**Default Memory Type (MEMTYPE):** Indicates default memory type used for physical memory address ranges that do not have a memory type specified for them by an MTRR. Legal values for this field are 0, 1, 4, 5 and 6.

8.38 Fixed-Range MTRR Format 64K-00000 (MTRR_FIX64K_00000_REG_0_0_0_VTDBAR) - Offset 120h

Fixed Range MTRR covering the 64K memory space from 0x00000 - 0x7FFFF.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 120h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RO	**R7:** Register Field 7
55:48	0h RO	**R6:** Register Field 6
47:40	0h RO	**R5:** Register Field 5
39:32	0h RO	**R4:** Register Field 4
31:24	0h RO	**R3:** Register Field 3
23:16	0h RO	**R2:** Register Field 2
15:8	0h RO	**R1:** Register Field 1
7:0	0h RO	**R0:** Register Field 0

8.39 Fixed-Range MTRR Format 16K-80000 (MTRR_FIX16K_80000_REG_0_0_0_VTDBAR) - Offset 128h

Fixed Range MTRR covering the 16K memory space from 0x80000 - 0x9FFFF.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 128h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RO	**R7:** Register Field 7
55:48	0h RO	**R6:** Register Field 6
47:40	0h RO	**R5:** Register Field 5
39:32	0h RO	**R4:** Register Field 4
31:24	0h RO	**R3:** Register Field 3
23:16	0h RO	**R2:** Register Field 2
15:8	0h RO	**R1:** Register Field 1
7:0	0h RO	**R0:** Register Field 0

8.40 Fixed-Range MTRR Format 16K-A0000 (MTRR_FIX16K_A0000_REG_0_0_0_VTDBAR) - Offset 130h

Fixed Range MTRR covering the 16K memory space from 0xA0000 - 0xBFFFF.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 130h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RO	**R7:** Register Field 7
55:48	0h RO	**R6:** Register Field 6
47:40	0h RO	**R5:** Register Field 5
39:32	0h RO	**R4:** Register Field 4
31:24	0h RO	**R3:** Register Field 3

Bit Range	Default & Access	Field Name (ID): Description
23:16	0h RO	**R2:** Register Field 2
15:8	0h RO	**R1:** Register Field 1
7:0	0h RO	**R0:** Register Field 0

8.41 Fixed-Range MTRR Format 4K-C0000 (MTRR_FIX4K_C0000_REG_0_0_0_VTDBAR) - Offset 138h

Fixed Range MTRR covering the 4K memory space 0xC0000 - 0xC7FFF.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 138h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RO	**R7:** Register Field 7
55:48	0h RO	**R6:** Register Field 6
47:40	0h RO	**R5:** Register Field 5
39:32	0h RO	**R4:** Register Field 4
31:24	0h RO	**R3:** Register Field 3
23:16	0h RO	**R2:** Register Field 2
15:8	0h RO	**R1:** Register Field 1
7:0	0h RO	**R0:** Register Field 0

8.42 Fixed-Range MTRR Format 4K-C8000 (MTRR_FIX4K_C8000_REG_0_0_0_VTDBAR) - Offset 140h

Fixed Range MTRR covering the 4K memory space from 0xC8000 - 0xCFFFF.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 140h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RO	**R7:** Register Field 7
55:48	0h RO	**R6:** Register Field 6
47:40	0h RO	**R5:** Register Field 5
39:32	0h RO	**R4:** Register Field 4
31:24	0h RO	**R3:** Register Field 3
23:16	0h RO	**R2:** Register Field 2
15:8	0h RO	**R1:** Register Field 1
7:0	0h RO	**R0:** Register Field 0

8.43 Fixed-Range MTRR Format 4K-D0000 (MTRR_FIX4K_D0000_REG_0_0_0_VTDBAR) - Offset 148h

Fixed Range MTRR covering the 4K memory space from 0xD0000 - 0xD7FFF.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 148h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RO	**R7:** Register Field 7
55:48	0h RO	**R6:** Register Field 6
47:40	0h RO	**R5:** Register Field 5
39:32	0h RO	**R4:** Register Field 4
31:24	0h RO	**R3:** Register Field 3

Bit Range	Default & Access	Field Name (ID): Description
23:16	0h RO	**R2:** Register Field 2
15:8	0h RO	**R1:** Register Field 1
7:0	0h RO	**R0:** Register Field 0

8.44 Fixed-Range MTRR Format 4K-D8000 (MTRR_FIX4K_D8000_REG_0_0_0_VTDBAR) - Offset 150h

Fixed Range MTRR covering the 4K memory space from 0xD80000 - 0xDFFFF.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 150h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RO	**R7:** Register Field 7
55:48	0h RO	**R6:** Register Field 6
47:40	0h RO	**R5:** Register Field 5
39:32	0h RO	**R4:** Register Field 4
31:24	0h RO	**R3:** Register Field 3
23:16	0h RO	**R2:** Register Field 2
15:8	0h RO	**R1:** Register Field 1
7:0	0h RO	**R0:** Register Field 0

8.45 Fixed-Range MTRR Format 4K-E0000 (MTRR_FIX4K_E0000_REG_0_0_0_VTDBAR) - Offset 158h

Fixed Range MTRR covering the 4K memory space from 0xE0000 - 0xE7FFF.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 158h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RO	**R7:** Register Field 7
55:48	0h RO	**R6:** Register Field 6
47:40	0h RO	**R5:** Register Field 5
39:32	0h RO	**R4:** Register Field 4
31:24	0h RO	**R3:** Register Field 3
23:16	0h RO	**R2:** Register Field 2
15:8	0h RO	**R1:** Register Field 1
7:0	0h RO	**R0:** Register Field 0

8.46 Fixed-Range MTRR Format 4K-E8000 (MTRR_FIX4K_E8000_REG_0_0_0_VTDBAR) - Offset 160h

Fixed Range MTRR covering the 4K memory space from 0xE8000 - 0xEFFFF.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 160h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RO	**R7:** Register Field 7
55:48	0h RO	**R6:** Register Field 6
47:40	0h RO	**R5:** Register Field 5
39:32	0h RO	**R4:** Register Field 4
31:24	0h RO	**R3:** Register Field 3

Bit Range	Default & Access	Field Name (ID): Description
23:16	0h RO	**R2:** Register Field 2
15:8	0h RO	**R1:** Register Field 1
7:0	0h RO	**R0:** Register Field 0

8.47 Fixed-Range MTRR Format 4K-F0000 (MTRR_FIX4K_F0000_REG_0_0_0_VTDBAR) - Offset 168h

Fixed Range MTRR covering the 4K memory space from 0xF0000 - 0xF7FFF.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 168h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RO	**R7:** Register Field 7
55:48	0h RO	**R6:** Register Field 6
47:40	0h RO	**R5:** Register Field 5
39:32	0h RO	**R4:** Register Field 4
31:24	0h RO	**R3:** Register Field 3
23:16	0h RO	**R2:** Register Field 2
15:8	0h RO	**R1:** Register Field 1
7:0	0h RO	**R0:** Register Field 0

8.48 Fixed-Range MTRR Format 4K-F8000 (MTRR_FIX4K_F8000_REG_0_0_0_VTDBAR) - Offset 170h

Fixed Range MTRR covering the 4K memory space from 0xF8000 - 0xFFFFF.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 170h	00000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:56	0h RO	**R7:** Register Field 7
55:48	0h RO	**R6:** Register Field 6
47:40	0h RO	**R5:** Register Field 5
39:32	0h RO	**R4:** Register Field 4
31:24	0h RO	**R3:** Register Field 3
23:16	0h RO	**R2:** Register Field 2
15:8	0h RO	**R1:** Register Field 1
7:0	0h RO	**R0:** Register Field 0

8.49 Variable-Range MTRR Format Physical Base 0 (MTRR_PHYSBASE0_REG_0_0_0_VTDBAR) - Offset 180h

Variable-Range MTRR BASE0.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 180h	00000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 0
11:8	0h RO	**Reserved**
7:0	0h RO	**MEMTYPE:** Memory type for variable memory type range 0

8.50 Variable-Range MTRR Format Physical Mask 0 (MTRR_PHYSMASK0_REG_0_0_0_VTDBAR) - Offset 188h

Variable-Range MTRR MASK0.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 188h	00000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 0
11	0h RO	**VALID:** Valid bit for variable range 0 mask
10:0	0h RO	**Reserved**

8.51 Variable-Range MTRR Format Physical Base 1 (MTRR_PHYSBASE1_REG_0_0_0_VTDBAR) - Offset 190h

Variable-Range MTRR BASE1.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 190h	00000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 1
11:8	0h RO	**Reserved**
7:0	0h RO	**MEMTYPE:** Memory type for variable memory type range 1

8.52 Variable-Range MTRR Format Physical Mask 1 (MTRR_PHYSMASK1_REG_0_0_0_VTDBAR) - Offset 198h

Variable-Range MTRR MASK1.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 198h	0000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 1
11	0h RO	**VALID:** Valid bit for variable range 1 mask
10:0	0h RO	**Reserved**

8.53 Variable-Range MTRR Format Physical Base 2 (MTRR_PHYSBASE2_REG_0_0_0_VTDBAR) - Offset 1A0h

Variable-Range MTRR BASE2.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 1A0h	0000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 2
11:8	0h RO	**Reserved**
7:0	0h RO	**MEMTYPE:** Memory type for variable memory type range 2

8.54 Variable-Range MTRR Format Physical Mask 2 (MTRR_PHYSMASK2_REG_0_0_0_VTDBAR) - Offset 1A8h

Variable-Range MTRR MASK2.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 1A8h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 2
11	0h RO	**VALID:** Valid bit for variable range 2 mask
10:0	0h RO	**Reserved**

8.55 Variable-Range MTRR Format Physical Base 3 (MTRR_PHYSBASE3_REG_0_0_0_VTDBAR) - Offset 1B0h

Variable-Range MTRR BASE3.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 1B0h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 3
11:8	0h RO	**Reserved**
7:0	0h RO	**MEMTYPE:** Memory type for variable memory type range 3

8.56 Variable-Range MTRR Format Physical Mask 3 (MTRR_PHYSMASK3_REG_0_0_0_VTDBAR) - Offset 1B8h

Variable-Range MTRR MASK3.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 1B8h	00000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 3
11	0h RO	**VALID:** Valid bit for variable range 3 mask
10:0	0h RO	**Reserved**

8.57 Variable-Range MTRR Format Physical Base 4 (MTRR_PHYSBASE4_REG_0_0_0_VTDBAR) - Offset 1C0h

Variable-Range MTRR BASE4.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 1C0h	00000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 4
11:8	0h RO	**Reserved**
7:0	0h RO	**MEMTYPE:** Memory type for variable memory type range 4

8.58 Variable-Range MTRR Format Physical Mask 4 (MTRR_PHYSMASK4_REG_0_0_0_VTDBAR) - Offset 1C8h

Variable-Range MTRR MASK4.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 1C8h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 4
11	0h RO	**VALID:** Valid bit for variable range 4 mask
10:0	0h RO	**Reserved**

8.59 Variable-Range MTRR Format Physical Base 5 (MTRR_PHYSBASE5_REG_0_0_0_VTDBAR) - Offset 1D0h

Variable-Range MTRR BASE5.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 1D0h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 5
11:8	0h RO	**Reserved**
7:0	0h RO	**MEMTYPE:** Memory type for variable memory type range 5

8.60 Variable-Range MTRR Format Physical Mask 5 (MTRR_PHYSMASK5_REG_0_0_0_VTDBAR) - Offset 1D8h

Variable-Range MTRR MASK5.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 1D8h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 5
11	0h RO	**VALID:** Valid bit for variable range 5 mask
10:0	0h RO	**Reserved**

8.61 Variable-Range MTRR Format Physical Base 6 (MTRR_PHYSBASE6_REG_0_0_0_VTDBAR) - Offset 1E0h

Variable-Range MTRR BASE6.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 1E0h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 6
11:8	0h RO	**Reserved**
7:0	0h RO	**MEMTYPE:** Memory type for variable memory type range 6

8.62 Variable-Range MTRR Format Physical Mask 6 (MTRR_PHYSMASK6_REG_0_0_0_VTDBAR) - Offset 1E8h

Variable-Range MTRR MASK6.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 1E8h	00000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 6
11	0h RO	**VALID:** Valid bit for variable range 6 mask
10:0	0h RO	**Reserved**

8.63 Variable-Range MTRR Format Physical Base 7 (MTRR_PHYSBASE7_REG_0_0_0_VTDBAR) - Offset 1F0h

Variable-Range MTRR BASE7.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 1F0h	00000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 7
11:8	0h RO	**Reserved**
7:0	0h RO	**MEMTYPE:** Memory type for variable memory type range 7

8.64 Variable-Range MTRR Format Physical Mask 7 (MTRR_PHYSMASK7_REG_0_0_0_VTDBAR) - Offset 1F8h

Variable-Range MTRR MASK7.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 1F8h	0000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 7
11	0h RO	**VALID:** Valid bit for variable range 7 mask
10:0	0h RO	**Reserved**

8.65 Variable-Range MTRR Format Physical Base 8 (MTRR_PHYSBASE8_REG_0_0_0_VTDBAR) - Offset 200h

Variable-Range MTRR BASE8.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 200h	0000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 8
11:8	0h RO	**Reserved**
7:0	0h RO	**MEMTYPE:** Memory type for variable memory type range 8

8.66 Variable-Range MTRR Format Physical Mask 8 (MTRR_PHYSMASK8_REG_0_0_0_VTDBAR) - Offset 208h

Variable-Range MTRR MASK8.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 208h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 8
11	0h RO	**VALID:** Valid bit for variable range 8 mask
10:0	0h RO	**Reserved**

8.67 Variable-Range MTRR Format Physical Base 9 (MTRR_PHYSBASE9_REG_0_0_0_VTDBAR) - Offset 210h

Variable-Range MTRR BASE9.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 210h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Base (PHYSBASE):** Base Address for variable memory type range 9
11:8	0h RO	**Reserved**
7:0	0h RO	**MEMTYPE:** Memory type for variable memory type range 9

8.68 Variable-Range MTRR Format Physical Mask 9 (MTRR_PHYSMASK9_REG_0_0_0_VTDBAR) - Offset 218h

Variable-Range MTRR MASK9.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 218h	00000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:39	0h RO	**Reserved**
38:12	0h RO	**Physical Mask (PHYSMASK):** Address mask for variable memory type range 9
11	0h RO	**VALID:** Valid bit for variable range 9 mask
10:0	0h RO	**Reserved**

8.69 Fault Recording Register Low [0] (FRCDL_REG_0_0_0_VTDBAR) - Offset 400h

Register to record fault information when primary fault logging is active. Hardware reports the number and location of fault recording registers through the Capability register. This register is relevant only for primary fault logging. This register is sticky and can be cleared only through power good reset or by software clearing the RW1C fields by writing a 1.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 400h	00000000000 00000h

Bit Range	Default & Access	Field Name (ID): Description
63:12	0h RO/V	**Fault Info (FI):** When the Fault Reason (FR) field indicates one of the DMA-remapping fault conditions, bits 63:12 of this field contain the page address in the faulted DMA request. Hardware treats bits 63:N as reserved (0), where N is the maximum guest address width (MGAW) supported. When the Fault Reason (FR) field indicates one of the interrupt-remapping fault conditions, bits 63:48 of this field indicate the interrupt_index computed for the faulted interrupt request, and bits 47:12 are cleared. This field is relevant only when the F field is Set.
11:0	0h RO	**Reserved**

8.70 Fault Recording Register High [0] (FRCDH_REG_0_0_0_VTDBAR) - Offset 408h

Register to record fault information when primary fault logging is active. Hardware reports the number and location of fault recording registers through the Capability register. This register is relevant only for primary fault logging. This register is sticky and can be cleared only through power good reset or by software clearing the RW1C fields by writing a 1.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 408h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/1C	**F:** Hardware sets this field to indicate a fault is logged in this Fault Recording register. The F field is set by hardware after the details of the fault is recorded in other fields. When this field is Set, hardware may collapse additional faults from the same source-id (SID) Software writes the value read from this field to Clear it.
62	0h RO/V	**T:** Type of the faulted request: • 0=0: Write request • 1=1: Read request or Atomic Op request This field is relevant only when the F field is Set, and when the fault reason (FR) indicates one of the DMA-remapping fault conditions.
61:60	0h RO/V	**Address Type (AT):** This field captures the AT field from the faulted DMA request. Hardware implementations not supporting Device-IOTLBs (DI field Clear in Extended Capability register) treat this field as RsvdZ. When supported, this field is valid only when the F field is Set, and when the fault reason (FR) indicates one of the DMA-remapping fault conditions.
59:40	0h RO/V	**PASID Value (PV):** PASID value in the faulted request. This field is relevant only when the PP field is set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
39:32	0h RO/V	**Fault Reason (FR):** Reason for the fault This field is relevant only when the F field is set.
31	0h RO/V	**PASID Present (PP):** When set, indicates the faulted request has a PASID tag. The value of the PASID field is reported in the PASID Value (PV) field. This field is relevant only when the F field is Set, and when the fault reason (FR) indicates one of the non-recoverable address translation fault conditions. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
30	0h RO/V	**Execute Permission Requested (EXE):** When set, indicates Execute permission was requested by the faulted read request. This field is relevant only when the PP field and T field are both Set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.

Bit Range	Default & Access	Field Name (ID): Description
29	0h RO/V	**Privilege Mode Requested (PRIV):** When set, indicates Supervisor privilege was requested by the faulted request. This field is relevant only when the PP field is Set. Hardware implementations not supporting PASID (PASID field Clear in Extended Capability register) implement this field as RsvdZ.
28:16	0h RO	**Reserved**
15:0	0h RO/V	**Source Identifier (SID):** Requester-id associated with the fault condition This field is relevant only when the F field is set.

8.71 Invalidate Address Register (IVA_REG_0_0_0_VTDBAR) - Offset 500h

Register to provide the DMA address whose corresponding IOTLB entry needs to be invalidated through the corresponding IOTLB Invalidate register. This register is a write-only register.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 500h	0000000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63:12	0h RW	**ADDR:** Software provides the DMA address that needs to be page-selectively invalidated. To make a page-selective invalidation request to hardware, software must first write the appropriate fields in this register, and then issue the appropriate page-selective invalidate command through the IOTLB_REG. Hardware ignores bits 63:N, where N is the maximum guest address width (MGAW) supported.A value returned on a read of this field is undefined. A value returned on a read of this field is undefined

Bit Range	Default & Access	Field Name (ID): Description
11:7	0h RO	**Reserved**
6	0h RW	**Invalidation Hint (IH):** The field provides hint to hardware about preserving or flushing the non-leaf (page-directory) entries that may be cached in hardware: • 0 = Software may have modified both leaf and non-leaf page-table entries corresponding to mappings specified in the ADDR and AM fields. On a page-selective invalidation request, hardware must flush both the cached leaf and non-leaf page-table entries corresponding to the mappings specified by ADDR and AM fields. • 1 = Software has not modified any non-leaf page-table entries corresponding to mappings specified in the ADDR and AM fields. On a page-selective invalidation request, hardware may preserve the cached non-leaf page-table entries corresponding to mappings specified by ADDR and AM fields. A value returned on a read of this field is undefined
5:0	0h RW	**Address Mask (AM):** The value in this field specifies the number of low order bits of the ADDR field that must be masked for the invalidation operation. This field enables software to request invalidation of contiguous mappings for size-aligned regions. For example:...Mask ADDR bits Pages. Value masked invalidated... 0 None 1... 1 12 2... 2 13:12 4... 3 14:12 8... 4 15:12 16 When invalidating mappings for super-pages, software must specify the appropriate mask value. For example, when invalidating mapping for a 2MB page, software must specify an address mask value of at least 9...Hardware implementations report the maximum supported mask value through the Capability register.

8.72 IOTLB Invalidate Register (IOTLB_REG_0_0_0_VTDBAR) - Offset 508h

Register to invalidate IOTLB. The act of writing the upper byte of the IOTLB_REG with IVT field Set causes the hardware to perform the IOTLB invalidation.

Type	Size	Offset	Default
MEM	64 bit	GFXVTBAR + 508h	0200000000000000h

Bit Range	Default & Access	Field Name (ID): Description
63	0h RW/V	**Invalidate IOTLB (IVT):** Software requests IOTLB invalidation by setting this field. Software must also set the requested invalidation granularity by programming the IIRG field. Hardware clears the IVT field to indicate the invalidation request is complete. Hardware also indicates the granularity at which the invalidation operation was performed through the IAIG field. Software must not submit another invalidation request through this register while the IVT field is Set, nor update the associated Invalidate Address register. Software must not submit IOTLB invalidation requests when there is a context-cache invalidation request pending at this remapping hardware unit. Hardware implementations reporting write-buffer flushing requirement (RWBF=1 in Capability register) must implicitly perform a write buffer flushing before invalidating the IOTLB.
62	0h RO	**Reserved**
61:60	0h RW	**IOTLB Invalidation Request Granularity (IIRG):** When requesting hardware to invalidate the IOTLB (by setting the IVT field), software writes the requested invalidation granularity through this field. The following are the encodings for the field • 00 = Reserved • 01 = Global invalidation request • 10 = Domain-selective invalidation request. The target domain-id must be specified in the DID field • 11 = Page-selective invalidation request. The target address, mask and invalidation hint must be specified in the Invalidate Address register, and the domain-id must be provided in the DID field Hardware implementations may process an invalidation request by performing invalidation at a coarser granularity than requested. Hardware indicates completion of the invalidation request by clearing the IVT field. At this time, the granularity at which actual invalidation was performed is reported through the IAIG field
59	0h RO	**Reserved**
58:57	1h RO/V	**IOTLB Actual Invalidation Granularity (IAIG):** Hardware reports the granularity at which an invalidation request was processed through this field when reporting invalidation completion (by clearing the IVT field). The following are the encodings for this field • 00 = Reserved. This indicates hardware detected an incorrect invalidation request and ignored the request. Examples of incorrect invalidation requests include detecting an unsupported address mask value in Invalidate Address register for page-selective invalidation requests • 01 = Global Invalidation performed. This could be in response to a global, domain-selective, or page-selective invalidation request • 10 = Domain-selective invalidation performed using the domain-id specified by software in the DID field. This could be in response to a domain-selective or a page-selective invalidation request • 11 = Domain-page-selective invalidation performed using the address, mask and hint specified by software in the Invalidate Address register and domain-id specified in DID field. This can be in response to a page-selective invalidation request.
56:50	0h RO	**Reserved**
49	0h RW	**Drain Reads (DR):** This field is ignored by hardware if the DRD field is reported as clear in the Capability register. When the DRD field is reported as Set in the Capability register, the following encodings are supported for this field: • 0 = Hardware may complete the IOTLB invalidation without draining any translated DMA read requests • 1 = Hardware must drain DMA read requests.

Bit Range	Default & Access	Field Name (ID): Description
48	0h RW	**Drain Writes (DW):** This field is ignored by hardware if the DWD field is reported as Clear in the Capability register. When the DWD field is reported as Set in the Capability register, the following encodings are supported for this field: • 0 = Hardware may complete the IOTLB invalidation without draining DMA write requests • 1 = Hardware must drain relevant translated DMA write requests.
47:32	0h RW	**DID:** Indicates the ID of the domain whose IOTLB entries need to be selectively invalidated. This field must be programmed by software for domain-selective and page-selective invalidation requests. The Capability register reports the domain-id width supported by hardware. Software must ensure that the value written to this field is within this limit. Hardware ignores and not implements bits 47:(32+N), where N is the supported domain-id width reported in the Capability register.
31:0	0h RO	**Reserved**

9 Dynamic Power Performance Management (DPPM) Registers (D4:F0)

This chapter documents the registers in Bus: 0, Device 4, Function 0.

Table 9-1. Summary of Bus: 0 Device: 4 Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	2	VID_0_4_0_PCI	8086h
54h	4	DEVEN_0_4_0_PCI	0000FFFFh
E4h	4	CAPID0_A_0_4_0_PCI	00000000h

9.1 VID_0_4_0_PCI - Offset 0h

This register combined with the Device Identification register uniquely identifies any PCI device.

Type	Size	Offset	Default
CFG	16 bit	[B:0, D:4, F:0] + 0h	8086h

Bit Range	Default & Access	Field Name (ID): Description
15:0	8086h RO	**VID:** PCI standard identification for Intel.

9.2 DEVEN_0_4_0_PCI - Offset 54h

Allows for enabling/disabling of PCI devices and functions that are within the CPU package. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:4, F:0] + 54h	0000FFFFh

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15	1h RW/L	**D8EN:** 0: Bus 0 Device 8 is disabled and not visible. 1: Bus 0 Device 8 is enabled and visible. This bit will be set to 0b and remain 0b if Device 8 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.GMM_DIS
14	1h RO	**Reserved**
13	1h RO	**Reserved**
12	1h RW/L	**D9EN:** 0: Bus 0 Device 9 is disabled and not visible. 1: Bus 0 Device 9 is enabled and visible. This bit will be set to 0b and remain 0b if Device 9 capability is disabled. **Locked by:** CAPID0_B_0_0_0_PCI.NPK_DIS
11	1h RO	**Reserved**
10	1h RO	**Reserved**
9	1h RO	**Reserved**
8	1h RO	**Reserved**
7	1h RW/L	**D4EN:** 0: Bus 0 Device 4 is disabled and not visible. 1: Bus 0 Device 4 is enabled and visible. This bit will be set to 0b and remain 0b if Device 4 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.CDD
6	1h RO	**Reserved**
5	1h RO	**Reserved**
4	1h RW/L	**D2EN:** 0: Bus 0 Device 2 is disabled and hidden. 1: Bus 0 Device 2 is enabled and visible. This bit will be set to 0b and remain 0b if Device 2 capability is disabled. **Locked by:** CAPID0_A_0_0_0_PCI.IGD
3	1h RO	**Reserved**
2	1h RO	**Reserved**
1	1h RO	**Reserved**
0	1h RO	**D0EN:** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

9.3 CAPID0_A_0_4_0_PCI - Offset E4h

Control of bits in this register is only required for customer visible SKU differentiation.

Type	Size	Offset	Default
CFG	32 bit	[B:0, D:4, F:0] + E4h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31	0h RO	**Reserved**
30	0h RO	**Reserved**
29	0h RO	**Reserved**
28	0h RO	**Reserved**
27	0h RW/L	**PELWUD:** 0: Link width upconfig is supported. The CPU advertises upconfig capability using the data rate symbol in its TS2 training ordered sets during Configuration.Complete. The CPU responds to link width upconfigs initiated by the downstream device. 1: Link width upconfig is NOT supported. The CPU does not advertise upconfig capability using the data rate field in TS2 training ordered sets during Configuration.Complete. The CPU does not respond to link width upconfigs initiated by the downstream device.
26	0h RO	**Reserved**
25	0h RO	**Reserved**
24	0h RO	**Reserved**
23	0h RW/L	**VTDD:** 0: Enable VTd. 1: Disable VTd.
22	0h RO	**Reserved**
21	0h RO	**Reserved**
20:19	0h RW/L	**DDRSZ:** This field defines the maximum allowed memory size per channel. 00b Unlimited (64GB per channel). 01b Maximum 8GB per channel. 10b Maximum 4GB per channel. 11b Maximum 2GB per channel.
18	0h RO	**Reserved**
17	0h RW/L	**D1NM:** 0: Part is capable of supporting 1n mode timings on the DDR interface. 1: Part is not capable of supporting 1n mode. Only supported timings are 2n or greater.

Bit Range	Default & Access	Field Name (ID): Description
16	0h RO	**Reserved**
15	0h RW/L	**CDD:** 0: Camarillo Device enabled. 1: Camarillo Device disabled.
14	0h RO	**Reserved**
13	0h RW/L	**X2APIC_EN:** Extended Interrupt Mode. 0b: Hardware does not support Extended APIC mode. 1b: Hardware supports Extended APIC mode.
12	0h RW/L	**PDCD:** 0: Capable of Dual Channels 1: Not Capable of Dual Channel - only single channel capable.
11	0h RW/L	**IGD:** 0: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the CPU. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2. A selected amount of Graphics Memory space is preallocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is preallocated above TSEG Memory. 1: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on to DMI. In addition, all clocks to internal graphics logic are turned off. DEVEN [4:3] (Device 0, offset 54h) have no meaning. Device 2 Functions 0 and 1 are disabled and hidden.
10	0h RW/L	**DID0OE:** 0b Disable ability to override DID0 - For production. 1b Enable ability to override DID - For debug and samples only.
9:8	0h RO	**Reserved**
7:4	0h RW/L	**CRID:** Compatibility Rev ID: PCODE will update this field with the value of FUSE_CRID.
3	0h RO	**Reserved**
2	0h RO	**Reserved**
1	0h RO	**Reserved**
0	0h RO	**Reserved**

10 Gauss Newton Algorithm Registers (GNA) Registers (D8:F0)

This chapter documents the registers in Bus: 0, Device 8, Function 0.

Table 10-1. Summary of Bus: 0, Device: 8, Function: 0 Registers

Offset	Size (Bytes)	Register Name (Register Symbol)	Default Value
0h	4	IDENTIFICATION	00008086h
4h	2	Device Control (DCTRL)	0000h
6h	2	Device Status (DSTS)	0010h
8h	4	RID: Revision ID DLCO: Class Code (RID_DLCO)	08800000h
Ch	1	Cache Line Size (CLS)	00h
Eh	1	Header Type (HTYPE)	00h
Fh	1	Built-in Self Test (BIST)	00h
10h	4	GNA Base Address Low (GNABAL)	00000004h
14h	4	GNA Base Address High (GNABAH)	00000000h
2Ch	2	Sub System Vendor Identifiers (SSVI)	0000h
2Eh	2	Sub System Identifiers (SSI)	0000h
34h	4	Capabilities Pointers (CAPP)	00000090h
3Ch	1	Interrupt Line (INTL)	00h
3Dh	1	Interrupt Pin Register (INTP)	01h
3Eh	2	Min Grant And Min Latency Register (MINGNTLAT)	0000h
40h	4	Override Configuration Control (OVRCFGCTL)	00000000h
90h	2	Message Signaled Interrupt Capability ID (MSICAPID)	A005h
92h	2	Message Signaled Interrupt Message Control (MC)	0000h
94h	4	Message Signaled Interrupt Message Address (MA)	00000000h
98h	4	Message Signaled Interrupt Message Data (MD)	00000000h
A0h	2	D0i3 Capability ID (D0I3CAPID)	DC09h
A2h	2	D0i3 Capability (D0I3CAP)	F014h
A4h	4	D0i3 Vendor Extended Capability Register (D0I3VSEC)	01400010h
A8h	4	D0i3 SW LTR Pointer Register (D0I3SWLTRPTR)	00000000h
ACh	4	D0i3 DevIdle Pointer Register (D0I3DEVIDLEPTR)	00000A81h
B0h	2	D0i3 DevIdle Power On Latency (D0I3DEVIDLEPOL)	0800h
B2h	2	D0i3 Power Control Enables Register (PCE)	0028h
DCh	2	Power Management Capability ID (PMCAPID)	F001h
DEh	2	Power Management Capability (PMCAP)	0002h
E0h	2	Power Management Control Status (PMCS)	0000h
F0h	2	FLR Capability ID (FLRCAPID)	0013h
F2h	2	FLR Capability Length And Version (FLRMISC)	0306h
F4h	1	FLR Control Register (FLRCTL)	00h
F5h	1	FLR Status Register (FLRSTS)	00h

10.1 IDENTIFICATION — Offset 0h

Device ID assigned to GNA and Vendor ID

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 0h	00008086h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0000h RO/V	**Device Identification Number (DID):** Indicates the device ID assigned to the GNA
15:0	8086h RO	**Vendor Identification Number (VID):** Indicates Intel's Identification

10.2 Device Control (DCTRL) — Offset 4h

The Command register provides coarse control over GMM's abilities like Unsupported Request Error Reporting Enable, Poisoned TLP Error Reporting Enable, Interrupt Disable, Max Aligned Payload Size, Max Aligned Read Request Size, Special Cycle Enable, Bus Master Enable, Memory Space Enable

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 4h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Reserved**
14	0h RO	**Unsupported Request Error Reporting Enable (UNSPREQERREN):** Unsupported Request Error Reporting Enable
13	0h RO	**Poisoned TLP Error Reporting Enable (PTLPERREN):** Poisoned TLP Error Reporting Enable
12:11	0h RO	**Reserved**
10	0h RW	**Interrupt Disable (INTDIS):** Interrupt Disable: Controls the ability of the function to generate INTx interrupts. 0: INTx allowed 1: INTx disabled
9:6	0h RO	**Reserved**
5	0h RO	**Max Aligned Payload Size (MXAPAYLDSZ):** Max Aligned Payload Size - Reserved
4	0h RO	**Max Aligned Read Request Size (MXARDREQSZ):** Max Aligned Read Request Size - Reserved
3	0h RO	**Special Cycle Enable (SCEN):** Special Cycle Enable - Reserved

Bit Range	Default & Access	Field Name (ID): Description
2	0h RW	**Bus Master Enable (BME):** Bus Master Enable: 0: Disable (default) 1: Enabled. Device may generate bus master transactions depending on its mode of operation.
1	0h RW	**Memory Space Enable (MSE):** Memory Space Enable Controls the GMM devices response to memory space accesses 0: Disabled (default) 1: Enabled. Device will respond to memory space accesses.
0	0h RO	**IO Space Enable (IOSE):** IO Space Enable. Not implemented.

10.3 Device Status (DSTS) — Offset 6h

The Status register to record status information for PCI related events

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 6h	0010h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**Detected Parity Error (DPE):** This bit is Set by a Function whenever it receives a Poisoned TLP, regardless of the state the Parity Error Response bit in the Command register. On a Function with a Type 1 Configuration header, the bit is Set when the Poisoned TLP is received by its Primary Side. ***Note:*** Some implementations use this error type as non-fatal error indication.
14	0h RO	**Signaled System Error (SSE):** This bit is Set when a Function sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR# Enable bit in the Command register is 1. ***Note:*** Some implementations use this error for fatal. When received all operations are aborted.
13	0h RW/1C/V	**Received Master Abort (RMA):** This bit is Set when a Requester receives a Completion with Unsupported Request Completion Status. On a Function with a Type 1 Configuration header, the bit is Set when the Unsupported Request is received by its Primary Side.
12	0h RW/1C/V	**Received Target Abort (RTA):** This bit is set when a transaction abort is received to a GMM initiated transaction
11	0h RW/1C/V	**Signaled Target Abort (STA):** This bit is Set when a Function completes a Posted or Non-Posted Request as a Completer Abort error. This applies to a Function with a Type 1 Configuration header when the Completer Abort was generated by its Primary Side.
10:8	0h RO	**Reserved**
7	0h RO	**Fast Back-to-Back (FB2B):** Fast Back-to-Back (ignored by software)

Bit Range	Default & Access	Field Name (ID): Description
6:5	0h RO	**Reserved**
4	1h RO	**Capability List (CLIST):** Capability List 0: no capability list 1: the GMM contains a linked list of capabilities which is accessed via the CAPPTR register at offset 34h
3	0h RO/V	**Interrupt Status (INTSTS):** Interrupt Status Reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will this device send a virtual INTA. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit is controlled by HW. 0: No interrupt pending 1: Interrupt pending
2:0	0h RO	**Reserved**

10.4 RID: Revision ID DLCO: Class Code (RID_DLCO) — Offset 8h

RID: Revision ID

DLCO: This register identifies the type of device. The values are as defined in PCI 3.0 bus specification in Appendix D. The GMM is identified as an Other system Peripheral

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 8h	08800000h

Bit Range	Default & Access	Field Name (ID): Description
31:24	08h RO	**Base Class Code (BCC):** Base Class (Generic system Peripherals)
23:16	80h RO	**Sub Class Code (SCC):** Sub Class
15:8	00h RO	**Peripheral Interface (PROGINTERFACE):** Interface (other system peripheral)
7:0	00h RO/V	**Revision ID (RID):** Indicates stepping of this device. This register is set by side-band. All RID registers are sourced from a fuse/settings incremented for each stepping.

10.5 Cache Line Size (CLS) — Offset Ch

The system cacheline size in units of DWORDS

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + Ch	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Cache Line Size (CLS):** Implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express device functionality

10.6 Header Type (HTYPE) — Offset Eh

This byte identifies the layout of the second part of the predefined header and whether or not the device contains multiple functions (GMM is a single-function device of basic configuration space format, so this register is Read-Only and hardwired to 0)

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + Eh	00h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**Multi Function Device (MFD):** Hardwired to 0 indicating this device is not a multi-function device.
6:0	00h RO	**Header Type (HT):** The value 00h, indicates a basic (i.e., single function) configuration space format.

10.7 Built-in Self Test (BIST) — Offset Fh

This register describes the BIST capability of GMM and since GMM doesn't support BIST, the register is configured as Read Only

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + Fh	00h

Bit Range	Default & Access	Field Name (ID): Description
7	0h RO	**BIST Capable (BISTCAP):** BIST Capable. Hardwired to 0 since this device does not implement BIST.
6	0h RO	**Start BIST (BISTST):** Start BIST. Hardwired to 0 since this device does not implement BIST
5:4	0h RO	**Reserved**
3:0	0h RO	**BIST Completion Code (BISTCC):** Hardwired to 0 since this device does not implement BIST.

10.8 GNA Base Address Low (GNABAL) — Offset 10h

GNA Base Address Low: Lower 32-bits of the GNA Base Address register.

The GMM Base Address register may be accessed with Double Word (32bit) read/write operations.

In 32-bit OS, the address specified may be limited by 32-bit of space, and the renaming bits must stay with their default values

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 10h	00000004h

Bit Range	Default & Access	Field Name (ID): Description
31:12	00000h RW	**Memory Base Address Low (BAL):** Memory Base Address Low Base address of this device's memory mapped IO space. A page of 4KB of address is used
11:4	00h RO	**Address Mask (ADDRMSK):** Address Mask Hardwired to 0s to indicate at least 4KB address range
3	0h RO	**Prefetchable Memory (PREF):** Hardwired to 0 indicating that this range is not prefetchable
2:1	2h RO	**Memory Type (MEMTY):** Memory Type: 00: 32 bit base address 01: reserved 10: 64-bit base address 11: reserved
0	0h RO	**Space Type (SPTY):** Space Type: Memory/IO Space Hardwired to 0 indicating that this is a Memory BAR

10.9 GNA Base Address High (GNABAH) — Offset 14h

GNA Base Address High: Upper 32-bits of the GNA Base Address register.

The GNA Base Address register may be accessed with Double Word (32bit) read/write operations.

In 32-bit OS, the address specified may be limited by 32-bit of space, and the renaming bits must stay with their default values

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 14h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:7	0000000h RW	**Memory Base Address High (Reserved) (BAR):** These bits must be loaded with zeros
6:0	00h RW	**Memory Base Address High (BAH):** Memory Base Address High - bits Includes the high bits of the base address used by 64-bit OS. Must hold zero for 32-bit OS

10.10 Sub System Vendor Identifiers (SSVI) — Offset 2Ch

This register is initialized to logic 0 by the assertion of reset. This register can be written only once after reset de-assertion it is locked for writes after that.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 2Ch	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/O	**Subsystem Vendor ID (SSVID):** Subsystem Vendor ID (SSVID): This is written by BIOS. No hardware action taken on this value.

10.11 Sub System Identifiers (SSI) — Offset 2Eh

This register is initialized to logic 0 by the assertion of reset. This register can be written only once after reset de-assertion it is locked for writes after that.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 2Eh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:0	0000h RW/O	**Subsystem ID (SSID):** Subsystem ID (SSID): This is written by BIOS. No hardware action taken on this value.

10.12 Capabilities Pointers (CAPP) — Offset 34h

This register gives MSI capability pointer offset

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 34h	00000090h

Bit Range	Default & Access	Field Name (ID): Description
31:8	0h RO	**Reserved**
7:0	90h RO	**Capability Pointer (CAPP):** Indicates that the MSI capability pointer offset is offset 90h

10.13 Interrupt Line (INTL) — Offset 3Ch

This register contains interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + 3Ch	00h

Bit Range	Default & Access	Field Name (ID): Description
7:0	00h RW	**Interrupt Connection (INTCON):** Interrupt Connection Communicate interrupt line routing information. BIOS Requirement: POST software writes the routing information into this register as it initializes and configures the system. The value indicates to which input of the system interrupt controller this device's interrupt pin is connected

10.14 Interrupt Pin Register (INTP) — Offset 3Dh

Tells which PCI legacy interrupt pin a device will use (GMM uses only IntA).

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + 3Dh	01h

Bit Range	Default & Access	Field Name (ID): Description
7:3	0h RO	**Reserved**
2:0	1h RO	**Legacy Interrupt (LEGINT):** When Legacy interrupts are used, function use legacy interrupt INTA.

10.15 Min Grant And Min Latency Register (MINGNTLAT) — Offset 3Eh

Specifies a device's desired settings for Latency Timer values

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 3Eh	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Min Latency (MINLAT):** Reserved
7:0	00h RO	**Min Grant (MINGNT):** Reserved

10.16 Override Configuration Control (OVRCFGCTL) — Offset 40h

This register holds bits that may be used internal mechanisms in the GMM during debug operations. Special notes will be made to BIOS writers, if any 5 of these bits will need to be set to value other than default.

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 40h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:9	0h RO	**Reserved**
8	0h RW	**Sideband Clock Gating Enable (SBDCGEN):** This bit, when set, enables the sideband interface clock used for GMM bus interface operations (gated_side_clk) to be gated when conditions are met. When clear, clock gating is disabled.
7:0	0h RO	**Reserved**

10.17 Message Signaled Interrupt Capability ID (MSICAPID) — Offset 90h

This register contains a pointer to the next item in the capabilities list which is the Power Management Capability and also helps to identify linked list item (capability structure) as being for MSI registers.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 90h	A005h

Bit Range	Default & Access	Field Name (ID): Description
15:8	A0h RO	**Pointer to Next Capability (NXTPTR):** Pointer to Next Capability This contains a pointer to the next item in the capabilities list which is the Power Management Capability
7:0	05h RO	**Capability ID (CAPID):** Capability ID Value of 05h identifies this linked list item (capability structure) as being for MSI registers.

10.18 Message Signaled Interrupt Message Control (MC) — Offset 92h

This register is defined to meet PCI Local Bus Specification 3.0; definition of MSI messages.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + 92h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15:9	0h RO	**Reserved**
8	0h RO	**Per-Vector Masking Capable (PVMCAP):** Per-Vector Masking Capable. 0- not supported by GMM
7	0h RO	**64-bit Address Capable (ADDR64CAP):** 64-bit Address Capable Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address. This may need to change in future implementations when addressable system memory exceeds the 32bit/4GB limit.

Bit Range	Default & Access	Field Name (ID): Description
6:4	0h RW	**Multiple Message Enable (MMEN):** Multiple Message Enable System software program this field to indicate the number of vectors allocated to the GMM. At least one vector must be allocated when the MSI interrupts are enabled. This value is ignored by HW as only a single vector is in use by GMM.
3:1	0h RO	**Multiple Message Capable (MMCAP):** Indicates to software the number of vectors that the GMM module is requesting for use Value Number of Messages requested 000 1 001 2 (reserved) 010 4 (reserved) 011 8 (reserved) 100 16(reserved) 101 32(reserved) Other reserved
0	0h RW	**MSI Enable (MSIEN):** MSI Enable Controls the ability of GMM to generate MSI Messages. A device driver is prohibited from writing this bit to mask a functions service request. 0: MSI will not be generated 1: MSI will be generated. INTA will not be generated and INTA status is not set.

10.19 Message Signaled Interrupt Message Address (MA) — Offset 94h

This register is defined to meet PCI Local Bus Specification 3.0; definition of MSI messages

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 94h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:2	00000000h RW	**Message Address (MADDR):** Message Address Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address
1:0	0h RO	**Reserved**

10.20 Message Signaled Interrupt Message Data (MD) — Offset 98h

This register is defined to meet PCI Local Bus Specification 3.0; definition of MSI messages

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + 98h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:16	0h RO	**Reserved**
15:0	0000h RW	**Message Data (MDAT):** Message Data Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

10.21 D0i3 Capability ID (D0I3CAPID) — Offset A0h

Pointer to next capability and capability ID

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + A0h	DC09h

Bit Range	Default & Access	Field Name (ID): Description
15:8	DCh RO	**Pointer to Next Capability (NXTPTR):** This contains a pointer to the next item in the capabilities list which is the Power Management Capability
7:0	09h RO	**Capability ID (CAPID):** Value of 09h identifies this linked list item (capability structure) is a vendor specific capability.

10.22 D0i3 Capability (D0I3CAP) — Offset A2h

Vendor-Specific Capability ID

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + A2h	F014h

Bit Range	Default & Access	Field Name (ID): Description
15:12	Fh RO	**Vendor-Specific Capability ID (VSID):** Indicates that this Vendor Specific Capability is an Extended Capability, which use a VSEC 16-bit Extended Capability in the subsequent 4B., differentiating this from other vendor specific capabilities.
11:8	0h RO	**Vendor Specific Capability Revision (VSREV):** Reserved
7:0	14h RO	**Vendor Specific Capability Length (VSLEN):** This field indicates the number of bytes in this capability including the CapID and Cap registers.

10.23 D0i3 Vendor Extended Capability Register (D0I3VSEC) — Offset A4h

Vendor Specific Extended Capability Length

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + A4h	01400010h

Bit Range	Default & Access	Field Name (ID): Description
31:20	014h RO	**Vendor Specific Extended Capability Length (VSECLEN):** Indicates that this Vendor Specific Capability is an Extended Capability, which use a VSEC 16-bit Extended Capability in the subsequent 4B., differentiating this from other vendor specific capabilities.
19:16	0h RO	**Vendor Specific Extended Capability Revision (VSREV):** For this revision of DevIdle, this field is 0h
15:0	0010h RO	**Vendor Specific Extended Capability ID (VSECID):** DevIdle has been assigned the Intel VSEC ID of 10h

10.24 D0i3 SW LTR Pointer Register (D0I3SWLTRPTR) — Offset A8h

SW LTR Update MMIO Offset Location

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + A8h	00000000h

Bit Range	Default & Access	Field Name (ID): Description
31:4	0000000h RO	**SW LTR Update MMIO Offset Location (SWLTRLOC):** The value in this field is ignored as GMM does not support SW LTR
3:1	0h RO	**Base Address Register Number (BARNUM):** The value in this field is ignored as GMM does not support SW LTR
0	0h RO	**VALID:** Indicates the use of SW LTR by the function.GMM does not use SW LTR

10.25 D0i3 DevIdle Pointer Register (D0I3DEVIDLEPTR) — Offset ACh

DevIdle MMIO Offset Location

Type	Size	Offset	Default
PCI	32 bit	[B:0, D:8, F:0] + ACh	00000A81h

Bit Range	Default & Access	Field Name (ID): Description
31:4	00000A8h RO	**DevIdle MMIO Offset Location (DEVIDLELOC):** This location pointer to the DevIdle register in MMIO space, as an offset from the BAR base.
3:1	0h RO	**Base Address Register Number (BARNUM):** The DevIdle is located in BAR0
0	1h RO	**VALID:** GMM has a DevIdle register

10.26 D0i3 DevIdle Power On Latency (D0I3DEVIDLEPOL) — Offset B0h

D0idle_5 Max_Power_On_Latency is set by BIOS at boot and read by device driver software to calculate approximate cost of a D0idle entry + exit cycle. This allows driver to avoid idle entry in cases where device duty cycle is larger than D0idle entry + exit cycle.

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + B0h	0800h

Bit Range	Default & Access	Field Name (ID): Description
15:13	0h RO	**Reserved**
12:10	2h RO	**Power On Latency Scale (POLS):** Latency Scale multiplier: 010: 1us 011: 32us All other settings are reserved. This field is a RO as there is no need for BIOS programing of it.
9:0	000h RO	**Power On Latency Value (POLV):** A value of 0 indicates a power on latency of less than 1us. This field is a RO as there is no need for BIOS programing of it.

10.27 D0i3 Power Control Enables Register (PCE) — Offset B2h

This register controls the D0i3 features like Hardware Autonomous Enable, Sleep Enable, D3-Hot Enable, I3 Enable and PMC Request Enable

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + B2h	0028h

Bit Range	Default & Access	Field Name (ID): Description
15:6	0h RO	**Reserved**
5	1h RW	**Hardware Autonomous Enable (HAE):** If set, then the IP may request a PG whenever it is idle. ***Note***: If this bit is set, then bits[2:0] must be 000.
4	0h RO	**Reserved**
3	1h RW	**Sleep Enable (SE):** If clear, then IP will never asset Sleep to the retention flops. If set, then IP may assert Sleep during PGing. Note that some platforms may default this bit to 0, others to 1.
2	0h RW	**D3-Hot Enable (D3HE):** If set, then IP will PG when idle and the PMCSR[1:0] register in the IP =11.
1	0h RW	**I3 Enable (I3E):** If set, then IP will PG when idle and the D0i3 register (D0i3C[2] = 1) is set. ***Note:*** If bits [2:1] = 11, then the IP would PG whenever either PMCSR = 11 or the D0i3C.i3 bit is set.
0	0h RW	**PMC Request Enable (PMCRE):** If set, then IP will PG when idle and the PMC requests power gating by asserting the pmc_*_sw_pg_req_b signal.

10.28 Power Management Capability ID (PMCAPID) — Offset DCh

This register contains a pointer to next item in capabilities list and also helps to identify linked list item as being for PCI Power Management registers

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + DCh	F001h

Bit Range	Default & Access	Field Name (ID): Description
15:8	F0h RO	**Next Pointer (NXTPTR):** Next Pointer This contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	01h RO	**Capability Identifier (CAPID):** Capability Identifier Identifies this linked list item as being for PCI Power Management registers.

10.29 Power Management Capability (PMCAP) — Offset DEh

This register describes the Power Management Capability of GMM

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + DEh	0002h

Bit Range	Default & Access	Field Name (ID): Description
15:11	00h RO	**PME Support (PMES):** PME Support This device does not support PMEB signal
10	0h RO	**D2 Support (D2S):** D2 This device does not support D2
9	0h RO	**D1 Support (D1S):** D1 This device does not support D1
8:6	0h RO	**Auxiliary Current (AUXC):** Auxiliary Current Reserved. Not applicable for GMM
5	0h RO	**Device Specific Initialization (DSI):** Device specific Initialization Indicates that this device requires device specific initialization before generic class device driver is to use it

Bit Range	Default & Access	Field Name (ID): Description
4	0h RO	**Auxiliary Power (AUXP):** Aux Power This device does not use Aux power
3	0h RO	**PME Clock (PMEC):**
2:0	2h RO	**VER:** Version Hardwired to 010b to indicate there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification.

10.30 Power Management Control Status (PMCS) — Offset E0h

This register has the status of PME Generation from D3(cold), Data Scale, Data Select, PME Enable and Power State

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + E0h	0000h

Bit Range	Default & Access	Field Name (ID): Description
15	0h RO	**PME Generation from D3 (cold) (PMEGD3):** PME Generation from D3 (cold) Not supported
14:13	0h RO	**Data Scale (DATSC):** Data Scale No support for Power Management Data register
12:9	0h RO	**Data Select (DATSEL):** Data Select No support for Power Management Data register

Bit Range	Default & Access	Field Name (ID): Description
8	0h RO	**PME Enable (PMEE):** PME Enable PMEB is not supported
7:2	0h RO	**Reserved**
1:0	0h RW	**Power State (PS):** Indicates the current power state of this device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00: D0 01: D1 (Not supported in this device.) 10: D2 (Not supported in this device.) 11: D3 Write of reserved values is ignored and state will not change. Support of D3cold does not require any special action. While in the D3hot state, this device can only act as the target of PCI configuration transactions (for power management control). This device also cannot generate interrupts or respond to MMR cycles in the D3 state. The device must return to the D0 state in order to be fully-functional.

10.31 FLR Capability ID (FLRCAPID) — Offset F0h

This register contains a pointer to next item in capabilities list and capability of Advanced Features

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + F0h	0013h

Bit Range	Default & Access	Field Name (ID): Description
15:8	00h RO	**Next Pointer (NXTPTR):** Next Pointer This contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	13h RO	**Capability Identifier (CAPID):** Capability Identifier A value that indicates FLR (Vendor specific value) 0: 09h (FLR in use) A value of 09h in this register indicates that this is a FLR capabilities field.

10.32 FLR Capability Length And Version (FLRMISC) — Offset F2h

This register describe the FLR Capability, TXP Capability and Capability Length

Type	Size	Offset	Default
PCI	16 bit	[B:0, D:8, F:0] + F2h	0306h

Bit Range	Default & Access	Field Name (ID): Description
15:10	0h RO	**Reserved**
9	1h RO	**FLR Capability (FLRCAP):** Indicates support for Function Level Reset (FLR).
8	1h RO	**TXP Capability (TXPCAP):** Indicates that TP bit is supported
7:0	06h RO	**Capability Length (CAPLEN):** Capability Length This bit indicates the number of bytes this vendor specified capability requires. it has a value of 06h for the FLR capability

10.33 FLR Control Register (FLRCTL) — Offset F4h

This register controls the Functional Level reset operation of GMM

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + F4h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved**
0	0h WO	**Initiate FLR (INITFLR):** Writing 1 to this field starts the Functional Level Reset. This will act similar to the Abort + will bring all non-CFG registers to their reset value. The FLR is completed when the FLR status bit is cleared

10.34 FLR Status Register (FLRSTS) — Offset F5h

This register helps to identify whether FLR is in progress

Type	Size	Offset	Default
PCI	8 bit	[B:0, D:8, F:0] + F5h	00h

Bit Range	Default & Access	Field Name (ID): Description
7:1	0h RO	**Reserved**
0	0h RO/V	**Transaction Pending (XPEND):** Transaction Pending 0: FLR not in progress 1: FLR is in progress (due to internal operation or waiting for the completion of a non-posted transaction)

11 Intel® Trace Hub (Intel® TH) Register (D9:F0)

Device 9: Intel® Trace Hub. Logically, this device appears as a PCI device residing on PCI Bus 0. Device 9 contains the configuration registers for the Trace Hub device. Trace Hub documentation can be found at https://software.intel.com/sites/default/files/managed/f3/47/intel-trace-hub-developers-manual-v2.pdf.