

Intel® Server D50TNP Family

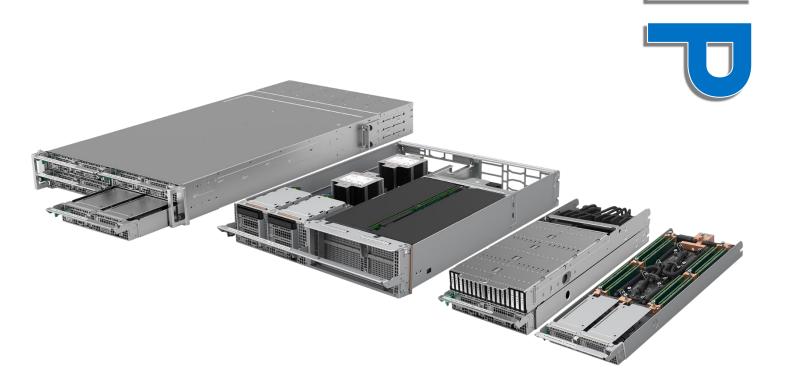
Intel® Server Board D50TNP
Intel® D50TNP Modules
Intel® Server System D50TNP

Technical Product Specification

An overview of product features, functions, architecture, and support specifications.

Rev. 1.4

July 2022



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Document Revision History

Date	Revision	Changes
May 2021	1.0	Initial production release.
July 2021	1.1	 Table 1, Documents Reference table Added two Intel® DCM documents Added 3rd Gen Intel® Xeon® Scalable processor TMSDG. Table 2. Updated Maximum Processor Thermal Design Power (TDP). Added note Tables 2, 4, 5, 6, 7. Updated the following rows USB Support. Added Important Note. Chipset. Added information Server Management Processor. Added row. Chapter 5, "Processor Support" Updated Section 5.1, "Processor Cooling Overview" Chapter 6, "Memory Support" Updated Table 12. Added Note 2. Updated Table 14. Updated row for Silver 4300 processors and added Note for Gold 6330 SKU. Section 11.4.1, "Powering on Cold Standby Supplies to Maintain Best Efficiency". Updated text. Section 11.4.2, "Powering on Cold Standby Supplies during a Fault or Over Current Condition". Updated text. Appendix G, "Board Sensors". Updated figure and table. Appendix G, "Board Sensors". Updated figure and table. Appendix E, "System Configuration Table for Thermal Compatibility". Added three processor SKUs to the tables. Appendix I, "Product Regulatory Compliance". Updated appendix. Appendix H, "Server Board Installation and Component Replacement". Added appendix Minor edits throughout for clarity
August 2021	1.2	 Updates on EVAC release/availability. Update BIOS and BMC documents titles. Minor edits on sections 10.5, 11, and 11.5. Update colors in Table 30. Update data from Table 40 and split it into Table 40 and Table 41. Update Figure 75. Minor language updates throughout the document for clarity.
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July 2022	1.4	 Updated the thermal configuration matrices for Intel® Xeon® Gold 6338T, Intel® Xeon® Platinum 8352M, and Intel® Xeon® Platinum 8362 in tables 51–56. Minor format edits throughout the document for consistency.

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1. Introduction

The Intel® Server D50TNP Family includes products that are designed to support demanding high-performance computing (HPC) and artificial intelligence (AI) applications and workloads. Building blocks in the product family allow custom development of server systems using an Intel developed server board or density optimized Intel® D50TNP Modules. The product family also includes fully integrated 2U rack mount, multi-module systems. The product family supports the 3rd Gen Intel® Xeon® Scalable processor family. Previous generation Intel® Xeon® processor and Intel® Xeon® Scalable processor families are not supported.

This document provides a high-level overview of the features, functions, architecture, and support specifications of the Intel® Server D50TNP Family. The document is divided into two main parts. The first four chapters provide feature information about the server board, modules, and system. The remaining chapters provide information about the technologies behind these features.

Note: In this document, the product name **Intel® D50TNP Modules** refers to all module types supported by the Intel® Server D50TNP Family: **Compute Module**, **Management Module**, **Storage Module**, and **Accelerator Module**.

In this document, the product name Intel® Server D50TNP Family refers to Intel® Server Board D50TNP, Intel® D50TNP Modules, and Intel® Server System D50TNP.

Note: In this document, the 3rd Gen Intel® Xeon® Scalable processor family may be referred to simply as "processor".

1.1 Product Family Overview

The core products that define the high-performance, density-optimized Intel Server D50TNP Family include:

- Intel® Server Board D50TNP
- Intel® D50TNP Modules
- Intel® Server Systems D50TNP

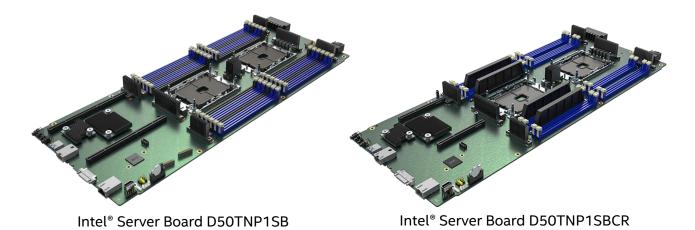


Figure 1. Intel® Server Board D50TNP

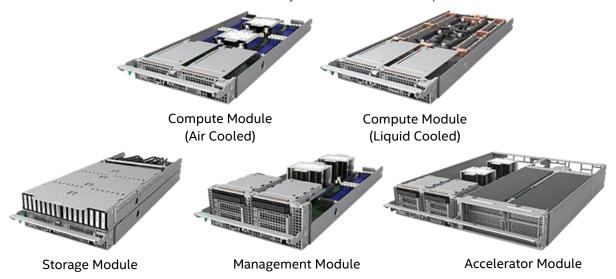


Figure 2. Intel® D50TNP Modules



Figure 3. Intel® Server System D50TNP Overview

The following options are available for ordering the board, modules, and systems.

- **L3** = Server board product
- **L6** = Modules Building Block Option with an integrated Intel® Server Board D50TNP1SB or D50TNP1SBCR. The base configuration is non-functional out of the box. Additional integration of Chassis and components required
- **L9** = Fully integrated system. Pre-configured. Base configuration is power-on ready. No operating system installed

Important Note: Fully configured (operation ready, no operating system) L9 systems are only orderable from Intel using its online Configure-To-Order (CTO) tool at <u>orderconfigurator.intel.com</u> (Intel NDA required) or contact your Intel field sales representative.

1.2 Reference Documents and Support Collaterals

For additional information, see the product support collaterals specified in the following table. The following webpage provides support information for the Intel® Server D50TNP Family:

https://www.intel.com/content/www/us/en/support/products/201583.html

Table 1. Intel® Server D50TNP Family Reference Documents and Support Collaterals

Topic	Document Title or Support Collateral	Document Classification
Technical information about this product family	Intel® Server D50TNP Family Technical Product Specification	Public
System integration instructions and service guidance	Intel® Server D50TNP Family Integration and Service Guide	Public
Server configuration guidance and compatibility	Intel® Server D50TNP Family Configuration Guide	Public
Information on the Integrated BMC Web Console	Integrated Baseboard Management Controller Web Console (Integrated BMC Web Console) User Guide	Public
BIOS technical information on Intel® Server D50TNP Family	BIOS Firmware External Product Specification (EPS)	Intel Confidential
BIOS setup information on Intel® Server D50TNP Family	BIOS Setup Utility User Guide	Public
BMC technical information on Intel® Server D50TNP Family	Integrated Baseboard Management Controller Firmware External Product Specification (EPS)	Intel Confidential
Base specifications for the IPMI architecture and interfaces	Intelligent Platform Management Interface Specification Second Generation v2.0	Intel Confidential
Specifications for the PCIe* 3.0 architecture and interfaces	PCIe* Base Specification, Revision 3.0 http://www.pcisig.com/specifications	Public
Specifications for the PCle* 4.0 architecture and interfaces	PCIe* Base Specification, Revision 4.0 http://www.pcisig.com/specifications	Public
TPM for PC Client specifications	TCG PC Client Platform TPM Profile Specifications, Revision 2.0	Public
Functional specifications of 3 rd Gen Intel® Xeon® Scalable processor family	f 3 rd 3rd Generation Intel® Xeon® Scalable Processors, Codename Ice Lake-SP External Design Specification (EDS): Document IDs: 574451, 574942, 575291	
Processor thermal design specifications and recommendations	3rd Generation Intel® Xeon® Scalable Processor, Codename Ice Lake-SP and Cooper Lake-SP - Thermal and Mechanical Specifications and Design Guide (TMSDG): Document ID 574080	Intel Confidential
BIOS and BMC Security Best Practices	Intel® Server Systems Baseboard Management Controller (BMC) and BIOS Security Best Practices White Paper https://www.intel.com/content/www/us/en/support/articles/000055785/server-products.html	Public
Managing an Intel Server Overview	Managing an Intel Server System 2020 https://www.intel.com/content/www/us/en/support/articles/0000577 41/server-products.html	Public
For technical information on Intel® Optane™ persistent memory 200	Intel® Optane™ Persistent Memory 200 Series Operations Guide	Intel Confidential
Setup information for Intel® Optane™ persistent memory 200	intel® (Intane® Persistent Memon/ Startlin (-Iliae	
	Intel® System Update Package (SUP) for Intel® Server D50TNP Family	
Latest system software updates: BIOS and Firmware	Intel® Server Firmware Update Utility - Various operating system support	Public
	Intel® Server Firmware Update Utility User Guide	

Intel® Server D50TNP Family Technical Product Specification

Торіс	Document Title or Support Collateral	Document Classification
To obtain full system information	Intel® Server Information Retrieval Utility - Various operating system support	Public
	Intel® Server Information Retrieval Utility User Guide	
To configure, save, and restore	Intel® Server Configuration Utility - Various operating system support	Public
various system options	Intel® Server Configuration Utility User Guide	1 dbiic
Product Warranty Information	Warranty Terms and Conditions https://www.intel.com/content/www/us/en/support/services/00000 5886.html	Public
Intel® Data Center Manager (Intel®	Intel® Data Center Manager (Intel® DCM) Product Brief https://software.intel.com/content/www/us/en/develop/download/d cm-product-brief.html	Public
DCM) information	Intel® Data Center Manager (Intel® DCM) Console User Guide https://software.intel.com/content/www/us/en/develop/download/d cm-user-guide.html	Public

Note: Intel Confidential documents are made available under a nondisclosure agreement (NDA) with Intel and must be ordered through your local Intel representative.

2. Server Board Overview

This chapter provides an overview of the server board features and architecture. The Intel® Server Board D50TNP1SB and D50TNP1SBCR are purpose built, rack-optimized server boards ideal for use in HPC and AI applications. The architecture of the server boards is developed around the features and functions of the 3rd Gen Intel® Xeon® Scalable processor family.

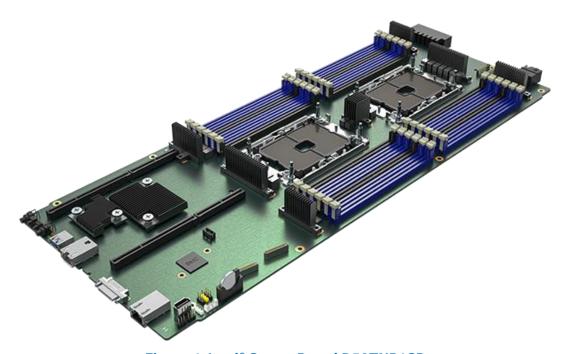


Figure 4. Intel® Server Board D50TNP1SB

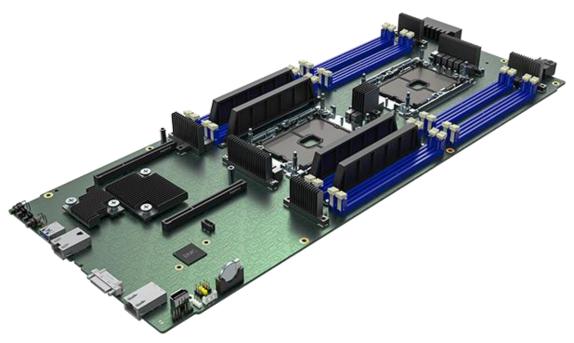


Figure 5. Intel® Server Board D50TNP1SBCR

2.1 Server Board Features Overview

See Table 2 for feature set specifications and Figure 6 and Figure 7 for feature identification.

Table 2. Intel® Server Boards D50TNP1SB and D50TNP1SBCR Feature Set

Feature	D50TNP1SB	D50TNP1SBCR	
Processor Support	 Dual Socket-P4 LGA4189 Supported 3rd Gen Intel® Xeon® Scalable processor family SKI Intel® Xeon® Platinum 8300 processor Intel® Xeon® Gold 6300 processor Intel® Xeon® Gold 5300 processor Intel® Xeon® Silver 4300 processor Intel® UPI links: three at 11.2 GT/s (Platinum and Gold SKUs) of the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the Supported 3rd Gen Intel® Xeon® Scalable processor SKUs in the State State	or two at 10.4 GT/s (Silver SKU)	
	processor SKUs are supported. Note: Previous generation Intel® Xeon® processor and Intel® Xeon® processor Scalable families are not supported.		
Maximum	• 3 rd Gen Intel® Xeon® Scalable processors up to 270 W (server Note: See Section 5.2.	board only)	
Processor Thermal Design Power (TDP)	Note: The maximum supported processor TDP at the system lever can support. Supported power, thermal, and configuration limits considered to determine if the system can support the maximum Refer to the server chassis/system documentation for additional	s of the chosen server chassis need to be n processor TDP limit of the server board.	
Chipset	 Intel® C621A Platform Controller Hub (PCH) chipset Embedded features enabled on this server board: SATA III support USB 3.0 support PCIe 3.0 support 		
Memory Support	 Up to 16 DDR4 DIMMs + up to 8 Intel® Optane™ persistent memory 200 series modules. See Chapter 6 for details. Registered DDR4 (RDIMM), 3DS-RDIMM, Load Reduced DDR4 (LRDIMM), 3DS-LRDIMM Note: 3DS = 3-dimensional stacking All DDR4 DIMMs must support ECC Up to 3200 MT/s memory data transfer rates Up to 2 TB DDR4 memory capacity for both processors (1 TB per processor), for all processor SKUs Up to 6 TB DDR4 and Intel® Optane™ PMem combined memory capacity for both processors (3 TB per processor), for all processor SKUs supporting both DDR4 and Intel® Optane™ PMem DDR4 standard voltage of 1.2 V Note: The speed supported depends on the installed 	Up to 16 DDR4 DIMMs Registered DDR4 (RDIMM), 3DS-RDIMM, Load Reduced DDR4 (LRDIMM), 3DS-LRDIMM Note: 3DS = 3-dimensional stacking All DDR4 DIMMs must support ECC Up to 3200 MT/s memory data transfer rates Up to 2 TB DDR4 memory capacity for both processors (1 TB per processor), for all processor SKUs DDR4 standard voltage of 1.2 V Note: The speed supported depends on the installed processor. See Chapter 6 for details.	
Front Panel Suppo	processor. See Chapter 6 for details.		
Tront Panet Suppt	One USB 3.0 port		
I/O Ports	 One I/O breakout cable connector supporting the following: Two USB 3.0 ports (dual-stack) One VGA connector (16 MB of DDR4 video memory) One serial port connector. The port follows Advanced Technology (AT) pinout specifications. Note: The I/O breakout cable is available as an accessory option (iPC: AXXCONNTDBG). 		
Networking	 One external 10GBASE-T Ethernet port (RJ45) One external dedicated 1000BASE-T Ethernet management p 		
LEDs	Module status Module ID		

Feature	D50TNP1SB	D50TNP1SBCR
Buttons Expansion Option	Power Module ID Module cold reset Non-maskable interrupt (NMI)	
Expansion Option		
Riser Slots	 Two riser slots on the server board: Riser Slot 1 x16 1U single PCIe* slot riser card option supporting PCIe* 4.0 lanes routed from CPU 0 x32 2U dual PCIe* slot riser card option supporting PCIe 4.0 lanes routed from CPU 0 and CPU 1 x4 SATA/PCIe NVMe* M.2 SSD option supporting PCIe 3.0 lanes routed from chipset Note: PCIe lanes routed from processor/chipset have Intel® VROC 7.5 (VMD NVMe RAID) support using Intel VROC key (accessory option) Riser Slot 2 x16 1U single PCIe slot riser card option supporting PCIe 4.0 lanes routed from CPU 1 x24 2U dual PCIe slot riser card option supporting PCIe 4.0 lanes routed from CPU 0 and CPU 1 x4 SATA/PCIe NVMe M.2 SSD option supporting PCIe 3.0 lanes routed from chipset Note: PCIe lanes routed from processor/chipset have Intel® VROC 7.5 (VMD NVMe RAID) support using Intel VROC key (accessory option) 	 Two riser slots on the server board: Riser Slot 1 x16 1U single PCIe slot riser card option supporting PCIe 4.0 lanes routed from CPU 0 x4 SATA/PCIe NVMe M.2 SSD option supporting PCIe 3.0 lanes routed from chipset Note: PCIe lanes routed from processor/chipset have Intel® VROC 7.5 (VMD NVMe RAID) support using Intel VROC key (accessory option) Riser Slot 2 x16 1U single PCIe slot riser card option supporting PCIe 4.0 lanes routed from CPU 1 x4 SATA/PCIe NVMe M.2 SSD option supporting PCIe 3.0 lanes routed from chipset Note: PCIe lanes routed from processor/chipset have Intel® VROC 7.5 (VMD NVMe RAID) support using Intel VROC key (accessory option)
Supported Onboa	ard Connectors and Headers	
PCIe* NVMe* Interface Support	 Four OCuLink connectors with x8 PCIe 4.0 lanes routed from CPU 0 Four OCuLink connectors with x8 PCIe 4.0 lanes routed from CPU 1 Note: PCIe lanes routed from processor/chipset have Intel® VROC (VMD NVMe RAID) support using Intel VROC key (accessory option) 	OCuLink connectors not available
USB Support	One USB 2.0 onboard type-A connector for internal use Important Note: Not all Intel Server Boards D50TNP1SB and D50TNP1SBCR ship with the USB 2.0 onboard type-A connector installed. Intel does not support requests to have this connector installed on Intel Server Boards D50TNP1SB and D50TNP1SBCR that are shipped without the connector.	
Security Support	 Intel® Platform Firmware Resilience (Intel® PFR) technology Intel® Total Memory Encryption (Intel® TME) Intel® Software Guard Extensions (Intel® SGX) Intel® CBnT – Converged Intel® Boot Guard and Trusted Executed Trusted platform module 2.0 (Rest of World) – iPC: AXXTPME Trusted platform module 2.0 (China Version) – iPC: AXXTPMC 	NC8 (accessory option)
Serviceability		
Server Management	 Integrated Baseboard Management Controller (BMC) Intelligent Platform Management Interface (IPMI) 2.0 compliant Redfish* compliant Support for Intel® Data Center Manager (Intel® DCM) Support for Intel® Server Debug and Provisioning Tool (Intel® One external dedicated 1000BASE-T Ethernet management points intel® Light-Guided Diagnostics included onboard LEDs 	SDP Tool)

Feature	D50TNP1SB	D50TNP1SBCR
Server Management Processor	 Aspeed* AST2500 Advanced PCIe Graphics and Remote Management Processor Embedded features enabled on this server board: Baseboard Management Controller (BMC) 2D Video Graphics Adapter 	
Onboard Configuration and Service Jumpers	 BIOS load defaults BIOS Password clear Intel® Management Engine (Intel® ME) firmware force update BMC force update BIOS Security Version Number (SVN) Downgrade BMC SVN Downgrade 	
BIOS	Unified Extensible Firmware Interface (UEFI)-based BIOS (legacy boot not supported)	
Module Support	 D50TNP1MHCPAC D50TNP2MHSVAC D50TNP2MHSTAC D50TNP2MFALAC See Table 3 for more information on Intel® D50TNP Modules. 	 D50TNP1MHCRAC D50TNP1MHEVAC D50TNP1MHCRLC See Table 3 for more information on Intel® D50TNP Modules.

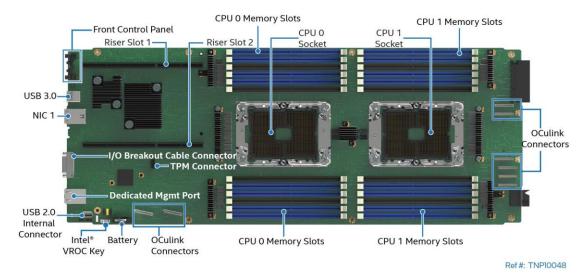


Figure 6. Intel® Server Board D50TNP1SB Feature Identification

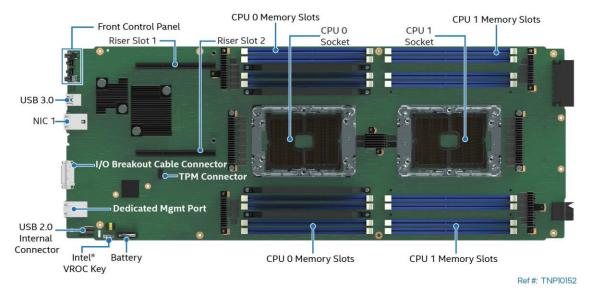


Figure 7. Intel® Server Board D50TNP1SBCR Feature Identification

The server boards include several jumper blocks to configure, protect, or recover specific features of the server board. The following figure identifies the location of each jumper header on the server board. Pin 1 of each jumper can be identified by the arrowhead (▼) silkscreened on the server board next to the pin. See Chapter 15 for details on how to use each jumper.

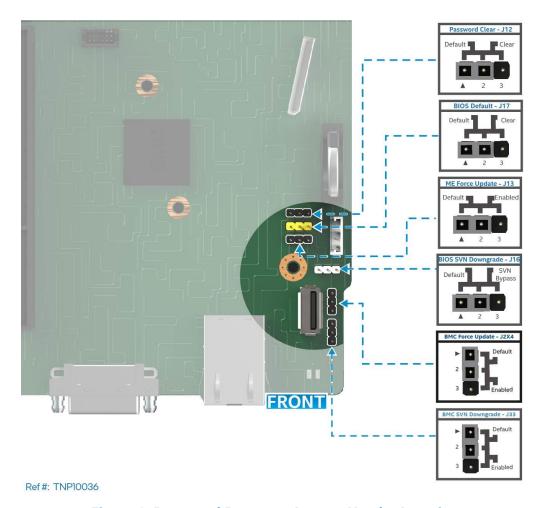


Figure 8. Reset and Recovery Jumper Header Location

A bank of eight POST code diagnostic LEDs is on the front edge of the server board (see following figure). During the boot process, the BIOS executes many module configuration steps, each of which is assigned a specific hex POST code number. As each configuration step is started, the BIOS displays the given POST code to the POST code diagnostic LEDs. The purpose of these LEDs is to assist in troubleshooting a system hang condition during the POST process. The diagnostic LEDs can be used to identify the last POST process executed. See Appendix C for a complete description of how these LEDs are read, and for a list of all supported POST codes.

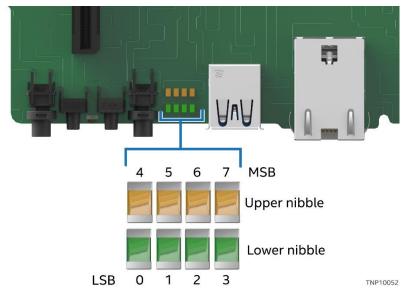


Figure 9. Onboard LED Location

The power and module and ID buttons are located next to the onboard LEDs as shown in the above figure. These buttons have integrated LEDs. See Section 9.1 for details.

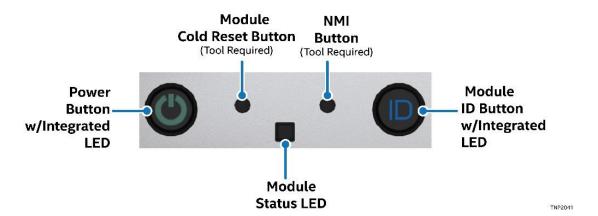


Figure 10. Front Control Panel Features

2.2 PCI Express (PCIe*)

The PCI Express (PCIe) interfaces on the Intel® Server D50TNP Family are fully compliant with the *PCIe Base Specification, Revision 4.0* supporting the following PCIe bit rates: 4.0 (16 GT/s), 3.0 (8.0 GT/s), 2.0 (5.0 GT/s), and 1.0 (2.5 GT/s). The interfaces supporting M.2 connectors from the Platform Controller Hub (PCH) chipset are fully compliant with the *PCIe Base Specification, Revision 3.0* supporting the following PCIe bit rates: 3.0 (8.0 GT/s), 2.0 (5.0 GT/s), and 1.0 (2.5 GT/s). For details on PCI Express, see Chapter 7.

2.3 Server Board Architecture

The architectures of the Intel® Server Boards D50TNP1SB and D50TNP1SBCR are developed around the integrated features and functions of the 3rd Gen Intel® Xeon® Scalable processor family, the Intel® C621A Platform Controller Hub (PCH) chipset, Intel® Ethernet Controller X550, and the ASPEED* AST2500 Server Management Processor (SMP).

The following figures provide an overview of the Intel® Server Boards D50TNP1SB and D50TNP1SBCR architecture, showing the features and interconnects of each of the major subsystem components.

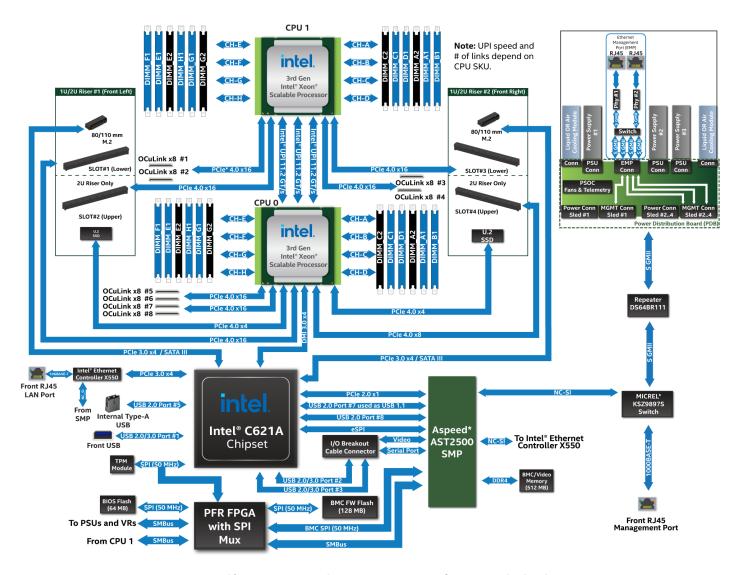


Figure 11. Intel® Server Board D50TNP1SB Architectural Block Diagram

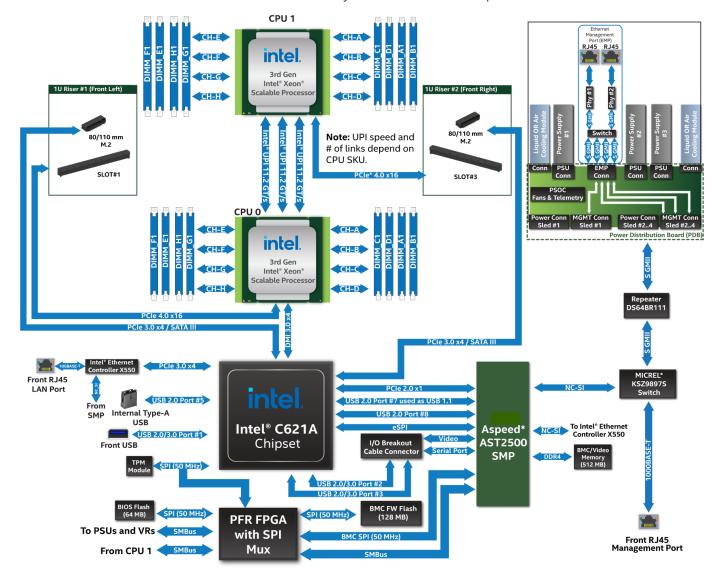


Figure 12. Intel® Server Board D50TNP1SBCR Architectural Block Diagram

2.4 Server Board Additional Information

Additional board-only information is in the following appendices.

- Mechanical Dimension Diagrams (see Appendix B)
- Server Board Mechanical Drawings (see Appendix F)
- Server Board Installation and Component Replacement (see Appendix H)

Pinout definitions for server board connectors and headers are only made available by obtaining the board schematics directly from Intel (NDA required).

3. Intel[®] D50TNP Modules Overview

The Intel® Server D50TNP Family offers a variety of modules that address different workloads in today's modern data centers. From liquid-cooled processor hungry to storage heavy to accessory flexible, available D50TNP module options are available to support each of these workload criteria. This chapter provides an overview of the functions and supported features of each module supported by the Intel® Server D50TNP Family.



Figure 13. Chassis with Empty Module Bay

Each module in a system configuration is independently operated from the others. The installed modules in a system chassis share resources like power and cooling. The following table describes the different ways that an Intel® Server System D50TNP can be configured.

For additional information regarding configuration options, see the *Intel® Server D50TNP Family Configuration Guide*.

Module Type	iPC	Height	Width	Cooling	Maximum Processor Thermal Design Power (TDP) ¹	Modules per Chassis	
	D50TNP1MHCPAC	10		205 W	205 W		
C	D50TNP1MHCRAC		111 11616.	ملغام المراجع المراجع	Air cooled	205 W	Up to four
Compute	D50TNP1MHEVAC		1U Half width	ir wiatn	270 W		
	D50TNP1MHCRLC			Liquid cooled	270 W	Up to four	
Management	D50TNP2MHSVAC	2U	Half width	Air cooled	270 W	Up to two	
Storage	D50TNP2MHSTAC	2U	Half width	Air cooled	205 W	Up to two	
Accelerator	D50TNP2MFALAC	2U	Full width	Air cooled	270 W	One	

Table 3. Intel® D50TNP Modules

Note 1: See Appendix E for detailed information on TDP.

Mixing different types of modules in the same chassis can be done as follows:

- Up to two 1U air-cooled Compute Modules with one 2U Management Module
- Up to two 1U air-cooled Compute Modules with one 2U Storage Module
- One 2U Management Module with one 2U Storage Module

The Intel® Server Board D50TNP1SB and D50TNP1SBCR are at the heart of the modules in the product family, supporting 3rd Gen Intel® Xeon® Scalable processors. Each module type supports a different feature set in terms of type of cooling, storage options, memory options, and PCIe add-in card support. The following subsections provide details about the differentiation that each module provides.

3.1 1U Compute Module

The Compute Modules are 1U, half-width modules. A common 2U system supports up to four Compute Modules for maximum density and performance. The Compute Modules are available for air-cooled or liquid-cooled configurations. Air-cooled Compute Modules have either regular processor heat sinks or Enhanced Volume Air Cooling (EVAC) processor heat sinks for improved maximum processor Thermal Design Power (TDP).

Note: Mixing liquid-cooled modules with air-cooled modules in a single system is not supported.

Note: Mixing 1U air-cooled Compute Module with regular processor heat sinks and 1U Compute Module with EVAC processor heat sinks in a single system is not supported.



Figure 14. Air-Cooled (Standard Heat Sinks Shown) and Liquid-Cooled Compute Modules

1U Compute Modules include the Intel® Server Board D50TNP1SB or D50TNP1SBCR with support for dual 3rd Gen Intel® Xeon® Scalable processors, and up to 16 DDR4 DIMMs + up to 8 Intel® Optane™ persistent memory 200 series modules (depending on configuration).

Each module includes two riser card assemblies. Each riser card assembly supports a single, x16 PCIe 4.0 add-in card slot compatible with low-profile PCIe add-in cards. Each riser assembly also includes support for a single 80/110 mm PCIe or SATA M.2 SSD storage device.

Important Note: D50TNP1MHEVAC does not support a low-profile PCIe 4.0 add-in card because the EVAC extension occupies this space. M.2 SSD is still supported on Riser Slot 2.

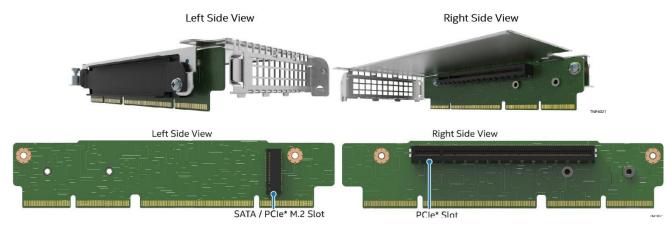


Figure 15. 1U Riser Card Assembly (D50TNP1MHCPAC)

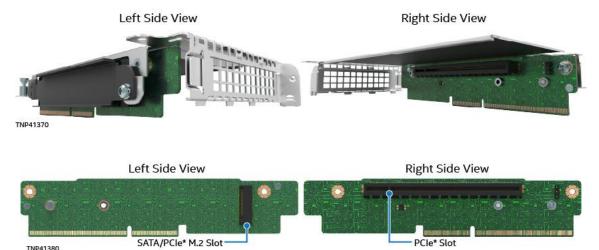


Figure 16. 1U Riser Card Assembly (D50TNP1MHCRAC, D50TNP1MHCRLC, and D50TNP1MHEVAC)

3.1.1 Supported Features

The following table provides the Compute Module supported features.

Table 4. Compute Module Supported Features

Feature	D50TNP1MHCPAC	D50TNP1MHCRAC, D50TNP1MHCRLC, D50TNP1MHEVAC
Processor Support	 Dual Socket-P4 LGA4189 Supported 3rd Gen Intel® Xeon® Scalable processor family SKUs: Intel® Xeon® Platinum 8300 processor Intel® Xeon® Gold 6300 processor Intel® Xeon® Gold 5300 processor Intel® Xeon® Silver 4300 processor Intel® UPI links: three at 11.2 GT/s (Platinum and Gold SKUs) or two at 10.4 GT/s (Silver SKU) Note: Supported 3rd Gen Intel® Xeon® Scalable processor SKUs must Not end in (H), (L), or (U). All other processor SKUs are supported. Note: Previous generation Intel® Xeon® processor and Intel® Xeon® Scalable processor families are not supported. 	
Maximum Processor Thermal Design Power (TDP)	 Up to 270 W (D50TNP1MHCRLC and D50TNP1MHEVAC) Up to 205 W (D50TNP1MHCPAC and D50TNP1MHCRAC) Note: See Appendix E for details. 	
Chipset	 Intel® C621A Platform Controller Hub (PCH) chipset Embedded features enabled on this server board: SATA III support USB 3.0 support PCIe 3.0 support 	

Feature	D50TNP1MHCPAC	D50TNP1MHCRAC, D50TNP1MHCRLC, D50TNP1MHEVAC	
Memory Support	 Up to 16 DDR4 DIMMs + up to 8 Intel® Optane™ persistent memory 200 series modules Registered DDR4 (RDIMM), 3DS-RDIMM, Load Reduced DDR4 (LRDIMM), 3DS-LRDIMM Note: 3DS = 3-dimensional stacking All DDR4 DIMMs must support ECC Intel® Optane™ persistent memory 200 series module (air-cooled systems only) Up to 3200 MT/s memory data transfer rates Up to 2 TB DDR4 memory capacity for both processors (1 TB per processor), for all processor SKUs Up to 6 TB DDR4 and Intel® Optane™ PMem combined memory capacity for both processor (3 TB per processor), for all processor SKUs supporting both DDR4 and Intel® Optane™ PMem DDR4 standard voltage of 1.2 V Note: The speed supported depends on the installed processor. See Chapter 6 for details. 		
Storage Support	Via riser assemblies: Two M.2 SATA/PCIe* NVMe* SSDs with PCIe* 3.0 lanes routed from chipset Note: PCIe lanes routed from processor/chipset have Intel® VROC 7.5 (VMD NVMe RAID) support using Intel VROC key (accessory option).		
Front Panel			
I/O Ports	 One USB 3.0 port One I/O breakout cable connector supporting the fo Two USB 3.0 ports (dual-stack) One VGA connector (16 MB of DDR4 video memo One serial port connector. The port follows AT pin Note: The I/O breakout cable is available as an access 	ry) out specifications	
Networking	One external 10GBASE-T Ethernet port (RJ45) One external dedicated 1000BASE-T Ethernet mana	gement port (RJ45)	
LEDs	Module status Module ID		
Buttons	Power Module ID Module cold reset Non-maskable interrupt (NMI)		
Expansion Option	is		
Riser Slot 1	Riser Slot 1 supports 1U single PCIe* slot riser card assembly (iPC: TNP1URISER) PCIe slot (CPU 0): low-profile PCIe 4.0 (x16 mechanical, x16 electrical) M.2 slot (chipset): 80/110 mm SATA/PCIe 3.0 NVMe	Riser Slot 1 supports 1U single PCIe* slot riser card assembly (iPC: TNP1UCRRISER) PCIe slot (CPU 0): low-profile PCIe 4.0 (x16 mechanical, x16 electrical) M.2 slot (chipset): 80/110 mm SATA/PCIe 3.0 NVMe	

Feature	D50TNP1MHCPAC	D50TNP1MHCRAC, D50TNP1MHCRLC, D50TNP1MHEVAC	
Riser Slot 2	Riser Slot 2 supports 1U single PCIe* slot riser card assembly (iPC: TNP1URISER) PCIe slot (CPU 1): low-profile PCIe 4.0 (x16 mechanical, x16 electrical) M.2 slot (chipset): 80/110 mm SATA/PCIe 3.0 NVMe Note: The PCIe slots in 1U riser cards provide up to 25 W of power.	Riser Slot 2 supports 1U single PCIe* slot riser card assembly (iPC: TNP1UCRRISER) PCIe slot (CPU 1): low-profile PCIe 4.0 (x16 mechanical, x16 electrical) M.2 slot (chipset): 80/110 mm SATA/PCIe 3.0 NVMe Note: The PCIe slots in 1U riser cards provide up to 25 W of power. Important Note: D50TNP1MHEVAC does not support a low-profile PCIe 4.0 add-in card because the EVAC extension occupies this space. M.2 SSD is still supported on Riser Slot 2.	
Supported Onboa	ard Connectors and Headers		
USB Support	One USB 2.0 onboard type-A connector for internal use Important Note: Not all Compute Modules ship with the USB 2.0 onboard type-A connector installed on the server board. Intel does not support requests to have this connector installed on Compute Module server boards that are shipped without the connector.		
Security Support	 Intel® Platform Firmware Resilience (Intel® PFR) technology Intel® Total Memory Encryption (Intel® TME) Intel® Software Guard Extensions (Intel® SGX) Intel® CBnT – Converged Intel® Boot Guard and Trusted Execution Technology (Intel® TXT) Trusted platform module 2.0 (Rest of World) – iPC AXXTPMENC8 (accessory option) Trusted platform module 2.0 (China Version) – iPC AXXTPMCHNE8 (accessory option) 		
Serviceability	- Trusted platform module 2.0 (china version) in e AVVIII Pierrite (accessory option)		
Server Management	• Support for Intel® Data Center Manager (Intel® DCM)		
Server Management Processor	 Aspeed* AST2500 Advanced PCIe Graphics and Remote Management Processor Embedded features enabled on this server board: Baseboard Management Controller (BMC) 2D Video Graphics Adapter 		
Onboard Configuration and Service Jumpers	 BIOS load defaults BIOS Password clear Intel® Management Engine (Intel® ME) firmware force update BMC force update BIOS SVN Downgrade BMC SVN Downgrade For more information, see Chapter 15. 		
BIOS	Unified Extensible Firmware Interface (UEFI) -based BIOS (legacy boot not supported)		

3.1.2 Feature Identification

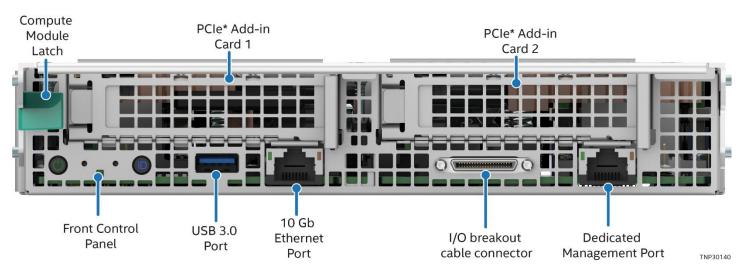


Figure 17. 1U Compute Module Front Panel Features

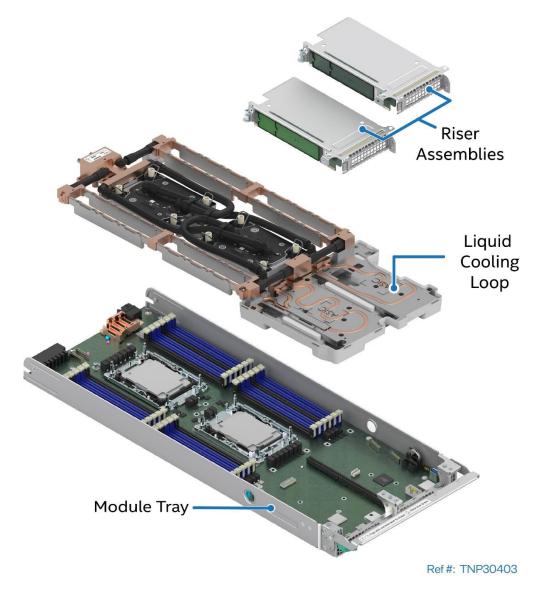


Figure 18. 1U Liquid-Cooled Compute Module Components

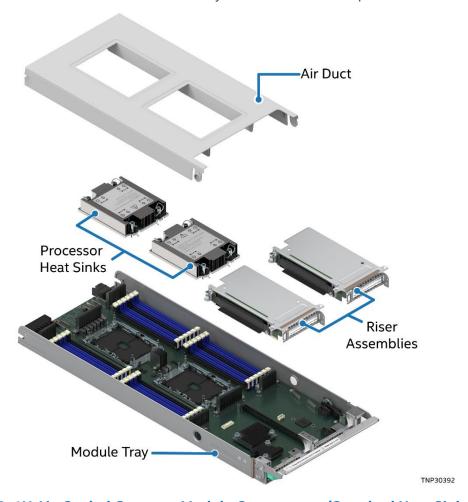


Figure 19. 1U Air-Cooled Compute Module Components (Standard Heat Sinks Shown)

3.1.3 Dimensions

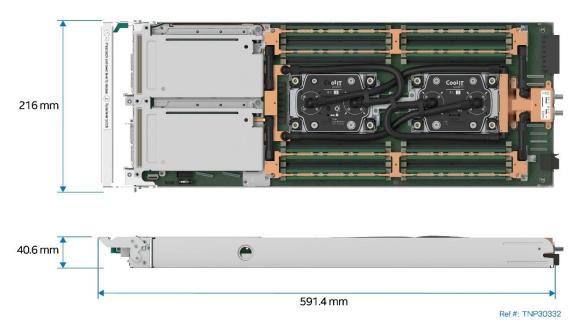


Figure 20. 1U Liquid-Cooled Compute Module Dimensions

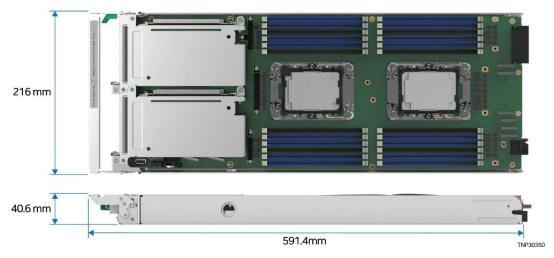


Figure 21. 1U Air-Cooled Compute Module Dimensions

3.2 2U Management Module

The Management Modules are 2U, half-width modules. A common 2U system supports up to two Management Modules for maximum density and performance. The Management Modules are available for air-cooled configurations.

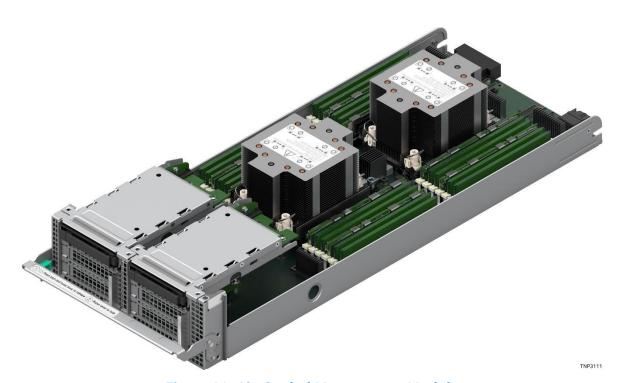


Figure 22. Air-Cooled Management Module

2U Management Modules include the Intel® Server Board D50TNP1SB with support for dual 3rd Gen Intel® Xeon® Scalable processors, and up to 16 DDR4 DIMMs + up to 8 Intel® Optane™ persistent memory 200 series modules. Each module includes two riser card assemblies.

Each riser card assembly supports a dual, x16 PCIe 4.0 add-in card slot compatible with low-profile PCIe add-in cards. Each riser assembly also includes support for a NVMe U.2 SSD and a single 80/110 mm PCIe or SATA M.2 SSD storage device.

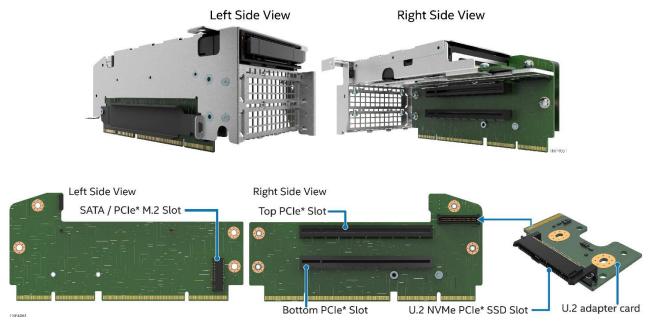


Figure 23. 2U Riser Card Assembly

3.2.1 Supported Features

The following table provides the Management Module supported features.

Table 5. Management Module Supported Features

Feature	Description	
Processor Support	o litter Acon Silver 4300 processor	
Maximum Processor Thermal Design Power (TDP)	Up to 270 W Note: See Appendix E for details.	
Chipset	 Intel® C621A Platform Controller Hub (PCH) chipset Embedded features enabled on this server board: SATA III support USB 3.0 support PCIe 3.0 support 	

Feature	Description				
Memory Support	 Up to 16 DDR4 DIMMs + up to 8 Intel® Optane™ persistent memory 200 series modules (air cooled) Registered DDR4 (RDIMM), 3DS-RDIMM, Load Reduced DDR4 (LRDIMM), 3DS-LRDIMM Note: 3DS = 3-Dimensional stacking All DDR4 DIMMs must support ECC Intel® Optane™ persistent memory 200 series modules (air-cooled systems only) Up to 3200 MT/s memory data transfer rates Up to 2 TB DDR4 memory capacity for both processors (1 TB per processor), for all processor SKUs Up to 6 TB DDR4 and Intel® Optane™ PMem combined memory capacity for both processors (3 TB per processor), for all processor SKUs supporting both DDR4 and Intel® Optane™ PMem DDR4 standard voltage of 1.2 V Note: The speed supported depends on the installed processor. See Chapter 6 for details. 				
	Via riser assemblies:				
Storage Support	 Two M.2 SATA/PCIe NVMe SSDs with PCIe 3.0 lanes routed from chipset Two hot-swap 2.5" U.2 PCIe NVMe SSDs with PCIe 4.0 lanes routed from CPU 0 Note: PCIe lanes routed from processor/chipset have Intel® VROC 7.5 (VMD NVMe RAID) support using Intel 				
	VROC key (accessory option).				
Front Panel	O ve HICD 2 O ve et				
 One USB 3.0 port One I/O breakout cable connector supporting the following: Two USB 3.0 ports (dual-stack) One VGA connector (16 MB of DDR4 video memory) One serial port connector. The port follows AT pinout specifications. Note: The I/O breakout cable is available as an accessory option (iPC: AXXCONNTDBG). 					
Networking	 One external 10GBASE-T Ethernet port (RJ45) One external dedicated 1000BASE-T Ethernet management port (RJ45) 				
LEDs	Module statusModule ID				
Buttons	 Power Module ID Module cold reset Non-maskable interrupt (NMI) 				
Expansion Options					
Riser Slot 1	Riser Slot 1 supports 2U dual PCIe* slot riser card assembly (iPC: TNP2URISER) Top Slot (CPU 0): low-profile PCIe 4.0 (x16 mechanical, x16 electrical) Bottom Slot (CPU 1): low-profile PCIe 4.0 (x16 mechanical, x16 electrical) NVMe U.2 SSD slot (CPU 0): x4 PCIe 4.0 M.2 slot (chipset): 80/110 mm SATA/PCIe 3.0 NVMe				
Riser Slot 2	Riser Slot 2 supports 2U dual PCIe* slot riser card assembly (iPC: TNP2URISER) • Top Slot (CPU 0): low-profile PCIe 4.0 (x16 mechanical, x8 electrical) • Bottom Slot (CPU 1): low-profile PCIe 4.0 (x16 mechanical, x16 electrical) • NVMe U.2 SSD slot (CPU 0): x4 PCIe 4.0 • M.2 slot (chipset): 80/110 mm SATA/PCIe 3.0 NVMe Note: The PCIe slots in 2U riser cards provide up to 25 W of power.				
Supported Onboar	d Connectors and Headers				
	One USB 2.0 onboard type-A connector for internal use				
USB Support	Important Note : Not all Management Modules ship with the USB 2.0 onboard type-A connector installed on the server board. Intel does not support requests to have this connector installed on Management Module server boards that are shipped without the connector.				

Feature	Description					
Security Support	 Intel® Platform Firmware Resilience (Intel® PFR) technology Intel® Total Memory Encryption (Intel® TME) Intel® Software Guard Extensions (Intel® SGX) Intel® CBnT – Converged Intel® Boot Guard and Trusted Execution Technology (Intel® TXT) Trusted platform module 2.0 (Rest of World) – iPC AXXTPMENC8 (accessory option) Trusted platform module 2.0 (China Version) – iPC AXXTPMCHNE8 (accessory option) 					
Serviceability						
Server Management	 Integrated Baseboard Management Controller (BMC) Intelligent Platform Management Interface (IPMI) 2.0 compliant Redfish* compliant Support for Intel® Data Center Manager (Intel® DCM) Support for Intel® Server Debug and Provisioning Tool (Intel® SDP Tool) One external dedicated 1000BASE-T Ethernet management port (RJ45) Intel® Light-Guided Diagnostics included onboard LEDs 					
Server Management Processor	 Aspeed* AST2500 Advanced PCIe Graphics and Remote Management Processor Embedded features enabled on this server board: Baseboard Management Controller (BMC) 2D Video Graphics Adapter 					
Onboard Configuration and Service Jumpers	 BIOS load defaults BIOS Password clear Intel® Management Engine (Intel® ME) firmware force update BMC force update BIOS SVN Downgrade BMC SVN Downgrade For more information, see Chapter 15. 					
BIOS	Unified Extensible Firmware Interface (UEFI) -based BIOS (legacy boot not supported)					

3.2.2 Feature Identification

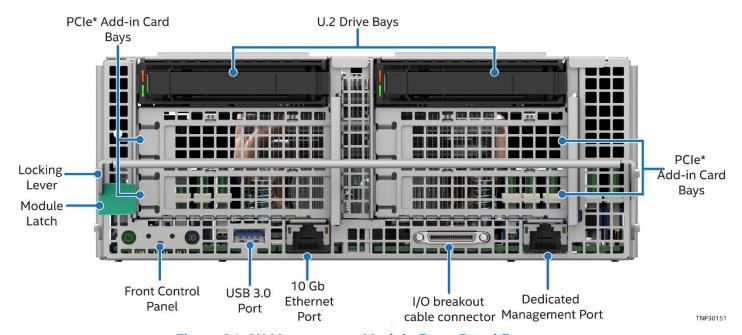


Figure 24. 2U Management Module Front Panel Features

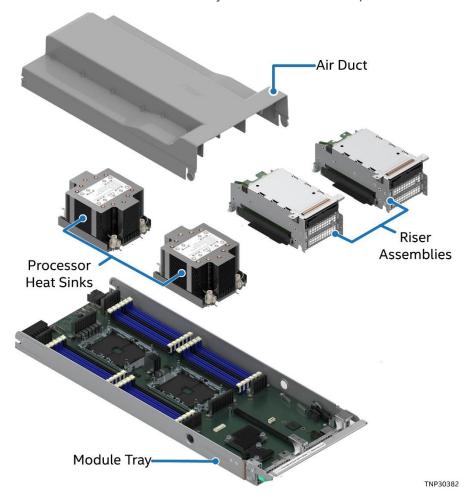


Figure 25. 2U Management Module Components

3.2.3 Dimensions

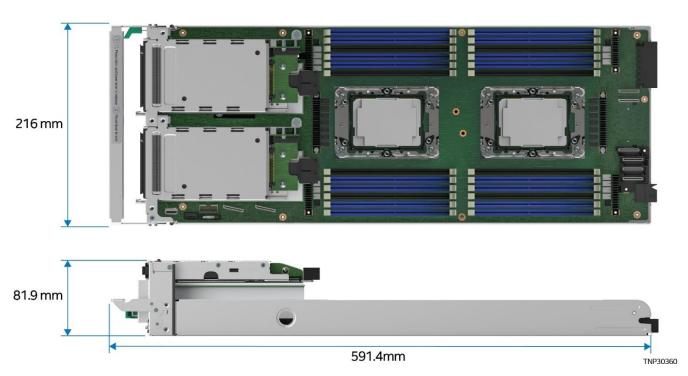


Figure 26. 2U Management Module Dimensions

3.3 2U Storage Module

The Storage Modules are 2U, half-width modules intended for dense and fast storage solutions. The Storage Module supports up to two SATA or PCIe M.2 storage SSDs and can support up to 16 full-length (E1.L) Enterprise and Datacenter SSD Form Factor (EDSFF) NVMe SSDs. They provide the fastest storage interface and maximum storage capacity available in a single high density module. The Storage Modules are available for air-cooled configurations.

Note: Enterprise and Data Center SSD Form Factor (EDSFF) is a revolutionary industry standard storage form factor that provides high capacity, thermal efficiency, and full serviceability.



Figure 27. Air-Cooled Storage Module

Each Storage Module supports riser assemblies that go into the base of the module while the upper part houses the enterprise data center SSD form factor (EDSFF) units.

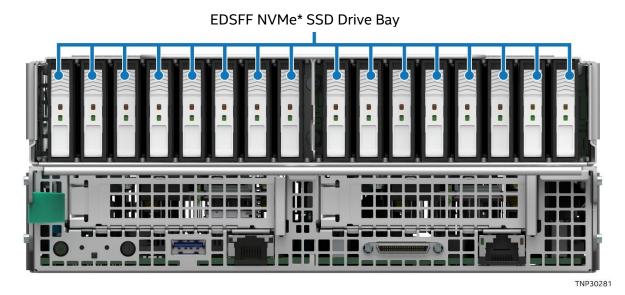


Figure 28. EDSFF NVMe* Drive Bay - 2U Storage Modules

40

Intel® Server D50TNP Family Technical Product Specification

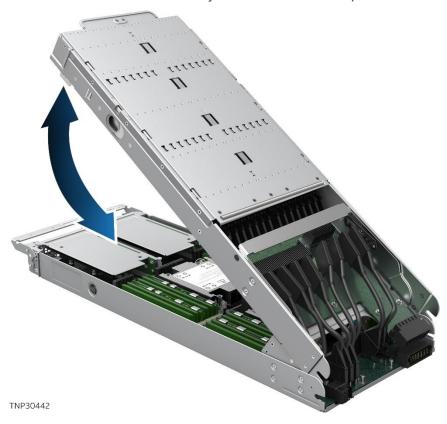


Figure 29. Air-Cooled Storage Module -- Service View

2U Storage Modules include the Intel® Server Board D50TNP1SB with support for dual 3rd Gen Intel® Xeon® Scalable processors, and up to 16 DDR4 DIMMs + up to 8 Intel® Optane™ persistent memory 200 series modules. Each module includes two riser card assemblies.

Each riser card assembly supports a single, x16 PCIe 4.0 add-in card slot compatible with low-profile PCIe add-in cards. Each riser assembly also includes support for a single 80/110 mm PCIe or SATA M.2 SSD storage device.

Up to 16 full-length 1U PCIe NVMe EDSFFs can be installed in the Storage Module.

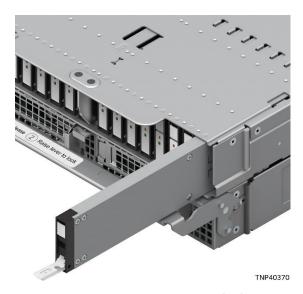


Figure 30. EDSFF NVMe* SSD in Air-Cooled Storage Module

Each EDSFF NVMe SSD in the Storage Module is hot-swappable and connected to a docking board. The docking board is connected to the server board through high-performance OCuLink cables inside the module.

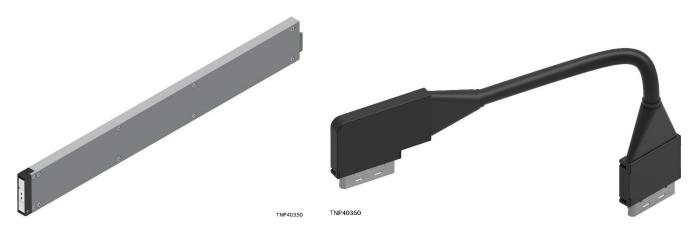


Figure 31. EDSFF NVMe* SSD and OCuLink Cable

Both M.2 and EDSFF NVMe SSD storage solutions support Intel® VROC 7.5 (VMD NVMe RAID) using an Intel® VROC key (accessory option). See Chapter 7 for detailed information.

3.3.1 Supported Features

The following table provides the Storage Module supported features.

Table 6. Storage Module Supported Features

Feature	Description					
Processor Support	 Dual Socket-P4 LGA4189 Supported 3rd Gen Intel® Xeon® Scalable processor family SKUs: Intel® Xeon® Platinum 8300 processor Intel® Xeon® Gold 6300 processor Intel® Xeon® Gold 5300 processor Intel® Xeon® Silver 4300 processor Intel® UPI links: three at 11.2 GT/s (Platinum and Gold SKUs) or two at 10.4 GT/s (Silver SKU) Note: Supported 3rd Gen Intel® Xeon® Scalable processor SKUs must Not end in (H), (L), or (U). All other processor SKUs are supported. Note: Previous generation Intel® Xeon® processor and Intel® Xeon® Scalable processor families are not supported. 					
Maximum Processor Thermal Design Power (TDP)	Up to 205 W Note: See Appendix E for details.					
Chipset	 Intel® C621A Platform Controller Hub (PCH) chipset Embedded features enabled on this server board: SATA III support USB 3.0 support PCIe 3.0 support 					

Feature	Description					
Memory Support	 Up to 16 DDR4 DIMMs + up to 8 Intel® Optane™ persistent memory 200 series modules (air cooled) Registered DDR4 (RDIMM), 3DS-RDIMM, Load Reduced DDR4 (LRDIMM), 3DS-LRDIMM Note: 3DS = 3-dimensional stacking All DDR4 DIMMs must support ECC Intel® Optane™ persistent memory 200 series module (air-cooled systems only) Up to 3200 MT/s memory data transfer rates Up to 2 TB DDR4 memory capacity for both processors (1 TB per processor), for all processor SKUs Up to 6 TB DDR4 and Intel® Optane™ PMem combined memory capacity for both processors (3 TB per processor), for all processor SKUs supporting both DDR4 and Intel® Optane™ PMem DDR4 standard voltage of 1.2 V Note: The speed supported depends on the installed processor. See Chapter 6 for details. 					
Storage Support	 Via riser assemblies: Two M.2 SATA/PCle* NVMe* SSDs with PCle 3.0 lanes routed from chipset Note: PCle lanes routed from processor/chipset have Intel® VROC 7.5 (VMD NVMe RAID) support using Intel VROC key (accessory option). Via onboard connectors: Sixteen full-length PCle NVMe EDSFF SSDs with PCle 4.0 lanes routed from CPU 0 / CPU 1 Note: PCle lanes routed from processor/chipset have Intel® VROC 7.5 (VMD NVMe RAID) support using Intel VROC key (accessory option). 					
Front Panel						
I/O Ports	 One USB 3.0 port One I/O breakout cable connector supporting the following: Two USB 3.0 ports (dual-stack) One VGA connector (16 MB of DDR4 video memory) One serial port connector. The port follows AT pinout specifications Note: The I/O breakout cable is available as an accessory option (iPC: AXXCONNTDBG). 					
Networking	 One external 10GBASE-T Ethernet port (RJ45) One external dedicated 1000BASE-T Ethernet management port (RJ45) 					
LEDs	Module status Module ID					
Buttons	Power Module ID Module cold reset Non-maskable interrupt (NMI)					
Expansion Options						
Riser Slot 1	 Riser Slot 1 supports 1U single PCIe* slot riser card assembly (iPC: TNP1URISER) PCIe slot (CPU 0): low-profile PCIe 4.0 (x16 mechanical, x16 electrical) M.2 slot (chipset): 80/110 mm SATA/ PCIe 3.0 NVMe 					
Riser Slot 2	 Riser Slot 2 supports 1U single PCIe* slot riser card assembly (iPC: TNP1URISER) PCIe slot (CPU 1): low-profile PCIe 4.0 (x16 mechanical, x16 electrical) M.2 slot (chipset): 80/110 mm SATA/ PCIe 3.0 NVMe Note: The PCIe slots in 1U riser cards provide up to 25 W of power. 					
Supported Onboard	d Connectors and Headers					
Onboard NVMe* Interface Support	 Four OCuLink connectors with x8 PCIe 4.0 lanes routed from CPU 0. Four OCuLink connectors with x8 PCIe 4.0 lanes routed from CPU 1 Note: Each connector supports up to two EDSFF NVMe SSDs through the docking board. Note: PCIe lanes routed from processor/chipset have Intel® VROC (VMD NVMe RAID) support using Intel VROC key (accessory option) 					

Feature	Description					
USB Support	One USB 2.0 onboard type-A connector for internal use Important Note: Not all Storage Modules ship with the USB 2.0 onboard type-A connector installed on the server board. Intel does not support requests to have this connector installed on Storage Module server boards that are shipped without the connector.					
Security Support	 Intel® Platform Firmware Resilience (Intel® PFR) technology Intel® Total Memory Encryption (Intel® TME) Intel® Software Guard Extensions (Intel® SGX) Intel® CBnT – Converged Intel® Boot Guard and Trusted Execution Technology (Intel® TXT) Trusted platform module 2.0 (Rest of World) – iPC AXXTPMENC8 (accessory option) Trusted platform module 2.0 (China Version) – iPC AXXTPMCHNE8 (accessory option) 					
Serviceability						
Server Management	 Integrated Baseboard Management Controller (BMC) Intelligent Platform Management Interface (IPMI) 2.0 compliant Redfish compliant Support for Intel® Data Center Manager (Intel® DCM) Support for Intel® Server Debug and Provisioning Tool (Intel® SDP Tool) One external dedicated 1000BASE-T Ethernet management port (RJ45) Intel® Light-Guided Diagnostics included onboard LEDs 					
Server Management Processor	 Aspeed* AST2500 Advanced PCIe Graphics and Remote Management Processor Embedded features enabled on this server board: Baseboard Management Controller (BMC) 2D Video Graphics Adapter 					
Onboard Configuration and Service Jumpers	 BIOS load defaults BIOS Password clear Intel® Management Engine (Intel® ME) firmware force update BMC force update BIOS SVN Downgrade BMC SVN Downgrade For more information, see Chapter 15. 					
BIOS	Unified Extensible Firmware Interface (UEFI) -based BIOS (legacy boot not supported)					

3.3.2 Feature Identification

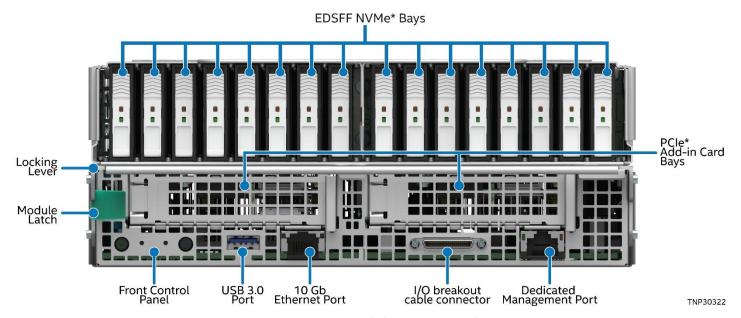


Figure 32. 2U Storage Module Front Panel Features

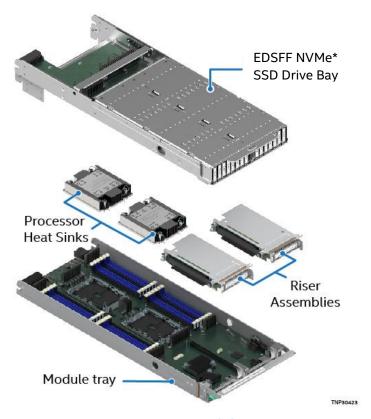


Figure 33. 2U Storage Module Components

3.3.3 Dimensions

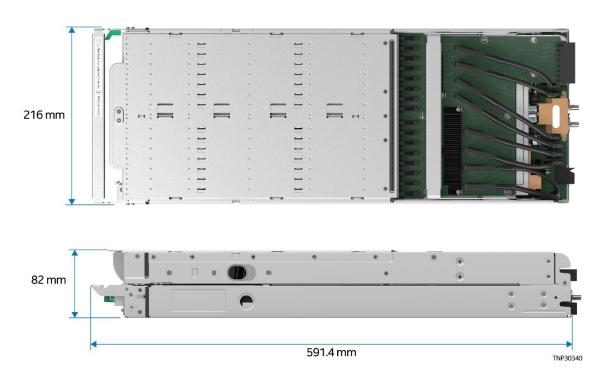


Figure 34. 2U Storage Module Dimensions

3.4 2U Accelerator Module

The Accelerator Modules are 2U, full-width modules intended to address acceleration solutions. The module includes two riser card assemblies along with the addition of four x16 full height, full length, double width PCIe slots that support up to four 300 W PCIe accelerator add-in cards. The Accelerator Modules are available for air-cooled configurations.

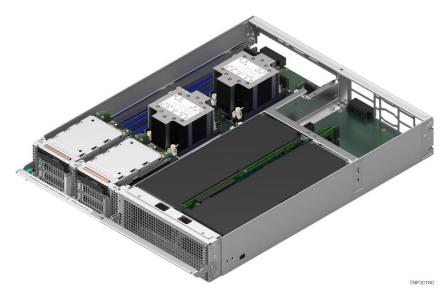


Figure 35. Air-Cooled Accelerator Module

The Accelerator Module supports up to eight PCIe add-in cards. Two riser assemblies support four low profile x16 PCIe add-in cards, and two additional accelerator riser cards support four full length / full height, double wide X16 PCIe accelerator add-in cards. The following figure shows the front view of the accelerator riser card 2.

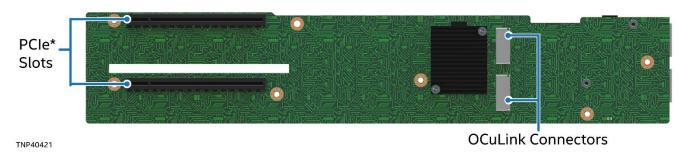


Figure 36. Accelerator Module Riser Card 2 - Front View

The accelerator riser cards are connected to the base board using onboard OCuLink connectors.

The Intel® D50TNP Accelerator Modules support three types of accelerator add-in cards:

- Nvidia* Tesla* V100
- Nvidia* Tesla* A100
- Programmable Acceleration Card with the Intel® Stratix® 10 SX FPGA

Note: Installation of mixed types in a single module is not supported.

All accelerator add-in cards are connected directly to the server system power supplies using a power connector board. The same power connector board also supplies the power to the two accelerator riser cards. The following figure shows the power connector board in the Intel® D50TNP Accelerator Modules.

Intel® Server D50TNP Family Technical Product Specification

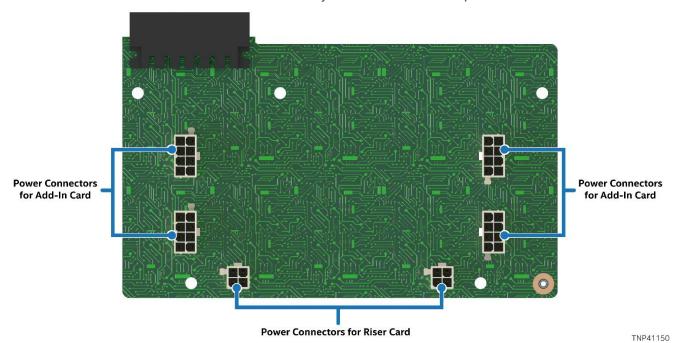


Figure 37. Power Connector Board for Accelerator Module

2U Accelerator Modules include the Intel® Server Board D50TNP1SB with support for dual 3rd Gen Intel® Xeon® Scalable processors, and up to 16 DDR4 DIMMs + up to 8 Intel® Optane™ persistent memory 200 series modules.

Each module includes two riser card assemblies. Each riser card assembly supports a dual, x16 PCIe 4.0 add-in card slot compatible with low-profile PCIe add-in cards. Each riser assembly also includes support for a NVMe U.2 SSD and a single 80/110 mm PCIe or SATA M.2 SSD storage device.

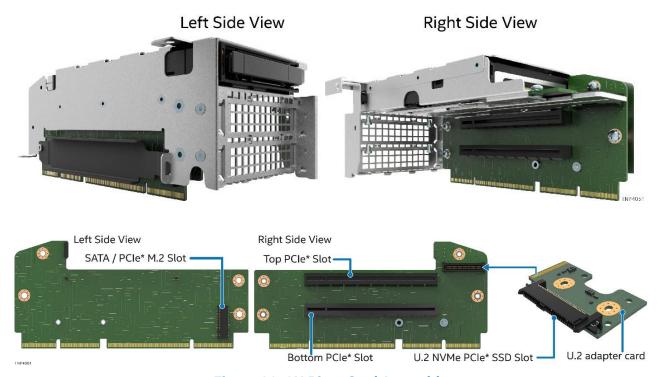


Figure 38. 2U Riser Card Assembly

3.4.1 Supported Features

The following table provides the Accelerator Module supported features.

Table 7. Accelerator Module Supported Features

Feature	Description					
Processor Support	 Dual Socket-P4 LGA4189 Supported 3rd Gen Intel® Xeon® Scalable processor family SKUs: Intel® Xeon® Platinum 8300 processor Intel® Xeon® Gold 6300 processor Intel® Xeon® Gold 5300 processor Intel® Xeon® Silver 4300 processor Intel® UPI links: three at 11.2 GT/s (Platinum and Gold SKUs) or two at 10.4 GT/s (Silver SKU) Note: Supported 3rd Gen Intel® Xeon® Scalable processor SKUs must Not end in (H), (L), or (U). All other processor SKUs are supported. Note: Previous generation Intel® Xeon® processor and Intel® Xeon® Scalable processor families are not supported. 					
Maximum Processor Thermal Design Power (TDP)	Up to 270 W Note: See Appendix E for details.					
Chipset	 Intel® C621A Platform Controller Hub (PCH) chipset Embedded features enabled on this server board: SATA III support USB 3.0 support PCIe 3.0 support 					
Memory Support	 Up to 16 DDR4 DIMMs + up to 8 Intel® Optane™ persistent memory 200 series modules (air cooled) Registered DDR4 (RDIMM), 3DS-RDIMM, Load Reduced DDR4 (LRDIMM), 3DS-LRDIMM Note: 3DS = 3-dimensional stacking All DDR4 DIMMs must support ECC Intel® Optane™ persistent memory 200 series module (air-cooled systems only) Up to 3200 MT/s memory data transfer rates Up to 2 TB DDR4 memory capacity for both processors (1 TB per processor), for all processor SKUs Up to 6 TB DDR4 and Intel® Optane™ PMem combined memory capacity for both processors (3 TB per processor), for all processor SKUs supporting both DDR4 and Intel® Optane™ PMem DDR4 standard voltage of 1.2 V Note: The speed supported depends on the installed processor. See Chapter 6 for details. 					
Storage Support	Via riser assemblies: • Two M.2 SATA/PCIe* NVMe* SSDs with PCIe* 3.0 lanes routed from chipset • Two hot-swap 2.5" U.2 PCIe NVMe SSDs with PCIe 4.0 lanes routed from CPU 0 Note: PCIe lanes routed from processor/chipset have Intel® VROC 7.5 (VMD NVMe RAID) support using Intel VROC key (accessory option).					
Front Panel						
I/O Ports	 One USB 3.0 port One I/O breakout cable connector supporting the following: Two USB 3.0 ports (dual-stack) One VGA connector (16 MB of DDR4 video memory) One serial port connector. The port follows AT pinout specifications Note: The I/O breakout cable is available as an accessory option (iPC: AXXCONNTDBG). 					
Networking	 One external 10GBASE-T Ethernet port (RJ45) One external dedicated 1000BASE-T Ethernet management port (RJ45) 					
LEDs	Module statusModule ID					

Feature	Description					
Buttons	 Power Module ID Module cold reset Non-maskable interrupt (NMI) 					
Expansion Options	Expansion Options					
Riser Slot 1	Riser Slot 1 supports 2U dual PCIe* slot riser card assembly (iPC: TNP2URISER) Top Slot (CPU 0): low-profile PCIe 4.0 (x16 mechanical, x16 electrical) Bottom Slot (CPU 1): low-profile PCIe 4.0 (x16 mechanical, x16 electrical) NVMe U.2 SSD slot (CPU 0): x4 PCIe 4.0 M.2 slot (chipset): 80/110 mm SATA/PCIe 3.0 NVMe					
Riser Slot 2	Riser Slot 2 supports 2U dual PCIe* slot riser card assembly (iPC: TNP2URISER) Top Slot (CPU 0): low-profile PCIe 4.0 (x16 mechanical, x8 electrical) Bottom Slot (CPU 1): low-profile PCIe 4.0 (x16 mechanical, x16 electrical) NVMe U.2 SSD slot (CPU 0): x4 PCIe 4.0 M.2 slot 2 (chipset): 80/110 mm SATA/PCIe 3.0 NVMe Note: The PCIe slots in 2U riser cards provide up to 25 W of power.					
Accelerator Riser 1	 2U full-length, dual PCIe* slot riser card (iPC: TNPACCLRISER1) Slot top (CPU 1): FHFL, double-width PCIe 4.0 (x16 mechanical, x16 electrical) Slot bottom (CPU 1): FHFL, double-width PCIe 4.0 (x16 mechanical, x16 electrical) 					
Accelerator Riser 2	 2U full-length, dual PCIe* slot riser card (iPC: TNPACCLRISER2) Slot top (CPU 0): FHFL, double-width PCIe 4.0 (x16 mechanical, x16 electrical) Slot bottom (CPU 0): FHFL, double-width PCIe 4.0 (x16 mechanical, x16 electrical) 					
Supported Onboar	d Connectors and Headers					
Onboard NVMe* Interface Support	 Four OCuLink connectors with x8 PCIe 4.0 lanes routed from CPU 0 Four OCuLink connectors with x8 PCIe 4.0 lanes routed from CPU 1 Note: PCIe lanes routed from processor/chipset have Intel® VROC (VMD NVMe RAID) support using Intel VROC key (accessory option) 					
USB Support	One USB 2.0 onboard type-A connector for internal use Important Note: Not all Accelerator Modules ship with the USB 2.0 onboard type-A connector installed on the server board. Intel does not support requests to have this connector installed on Accelerator Module server boards that are shipped without the connector.					
Security Support	 Intel® Platform Firmware Resilience (Intel® PFR) technology Intel® Total Memory Encryption (Intel® TME) Intel® Software Guard Extensions (Intel® SGX) Intel® CBnT – Converged Intel® Boot Guard and Trusted Execution Technology (Intel® TXT) Trusted platform module 2.0 (Rest of World) – iPC AXXTPMENC8 (accessory option) Trusted platform module 2.0 (China Version) – iPC AXXTPMCHNE8 (accessory option) 					
Serviceability						
Server Management	 Integrated Baseboard Management Controller (BMC) Intelligent Platform Management Interface (IPMI) 2.0 compliant Redfish* compliant Support for Intel® Data Center Manager (Intel® DCM) Support for Intel® Server Debug and Provisioning Tool (Intel® SDP Tool) One external dedicated 1000BASE-T Ethernet management port (RJ45) Intel® Light-Guided Diagnostics included onboard LEDs 					
Server Management Processor	 Aspeed* AST2500 Advanced PCIe Graphics and Remote Management Processor Embedded features enabled on this server board: Baseboard Management Controller (BMC) 2D Video Graphics Adapter 					

Feature	Description			
Onboard Configuration and Service Jumpers	 BIOS load defaults BIOS Password clear Intel® Management Engine (Intel® ME) firmware force update BMC force update BIOS SVN Downgrade BMC SVN Downgrade For more information, see Chapter 15. 			
BIOS	Unified Extensible Firmware Interface (UEFI) -based BIOS (legacy boot not supported)			

3.4.2 Feature Identification

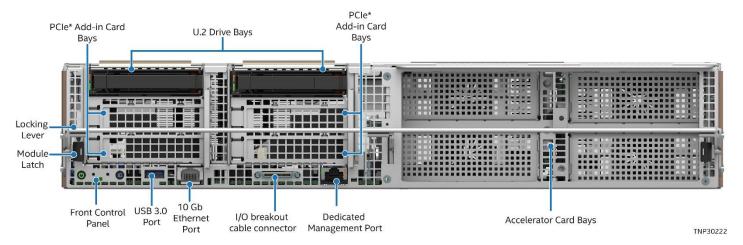


Figure 39. 2U Accelerator Module Front Panel Features

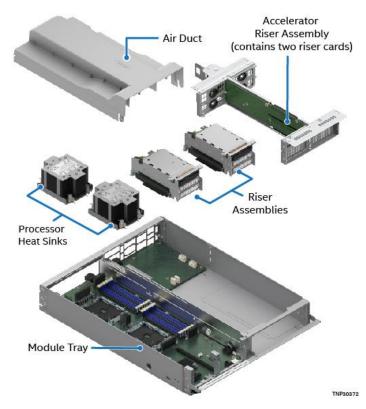


Figure 40. 2U Accelerator Module Components

3.4.3 Dimensions

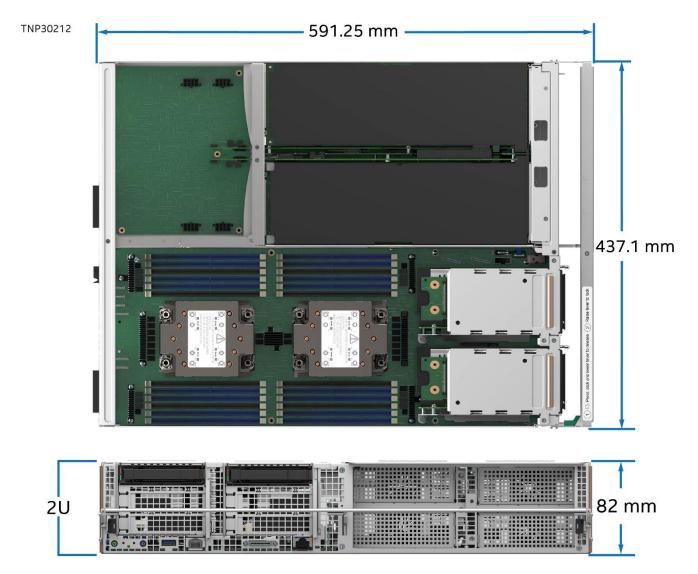


Figure 41. 2U Accelerator Module Dimensions

4. System / Chassis Overview

This chapter provides an overview of the system and chassis features, dimensions, and environmental and packaging specifications.

4.1 System / Chassis Features

The Intel® Server D50TNP Family offers options for custom configuration and self-integration to custom fully configured and integrated power on ready system solutions. A power-on ready system can include chassis, modules, power supplies, cooling components, and rails for rack or cabinet mounting. The modules are preconfigured and independent, allowing for a power-on ready installation, with configurable memory, storage, and network component options. The Intel Server D50TNP Family offers systems for liquid-cooled and air-cooled configurations. See the Intel® Server D50TNP Family Configuration Guide for a complete list of available options.

As a building block, the Intel® Server D50TNP Family includes four Intel® Server chassis FC2000 products. These four chassis-only products are listed below.

- 2U Half-width configuration, liquid cooled, 2100 W PSU chassis iPC FC2HLC21W3
 - Supports up to four 1U half-width modules (liquid cooled)
- 2U Half-width configuration, air cooled, 2100 W PSU chassis iPC FC2HAC21W3
 - Supports up to four 1U half-width modules (air cooled)
 - Supports up to two 2U half-width modules (air cooled)
 - o Supports one 2U half-width module and two 1U half-width modules (air cooled)
- 2U Half-width configuration, air cooled, 1600 W PSU chassis iPC FC2HAC16W3
 - Supports up to two 2U half-width modules (air cooled)
- 2U Full-width configuration, air cooled, 1600 W PSU chassis iPC FC2FAC16W3
 - Supports one 2U full-width module (air cooled)

See Table 8 for a feature list of system and chassis-only features.



Figure 42. Example of Intel® Server System D50TNP

Table 8. Intel® Server Chassis / Intel® Server System D50TNP Feature Set

	Description					
Feature	Chassis SKU iPC FC2HLC21W3	Chassis SKU iPC FC2HAC21W3	Chassis SKU iPC FC2HAC16W3	Chassis SKU iPC FC2FAC16W3		
Chassis Definition	FC2000 half-width configuration, Liquid Cooled (2100 W)	FC2000 half-width configuration, Air Cooled (2100 W)	FC2000 half-width configuration, Air Cooled (1600 W)	FC2000 full-width configuration, Air Cooled (1600 W)		
Chassis Type	2U, rack-mount, multi-mo	odule		2U rack-mount, single module		
Chassis Dimensions	• 865 x 441.8 x 86.8 mm					
Packaging Dimensions	• 1192 x 758 x 317 mm	(L x W x H)				
Supported Intel® D50TNP Modules	Up to four 1U half-width modules (liquid cooled)	 Up to four 1U half-width modules (air cooled) One 2U half-width module and two 1U half-width modules (air cooled) Up to two 2U half-width modules (air cooled) 	Up to two 2U half-width modules (air cooled)	One 2U full-width Accelerator Module		
Cooling	Liquid-cooled configurations: • Three 60 x 60 x 56 mm dual-rotor hotswap system fans with support for fan redundancy one fan per installed power supply unit (PSU) Air-cooled configurations: • Five dual-rotor hot-swap system fans with support for fan redundancy one fan per installed power supply unit (PSU) • Cooled configurations: • Five dual-rotor hot-swap system fans with support for fan redundancy one fan per installed power supply unit (PSU)					
Power	PSU Three 2100 W AC power supplies with power redundancy support (dependent on system configuration). Three 1600 W AC power supplies with power redundancy support (dependent on system configuration).					
Rack Mount Kit (FCXXRAILKIT)	Tool-less installation Fixed position Note: Rack mount kit is included with chassis.					
Serviceability	Modular chassis features for simplified serviceability: Fully independent Intel® D50TNP Modules Hot-swap power supplies Hot-swap system fans Hot-swap U.2 solid state drive (SSD) storage (dependent on Intel® D50TNP Module) Hot-swap full-length PCIe NVMe EDSFF SSDs (dependent on Intel® D50TNP Module)					
Operating Temperature	10–35 °C ambient temperature					
Server Management	Optional Ethernet Management Port (EMP) to remotely manage the Intel® D50TNP Modules					

4.2 System Feature Identification

All systems feature front loading modules. The following illustrations provide system views for all supported system configurations.

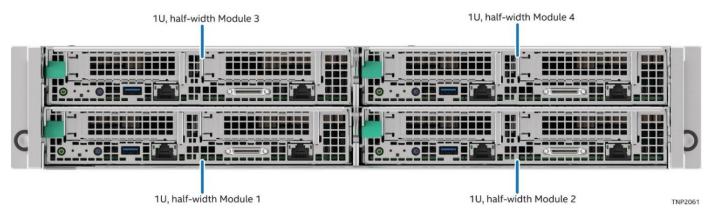


Figure 43. Module Identification for Four-Module System Configuration Chassis IPCs: FC2HLC21W3, FC2HAC21W3, FC2HAC16W3



Figure 44. Module Identification for Two-Module System Configuration Chassis IPCs: FC2HLC21W3, FC2HAC21W3, FC2HAC16W3

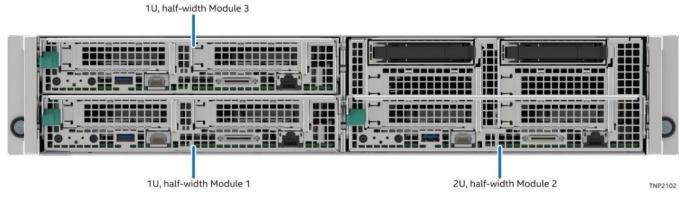


Figure 45. Module Identification for Three-Module System Configuration Chassis IPCs: FC2HLC21W3, FC2HAC21W3, FC2HAC16W3

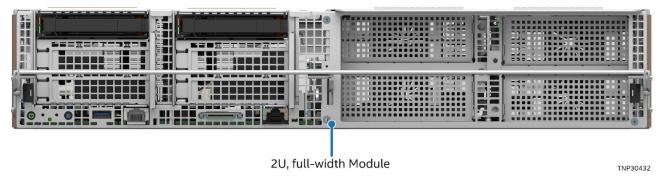


Figure 46. Module Identification for One-Module System Configuration
Chassis IPC: FC2FAC16W3

Systems are offered with either liquid-cooling or air-cooling options. The following illustrations identify key system features for both cooling options.

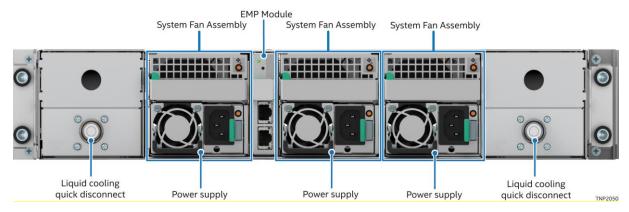


Figure 47. Liquid-Cooled System Back View



Figure 48. Air-Cooled System Back View

4.3 Rack and Cabinet Mounting Kit

The Intel® Server System D50TNP supports a fixed rail kit for installation into a four-post rack or cabinet. Features and specifications for the rail kit are listed below:

- iPC FCXXRAILKIT- Fixed Rail Kit
 - Tool-less installation
 - Maximum supported weight: 150 kg (330 lbs.)

Safety Note: Due to the weight of a fully configured system, Intel recommends the following: Use a mechanical lift to aid with the installation of the system into the rack, and/or use at least two people to install the system into the rack, or remove all installed modules from the system before attempting to install the system into a rack or cabinet.

4.4 System / Chassis Level Environmental Limits

The following table defines the system level operating and non-operating environmental limits.

Table 9. System Environmental Limits Summary

Para	meter	Limits				
Temperature	Operating	ASHRAE Class A2 – Continuous Operation. 10–35 °C (50–95 °F) with the maximum rate of change not to exceed 10 °C per hour. ASHRAE Class A3 – Includes operation up to 40 °C for up to 900 hrs. per year. ** ASHRAE Class A4 – Includes operation up to 45 °C for up to 90 hrs. per year. **				
	Non-Operating	-40 through 70 °C (-40 through 158 °F)				
Altitude	Operating	Support operation up to 3050 m with ASHRAE class de-ratings.				
Humidity	Shipping	50% to 90%, non-condensing with a maximum wet bulb of 28 °C (at temperatures 25–35 °C)				
	Operating	Half sine, 2 g, 11 msec				
Shock	Unpackaged	Trapezoidal, 25 g, velocity change is based on packaged weight				
	Packaged	ISTA (International Safe Transit Association) Test Procedure 3A 2008				
Wile we did no	Unpackaged	5–500 Hz, 2.20 g RMS random				
Vibration	Packaged	ISTA (International Safe Transit Association) Test Procedure 3A 2008				
	Voltage	200–240 V				
	Frequency	47–63 Hz				
	Source Interrupt	No loss of data for power line drop-out of 12 msec				
AC-DC	Surge Non- operating and operating	Unidirectional				
	Line to earth Only	AC Leads 2.0 kV I/O Leads 1.0 kV DC Leads 0.5 kV				
	Air Discharged	12.0 kV				
ESD	Contact Discharge	8.0 kV				
A	Power	<300 W ≥300 W ≥600 W ≥1000 W				
Acoustics Sound Power Measured	Servers/Rack Mount Sound Power Level	7.0 BA 7.0 BA 7.0 BA				
Projected Sound	Maximum	~ 8.9 BA				
Power (environmental	Active	~ 7.7 BA				
condition: 23 °C ±2 °C)	Idle	~ 6.5 BA				

Note: ** For system configuration requirements and limitations, See Appendix E in this document and an online power calculator tool accessible at the following Intel web site: https://servertools.intel.com/tools/power-calculator/ **Disclaimer:** Intel server boards contain and support several high-density VLSI and power delivery components that need adequate airflow to cool and remain within their thermal operating limits. Intel ensures through its own chassis development and testing that when an Intel server board and Intel chassis are used together, the fully integrated system meets the thermal requirements of these components. It is the responsibility of the system architect or system integrator who chooses to develop their own server system using an Intel server board and a non-Intel chassis, to consult relevant specifications and datasheets to determine thermal operating limits and necessary airflow to support intended system configurations and workloads when the system is operating within target ambient temperature limits. It is also their responsibility to perform adequate environmental validation testing to ensure reliable system operation. Intel cannot be held responsible if components fail or the server board does not operate correctly when published operating and nonoperating limits are exceeded.

4.5 System / Chassis Packaging

The original Intel packaging is designed to provide protection to a fully configured system and tested to meet International Safe Transit Association (ISTA) Test Procedure 3A (2018). The packaging is designed to be re-used for shipment after system integration has been completed.

The original packaging includes two layers of boxes – an inner box and the outer shipping box – and various protective inner packaging components. The boxes and packaging components are designed to function together as a protective packaging system. When reused, all of the original packaging material must be used, including both boxes and each inner packaging component. In addition, all inner packaging components must be reinstalled in the proper location to ensure adequate protection of the system for subsequent shipment.

Note: The design of the inner packaging components does not prevent improper placement in the packaging assembly. Only one correct packaging assembly allows the package to meet the ISTA Test Procedure 3A (2018) limits. See the *Intel® Server D50TNP Family Integration and Service Guide* for complete packaging assembly instructions.

Failure to follow the specified packaging assembly instructions may result in damage to the system during shipment.

Outer shipping box external dimensions

o Length: 46.93" (1192 mm)

o Breadth: 29.84" (758 mm)

Height: 12.48" (317 mm)

• Inner box internal dimension

o Length: 46.22" (1174 mm)

o Breadth: 29.21" (742 mm)

Height: 11.30" (287 mm)

5. Processor Support

The Intel® Server D50TNP Family includes two Socket-P4 LGA4189 server board processor sockets compatible with the 3rd Gen Intel® Xeon® Scalable processor family. This chapter provides information on processor heat sinks, thermal design power (TDP), and population rules. The chapter also provides a processor family overview.

Note: Previous-generation Intel® Xeon® processors and Intel® Xeon® Scalable processor families and their supported processor heat sinks are not compatible with server boards described in this document.

5.1 Processor Cooling Overview

The server board includes two processor socket assemblies, each consisting of a processor socket and bolster plate. The factory installed bolster plate is secured to the server board and is generally used to align the processor cooling hardware over the processor socket and secure it to the server board.

Processor cooling options in a server system may use a passive or active heat sink that use airflow to dissipate heat generated by the processors. Other processor cooling options may use liquid cooling plates, where cool liquid is pumped through the cooling plates to dissipate the heat from the processor.

For air cooled systems, the processor and heat sink are generally preassembled into a single Processor Heatsink Module (PHM) before being installed onto the processor socket assembly. The PHM concept reduces the risk of damaging pins in the processor socket during the processor installation process.

Note: The Intel Server D50TNP Family does not support active air-cooled heat sinks.

A PHM assembly consists of a processor, a processor carrier clip, and the processor heat sink. The following figure identifies each component associated with the PHM and processor socket assembly (1U heat sink shown in figure).

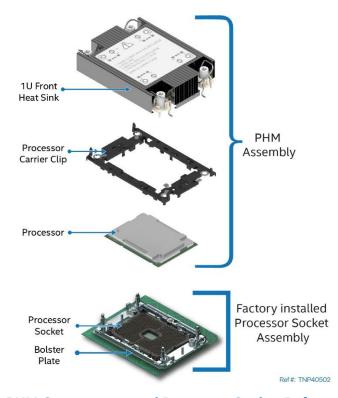


Figure 49. PHM Components and Processor Socket Reference Diagram

Note: For detailed processor assembly and installation instructions, see the *Intel® Server D50TNP Family Integration and Service Guide*.

5.1.1 Processor Cooling Requirements

For the server system to support optimal operation and long-term reliability, the thermal management solution of the selected server chassis and module must dissipate enough heat generated from within the chassis to keep the processors and other system components within their specified thermal limits.

For optimal operation and long-term reliability, processors in the 3rd Gen Intel® Xeon® Scalable processor family must operate within their defined minimum and maximum case temperature (T_{CASE}) limits. Refer to the 3rd Gen Intel® Xeon® Processor Scalable Family – Thermal Mechanical Specifications and Design Guide (TMSDG) for additional information concerning processor thermal limits.

Note: It is the responsibility of the system and components architects to ensure compliance with the processor thermal specifications. Compromising processor thermal requirements will impact the processor performance and reliability.

For air-cooled heat sink solutions, see the following section. For Intel's liquid cooling solution, see Section 10.6.

5.1.2 Processor Heat Sink (Air Cooled)

Intel® Server D50TNP Family supports 1U height heat sinks and 2U height heat sinks as shown in the following figures. The Compute Module uses 1U height heat sinks. Even though the Storage Module is a 2U height module, it uses the 1U height heat sinks. The Management Module and Accelerator Module use 2U height heat sinks.

As the following figures show, the available options are: two types of 2U heat sinks and three types of 1U heat sinks – front heat sink, back heat sink, and Enhanced Volume Air Cooling (EVAC) heat sink (front position only). The front heat sink type is used for CPU 0 and the back heat sink type is used for CPU 1. The exploded views in the figures show the difference. The back heat sink types have more heat venting fins.

Note: Heat sinks are not interchangeable. The descriptions above must be followed.

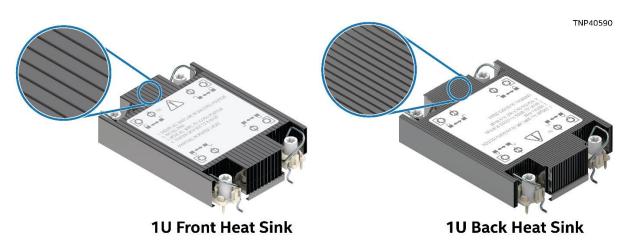
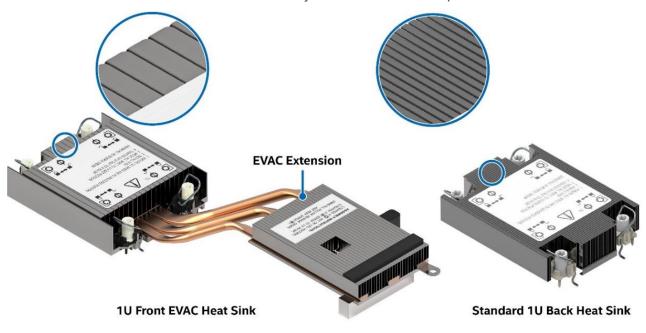


Figure 50. 1U Supported Regular Processor Heat Sinks

The EVAC heat sink is only used in the front for CPU 0. The Compute Module supporting the EVAC heat sink uses standard back heat sink for CPU 1.



Ref #: TNP41531

Figure 51. 1U Supported EVAC Processor Heat Sinks

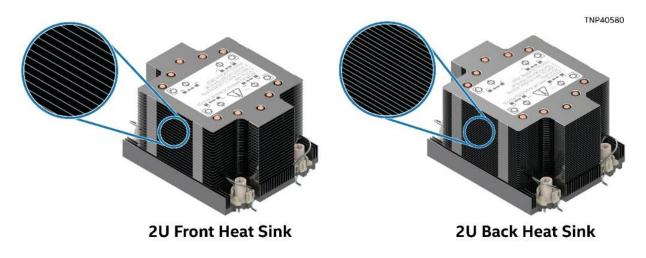


Figure 52. 2U Supported Processor Heat Sinks

The following figure shows a module with 1U front and back heat sinks installed. Only 1U standard front heat sink and 1U back heat sink are shown. However, the concept applies to modules using 1U EVAC front heat sink and 1U back heat sink or 2U front heat sink and 2U back heat sink.

Intel® Server D50TNP Family Technical Product Specification

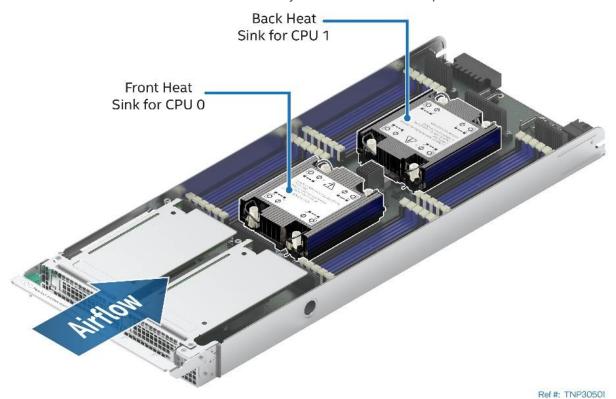


Figure 53. 1U Heat Sinks Installed in Module

5.2 Processor Population Rules

When two processors are installed, the following population rules apply:

- Both processors must have identical extended family, extended model number and processor type
- Both processors must have the same number of cores
- Both processors must have the same cache sizes for all levels of processor cache memory
- Both processors must support identical DDR4 memory frequencies

Note: Processors with different steppings can be mixed in a system as long as the rules mentioned above are met.

Population rules are applicable to any combination of processors in the 3rd Gen Intel® Xeon® Scalable processor family.

For additional information on processor population rules, see the *BIOS Firmware External Product Specification (EPS)*.

Note: The server board may support dual-processor configurations consisting of different processors that meet the defined criteria. However, Intel does not perform validation testing of this configuration. In addition, Intel does not ensure that a server system configured with unmatched processors will operate reliably. The system BIOS attempts to operate with processors that are not matched but are generally compatible. For optimal system performance in dual-processor configurations, Intel recommends that identical processors be installed.

5.3 Processor Thermal Design Power (TDP) Support

Electrically, the Intel® Server Board D50TNP supports processors in the 3rd Gen Intel® Xeon® Scalable processor family that support a maximum thermal design power (TDP) of 270 W.

Note: The maximum supported processor TDP at the system level may be lower than what the server board can support. Supported power, thermal, and configuration limits of the chosen server chassis / system need to be considered to determine if the system can support the maximum processor TDP limit of the server board or not. Refer to the chosen server chassis/system documentation for additional processor support guidance.

Depending on the system module and configuration, the Intel® Server System D50TNP may support a TDP up to and including 270 W. For details, see Appendix E.

5.4 Processor Family Overview

The supported 3rd Gen Intel® Xeon® Scalable processor family processor shelves are identified as shown in the following figure.

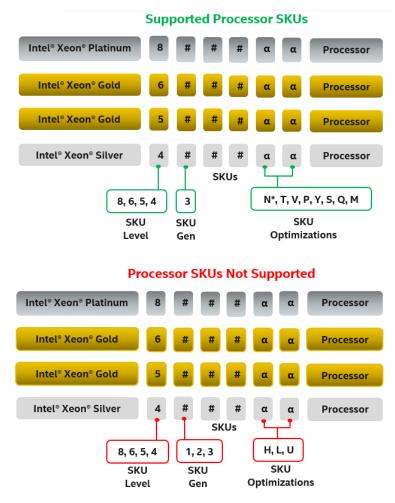


Figure 54. 3rd Gen Intel® Xeon® Scalable Processor Identification

Note: Supported 3rd Gen Intel® Xeon® Scalable processor SKUs must Not end in (H), (L), or (U). All other processor SKUs are supported.

* **Note:** The 8351N SKU is a single-socket optimized SKU and is not supported on the Intel® Server D50TNP Family.

Intel® Server D50TNP Family Technical Product Specification

Table 10. 3rd Gen Intel® Xeon® Scalable Processor Family Feature Comparison

Feature	Platinum 8300 Processors	Gold 6300 Processors	Gold 5300 Processors	Silver 4300 Processor
# of Intel® UPI Links	3	3	3	2
Intel® UPI Speed	11.2 GT/s	11.2 GT/s	11.2 GT/s	10.4 GT/s
Supported Topologies	2S-2UPI 2S-3UPI	2S-2UPI 2S-3UPI	2S-2UPI 2S-3UPI	2S-2UPI
Node Controller Support	No	No	No	No
Processor RAS Capability	Advanced	Advanced	Advanced	Standard
# of DDR4 Integrated Memory Controllers (IMC)	4	4	4	4
# DDR4 Channels	8	8	8	8
Intel® Turbo Boost Technology	Yes	Yes	Yes	Yes
Intel® HT Technology	Yes	Yes	Yes	Yes
Intel® AVX-512 ISA Support	Yes	Yes	Yes	Yes
Intel® AVX-512 - # of 512b FMA Units	2	2	2	2
# of PCle* Lanes	64	64	64	64
Intel® VMD 2.0	Yes	Yes	Yes	Yes

Note: Feature may vary between processor SKUs.

See the 3rd Gen Intel® Xeon® Scalable processor specifications and product briefs for additional information.

6. System Memory

This chapter describes the architecture that drives the memory subsystem, supported memory types, memory population rules, and supported memory RAS features.

6.1 Memory Subsystem Architecture

The Intel® D50TNP Modules include one of the following server boards:

- D50TNP1SB server board: 8 DDR4 DIMM slots and 4 Intel® Optane™ PMem DIMM slots, for a total of 12 DIMM slots per processor
- D50TNP1SBCR server board: 8 DDR4 DIMM slots per processor

Each 3rd Gen Intel® Xeon® Scalable processor supports eight memory channels using four integrated memory controllers (IMCs). Each memory channel is assigned an identifying letter A-H. On the D50TNP1SB server board, channels A, C, E, and G each support two DIMM slots – slot 1 (blue slot for DDR4 DIMM) and slot 2 (black slot for Intel® Optane™ PMem). The remaining channels each support one DIMM slot (blue slot for DDR4 DIMM). On the D50TNP1SBCR server board, all the channels each support one DIMM slot (blue slot for DDR4 DIMM).

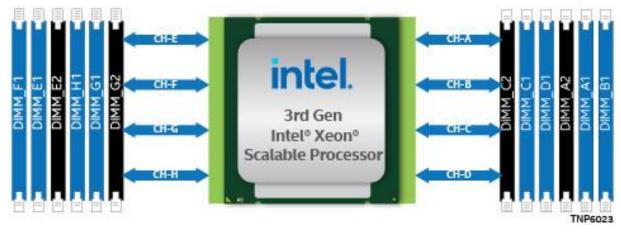


Figure 55. Memory Slot Connectivity for D50TNP1SB

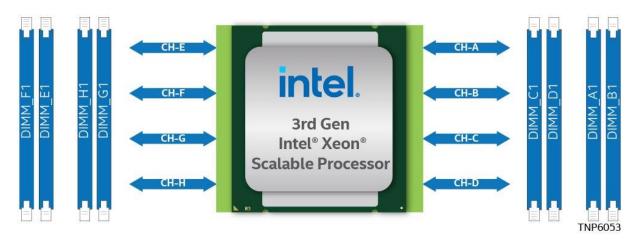


Figure 56. Memory Slot Connectivity for D50TNP1SBCR

6.2 Supported Memory

The Intel® D50TNP Modules with D50TNP1SB or D50TNP1SBCR server board support standard DDR4, RDIMMs, and LDRIMMs. In addition, modules with the D50TNP1SB server board support Intel® Optane™ persistent memory 200 series modules.

Note: Previous generation Intel® Optane™ persistent memory modules are not supported.

Note: Liquid-cooled configurations require all DIMM slots to be populated with DDR4 DIMMs.

Intel® Optane™ persistent memory is an innovative technology that delivers a unique combination of affordable large memory capacity and data persistence (non-volatility). It represents a new class of memory and storage technology architected specifically for data center usage. The Intel® Optane™ persistent memory 200 series modules enable higher density (capacity per DIMM) DDR4-compatible memory modules with near-DRAM performance and advanced features not found in standard SDRAM. The persistent memory technology can help boost the performance of data-intensive applications, such as in-memory analytics, databases, content delivery networks, and high-performance computing (HPC).

6.2.1 Standard DDR4 DIMM Support

The following figure shows a standard DDR4 DIMM module.

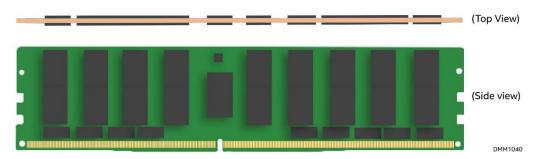


Figure 57. Standard SDRAM DDR4 DIMM Module

The Intel® Server D50TNP Family supports DDR4 DIMMs with the following features:

- All DDR4 DIMMs must support ECC
- Registered DDR4 (RDIMM), 3DS-RDIMM, Load Reduced DDR4 (LRDIMM), 3DS-LRDIMM
 Note: 3DS = 3-dimensional stacking
- RDIMMs and LRDIMMs with thermal sensor on-DIMM (TSOD)
- DIMM speeds of up to 3200 MT/s (for 2 DPC)
- DIMM capacities of 8 GB, 16 GB, 32 GB, 64 GB, and 128 GB
- RDIMMs organized as Single Rank (SR), Dual Rank (DR)
- 3DS-RDIMM organized as Quad Rank (QR), or Oct Rank (OR)
- LRDIMMs organized as Quad Rank (QR)
- 3DS-LRDIMM organized as Quad Rank (QR), or Oct Rank (OR)

The following tables list the DDR4 DIMM support guidelines.

Table 11. Supported DDR4 DIMM Memory

Туре	Ranks per DIMM and Data Width	DIMM Capacity (GB)		Maximum Speed (MT/s) at 1.2 V	
		8 Gb DDR4 Density	16 Gb DDR4 Density	1 DPC	
	SR x8	8	16	3200	
RDIMM	SR x4	16	32	3200	
KDIMM	DR x8	16	32	3200	
	DR x4	32	64	3200	
3DS-RDIMM	QR/OR x4	64 (2H) 128 (4H)	128 (2H)	3200	
LRDIMM	QR x4	64	128	3200	
3DS-LRDIMM	QR/OR x4	128 (4H)	128 (2H)	3200	

Notes:

- 1. Specification applies only to memory chips mounted by the surface mounted technology (SMT) method. For the plated through hole (PTH) mounted method, the maximum speed is 2933 MT/s.
- 2. SR = Single Rank, DR = Dual Rank, QR = Quad Rank, OR = Oct Rank, H = Stack Height, DPC = DIMMs Per Channel

The maximum supported SDRAM DIMM speed depends on the processor tier as shown in the following table.

Table 12. Maximum Supported Standard SDRAM DIMM Speed by Processor Shelves

	Maximum DIMM Speed (MT/s) by processor Shelf			
Processor Family	Platinum 8300 Processors	Gold 6300 Processors ²	Gold 5300 Processors	Silver 4300 Processors
3 rd Gen Intel® Xeon® Scalable processors	3200	3200	2933	2666

Notes:

- Specification applies only to memory chips mounted by the surface mounted technology (SMT) method.
- 2. Gold processor SKU 6330 maximum speed is 2933 (MT/s).

6.2.2 Intel® Optane™ Persistent Memory 200 Series Support (Intel® D50TNP Modules with Intel® D50TNP1SB Server Board Only)

The Intel® D50TNP Modules with the D50TNP1SB server board support Intel® Optane™ persistent memory 200 series.

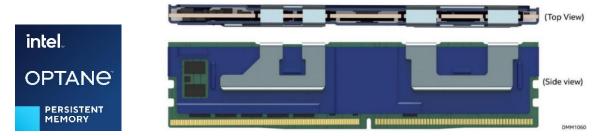


Figure 58. Intel® Optane™ Persistent Memory 200 Series Module

Intel® Optane™ PMem is an innovative technology that delivers a unique combination of affordable large memory capacity and data persistence (non-volatility). It represents a new class of memory and storage technology architected specifically for data center usage. Intel® Optane™ PMem 200 series enables higher

density (capacity per DIMM) DDR4-compatible memory modules with near-DRAM performance and advanced features not found in standard SDRAM.

Intel® Optane™ PMem 200 series supports the following features:

- DDR4 Pin Compatible
- Available PMem Capacities 128, 256, 512 GB
- Up to 2 TB per processor socket
- Up to 3200 MT/sec
- TDP = 15 W
- AES256 Bit Encryption
- Secure Erase
- Data persistence in power failure event ADR, eADR (optional)

See Section 6.4 for memory RAS features and Intel® Optane™ PMem 200 series compatibility with security features Intel® Software Guard Extensions (Intel® SGX), Intel® Total Memory Encryption (Intel® TME), and Intel® Total Memory Encryption – Multi-Tenant (Intel® TME-MT).

Supported operating modes:

- Memory mode (MM)
- App Direct (AD) mode

6.2.2.1 Intel® Optane™ Persistent Memory 200 Series – Memory Mode (MM)

In Memory mode, the standard DDR4 DRAM acts as a cache for the most frequently accessed data, while Intel® Optane™ persistent memory 200 series modules provide large memory capacity by acting as direct load/store memory. In this mode, applications and operating system are explicitly aware that the Intel® Optane™ persistent memory 200 series is the only type of direct load/store memory in the system. Cache management operations are handled by the integrated memory controller in the Intel® Xeon® Scalable processor. When data is requested from memory, the memory controller first checks the DRAM cache. If the data is present, the response latency is identical to DRAM. If the data is not in the DRAM cache, it is read from the Intel® Optane™ persistent memory 200 series modules with slightly longer latency. The applications with consistent data retrieval patterns that the memory controller can predict, will have a higher cache hit rate. Data is volatile in Memory mode. It will not be saved in the event of power loss. Persistence is enabled in App Direct mode.

6.2.2.2 Intel® Optane™ Persistent Memory 200 Series – App Direct (AD) Mode

In App Direct mode, the operating system sees Intel® Optane™ persistent memory and DDR4 SDRAM DIMMs as two separate pools of memory. App Direct mode can direct which type of data read or write is suitable for SDRAM or Intel® Optane™ PMem. Operations that require the lowest latency and do not need permanent data storage can be executed on SDRAM DIMMs, such as database "scratch pads". Data that needs to be made persistent or structures that are very large can be routed to Intel® Optane™ persistent memory. The App Direct mode must be used to make data persistent in memory. This mode requires an operating system or virtualization environment enabled with a persistent memory-aware file system.

App Direct mode requires both driver and explicit software support. To ensure operating system compatibility, visit https://www.intel.com/content/www/us/en/architecture-and-technology/optane-memory.html.

6.2.2.3 Intel® Optane™ PMem configuration using the <F2> BIOS Setup Utility

Following the installation of Intel® Optane™ PMem devices into the system, they need to be configured using the <F2> BIOS Setup utility. The BIOS Setup utility includes several Intel® Optane™ PMem configuration options across multiple BIOS Setup screens. The following illustration provides a BIOS Setup screen navigation directing the user to the main Intel® Optane™ PMem configuration screen.



Figure 59. <F2> BIOS Setup Screen Navigation for Intel® Optane™ PMem Setup Options

The main Intel® Optane™ PMem Configuration screen provides links to the various device information and setup screens.

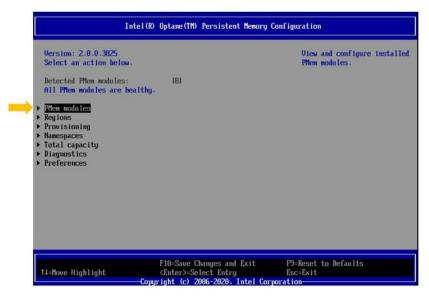


Figure 60. Intel® Optane™ PMem Configuration Menu in <F2> BIOS Setup

6.3 Memory Population

The Intel® D50TNP Modules with the D50TNP1SB board support memory configurations that consists of both standard DDR4 DIMMs and Intel® Optane™ persistent memory 200 series modules. With two processors installed, 8 memory slots are available for Intel® Optane™ persistent memory 200 series and 16 memory slots are available for DDR4 DIMMs. The Intel® D50TNP Modules with the D50TNP1SBCR board support up to 16 DDR4 DIMMs.

This section provides memory population rules and recommendations for standard DIMMs and Intel® Optane™ persistent memory 200 series modules. Figure 61 and Figure 62 show the full board layout for all memory slots on both processor sockets.

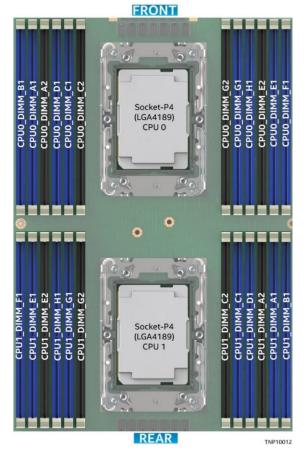


Figure 61. Intel® Server Board D50TNP1SB Memory Slot Layout

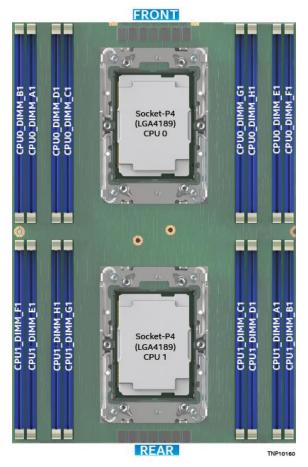


Figure 62. Intel® Server Board D50TNP1SBCR Memory Slot Layout

6.3.1 Standard DDR4 DIMM Population Rules

Intel DDR4 DIMM Support Disclaimer:

Intel validates and will only provide support for system configurations where all installed DDR4 DIMMs have matching "Identical" or "Like" attributes. See Table 13. A system configured concurrently with DDR4 DIMMs from different vendors will be supported by Intel if all other DDR4 "Like" DIMM attributes match.

Intel does not perform system validation testing nor will it provide support for system configurations where all populated DDR4 DIMMs do not have matching "Like" DIMM attributes as listed in Table 13.

Intel will only provide support for Intel server systems configured with DDR4 DIMMs that have been validated by Intel and are listed on Intel's Tested Memory list for the given Intel server product family.

Intel configures and ships pre-integrated L9 server systems. All DDR4 DIMMs within a given L9 server system as shipped by Intel will be identical. All installed DIMMs will have matching attributes as those listed in the "Identical" DDR4 DIMM4 Attributes column in Table 13.

When purchasing more than one integrated L9 server system with the same configuration from Intel, Intel reserves the right to use "Like" DIMMs between server systems. At a minimum "Like" DIMMS will have matching DIMM attributes as listed in the table below. However, the DIMM model #, revision #, or vendor may be different.

For warranty replacement, Intel will make every effort to ship back an exact match to the one returned. However, Intel may ship back a validated "Like" DIMM. A "Like" DIMM may be from the same vendor but may not be the same revision # or model #, or it may be an Intel validated DIMM from a different vendor. At a minimum, all "Like" DIMMs shipped from Intel will match attributes of the original part according to the definition of "Like" DIMMs in the following table.

Table 13. DDR4 DIMM Attributes Table for "Identical" and "Like" DIMMs

- DDR4 DIMMs are considered "Identical" when ALL listed attributes between the DIMMs match
- Two or more DDR4 DIMMs are considered "Like" DIMMs when all attributes minus the Vendor, and/or DIMM Part # and/or DIMM Revision#, are the same.

Attribute	"Identical" DDR4 DIMM Attributes	"Like" DDR4 DIMM Attributes	Possible DDR4 Attribute Values	
Vendor	Match	Maybe Different	Memory Vendor Name	
DIMM Part #	Match	Maybe Different	Memory Vendor Part #	
DIMM Revision #	Match	Maybe Different	Memory Vendor Part Revision #	
SDRAM Type	Match	Match	DDR4	
DIMM Type	Match	Match	RDIMM, LRDIMM	
Speed (MHz)	Match	Match	2666, 2933, 3200	
Voltage	Match	Match	1.2V	
DIMM Size (GB)	Match	Match	8GB, 16GB, 32GB, 64GB, 128GB, 256GB	
Organization	Match	Match	1Gx72; 2Gx72; 4Gx72; 8Gx72; 16Gx72; 32Gx72	
DIMM Rank	Match	Match	1R, 2R, 4R, 8R	
DRAM Width	Match	Match	x4, x8	
DRAM Density	Match	Match	8Gb, 16Gb	

Note: Intel only supports mixed DDR4 DRAM DIMM configurations as defined in the Intel DDR4 Support Disclaimer above.

- DDR4 DIMMs can only be installed in blue slots.
- Mixed DDR4 DIMM rules:
 - Mixing DDR4 DIMMs of different speeds and latencies is not supported within or across processors. If a mixed configuration is encountered, the BIOS attempts to operate at the highest common speed and the lowest latency possible.
 - o x4 and x8 width DDR4 DIMMs may be mixed in the same channel.
 - o Mixing of DDR4 DIMM types (RDIMM, LRDIMM, 3DS-RDIMM, 3DS-LRDIMM) within or across processors is not supported. This is a Fatal Error Halt in Memory Initialization.
- If channels A, C, E, and G are populated, they must be populated with same total DDR4 DIMM capacity per channel.
- If channels B, F, D, and H are populated, they must be populated with same total DDR4 DIMM capacity per channel
- Memory slots associated with a given processor are unavailable if the corresponding processor socket is not populated.
- Processor sockets are self-contained and autonomous. However, all memory subsystem support (such as memory RAS and error management) in the BIOS Setup is applied commonly for each installed processor.
- For best system performance, memory must be installed in all eight channels for each installed processor.
- For best system performance in dual processor configurations, installed DDR4 DIMM type and population for DDR4 DIMMs configured to CPU 1 must match DDR4 DIMM type and population configured to CPU 0. For additional information, see Section 6.3.3.

6.3.2 Intel® Optane™ Persistent Memory 200 Series Module Rules (Intel® Server Board D50TNP1SB Only)

All operating modes:

- Only Intel® Optane™ persistent memory 200 series modules are supported.
- In an Intel server system, support for Intel® Optane™ persistent memory 200 series module is only available on air-cooled systems.
- Intel® Optane™ persistent memory 200 series modules are only supported in DIMM slot 2 (black slot) and the slot 1 (blue slot) in the same memory channel must be populated with one DDR4 DIMM.
- Mixing of different DDR4 DIMM types on the system is not supported nor validated. Intel® Optane™
 persistent memory 200 series and DDR4 must have the same capacity and type across or within all
 sockets.

Memory mode:

- Populate each memory channel with at least one DDR4 to maximize bandwidth.
- Intel® Optane™ persistent memory 200 series modules must be populated symmetrically for each installed processor (corresponding slots populated on either side of each processor) and across both processors.

App Direct mode:

- Minimum of one Intel® Optane™ persistent memory 200 series module for the board.
- Intel® Optane™ persistent memory 200 series modules must be populated symmetrically for each installed processor (corresponding slots populated on either side of each processor) and across both processors.

Intel® Server D50TNP Family Technical Product Specification

Table 14. Intel® Optane™ Persistent Memory 200 Series Module Support

Processor SKU Level	Intel® Optane™ Persistent Memory 200 Series Capacity (GB)	Speed (MT/s)
Silver 4300 processors (Silver 4314 processor SKU only)	128 256 512	2666 2400
Gold 5300 processors	128 256 512	2933 2666 2400
Gold 6300 processors ¹	128 256 512	3200 2933 2666 2400
Platinum 8300 processors	128 256 512	3200 2933 2666 2400

Note:

1. Gold processor SKU 6330 maximum speed is 2933 (MT/s).

Table 15. Standard DDR4 DIMMs Compatible with Intel® Optane™ Persistent Memory 200 Series Modules

Time	Ranks per DIMM and Data Width	DIMM Size (GB)		
Туре		8 Gb DRAM Density	16 Gb DRAM Density	
RDIMM (PTH – up to 2933 MT/s) (SMT – up to 3200 MT/s)	SR x8	N/A	N/A	
	SR x4	16	32	
	DR x8	16	32	
	DR x4	32	64	
3DS-RDIMM (PTH – up to 2933 MT/s) (SMT – up to 3200 MT/s)	QR x4 (2H)	N/A	128	
	OR x4 (4H)	N/A	N/A	
LRDIMM (PTH/SMT – up to 3200 MT/s)	QR x4	64	128	
3DS-LRDIMM (PTH/SMT – up to 3200 MT/s)	QR x4 (2H)	N/A	128	
	OR x4 (4H)	128	N/A	

Note: SR = Single Rank, DR = Dual Rank, QR = Quad Rank, OR = Oct Rank, H = Stack Height, PTH = Plated Through Hole, SMT = Surface-Mount Technology

6.3.3 Recommended Memory Configurations

This section provides the recommended memory population configurations for the Intel® Server D50TNP Family. For best system performance in dual-processor configurations, installed memory type and population should be the same for both processors.

See the following figures and tables to identify the memory slot locations and recommended population configurations.

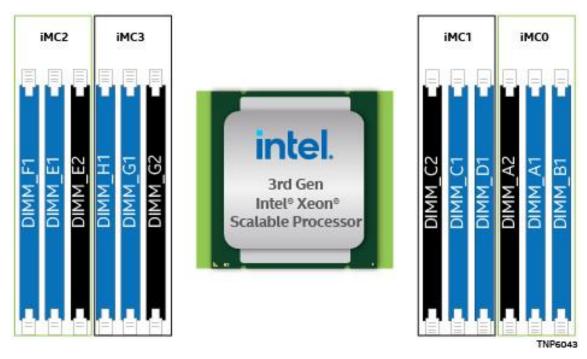


Figure 63. Memory Slot Identification for Modules with Intel® Server Board D50TNP1SB

Table 16. Standard DDR4 DIMM-only per Socket Population Configurations (Intel® Server Board D50TNP1SB)

	IMC 2		IMC 3		IMC 1			IMC 0				
# of DIMMs	CH F	CH F CH E		СН Н	CH G		CH C		CH D	CH A		СН В
DII 11 13	Slot 1	Slot 1	Slot 2	Slot 1	Slot 1	Slot 2	Slot 2	Slot 1	Slot 1	Slot 2	Slot 1	Slot 1
1	-	-	-	-	-	-	-	-	-	-	DDR4 ¹	-
2	-	DDR4	-	-	-	-	-	-	-	-	DDR4	-
2	-	-	-	-	DDR4	-	-	DDR4	-	-	-	-
2	-	-	-	-	-	-	-	DDR4	-	-	DDR4	-
2	-	DDR4	-	-	DDR4	-	-	-	_	-	-	-
2	-	-	-	-	-	-	-	-	DDR4	-	DDR4	-
4	-	DDR4	-	-	DDR4	-	-	DDR4	-	-	DDR4	-
6	DDR4	DDR4	-	-	DDR4	-	-	DDR4	-	-	DDR4	DDR4
8	DDR4	DDR4	-	DDR4	DDR4	-	-	DDR4	DDR4	-	DDR4	DDR4

Notes:

- 1. Recommended location. DDR4 may be populated in slot 1 on any channel.
- 2. Liquid-cooled configurations require all DIMM slots to be populated with DDR4 DIMMs.

Table 17. Standard DDR4 DIMM and Intel® Optane™ Persistent Memory 200 Series Module (PMem) per Socket Population Configurations (Intel® Server Board D50TNP1SB)

ш - с		IMC 2			IMC 3		IMC 1			IMC 0			
# of DIMMs	Mode	CH F	CH	1 E	СНН	CH	1 G	CH	I C	CH D	CH	I A	СН В
Diriris		Slot 1	Slot 1	Slot 2	Slot 1	Slot 1	Slot 2	Slot 2	Slot 1	Slot 1	Slot 2	Slot 1	Slot 1
	AD	DDR4	DDR4	-	DDR4	DDR4	-	-	DDR4	DDR4	PMem	DDR4	DDR4
8 DDR4 /	AD	DDR4	DDR4	-	DDR4	DDR4	-	PMem	DDR4	DDR4	-	DDR4	DDR4
1 PMem	AD	DDR4	DDR4	PMem	DDR4	DDR4	-	-	DDR4	DDR4	-	DDR4	DDR4
	AD	DDR4	DDR4	-	DDR4	DDR4	PMem	-	DDR4	DDR4	-	DDR4	DDR4
8 DDR4 / 4 PMem	AD or MM	DDR4	DDR4	PMem	DDR4	DDR4	PMem	PMem	DDR4	DDR4	PMem	DDR4	DDR4

Note: AD = App Direct mode, MM = Memory Mode, PMem = Persistent Memory

Notes on Intel® Optane™ persistent memory 200 series module population:

- For MM, standard DDR4 / Intel® Optane™ persistent memory 200 series module capacity recommended ratio is 1 GB:8 GB.
- For each individual population, rearrangements between channels are allowed as long as the resulting population is consistent with defined memory population rules.
- For each individual population, the same DDR4 DIMM must be used in all slots, as specified by the defined memory population rules.

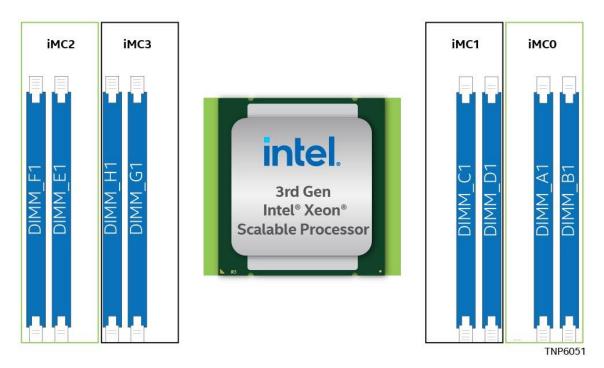


Figure 64. Memory Slot Identification for Modules with Intel® Server Board D50TNP1SBCR

Table 18. Standard DDR4 DIMM-only per Socket Population Configurations (Intel® Server Board D50TNP1SBCR)

	IMC 2		IMC 3		IM	C 1	IMC 0	
# of DIMMs	CH F	CH E	СН Н	CH G	CH C	CH D	CH A	СН В
DII II 13	Slot 1	Slot 1						
1	-	-	-	-	-	-	DDR4 ¹	-
2	-	DDR4	-	-	-	-	DDR4	-
2	-	-	-	DDR4	DDR4	-	-	-
2	-	-	-	-	DDR4	-	DDR4	-
2	-	DDR4	-	DDR4	-	-	-	-
2	-	-	-	-	-	DDR4	DDR4	-
4	-	DDR4	-	DDR4	DDR4	-	DDR4	-
6	DDR4	DDR4	-	DDR4	DDR4	-	DDR4	DDR4
8	DDR4	DDR4						

Notes:

- 1. Recommended location. DDR4 may be populated in slot 1 on any channel.
- 2. Liquid-cooled configurations require all DIMM slots to be populated with DDR4 DIMMs.

6.4 Memory RAS Support

Processors in the 3rd Gen Intel® Xeon® Scalable processor family support standard or advanced memory RAS features, depending on processor SKU, defined in the Table 19. This table lists the RAS features pertaining to system memory that consists of standard DDR4 DIMMs or a combination of standard DDR4 DIMMS and Intel® Optane™ persistent memory 200 series modules. These features are managed by the processor's IMC.

Table 19. Memory RAS Features

Memory RAS Feature	Description	Standard	Advanced
Partial Cache-Line Sparing (PCLS)	Allows replacing failed single bit in a device using spare capacity available in the processor's integrated memory controller (IMC). Up to 16 failures allowed per memory channel and no more than one failure per cache line. After failure is detected, replacement is performed at a nibble level. Supported with x4 DIMMs only.		√
	Single Device Data Correction (SDDC) via static virtual lockstep Supported with x4 DIMMs only.	V	√
Device Data Correction	Adaptive Data Correction – Single Region (ADC-SR) via adaptive virtual lockstep (applicable to x4 DDR4 DIMMs). Cannot be enabled with "Memory Multi-Rank Sparing" or "Write Data CRC Check and Retry."	√	√
	Adaptive Double Data Correction – Multiple Regions (ADDDC-MR, + 1) Supported with x4 DIMMs only.	-	√
DDR4 Command/Address (CMD/ADDR) Parity Check and Retry	DDR4 technology based CMD/ADDR parity check and retry with CMD/ADDR parity error "address" logging and CMD/ADDR retry.	V	√
DDR4 Write Data CRC Check and Retry	Checks for CRC mismatch and sends a signal back to the processor for retry. Cannot be enabled with "ADC-SR" or "ADDDC-MR, +1."	√	√
Memory Data Scrambling with Command and Address	Scrambles the data with address and command in "write cycle" and unscrambles the data in "read cycle". Addresses reliability by improving signal integrity at the physical layer. Additionally, assists with detection of an address bit error.	√	V

Memory RAS Feature	Description	Standard	Advanced
Memory Demand and Patrol Scrubbing	Demand scrubbing is the ability to write corrected data back to the memory once a correctable error is detected on a read transaction. Patrol scrubbing proactively searches the system memory, repairing correctable errors. Prevents accumulation of single-bit errors.	√	√
Memory Mirroring	Full memory mirroring: An intra-IMC method of keeping a duplicate (secondary or mirrored) copy of the contents of memory as a redundant backup for use if the primary memory fails. The mirrored copy of the memory is stored in memory of the same processor socket's IMC. Dynamic (without reboot) failover to the mirrored DIMMs is transparent to the operating system and applications.		V
	Address range/partial memory mirroring: Provides further intra socket granularity to mirroring of memory. It does this task by allowing the firmware or operating system to determine a range of memory addresses to be mirrored, leaving the rest of the memory in the socket in non-mirror mode.	_	√
DDR Memory Multi-Rank Memory Sparing	Up to two ranks out of a maximum of eight ranks can be assigned as spare ranks. Cannot be enabled with "ADC-SR", "ADDDC-MR, +1", and "Memory Mirroring".	√	√
Memory SMBus* Hang Recovery	Allows system recovery if the SMBus* fails to respond during runtime thus preventing system crash.	√	√
Memory Disable and Map Out for Fault Resilient Boot (FRB)	Allows memory initialization and booting to an operating system even when memory fault occurs.	√	√
Post Package Repair (PPR)	PPR offers additional spare capacity within the DDR4 that can be used to replace faulty cell areas detected during system boot time.	√	√
Memory Thermal Throttling	Management controller monitors the memory DIMM temperature and can temporarily slow down the memory access rates to reduce the DIMM temperature if needed.	√	√
MEMHOT Pin Support for Error Reporting	MEMHOT pin can be configured as an output and used to notify if DIMM is operating within the target temperature range. Used to implement "Memory Thermal Throttling".	√	√

Notes: Population Rules and BIOS Setup for Memory RAS

- Memory sparing and memory mirroring options are enabled in BIOS Setup.
- Memory sparing and memory mirroring options are mutually exclusive in this product. Only one operating mode at a time may be selected in BIOS Setup.
- If a RAS mode has been enabled and the memory configuration is not able to support it during boot, the system will fall back to independent channel mode and log and display errors.
- Rank sparing mode is only possible when all channels that are populated with memory have at least two single-rank or double-rank DIMMs installed, or at least one quad-rank DIMM installed, on each populated channel.
- Memory mirroring mode requires that for any channel pair that is populated with memory, the memory population on both channels of the pair must be identically sized.
- The Intel® Optane™ persistent memory 200 series RAS features listed in the following table are integrated into the system memory RAS features.

Table 20 lists additional memory RAS features specific to the Intel® Optane™ persistent memory 200 series memory. These features are managed by the processor's IMC.

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Table 20. Intel® Optane™ Persistent Memory 200 Series RAS Features

Memory RAS Feature	Description
DIMM Error Detection and Correction	Protects against random bit failures across media devices.
DIMM Device Failure Recovery (Single Device Data Correction (SDDC)	Corrects errors resulting from the failure of a single media device.
DIMM Package Sparing (Double Device Data Correction (DDDC)	Achieved by a spare device on the DIMM and erasure decoding.
DIMM Patrol Scrubbing	Proactively searches the DIMM memory, repairing correctable errors. This can prevent correctable errors from becoming uncorrectable due to accumulation of failed bits.
DIMM Address Error Detection	Ensures the correctness of addresses when data is read from media devices.
DIMM Data Poisoning	Mechanism to contain, and possibly recover from, uncorrectable data errors. Depending on the mode used, poisoning has different reset behavior: In memory mode, poison is cleared after reset. In App Direct, poison is not cleared with reset.
DIMM Viral	Ensures that potentially corrupted data is not committed to persistent memory in App Direct and is supported only in tandem with poison. Viral mode does not apply to memory mode.
DIMM Address Range Scrub (ARS)	Obtains the healthy memory media range before assigning it to a persistent memory region.
DDR-T Command and Address Parity Check and Retry	Host retries a CMD/ADDR transaction if the DIMM controller detects a parity error and initiates an error flow.
DDR-T Read Write Data ECC Check and Retry	Host continuously retries a data transaction as long as the DIMM controller detects an ECC error and initiates an error flow.
Faulty DIMM Isolation	Identifies a specific failing DIMM enabling replacement of only the DIMM that has failed.

Intel® Server D50TNP Family security feature support includes Intel® Software Guard Extensions (Intel® SGX), Intel® Total Memory Encryption (Intel® TME), and Intel® Total Memory Encryption – Multi-Tenant (Intel® TME–MT). When any of these security features are enabled, Intel® Optane™ PMem 200 series will be disabled. In addition, some of the memory RAS features will be disabled as indicated in the following table.

Table 21. Compatibility of RAS features Intel® SGX, Intel® TME, and Intel® TME-MT

Feature/Technology	Intel® SGX	Intel® TME, Intel® TME-MT
Intel® Optane™ persistent memory 200 series	No	No
ADC(SR)/ADDDC(MR)	No	Yes
MCA Recovery – Execution Path	No	Yes
MCA Recovery – Non-execution Path	Yes	Yes
Address Range Mirroring	No	Yes
Dynamic Capacity change: CPU/Memory/IIO, Physical CPU Board Hot Add/Remove, OS CPU/Memory/IIO On-lining (Capacity change), OS CPU off-lining (Capacity change), Intel® UPI link Hot pluggability, and Intel® UPI System Quiescence.	No	Yes
Static/Hard Partitioning, Electronically Isolated (Static/Hard) Partitioning, Dynamic Partitioning (Via Resource/Capacity Addition), Multiple South Bridge (PCH) Presence for supporting system partitioning	No	Yes

7. PCI Express (PCIe*) Support

The PCI Express (PCIe) interfaces on the Intel® Server D50TNP Family are fully compliant with the *PCI Express Base Specification, Revision 4.0* supporting the following PCIe bit rates: 4.0 (16 GT/s), 3.0 (8.0 GT/s), 2.0 (5.0 GT/s), and 1.0 (2.5 GT/s). The interfaces supporting M.2 connectors from the Platform Controller Hub (PCH) chipset are fully compliant with the *PCI Express Base Specification, Revision 3.0* supporting the following PCIe bit rates: 3.0 (8.0 GT/s), 2.0 (5.0 GT/s), and 1.0 (2.5 GT/s).

7.1 PCI Express Port Routing

The following table provides the PCIe* port routing for the supported riser slots and onboard OCuLink connectors.

Host	Port	Width	Gen.	Server Board Connector	Server System Usage	Module Used	
	Port 0A-0D	x16	4.0	2 x8 OCuLink connectors (7 and 8)	OCuLink	Storage, Accelerator	
	Port 1A-1D	x16	4.0	2 x8 OCuLink connectors (5 and 6)	OCuLink		
CPU 0	Port 2A-2D	x16	4.0	Riser Slot 1 1U PCIe* slot / 2U bottom PCIe* slot		Compute, Management, Storage, Accelerator	
	Port 3D	x4	4.0	Riser Slot 1	U.2 SSD	Management,	
	Port 3C	x4	4.0	Riser Slot 2	U.2 SSD	Accelerator	
	Port 3A-3B	х8	4.0	Riser Slot 2	2U top PCIe* slot	-	
	Port 0A-0D	x16	4.0	2 x8 OCuLink connectors (1 and 2)	OCuLink	Storage, Accelerator	
	Port 1A-1D	x16	4.0	Riser Slot 1	2U top PCIe* slot	Compute,	
CPU 1	Port 2A-2D	x16	4.0	Riser Slot 2	1U PCIe* slot / 2U bottom PCIe* slot	Management, Storage, Accelerator	
	Port 3A-3D	x16	4.0	2 x8 OCuLink connectors (3 and 4)	OCuLink	Storage, Accelerator	
	Port 4–7	x4	3.0	Riser Slot 2	M.2 SSD	Compute,	
PCH Chipset	Port 8–11	x4	3.0	Riser Slot 1	M.2 SSD	Management, Storage, Accelerator	

Table 22. PCIe* Port Routing

7.2 PCI Express Enumeration and Allocation

The BIOS assigns PCIe bus numbers in a depth-first hierarchy, in accordance with the *PCIe Base Bus Specification, Revision 4.0.* The bus number is incremented when the BIOS encounters a PCI-PCI bridge device.

Scanning continues on the secondary side of the bridge until all subordinate buses are assigned numbers. PCIe bus number assignments may vary from boot to boot with varying presence of PCIe devices with PCI-PCI bridges.

If a bridge device with a single bus behind it is inserted into a PCIe bus, all subsequent PCIe bus numbers below the current bus are increased by one. The bus assignments occur once, early in the BIOS boot process, and never change during the pre-boot phase.

7.3 PCI Express Bifurcation

All modules in the Intel® Server D50TNP Family support the following bifurcation of x16 PCIe data lanes into smaller PCIe groups:

- Riser Slot 1 1U PCIe slot riser card / 2U bottom PCIe slot riser card: x16/x8x8/x8x4x4/x4x4x8/x4x4x4
- Riser Slot 1 2U top PCIe slot riser card: x16/x8x8/x8x4x4/x4x4x8/x4x4x4x4
- Riser Slot 2 1U PCIe slot riser card / 2U bottom PCIe slot riser card: x16/x8x8/x8x4x4/x4x4x8/x4x4x4
- Riser Slot 2 2U top PCIe slot riser card: No bifurcation support

In addition, the Accelerator Module also supports the following bifurcation of x16 PCIe data lanes into smaller PCIe groups:

- Accelerator riser card 1 slot 1: x16/x8x8/x4x4x4x4
- Accelerator riser card 1 slot 2: x16/x8x8/x4x4x4x4
- Accelerator riser card 2 slot 1: x16/x8x8/x4x4x4x4
- Accelerator riser card 2 slot 2: x16/x8x8/x4x4x4x4

Note: The server boards include a clock signal for each PCIe riser slot that is used when the PCIe slot is configured to work at full link width. When a PCIe riser slot is configured with any of the available bifurcation options above, this clock signal is used for one of the PCIe groups. The installed PCIe add-in card must provide clock signals for the remaining PCIe groups and all devices exposed to the system.

To change PCIe bifurcation setting, access the BIOS Setup menu by pressing **<F2>** key during POST. Navigate to the following menu: **Advanced > Integrated IO Configuration > PCIe Slot Bifurcation Setting**

7.4 Non-Transparent Bridge

The PCIe Non-Transparent Bridge (NTB) acts as a gateway that enables high performance, low latency communication between two PCIe Hierarchies, such as a local and remote system. The NTB allows a local processor to independently configure and control the local system and provides isolation of the local host memory domain from the remote host memory domain, while enabling status and data exchange between the two domains.

The Intel® Server D50TNP Family supports NTB configuration with NTB port to NTB port connection (back-to-back) on the following PCIe ports:

- Port 2A of CPU 0
- Port 1A of CPU 1
- Port 2A of CPU 1

NTB port to root port connection is not supported.

Note: When NTB is enabled, Spread Spectrum Clocking (SSC) is required to be disabled at each NTB link.

To enable NTB, access the BIOS Setup menu by pressing <F2> key during POST. Navigate to the following menu: Advanced > Integrated IO Configuration > NTB Configuration

8. Data Storage Options

This chapter provides an overview of the available storage options for the Intel® D50TNP Modules. See Chapter 3 for details on the storage options supported by each Intel® D50TNP Module type.

8.1 M.2 SSD Storage Support

All modules include support for up to two M.2 storage devices via riser assemblies as shown in the following figure. The M.2 slots are labeled "M.2_x4_PCIE/SATA" on risers 1 and 2. Each M.2 slot supports a PCIe NVMe or SATA drive that conforms to a 2280 (80 mm) or 22110 (110 mm) form factor.

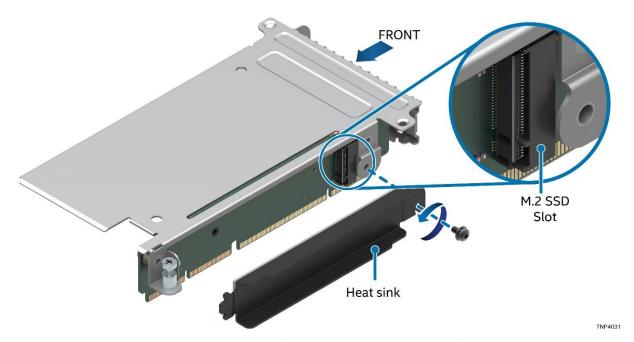


Figure 65. M.2 Slot Location on Riser Card

Note: Riser slot locations are the same for 1U and 2U modules.

The M.2 slots on both risers have four PCIe 3.0 lanes from the chipset embedded controller. Both risers include a heat sink for M.2 SSDs that must be installed whether an M.2 SSD is present or not.

When operating in PCIe NVMe mode, the M.2 storage devices support Intel® VROC (VMD NVMe RAID). See Section 8.4 for more information on Intel® VROC and Intel® VMD.

The M.2 storage devices can also operate in SATA III mode, providing up to two 6 Gb/sec SATA ports. The M.2 slots on both risers use the same chipset embedded sSATA controller. Therefore, the M.2 storage devices support Intel® VROC SATA RAID. See Section 8.6 for more information on Intel® VROC SATA RAID.

Note: The Intel® Server D50TNP Family only supports sSATA on M.2.

8.2 U.2 SSD Storage Support

Up to two hot-swappable 2.5" U.2 PCIe NVMe SSDs are supported on 2U Intel® D50TNP Management and 2U Intel® D50TNP Accelerator Modules. The drive bays are in the upper part of the front of the module as shown in the following figures.

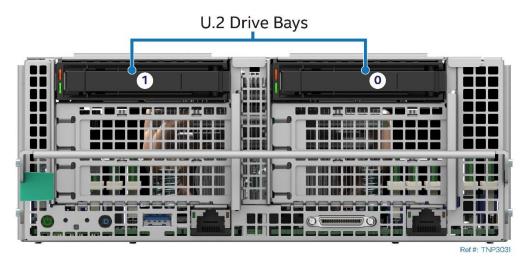


Figure 66. U.2 Drive Bay Identification - 2U Management Module



Figure 67. U.2 Drive Bay Identification - 2U Accelerator Module

Each installed NVMe drive is connected to the PCIe bus through a dedicated U.2 connector attached to the riser assemblies in the 2U Management Module and Accelerator Module.

The U.2 NVMe SSD devices support Intel® VROC (VMD NVMe RAID). See Section 8.4 for more information on Intel® VROC and Intel® VMD.

Each drive carrier includes separate LED indicators for drive activity and drive status. Two LEDs for each drive carrier are: Amber Status LED and Green Activity LED. The following tables provide the LED states.



Figure 68. Drive Carrier LED Identification

Table 23. Drive Activity LED States

	LED State	Condition
	On	Drive present, no activity
Green	4 Hz Blinking	LED blinks off when processing a command
	Off	Drive not present
	4 Hz Blinking	Locate drive (identify)

Note: The drive activity LED is driven by signals coming from the drive itself. Drive vendors may choose to operate the activity LED different from what is described in the table above. If the activity LED on a given drive type behaves differently than what is described, customers should reference the drive vendor specifications for the specific drive model to determine the expected drive activity LED operation.

Table 24. Drive Status LED States

	LED State	Drive Status
	Off	No fault, OK
Amber	4 Hz blinking	Locate (identify)
	Solid on	Fault/fail
	1 Hz blinking	Rebuild

Note: The drive status LED state for Rebuild in the previous table assumes that Intel® Volume Management (Intel® VMD) is enabled. If Intel® VMD is disabled, the drive status LED for Rebuild is always off.

8.3 NVMe* Enterprise Data Center SSD Form Factor (EDSFF) Storage

Up to 16 hot-swappable full-length (E1.L) PCIe* EDSFF NVMe* SSDs are supported on the 2U Storage Modules as shown in the following figure.

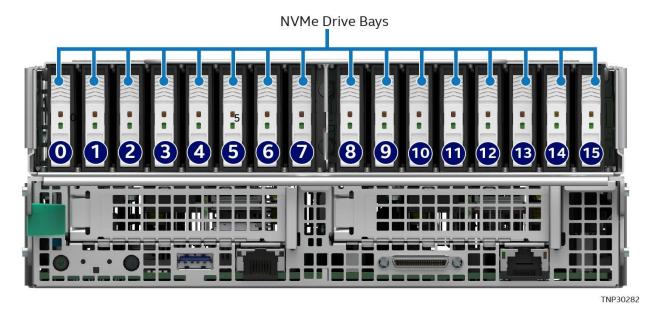


Figure 69. EDSFF NVMe* SSD Drive Identification – 2U Storage Modules

Each installed EDSFF NVMe device is connected to the PCIe bus through a dedicated docking board in the 2U Storage Module.

The EDSFF NVMe devices support Intel® VROC (VMD NVMe RAID). See Section 8.4 for more information on Intel® VROC and Intel® VMD.

Each EDSFF NVMe device includes separate LED indicators for drive activity and drive status. Two LEDs for each drive are: Amber Status LED and Green Activity LED. The LED states for EDSFF NVMe drives are the same as U.2 SSD drives provided in Table 23 and Table 24 above.

8.4 Intel® Volume Management Device (Intel® VMD) 2.0 for NVMe*

Intel® Volume Management Device (Intel® VMD) is hardware logic inside the processor root complex to help manage PCIe NVMe SSDs. It provides robust hot plug support and status LED management. This allows servicing of storage system NVMe SSD media without fear of system crashes or hangs when ejecting or inserting NVMe SSD devices on the PCIe bus.

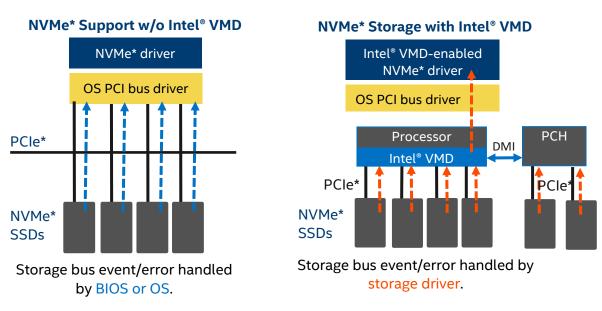


Figure 70. NVMe* Storage Bus Event / Error Handling

Intel® VMD handles the physical management of NVMe storage devices as a stand-alone function but can be enhanced when Intel® VROC support options are enabled to implement RAID based storage systems. See Section 8.5 for more information.

8.4.1 Intel® VMD 2.0 Features

The Intel® D50TNP Modules support the following Intel® VMD 2.0 features and capabilities:

- Intel® VMD enable hardware is integrated inside the processor PCIe root complex.
- Entire PCIe trees are mapped into their own address spaces (domains).
- Each domain manages x16 PCIe lanes.
- Can be enabled/disabled in BIOS Setup at x4 lane granularity.
- Driver sets up and manages the domain (enumerate, event/error handling).
- May load an additional child device driver that is Intel® VMD aware.
- Hot plug support hot insert array of PCIe NVMe SSDs.
- Support for PCIe NVMe SSDs only (no network interface controllers (NICs), graphics cards, and so on).
- Support for MMIO only (no port-mapped I/O).
- Does not support NTB, Quick Data Tech, Intel® Omni-Path Architecture (Intel® OPA), or SR-IOV.
- Correctable errors do not bring down the system.
- Intel® VMD only manages devices on PCIe lanes routed directly from the processor or PCH chipset.
- When Intel® VMD is enabled, the BIOS does not enumerate devices that are behind Intel® VMD. The Intel® VMD-enabled driver enumerates these devices and exposing them to the host.

8.4.2 Enabling Intel® VMD 2.0 Support

By default, Intel® VMD support is disabled on all processor PCIe root ports in BIOS. For installed NVMe devices to use the Intel® VMD features supported, Intel® VMD must be enabled on the appropriate processor PCIe root ports in BIOS. To enable VMD, access the BIOS Setup menu by pressing **<F2>** key during POST. Navigate to the following menu: **Advanced > Integrated IO Configuration > Volume Management Device**

Options are available in the menu to enable all PCIe root ports, disable all PCIe root ports, or enable specific PCIe root ports.

Table 22 provides the PCIe root port mapping for all onboard PCIe devices and riser card slots.

8.5 Intel® Virtual RAID on Chip (Intel® VROC) for NVMe*

The Intel® D50TNP Modules support the following Intel® VROC features:

- I/O processor with controller (ROC) and DDR4.
- Protected write-back cache
- Isolated storage devices from operating system for error handling.
- Protected R5 data from operating system crash.
- NVMe SSD hot plug and surprise removal on processor PCIe lanes.
- LED management for PCIe attached storage.
- RAID/storage management using Representational State Transfer (RESTful) application programming interfaces (APIs).
- Graphical user interface (GUI) for Windows* and Linux*.
- 4K built-in NVMe* SSD support.

Intel® VROC (VMD NVMe RAID) offers several options for RAID to meet the needs of the end user. Supported RAID levels include RAID 0 and RAID 1 on all Intel® D50TNP Modules, plus RAID 5 and RAID 10 on Intel® D50TNP Storage Modules only.

- RAID 0 Uses striping to provide high data throughput, especially for large files in an environment that does not require fault tolerance.
- RAID 1 Uses mirroring so that data written to one disk drive simultaneously writes to another disk drive. This is good for small databases or other applications that require small capacity but complete data redundancy.
- RAID 5 Uses disk striping and parity data across all drives (distributed parity) to provide high data throughput, especially for small random access. A minimum of three drives required.
- RAID 10 A combination of RAID 0 and RAID 1 on four drives, consists of striped data across
 mirrored spans. It provides high data throughput and complete data redundancy but uses a larger
 number of spans.

Enabling Intel® VROC (VMD NVMe RAID) support requires the installation of an optional upgrade key (iPC: VROCSTANMOD or iPC: VROCPREMMOD) as shown in the following figure. Table 25 identifies the supported RAID features by each of the optional upgrade keys.

Intel® Server D50TNP Family Technical Product Specification

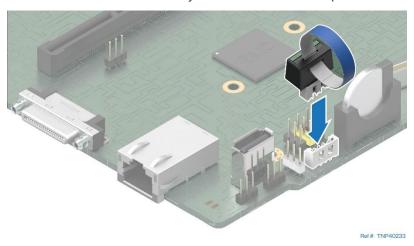


Figure 71. Intel® VROC Upgrade Key

Table 25. Optional VROC Upgrade Key - Supported NVMe* RAID Features

NVMe* RAID Major Features	Standard Intel® VROC 7.5 Key (iPC: VROCSTANMOD)	Premium Intel® VROC 7.5 Key (iPC: VROCPREMMOD)
Processor/chipset-attached NVMe* SSD – high performance	√	V
Boot on RAID volume	√	√
Third party vendor SSD support	√	√
RAID 0/1	√	√
RAID 10 – Supported on Intel® D50TNP Storage Modules only	√	√
RAID 5 – Supported on Intel® D50TNP Storage Modules only	-	√
RAID write hole closed	-	√
Hot plug/ surprise removal (2.5" SSD form factor only)	√	V
Enclosure LED management	√	V

8.6 Intel® Virtual RAID on Chip (Intel® VROC) for SATA

Intel® VROC (SATA RAID) provides an enterprise RAID solution for SATA devices connected to the sSATA controller on the Intel® Platform Control Hub (PCH).

By default, Intel® VROC (SATA RAID) options are disabled in BIOS Setup. To enable the RAID support, access the BIOS Setup utility by pressing **<F2>** key during POST. Navigate to the onboard RAID configuration menu: **Advanced > Mass Storage Controller Configuration > sSATA Controller**.

From the options available in the menu, select the RAID mode to enable the RAID support.

Note: The Intel® Server D50TNP Family system only supports sSATA III on M.2.

Supported SATA RAID levels on Intel® D50TNP Modules include RAID 0 and RAID 1.

- RAID 0 Uses striping to provide high data throughput, especially for large files in an environment that does not require fault tolerance.
- RAID 1 Uses mirroring so that data written to one disk drive simultaneously writes to another disk
 drive. This is good for small databases or other applications that require small capacity but complete
 data redundancy.

Intel® VROC 7.5 functionality requires the following:

- The embedded RAID option must be enabled in BIOS Setup.
- Intel® VROC 7.5 option must be selected in BIOS Setup.
- Intel® VROC 7.5 drivers must be loaded for the installed operating system.
- At least two SATA drives needed to support RAID 0 or RAID 1.
- NVMe SSDs and SATA drives must not be mixed in a single RAID volume.

8.7 Server Board sSATA Support

The sSATA controller can be enabled and disabled and configured through the BIOS Setup utility under the **Mass Storage Controller Configuration** menu screen. The following table lists the supported features by the embedded sSATA controller.

Table 26. SATA and sSATA Controller Feature Support

Feature	Description	AHCI Mode	RAID Mode Intel® VROC (SATA RAID)
Native Command Queuing (NCQ)	Allows the device to reorder commands for more efficient data transfers	Supported	Supported
Auto Activate for DMA	Improves efficiency of data transfer by skipping DMA Activate command after DMA Setup command	Supported	Supported
Asynchronous Signal Recovery	Provides a recovery from a loss of signal or establishing communication after hot plug	Supported	Supported
6 Gb/s Transfer Rate	Capable of data transfers up to 6 Gb/s	Supported	Supported
ATAPI Asynchronous Notification	A mechanism for a device to send a notification to the host that the device requires attention	Supported	Supported
Host and Link Initiated Power Management	Capability for the host controller or device to request Partial and Slumber interface power states	Supported	Supported
Staggered Spin-Up	Enables the host to spin up hard drives sequentially to prevent power load problems on boot	Supported	Supported
Command Completion Coalescing	Reduces interrupt and completion overhead by allowing a specified number of commands to complete and then generating an interrupt to process the commands	Supported	N/A

9. Front Control Panel and I/O

This chapter provides information on the control panel and I/O available on the front of the Intel® D50TNP Modules.

9.1 Control Panel Features

The control panel that provides push button controls and LED indicators for several features. This section provides a description for each front control panel feature.

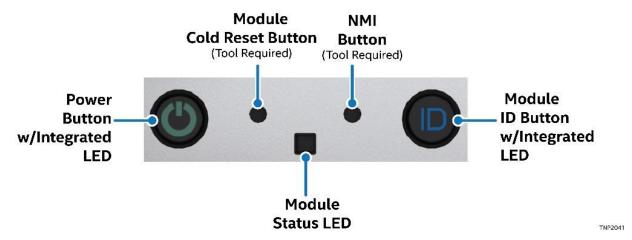


Figure 72. Front Control Panel Features

• **Power button with integrated LED** – Toggles the module power on and off. This button also functions as a sleep button if enabled by an ACPI compliant operating system. Pressing this button sends a signal to the integrated BMC that either powers on or powers off the module. The integrated LED is a single color (green) and supports different indicator states as defined in the following table.

Note: After AC power is connected, several subsystems are initialized and low-level FRU discovery is performed. This process can take up to 90 seconds. When this process is completed, the ID LED will turn solid on, indicating that the system is ready to be powered on.

Power Mode	LED	Module State	Description
Non-ACPI	Off	Power-off	Module power is off, and the BIOS has not initialized the chipset.
NOTI-ACPI	On	Power-on	Module power is on
ACPI	Off S5		Mechanical is off and the operating system has not saved any context to the hard disk.
	On	S0	Module and the operating system are up and running.

Table 27. Power / Sleep LED Functional States

Module ID button w/ integrated LED – Toggles the integrated blue ID LED on and off. The module ID LED is used to identify an Intel® D50TNP Module in a chassis for maintenance when installed in a rack of similar server systems. The module ID LED can also be toggled on and off remotely using the IPMI "Chassis Identify" command that causes the LED to blink for 15 seconds.

- NMI Button When the NMI button is pressed, it puts the Intel® D50TNP Module in a halt state and issues a non-maskable interrupt (NMI). This operation can be useful when performing diagnostics for a given issue where a memory download is necessary to help determine the cause of the problem. To prevent an inadvertent module halt, the actual NMI button is located behind the front control panel faceplate where it is only accessible with the use of a small-tipped tool like a pin or paper clip.
- Module cold reset button When pressed, this button reboots and re-initializes the Intel® D50TNP Module. Unlike the power button, the reset button does not disconnect the power to the module. It just starts the module's Power-On Self-Test (POST) sequence over again.
- Module status LED The module status LED is a bi-color (green/amber) indicator that shows the
 current health of the module. The module status LED states are driven by the integrated platform
 management subsystem. Table 28 provides a description of each supported LED state.

Table 28. Intel® D50TNP Module Status LED State Definitions

	rabic 201 mici	D301111 Ploudle Status LED State Definitions
LED State	Module State	BIOS Status Description
Off	No AC Power to system	System power is not present.Module is in EuP Lot 6 off mode.
Solid green	Module is operating normally.	 Module is in S5 soft-off state. Module is running (in S0 State) and its status is healthy. The module is not exhibiting any errors. Source power is present BMC has booted and manageability functionality is up and running. After a BMC reset, and in conjunction with the module ID LED solid on, the BMC is booting Linux*. Control has been passed from BMC U-Boot to BMC Linux*. It is in this state for roughly 10–20 seconds.
Blinking green	Module is operating in a degraded state although still functioning, or module is operating in a redundant state but with an impending failure warning.	 Redundancy loss such as power-supply or fan. Applies only if the associated platform subsystem has redundancy capabilities. Fan warning or failure when the number of fully operational fans is less than the minimum number needed to cool the system. Non-critical threshold crossed – Temperature, voltage, input power to power supply, output current for main power rail from power supply and Processor Thermal Control (Therm Ctrl) sensors. Power supply predictive failure occurred while redundant power supply configuration was present. Unable to use all installed memory (more than 1 DIMM installed). Correctable Errors over a threshold and migrating to a spare DIMM (memory sparing). This indicates that the module no longer has spared DIMMs (a redundancy lost condition). In mirrored configuration, when memory mirroring takes place and the module loses memory redundancy. Battery failure. BMC executing in U-Boot. (Indicated by module ID LED blinking at 3 Hz while Status blinking at 1 Hz). Module in degraded state (no manageability). BMC U-Boot is running but has not transferred control to BMC Linux*. The module will be in this state 6–8 seconds after BMC reset while it pulls the Linux* image into flash. BMC Watchdog has reset the BMC. Power Unit sensor offset for configuration error is asserted. SSD Hot Swap Controller (HSC) is off-line or degraded.
Blinking amber and green alternatively	Module is initializing after AC power is applied	 PFR in the process of updating/authenticating/recovering when AC power is connected, module firmware being updated. Module not ready to take power button event/signal.

LED State	Module State	BIOS Status Description
Blinking amber	Module is operating in a degraded state with an impending failure warning, although still functioning. Module is likely to fail.	 Critical threshold crossed – Voltage, temperature, input power to power supply, output current for main power rail from power supply and PROCHOT (Therm Ctrl) sensors. VRD Hot asserted. Minimum number of fans to cool the system not present or failed. Storage drive fault. Power Unit Redundancy sensor – Insufficient resources offset (indicates not enough power supplies present). In non-sparing and non-mirroring mode, if the threshold of correctable errors is crossed within the window. Invalid firmware image detected during boot or firmware update.
Solid amber	Critical/non-recoverable – module is halted. Fatal alarm – module has failed or shut down.	 CPU CATERR signal asserted. MSID mismatch detected (CATERR also asserts for this case). CPU 0 is missing. CPU Thermal Trip. No power good – power fault. DIMM failure when there is only 1 DIMM present and hence no good memory present. Runtime memory uncorrectable error in non-redundant mode. DIMM Thermal Trip or equivalent. SSB Thermal Trip or equivalent. Processor ERR2 signal asserted. BMC/Video memory test failed (module ID LED shows blue/solid-on for this condition). Both U-Boot BMC firmware images are bad (module ID LED shows blue/solid-on for this condition). 240 VA fault. Fatal Error in processor initialization: Processor family not identical Processor model not identical Processor core/thread counts not identical Processor cache size not identical Unable to synchronize processor frequency Unable to synchronize Intel® UPI link frequency BMC fail authentication with non-recoverable condition, system hang at T-1; boot PCH only, system hang; PIT failed, system lockdown

9.2 Front I/O

Several connectors are on the front panel. The following sections describe each of the available connectors.

9.2.1 Networking

The server modules include two RJ45 connectors:

- 10 Gb network interface Ethernet port
- Dedicated 1 Gb server management port

The following figures show the location of the ports on the Intel® D50TNP Modules.

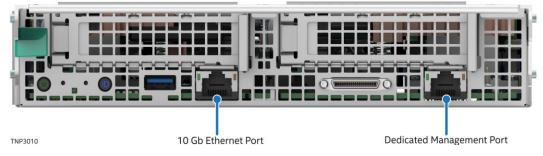


Figure 73. RJ45 Connector Identification – 1U Compute Module

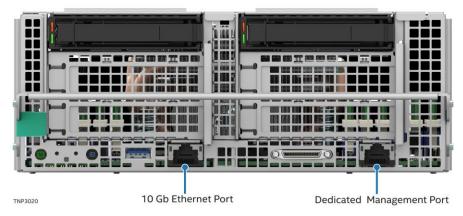


Figure 74. RJ45 Connector Identification – 2U Management Module

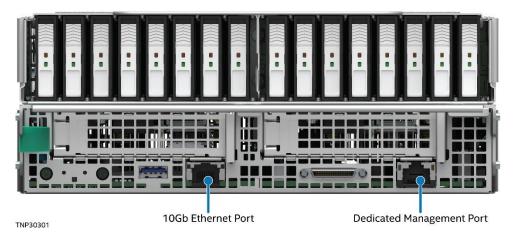


Figure 75. RJ45 Connector Identification – 2U Storage Module

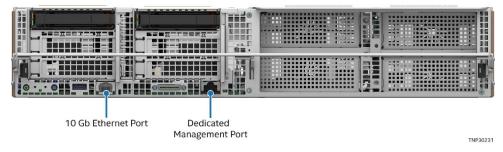


Figure 76. RJ45 Connector Identification – 2U Accelerator Module

9.2.1.1 Network Interface

Network connectivity is provided by the onboard Intel® Ethernet Controller X550 providing 1/2.5/5/10 Gb Ethernet support. The Intel® Ethernet Controller X550 is a single, compact, low-power component that offers a fully-integrated Gigabit Ethernet Media Access Control (MAC) and Physical Layer (PHY) port. The Intel® Ethernet Controller X550 uses the PCIe architecture from the Intel® C621A PCH chipset and provides a single-port implementation.

See the respective product datasheet for a complete list of supported features.

The RJ45 network interface connector includes two LEDs. The LED at the left of the connector is the link/activity LED and indicates a network connection when on and transmit/receive activity when blinking. The LED at the right of the connector indicates link speed as defined in Table 29.



Figure 77. RJ45 Network Interface Connector LEDs

LED LED State		NIC State	
	Off	LAN link not established	
Link/activity (left)	Solid green	LAN link is established	
	Blinking green	Transmit/receive activity	
Transmit/receive (right)	Solid amber	1 Gb data rate	
	Solid green	10 Gb data rate	

Table 29. RJ45 Network Interface Connector Port LED Definition

9.2.1.2 Dedicated Management Port

Each module includes a dedicated 1 GbE RJ45 management port. See Chapter 12 for additional information about server management support.

The dedicated management port includes two LEDs. The behavior of the LEDs is defined in Table 30.



Figure 78. Dedicated Management Port LEDs

Table 30. Dedicated Management Port LED Definition

Left LED	Right LED	Network Status
Off	Off	No link
Solid on	Solid on	10 Mbps link
Blinking	Blinking	10 Mbps activity
Solid on	Off	100 Mbps link
Blinking	Off	100 Mbps activity
Off	Solid on	1 Gbps link
Off	Blinking	1 Gbps activity

9.2.1.3 MAC Address Definition

The server modules have the following MAC addresses assigned at the factory:

- RJ45 network interface connector (base MAC address)
- Dedicated management port (base MAC address + 1)

9.2.2 I/O Breakout Cable

The front panel of each server module contains a 40-pin connector supporting an I/O breakout cable as shown in Figure 79. Each system configuration includes one I/O breakout cable providing a single module with additional support for one serial port, one VGA port, and two USB 3.0 ports as needed.

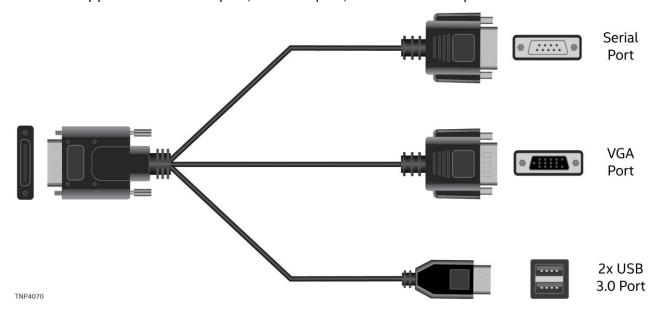


Figure 79. I/O Breakout Cable Port Identification

9.2.3 USB Support

Each server module provides one USB 3.0 port on the front panel. The system also provides two USB 3.0 ports through the dedicated I/O breakout cable (see Section 9.2.2). The following figures show the location of the front USB port.

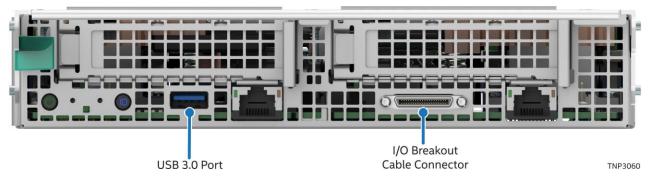


Figure 80. USB Port Location - 1U Compute Module

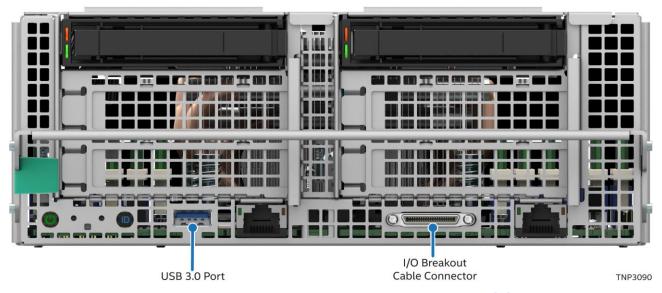


Figure 81. USB Port Location - 2U Management Module

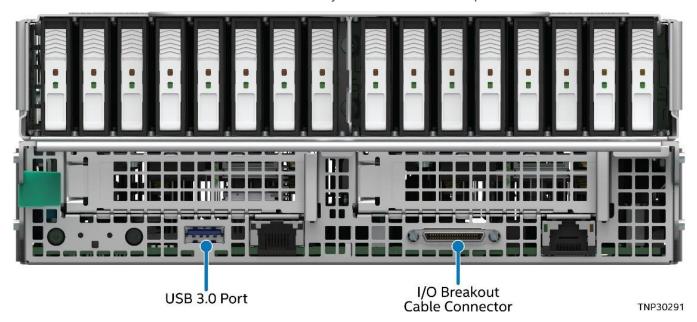


Figure 82. USB Port Location - 2U Storage Module



Figure 83. USB Port Location - 2U Accelerator Module

10. Thermal Management

This chapter provides an overview of the thermal management features and capabilities of the system.

Air-cooling configurations are supported for all server modules and the chassis. Liquid-cooling configurations are also supported for the Compute Module.

The fully integrated system is designed to operate at external ambient temperatures of 10–35 °C. Working with integrated platform management, several features are designed to move air from the front to the back of the system and over critical components to prevent them from overheating, allowing the system to operate optimally.

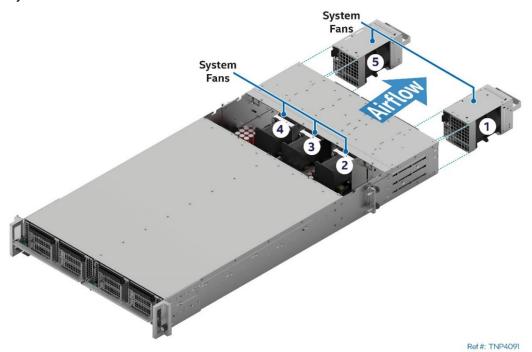


Figure 84. Air-Cooled System Airflow and Fan Identification

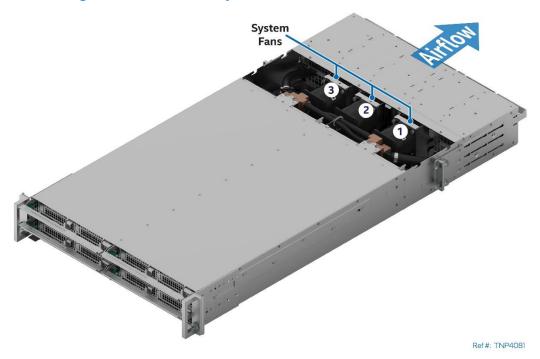


Figure 85. Liquid-Cooled System Airflow and Fan Identification

Intel® Server D50TNP Family Technical Product Specification

The following table provides airflow data associated with the Intel® Server System D50TNP and is provided for reference purposes only. The data was derived from actual wind tunnel test methods and measurements using fully configured (worst case) system configurations. Different system configurations may produce slightly different data results. In addition, the cubic feet per minute (CFM) data provided using server management utilities that use platform sensor data may vary slightly from the data listed in the tables.

Note: For system thermal data, see the online power calculator tool accessible at the following Intel web site: https://servertools.intel.com/tools/power-calculator/

System Fan	DCII For Crossed	1U AC	2U AC	2U ACCL (CFM)		1U LC	1U Storage
Speed	PSU Fan Speed	(CFM)	(CFM)	Node Side	Card Side	(CFM)	(CFM)
100%		68.9	149.5	134.7	180.4	73.3	149.1
50%	Auto	37.3	79.3	72.6	95.3	37.3	76.9
30%		24.3	49.9	45.9	59.4	22.2	48.1

Table 31. System Volumetric Airflow, Intel® Server System D50TNP

The installation and functionality of several system components is used to maintain system thermals. The components common in both air-cooling and liquid-cooling configurations are listed below:

- Three managed 60-mm dual rotor hot-swap system fans
- Fans integrated into each installed power supply module
- Add-in card bays
- Populated DIMM slots
- Board component heat sinks
- Populated drive carriers (for 2U Intel® D50TNP Modules). Drive carriers must be populated with either an SSD or supplied drive blank.

In addition, the following components contribute to maintaining system thermals depending on system cooling configuration:

- Liquid-cooled configurations
 - Liquid-cooling loop
- Air-cooled configurations
 - o Two managed 80-mm dual rotor hot-swap system fans
 - Installed DIMMs and DIMM blanks
 - Processor heat sinks
 - Air duct

In addition, it is necessary to have all blue DIMM slots populated with either DIMMs or supplied DIMM blanks. Depending on the shipping configuration from Intel, systems may or may not have DIMM blanks preinstalled. Preinstalled DIMM blanks should only be removed when installing a memory module in its place.

10.1 Thermal Operation and Configuration Requirements

To keep the system operating within supported maximum thermal limits, the system must meet the following operating and configuration guidelines:

- For air-cooled configurations:
 - The system is designed to sustain operations at an ambient temperature of up to 35 °C (ASHRAE Class A2) with short term excursion-based operation up to 45 °C (ASHRAE Class A4).
 - The system is designed to support long term reliability targets when operated at an external ambient temperature of up to 35 °C (ASHRAE A2).
 - o The system can operate up to 40 °C (ASHRAE Class A3) for up to 900 hours per year.
 - o The system can operate up to 45 °C (ASHRAE Class A4) for up to 90 hours per year.
 - There is no long-term system reliability impact when operating at the extended temperature range within the documented limits.
 - System performance may be impacted when operating within the extended operating temperature range.
- For liquid-cooled configurations:
 - The system is designed to sustain operations at an ambient temperature of up to 35 °C (ASHRAE Class A2) with short term excursion-based operation up to 45 °C (ASHRAE Class A4).
 - The system is designed to support long term reliability targets when operated at an external ambient temperature of up to 35 °C (ASHRAE A2).
 - o The system can operate up to 40 °C (ASHRAE Class A3) for up to 900 hours per year.
 - o The system can operate up to 45 °C (ASHRAE Class A4) for up to 90 hours per year.
 - No long-term system reliability impact when operating at the extended temperature range within the documented limits.
 - System performance may be impacted when operating within the extended operating temperature range.
 - \circ The system is designed to support facility coolant supply temperature of 2–45 °C (ASHRAE Class W4).

Specific configuration requirements and limitations are documented in the system configuration table for thermal compatibility in Appendix E and an online power calculator tool accessible at the following Intel web site: https://servertools.intel.com/tools/power-calculator/

For air-cooled Intel® D50TNP Modules, the CPU 0 processor and heat sink must be installed first.

10.2 Thermal Management Overview

To maintain the necessary airflow in the system, the previously listed components and top cover need to be properly installed. For optimal system performance, the external ambient temperature should remain below 35 °C and all system fans should be operational. System fan rotor redundancy can be supported with limited performance for some components in the system. See Appendix E for performance in fan failed mode.

For system configurations that support fan redundancy, if a single fan rotor failure occurs (system fan or power supply fan), integrated platform management does the following:

- Changes the state of the system status LED to blinking green,
- · Reports an error to the system event log, and
- Automatically adjusts fan speeds of operational fans as needed to maintain system temperatures below maximum thermal limits.

Fan redundancy is lost if more than one fan rotor in the same fan or different fans are in a failed state.

Note: All system fans are controlled independently of each other. The fan control system may adjust fan speeds for different fans based on increasing/decreasing temperatures in different thermal zones in the chassis.

If system temperatures continue to increase with the system fans operating at their maximum speed, platform management may begin to throttle bandwidth of either the memory subsystems, the processors, or both to keep components from overheating and keep the system operational. Throttling of these subsystems continues until system temperatures are reduced below preprogrammed limits.

If system thermals increase to a point beyond the maximum thermal limits, the system shuts down, the system status LED changes to solid amber, and the event is logged to the system event log.

If power supply thermals increase to a point beyond their maximum thermal limits or if a power supply fan should fail, the power supply shuts down.

Note: For proper system thermal management, sensor data records (SDRs) for any given system configuration must be loaded by the system integrator as part of the initial system integration process. SDRs are loaded using the FRUSDR utility that is part of the system update package (SUP) or System Firmware Update Package (SFUP) utility that can be downloaded from http://downloadcenter.intel.com.

10.3 System Fans

The system includes different fans depending on cooling configurations listed below:

- Liquid-cooled configuration
 - o Three managed 60-mm dual rotor hot-swap system fans
 - o Fans integrated into each installed power supply module
- Air-cooled configuration
 - o Three managed 60-mm dual rotor hot-swap system fans
 - o Two managed 80-mm dual rotor hot-swap system fans
 - o Fans integrated into each installed power supply module

The system fans and power supply module fans provide the primary airflow for the system.

The system is designed for fan redundancy when configured with three power supply modules. That is, all system fan rotors are operational and ambient air remains at or below ASHRAE class 2 limits. Should a single system fan rotor fail, platform management will adjust airflow of the remaining system fans and manage other platform features to maintain system thermals. Fan redundancy is lost if more than one fan rotor in the same fan or different fans are in a failed state.

The system supports up to a total of five system fans in air-cooled configurations and up to three system fans in liquid-cooled configurations. All system fans are mounted in an individual fan assembly module. Each system fan:

- Is hot-swappable.
- Is designed for tool-less insertion and extraction from the system chassis.
- Has a tachometer signal that allows the integrated BMC to monitor its status.
- Has its fan speed controlled by integrated platform management. As system thermals fluctuate high and low, the integrated BMC firmware increases and decreases the speeds to specific fans in the fan assembly to regulate system thermals.
- Is mounted inside a fan cage assembly that can be removed from the back of the system chassis. The fan cage assembly includes a fan fail LED visible from the back of the system chassis.
- Connects to the power distribution board through a 2x5-pin connector. Table 32 lists the connector pinout.

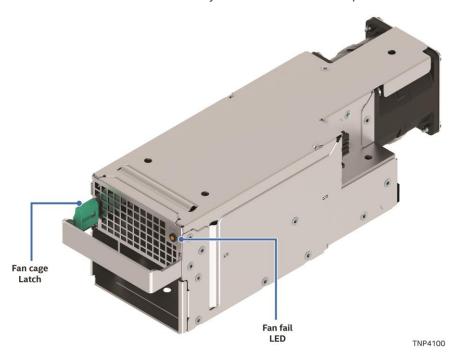


Figure 86. System Fan Cage Assembly

Table 32. System Fan Connector Pinout

Pin#	Signal Name
1	P12V_FAN_ROTOR1
2	GND
3	FAN_TACH1_FLT
4	FAN_TACH2_FLT
5	FAN_PWM_FLT

Pin#	Signal Name	
6	FAN_PRSNT_N	
7	FAN_CATH_LED	
8	FAN_ANODE_LED	
9	P12V_FAN_ROTOR2	
10	GND	

10.4 Power Supply Module Fans

Each installed power supply module includes embedded (non-removable) 40-mm fans. These fans provide airflow through the power supply module and are managed by the fan control system of the power supply. Should a fan fail, the power supply shuts down.

10.5 Fan Speed Control

The BMC controls and monitors system fans. Each fan is associated with a fan speed sensor that detects fan failure and may also be associated with a fan presence sensor for hot-swap support. For redundant fan configurations, the fan failure status and fan presence status determine the fan redundancy sensor state.

The system fans are divided into fan domains, each of which has a separate fan speed control signal and a separate configurable fan control policy. A fan domain can have a set of temperature and fan sensors associated with it. These sensors are used to determine the current fan domain state.

A fan domain has three states: sleep, boost, and nominal. The sleep and boost states have fixed (but configurable through OEM SDRs) fan speeds associated with them. The nominal state has a variable speed determined by the fan domain policy. An OEM SDR record is used to configure the fan domain policy.

The fan domain state is controlled by several factors, listed below in order of precedence from high to low. If any of these conditions apply, the fans are set to a fixed boost state speed.

- An associated fan is in a critical state or missing. The SDR describes which fan domains are boosted in response to a fan failure or removal in each domain. If a fan is removed when the system is in fans-off mode, it is not detected and there is not any fan boost until the system comes out of fans-off mode.
- Any associated temperature sensor is in a critical state. The SDR describes which temperaturethreshold violations cause fan boost for each fan domain.
- The BMC is in firmware update mode, or the operational firmware is corrupted.
- If any of the above conditions apply, the fans are set to a fixed boost state speed.

For more information on nominal fan speed, see Section 10.5.5.

10.5.1 Increasing Fan Speed

The system provides a BIOS Setup option to boost the system fan speed by a programmable Fan Pulse Width Modulation (PWM) positive offset setting. Enabling the **Fan PWM Offset** option causes the BMC to add the offset to the fan speeds to which it would otherwise be driving the fans. This setting causes the BMC to replace the domain minimum speed with alternate domain minimums that are also programmable through SDRs.

This capability is offered to provide system administrators the option to manually configure fan speeds in instances where the fan speed optimized for a given platform may not be sufficient when a high-end add-in adapter is configured into the system. This capability enables easier usage of the fan speed control to support Intel and non-Intel chassis and better support of ambient temperatures higher than 35 °C.

10.5.2 Hot-Swappable Fans

Hot-swap fans are supported, they can be removed and replaced while the system is powered on and operating. The BMC implements fan presence sensors (sensor type = Fan (04h), event / reading type = Generic (08h) for each hot-swappable fan.

When a fan is not present, the associated fan speed sensor is put into the reading/unavailable state, and any associated fan domains are put into the boost state. The fans may already be boosted due to a previous fan failure or fan removal.

When a removed fan is inserted, the associated fan speed sensor is re-armed. If no other critical conditions are causing a fan boost condition, the fan speed returns to the nominal state. Power cycling or resetting the system re-arms the fan speed sensors and clears fan failure conditions. If the failure condition is still present, the fan returns to its boosted state once the sensor has re-initialized and the threshold violation is detected again.

10.5.3 Fan Redundancy Detection

The BMC supports redundant fan monitoring and implements a fan redundancy sensor. A fan redundancy sensor generates events when its associated set of fans transitions between redundant and non-redundant states, as determined by the number and health of the fans.

Note: The definition of fan redundancy is server system configuration dependent. The BMC allows for redundancy to be configured on a per-fan redundancy sensor basis through OEM SDR records.

A fan failure or removal of hot-swap fans up to the number of redundant fans specified in the SDR in a fan configuration is a non-critical failure and is reflected in the front panel status. A fan failure or removal that exceeds the number of redundant fans is a non-fatal, insufficient-resources condition and is reflected in the front panel status as a non-fatal error. In the front control panel, a blinking green system status LED indicates non-critical error and a blinking amber LED indicates non-fatal error.

Redundancy is checked only when the system is in the DC-on state. Fan redundancy changes that occur when the system is DC-off or when AC is removed will not be logged until the system is turned on.

10.5.4 Fan Control Mechanism

System fan speeds are controlled through Pulse Width Modulation (PWM) signals that are driven separately for each domain by integrated PWM hardware. Fan speed is changed by adjusting the duty cycle, which is the percentage of time the signal is driven high in each pulse.

The BMC controls the average duty cycle of each PWM signal through direct manipulation of the integrated PWM control registers.

The same device may drive multiple PWM signals.

10.5.5 Nominal Fan Speed

A fan domain's nominal fan speed can be configured as static (fixed value) or controlled by the state of one or more associated temperature sensors.

OEM SDR records are used to configure which temperature sensors are associated with which fan control domains and the algorithmic relationship between the temperature and fan speed. Multiple OEM SDRs can reference or control the same fan control domain and multiple OEM SDRs can reference the same temperature sensors.

Hysteresis can be specified to minimize fan speed oscillation and to smooth fan speed transitions. If a Tcontrol SDR record does not contain a hysteresis definition (for example, an SDR adhering to a legacy format), the BMC assumes a hysteresis value of zero.

10.5.6 Thermal and Acoustic Management

This feature allows for enhanced fan management to keep the system optimally cooled while reducing the amount of noise generated by the system fans. Aggressive acoustics standards might require a trade-off between fan speed and system performance parameters that contribute to the cooling requirements, primarily memory bandwidth. The BIOS, BMC, and SDRs work together to provide control over how this trade-off is determined.

This capability requires the BMC to access temperature sensors on individual memory DIMMs. Additionally, closed-loop thermal throttling is only supported with DIMMs containing temperature sensors.

10.5.7 Thermal Sensor Input to Fan Speed Control

The BMC uses various IPMI sensors as input to the fan speed control. Some of the sensors are IPMI models of actual physical sensors, whereas some are "virtual" sensors whose values are derived from physical sensors using calculations and/or tabular information.

The following IPMI thermal sensors are used as input to fan speed control:

- Front panel temperature sensor ¹
- Processor margin sensors ^{2, 4, 5}
- DIMM thermal margin sensors ^{2, 4}
- Exit air temperature sensor 1, 7, 9
- PCH temperature sensor 3, 5
- Onboard Ethernet controller temperature sensors 3,5
- PSU thermal sensor 3,8
- Processor VR temperature sensors ^{3, 6}
- DIMM VR temperature sensors ^{3, 6}
- BMC temperature sensor 3, 6
- Global aggregate thermal margin sensors ⁷
- Riser card temperature sensors

Notes:

- ¹ For fan speed control in Intel® chassis
- ² Temperature margin to max junction temp
- ³ Absolute temperature
- ⁴ PECI value or margin value
- ⁵ On-die sensor
- ⁶ Onboard sensor
- ⁷ Virtual sensor
- ⁸ Available only when PSU has PMBus
- ⁹ Calculated estimate

The following figure shows a high-level representation of the fan speed control structure that determines fan speed.

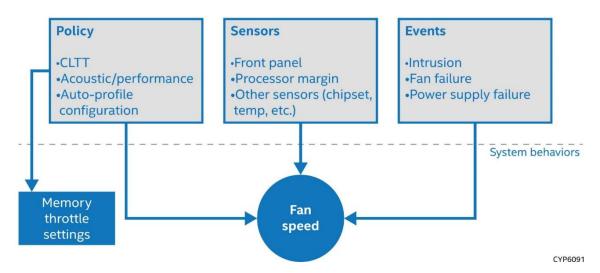


Figure 87. High-Level Fan Speed Control Model

10.6 Liquid-Cooling Support

Select system configurations in the Intel® Server System D50TNP support liquid-cooling on the installed server modules through an integrated liquid-cooling loop. The liquid-cooling loop is designed as a passive component in terms of coolant flow that captures heat from the processors and memory inside the module.

The coolant flow for the liquid-cooling loop is supported through liquid-cooling plumbing connections installed in the back of the server chassis. The liquid-cooling loops from all installed modules in the system are connected in parallel to the chassis plumbing connections. The chassis plumbing connections include two Staubli* SCG 06 quick disconnect couplings to connect to coolant supply and return.



Figure 88. Chassis Plumbing Couplings Identification

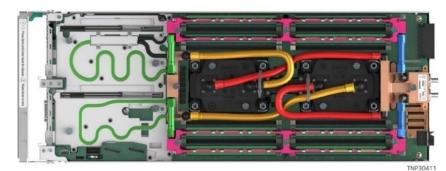
10.6.1 Liquid-Cooling Loop Components

The dedicated liquid-cooling loop in the modules consists of the following components:

- One passive cold plate loop
- Eight memory cooling clips
- Blind-mate quick disconnect couplings
- Liquid-cooling tubes (filled with liquid-coolant)

10.6.2 Liquid-Cooling Loop Operation

The dedicated liquid-cooling loop kit has three basic elements: retention and cold plate units, memory cooling heat spreaders, and coolant tubes to transport the liquid. The cold plates are a direct replacement for the standard processor air-cooled heat sink. The cold plates and cooling pads transfer the heat from the CPU and memory respectively to the cooling liquid. A non-Intel coolant distribution unit (not included) connected to the chassis plumbing continuously pushes the warm liquid to the exterior and draws cool liquid back to the cold plates. The flow rate in conjunction with the enhanced heat transfer cold plates and heat spreaders capture heat from the surface of the processor and the installed memory. The system fans pull air across the system exhausting heat from the other components on the Intel® D50TNP Modules and chassis to the outside of the system. Figure 89 shows the liquid-cooling loop kit flow path as the liquid-coolant passes through the module.



Flow order	Component
First	Quick disconnect inlet manifold
Second	DIMM Banks 1 and 2 – cooled in parallel
Third	Conduction plate for M.2, PCIe* add-in cards, PCH, and board components
Fourth	Cold plates for CPU 0 and CPU 1 – cooled in parallel
Fifth	Coolant return outlet

Figure 89. Liquid-Cooling Loop Flow Map

See the Intel® Server D50TNP Family Integration and Service Guide for specific instructions regarding the removal and installation of the liquid-cooling loop.

10.6.3 Liquid-Cooling Loop Specification

The cold plate assembly in the liquid-cooling loop mounts directly on top of the processors. The retention mechanism for installation on top of the processors is integrated into the cold plate. The liquid-coolant contained in the tubes is a mixture of demineralized water and propylene glycol with the benefits of being anti-freeze, anti-corrosion, and anti-bacterial. Table 33 and Table 34 list the features and specifications of the liquid-cooling loop kit.

Intel® Server D50TNP Family Technical Product Specification

Table 33. Liquid-Cooling Loop Specifications

Specification	Value	
Cold plate material	Copper	
Thermal Interface Material	Dowsil TC-5026	
Memory heat spreader Thermal Interface Material	Laird Tflex 340H	
Height	34.05 mm	
Weight	6.94 lbs. (3.15 kg)	

Table 34. Liquid-Cooling Loop Operation Temperature Specifications

Specification	Value	
Operating Liquid Temperature	Minimum: 2 °C	
Operating Liquid Temperature	Maximum: 65 °C	
Operating Air temperature	35 ℃	
Facility supply liquid temperature (primary loop)	2–45 °C (W4 ASHRAE)	
System supply liquid temperature (secondary loop)	7–50°C (Assumed 5°C Approach Temperature)	
Coolant flow rate	0.4–1.16 l/min (per Intel® D50TNP Module)	
Operating humidity	5–95%	
Storage temperature	-40 through 70 °C	
Storage humidity	5–95%	

Important Note: The liquid-cooling loop and the chassis plumbing are pre-charged with liquid coolant.

10.6.4 System Coolant Flow Rate Requirements

For liquid cooled system configurations, a minimum coolant flow rate is required depending on the coolant temperature. The following figure shows the required coolant flow rates per coolant temperature according to different processor and memory configurations. The flow rate is measured in liters per minute with a maximum supported flow rate of 4.6 liters/minute. The temperature is measured in degrees Celsius with a maximum supported temperature of 50 °C. This maximum temperature is based on a W4 class facility water-supply temperature (2–45 °C, ASHRAE) and a Coolant Distribution Unit (CDU) approach temperature of 5 °C. The different flow rates in the figure represent the minimum required conditions to keep the system operating within supported maximum thermal limits. Flow rates below the ones listed are not supported and may cause system throttling.

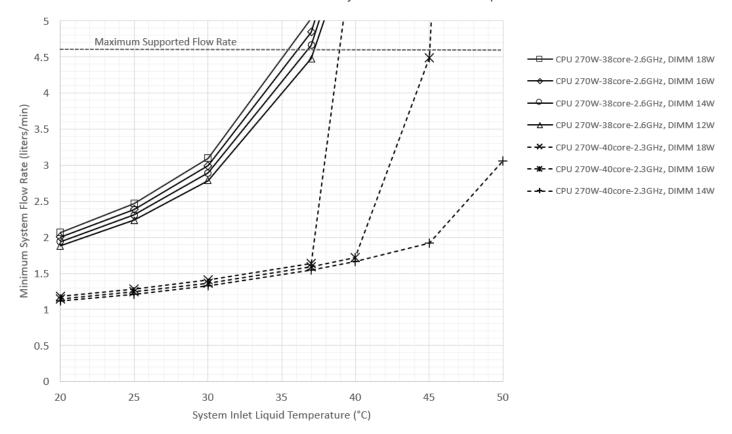


Figure 90. System Coolant Flow Rate Requirements

10.7 FRUSDR Utility

The purpose of the embedded platform management and fan control systems is to monitor and control various system features, and to maintain an efficient operating environment. Platform management is also used to communicate system health to supported platform management software and support mechanisms. The FRUSDR utility is used to program the server board with platform specific environmental limits, configuration data, and the appropriate sensor data records (SDRs) for use by these management features. As part of the system manufacturing process, a default software stack is loaded that contains FRU and SDR data. However, this software may not be the latest available version. Intel recommends updating the SDR to the latest available as part of a planned system software update.

The FRUSDR utility for the given server platform can be downloaded as part of the System Update Package (SUP) or System Firmware Update Package (SFUP) from http://downloadcenter.intel.com.

Note: The embedded platform management system may not operate as expected if the platform is not updated with accurate system configuration data. The FRUSDR utility must be run with the system fully configured during the initial system integration process for accurate system monitoring and event reporting.

11. System Power

The Intel® Server System D50TNP supports the following power supply options:

- AC 1600 W (80 Plus Titanium)
- AC 2100 W (80 Plus Platinum)

The server system can support up to three power supplies. Each power supply is hot-swappable and allows tool-less insertion and extraction from the rear of the chassis.

Disclaimer: The Intel® Server D50TNP Family is designed to operate as described in this technical product specification when connected to a 200–240 V power source. Connecting to a lower voltage power line is not supported and may result in unreliable system operation. If a 200–240 V power source is not available, it is the responsibility of the system integrator to recalculate the total power consumption of the system. See Table 9 for details.

Note: In systems with more than one power supply configurations, all power supplies must be identical. Using different power supply options concurrently is not supported. This invalid configuration will not provide power supply redundancy and will result in multiple errors being logged by the system.

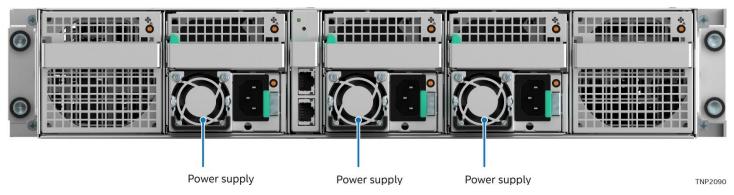


Figure 91. Power Supply Module Identification - Air Cooled

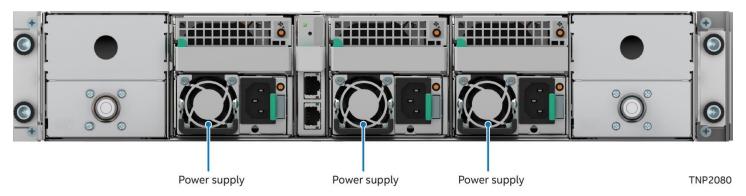


Figure 92. Power Supply Module Identification – Liquid Cooled

Intel® Server D50TNP Family Technical Product Specification



Figure 93. Power Supply Module Partially Out of Chassis



Figure 94. Power Supply Module

To minimize the risk of accidental power cord extraction, each power supply supports a power cord retention strap.

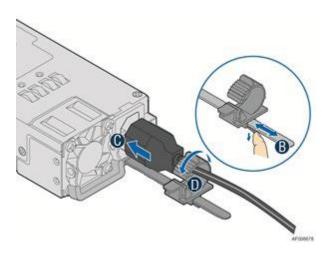


Figure 95. Power Cord Retention Strap

11.1 Power Supply Configurations

The server system can have up to three power supply modules installed and can support the following power supply configurations:

- 2+1 redundant power
- 3+0 combined power (non-redundant)

2+1 redundant power and 3+0 combined power configurations are automatically configured depending on the number of modules in the system. If the server system has two modules, the three power supplies will work in a 2+1 power configuration. If the server system has four modules, the three power supplies will work in a 3+0 power configuration. Should system thermal levels exceed programmed limits, platform management attempts to keep the system operational. For details, see Section 11.2 and Chapter 10.

In the event of a power supply failure, the redundant 2+1 power supply configuration supports hot-swap extraction and replacement of the failed power supply. The AC input is auto-ranging and power factor corrected. In the event of a power supply failure in a 3+0 configuration, the other two power supplies provide the power and the system may throttle.

11.2 Intel® Power Calculator Tool

For system integrators that would like to determine the system power draw and heat dissipation for a specific system configuration, Intel makes available an online power calculator tool accessible at the following Intel web site: https://servertools.intel.com/tools/power-calculator/

11.3 Closed Loop System Throttling (CLST)

Closed Loop System Throttling (CLST) is supported. CLST prevents the system from crashing if a power supply module is overloaded or overheats. If the system power reaches a pre-programmed power limit, CLST throttles system memory and/or processors to reduce power. System performance is degraded if throttling occurs.

11.4 Smart Ride Through (SmaRT) Throttling

Smart Ride Through (SmaRT) throttling is supported. SmaRT increases the reliability of a system operating in a heavy power load condition and to remain operational during an AC line dropout event.

When AC voltage is too low, a fast AC loss detection circuit inside each installed power supply asserts an SMBALERT# signal to initiate a throttle condition in the system. System throttling reduces the bandwidth to both system memory and processors, which, in turn, reduces the power load during the AC line drop out event.

11.5 Cold Redundancy Support

11.5.1 Powering on Cold Standby Supplies to Maintain Best Efficiency

The system assigns a cold standby state for each installed power supply, depending on the power demand for operation. The assigned state or position can be 1, 2, or 3. The BMC uses a signal that can be identified by the power supplies to enter an active state, should the system power demand rise above a predefined threshold. Depending on which position (1, 2, or 3) the system defines a power supply to be in, the cold standby configuration slightly changes the system power demand threshold that the power supply will power on at.

The VCR_ON_EN signal activates a power supply in cold standby state. The VCR_ON_DIS signal changes an active power supply to a cold standby state. These events are logged in the system event log as CR_BUS asserted or deasserted states.

Table 35. Example System Power Demand Threshold for Activating Power Supplies

State	Enable Threshold for VCR_ON_EN	Disable Threshold for VCR_ON_DIS	CR_BUS De-Asserted/ Asserted States		
Standard Redundancy	NA; Ignore dc/dc_ active# signal;	OK = Tri-state, Fault = Low			
Cold Redundant Active	NA; Ignore dc/dc_ active# signal;	NA; Ignore dc/dc_ active# signal; power supply is always ON			
Cold Standby 1 (02h)	3.2 V (40% of max)	3.2 V (40% of max) 3.2 V x 0.5 x 0.9 = 1.44 V			
Cold Standby 2 (03h)	5.0 V (62% of max) 5.0 V x 0.67 x 0.9 = 3.01 V		OK = Tri-state, Fault = Low		
Cold Standby 3 (04h)	6.7 V (84% of max)	6.7 V x 0.75 x 0.9 = 4.52 V	OK = Tri-state, Fault = Low		

Note: Maximum voltage for the VCR ON EN signal is 8.0 V at 100% of rated output power.

Note: Load share bus thresholds are examples. For a given power supply, these thresholds will be customized to maintain the best efficiency curve for that specific power supply model.

11.5.2 Powering on Cold Standby Supplies during a Fault or Over Current Condition

In the event of a power supply failure, the CR_BUS signal for the failing power supply will change to a fault state. When this happens, all parallel power supplies in cold standby mode will power on within 100 μ sec.

11.5.3 BMC Requirements

The BMC uses the <code>Cold_Redundancy_Config</code> command to define and configure the power supply's role in cold redundancy and to turn on/off cold redundancy.

To allow for equal loading over the life time of installed power supplies, the BMC schedules a rolling reconfiguration of installed power supplies. Each one alternates between being the "Active" power supply and the "Cold Stby" power supply.

Events that trigger a re-configuration of the power supplies using the Cold_Redundancy_Config command are listed below.

- AC power ON
- PSON power ON
- Power supply failure
- Power supply inserted into system

11.5.4 Power Supply Turn on Function

Powering on and off the cold standby power supplies is only controlled by each PSU sensing the Vshare bus. Once a power supply turns on after crossing the enable threshold, it lowers itself to the disabled threshold. The system defines the position of each power supply in the cold redundant operation. It does this each time the system is powered on, a power supply fails, or a power supply is added to the system.

The system is relied upon to tell each power supply where it resides in the cold redundancy scheme.

11.6 Power Supply Specification Overview

The Intel® Server System D50TNP supports the following power supply options:

- AC 1600 W (80 Plus Titanium)
- AC 2100 W (80 Plus Platinum)

AC power supplies are auto-ranging and power factor corrected.

The following sections provide an overview of select power supply features and functions.

Note: Full power supply specification documents are available upon request. Power supply specification documents are classified as Intel Confidential and will require a signed nondisclosure agreement (NDA) with Intel before being made available.

11.6.1 Power Supply Module Efficiency

Each power supply option is rated to meet specific power efficiency limits based on their 80 PLUS power efficiency rating: Titanium, Platinum, or Gold.

The following tables define the required minimum power efficiency levels based on their 80 PLUS efficiency rating at specified power load conditions: 100%, 50%, 20%, and 10%

The AC power supply efficiency is tested over an AC input voltage range of 115 VAC to 220 VAC.

Table 36. 1600 W AC Power Supply Option Efficiency (80 PLUS* Titanium)

80 PLUS TITANIUM	Loading	100% of maximum	50% of maximum	20% of maximum	10% of maximum
	Minimum Efficiency	91%	96%	94%	90%

Table 37. 2100 W AC Power Supply Option Efficiency (80 PLUS* Platinum)

80 PLUS' PLATINUM	Loading	100% of maximum	50% of maximum	20% of maximum	10% of maximum	
PLUS	Minimum Efficiency	91%	94%	90%	82%	

11.6.2 AC Power Cord Specifications



Figure 96. AC Power Cable Connector

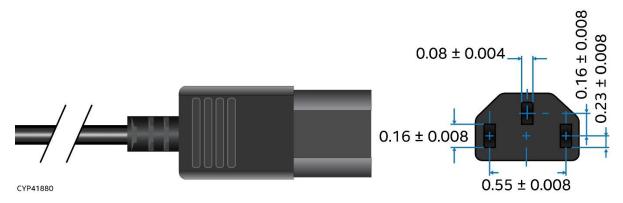


Figure 97. AC Power Cord Specification

The AC power cord used must meet the specification requirements listed in the following table.

Table 38. AC Power Cord Specifications

Item	Description		
Cable Type	SJT		
Wire Size	14 AWG		
Temperature Rating	105 ºC		
Amperage Rating	10 A at 240 V		
Voltage Rating	240 VAC		

11.7 Power Supply Features

The following sections describe features supported by the AC power supply options.

11.7.1 Power Supply Status LED

A single bi-color LED indicates power supply status. The operational states of this bi-color LED are defined in the following table.

Table 39. LED Indicators

LED State	Power Supply Condition
Solid green	Output ON and OK.
Off	No source power to all power supplies.
1 Hz blinking green	Source power present/only 12 VSB on (PS off) or PS in cold redundant state.
Solid amber	Source power cord unplugged or source power lost; with a second power supply in parallel still with AC input power. Or power supply critical event causing a shutdown; failure, OCP, OVP, fan fail.
1 Hz blinking amber	Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.
2 Hz blinking green	Power supply firmware updating.

11.7.2 Protection Circuits

Each installed power supply module includes several protection circuits that will shut down the power supply in the event a defined operating threshold is exceeded.

11.7.2.1 Over Current Protection (OCP)

Each installed power supply is protected against over current. The power supply unit shuts down for a specific time period after crossing current thresholds. A power supply that is shut down due to an exceeded protection circuit threshold can be reset by removing source power for 15 seconds.

Table 40. Over Current Protection, 2100 W Power Supply

Output Voltage	Input Voltage Range	Over Current Limits	OCP Delay
+12 V	180–264 VAC	252 A minimum / 258 A maximum	50 msec minimum / 200 msec maximum
		269 A minimum / 277 A maximum	5 msec minimum / 20 msec maximum
12 VSB	90–264 VAC	3.6 A minimum / 4.0 A maximum	10 msec minimum / 20 msec maximum

Table 41. Over Current Protection, 1600 W Power Supply

Output Voltage	Input Voltage Range	Over Current Limits	OCP Delay	
+12 V	180–264 VAC	155 A minimum / 165 A maximum	30 msec minimum / 100 msec maximum	
12 VSB	90–264 VAC	3.6 A minimum / 4.0 A maximum	1 msec minimum / 100 msec maximum	

Table 42. Over Voltage Protection (OVP) Limits, 1600 W and 2100 W Power Supply

Output Voltage	Minimum (V)	Maximum (V)
+12 V	13.5	14.5
+12 VSB	13.5	14.5

11.7.2.2 Over Temperature Protection (OTP)

Each installed power supply is protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. The power supply unit shuts down during an OTP condition. Once the power supply temperature drops to within specified limits, the power supply restores power automatically.

Note: The 12 VSB always remains on while the power supply is connected to the power source.

11.8 Power Distribution Board (PDB)

The Intel® Server System D50TNP includes a power distribution board in the back of the chassis that provides power and management connections for several components in the system. The following figure shows the location of the PDB in the system.

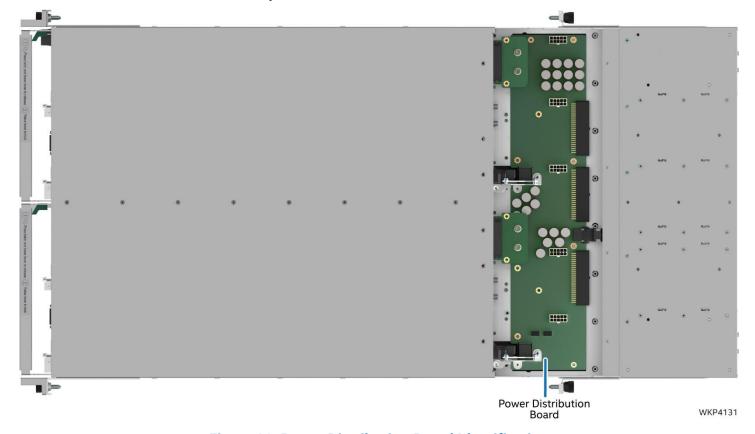


Figure 98. Power Distribution Board Identification

The power distribution board includes the following connectors:

- Three power supply interface connectors in the rear
- One EMP Module docking port in the rear
- Five system fan connectors on top
- Two management risers with high speed management ports, for communication between the Compute Modules, the EMP module and system fans
- Four power connectors in the front, for providing power to the Compute Modules

The following figure identifies the different connectors in the power distribution board.

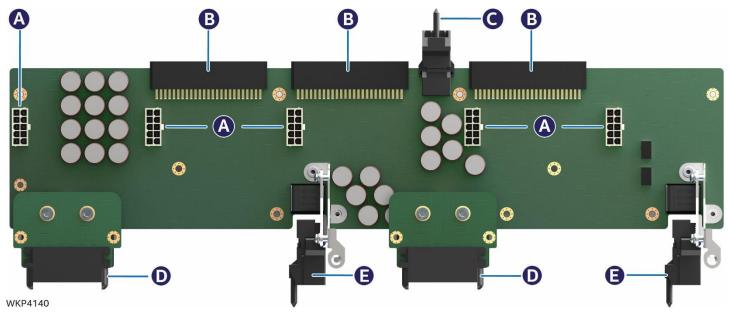


Figure 99. Power Distribution Board Connector Identification

Table 43. Power Distribution Board Connector Identifiers

Connector Identifier	Description
A	System fan connectors
В	Power supply connectors
С	EMP module docking port
D	Compute module power connectors
E	Management risers

12. Platform Management

The Intel® Server System D50TNP Family uses the baseboard management controller (BMC) features of an Aspeed* AST2500 server management processor. The BMC supports multiple system management features including intra-system sensor monitoring, fan speed control, system power management, and system error handling and messaging. It also provides remote platform management capabilities including remote access, monitoring, logging, and alerting features.

In support of system management, the system includes a dedicated management port and support for two system management tiers and optional system management software.

- Standard management features (Included)
- Advanced management features (\$\$ Optional)
- Intel® Data Center Manager (Intel® DCM) support (\$\$ Optional)

The following subsections provide a brief description of each.

12.1 Management Port

The Intel® D50TNP Modules include a dedicated 1 Gb/s RJ45 management port used to access embedded system management features remotely.

Note: The management port is dedicated for system management access purposes only. The port is not intended or designed to support standard LAN data traffic.

For more information on the dedicated management port, including LED definition, see Section 9.2.1.2.



Figure 100. Dedicated Management Port Location – 1U Compute Modules

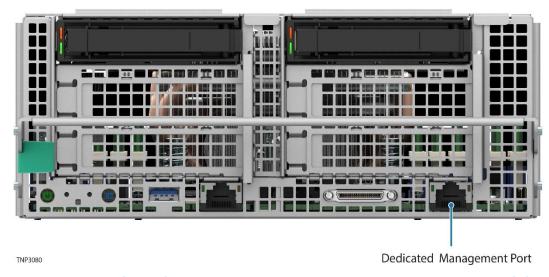


Figure 101. Dedicated Management Port Location – 2U Management Module

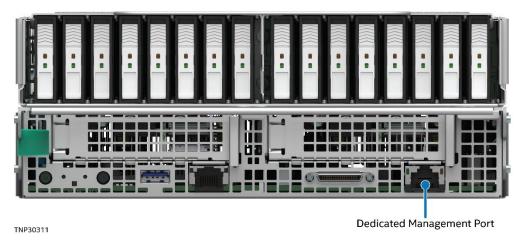


Figure 102. Dedicated Management Port Location – 2U Storage Module



Figure 103. Dedicated Management Port Location – 2U Accelerator Module

To access the server remotely using the management port requires network parameters to be configured using the <F2> BIOS Setup utility.

12.1.1 Configuring System Management Port Using <F2> BIOS Setup

- 1. During the system power-on POST process, press **<F2>** when prompted to go to the BIOS Setup utility main menu page.
- 2. Navigate to the **Server Management** tab and select **BMC LAN Configuration** to enter the BMC LAN Configuration screen (Figure 104).

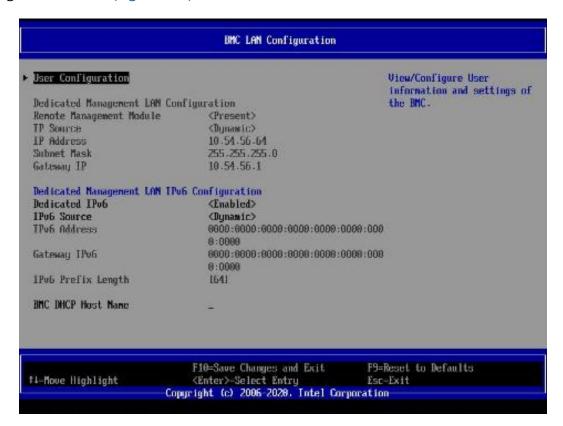


Figure 104. BIOS Setup BMC LAN Configuration Screen

- 3. The system is configured using the **BMC LAN Configuration**
- 4. For an IPv4 network:
 - If configuring the server management BMC LAN, scroll to Dedicated Management LAN
 configuration > IP source and then select either Static or Dynamic. If Static is selected, configure
 the IP address, Subnet mask, and Gateway IP as needed.
- 5. For an IPv6 network:
 - If configuring the server management BMC LAN, scroll to Dedicated Management LAN IPv6
 configuration > Dedicated IPv6 and then select Enabled. Then scroll to IPV6 source and select
 either Static or Dynamic. If Static is selected, configure the IPV6 address, Gateway IPV6, and
 IPV6 Prefix Length as needed.
- 6. To change the User and Password, select **BMC User Configuration** to enter the User Configuration screen (Figure 105).
- 7. Under **User ID**, set the following settings as desired:
 - Privilege Select the privilege to be used. (Administrator privilege is required to use KVM or media redirection).
 - User Status Select Enabled.
 - o **User Name** Enter the desired name. The anonymous user cannot be changed.
 - User password Enter the desired password twice.
- 8. Press **<F10>** to save the configured settings and exit BIOS Setup. The server reboots with the new LAN settings.



Figure 105. BIOS Setup User Configuration Screen

Once the management port is configured, the server can be accessed remotely to perform system management features defined in the following sections.

12.2 Standard System Management Features

The following system management features are supported on the Intel® Server D50TNP Family by default.

- Virtual KVM over HTML5
- Integrated BMC Web Console
- Redfish
- IPMI 2.0
 - Node Manager
- Out-of-band BIOS/BMC Update and Configuration
- System Inventory
- Autonomous Debug Log

The following subsections provide a brief description for each feature.

12.2.1 Virtual KVM over HTML5

The BMC firmware supports keyboard, video, and mouse redirection (KVM) over LAN. This feature is available remotely from the embedded web server as an HTML5 application. USB1.1 or USB 2.0 based mouse and keyboard redirection are supported. It is also possible to use the KVM-redirection (KVM-r) session concurrently with media-redirection (media-r). This feature allows a user to interactively use the keyboard, video, and mouse (KVM) functions of the remote server as if the user were physically at the managed server.

KVM redirection consoles support the following keyboard layouts: English, Chinese (traditional), Japanese, German, French, Spanish, Korean, Italian, and United Kingdom. KVM redirection includes a "soft keyboard" function. The "soft keyboard" is used to simulate an entire keyboard that is connected to the remote system. The "soft keyboard" functionality supports the following layouts: English, Dutch, French, German, Italian, Russian, and Spanish.

The KVM-redirection feature automatically senses video resolution for best possible screenshot and provides high-performance mouse tracking and synchronization. It allows remote viewing and configuration in pre-boot POST and BIOS Setup once BIOS has initialized video.

12.2.2 Integrated BMC Web Console

The BMC firmware has an embedded web server that can remotely serve web pages to any supported browser. This web console allows administrator to view system information including firmware versions, server health, diagnostic information, power statistics. The web console enables configuration of the BMC and BIOS. It provides the ability for users to perform power actions, launch KVM and set up virtual media redirection.

Enter the configured IP address of the BMC management port into the web browser to open the Integrated BMC Web Console module login page (See Figure 106). To use a secure connection, type:

```
https://<IPaddress or Hostname>/
```

Enter the username and password and select a language option. For example:

Username: rootPassword: superuserLanguage: English

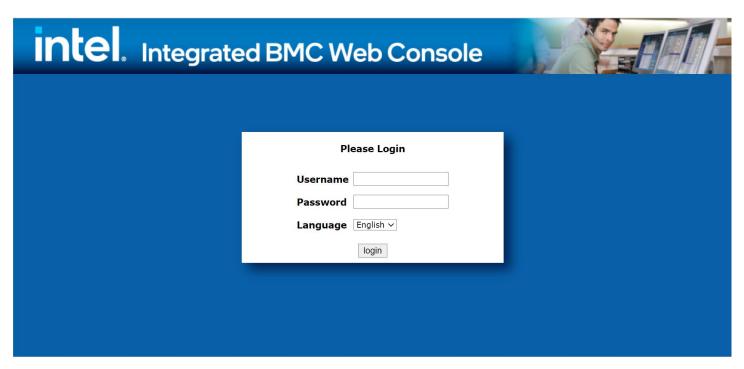


Figure 106. Integrated BMC Web Console Login Page

Click the **Login** button to view the home page.

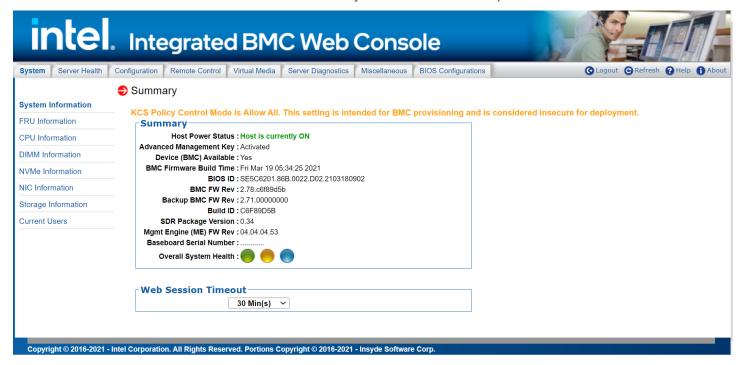


Figure 107. Integrated BMC Web Console - Main Console View

For setup and additional information about this utility, download the *Intel® Integrated Baseboard Management Controller Web Console (Intel® BMC Web Console) User Guide.*

12.2.3 Redfish* Support

The BMC currently supports version 1.7 and schema version 2019.1. DMTF's Redfish* is a standard designed to deliver simple and secure management for converged, hybrid IT and the Software Defined Data Center (SDDC). Both human readable and machine capable, Redfish leverages common Internet and web services standards to expose information directly to the modern tool chain.

12.2.4 IPMI 2.0 Support

The BMC is IPMI 2.0 compliant including support for Intel® Dynamic Power Node Manager. IPMI defines a set of interfaces used by system administrators for out-of-band management of computer systems and monitoring of their operation.

12.2.5 Out-of-Band BIOS / BMC Update and Configuration

The BMC supports Redfish schemas and embedded web console features that allow administrators to update the BMC, BIOS, Intel ME and SDR firmware. The BMC firmware also includes Power Supply and Back plan firmware. The BMC update will happen immediately and cause a BMC reset to occur at the end. The BIOS and Intel ME firmware is staged in the BMC and will be updated on the next reboot. The BMC also supports Redfish and embedded web console feature to view and modify BIOS settings. On each boot, BIOS provides all its settings and active value to the BMC to be displayed. BIOS also checks if any changes are requested and performs those changes.

12.2.6 System Inventory

The BMC supports Redfish schemas and embedded web console pages to display system inventory. This inventory includes FRU information, CPU, Memory, NVMe, networking, and storage. When applicable, the firmware version will also be provided.

12.2.7 Autonomous Debug Log

The BMC has a debug log that can be downloaded to facilitate support issues. This debug log can be downloaded from the embedded web console or using the Intel Server Configuration and Intel SDP Tool utilities. The debug log contains configuration data including SDR, SEL, BMC configuration, PCI configuration, power supply configuration, and power supply black box data. The debug log also contains SMBIOS data and the POST codes from the last two system boots. Finally, when the system has a catastrophic error condition leading to a system shutdown, the BMC will hold the CPU in reset long enough to collect processor machine check registers, memory controller machine check registers, I/O global error registers, and other processor state information.

12.2.8 Security Features

The BMC contains several security features including OpenLDAP and Active Directory, security logs, ability to turn off any remote port, Secure Sockets Layer (SSL) certificate upload, VLAN support, and KCS control. The BMC also supports full user management with the ability to define password complexity rules. Each BMC release is given a security version number to prevent firmware downgrades from going to lower security versions. Intel provides a best practices security guide, available at

https://www.intel.com/content/www/us/en/support/articles/000055785/server-products.html

12.3 Advanced System Management Features

Purchasing an optional Advanced System Management product key (iPC: ADVSYSMGMTKEY), unlocks the following advanced system management features:

- Virtual Media Image Redirection (HTML5 and Java)
- Virtual Media over network share and local folder
- Active Directory support
- Included single system license for Intel® Data Center Manager (Intel® DCM)
 - Intel® Data Center Manager (Intel® DCM) is a software solution that collects and analyzes the realtime health, power, and thermals of a variety of devices in data centers helping you improve the efficiency and uptime. For more information, go to https://www.intel.com/content/www/us/en/software/intel-dcm-product-detail.html
- Future Feature Additions Tentative availability Q4 2022
 - Full system firmware update including drives, memory, and RAID
 - Storage and network device monitoring
 - Out-of-band hardware RAID Management for latest Intel RAID cards

The Advanced System Management product key can be purchased and pre-loaded onto the system when ordering a fully integrated server system directly from Intel using its online Configure-to-Order (CTO) tool. Or the Advanced System Management product key can be purchased separately and installed later. When purchasing the product key separately from the system, instructions will be provided on where to register the product key with Intel. A license file is then downloaded onto the system where the Integrated BMC Web Console or the Intel Server Configuration Utility are used to upload the key to the BMC firmware to unlock the advanced features.

12.3.1 Virtual Media Image Redirection (HTML5 and Java)

The BMC supports media redirection of local folders and .IMG and .ISO image files. This redirection is supported in both HTML5 and Java remote console clients. When the user selects "Virtual Media over HTML5", a new web page will be displayed that provides the user interface to select which type of source media (image file or file folder*) to mount. The web page then allows the user to select the desired media to make available to the server system. After the type and specific media are selected, the interface provides a mount/unmount interface so the user can connect the media to or disconnect the media from the server

system. Once connected, the selected image file or file folder is presented in the server system as standard removable media and may be interacted within the normal fashion based on the operating system running on the server system. This feature allows system administrators the ability to install software (including operating system installation), copy files, perform firmware updates, and so on from media on their remote workstation.

Note: The file folder share is presented to the server system as a UDF file system; the server system operating system must be able to interact with UDF file systems for this feature to be used with the operating system.

12.3.2 Virtual Media over Network Share and Local Folder

In addition to supporting virtual media redirection from the remote workstation (see Section 12.3.1), the BMC also supports media redirection of file folders and .IMG and .ISO files hosted on a network file server accessible to the BMC network interface. The current version supports Samba shares (Microsoft* Windows* file shares) and NFS shares. This virtual media redirection is more effective for mounting virtual media at scale, instead of processing all files from the workstation's drive through the HTML5 application and over the workstation's network. Each BMC makes a direct network file share connection to the file server and accesses files across that network share directly.

12.3.3 Active Directory* Support

The BMC supports Active Directory. Active Directory (AD) is a directory service developed by Microsoft* for Windows domain networks. This feature allows users to log in to the web console or Redfish* using an Active Directory username instead of local authentication. The feature allows administrators to only change passwords on this single domain account instead on every remote system.

12.4 Intel® Data Center Manager (Intel® DCM) Support

Intel® DCM is a solution for out-of-band monitoring and managing the health, power, and thermals of servers and a variety of other types of devices.

What can you do with Intel® DCM?

- Automate health monitoring
- Improve system manageability
- Simplify capacity planning
- Identify underutilized servers
- Measure energy use by device
- Pinpoint power/thermal issues
- Create power-aware job scheduling tasks
- Increase rack densities
- Set power policies and caps
- Improve data center thermal profile
- Optimize application power consumption
- Avoid expensive PDUs and smart power strips

For more information, go to

https://www.intel.com/content/www/us/en/software/intel-dcm-product-detail.html

Note: See Section 1.2 for references to the Intel® Data Center Manager (Intel® DCM) Product Brief and Intel® Data Center Manager (Intel® DCM) Console User Guide.

13. System Software Stack

The server modules include a system software stack that consists of the following components:

- System BIOS
- BMC firmware
- Intel® Management Engine (Intel® ME) firmware / Intel® Server Platform Services (Intel® SPS)
- Field Replaceable Unit (FRU) and Sensor Data Record (SDR) data

Together, they configure and manage features and functions of the server system.

Many features and functions of the server system are managed jointly by the system BIOS and the BMC firmware, including:

- Intelligent Platform Management Interface (IPMI) watchdog timer
- Messaging support, including command bridging and user/session support
- BIOS boot flags support
- Event receiver device: The BMC receives and processes events from the BIOS.
- Serial-over-LAN (SOL)
- ACPI state synchronization: The BMC tracks ACPI state changes that are provided by the BIOS.
- Fault resilient booting (FRB): Fault resistant boot level 2 (FRB-2) is supported by the watchdog timer functionality.
- Front panel management: The BMC controls the system status LED and system ID LED. It supports
 secure lockout of certain front panel functionality and monitors button presses. The system ID LED is
 turned on using a front panel button or a command
- DIMM temperature monitoring: New sensors and improved acoustic management using closed-loop fan control algorithm comprehending DIMM temperature readings
- Integrated KVM (Keyboard, Video, and Mouse)
- Integrated remote media redirection
- Intel® Intelligent Power Node Manager support
- Sensor and system event log (SEL) logging additions/enhancements (e.g., additional thermal monitoring capability)
- Embedded platform debug feature that allows capture of detailed data for later analysis by Intel

A factory installed system software stack is pre-programmed on each server module. However, later revisions may be available. To ensure optimal system operation, Intel recommends the following:

- Power up the module and access the onboard BIOS Setup utility to verify the version numbers of the installed system software stack: BIOS, BMC firmware, Intel® ME firmware, FRU, and SDR.
- Check the following Intel website for possible updates: http://downloadcenter.intel.com
- Download and update the software stack if later revisions are available

System updates can be performed in several operating environments, including the UEFI shell using the UEFI-only system update package (SUP), or under different operating systems using the System Firmware Update Package(SFUP) utility.

See the following Intel documents for more in depth information concerning the system software stack and its functions:

- BIOS Firmware External Product Specification (EPS): Intel NDA Required
- Integrated Baseboard Management Controller Firmware External Product Specification (EPS): Intel NDA Required

13.1 Hot Keys Supported During POST

Certain hot keys are recognized during power-on self-test (POST). A hot key is a key or key combination that is recognized as an unprompted command input. In most cases, hot keys are recognized even while other processing is in progress.

BIOS supported hot keys are only recognized by the system BIOS during the system boot time POST process. Once the POST process has completed and transitions the system boot process to the operating system, BIOS supported hot keys are no longer recognized.

The following table provides a list of available POST hot keys along with a description for each.

Hot Key	Function
<f2></f2>	Enter the BIOS Setup utility
<f6></f6>	Pop-up BIOS boot menu
<f12></f12>	Network boot
<esc></esc>	Switch from logo screen to diagnostic screen
<pause></pause>	Stop POST temporarily (press any key to resume)

Table 44. POST Hot Keys

13.1.1 POST Logo/Diagnostic Screen

If Quiet Boot is enabled in the BIOS Setup utility, a splash screen is displayed with the standard Intel logo screen or a customized original equipment manufacturer (OEM) logo screen if one is present in the designated flash memory location. By default, Quiet Boot is enabled in the BIOS Setup utility and the logo screen is the default POST display. However, pressing **<Esc>** hides the logo screen and displays the diagnostic screen instead during the current boot.

If a logo is not present in the BIOS flash memory space, or if Quiet Boot is disabled in the system configuration, the POST diagnostic screen is displayed with a summary of system configuration information. The POST diagnostic screen is purely a text mode screen, as opposed to the graphics mode logo screen.

If console redirection is enabled in the BIOS Setup utility, the Quiet Boot setting is disregarded, and the text mode diagnostic screen is displayed unconditionally. This situation is due to the limitations of console redirection that transfers data in a mode that is not graphics-compatible.

13.1.2 BIOS Boot Pop-Up Menu

The BIOS boot selection (BBS) menu provides a boot device pop-up menu that is invoked by pressing the **<F6>** key during POST. The BBS pop-up menu displays all available boot devices. The boot order in the pop-up menu is different from the boot order in the BIOS Setup utility. The pop-up menu simply lists all the available devices from which the system can be booted and allows a manual selection of the desired boot device.

When an administrator password is configured in the BIOS Setup utility, the administrator password is required to access the boot pop-up menu. If a user password is entered, the user is taken directly to the boot manager in the BIOS Setup utility, only allowing booting in the order previously defined by the administrator.

13.1.3 Entering BIOS Setup

To enter the BIOS Setup utility using a keyboard (or emulated keyboard), press the **<F2>** function key during boot time when the OEM or Intel logo screen or the POST diagnostic screen is displayed.

The following instructional message is displayed on the diagnostic screen or under the Quiet Boot logo screen:

```
Press <F2> to enter setup, <F6> Boot Menu, <F12> Network Boot
```

Note: With a USB keyboard, it is important to wait until the BIOS discovers the keyboard. Until the USB controller has been initialized and the keyboard activated, key presses are not read by the system.

When the BIOS Setup Utility is entered, the main screen is displayed initially. However, if a serious error occurs during POST, the system enters the BIOS Setup Utility and displays the error manager screen instead of the main screen.

For additional BIOS Setup utility information, see the BIOS Setup Utility User Guide.

13.1.4 BIOS Update Capability

To bring BIOS fixes or new features into the system, it is necessary to replace the current installed BIOS image with an updated one. Full BIOS update instructions are provided with update packages downloaded from the Intel website.

13.2 Field Replaceable Unit (FRU) and Sensor Data Record (SDR) Data

As part of the manufacturing process, FRU and SDR data is loaded into the Intel® D50TNP Modules in the system. This process ensures that the embedded platform management system can monitor the appropriate sensor data and operate the system with best cooling and performance. This process also ensures that autoconfiguration occurs without the need to perform additional SDR updates or provide other user input to the system when any of the following components are added or removed:

- Module
- Memory
- Power supply
- Fan
- Power distribution board

Intel recommends updating the SDR to the latest available version whenever a system software update is performed.

13.2.1 Loading FRU and SDR Data

The FRU and SDR data can be updated using a stand-alone FRUSDR utility in the UEFI shell or can be done using the Intel utility program under a supported operating system. Full FRU and SDR update instructions are provided with the appropriate system update package (SUP) or System Firmware Update Package (SFUP) utility that can be downloaded from http://downloadcenter.intel.com.

14. System Security

The Intel® Server D50TNP Family supports a variety of security options designed to prevent unauthorized access or tampering of settings. Security options supported include:

- Password protection
- Front panel lockout
- Intel® Platform Firmware Resilience (Intel® PFR)
- Intel® Software Guard Extensions (Intel® SGX)
- Intel® Total Memory Encryption (Intel® TME)
- Trusted Platform Module (TPM) support
- Intel® CBnT Converged Boot Guard and Trusted Execution Technology (Intel® TXT)
- Unified Extensible Firmware Interface (UEFI) Secure Boot Technology

14.1 Password Protection

The BIOS Setup Utility includes a Security tab where options to configure passwords, front panel lockout, and TPM settings are found.

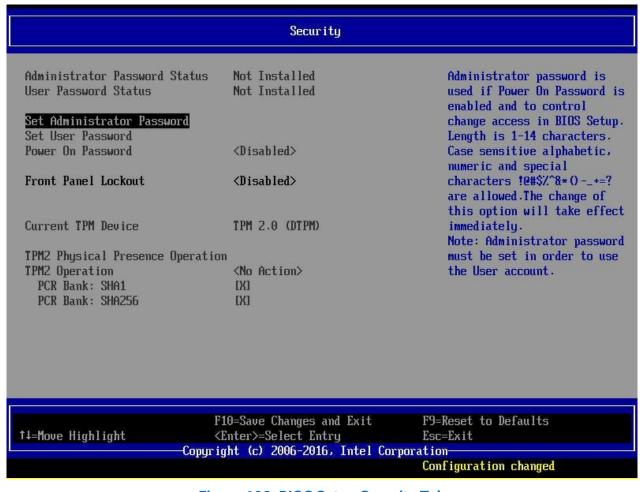


Figure 108. BIOS Setup Security Tab

14.1.1 Password Setup

The BIOS uses passwords to prevent unauthorized access to the server modules. Passwords can restrict entry to the BIOS Setup utility, restrict use of the Boot Device popup menu during POST, suppress automatic USB device re-ordering, and prevent unauthorized system power-on. Intel strongly recommends that an administrator password be set. A system with no administrator password set allows anyone who has access to the server module to change BIOS settings.

An administrator password must be set to set the user password.

The maximum length of a password is 14 characters. The minimum length is one character. The password can be made up of a combination of alphanumeric (a-z, A-Z, 0-9) characters and any of the following special characters:

Passwords are case-sensitive.

The administrator and user passwords must be different from each other. An error message is displayed, and a different password must be entered if there is an attempt to enter the same password for both. The use of strong passwords is encouraged, but not required. To meet the criteria for a strong password, the password entered must be at least eight characters in length, and must include at least one each of alphabetical, numeric, and special characters. If a weak password is entered, a warning message is displayed, and the weak password is accepted. Once set, a password can be cleared by changing it to a null string. This task requires the administrator password and must be done through BIOS Setup. Clearing the administrator password also clears the user password. Passwords can also be cleared by using the password clear jumper on the server board. For more information on the password clear jumper, see Section 15.2.

Resetting the BIOS configuration settings to default values (by any method) has no effect on the administrator and user passwords.

As a security measure, if a user or administrator enters an incorrect password three times in a row during the boot sequence, the system is placed into a halt state. A system reset is required to exit out of the halt state. This feature makes it more difficult to guess or break a password.

In addition, on the next successful reboot, the Error Manager displays a Major Error code 0048. A SEL event is also logged to alert the authorized user or administrator that a password access failure has occurred.

14.1.2 System Administrator Password Rights

When the correct administrator password is entered, the user may perform the following actions:

- Access the BIOS Setup utility.
- Configure all BIOS Setup options in the BIOS Setup Utility.
- Clear both the administrator and user passwords.
- Access the Boot Menu during POST.

If the Power On Password function is enabled in BIOS Setup, the BIOS halts early in POST to request a password (administrator or user) before continuing POST.

14.1.3 Authorized System User Password Rights and Restrictions

When the correct user password is entered, the user can perform the following actions:

- Access the BIOS Setup utility.
- View, but not change, any BIOS Setup options in the BIOS Setup utility.
- Modify system time and date in the BIOS Setup utility.

If the Power On Password function is enabled in BIOS Setup, the BIOS halts early in POST to request a password (administrator or user) before continuing POST.

Configuring an administrator password imposes restrictions on booting the system and configures most setup fields to read-only if the administrator password is not provided. The boot popup menu requires the administrator password to function, and the USB reordering is suppressed as long as the administrator password is enabled. Users are restricted from booting in anything other than the boot order defined in setup by an administrator.

14.2 Front Panel Lockout

If enabled in BIOS Setup from the Security screen, this option disables the following front panel features:

- The off function of the power button.
- System reset button.

If front panel lockout is enabled, power off and reset must be controlled via a system management interface.

14.3 Intel® Platform Firmware Resilience (Intel® PFR)

As the intensity, sophistication, and disruptive impact of security attacks continue to escalate, data centers are driving a holistic approach to protect their critical infrastructure. This includes protecting server systems at the firmware level, the lowest layers of the platform, where threats are most difficult to detect. To address this situation, Intel has developed Intel® Platform Firmware Resilience (Intel® PFR) technology where platforms can provide security starting with power-on, system boot, and operating system load activities.

The Intel® Server D50TNP Family supports Intel® PFR technology, a hardware-enhanced platform security that uses an Intel® FPGA to protect, detect, and recover platform firmware.

- **Protect:** Monitors and filters malicious traffic on system buses. All platform firmware is attested safe before code execution.
- **Detect:** Verifies integrity of platform firmware images before executing. Performs boot and runtime monitoring to assure server is running a known good firmware.
- Recover: Automatically restores corrupted firmware from a protected gold recovery image within minutes.

Critical firmware elements protected in an Intel Server D50TNP Family include: BIOS, SPI Descriptor, BMC, Intel® Management Engine (Intel® ME), and Power Supply firmware. This capability to mitigate firmware corruption is an important industry innovation and provides an optimal solution for security-sensitive organizations.

Intel® PFR fully supports the National Institute of Standards and Technology (NIST*) proposed firmware resiliency guidelines (SP800-193) that have wide industry support.

14.4 Intel® Total Memory Encryption (Intel® TME)

To better protect computer system memory, the 3rd Gen Intel® Xeon Scalable processor has a security feature called Intel® Total Memory Encryption (Intel TME). This feature is supported on the Intel® Server D50TNP Family. Intel TME helps ensure that all memory accessed from the Intel® processors is encrypted, including customer credentials, encryption keys, and other IP or personal information on the external memory bus. Intel® TME is also available for multi-tenant server platforms, called Intel® Total Memory Encryption – Multi-Tenant (Intel® TME-MT).

Intel developed this feature to provide greater protection for system memory against hardware attacks, such as removing and reading the dual in-line memory module (DIMM) after spraying it with liquid nitrogen or installing purpose-built attack hardware. Using the National Institute of Standards and Technology (NIST) storage encryption standard AES XTS, an encryption key is generated using a hardened random number generator in the processor without exposure to software. This situation allows existing software to run unmodified while better protecting memory.

Intel® TME can be enabled directly in the server BIOS and is compatible with Intel® Software Guard Extensions application enclave solutions.

Intel® TME has the following characteristics:

- Encrypts the entire memory using a NIST standard "storage-class" algorithm for encryption: AES-XTS
- **Transparent to software**, it encrypts data before writing to server memory and then decrypts on read.
- **Easy enablement** that requires no operating system or application enabling and is applicable to all operating systems.

To enable/disable Intel® TME, access the BIOS Setup menu by pressing **<F2>** key during POST. Navigate to the following menu: **Advanced > Processor Configuration**

Important Note: When either Intel® TME or Intel® TME-MT is enabled, a subset of memory RAS features and Intel® Optane™ persistent memory 200 series (if installed) will be disabled. See Table 21 for details.

For more information on Intel® TME, see the BIOS Setup Utility User Guide and the BIOS Firmware External Product Specification (EPS).

14.5 Intel Software Guard Extensions (Intel SGX)

Intel Software Guard Extensions (Intel SGX) is a set of instructions that increases the security of application code and data, giving them more protection from disclosure or modification. Developers can partition sensitive information into enclaves that are areas of execution in memory with more security protection.

Intel SGX helps protect selected code and data from disclosure or modification. Intel SGX helps partition applications into enclaves in memory that increase security. Enclaves have hardware-assisted confidentiality and integrity-added protections to help prevent access from processes at higher privilege levels. Through attestation services, a relying party can receive some verification on the identity of an application enclave before launch.

The Intel® Server D50TNP Family provides Intel® SGX as part of the platform system security. Intel® SGX provides fine grain data protection via application isolation in memory. Protected data includes: code, transactions, IDs, keys, key material, private data, algorithms. Intel® SGX provides enhanced security protections for application data independent of operating system or hardware configuration. Intel® SGX provides the following security features:

- Helps protect against attacks on software, even if OS/drivers/BIOS/VMM/SMM are compromised.
- Increases protections for secrets, even when the attacker has full control of platform.
- Helps prevent attacks, such as memory bus snooping, memory tampering, and "cold boot" attacks, against memory contents in RAM.
- **Provides an option for hardware-based attestation** capabilities to measure and verify valid code and data signatures.

Intel® SGX for Intel® Xeon® Scalable processors are optimized to meet the application isolation needs of server systems in cloud environments:

- Massively increased Enclave Page Cache (EPC) size (up to 1 TB for typical two-socket server system).
- Significant performance improvements: minimal impact versus built-in non-encrypted execution (significantly reduced overhead depending on workload).
- Fully software and binary-compatibility with applications written on other variants of Intel® SGX.
- Support for deployers to control which enclaves can be launched.
- Provides deployers full control over Attestation stack, compatible with Intel® Datacenter Attestation primitives.
- Full protection against cyber (software) attacks, some reduction in protection against physical attacks (no integrity/anti-replay protections) vs other Intel SGX variants.
- Designed for environments where the physical environment is still trusted.

Note: Intel® SGX can only be enabled when Intel® TME is enabled. See Section 14.4 to enable Intel® TME.

To enable/disable Intel® SGX, access the BIOS Setup menu by pressing the **<F2>** key during POST. Navigate to the following menu: **Advanced > Processor Configuration**

Important Note: When either Intel® TME or Intel® TME-MT is enabled, a subset of memory RAS features and Intel® Optane™ PMem 200 series (if installed) will be disabled. See Table 21 for details.

For more information on Intel® SGX, see the BIOS Setup Utility User Guide and BIOS Firmware External Product Specification (EPS).

14.6 Trusted Platform Module (TPM) Support

The Trusted Platform Module (TPM) option is a hardware-based security device that addresses the growing concern about boot process integrity and offers better data protection. TPM protects the system startup process by ensuring that it is tamper-free before releasing system control to the operating system. A TPM device provides secured storage to store data, such as security keys and passwords. In addition, a TPM device has encryption and hash functions. The Intel® D50TNP Modules implements TPM as per *TPM PC Client Specifications, Revision 2.0*, published by the Trusted Computing Group (TCG).

A TPM device is optionally installed on the Intel® D50TNP Modules. The device is secured from external software attacks and physical theft. A pre-boot environment, such as the BIOS and operating system loader, uses the TPM to collect and store unique measurements from multiple factors within the boot process to create a system fingerprint. This unique fingerprint remains the same unless the pre-boot environment is tampered with. Therefore, it is used to compare to future measurements to verify the integrity of the boot process.

After the BIOS completes the measurement of its boot process, it hands off control to the operating system loader and, in turn, to the operating system. If the operating system is TPM-enabled, it compares the BIOS TPM measurements to those of previous boots to make sure that the system was not tampered with before continuing the operating system boot process. Once the operating system is in operation, it optionally uses the TPM to provide additional system and data security (for example, Microsoft Windows* 10 supports BitLocker* drive encryption).

Intel offers the following TPM kits for Intel® D50TNP Modules:

- Trusted platform module 2.0 (Rest of World): iPC: AXXTPMENC8 (accessory part)
- Trusted platform module 2.0 (China Version): iPC: AXXTPMCHNE8 (accessory part)

14.6.1 Trusted Platform Module (TPM) Security BIOS

The BIOS TPM support conforms to the TCG (Trusted Computing Group) PC Client Specific Implementation Specification for Conventional BIOS the TCG PC Client Specific TPM Interface Specification, and the Microsoft Windows* BitLocker Requirements. The role of the BIOS for TPM security includes the following:

- Measures and stores the boot process in the TPM microcontroller to allow a TPM-enabled operating system to verify system boot integrity.
- Produces Extensible Firmware Interface (EFI) to a TPM-enabled operating system for using TPM.
- Produces Advanced Configuration and Power Interface (ACPI) TPM device and methods to allow a TPM-enabled operating system to send TPM administrative command requests to the BIOS.
- Verifies operator physical presence. Confirms and executes operating system TPM administrative command requests.
- Provides BIOS Setup options to change TPM security states and to clear TPM ownership.

For additional details, see the TCG PC Client Specific Implementation Specification, the TCG PC Client Platform Physical Presence Interface Specification, and the Microsoft Windows* BitLocker* Requirements documents.

14.6.2 Physical Presence

Administrative operations to the TPM require TPM ownership or physical presence indication by the operator to confirm the execution of administrative operations. The BIOS implements the operator presence indication by verifying the administrator password.

A TPM administrative sequence invoked from the operating system proceeds as follows:

- 1. A user makes a TPM administrative request through the operating system's security software.
- 2. The operating system requests the BIOS to execute the TPM administrative command through TPM ACPI methods and then resets the system.
- 3. The BIOS verifies the physical presence and confirms the command with the operator.
- 4. The BIOS executes TPM administrative command, inhibits BIOS Setup entry, and boots directly to the operating system that requested the TPM command.

14.6.3 TPM Security Setup Options

The BIOS TPM setup allows the operator to view the current TPM state and to carry out rudimentary TPM administrative operations. Performing TPM administrative options through the BIOS Setup requires TPM physical presence verification.

Using the BIOS TPM setup, the operator can turn TPM functionality on or off and clear the TPM ownership contents. After the requested BIOS TPM setup operation is carried out, the option reverts to No Operation.

The BIOS TPM setup also displays the current state of the TPM, whether TPM is enabled or disabled and activated or deactivated. While using TPM, a TPM-enabled operating system or application may change the TPM state independently of the BIOS Setup. When an operating system modifies the TPM state, the BIOS Setup displays the updated TPM state.

The BIOS Setup **TPM Clear** option allows the operator to clear the TPM ownership key and allows the operator to take control of the system with TPM. This option is used to clear security settings for a newly initialized system or to clear a system for which the TPM ownership security key was lost.

14.7 Intel® CBnT – Converged Intel® Boot Guard and Trusted Execution Technology (Intel® TXT)

Previous generation Intel servers supported Intel® Boot Guard and Intel® Trusted Execution Technology (Intel® TXT).

Intel® Boot Guard

- Provides mechanism to authenticate the initial BIOS Code, before BIOS starts
- Hardware-based Static Root of Trust for Measurement (SRTM)
- Defends against attackers replacing/modifying the platform firmware

Intel® TXT

- Provides the ability to attest the authenticity of a platform configuration and OS environment; Establish trust
- Hardware-based Dynamic Root of Trust for Measurement (DRTM)
- Defends against software-based attacks aimed at stealing sensitive information

The two security features combined included some redundancies and inefficiencies between them. With this product generation, Intel rearchitected and fused together the two technologies into Intel® CBnT (Converged Intel® Boot Guard and Trusted Execution Technology). Combining the two technologies into one made them more efficient, eliminated redundancies between them, simplified their implementation, and provided stronger protections.

For more information, visit

https://www.intel.com/content/www/us/en/support/articles/000025873/technologies.html

14.8 Unified Extensible Firmware Interface (UEFI) Secure Boot Technology

UEFI secure boot technology defines how a platform's firmware can authenticate a digitally signed UEFI image, such as an operating system loader or a UEFI driver stored in an option ROM. This situation provides the capability to ensure that those UEFI images are only loaded in an owner authorized fashion and provides a common means to ensure platform security and integrity over systems running UEFI-based firmware. The Intel® Server D50TNP Family BIOS is compliant with the UEFI Specification 2.3.1 Errata C for UEFI secure boot feature.

UEFI secure boot requires built-in UEFI boot mode and it disables legacy Option ROM dispatch. By default, secure boot on Intel® Server D50TNP Family is disabled as the default boot mode is legacy mode.

To enable / disable UEFI Secure Boot, access the BIOS Setup menu by pressing **<F2>** key during POST. Navigate to the following menu: **Boot Maintenance Manager** > **Advanced Boot Options** > **Secure Boot Configuration**.

For more information on UEFI Secure Boot Technology, see the BIOS Setup Utility User Guide and the BIOS Firmware External Product Specification (EPS).

15. Onboard Configuration and Service Jumpers

The server boards include several jumper blocks to configure, protect, or recover specific features of the server board. The following figure identifies the location of each jumper block on the server board. Pin 1 of each jumper is identified by the arrowhead (\P) silkscreened on the server board next to the pin. The following sections describe how each jumper is used.

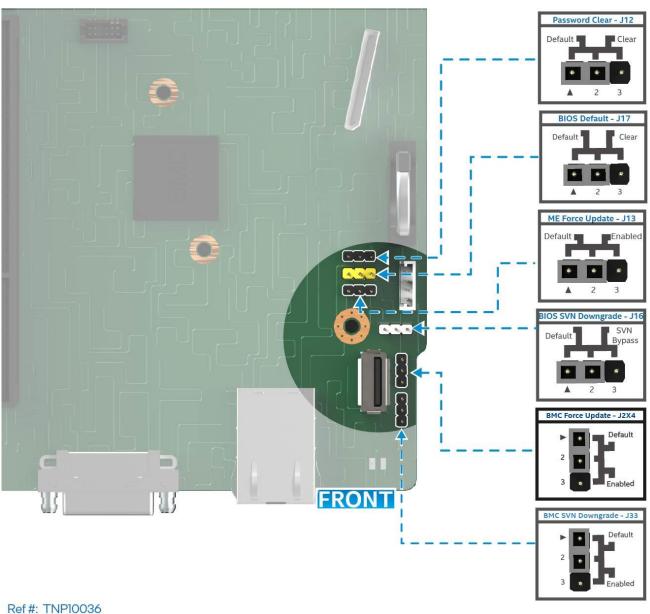


Figure 109. Reset and Recovery Jumper Block Location

15.1 BIOS Default Jumper (BIOS DFLT - J17)

This jumper resets BIOS options, configured using the BIOS Setup utility, back to their original default factory settings.

Note: This jumper does not reset administrator or user passwords. To reset passwords, the password clear jumper must be used.

To use the BIOS default jumper, perform the following steps:

- 1. Power down the server module.
- 2. Remove the module from the chassis
- 3. Remove the riser assemblies from the module. See the Intel® Server D50TNP Family Installation and Service Guide for instructions.
- 4. Move the "BIOS DFLT" (J17) jumper from pins 1-2 (normal operation) to pins 2-3 (set BIOS defaults).
- 5. Wait five seconds then move the "BIOS DFLT" (J17) jumper back to pins 1–2.
- 6. Reinstall the riser assemblies.
- 7. Reinstall module in the chassis.

Note: The system automatically powers on after AC is applied to the system.

8. Power on the module and press **<F2>** during POST to access the BIOS Setup utility to configure and save desired BIOS options.

After resetting BIOS options using the BIOS default jumper, the Error Manager Screen in the BIOS Setup utility displays two errors:

- 0012 System RTC date/time not set
- 5220 BIOS Settings reset to default settings

The system time and date will need to be reset.

15.2 Password Clear Jumper (PASSWD_CLR – J12)

This jumper causes both the user password and the administrator password to be cleared if they were set. The operator should be aware that this situation creates a security gap until passwords have been configured again through the BIOS Setup utility. This is the only method by which the administrator and user passwords can be cleared unconditionally. Other than this jumper, passwords can only be set or cleared by changing them explicitly in BIOS Setup. No method of resetting BIOS configuration settings to default values affects either the administrator or user passwords.

To use the password clear jumper, perform the following steps:

- 1. Power down the server module.
- 2. Remove the module from the chassis
- 3. Remove the riser assemblies from the module. See the Intel® Server D50TNP Family Installation and Service Guide for instructions.
- 4. Move the "PASSWD CLR" (J12) jumper from pins 1–2 (default) to pins 2–3 (password clear position).
- 5. Reinstall the riser assemblies
- 6. Reinstall the module in the chassis.
- 7. Power on the module and press <F2> during POST to access the BIOS Setup utility.

- 8. Verify the password clear operation was successful by viewing the Error Manager screen. Two errors should be logged:
 - o 5221 Passwords cleared by jumper
 - o 5224 Password clear jumper is set
- 9. Exit the BIOS Setup utility and power down the module.
- 10. Remove the module from the chassis and remove the riser assemblies from the module. See the Intel® Server D50TNP Family Installation and Service Guide for instructions.
- 11. Move the "PASSWD_CLR" (J12) jumper back to pins 1-2 (default).
- 12. Reinstall the riser assemblies
- 13. Reinstall the module in the chassis.
- 14. Power up the module.
- 15. It is strongly recommended to boot into BIOS Setup immediately, navigate to the Security tab, and set the administrator and user passwords if intending to use BIOS password protection.

15.3 Intel® Management Engine (Intel® ME) Firmware Force Update Jumper (ME FRC UPDT – J13)

When the Intel® ME firmware force update jumper is moved from its default position, the Intel® ME is forced to operate in a reduced minimal operating capacity. This jumper should only be used if the Intel® ME firmware has gotten corrupted and requires reinstallation.

Note: The Intel® ME firmware update files are included in the system update packages (SUP) posted to Intel's download center. See Section 1.2.

To use the Intel® ME firmware force update jumper, perform the following steps:

- 1. Power down the server module.
- 2. Remove the module from the chassis
- 3. Remove the riser assemblies from the module. See the Intel® Server D50TNP Family Installation and Service Guide for instructions.
- 4. Move the "ME FRC UPDT" (J13) jumper from pins 1–2 (default) to pins 2–3 (force update position).
- 5. Reinstall the riser assemblies
- 6. Reinstall the module in the chassis.
- 7. Power on the module.
- 8. Boot to the EFI shell.
- 9. Change directories to the folder containing the update files.
- 10. Update the Intel® ME firmware using the following command:

```
Sysfwupdt -u <version#> UpdateCapsule.bin
```

- 11. When the update has successfully completed, power off the module.
- 12. Remove the module from the chassis
- 13. Remove the riser assemblies from the module.
- 14. Move the "ME FRC UPDT" (J13) jumper back to pins 1-2 (default).
- 15. Reinstall the riser assemblies
- 16. Reinstall the module in the chassis.
- 17. Power on the module.

15.4 BMC Force Update Jumper (BMC FRC UPDT – J2X4)

The BMC force update jumper is used to put the BMC in boot recovery mode for a low-level update. It causes the BMC to abort its normal boot process and stay in the bootloader without executing any Linux* code. This jumper should only be used if the BMC firmware has become corrupted and requires reinstallation.

Note: The BMC firmware update files are included in the SUP posted to Intel's download center. See Section 1.2.

To use the BMC force update jumper, perform the following steps:

- 1. Power down the server module.
- 2. Remove the module from the chassis
- 3. Remove the riser assemblies from the module. See the Intel® Server D50TNP Family Installation and Service Guide for instructions.
- 4. Move the "BMC FRC UPDT" (J2X4) jumper from pins 1–2 (default) to pins 2–3 (force update position).
- 5. Reinstall the riser assemblies
- 6. Reinstall the module in the chassis.
- 7. Power on the module.
- 8. Boot to the EFI shell.
- 9. Change directories to the folder containing the update files.
- 10. Update the BMC firmware using the following command:

```
sysfwupdt.efi -u <filename.bin>
```

- 11. When the update has successfully completed, power down the module.
- 12. Remove the module from the chassis and remove the riser assemblies from the module.
- 13. Move the "BMC FRC UPDT" (J2X4) jumper back to pins 1–2 (default).
- 14. Reinstall the riser assemblies
- 15. Reinstall the module in the chassis.
- 16. Power on the module.
- 17. Boot to the EFI shell.
- 18. Change directories to the folder containing the update files.
- 19. Reinstall the board/system SDR data by running the FRUSDR utility.
- 20. After the SDRs have been loaded, reboot the module.

15.5 BIOS SVN Downgrade (SVN_Bypass - J16)

The BIOS SVN Downgrade Jumper is labeled SVN_BYPASS on the server board. When this jumper is moved from its default pin position (pins 1–2), it allows the module firmware (including BIOS) in the PFR-controlled PCH capsule file to be downgraded to a lower Security Version Number (SVN). This jumper is used when there is a need for the module to power on using a BIOS revision with lower SVN.

Caution: Downgrading to an older version of BIOS may result in the loss of functionality and security features that are present in a higher SVN.

Caution: When downgrading to an older version of BIOS, modules may end up with a firmware stack combination that is not supported, and therefore could experience unpredictable behavior.

Note: Latest system update packages are included in the SUP posted to Intel's download center. See Section 1.2.

To use the SVN Bypass jumper, perform the following steps:

- 1. Power down the server module.
- 2. Remove the module from the chassis
- 3. Remove the riser assemblies from the module. See the Intel® Server D50TNP Family Installation and Service Guide for instructions.
- 4. Move the "SVN_Bypass" (J16) jumper from pins 1-2 (default) to pins 2-3 (SVN Bypass).
- 5. Reinstall the riser assemblies.
- 6. Reinstall the module in the chassis.
- 7. Power on the module. The system automatically boots to the EFI shell.
- 8. Update the BIOS using the recovery BIOS update instructions provided with the system update package.
- 9. After the BIOS update has successfully completed, power down the module.
- 10. Remove the module from the chassis and remove the riser assemblies from the module.
- 11. Move the "SVN Bypass" (J16) jumper back to pins 1-2 (default).
- 12. Reinstall the module in the chassis.
- 13. Power on the module. During POST, press **<F2>** to access the BIOS Setup utility to configure and save desired BIOS options.

15.6 BMC SVN Downgrade (J33)

When this jumper is moved from its default pin position (pins 1–2), it allows the module BMC firmware in the PFR-controlled BMC capsule file to be downgraded to lower Security Version Number (SVN). This jumper is used when there is a need for the module to power on using BMC revision with lower SVN.

Caution: Downgrading to a BMC version with lower SVN may result in the loss of functionality and security features that are present in a higher SVN but were not implemented in the lower SVN.

Caution: When downgrading to an older version of BMC, modules may end up with a firmware stack combination that is not supported, and therefore could experience unpredictable behavior.

Note: Latest system update packages are included in the SUP posted to Intel's download center. See Section 1.2.

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To use the BMC SVN Downgrade jumper, perform the following steps:

- 1. Power down the server module.
- 2. Remove the module from the chassis
- 3. Remove the riser assemblies from the module. See the Intel® Server D50TNP Family Installation and Service Guide for instructions.
- 4. Using tweezers, move the BMC SVN Downgrade jumper (J33) from pins 1–2 (default) to pins 2–3 (Enabled).
- 5. Reinstall the riser assemblies.
- 6. Reinstall the module in the chassis.
- 7. Power on the module. The system automatically boots to the EFI shell.
- 8. Update the BMC using the recovery BMC update instructions provided with the system update package.
- 9. After the BMC update has successfully completed, power down the module.
- 10. Remove the module from the chassis and remove the riser assemblies from the module.
- 11. Using tweezers, move the BMC SVN Downgrade jumper (J33) jumper back to pins 1–2 (default).
- 12. Reinstall the riser assemblies
- 13. Reinstall the module in the chassis.
- 14. Power on the module.

Appendix A. Getting Help

Available Intel support options with your Intel Server System:

- 1. 24x7 support through Intel's support webpage at https://www.intel.com/content/www/us/en/support/products/1201/server-products.html
 - Information available at the support site includes:
 - Latest BIOS, firmware, drivers, and utilities
 - Product documentation, setup, and service guides
 - Full product specifications, technical advisories, and errata
 - Compatibility documentation for memory, hardware add-in cards, and operating systems
 - Server and chassis accessory parts list for ordering upgrades or spare parts
 - A searchable knowledge base to search for product information throughout the support site

Quick Links:

Use the following links for	Download Center	BIOS Support Page	Troubleshooting Boot Issue
support on Intel Server Boards and Server Systems			
	http://www.intel.com/support/d ownloadserversw	http://www.intel.com/support/serv erbios	http://www.intel.com/support/ts boot
Use the following links for support on Intel® Data Center Block (DCB)	Download Center	Technical Support Documents	Warranty and Support Information
* Intel DCB comes pre- populated with processors, memory, storage, and peripherals based on how it was ordered through the Intel Configure to Order tool.	http://www.intel.com/support/downloaddcbsw	http://www.intel.com/support/dcb	http://www.intel.com/support/d

- 2. If a solution cannot be found at Intel's support site, submit a service request via Intel's online service center at https://supporttickets.intel.com/servicecenter?lang=en-US. In addition, you can also view previous support requests. (Login required to access previous support requests)
- 3. Contact an Intel support representative using one of the support phone numbers available at https://www.intel.com/content/www/us/en/support/contact-support.html (charges may apply).

Intel also offers Partner Alliance Program members around-the-clock 24x7 technical phone support on Intel® server boards, server chassis, server RAID controller cards, and Intel® Server Management at https://www.intel.com/content/www/us/en/partner-alliance/overview.html

Note: The 24x7 support number is available after logging in to the Intel Partner Alliance website.

Warranty Information

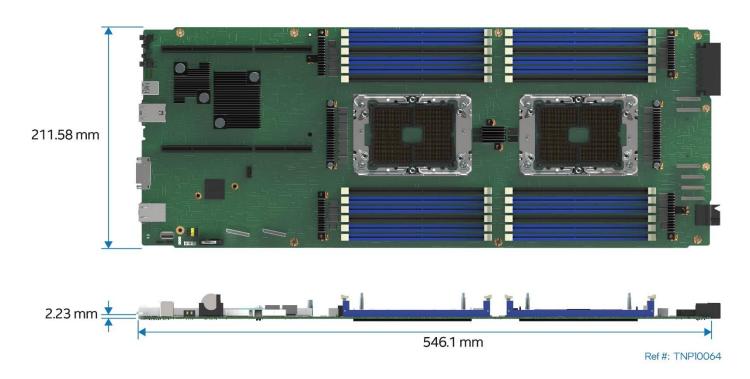
To obtain warranty information, visit http://www.intel.com/p/en_US/support/warranty.

Appendix B. Mechanical Dimension Diagrams

This appendix provides server board, module, and server system dimensions. Location of the chassis pull-out tab is also in this appendix.

B.1 Intel® Server Board D50TNP1SB / D50TNP1SBCR Mechanical Dimension Diagrams

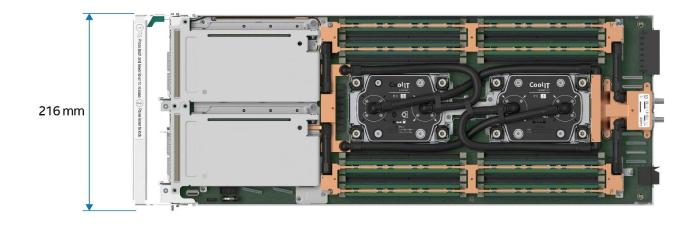
The following figure provides the server board dimensional data for the Intel® Server Board D50TNP1SB / D50TNP1SBCR.



Note: Intel® Server Board D50TNP1SB shown.

Figure 110. Intel® Server Board D50TNP1SB Dimensions

B.2 Intel® D50TNP Module Dimension Diagrams



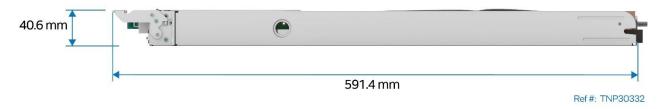


Figure 111. 1U Liquid-Cooled Compute Module Dimensions

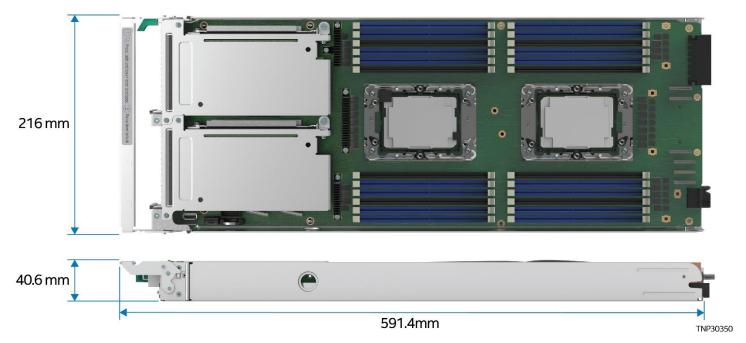
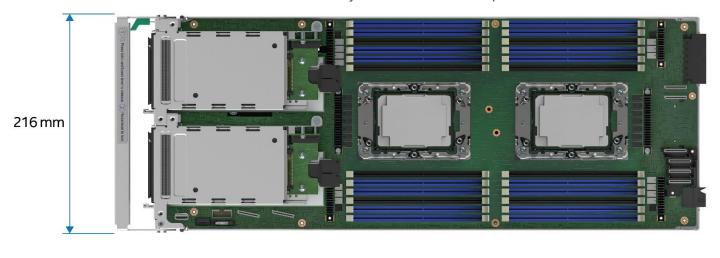


Figure 112. 1U Air-Cooled Compute Module Dimensions



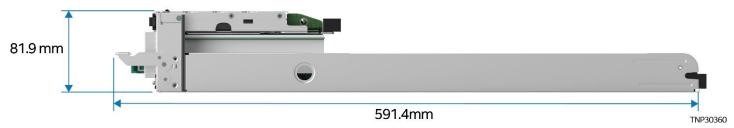


Figure 113. 2U Management Module Dimensions

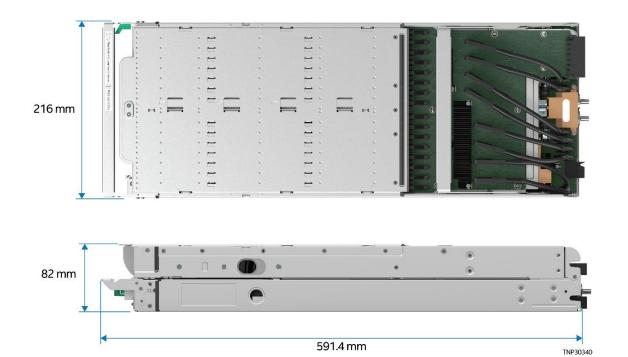


Figure 114. 2U Storage Module Dimensions

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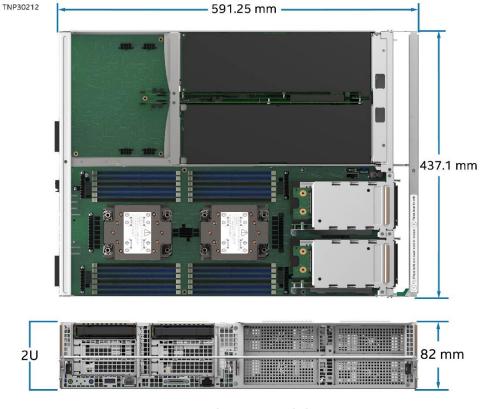


Figure 115. 2U Accelerator Module Dimensions

B.3 System Chassis Dimension Diagrams

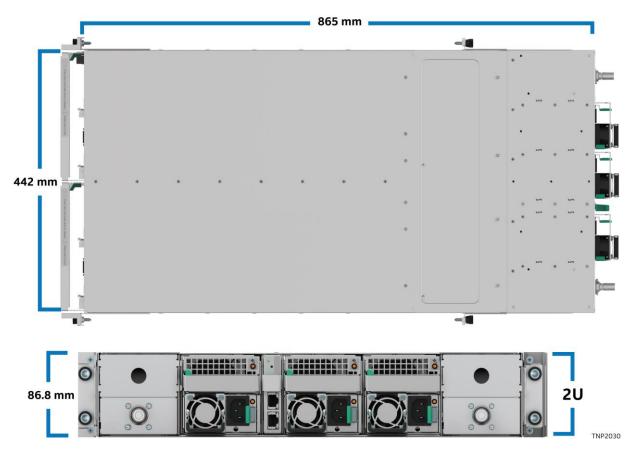


Figure 116. System chassis Dimensions

B.4 Pull-Out Tab

The chassis includes a pull-out tab that can be used for asset tracking and identification. Figure 117 identifies the location of the pull-out tab and Figure 118 shows its dimensions.

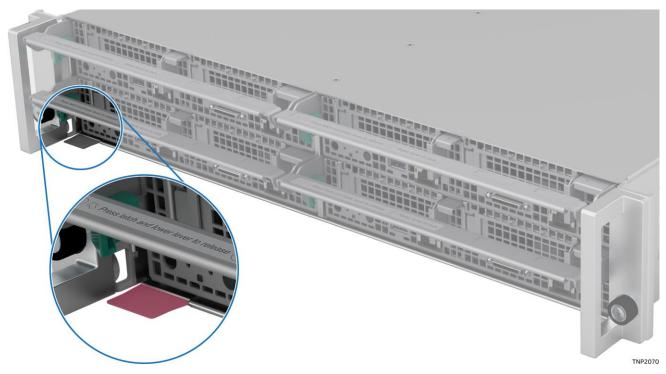


Figure 117. Pull-out Tab Location

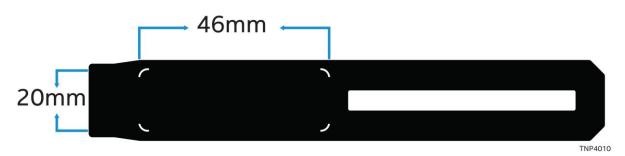


Figure 118. Pull-out Tab Dimensions

Appendix C. Post Code Diagnostic LED Decoder

As an aid in troubleshooting a system hang that occurs during a system POST process, the server board includes a bank of eight POST code diagnostic LEDs on the front edge of the server board.

During the system boot process, Memory Reference Code (MRC) and system BIOS execute several memory initialization and platform configuration routines, each of which is assigned a hexadecimal POST code number.

As each routine is started, the given POST code number is displayed to the POST code diagnostic LEDs on the front edge of the server board.

During a POST system hang, the displayed POST code can be used to identify the last POST routine that was run before the error occurred, helping to isolate the possible cause of the hang condition.

Each POST code is represented by eight LEDs, four green LEDs, and four amber LEDs. The POST codes are divided into two nibbles, an upper nibble, and a lower nibble. The upper nibble bits are represented by amber diagnostic LEDs and the lower nibble bits are represented by green diagnostics. If the bit is set, the corresponding LED is lit. If the bit is clear, the corresponding LED is off. For each set of nibble bits, LED 0 represents the least significant bit (LSB) and LED 3 represents the most significant bit (MSB).

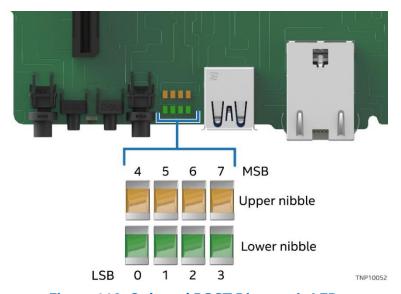


Figure 119. Onboard POST Diagnostic LEDs

In the following example, the BIOS sends a value of AC to the diagnostic LED decoder. The LEDs are decoded as shown in the following table.

	Upper Nibble AMBER LEDs			Lower Nibble GREEN LEDs					
LEDs		MSB							LSB
		LED #7	LED #6	LED #5	LED #4	LED #3	LED #2	LED #1	LED #0
		8h	4h	2h	1h	8h	4h	2h	1h
Status		ON	OFF	ON	OFF	ON	ON	OFF	OFF
Read	Binary	1	0	1	0	1	1	0	0
Value	Hexadecimal		A h				C h		
	Result	lt ACh							

Table 45. POST Progress Code LED Example

Upper nibble bits = 1010b = Ah; Lower nibble bits = 1100b = Ch; the two Hex Nibble values are combined to create a single **AC**h POST Progress Code.

C.1 Early POST Memory Initialization MRC Diagnostic Codes

Memory initialization at the beginning of POST includes multiple functions: discovery, channel training, validation that the DIMM population is acceptable and functional, initialization of the IMC and other hardware settings, and initialization of applicable RAS configurations.

The MRC progress codes are displayed to the diagnostic LEDs that show the execution point in the MRC operational path at each step.

Table 46. Memory Reference Code (MRC) Progress Codes

Post Code		Upper	Nibble	:		Lower	Nibble		
(Hex)	8h	4h	2h	1h	8h	4h	2h	1h	Description
ВО	1	0	1	1	0	0	0	0	Detect DIMM population
B1	1	0	1	1	0	0	0	1	Set DDR4 frequency
B2	1	0	1	1	0	0	1	0	Gather remaining SPD data
В3	1	0	1	1	0	0	1	1	Program registers on the memory controller level
B4	1	0	1	1	0	1	0	0	Evaluate RAS modes and save rank information
B5	1	0	1	1	0	1	0	1	Program registers on the channel level
В6	1	0	1	1	0	1	1	0	Perform the JEDEC defined initialization sequence
В7	1	0	1	1	0	1	1	1	Train DDR4 ranks
1	0	0	0	0	0	0	0	1	Train DDR4 ranks
2	0	0	0	0	0	0	1	0	Train DDR4 ranks – Read DQ/DQS training
3	0	0	0	0	0	0	1	1	Train DDR4 ranks – Receive enable training
4	0	0	0	0	0	1	0	0	Train DDR4 ranks – Write DQ/DQS training
5	0	0	0	0	0	1	0	1	Train DDR4 ranks – DDR channel training done
В8	1	0	1	1	1	0	0	0	Initialize CLTT/OLTT
В9	1	0	1	1	1	0	0	1	Hardware memory test and initialization
ВА	1	0	1	1	1	0	1	0	Execute software memory initialization
ВВ	1	0	1	1	1	0	1	1	Program memory map and interleaving
ВС	1	0	1	1	1	1	0	0	Program RAS configuration
BE	1	0	1	1	1	1	1	0	Execute BSSA RMT
BF	1	0	1	1	1	1	1	1	MRC is done

If a major memory initialization error occurs, preventing the system from booting with data integrity, the MRC displays a fatal error code on the diagnostic LEDs, and a system halt command is executed. Fatal MRC error halts do not change the state of the system status LED and they do not get logged as SEL events. Table 47 lists all MRC fatal errors that are displayed to the diagnostic LEDs.

Note: Fatal MRC errors display POST error codes that may be the same as BIOS POST progress codes displayed later in the POST process.

Table 47. Memory Reference Code (MRC) Fatal Error Codes

Post Code	U	lpper	Nibbl	.e	L	ower	Nibbl	.e	Description
(Hex)	8h	4h	2h	1h	8h	4h	2h	1h	Description
E8	1	1	1	0	1	0	0	0	No usable memory error 01h = No memory was detected from SPD read, or invalid config that causes no operable memory. 02h = Memory DIMMs on all channels of all sockets are disabled due to hardware memory test error. 03h = No memory installed. All channels are disabled.
E9	1	1	1	0	1	0	0	1	Memory is locked by Intel® TXT and is inaccessible
EA	1	1	1	0	1	0	1	0	DDR4 channel training error 01h = Error on read DQ/DQS (Data/Data Strobe) initialization 02h = Error on Receive Enable 03h = Error on Write Leveling 04h = Error on write DQ/DQS (Data/Data Strobe
ЕВ	1	1	1	0	1	0	1	1	Memory test failure 01h = Software memory test failure. 02h = Hardware memory test failed.
ED	1	1	1	0	1	1	0	1	DIMM configuration population error 01h = Different DIMM types (RDIMM, LRDIMM) are detected installed in the system. 02h = Violation of DIMM population rules. 03h = The 3rd DIMM slot cannot be populated when QR DIMMs are installed. 04h = UDIMMs are not supported. 05h = Unsupported DIMM Voltage.
EF	1	1	1	0	1	1	1	1	Indicates a CLTT table structure error

C.2 BIOS POST Progress Codes

The following table provides a list of all POST progress codes.

Table 48. POST Progress Codes

Post	L	Jpper l	Nibble	•		Lower	Nibble	e	
Code	8h	4h	2h	1h	8h	4h	2h	1h	Description
(Hex) Security			211	III	011	411	211	In	
01	0	0	0	0	0	0	0	1	First POST code after CPU reset
02	0	0	0	0	0	0	1	0	Microcode load begin
03	0	0	0	0	0	0	1	1	CRAM initialization begin
04	0	0	0	0	0	1	0	0	PEI cache when disabled
05	0	0	0	0	0	1	0	1	SEC core at power on begin.
06	0	0	0	0	0	1	1	0	Early CPU initialization during SEC phase.
Intel® UP	I RC (Fu	ılly lev	erage	witho	ut pla	tform	change	e)	
A1	1	0	1	0	0	0	0	1	Collect information such as SBSP, boot mode, reset type, etc.
А3	1	0	1	0	0	0	1	1	Setup minimum path between SBSP and other sockets
A6	1	0	1	0	0	1	1	0	Sync up with PBSPs
A 7	1	0	1	0	0	1	1	1	Topology discovery and route calculation
A8	1	0	1	0	1	0	0	0	Program final route
A9	1	0	1	0	1	0	0	1	Program final IO SAD setting
AA	1	0	1	0	1	0	1	0	Protocol layer and other uncore settings
AB	1	0	1	0	1	0	1	1	Transition links to full speed operation
AE	1	0	1	0	1	1	1	0	Coherency settings
AF	1	0	1	0	1	1	1	1	KTI initialization done
Pre-EFI I	nitializa	ation (F	PEI) PI	nase	•				
10	0	0	0	1	0	0	0	0	PEI Core
11	0	0	0	1	0	0	0	1	CPU PEIM
15	0	0	0	1	0	1	0	1	Platform type initialization
19	0	0	0	1	1	0	0	1	Platform PEIM initialization
Integrate		-			1		1		
EO	1	1	1	0	0	0	0	0	IIO early initialization entry
E1	1	1	1	0	0	0	0	1	IIO Pre-link training
E2	1	1	1	0	0		1	0	IIO EQ programming
E3	1	1	1	0	0	0	1	1	IIO Link training
E4	1	1	1	0	0	1	0	0	Internal use
E5	1	1	1	0	0	1	0	1	IIO early initialization exit
E6	1	1	1	0	0	1	1	0	IIO late initialization entry
E7	1	1	1	0	0	1	1	1	IIO PCIe ports initialization
E8	1	1	1	0	1	0	0	0	IIO IOAPIC initialization
E9	1	1	1	0	1	0	0	1	IIO VTD initialization
EA	1	1	1	0	1	0	1	0	IIO IOAT initialization
EB EC	1	1	1	0	1	0	0	0	IIO DXF initialization IIO NTB initialization
ED	1	1	1	0	1	1	0	1	IIO Security initialization
EE	1	1	1	0	1	1	1	0	IIO late initialization exit
EF	1	1	1	0	1	1	1	1	IIO ready to boot
EF	l l			U	'				110 ready to boot

Post	ι	Jpper N	libble	!	l	Lower	Nibbl	e	
Code	8h	4h	2h	1h	8h	4h	2h	1h	Description
(Hex)									sequence is executed.
31	0	0	1	3 point	O	0	0	1	Memory installed
32	0	0	1	1	0	0	1	0	CPU PEIM (CPU initialization)
33	0	0	1	1	0	0	1	1	CPU PEIM (Cache initialization)
34	0	0	1	1	0	1	0	0	CPU BSP select
35	0	0	1	1	0	1	0	1	CPU AP initialization
36	0	0	1	1	0	1	1	0	CPU SMM initialization
4F	0	1	0	0	1	1	1	1	DXE IPL started
Memory	Feature	Progr	ess Co	odes					
C 1	1	1	0	0	0	0	0	1	Memory POR check
C2	1	1	0	0	0	0	1	0	Internal use
С3	1	1	0	0	0	0	1	1	Internal use
C4	1	1	0	0	0	1	0	0	Internal use
C 5	1	1	0	0	0	1	0	1	Memory early initialization
C6	1	1	0	0	0	1	1	0	Display DIMM information in debug mode
C 7	1	1	0	0	0	1	1	1	JEDEC NVDIMM training
C9	1	1	0	0	1	0	0	1	Setup SVL and scrambling
CA	1	1	0	0	1	0	1	0	Internal use
СВ	1	1	0	0	1	0	1	1	Check RAS support
СС	1	1	0	0	1	1	0	0	PMem ADR initialization
CD	1	1	0	0	1	1	0	1	Internal use
CE	1	1	0	0	1	1	1	0	Memory late initialization
CF	1	1	0	0	1	1	1	1	Determine MRC boot mode
D0	1	1	0	1	0	0	0	0	MKTME early initialization
D1	1	1	0	1	0	0	0	1	SGX early initialization
D2	1	1	0	1	0	0	1	0	Memory margin test
D3	1	1	0	1	0	0	1	1	Internal use
D5	1	1	0	1	0	1	0	1	Internal use
D6	1	1	0	1	0	1	1	0	Offset training result
Driver Ex								_	575
60	0	1	1	0	0	0	0	0	DXE core started
62	0	1	1	0	0	0	1	0	DXE setup initialization
68	0	1	1	0	1	0	0	0	DXE PCI host bridge initialization
69	0	1	1	0	1	0	0	1	DXE NB shitialization
6A 70	0	1	1	0	0	0	0	0	DXE NB SMM initialization DXE SB initialization
70	0	1	1	1	0	0	0	1	DXE SB SMM initialization
71	0	1	1	1	0	0	1	0	DXE SB devices initialization
78	0	1	1	1	1	0	0	0	DXE ACPI initialization
79	0	1	1	1	1	0	0	1	DXE CSM initialization
75 7D	0	1	1	1	1	1	0	1	DXE removable media detect
7E	0	1	1	1	1	1	1	0	DXE removable media detect
90	1	0	0	1	0	0	0	0	DXE BDS started
91	1	0	0	1	0	0	0	1	DXE BDS connect drivers
92	1	0	0	1	0	0	1	0	DXE PCI bus begin
									57.2 F 61 503 506111

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Post	ι	Jpper N	libble		l	Lower	Nibbl	e	
Code (Hex)	8h	4h	2h	1h	8h	4h	2h	1h	Description
93	1	0	0	1	0	0	1	1	DXE PCI bus HPC initialization
94	1	0	0	1	0	1	0	0	DXE PCI bus enumeration
95	1	0	0	1	0	1	0	1	DXE PCI bus resource requested
96	1	0	0	1	0	1	1	0	DXE PCI bus assign resource
97	1	0	0	1	0	1	1	1	DXE CON_OUT connect
98	1	0	0	1	1	0	0	0	DXE CON_IN connect
99	1	0	0	1	1	0	0	1	DXE SIO initialization
9A	1	0	0	1	1	0	1	0	DXE USB start
9B	1	0	0	1	1	0	1	1	DXE USB reset
9C	1	0	0	1	1	1	0	0	DXE USB detect
9D	1	0	0	1	1	1	0	1	DXE USB enable
A1	1	0	1	0	0	0	0	1	DXE IDE begin
A2	1	0	1	0	0	0	1	0	DXE IDE reset
А3	1	0	1	0	0	0	1	1	DXE IDE detect
A4	1	0	1	0	0	1	0	0	DXE IDE enable
A5	1	0	1	0	0	1	0	1	DXE SCSI begin
A6	1	0	1	0	0	1	1	0	DXE SCSI reset
A7	1	0	1	0	0	1	1	1	DXE SCSI detect
A8	1	0	1	0	1	0	0	0	DXE SCSI enable
AB	1	0	1	0	1	0	1	1	DXE SETUP start
AC	1	0	1	0	1	1	0	0	DXE SETUP input wait
AD	1	0	1	0	1	1	0	1	DXE ready to boot
AE	1	0	1	0	1	1	1	0	DXE legacy boot
AF	1	0	1	0	1	1	1	1	DXE exit boot services
ВО	1	0	1	1	0	0	0	0	RT set virtual address map begin
B1	1	0	1	1	0	0	0	1	RT set virtual address map end
B2	1	0	1	1	0	0	1	0	DXE legacy option ROM initialization
B3	1	0	1	1	0	0	1	1	DXE reset system
B4	1	0	1	1	0	1	0	0	DXE USB hot plug
B5	1	0	1	1	0	1	0	1	DXE PCI BUS hot plug
B8	1	0	1	1	1	0	0	0	PWRBTN shutdown
B9	1	0	1	1	1	0	0	1	SLEEP shutdown
C0	1	1	0	0	0	0	0	0	End of DXE
C7	1	1	0	0	0	1	1	1	DXE ACPI enable
0 S3 Resur	0	0	0	0	0	0	0	0	Clear POST code
E0	ne 1	1	1	0	0	0	0	0	S3 resume PEIM (S3 started)
E1	1	1	1	0	0	0	0	1	S3 resume PEIM (S3 started) S3 resume PEIM (S3 boot script)
E2	1	1	1	0	0	0	1	0	S3 resume PEIM (S3 video repost)
E3	1	1	1	0	0	0	1	1	S3 resume PEIM (S3 OS wake)
	'								33 resume i Elin (33 03 wane)

Appendix D. Post Code Errors

Most error conditions encountered during POST are reported using POST error codes. These codes represent specific failures, warnings, or information. POST error codes may be displayed in the error manager display screen and are always logged to the System Event Log (SEL). Logged events are available to system management applications, including remote and Out of Band (OOB) management.

Exception cases exist in early initialization where system resources are not adequately initialized for handling POST Error Code reporting. These cases are primarily fatal error conditions resulting from initialization of processors and memory, and they are handed by a diagnostic LED display with a system halt.

Table 49 lists the supported POST error codes. Each error code is assigned an error type that determines the action the BIOS takes when the error is encountered. Error types include minor, major, and fatal. The BIOS action for each is defined as follows:

- Minor: An error message may be displayed to the screen or to the BIOS Setup error manager and the
 POST error code is logged to the SEL. The system continues booting in a degraded state. The user
 may want to replace the erroneous unit. The "POST Error Pause" option setting in the BIOS Setup
 does not have any effect on this error.
- Major: An error message is displayed to the error manager screen and an error is logged to the SEL. If
 the BIOS Setup option "Post Error Pause" is enabled, operator intervention is required to continue
 booting the system. If the BIOS Setup option "POST Error Pause" is disabled, the system continues to
 boot.

Note: For 0048 "Password check failed", the system halts and then, after the next reset/reboot, displays the error code on the error manager screen.

• Fatal: If the system cannot boot, POST halts and displays the following message:

Unrecoverable fatal error found. System will not boot until the error is resolved.

Press <F2> to enter setup.

When the **<F2>** key on the keyboard is pressed, the error message is displayed on the error manager screen and an error is logged to the system event log (SEL) with the POST error code. The system cannot boot unless the error is resolved. The faulty component must be replaced. The "POST Error Pause" option setting in the BIOS Setup does not have any effect on this error.

Note: The POST error codes in the following table are common to all current generation Intel® server platforms. Features present on a given server board/system determine which of the listed error codes are supported.

Table 49. POST Error Messages and Handling

Error Code	Error Message	Action Message	Туре
0012	System RTC date/time not set		Major
0048	Password check failed	Put right password.	Major
0140	PCI component encountered a PERR error		Major
0141	PCI resource conflict		Major
0146	PCI out of resources error	Enable Memory Mapped I/O above 4 GB item at SETUP to use 64-bit MMIO.	Major
0191	Processor core/thread count mismatch detected	Use identical CPU type.	Fatal
0192	Processor cache size mismatch detected	Use identical CPU type.	Fatal
0194	Processor family mismatch detected	Use identical CPU type.	Fatal
0195	Processor Intel® UPI link frequencies unable to synchronize		Fatal
0196	Processor model mismatch detected	Use identical CPU type.	Fatal
0197	Processor frequencies unable to synchronize	Use identical CPU type.	Fatal
5220	BIOS Settings reset to default settings		Major
5221	Passwords cleared by jumper		Major
5224	Password clear jumper is Set	Recommend reminding user to install BIOS password as BIOS admin password is the master keys for several BIOS security features.	Major
8130	CPU 0 disabled		Major
8131	CPU 1 disabled		Major
8160	CPU 0 unable to apply microcode update		Major
8161	CPU 1 unable to apply microcode update		Major
8170	CPU 0 failed Self-Test (BIST)		Major
8171	CPU 1 failed Self-Test (BIST)		Major
8180	CPU 0 microcode update not found		Minor
8181	CPU 1 microcode update not found		Minor
8190	Watchdog timer failed on last boot.		Major
8198	OS boot watchdog timer failure.		Major
8300	Baseboard Management Controller failed self-test.		Major
8305	Hot Swap Controller failure		Major
83A0	Management Engine (ME) failed self-test.		Major
83A1	Management Engine (ME) Failed to respond.		Major
84F2	Baseboard management controller failed to respond		Major
84F3	Baseboard Management Controller in Update Mode.		Major
84F4	Baseboard Management Controller Sensor Data Record empty.	Update right SDR.	Major
84FF	System Event Log full	Clear SEL through EWS or SELVIEW utility.	Minor
85FC	Memory component could not be configured in the selected RAS mode		Major
8501	Memory Population Error	Plug DIMM at right population.	Major
8502	PMem invalid DIMM population found on the system.	Populate valid POR PMem DIMM population.	Major
8520	Memory failed test/initialization CPU0_DIMM_A1	Remove the disabled DIMM.	Major
8521	Memory failed test/initialization CPU0_DIMM_A2	Remove the disabled DIMM.	Major
8522	Memory failed test/initialization CPU0_DIMM_A3	Remove the disabled DIMM.	Major

Error Code	Error Message	Action Message	Туре
8523	Memory failed test/initialization CPU0_DIMM_B1	Remove the disabled DIMM.	Major
8524	Memory failed test/initialization CPU0_DIMM_B2	Remove the disabled DIMM.	Major
8525	Memory failed test/initialization CPU0_DIMM_B3	Remove the disabled DIMM.	Major
8526	Memory failed test/initialization CPU0_DIMM_C1	Remove the disabled DIMM.	Major
8527	Memory failed test/initialization CPU0_DIMM_C2	Remove the disabled DIMM.	Major
8528	Memory failed test/initialization CPU0_DIMM_C3	Remove the disabled DIMM.	Major
8529	Memory failed test/initialization CPU0_DIMM_D1	Remove the disabled DIMM.	Major
852A	Memory failed test/initialization CPU0_DIMM_D2	Remove the disabled DIMM.	Major
852B	Memory failed test/initialization CPU0_DIMM_D3	Remove the disabled DIMM.	Major
852C	Memory failed test/initialization CPU0_DIMM_E1	Remove the disabled DIMM.	Major
852D	Memory failed test/initialization CPU0_DIMM_E2	Remove the disabled DIMM.	Major
852E	Memory failed test/initialization CPU0_DIMM_E3	Remove the disabled DIMM.	Major
852F	Memory failed test/initialization CPU0_DIMM_F1	Remove the disabled DIMM.	Major
8530	Memory failed test/initialization CPU0_DIMM_F2	Remove the disabled DIMM.	Major
8531	Memory failed test/initialization CPU0_DIMM_F3	Remove the disabled DIMM.	Major
8532	Memory failed test/initialization CPU0_DIMM_G1	Remove the disabled DIMM.	Major
8533	Memory failed test/initialization CPU0_DIMM_G2	Remove the disabled DIMM.	Major
8534	Memory failed test/initialization CPU0_DIMM_G3	Remove the disabled DIMM.	Major
8535	Memory failed test/initialization CPU0_DIMM_H1	Remove the disabled DIMM.	Major
8536	Memory failed test/initialization CPU0_DIMM_H2	Remove the disabled DIMM.	Major
8537	Memory failed test/initialization CPU0_DIMM_H3	Remove the disabled DIMM.	Major
8538	Memory failed test/initialization CPU1_DIMM_A1	Remove the disabled DIMM.	Major
8539	Memory failed test/initialization CPU1_DIMM_A2	Remove the disabled DIMM.	Major
853A	Memory failed test/initialization CPU1_DIMM_A3	Remove the disabled DIMM.	Major
853B	Memory failed test/initialization CPU1_DIMM_B1	Remove the disabled DIMM.	Major
853C	Memory failed test/initialization CPU1_DIMM_B2	Remove the disabled DIMM.	Major
853D	Memory failed test/initialization CPU1_DIMM_B3	Remove the disabled DIMM.	Major
853E	Memory failed test/initialization CPU1_DIMM_C1	Remove the disabled DIMM.	Major
853F (Go to 85C0)	Memory failed test/initialization CPU1_DIMM_C2	Remove the disabled DIMM.	Major
8540	Memory disabled.CPU0_DIMM_A1	Remove the disabled DIMM.	Major
8541	Memory disabled.CPU0_DIMM_A2	Remove the disabled DIMM.	Major
8542	Memory disabled.CPU0_DIMM_A3	Remove the disabled DIMM.	Major
8543	Memory disabled.CPU0_DIMM_B1	Remove the disabled DIMM.	Major
8544	Memory disabled.CPU0_DIMM_B2	Remove the disabled DIMM.	Major
8545	Memory disabled.CPU0_DIMM_B3	Remove the disabled DIMM.	Major
8546	Memory disabled.CPU0_DIMM_C1	Remove the disabled DIMM.	Major
8547	Memory disabled.CPU0_DIMM_C2	Remove the disabled DIMM.	Major
8548	Memory disabled.CPU0_DIMM_C3	Remove the disabled DIMM.	Major
8549	Memory disabled.CPU0_DIMM_D1	Remove the disabled DIMM.	Major
854A	Memory disabled.CPU0_DIMM_D2	Remove the disabled DIMM.	Major
854B	Memory disabled.CPU0_DIMM_D3	Remove the disabled DIMM.	Major
854C	Memory disabled.CPU0_DIMM_E1	Remove the disabled DIMM.	Major
854D	Memory disabled.CPU0_DIMM_E2	Remove the disabled DIMM.	Major
854E	Memory disabled.CPU0_DIMM_E3	Remove the disabled DIMM.	Major
854F	Memory disabled.CPU0_DIMM_F1	Remove the disabled DIMM.	Major

Error Code	Error Message	Action Message	Туре
8550	Memory disabled.CPU0_DIMM_F2	Remove the disabled DIMM.	Major
8551	Memory disabled.CPU0_DIMM_F3	Remove the disabled DIMM.	Major
8552	Memory disabled.CPU0_DIMM_G1	Remove the disabled DIMM.	Major
8553	Memory disabled.CPU0_DIMM_G2	Remove the disabled DIMM.	Major
8554	Memory disabled.CPU0_DIMM_G3	Remove the disabled DIMM.	Major
8555	Memory disabled.CPU0_DIMM_H1	Remove the disabled DIMM.	Major
8556	Memory disabled.CPU0_DIMM_H2	Remove the disabled DIMM.	Major
8557	Memory disabled.CPU0_DIMM_H3	Remove the disabled DIMM.	Major
8558	Memory disabled.CPU1_DIMM_A1	Remove the disabled DIMM.	Major
8559	Memory disabled.CPU1_DIMM_A2	Remove the disabled DIMM.	Major
855A	Memory disabled.CPU1_DIMM_A3	Remove the disabled DIMM.	Major
855B	Memory disabled.CPU1_DIMM_B1	Remove the disabled DIMM.	Major
855C	Memory disabled.CPU1_DIMM_B2	Remove the disabled DIMM.	Major
855D	Memory disabled.CPU1_DIMM_B3	Remove the disabled DIMM.	Major
855E	Memory disabled.CPU1_DIMM_C1	Remove the disabled DIMM.	Major
855F (Go to 85D0)	Memory disabled.CPU1_DIMM_C2	Remove the disabled DIMM.	Major
8560	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_A1		Major
8561	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_A2		Major
8562	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_A3		Major
8563	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_B1		Major
8564	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_B2		Major
8565	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_B3		Major
8566	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_C1		Major
8567	Memory encountered a Serial Presence Detection (SPD) failure.CPU0_DIMM_C2		Major
8568	Memory encountered a Serial Presence Detection (SPD) failure.CPU0_DIMM_C3		Major
8569	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_D1		Major
856A	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_D2		Major
856B	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_D3		Major
856C	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_E1		Major
856D	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_E2		Major
856E	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_E3		Major
856F	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_F1		Major

Error Code	Error Message	Action Message	Туре
8570	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_F2		Major
8571	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_F3		Major
8572	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_G1		Major
8573	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_G2		Major
8574	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_G3		Major
8575	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_H1		Major
8576	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_H2		Major
8577	Memory encountered a Serial Presence Detection(SPD) failure.CPU0_DIMM_H3		Major
8578	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_A1		Major
8579	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_A2		Major
857A	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_A3		Major
857B	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_B1		Major
857C	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_B2		Major
857D	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_B3		Major
857E	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_C1		Major
857F (Go to 85E0)	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_C2		Major
85C0	Memory failed test/initialization CPU1_DIMM_C3	Remove the disabled DIMM.	Major
85C1	Memory failed test/initialization CPU1_DIMM_D1	Remove the disabled DIMM.	Major
85C2	Memory failed test/initialization CPU1_DIMM_D2	Remove the disabled DIMM.	Major
85C3	Memory failed test/initialization CPU1_DIMM_D3	Remove the disabled DIMM.	Major
85C4	Memory failed test/initialization CPU1_DIMM_E1	Remove the disabled DIMM.	Major
85C5	Memory failed test/initialization CPU1_DIMM_E2	Remove the disabled DIMM.	Major
85C6	Memory failed test/initialization CPU1_DIMM_E3	Remove the disabled DIMM.	Major
85C7	Memory failed test/initialization CPU1_DIMM_F1	Remove the disabled DIMM.	Major
85C8	Memory failed test/initialization CPU1_DIMM_F2	Remove the disabled DIMM.	Major
85C9	Memory failed test/initialization CPU1_DIMM_F3	Remove the disabled DIMM.	Major
85CA	Memory failed test/initialization CPU1_DIMM_G1	Remove the disabled DIMM.	Major
85CB	Memory failed test/initialization CPU1_DIMM_G2	Remove the disabled DIMM.	Major
85CC	Memory failed test/initialization CPU1_DIMM_G3	Remove the disabled DIMM.	Major
85CD	Memory failed test/initialization CPU1_DIMM_H1	Remove the disabled DIMM.	Major
85CE	Memory failed test/initialization CPU1_DIMM_H2	Remove the disabled DIMM.	Major
85CF	Memory failed test/initialization CPU1_DIMM_H3	Remove the disabled DIMM.	Major
85D0	Memory disabled.CPU1_DIMM_C3	Remove the disabled DIMM.	Major
85D1	Memory disabled.CPU1_DIMM_D1	Remove the disabled DIMM.	Major

Error Code	Error Message	Action Message	Туре
85D2	Memory disabled.CPU1_DIMM_D2	Remove the disabled DIMM.	Major
85D3	Memory disabled.CPU1_DIMM_D3	Remove the disabled DIMM.	Major
85D4	Memory disabled.CPU1_DIMM_E1	Remove the disabled DIMM.	Major
85D5	Memory disabled.CPU1_DIMM_E2	Remove the disabled DIMM.	Major
85D6	Memory disabled.CPU1_DIMM_E3	Remove the disabled DIMM.	Major
85D7	Memory disabled.CPU1_DIMM_F1	Remove the disabled DIMM.	Major
85D8	Memory disabled.CPU1_DIMM_F2	Remove the disabled DIMM.	Major
85D9	Memory disabled.CPU1_DIMM_F3	Remove the disabled DIMM.	Major
85DA	Memory disabled.CPU1_DIMM_G1	Remove the disabled DIMM.	Major
85DB	Memory disabled.CPU1_DIMM_G2	Remove the disabled DIMM.	Major
85DC	Memory disabled.CPU1_DIMM_G3	Remove the disabled DIMM.	Major
85DD	Memory disabled.CPU1_DIMM_H1	Remove the disabled DIMM.	Major
85DE	Memory disabled.CPU1_DIMM_H2	Remove the disabled DIMM.	Major
85DF	Memory disabled.CPU1_DIMM_H3	Remove the disabled DIMM.	Major
85E0	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_C3		Major
85E1	Memory encountered a Serial Presence Detection (SPD) failure. CPU1_DIMM_D1		Major
85E2	Memory encountered a Serial Presence Detection (SPD) failure.CPU1_DIMM_D2		Major
85E3	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_D3		Major
85E4	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_E1		Major
85E5	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_E2		Major
85E6	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_E3		Major
85E7	Memory encountered a Serial Presence Detection (SPD) failure.CPU1_DIMM_F1		Major
85E8	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_F2		Major
85E9	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_F3		Major
85EA	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_G1		Major
85EB	Memory encountered a Serial Presence Detection (SPD) failure. CPU1_DIMM_G2		Major
85EC	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_G3		Major
85ED	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_H1		Major
85EE	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_H2		Major
85EF	Memory encountered a Serial Presence Detection(SPD) failure.CPU1_DIMM_H3		Major
8604	POST Reclaim of non-critical NVRAM variables		Minor
8605	BIOS Settings are corrupted		Major
8606	NVRAM variable space was corrupted and has been reinitialized		Major

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Error Code	Error Message	Action Message	Туре
8607	Recovery boot has been initiated. Note: The Primary BIOS image may be corrupted or the system may hang during POST. A BIOS update is required.		Fatal
A100	BIOS ACM Error		Major
A421	PCI component encountered a SERR error		Fatal
A5A0	PCI Express component encountered a PERR error		Minor
A5A1	PCI Express component encountered an SERR error		Fatal
A6A0	DXE Boot Services driver: Not enough memory available to shadow a Legacy Option ROM.	Disable OpRom at SETUP to save runtime memory.	Minor

D.1 Processor Initialization Error Summary

The following table describes mixed processor conditions and actions for all Intel® server boards and Intel® server systems designed with the Intel® Xeon® Scalable processor family architecture. The errors fall into one of the following categories:

• Fatal: If the system cannot boot, POST halts and displays the following message:

```
Unrecoverable fatal error found. System will not boot until the error is resolved Press <F2> to enter setup
```

When the <F2> key on the keyboard is pressed, the BIOS Setup Error Message is displayed on the BIOS Setup Error Manager screen. An error is logged to the system event log (SEL) with the POST error code.

The "POST Error Pause" option setting in the BIOS Setup does not affect this error.

The system status LED is set to a steady amber color for all fatal errors that are detected during processor initialization. A steady amber system status LED indicates that an unrecoverable system failure condition has occurred.

- Major: An error message is displayed to the BIOS Setup Error Message screen and an error is logged to
 the SEL. If the BIOS Setup option "Post Error Pause" is enabled, operator intervention is required to
 continue booting the system. If the BIOS Setup option "POST Error Pause" is disabled, the system
 continues to boot.
- Minor: An error message may be displayed to the screen or to the BIOS Setup Error Manager and the
 POST error code is logged to the SEL. The system continues booting in a degraded state. The user
 may want to replace the erroneous unit. The "POST Error Pause" option setting in the BIOS Setup
 does not affect this error.

Table 50. Mixed Processor Configurations Error Summary

Error	Severity	System Action when BIOS Detects the Error Condition
Processor family not identical	Fatal	 Halts at POST code 0xE6. Takes fatal error action (see above) and does not boot until the fault condition is remedied.
Processor model not identical	Fatal	 Logs the POST error code into the SEL. Alerts the BMC to set the system status LED to steady amber. Displays 0196: Processor model mismatch detected message in the error manager. Takes fatal error action (see above) and does not boot until the fault condition is remedied.
Processor cores/threads not identical	Fatal	 Halts at POST code 0xE5. Takes fatal error action (see above) and does not boot until the fault condition is remedied.
Processor cache or home agent not identical	Fatal	 Halts at POST code 0xE5. Takes fatal error action (see above) and does not boot until the fault condition is remedied.
Processor frequency (speed) not identical	Fatal	If the frequencies for all processors can be adjusted to be the same: Adjusts all processor frequencies to the highest common frequency. Does not generate an error – this is not an error condition. Continues to boot the system successfully. If the frequencies for all processors cannot be adjusted to be the same: Logs the POST error code into the SEL. Alerts the BMC to set the system status LED to steady amber. Does not disable the processor. Displays 0197: Processor speeds unable to synchronize message in the error manager. Takes fatal error action (see above) and does not boot until the fault condition is remedied
Processor Intel® UPI link frequencies not identical	Fatal	If the link frequencies for all Intel® Ultra Path Interconnect (Intel® UPI) links can be adjusted to be the same: • Adjusts all Intel® UPI interconnect link frequencies to highest common frequency. • Does not generate an error – this situation is not an error condition. • Continues to boot the system successfully. If the link frequencies for all Intel® UPI links cannot be adjusted to be the same: • Logs the POST error code into the SEL. • Alerts the BMC to set the system status LED to steady amber. • Does not disable the processor. • Displays 0195: Processor Intel® UPII link frequencies unable to synchronize message in the error manager. • Takes fatal error action (see above) and does not boot until the fault condition is remedied.
Processor microcode update failed	Major	 Logs the POST error code into the SEL. Displays 816x: Processor 0x unable to apply microcode update message in the error manager or on the screen. Takes major error action. The system may continue to boot in a degraded state, depending on the "POST Error Pause" setting in setup, or may halt with the POST error code in the error manager waiting for operator intervention.
Processor microcode update missing	Minor	 Logs the POST error code into the SEL. Displays 818x: Processor 0x microcode update not found message in the error manager or on the screen. The system continues to boot in a degraded state, regardless of the "POST Error Pause" setting in setup.

Appendix E. System Configuration Table for Thermal Compatibility

This appendix provides tables listing system configuration compatibility data based on various supported system operating thermal limits. Section E.1 identifies supported system configurations while the system is in "normal" operating mode, meaning that all systems fans are present, online, and operational. Section E.2 identifies supported system configurations while the system is in a "fan fail" mode, meaning more than one fan rotor in the same fan or different fans are no longer operational and fan redundancy is lost.

E1 Normal Operating Mode

For the tables in this section, a bullet (•) indicates full support without limitation. A cell with a number indicates conditional support. See the following notes. A blank cell indicates that the configuration is not supported.

The following list of notes support criteria associated with specific configurations identified in the following tables.

Notes:

- 1. The 27 °C configuration alone is limited to elevations of 900 m or less. Altitude higher than 900 m needs to be derated, same as ASHRAE Class 2.
- 2. PSU inlet temperature sensor will exceed 61 °C Over Temperature Protection (OTP), which impacts system power to limit system performance.
- 3. Processor and memory throttling (over specification ≤10 °C) may occur, which may impact system performance, but system is not shut down.
- 4. Processor and memory heavy throttling (over specification >10 °C) may impact system performance, but system is not shut down.
- 5. Use of the designated PCIe slot is limited to add-in cards that have airflow requirements of 100 LFM or less. See the add-in card specifications for airflow requirements.
- 6. Liquid Cooled SKU support ASHRAE W4 (45 °C).
- 7. Liquid Temperature derate to W2 (27 °C).
- 8. SSD Throughput throttling is expected when SSD SMART thermal sensor exceeds 70 °C.

Table 51. Thermal Configuration Matrix – Normal Operating Mode (Table 1 of 3) (1U Air Cooled, 1U EVAC)

N "•" = Fi "4,5" (Cell with lim	lormal Op ull Suppor number) nitation (Se ' " (Blank)	guration Matrix – erating Mode t without limitation = Conditional support with ee notes above) = No support				D50TN	em SKUs P 1U AC							Base Syst D50TNP	1U EVAC			
ASHRAE (see Note 1)	Classific	ations n Ambient	15 °C	20 °C	25 °C 25 °C	27 °C	32 °C	A2 35 °C	A3 40 °C	A4 45 °C	15 °C	20°C	25 °C	27 °C	32 °C 32 °C	A2 35 °C	A3 40 °C	45 °C
	2100 \\		•	•	•	(1)	•	2	2	2	•	•	•	(1)	•	2	2	2
PSU	2100 W 1600 W			•	•	•	•	2	2	2	•	•	•	•	•	2	2	2
	1000 W	40C (SP XCC) Intel® Xeon® Platinum 8380	•	3	·						•	•	•	•	3	3	4	
	270 W	38C (SP XCC) Intel® Xeon® Platinum 8368 38C (SP XCC) Intel® Xeon®	•	3							•	•	•	•	3	3	4	
		Platinum 8368Q																
	265 W	32C (SP XCC) Intel® Xeon® Platinum 8362	3	4							•	•	3	3	4	4		
	250 W	36C (SP XCC) Intel® Xeon® Platinum 8360Y	•	3							•	•	•	•	3	3	4	
	230 11	32C (SP XCC) Intel® Xeon® Platinum 8358	•	3							•	•	•	•	3	3	4	
	240 W	32C (SP XCC) Intel® Xeon® Platinum 8358P	•	3							•	•	•	•	3	3	4	
3 rd Gen Intel®	235 W	28C (SP XCC) Intel® Xeon® Gold 6348	•	3							•	•	•	•	3	3	4	
Xeon® Scalable		32C (SP XCC) Intel® Xeon® Platinum 8352Y 32C (SP XCC) Intel® Xeon®	•	•	•	•	3	3	4		•	•	•	•	•	•	3	4
Processors (see Note 3)		Platinum 8352S 18C (SP XCC) Intel® Xeon®	•	•	•	•	3	3	4		•	•	•	•	•	•	3	4
	205 W	Gold 6354 16C (SP XCC) Intel® Xeon®	•	3	3	3	4	4			•	•	•	•	3	3	4	
		Gold 6346 32C (SP XCC) Intel® Xeon®	•	3	3	3	4	4			•	•	•	•	3	3	4	
		Gold 6338	•	•	•	•	3	3	4		•	•	•	•	•	•	3	4
	28C (SP XCC) Intel® Xeon® Gold 6330 36C (SP XCC) Intel® Xeon® 195 W Platinum 8352V 32C (SP XCC) Intel® Xeon® Platinum 8352M	Gold 6330	•	•	•	•	3	3	4		•	•	•	•	•	•	3	4
		•	•	3	3	3	4			•	•	•	•	3	3	4		
			•	•	•	•	3	3	4		•	•	•	•	•	•	3	4
		Gold 6338N	•	•	•	•	3	3	4		•	•	•	•	•	•	3	4
	165 W	28C (SP XCC) Intel® Xeon® Gold 6330N	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	•

! "•" = F "4,5" (Cell with lin	Normal Op ull Suppor n number) nitation (Se " " (Blank)	guration Matrix – erating Mode t without limitation = Conditional support with ee notes above) = No support					P 1U AC	s:						Base Syst D50TNP	1U EVAC			
ASHRAE (see Note 1)	Classific	ations m Ambient	15 °C 15 °C	20 °C	25 °C	27 °C 27 °C (1)	32 °C	A2 35 °C	A3 40 °C	45 °C	15 °C	20 °C	25 °C 25 °C	27 °C 27 °C (1)	32 °C	A2 35 °C	A3 40 °C	45 °C
	150 W	24C (SP XCC) Intel® Xeon® Gold 5318N	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	•
	230 W	24C (SP HCC) Intel® Xeon® Gold 6342	•	•	3	3	3	4			•	•	•	•	3	3	4	
		26C (SP HCC) Intel® Xeon® Gold 5320	•	•	3	3	3	4			•	•	•	•	3	3	4	
	185 W	24C (SP HCC) Intel® Xeon® Gold 6336Y	•	•	3	3	3	4			•	•	•	•	3	3	4	
		16C (SP HCC) Intel® Xeon® Gold 6326	•	•	3	3	3	4			•	•	•	•	3	3	4	
		24C (SP HCC) Intel® Xeon® Gold 5318S	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	•
	165 W	8C (SP HCC) Intel® Xeon® Gold 6334	•	3	3	3	3	4			•	•	•	•	3	3	4	_
		24C (SP HCC) Intel® Xeon® Gold 5318Y	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	•
	150 W	20C (SP HCC) Intel® Xeon® Silver 4316 12C (SP HCC) Intel® Xeon®	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	•
		Gold 5317 8C (SP HCC) Intel® Xeon®	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	•
	140 W	Gold 5315Y 16C (SP HCC) Intel® Xeon®	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	135 W	Silver 4314 12C (SP HCC) Intel® Xeon®	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	120 W	Silver 4310 8C (SP HCC) Intel® Xeon®	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	•
	105 W	Silver 4309Y 24C (SP NEBS) Intel® Xeon®	•	•	•	•	•	•	3	3	•	•	•	•	•	•	•	3
	165 W	Gold 6338T 20C (SP NEBS) Intel® Xeon®	•	•	•	3	3	4	4		•	•	•	•	•	3	3	4
	150 W	Gold 5320T 10C (SP NEBS) Intel® Xeon®	•	•	•	3	3	4	_		•	•	•	•	•	3	3	3
	105 W	Silver 4310T	•	•	•	•	•	3	3	3	•	•	•	•	•	•	•	•
		QRx4 (16Gb) - 2DPC 13 W	•	•	•	•	•	•	3	3	•	•	•	•	3	3	4	4
		1 8Rx4 - 2DPC 16 W QRx4 - 2DPC 12 W	•	•	3	3	3	3	3	3	•	•	3	3	3	3	4	4
Memory Type		ORx4 - 2DPC 12 W	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
. icinory rype		DRx8 - 2DPC 4 W		•	•	•	•	•	•	•		•	•	•	•	•		•
		SRx4 - 2DPC 5 W	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
		SRx8 -2DPC 3 W	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

N "•" = Fi "4,5" (Cell with lim	mal Configuration Matrix – lormal Operating Mode all Support without limitation number) = Conditional support with itation (See notes above) " (Blank) = No support			ı	Base Syst D50TN	em SKU: P 1U AC	s:						•	tem SKU 1U EVA			
ASHRAE (see	Classifications	15 °C	20 °C	25 °C	27 °C	32 °C	A2	A3	A4	15 °C	20 °C	25 ℃	27 °C	32 °C	A2	А3	A4
Note 1)	Maximum Ambient	15 ℃	20 °C	25 °C	27 °C (1)	32 °C	35 °C	40 °C	45 °C	15 °C	20 °C	25 °C	27 °C (1)	32 °C	35 °C	40 °C	45 °C
Intel® Optane™	128 Gb (TDP=12 W)	•	•	•	•	•	3	4	4								
PMem 200	256 GB (TDP=15 W)	•	•	3	3	3	3	4	4								
series	512 GB (TDP=15 W)	•	•	3	3	3	3	4	4								
	Riser #1 - Bottom Slot - 300 LFM	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Add-in Cards	Riser #1 - Middle Slot - 300 LFM																
Add-III Calds	Riser #2 - Bottom Slot - 300 LFM	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	Riser #2 - Middle Slot - 300 LFM																
2.5" PCle	D7-P5510/D5-P4326 Series																
NVMe SSD	DC P4800X/P4610/P4510/P5800x																
(rated to 70 °C)	Kioxia* CM6&CD6/ Samsung PM1733																
14.0.CCD	DC P4511 (8.25 W)	•	•	•	•	•	•	8	8	•	•	•	•	•	•	8	8
M.2 SSD (rated to	Kioxia* XG6 (5 W)	•	•	•	•	•	•	•	8	•	•	•	•	•	•	•	8
70 °C)	DC P4801 (11.7 W)	•	•	•	•	8	8	8	8	•	•	•	•	8	8	8	8
70 C)	DC S4510 (4 W)	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
NVMe RSSD	D5-P4326 Series (rated to 70 °C)																
NVME KSSD	DC P4510 Series (rated to 70 °C)																
	Tesla* V100 - DW – 250 W																
PCIe Card	Intel® FPGA PAC D5005 - DW – 225 W																
	Tesla* A100 - DW																

Table 52. Thermal Configuration Matrix – Normal Operating Mode (Table 2 of 3) (2U Air Cooled, Accelerator)

!"•" = F "•" = F "4,5" (Cell with lim	Normal Op ull Suppor n number) nitation (Se " " (Blank)	guration Matrix – erating Mode t without limitation = Conditional support with ee notes above) = No support					P 2U AC								P ACCL	s:		
ASHRAE	Classific	ations	15 ℃	20 °C	25 °C	27 °C	32 °C	A2	A3	A4	15 °C	20 °C	25 °C	27 °C	32 °C	A2	A3	A4
(see Note 1)		m Ambient	15 °C	20 °C	25 °C	27 °C (1)	32 °C	35 °C	40 °C	45 °C	15 °C	20 °C	25 ℃	27 °C (1)	32 °C	35 °C	40°C	45°C
PSU	2100 W		•	•	•	•	•	•	2	2	•	•	•	•	•	•	2	2
	1600 W	T	•	•	•	•	•	•	2	2	•	•	•	•	•	•	2	2
		40C (SP XCC) Intel® Xeon® Platinum 8380	•	•	•	•	•	•	3	4	•	•	•	•	•	•	3	4
	270 W	38C (SP XCC) Intel® Xeon® Platinum 8368	•	•	•	•	•	•	3	4	•	•	•	•	•	•	3	4
		38C (SP XCC) Intel® Xeon® Platinum 8368Q																
	265 W	32C (SP XCC) Intel® Xeon® Platinum 8362	•	•	•	•	•	•	3	4	•	•	•	•	•	•	3	4
	250 W	36C (SP XCC) Intel® Xeon® Platinum 8360Y	•	•	•	•	•	•	3	4	•	•	•	•	•	•	3	4
	230 W	32C (SP XCC) Intel® Xeon® Platinum 8358	•	•	•	•	•	•	3	4	•	•	•	•	•	•	3	4
	240 W	32C (SP XCC) Intel® Xeon® Platinum 8358P	•	•	•	•	•	•	3	4	•	•	•	•	•	•	3	4
3 rd Gen Intel®	235 W	28C (SP XCC) Intel® Xeon® Gold 6348	•	•	•	•	•	•	3	4	•	•	•	•	•	•	3	4
Xeon® Scalable		32C (SP XCC) Intel® Xeon® Platinum 8352Y	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	3
Processors (See Note 3)		32C (SP XCC) Intel® Xeon® Platinum 8352S	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	3
(000 11010 0)	205 W	18C (SP XCC) Intel® Xeon® Gold 6354	•	•	•	•	•	•	3	4	•	•	•	•	•	•	3	4
	203 11	16C (SP XCC) Intel® Xeon® Gold 6346	•	•	•	•	•	•	3	4	•	•	•	•	•	•	3	4
		32C (SP XCC) Intel® Xeon® Gold 6338	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	3
	28C (S Gold 6 195 W 36C (S Platinu	28C (SP XCC) Intel® Xeon® Gold 6330	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	3
		36C (SP XCC) Intel® Xeon® Platinum 8352V	•	•	•	•	•	•	3	4	•	•	•	•	•	•	3	4
	185 \//	32C (SP XCC) Intel® Xeon® Platinum 8352M	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	3
	185 W	32C (SP XCC) Intel® Xeon® Gold 6338N	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	3
	165 W	28C (SP XCC) Intel® Xeon® Gold 6330N	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

^ "•" = F "4,5" (Cell with lim	lormal Op ull Suppor number) nitation (Se ' " (Blank)	guration Matrix – erating Mode t without limitation = Conditional support with te notes above) = No support				D50TN	tem SKUs P 2U AC							D50TN	tem SKU IP ACCL			
ASHRAE (see Note 1)	Classific Maximur	ations n Ambient	15 °C	20 °C	25 °C 25 °C	27 °C 27 °C (1)	32 °C	A2 35 °C	A3 40 °C	45 °C	15 °C	20 °C	25 °C 25 °C	27 °C 27 °C (1)	32 °C	A2 35 °C	A3 40°C	45°C
	150 W	24C (SP XCC) Intel® Xeon® Gold 5318N	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	230 W	24C (SP HCC) Intel® Xeon® Gold 6342	•	•	•	•	•	•	3	4	•	•	•	•	•	•	3	4
		26C (SP HCC) Intel® Xeon® Gold 5320	•	•	•	•	•	•	3	4	•	•	•	•	•	•	3	4
	185 W	24C (SP HCC) Intel® Xeon® Gold 6336Y	•	•	•	•	•	•	3	4	•	•	•	•	•	•	3	4
		16C (SP HCC) Intel® Xeon® Gold 6326	•	•	•	•	•	•	3	4	•	•	•	•	•	•	3	4
		24C (SP HCC) Intel® Xeon® Gold 5318S	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	165 W	8C (SP HCC) Intel® Xeon® Gold 6334	•	•	•	•	•	•	3	4	•	•	•	•	•	•	3	4
		24C (SP HCC) Intel® Xeon® Gold 5318Y	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	150 W	20C (SP HCC) Intel® Xeon® Silver 4316 12C (SP HCC) Intel® Xeon®	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
		Gold 5317	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	140 W	8C (SP HCC) Intel® Xeon® Gold 5315Y	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	135 W	16C (SP HCC) Intel® Xeon® Silver 4314	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	120 W	12C (SP HCC) Intel® Xeon® Silver 4310	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	105 W	8C (SP HCC) Intel® Xeon® Silver 4309Y 24C (SP NEBS) Intel® Xeon®	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	165 W	Gold 6338T 20C (SP NEBS) Intel® Xeon®	•	•	•	•	•	•	3	3	•	•	•	•	•	•	3	3
	150 W	Gold 5320T 10C (SP NEBS) Intel® Xeon® Silver 4310T	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
		Silver 4310T QRx4 (16Gb) - 2DPC 13 W	•	•	•	•	•	•	3	3	•	•	•	•	•	•	3	3
		1 8Rx4 - 2DPC 16 W	•	•	•	•	•	•	3	3	•	•	•	•	•	•	3	3
		QRx4 - 2DPC 12 W	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	3
Memory Type		DRx4 - 2DPC 7 W		•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
7 - 7 - 9		DRx8 - 2DPC 4 W	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
		Rx4 - 2DPC 5 W	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
		Rx8 -2DPC 3 W	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

! o" = F" 4,5" (Cell with lin	rmal Configuration Matrix – Normal Operating Mode ull Support without limitation n number) = Conditional support with nitation (See notes above) " " (Blank) = No support			E	•	em SKUs P 2U AC	s:					E	Base Syst D50TN	em SKU P ACCL	s:		
ASHRAE	Classifications	15 °C	20 °C	25 °C	27 °C	32 °C	A2	А3	A4	15 °C	20 °C	25 °C	27 °C	32 °C	A2	А3	A4
(see Note 1)	Maximum Ambient	15 ℃	20 °C	25 °C	27 °C (1)	32 °C	35 °C	40 °C	45 °C	15 °C	20 °C	25 °C	27 °C (1)	32 °C	35 °C	40°C	45°C
Intel® Optane™	128 Gb (TDP=12 W)	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	3
PMem 200	256 GB (TDP=15 W)	•	•	•	•	•	•	3	3	•	•	•	•	•	•	3	3
series	512 GB (TDP=15 W)	•	•	•	•	•	•	3	3	•	•	•	•	•	•	3	3
	Riser #1 - Bottom Slot - 300 LFM	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Add-in Cards	Riser #1 - Middle Slot - 300 LFM	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Add-III Cards	Riser #2 - Bottom Slot - 300 LFM	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	Riser #2 - Middle Slot - 300 LFM	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
2.5" PCle	D7-P5510/D5-P4326 Series	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
NVMe SSD	DC P4800X/P4610/P4510/P5800x	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
(rated to 70°C)	Kioxia* CM6&CD6/ Samsung PM1733	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
M 2 66D	DC P4511 (8.25 W)	•	•	•	•	•	•	8	8	•	•	•	•	•	•	8	8
M.2 SSD	Kioxia* XG6 (5 W)	•	•	•	•	•	•	•	8	•	•	•	•	•	•	•	8
(rated to 70°C)	DC P4801 (11.7 W)	•	•	•	•	8	8	8	8	•	•	•	•	8	8	8	8
70 C)	DC S4510 (4 W)	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
NVMe RSSD	D5-P4326 Series (rated to 70 °C)																
NVME RSSD	DC P4510 Series (rated to 70 °C)																
	Tesla* V100 - DW – 250 W									•	•	•	•	•	•	•	•
PCIe Card	Intel® FPGA PAC D5005 - DW – 225 W									•	•	•	•	•	•	•	•
	Tesla* A100 - DW									•	•	•	•	•	•	•	•

Table 53. Thermal Configuration Matrix – Normal Operating Mode (Table 3 of 3) (1U Storage, 1U Liquid Cooled)

"•" = F "4,5" (Cell wit lir	Normal Op full Suppo h number nitation (S " " (Blank)	iguration Matrix – perating Mode rt without limitation) = Conditional support with iee notes above) = No support				D50TNP	tem SKU: Storage							Base Syst D50TNP	1U LC[6]	1		
ASHRAE (see	Classific	ations	15 °C	20 °C	25 °C	27 °C	32 °C	A2	А3	A4	15 °C	20 °C	25 °C	27 °C	32 °C	A2	A3	A4
Note 1)	Maximu	m Ambient	15 °C	20 °C	25 °C	27 °C (1)	32 °C	35 °C	40 °C	45 °C	15 °C	20 °C	25 °C	27 °C (1)	32 °C	35°C	40 °C	45 °C
PSU	2100 W		•	•	•	•	•	2	2	2	•	•	•	•	•	•	2	2
P30	1600 W		•	•	•	•	•	2	2	2	•	•	•	•	•	•	2	2
		40C (SP XCC) Intel® Xeon® Platinum 8380	•	3							•	•	•	•	•	•	•	•
	270 W	38C (SP XCC) Intel® Xeon® Platinum 8368	•	3							•	•	•	•	•	•	•	•
		38C (SP XCC) Intel® Xeon® Platinum 8368Q									7	7	7	7	7	7	7	7
	265 W	32C (SP XCC) Intel® Xeon® Platinum 8362	3	4							•	•	•	•	•	•	•	•
	250 W	36C (SP XCC) Intel® Xeon® Platinum 8360Y	•	3							•	•	•	•	•	•	•	•
	250 W	32C (SP XCC) Intel® Xeon® Platinum 8358	•	3							•	•	•	•	•	•	•	•
	240 W	32C (SP XCC) Intel® Xeon® Platinum 8358P	•	3							•	•	•	•	•	•	•	•
3 rd Gen Intel®	235 W	28C (SP XCC) Intel® Xeon® Gold 6348	•	3							•	•	•	•	•	•	•	•
Xeon® Scalable		32C (SP XCC) Intel® Xeon® Platinum 8352Y	•	•	•	•	3	3	4		•	•	•	•	•	•	•	•
Processors (see Note 3)		32C (SP XCC) Intel® Xeon® Platinum 8352S	•	•	•	•	3	3	4		•	•	•	•	•	•	•	•
(See Note 3)	205 W	18C (SP XCC) Intel® Xeon® Gold 6354	•	3	3	3	4	4			•	•	•	•	•	•	•	•
	203 W	16C (SP XCC) Intel® Xeon® Gold 6346	•	3	3	3	4	4			•	•	•	•	•	•	•	•
		32C (SP XCC) Intel® Xeon® Gold 6338	•	•	•	•	3	3	4		•	•	•	•	•	•	•	•
	2	28C (SP XCC) Intel® Xeon® Gold 6330	•	•	•	•	3	3	4		•	•	•	•	•	•	•	•
	195 W	36C (SP XCC) Intel® Xeon® 95 W Platinum 8352V	•	•	3	3	3	4			•	•	•	•	•	•	•	•
	195 W Plat 320 105 W Plat	32C (SP XCC) Intel® Xeon® Platinum 8352M	•	•	•	3	3	4	4		•	•	•	•	•	•	•	•
	100 W	32C (SP XCC) Intel® Xeon® Gold 6338N	•	•	•	•	3	3	4		•	•	•	•	•	•	•	•
	165 W	28C (SP XCC) Intel® Xeon® Gold 6330N	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	•

"•" = F "4,5" (Cell with lin	Normal Opull Suppo n number nitation (S "" (Blank)	iguration Matrix – perating Mode rt without limitation = Conditional support with = No support				D50TNP	em SKUs Storage							D50TNP	tem SKU: 1U LC[6]	l		
ASHRAE (see Note 1)	Classific Maximu	ations m Ambient	15 °C 15 °C	20 °C	25 °C 25 °C	27 °C 27 °C (1)	32 °C 32 °C	A2 35 °C	A3 40 °C	A4 45 °C	15 °C	20 °C	25 °C	27 °C 27 °C (1)	32 °C	A2 35°C	A3 40 °C	45 °C
	150 W	24C (SP XCC) Intel® Xeon® Gold 5318N	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	•
	230 W	24C (SP HCC) Intel® Xeon® Gold 6342	•	•	3	3	3	4			•	•	•	•	•	•	•	•
		26C (SP HCC) Intel® Xeon® Gold 5320	•	•	3	3	3	4			•	•	•	•	•	•	•	•
	185 W	24C (SP HCC) Intel® Xeon® Gold 6336Y	•	•	3	3	3	4			•	•	•	•	•	•	•	•
		16C (SP HCC) Intel® Xeon® Gold 6326	•	•	3	3	3	4			•	•	•	•	•	•	•	•
		24C (SP HCC) Intel® Xeon® Gold 5318S	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	•
	165 W	8C (SP HCC) Intel® Xeon® Gold 6334	•	3	3	3	3	4			•	•	•	•	•	•	•	•
		24C (SP HCC) Intel® Xeon® Gold 5318Y 20C (SP HCC) Intel® Xeon®	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	•
	150 W	Silver 4316 12C (SP HCC) Intel® Xeon®	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	•
		Gold 5317 8C (SP HCC) Intel® Xeon®	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	•
	140 W	Gold 5315Y 16C (SP HCC) Intel® Xeon®	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	135 W	Silver 4314 12C (SP HCC) Intel® Xeon®	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	120 W	Silver 4310 8C (SP HCC) Intel® Xeon®	•	•	•	•	•	•	•	3	•	•	•	•	•	•	•	•
	105 W	Silver 4309Y 24C (SP NEBS) Intel® Xeon®	•	•	•	•	•	•	3	3	•	•	•	•	•	•	•	•
	165 W	Gold 6338T 20C (SP NEBS) Intel® Xeon®	•	•	3	3	3	4			•	•	•	•	•	•	•	•
	150 W	Gold 5320T	•	•	•	3	3	4			•	•	•	•	•	•	•	•
	105 W	Silver 4310T	•	•	•	•	•	3	3	3	•	•	•	•	•	•	•	•
		QRx4 (16Gb) - 2DPC 13 W 4 8Rx4 - 2DPC 16 W	•	•	3	3	3	3	3 4	3 4	•	•	3	3	3 4	3	3 4	3
		QRx4 - 2DPC 16 W	•	•	•	•	•	•	3	3	•	•	•	•	•	•	•	•
Memory Type		DRx4 - 2DPC 7 W	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
, ,,,,			•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	RDIMM S	SRx4 - 2DPC 5 W	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	RDIMM-DRx8 - 2DPC 4 W RDIMM SRx4 - 2DPC 5 W RDIMM SRx8 -2DPC 3 W			•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

"•" = F "4,5" (Cell wit lin	rmal Configuration Matrix – Normal Operating Mode full Support without limitation h number) = Conditional support with nitation (See notes above) " " (Blank) = No support			Ē	•	tem SKUs Storage								tem SKU: 1U LC[6]			
ASHRAE (see	Classifications	15 ℃	20 °C	25 °C	27 °C	32 °C	A2	А3	A4	15 °C	20 °C	25 °C	27 °C	32 °C	A2	А3	A4
Note 1)	Maximum Ambient	15 ℃	20 °C	25 °C	27 °C (1)	32 °C	35 °C	40 °C	45 °C	15 °C	20 °C	25 °C	27 °C (1)	32 °C	35°C	40 °C	45 °C
Intel®	128 Gb (TDP=12 W)	•	•	•	•	•	3	4	4								
Optane™	256 GB (TDP=15 W)	•	•	3	3	3	3	4	4								
PMem 200 series	512 GB (TDP=15 W)	•	•	3	3	3	3	4	4								
	Riser #1 - Bottom Slot - 300 LFM	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
Add-in Cards	Riser #1 - Middle Slot - 300 LFM																
Add-III Calds	Riser #2 - Bottom Slot - 300 LFM	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	Riser #2 - Middle Slot - 300 LFM																
2.5" PCle	D7-P5510/D5-P4326 Series																
NVMe SSD	DC P4800X/P4610/P4510/P5800x																
(rated to 70 °C)	Kioxia* CM6&CD6/ Samsung PM1733																
M.2 SSD	DC P4511 (8.25 W)	•	•	•	•	•	•	8	8	•	•	•	•	•	•	8	8
M.2 SSD (rated to	Kioxia* XG6 (5 W)	•	•	•	•	•	•	•	8	•	•	•	•	•	•	•	8
70 °C)	DC P4801 (11.7 W)	•	•	•	•	8	8	8	8	•	•	•	•	8	8	8	8
70 6	DC S4510 (4 W)	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
NVMe RSSD	D5-P4326 Series (rated to 70 °C)	•	•	•	•	•	•	•	•								
INVIVIE KOOD	DC P4510 Series (rated to 70 °C)	•	•	•	•	•	•	•	•								
	Tesla* V100 - DW – 250 W																
PCIe Card	Intel® FPGA PAC D5005 - DW – 225 W																
	Tesla* A100 - DW																

E2 Fan Fail Mode

For the tables in this section, a bullet (•) indicates full support without limitation. A cell with a number indicates conditional support. See the following notes. A blank cell indicates that the configuration is not supported.

The following list of notes support criteria associated with specific configurations identified in the following tables.

Notes:

- 1. The 27°C configuration alone is limited to elevations of 900 m or less. Altitude higher than 900 m need to be derated same as ASHRAE Class 2.
- 2. PSU inlet temperature sensor will exceed 61 °C Over Temperature Protection (OTP), which impacts system power to limit system performance.
- 3. Processor and memory throttling (over specification ≤10 °C) may occur, which may impact system performance, but system does not shut down.
- 4. Processor and memory heavy throttling (over specification >10 °C) may impact system performance, but the system is not shut down.
- 5. Use of the designated PCIe slot is limited to add-in cards that have airflow requirements of 100 LFM or less. See add-in card specifications for airflow requirements.
- 6. LC SKU support ASHRAE W4 (45 °C)
- 7. Liquid Temperature derate to W2 (27 °C)
- 8. SSD Throughput throttling is expected when SSD SMART thermal sensor exceeds 70 °C.

Table 54. Thermal Configuration Matrix – Fan Fail Mode (Table 1 of 3) (1U Air Cooled, 1U EVAC)

"•" = F: "4,5" (Cell with lim	Fan Faull Suppor n number) nitation (Se " " (Blank)	guration Matrix – ail Mode t without limitation = Conditional support with te notes above) = No support				D50TNI	em SKl P 1U AC						D	se Syst 50TNP	1U EVA	\C		
ASHRAE	Classific	ations	15 °C	20 °C	25 °C	27 °C	32 °C	A2	А3	A4	15 °C	20 °C	25 °C	27 °C	32 °C	A2	А3	A4
(see Note 1)	Maximu	m Ambient	15 °C	20 °C	25 °C	27 °C (1)	32 °C	35 ℃	40 °C	45 °C	15 °C	20 °C	25 °C	27 °C (1)	32 °C	35 °C	40°C	45 °C
PSU	2100 W		•	•	•	•	2	2			•	•	•	•	2	2		
. 50	1600 W	1	•	•	•	•	2	2			•	•	•	•	2	2		<u> </u>
		40C (SP XCC) Intel® Xeon® Platinum 8380	3	4							•	•	3	3	3	3		
	270 W	38C (SP XCC) Intel® Xeon® Platinum 8368	3	4							•	•	3	3	3	3		
		38C (SP XCC) Intel® Xeon® Platinum 8368Q																
	265 W	32C (SP XCC) Intel® Xeon® Platinum 8362									3	4						
	250 W	36C (SP XCC) Intel® Xeon® Platinum 8360Y	3	4							•	•	3	3	3	3		
	250 W	32C (SP XCC) Intel® Xeon® Platinum 8358	3	4							•	•	3	3	3	3		
	240 W	32C (SP XCC) Intel® Xeon® Platinum 8358P	3	4							•	•	3	3	3	3		
3 rd Gen Intel®	235 W	28C (SP XCC) Intel® Xeon® Gold 6348	3	4							•	•	3	3	3	3		
Xeon® Scalable		32C (SP XCC) Intel® Xeon® Platinum 8352Y	•	•	3	3	4	4			•	•	•	•	3	3		
Processors (see Note 3)		32C (SP XCC) Intel® Xeon® Platinum 8352S	•	•	3	3	4	4			•	•	•	•	3	3		
(See Note 3)	205 W	18C (SP XCC) Intel® Xeon® Gold 6354	3	3	4	4	4	4			•	•	3	3	3	3		
	203 11	16C (SP XCC) Intel® Xeon® Gold 6346	3	3	4	4	4	4			•	•	3	3	3	3		
		32C (SP XCC) Intel® Xeon® Gold 6338	•	•	3	3	4	4			•	•	•	•	•	•		
	28C (SP XCC) Intel® Xeon® Gold 6330 36C (SP XCC) Intel® Xeon® Platinum 8352V, 32C (SP XCC) Intel® Xeon® Platinum 8352M 32C (SP XCC) Intel® Xeon® Gold 6338N, NFV	Gold 6330	•	•	3	3	4	4			•	•	•	•	•	•		
		3	3	3	4	4	4			•	•	3	3	3	3			
		Platinum 8352M	3	3	4	4					•	•	•	3	3	4		
		•	•	3	3	4	4			•	•	•	•	3	3			
	165 W	28C (SP XCC) Intel® Xeon® Gold 6330N, NFV	•	•	•	•	3	3			•	•	•	•	•	•		

"•" = F "4,5" (Cell with lin	Fan Fa ull Suppor n number) nitation (Se ' " (Blank)	guration Matrix – ail Mode t without limitation = Conditional support with ee notes above) = No support				ise Syst D50TNI	P 1U AC						D	ise Syst 50TNP	1U EVA	AC .		
ASHRAE (see Note 1)	Classific Maximu	ations m Ambient	15 °C	20 °C	25 °C	27 °C 27 °C (1)	32 °C	A2 35 °C	40 °C	45 °C	15 °C	20 °C	25 °C	27 °C 27 °C (1)	32 °C	A2 35 °C	40°C	45 °C
	150 W	24C (SP XCC) Intel® Xeon® Gold 5318N	•	•	•	•	3	3			•	•	•	•	•	•		
	230 W	24C (SP HCC) Intel® Xeon® Gold 6342	•	3	4	4	4	4			•	•	3	3	3	3		
		26C (SP HCC) Intel® Xeon® Gold 5320	•	3	4	4	4	4			•	•	3	3	3	3		
	185 W	24C (SP HCC) Intel® Xeon® Gold 6336Y	•	3	4	4	4	4			•	•	3	3	3	3		
		16C (SP HCC) Intel® Xeon® Gold 6326	•	3	4	4	4	4			•	•	3	3	3	3		
		24C (SP HCC) Intel® Xeon® Gold 5318S	•	•	•	•	3	3			•	•	•	•	•	•		
	165 W	8C (SP HCC) Intel® Xeon® Gold 6334	3	3	4	4	4	4			•	•	3	3	3	3		
		24C (SP HCC) Intel® Xeon® Gold 5318Y	•	•	•	•	3	3			•	•	•	•	•	•		
	150 W	20C (SP HCC) Intel® Xeon® Silver 4316	•	•	•	•	•	•			•	•	•	•	•	•		_
		12C (SP HCC) Intel® Xeon® Gold 5317	•	•	•	•	•	•			•	•	•	•	•	•		
	140 W	8C (SP HCC) Intel® Xeon® Gold 5315Y	•	•	•	•	•	•			•	•	•	•	•	•		_
	135 W	16C (SP HCC) Intel® Xeon® Silver 4314	•	•	•	•	•	•			•	•	•	•	•	•		_
	120 W	12C (SP HCC) Intel® Xeon® Silver 4310 8C (SP HCC) Intel® Xeon®	•	•	•	•	•	•			•	•	•	•	•	•		_
	105 W	Silver 4309Y 24C (SP NEBS) Intel® Xeon®	•	•	•	•	•	•			•	•	•	•	•	•		
	165 W	Gold 6338T 20C (SP NEBS) Intel® Xeon®	3	3	4						•	•	3	3	4	4		
	150 W	Gold 5320T 10C (SP NEBS) Intel® Xeon®	•	•	3	3	3	4			•	•	•	•	3	3		
	105 W	Silver 4310T	•	•	•	•	•	3			•	•	•	•	•	•		
		QRx4 (16Gb) - 2DPC 13 W 1 8Rx4 - 2DPC 16 W	•	3	3	3	3	3			•	•	3	3	4	4		
		QRx4 - 2DPC 18 W	•	•	•	•	•	•				•	•	•	•	•		
Memory Type		DRx4 - 2DPC 7 W	•	•	•	•	•	•			•	•	•	•	•	•		
)) _[DRx8 - 2DPC 4 W	•	•	•	•	•	•			•	•	•	•	•	•		
	-	SRx4 - 2DPC 5 W	•	•	•	•	•	•			•	•	•	•	•	•		
	RDIMM S	SRx8 -2DPC 3 W	•	•	•	•	•	•			•	•	•	•	•	•		

"•" = Fı "4,5" (Cell with lim	mal Configuration Matrix – Fan Fail Mode ull Support without limitation number) = Conditional support with itation (See notes above) " (Blank) = No support				•	em SKl P 1U AC							-	em SKI 1U EV <i>F</i>			
ASHRAE	Classifications	15 °C	20 °C	25 ℃	27 °C	32 °C	A2	А3	A4	15 °C	20 °C	25 ℃	27 °C	32 °C	A2	А3	A4
(see Note 1)	Maximum Ambient	15 °C	20 °C	25 °C	27 °C (1)	32 °C	35 °C	40 °C	45 °C	15 °C	20 °C	25 °C	27 °C (1)	32 °C	35 °C	40°C	45 °C
Intel® Optane™	128 Gb (TDP=12 W)	•	•	•	•	3	3										
PMem 200	256 GB (TDP=15 W)	•	3	3	3	3	3										
series	512 GB (TDP=15 W)	•	3	3	3	3	3										
	Riser #1 - Bottom Slot - 300 LFM	•	•	•	•	•	•			•	•	•	•	•	•		
Add-in Cards	Riser #1 - Bottom Slot - 300 LFM Riser #1 - Middle Slot - 300 LFM																
Add-III Calds	Riser #2 - Bottom Slot - 300 LFM	•	•	•	•	•	•			•	•	•	•	•	•		
	Riser #2 - Middle Slot - 300 LFM																
2.5" PCle	D7-P4510/P4326 Series																
NVMe SSD	DC P4800X/P4610/P4510/P5800x																
(rated to 70°C)	Kioxia* CM6&CD6/ Samsung PM1733																
	DC P4511 (8.25 W)	•	•	•	•	8	8			•	•	•	•	8	8		
M.2 SSD	Kioxia* XG6 (5 W)	•	•	•	•	•	•			•	•	•	•	•	•		
(rated to 70°C)	DC P4801 (11.7 W)	•	•	8	8	8	8			•	•	8	8	8	8		
70 C)	DC S4510 (4 W)	•	•	•	•	•	•			•	•	•	•	•	•		
NVMe RSSD	D5-P4326 Series (rated to 70 °C)																
MAME K22D	DC P4510 Series (rated to 70 °C)																
_	Tesla* V100 - DW – 250 W																
PCIe Card	Intel® FPGA PAC D5005 - DW – 225 W																
	Tesla* A100 - DW																

Table 55. Thermal Configuration Matrix – Fan Fail Mode (Table 2 of 3) (2U Air Cooled, Accelerator)

Thermal Configuration Matrix – Fan Fail Mode "•" = Full Support without limitation "4,5" (Cell with number) = Conditional support with limitation (See notes above) "" (Blank) = No support						D50TN	tem SKU: P 2U AC	5:		Base System SKUs: D50TNP ACCL									
ASHRAE (see	Classific	ations	15 ℃	20 °C	25 °C	27 °C	32°C	A2	А3	A4	15 °C	20 °C	25 °C	27 °C	32 °C	A2	A3	A4	
Note 1)	Maximum Ambient		15 °C	20 °C	25 °C	27 °C (1)	32 °C	35 °C	40 °C	45 °C	15 °C	20 °C	25 °C	27 °C (1)	32 °C	35 °C	40 °C	45 °C	
PSU	2100 W		•	•	•	•	•	•			•	•	•	•	•	•		ļ	
	1600 W	T	•	•	•	•	•	•			•	•	•	•	•	•			
	270 W	40C (SP XCC) Intel® Xeon® Platinum 8380	•	•	•	•	3	3			•	•	•	•	3	3			
		38C (SP XCC) Intel® Xeon® Platinum 8368	•	•	•	•	3	3			•	•	•	•	3	3			
		38C (SP XCC) Intel® Xeon® Platinum 8368Q																	
	265 W	32C (SP XCC) Intel® Xeon® Platinum 8362	•	•	•	3	3	4			•	•	•	3	3	4			
	250 W	36C (SP XCC) Intel® Xeon® Platinum 8360Y	•	•	•	•	3	3			•	•	•	•	3	3			
	230 11	32C (SP XCC) Intel® Xeon® Platinum 8358	•	•	•	•	3	3			•	•	•	•	3	3			
	240 W	32C (SP XCC) Intel® Xeon® Platinum 8358P	•	•	•	•	3	3			•	•	•	•	3	3			
3 rd Gen Intel®	235 W	28C (SP XCC) Intel® Xeon® Gold 6348	•	•	•	•	3	3			•	•	•	•	3	3			
Xeon® Scalable		32C (SP XCC) Intel® Xeon® Platinum 8352Y	•	•	•	•	•	•			•	•	•	•	•	•			
Processors (see Note 3)		32C (SP XCC) Intel® Xeon® Platinum 8352S	•	•	•	•	•	•			•	•	•	•	•	•			
(000 110 00 0)	205 W	18C (SP XCC) Intel® Xeon® Gold 6354	•	•	•	•	3	3			•	•	•	•	3	3			
	200 11	16C (SP XCC) Intel® Xeon® Gold 6346	•	•	•	•	3	3			•	•	•	•	3	3			
		32C (SP XCC) Intel® Xeon® Gold 6338	•	•	•	•	•	•			•	•	•	•	•	•			
		28C (SP XCC) Intel® Xeon® Gold 6330	•	•	•	•	•	•			•	•	•	•	•	•			
	195 W	36C (SP XCC) Intel® Xeon® Platinum 8352V,	•	•	•	•	3	3			•	•	•	•	3	3			
	185 W	32C (SP XCC) Intel® Xeon® Platinum 8352M	•	•	•	•	•	•			•	•	•	•	•	•			
		32C (SP XCC) Intel® Xeon® Gold 6338N, NFV	•	•	•	•	•	•			•	•	•	•	•	•			
	165 W	28C (SP XCC) Intel® Xeon® Gold 6330N, NFV	•	•	•	•	•	•			•	•	•	•	•	•			

"•" = F "4,5" (Cell with lin	nitation (Se " " (Blank)					P 2U AC			Base System SKUs: D50TNP ACCL									
ASHRAE (see Note 1)	Classifications Maximum Ambient		15 °C	20 °C	25 °C 25 °C	27 °C 27 °C (1)	32°C	A2 35 °C	A3 40 °C	45 °C	15 °C	20 °C	25 °C 25 °C	27 °C 27 °C (1)	32 °C	A2 35 °C	A3 40 °C	45 °C
	150 W	24C (SP XCC) Intel® Xeon® Gold 5318N	•	•	•	•	•	•			•	•	•	•	•	•		
	230 W	24C (SP HCC) Intel® Xeon® Gold 6342	•	•	•	•	3	3			•	•	•	•	3	3		
		26C (SP HCC) Intel® Xeon® Gold 5320	•	•	•	•	3	3			•	•	•	•	3	3		
	185 W	24C (SP HCC) Intel® Xeon® Gold 6336Y	•	•	•	•	3	3			•	•	•	•	3	3		
		16C (SP HCC) Intel® Xeon® Gold 6326	•	•	•	•	3	3			•	•	•	•	3	3		
		24C (SP HCC) Intel® Xeon® Gold 5318S	•	•	•	•	•	•			•	•	•	•	•	•		
	165 W	8C (SP HCC) Intel® Xeon® Gold 6334	•	•	•	•	3	3			•	•	•	•	3	3		
		24C (SP HCC) Intel® Xeon® Gold 5318Y 20C (SP HCC) Intel® Xeon®	•	•	•	•	•	•			•	•	•	•	•	•		
	150 W	Silver 4316 12C (SP HCC) Intel® Xeon®	•	•	•	•	•	•			•	•	•	•	•	•		
		Gold 5317 8C (SP HCC) Intel® Xeon®	•	•	•	•	•	•			•	•	•	•	•	•		
	140 W	Gold 5315Y 16C (SP HCC) Intel® Xeon®	•	•	•	•	•	•			•	•	•	•	•	•		
	135 W	Silver 4314 12C (SP HCC) Intel® Xeon®	•	•	•	•	•	•			•	•	•	•	•	•		
	120 W	Silver 4310 8C (SP HCC) Intel® Xeon®	•	•	•	•	•	•			•	•	•	•	•	•		
	105 W	Silver 4309Y 24C (SP NEBS) Intel® Xeon®	•	•	•	•	•	•			•	•	•	•	•	•		
	165 W	Gold 6338T 20C (SP NEBS) Intel® Xeon®	•	•	•	•	•	3			•	•	•	•	•	3		
	150 W	Gold 5320T	•	•	•	•	•	•			•	•	•	•	•	•		
	105 W	Silver 4310T																
		QRx4 (16Gb) - 2DPC 13 W	•	•	•	•	3	3			•	•	•	•	3	3		
		1 8Rx4 - 2DPC 16 W QRx4 - 2DPC 12 W	•	•	•	•	3	3		-	•	•	•	•	3	3		
Memory Type		ORx4 - 2DPC 12 W	•	•	•	•	•	3		 	•	•	•	•	•	3		
racinory rype	-	DRx8 - 2DPC 4 W		•	•		•	•		 	· ·	•	•	•	•	•		
		RDIMM SRx4 - 2DPC 5 W		•	•	•	•	•			•	•	•	•	•	•		
		SRx8 -2DPC 3 W	•	•	•	•	•	•			•	•	•	•	•	•		

Thermal Configuration Matrix – Fan Fail Mode "•" = Full Support without limitation "4,5" (Cell with number) = Conditional support with limitation (See notes above) "" (Blank) = No support			Base System SKUs: D50TNP 2U AC									Base System SKUs: D50TNP ACCL									
ASHRAE (see	Classifications	15 ℃	20 °C	25 °C	27 °C	32°C	A2	А3	A4	15 °C	20 °C	25 ℃	27 °C	32 °C	A2	A3	A4				
Note 1)	Maximum Ambient	15 ℃	20 °C	25 °C	27 °C (1)	32 °C	35 ℃	40 °C	45 °C	15 ℃	20 °C	25 °C	27 °C (1)	32 °C	35 °C	40 °C	45 °C				
Intel® Optane™	128 Gb (TDP=12 W)	•	•	•	•	•	3			•	•	•	•	•	3						
PMem 200	256 GB (TDP=15 W)	•	•	•	•	3	3			•	•	•	•	3	3						
series	512 GB (TDP=15 W)	•	•	•	•	3	3			•	•	•	•	3	3						
	Riser #1 - Bottom Slot - 300 LFM	•	•	•	•	•	•			•	•	•	•	•	•						
Add-in Cards	Riser #1 - Middle Slot - 300 LFM	•	•	•	•	•	•			•	•	•	•	•	•						
Add-III Calds	Riser #2 - Bottom Slot - 300 LFM	•	•	•	•	•	•			•	•	•	•	•	•						
	Riser #2 - Middle Slot - 300 LFM	•	•	•	•	•	•			•	•	•	•	•	•						
2.5" PCle	D7-P4510/P4326 Series	•	•	•	•	•	•			•	•	•	•	•	•						
NVMe SSD	DC P4800X/P4610/P4510/P5800x	•	•	•	•	•	•			•	•	•	•	•	•						
(rated to 70 °C)	Kioxia* CM6&CD6/ Samsung PM1733	•	•	•	•	•	•			•	•	•	•	•	•						
Macco	DC P4511 (8.25 W)	•	•	•	•	8	8			•	•	•	•	8	8						
M.2 SSD (rated to	Kioxia* XG6 (5 W)	•	•	•	•	•	•			•	•	•	•	•	•						
(rated to 70 °C)	DC P4801 (11.7 W)	•	•	8	8	8	8			•	•	8	8	8	8						
70 C)	DC S4510 (4 W)	•	•	•	•	•	•			•	•	•	•	•	•						
NVMe RSSD	D5-P4326 Series (rated to 70 °C)																				
INVIVIE KOOD	DC P4510 Series (rated to 70 °C)																				
	Tesla* V100 - DW – 250 W									•	•	•	•	•	•						
PCIe Card	Intel® FPGA PAC D5005 - DW – 225 W									•	•	•	•	•	•						
	Tesla* A100 - DW									•	•	•	•	•	•						

Table 56. Thermal Configuration Matrix – Fan Fail Mode (Table 3 of 3) (Storage, 1U Liquid Cooled)

Thermal Configuration Matrix – Fan Fail Mode "•" = Full Support without limitation "4,5" (Cell with number) = Conditional support with limitation (See notes above) "" (Blank) = No support					E	-	em SKUs Storage			Base System SKUs: D50TNP 1U LC[6]									
	Classific		15 °C	20 °C	25 °C	27 °C	32 °C	A2	А3	A4	15 °C	20 °C	25 °C	27 °C	32 °C	A2	А3	A4	
ASHRAE (see Note 1)			15 °C	20 °C	25 °C	27 °C (1)	32 °C	35 °C	40 °C	45 °C	15 °C	20 °C	25 ℃	27 °C (1)	32 °C	35 °C	40 °C	45 °C	
	2100 W		•	•	•	•	2	2			•	•	•	•	•	•			
PSU	1600 W		•	•	•	•	2	2			•	•	•	•	•	•			
	270 W	40C (SP XCC) Intel® Xeon® Platinum 8380	3	4							•	•	•	•	•	•			
		38C (SP XCC) Intel® Xeon® Platinum 8368	3	4							•	•	•	•	•	•			
		38C (SP XCC) Intel® Xeon® Platinum 8368Q									7	7	7	7	7	7			
	265 W	32C (SP XCC) Intel® Xeon® Platinum 8362									•	•	•	•	•	•			
	250 W	36C (SP XCC) Intel® Xeon® Platinum 8360Y	3	4							•	•	•	•	•	•			
		32C (SP XCC) Intel® Xeon® Platinum 8358	3	4							•	•	•	•	•	•			
	240 W	32C (SP XCC) Intel® Xeon® Platinum 8358P	3	4							•	•	•	•	•	•			
3 rd Gen Intel®	235 W	28C (SP XCC) Intel® Xeon® Gold 6348	3	4							•	•	•	•	•	•			
Xeon® Scalable		32C (SP XCC) Intel® Xeon® Platinum 8352Y	•	•	3	3	4	4			•	•	•	•	•	•			
Processors (see Note 3)		32C (SP XCC) Intel® Xeon® Platinum 8352S	•	•	3	3	4	4			•	•	•	•	•	•			
	205 W	18C (SP XCC) Intel® Xeon® Gold 6354	3	3	4	4	4	4			•	•	•	•	•	•			
		16C (SP XCC) Intel® Xeon® Gold 6346	3	3	4	4	4	4			•	•	•	•	•	•			
		32C (SP XCC) Intel® Xeon® Gold 6338	•	•	3	3	4	4			•	•	•	•	•	•			
		28C (SP XCC) Intel® Xeon® Gold 6330	•	•	3	3	4	4			•	•	•	•	•	•			
	195 W	36C (SP XCC) Intel® Xeon® Platinum 8352V	3	3	3	4	4	4			•	•	•	•	•	•			
	185 W	32C (SP XCC) Intel® Xeon® Platinum 8352M	•	•	3	3	4				•	•	•	•	•	•		<u> </u>	
		32C (SP XCC) Intel® Xeon® Gold 6338N, NFV	•	•	3	3	4	4			•	•	•	•	•	•		<u> </u>	
	165 W	28C (SP XCC) Intel® Xeon® Gold 6330N, NFV	•	•	•	•	3	3			•	•	•	•	•	•			

"•" = F "4,5" (Cell with lin	nitation (Se " " (Blank)				Base Syst D50TNP	Storage			Base System SKUs: D50TNP 1U LC[6]									
ASHRAE (see Note 1)	Classifications Maximum Ambient		15 °C	20°C	25 °C 25 °C	27 °C	32 °C	A2 35 °C	A3 40 °C	45 °C	15 °C	20 °C	25 °C 25 °C	27 °C	32 °C	A2 35 °C	A3 40 °C	45 °C
	150 W	24C (SP XCC) Intel® Xeon® Gold 5318N	•	•	•	(1)	3	3			•	•	•	(1)	•	•		
	230 W	24C (SP HCC) Intel® Xeon® Gold 6342	•	3	4	4	4	4			•	•	•	•	•	•		
		26C (SP HCC) Intel® Xeon® Gold 5320	•	3	4	4	4	4			•	•	•	•	•	•		
	185 W	24C (SP HCC) Intel® Xeon® Gold 6336Y	•	3	4	4	4	4			•	•	•	•	•	•		
		16C (SP HCC) Intel® Xeon® Gold 6326	•	3	4	4	4	4			•	•	•	•	•	•		
		24C (SP HCC) Intel® Xeon® Gold 5318S 8C (SP HCC) Intel® Xeon®	•	•	•	•	3	3			•	•	•	•	•	•		
	165 W	Gold 6334 24C (SP HCC) Intel® Xeon®	3	3	4	4	4	4			•	•	•	•	•	•		
		Gold 5318Y 20C (SP HCC) Intel® Xeon®	•	•	•	•	3	3			•	•	•	•	•	•		
	150 W	Silver 4316 12C (SP HCC) Intel® Xeon®	•	•	•	•	•	•			•	•	•	•	•	•		
	14034	Gold 5317 8C (SP HCC) Intel® Xeon®	•	•	•	•	•	•			•	•	•	•	•	•		
	140 W	Gold 5315Y 16C (SP HCC) Intel® Xeon®	•	•	•	•	•	•			•	•	•	•	•	•		
	133 W	Silver 4314 12C (SP HCC) Intel® Xeon®	•	•	•	•	•	•			•	•	•	•	•	•		
	105 W	Silver 4310 8C (SP HCC) Intel® Xeon®	•	•	•	•	•	•			•	•	•	•	•	•		
	165 W	Silver 4309Y 24C (SP NEBS) Intel® Xeon® Gold 6338T	•	3	3	4	4					•	•	•	•	•		
	150 W	20C (SP NEBS) Intel® Xeon® Gold 5320T	•	•	3	3	3	4			•	•	•	•	•	•		
	105 W	10C (SP NFBS) Intel® Xeon®	•	•	•	•	•	3			•	•	•	•	•	•		
	LRDIMM	QRx4 (16Gb) - 2DPC 13 W	•	•	•	•	3	3			•	•	3	3	3	3		
		1 8Rx4 - 2DPC 16 W	•	3	3	3	3	3			•	•	4	4	4	4		
	LRDIMM	QRx4 - 2DPC 12 W	•	•	•	•	•	•			•	•	•	•	•	•		
Memory Type	RDIMM-I	DRx4 - 2DPC 7 W	•	•	•	•	•	•			•	•	•	•	•	•	-	
	RDIMM-I	RDIMM-DRx8 - 2DPC 4 W		•	•	•	•	•			•	•	•	•	•	•		
		RDIMM SRx4 - 2DPC 5 W		•	•	•	•	•			•	•	•	•	•	•		
	RDIMM SRx8 -2DPC 3 W		•	•	•	•	•	•			•	•	•	•	•	•		

Thermal Configuration Matrix – Fan Fail Mode "•" = Full Support without limitation "4,5" (Cell with number) = Conditional support with limitation (See notes above) " " (Blank) = No support				E	•	em SKUs Storage			Base System SKUs: D50TNP 1U LC[6]									
ASHRAE	Classifications	15 °C	20 °C	25 °C	27 °C	32 °C	A2	А3	A4	15 °C	20 °C	25 °C	27 °C	32 °C	A2	A3	A4	
(see Note 1)	Maximum Ambient	15 °C	20 °C	25 °C	27 °C (1)	32 °C	35 °C	40 °C	45 °C	15 °C	20 °C	25 °C	27 °C (1)	32 °C	35 °C	40 °C	45 °C	
Intel® Optane™	128 Gb (TDP=12 W)	•	•	•	•	3	3											
PMem 200	256 GB (TDP=15 W)	•	3	3	3	3	3											
series	512 GB (TDP=15 W)	•	3	3	3	3	3											
	Riser #1 - Bottom Slot - 300 LFM	•	•	•	•	•	•			•	•	•	•	•	•			
Add-in Cards	Riser #1 - Middle Slot - 300 LFM																	
Add-III Calds	Riser #2 - Bottom Slot - 300 LFM	•	•	•	•	•	•			•	•	•	•	•	•			
	Riser #2 - Middle Slot - 300 LFM																	
2.5" PCle	D7-P4510/P4326 Series																	
NVMe SSD	DC P4800X/P4610/P4510/P5800x																	
(rated to 70 °C)	Kioxia* CM6&CD6/ Samsung PM1733																	
Macco	DC P4511 (8.25 W)	•	•	•	•	8	8			•	•	•	•	8	8			
M.2 SSD (rated to	Kioxia* XG6 (5 W)	•	•	•	•	•	•			•	•	•	•	•	8			
70 °C)	DC P4801 (11.7 W)	•	•	8	8	8	8			•	•	8	8	8	8			
70 C)	DC S4510 (4 W)	•	•	•	•	•	•			•	•	•	•	•	•			
NVMe RSSD	D5-P4326 Series (rated to 70 °C)	•	•	•	•	•	•											
INVINE KSSD	DC P4510 Series (rated to 70 °C)	•	•	•	•	•	•											
	Tesla* V100 - DW – 250 W																	
PCIe Card	Intel® FPGA PAC D5005 - DW – 225 W																	
<u> </u>	Tesla* A100 - DW																	

Appendix F. Server Board Mechanical Drawings

The following figures provide the server board components and holes positions, also the keep-out zones.

F.1 Intel® Server Board D50TNP1SB

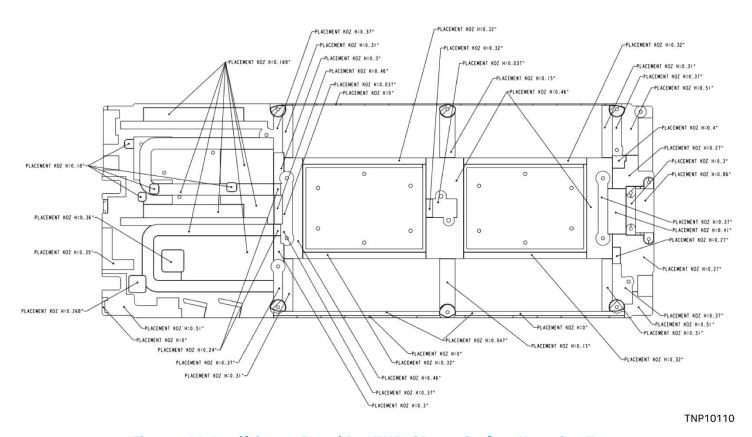


Figure 120. Intel® Server Board D50TNP1SB Top Surface Keep Out Zone

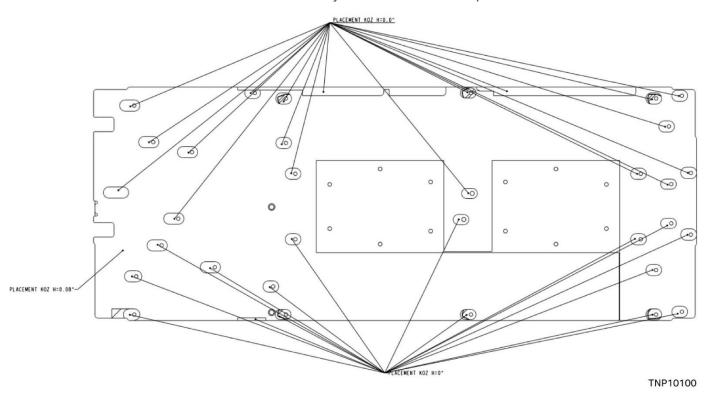


Figure 121. Intel® Server Board D50TNP1SB Bottom Surface Keep Out Zone

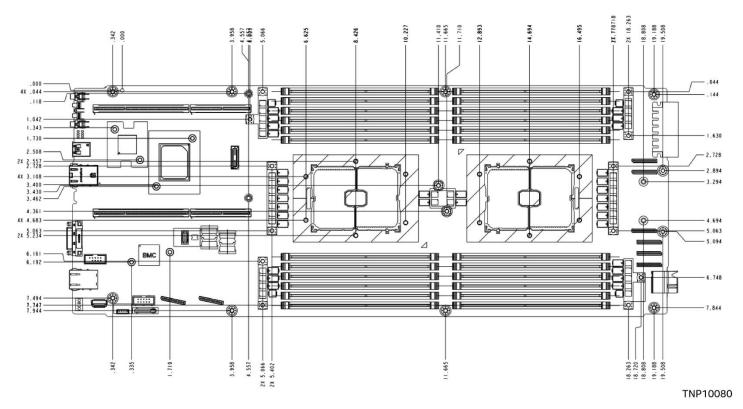


Figure 122. Intel® Server Board D50TNP1SB Components Position

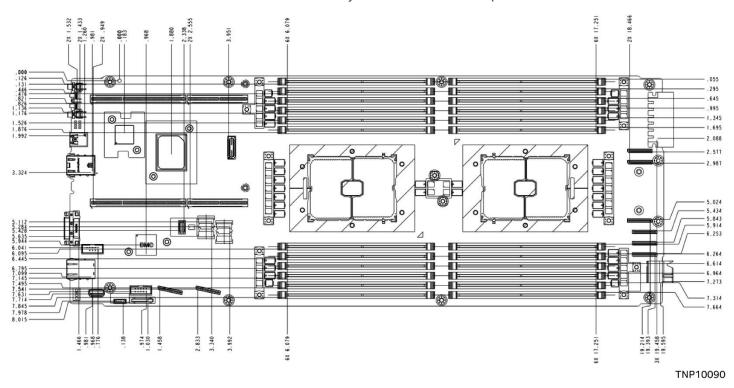


Figure 123. Intel® Server Board D50TNP1SB Holes Position

F.2 Intel® Server Board D50TNP1SBCR

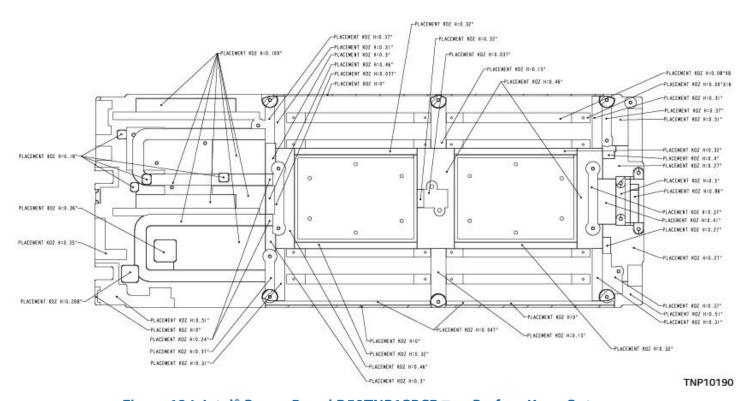


Figure 124. Intel® Server Board D50TNP1SBCR Top Surface Keep Out zone

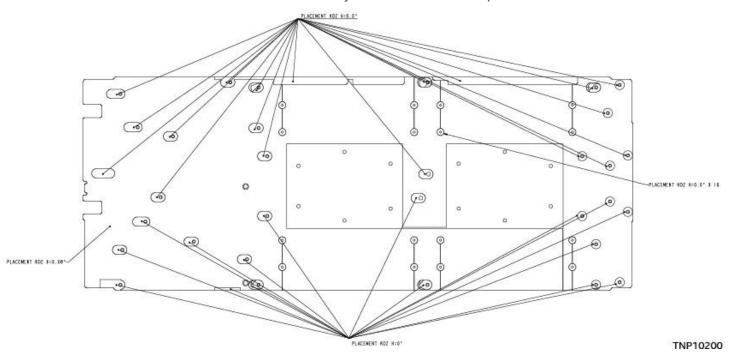


Figure 125. Intel® Server Board D50TNP1SBCR Bottom Surface Keep Out zone

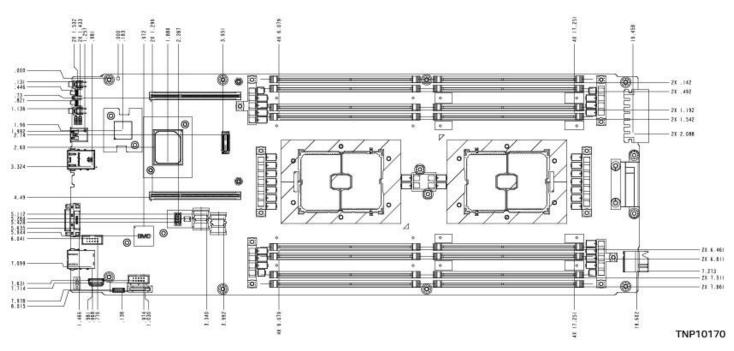


Figure 126. Intel® Server Board D50TNP1SBCR Components Position

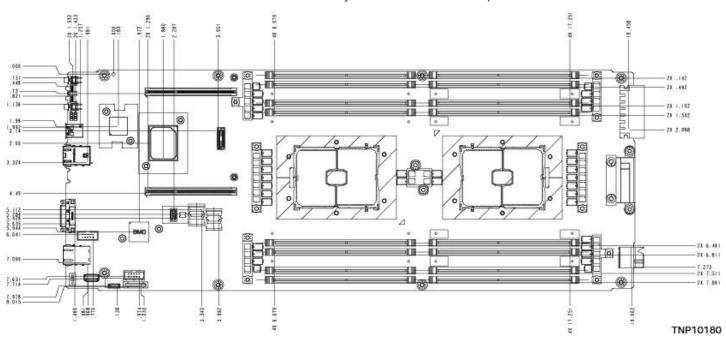
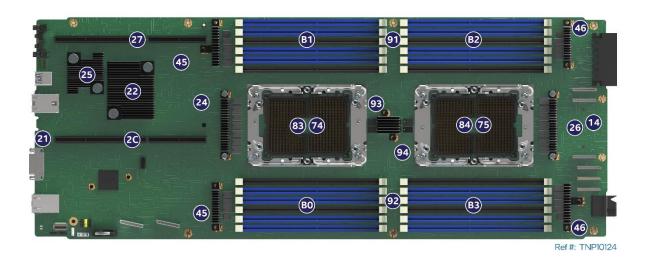


Figure 127. Intel® Server Board D50TNP1SBCR Holes Position

Appendix G. Board Sensors

The following figure provides the location of the sensors on the Intel® Server Board D50TNP1SB and D50TNP1SBCR. The following table provides a list of the sensors.



Note: Numbers in the figure are hexadecimal numbers.

Note: Intel® Server Board D50TNP1SB shown.

Figure 128. Board Sensor Map

Table 57. Available Sensors Monitored by the BMC

Sensor Number	Sensor Name
14h	Baseboard Outlet Temperature
21h	Baseboard Inlet Temperature
22h	PCH Temp
24h	CPU0 VCCIN
26h	CPU1 VCCIN
25h	Integrated LAN Controller Temperature
27h	PCI Riser 1 Temperature
2Ch	PCI Riser 2 Temperature
45h	Memory CPU0 VR Temperature
46h	Memory CPU1 VR Temperature
74h	CPU0 Therm Margin
75h	CPU1 Therm Margin
83h	CPU0 DTS Therm Margin
84h	CPU1 DTS Therm Margin
91h	CPU0 VCCIO
92h	CPU1 VCCIO
93h	CPU0 VCCANA
94h	CPU1 VCCANA
B0h	DIMM Aggregate Margin CPU0 ABCD
B1h	DIMM Aggregate Margin CPU0 EFGH
B2h	DIMM Aggregate Margin CPU1 ABCD
B3h	DIMM Aggregate Margin CPU1 EFGH

Appendix H. Server Board Installation and Component Replacement

This appendix provides general information necessary to install the server board into a server chassis. The system integrator should reference and follow all available system assembly instructions provided by the chassis manufacturer for full system assembly instructions.

This appendix also provides instructions for processor and memory replacement. Replacement instructions for all other system options should be provided by the chassis or system manufacturer.

Safety Warnings

Heed safety instructions: Before working with your server product, whether you are using this guide or any other resource as a reference, pay close attention to the safety instructions. You must adhere to the assembly instructions in this guide to ensure and maintain compliance with existing product certifications and approvals. Use only the described, regulated components specified in this guide. Use of other products/components will void the UL listing and other regulatory approvals of the product and will most likely result in noncompliance with product regulations in one or more regions in which the product is sold.

System power on/off: The power button DOES NOT turn off the system AC power. To remove power from the system, you must unplug the AC power cord. Make sure that the AC power cord is unplugged before you open the chassis, add, or remove any components.

Hazardous conditions, devices, and cables: Hazardous electrical conditions may be present on power, telephone, and communication cables. Turn off the server and disconnect the power cord, telecommunications systems, networks, and modems attached to the server before opening it. Otherwise, personal injury or equipment damage can result.

Installing or removing jumpers: A jumper is a small plastic encased conductor that slips over two jumper pins. Some jumpers have a small tab on top that you can grip with your fingertips or with a pair of fine needle nosed pliers. If your jumpers do not have such a tab, take care when using needle nosed pliers to remove or install a jumper; grip the narrow sides of the jumper with the pliers, never the wide sides. Gripping the wide sides can damage the contacts inside the jumper, causing intermittent problems with the function controlled by that jumper. Take care to grip with, but not squeeze, the pliers or other tool you use to remove a jumper, or you may bend or break the pins on the board.

Electrostatic Discharge (ESD)

Electrostatic discharge can damage the computer or the components within it. ESD can occur without the user feeling a shock while working inside the system chassis or while improperly handling electronic devices like processors, memory or other storage devices, and add-in cards.



Intel recommends that the following steps be taken when performing any procedures described within this document or while performing service to any computer system.

• Where available, all system integration and/or service should be performed at a properly equipped ESD workstation

- Wear ESD protective gear like a grounded antistatic wrist strap, sole grounders, and/or conductive shoes
- Wear an anti-static smock or gown to cover any clothing that may generate an electrostatic charge
- Remove all jewelry
- Disconnect all power cables and cords attached to the server before performing any integration or service
- Touch any unpainted metal surface of the chassis before performing any integration or service
- Hold all circuit boards and other electronic components by their edges only
- After removing electronic devices from the system or from their protective packaging, place them
 component side up on to a grounded anti-static surface or conductive workbench pad. Do not place
 electronic devices on to the outside of any protective packaging.

H.1 Server Board Installation Guidelines

This section provides general guidelines and recommendations for installing the server board into a server chassis. However, Intel highly recommends that system integrators follow all installation guidelines and instructions provided by the chassis manufacturer when integrating the server board into the chosen chassis.

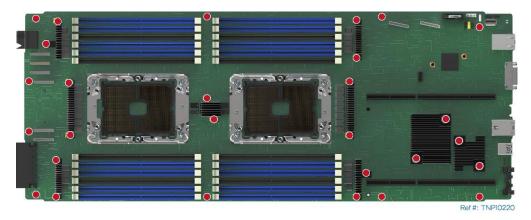


Figure 129. Server Board Mounting Hole Locations

This server board conforms to the industry standard extended ATX (EATX) form factor. This form factor should be considered when selecting a server chassis to mount the server board into.

Server boards and server chassis that conform to the EATX form factor will share compatible mounting features that match the server board mounting holes to fastener locations on the chassis base plate.

Server chassis may use different methods for securing the server board to the chassis. The selected chassis may have integrated mounting features or they may include separate mounting stand-offs that must be installed.

The following illustration identifies possible mounting options that can be used.

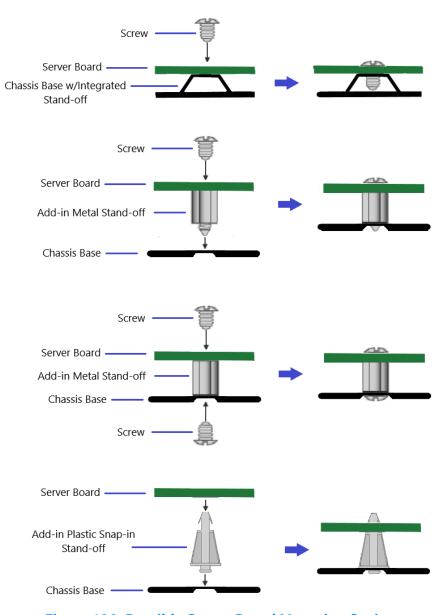


Figure 130. Possible Server Board Mounting Options

For mounting options that require the server board to be secured to the chassis using screws, Intel recommends tightening the screws using a torque or pneumatic screwdriver. The recommended torque setting is dependent on the screw type used. See the following table.

Table 58. Server Board Mounting Screw Torque Requirements

Screw Size	Torque Value	Tolerance ±
6–32	8 in-lb	1
М3	5 in-lb	1

H.2 Processor Replacement

Processors are part of an assembly referred to as a PHM (Processor Heat sink Module). A PHM consists of a processor, a processor carrier clip, and the processor heat sink that is preassembled into a single module before placement onto the processor socket assembly on the server board. The PHM concept reduces the risk of damaging pins in the processor socket during the replacement process.

The system may use 1U (Low-profile) or 2U size processor heat sinks. The following procedures can be applied to either option. The following procedure applies to processor heat sinks that are used by Intel for use in its server systems. If the processor heat sink is different from those depicted in the following procedures, then Intel recommends following the processor replacement procedures included in documentation supplied with the chosen non-Intel server system.

H.2.1 Processor Replacement for Standard Air-Cooled Heat Sinks

Components Required for each faulty processor:

- New 3rd Gen Intel® Xeon® Scalable processor + included shipping tray
- Existing processor carrier clip
- New processor heat sink or existing processor heat sink + new thermal interface material (TIM)

Required Tools and Supplies:

- Anti-static wrist strap and conductive workbench pad (recommended)
- ESD Gloves (recommended)
- T-30 Torx* screwdriver

Note: The installation figures in this section only display the 1U front heat sink. However, the processor installation procedure is the same, regardless of the size of the heat sink.

Caution: Fin edges of the processor heat sink are very sharp. Intel recommends wearing thin ESD protective gloves when handling the PHM during the following procedures.

Caution: Processor heat sinks are easily damaged if handled improperly. See the following figure for proper handling.

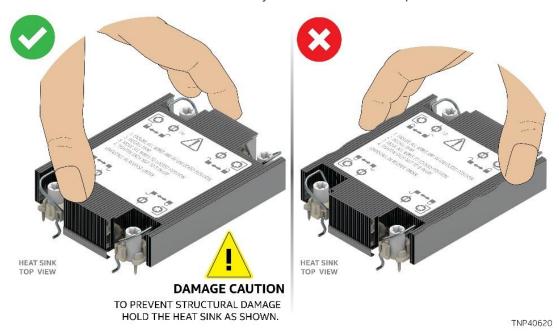


Figure 131. Processor Heat Sink Handling

H.2.1.1 Processor Heat Sink Module (PHM) Removal

1. Identify and locate the faulty processor.

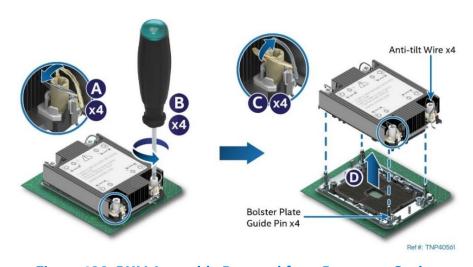


Figure 132. PHM Assembly Removal from Processor Socket

- 2. Ensure that the heat sink anti-tilt wires located over each of the four heat sink fasteners are in the outward position (see Letter A).
- 3. Using T-30 Torx* screwdriver, fully loosen all four heat sink fasteners in any order (see Letter B).
- 4. Set all four anti-tilt wires on the heat sink to the inward position (see Letter C).
- 5. Carefully grasp the PHM and lift it straight up and off the server board (see Letter D).
- 6. With the processor facing up, set the PHM down onto a flat surface.
- 7. Visually inspect that the processor socket is free of damage or contamination.

Caution: If debris is observed, blow it away gently. Do not use tweezers or any other hard tools to remove the debris.

8. If not replacing the processor, install the original plastic socket cover over the processor socket.

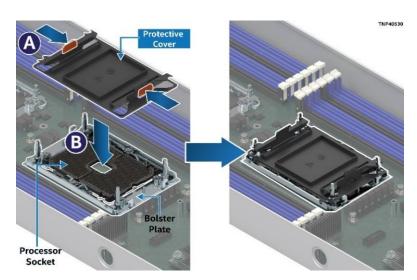


Figure 133. Reinstall the Socket Cover

- Squeeze the finger grips at each end of the cover (see Letter A).
- Carefully lower the cover over the four alignment pins of the bolster plate and onto the processor socket (see Letter B).
- Release finger grips to lock the cover in place.
- Ensure that the socket cover is locked in place.

Caution: Do not press down on the center of the socket cover.

H.2.1.2 PHM Disassembly

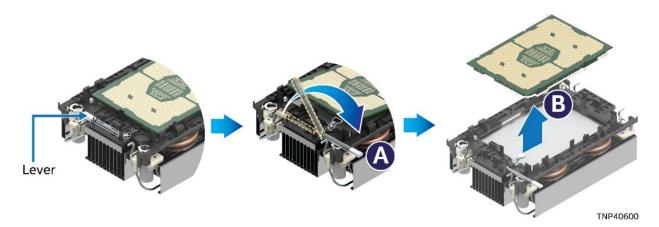


Figure 134. Processor Removal from PHM Assembly

- 1. While holding down the PHM, rotate the lever (see Letter A) from left to right until the processor lifts free from the processor carrier clip.
- 2. Holding down the processor carrier clip, carefully lift the processor and slide it out of the processor carrier clip (see Letter B).

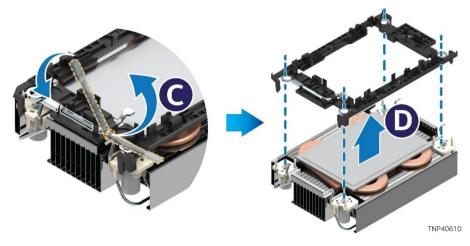


Figure 135. Processor Carrier Clip Removal from PHM Assembly

- 3. Return the lever to the original position (see Letter C).
- 4. Detach the processor carrier clip from the heat sink.
 - Unlatch the hook on each corner of the processor carrier clip and lift it from the heat sink (see Letter D).

H.2.1.3 PHM Reassembly

To properly reassemble the PHM and install it onto the server board, the procedures described in the following sections must be followed in the order specified. These instructions assume that the processor heat sink (new or reuse of existing) has the necessary Thermal Interface Material (TIM) (Honeywell* PTM7000) already applied to the bottom of the heat sink.

Caution: Full ESD precautions should be followed to perform reassembly of the PHM and reinstallation of the PHM to the server board. The processor itself should Not be handled.

Each component in the PHM assembly includes a Pin 1 indicator. Pin 1 indicator alignment between all components is required throughout the assembly process.

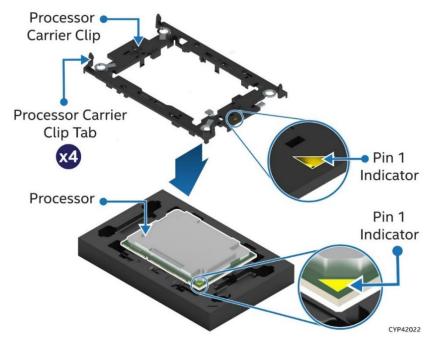


Figure 136. Installing Processor Carrier Clip onto Processor - Part 1

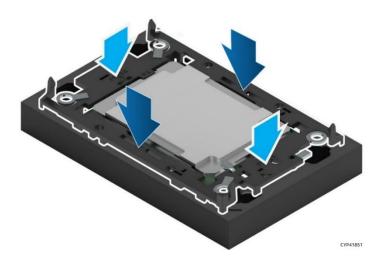


Figure 137. Installing Processor Carrier Clip onto Processor – Part 2

- 1. With the processor still in its tray, place the processor carrier clip over the processor.
- 2. Ensure that the Pin 1 indicator on the processor carrier clip is aligned with the Pin 1 indicator of the processor.
- 3. Gently press down simultaneously on two opposite sides of the processor carrier clip until it clicks in place.
- 4. Repeat step 3 for the other two sides.
- 5. Locate the processor heat sink. To avoid damage, grasp it by its narrower sides as shown below.

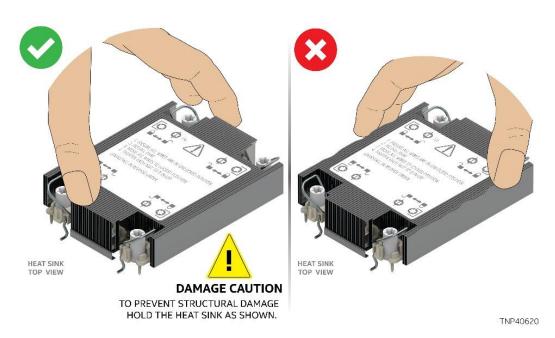


Figure 138. Processor Heat Sink Handling

6. Place the heat sink bottom side up onto a flat surface.

If reusing an existing heat sink

- Properly clean off existing thermal interface material (TIM) from the bottom of the heat sink
- Apply new TIM (Honeywell* PTM7000)

If using a new heat sink

Remove the plastic protective film (if present) from the Thermal Interface Material (TIM).

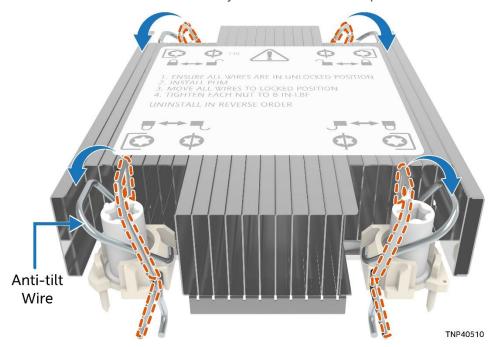


Figure 139. Processor Heat Sink Anti-tilt Wires in the Outward Position

7. Set the anti-tilt wire over each of the four heat sink fasteners to their outward position.

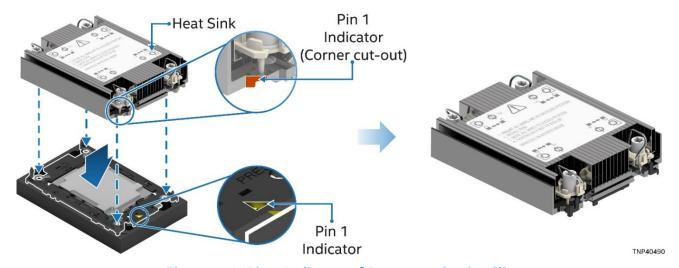


Figure 140. Pin 1 Indicator of Processor Carrier Clip

- 8. Align the Pin 1 indicator of processor carrier clip with one of the diagonally cut corners on the base of the heat sink. Or (if present) look for the Pin 1 indicator on the corner of the heat sink label.
- 9. Gently press down the heat sink onto the processor carrier clip until it clicks into place.
- 10. Ensure that all four heat sink corners are securely latched to the processor carrier clip tabs.

H.2.1.4 PHM Installation

1. If installed, remove the plastic cover from the processor socket.

Caution: Do not touch the socket pins. The pins inside the processor socket are extremely sensitive. A damaged processor socket may produce unpredictable system errors.

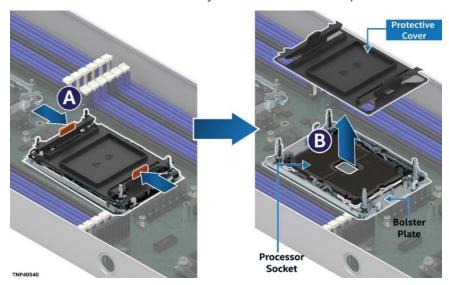


Figure 141. Socket Protective Cover Removal

- 2. Remove the protective cover by squeezing the finger grips (see Letter A) and pulling the cover up (see Letter B).
- 3. Ensure that the socket is free of damage or contamination before installing the PHM.

Caution: If debris is observed, blow it away gently. Do not remove it manually, such as with tweezers.

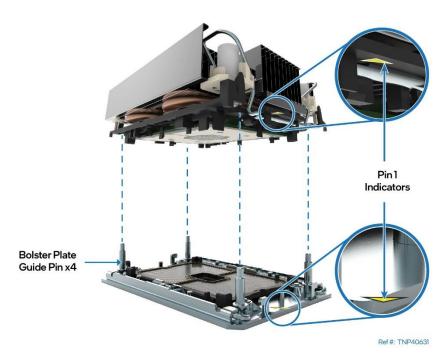


Figure 142. PHM Alignment with Socket Assembly

Caution: Processor socket pins are delicate and bend easily. Use extreme care when placing the PHM onto the processor socket. Do not drop it.

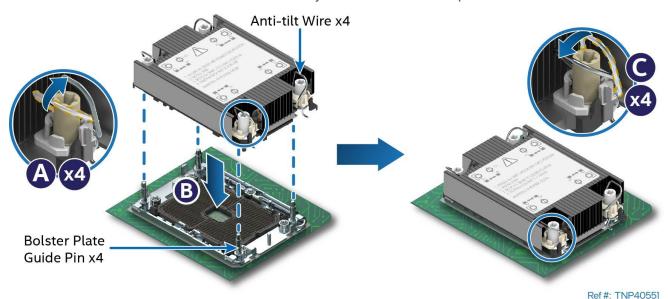


Figure 143. PHM Installation onto Server Board

- 4. Set all four anti-tilt wires on the heat sink to the inward position (see Letter A).
- 5. Align the Pin 1 indicators of the processor carrier clip and processor with the Pin 1 indicator on the socket assembly bolster plate.
- 6. Carefully lower the PHM over the four bolster plate alignment pins (see Letter B).
- 7. Ensure that the PHM is sitting flat and even on the bolster plate.
- 8. Set all four anti-tilt wires on the heat sink to the outward position (see Letter C).



Figure 144. Tighten Heat Sink Fasteners

9. Using a T30 Torx* screwdriver, tighten the heat sink fasteners to 8 in-lb. No specific sequence is needed for tightening.

Note: Intel strongly recommends that both processors are installed. If only one processor is installed, do not install a processor heat sink on an empty socket.

H.3 DIMM / Intel® Optane™ PMem Replacement Instructions

The Intel® Server Board D50TNP1SB and D50TNP1SBCR support standard DDR4, RDIMMs, and LDRIMMs. In addition, the D50TNP1SB server board supports Intel® Optane™ persistent memory 200 series modules (also known as, Intel® Optane™ PMem).

Required Tools and Supplies:

Anti-static wrist strap and conductive workbench pad (recommended)

The figures below show standard DDR4 DIMMs but the steps of DDR4 DIMM installation and replacement are the same between standard DDR4 DIMMs and Intel® Optane™ PMem modules.

Standard DDR4 DIMMs and Intel® Optane™ PMem devices will be commonly referred to as "memory device" in the following instructions.

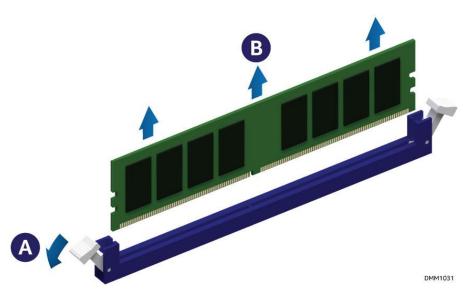


Figure 145. Removing the DIMM from an Air-Cooled System

- 1. Identify and locate the memory module to be replaced.
- 2. Ensure that the ejection tabs of adjacent memory slots are closed.
- 3. Open the ejection tabs at both ends of the selected memory slot (see Letter A). The memory module will slightly lift from the slot.
- 4. Holding the memory module by its edges, lift it away from the slot (see Letter B).

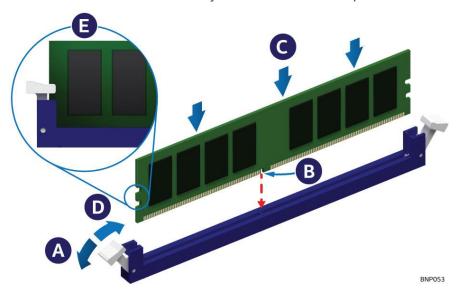


Figure 146. Installing the DIMM in an Air-Cooled System

- 5. Ensure that the ejection tabs at both ends of the memory slot are pushed outward to the open position (see Letter A).
- 6. Carefully unpack the replacement memory module, taking care to only handle the device by its outer edges.
- 7. Align the notch at the bottom edge of the memory module with the key in the memory slot (see Letter B).
- 8. Insert the memory module into the memory slot:
 - a. Using even pressure along the top edge, push down on the memory module (see letter C) until the ejection tabs of the memory slot snap into place (see Letter D).
- 9. Ensure that the ejection tabs are firmly in place (see Letter E).

Appendix I. Statement of Volatility

This Appendix describes the volatile and non-volatile components on the Intel® Server System D50TNP. It is not the intention of this document to include any components not directly mounted to the server board in the Intel® D50TNP Module or riser cards used within the Intel® D50TNP Modules or supported Intel chassis. These may include processors, memory, storage devices, or add-in cards.

The tables in this appendix provide the following data for each identified component.

Component Type

Three types of memory components are used on the Compute Module server board assembly. These include:

- **Non-volatile:** Non-volatile memory is persistent and is not cleared when power is removed from the system. Non-Volatile memory must be erased to clear data. The exact method of clearing these areas varies by the specific component. Some areas are required for normal operation of the server and clearing these areas may render the server board inoperable.
- Volatile: Volatile memory is cleared automatically when power is removed from the system.
- **Battery powered RAM:** Battery powered RAM is similar to volatile memory; however, is powered by a battery on the server board. Data in Battery powered RAM is persistent until the battery is removed from the server board.

Size

The size of each component includes sizes in bits, Kbits, bytes, kilobytes (KB), or megabytes (MB).

Board Location

The physical location of each component is specified in the Board Location column. The board location information corresponds to information on the silkscreen in the Compute Module server board.

User Data

The flash components on the Intel® Server D50TNP Family do not store user data from the operating system. No operating system level data is retained in any listed components after AC power is removed. The persistence of information written to each component is determined by its type as described in the table.

Each component stores data specific to its function. Some components may contain passwords that provide access to that device's configuration or functionality. These passwords are specific to the device and are unique and unrelated to operating system passwords. The specific components that may contain password data are:

- BIOS: The BIOS provides the capability to prevent unauthorized users from configuring BIOS settings
 when a BIOS password is set. This password is stored in BIOS flash and is only used to set BIOS
 configuration access restrictions.
- **BMC:** The Intel® Server D50TNP Family supports an Intelligent Platform Management Interface (IPMI) 2.0 conformant baseboard management controller (BMC). The BMC provides health monitoring, alerting, and remote power control capabilities for the Intel® D50TNP Module. The BMC does not have access to operating system level data.

The BMC supports the capability for remote software to connect over the network and perform health monitoring and power control. This access can be configured to require authentication by a password. If configured, the BMC will maintain user passwords to control this access. These passwords are stored in the BMC flash.

The server board in the Intel® D50TNP Module includes several components that can be used to store data. A list of those components is included in the following table.

Table 59. Intel® Server Board D50TNP1SB and D50TNP1SBCR Components

Component Type	Size	Board Location	User Data	Name
Non-Volatile	64 Mb	XU2	No (BIOS)	BIOS Flash
Non-Volatile	128 Mb	XU7D1	No (BMC FW)	BMC Flash
Non-Volatile	4 Mb	U61	No	LAN Flash
Non-Volatile	6962 B	J4E3	No (TPM)	ТРМ
Non-Volatile	UFM 3,200 Kb CFM 5,888 Kb	U41	No	FPGA
Volatile	512 Mb	U53	No	BMC SDRAM

Server boards in Intel® D50TNP Modules may include components used to store data. The following tables provide a list of components associated with specific system boards supported by this product family. For server board components, see the table above.

Table 60. Intel® D50TNP Module Components

Component Type	Size	Board Location	User Data	Name
Non-Volatile	256 B	U1	No	1U riser card FRU
Non-Volatile	256 B	U1	No	2U riser card FRU
Non-Volatile	256 B	U1N1	No	Storage Docking Board FRU
Non-Volatile	256 KB	U6	No	Storage Docking Board Re-timer EEPROM1
Non-Volatile	256 KB	U5	No	Storage Docking Board Re-timer EEPROM2
Non-Volatile	256 KB	U7	No	Storage Docking Board Re-timer EEPROM3
Non-Volatile	UFM 1,376 Kb CFM 2,240 Kb	U2	No	Storage Docking Board FPGA
Non-Volatile	256 B	U1	No	Accelerator riser card 1 FRU
Non-Volatile	256 Kb	U11	No	Accelerator riser card 1 Re-timer EEPROM1
Non-Volatile	256 Kb	U18	No	Accelerator riser card 1 Re-timer EEPROM2
Non-Volatile	256 B	U1	No	Accelerator riser card 2 FRU
Non-Volatile	256 Kb	U11	No	Accelerator riser card 2 Re-timer EEPROM1
Non-Volatile	256 Kb	U18	No	Accelerator riser card 2 Re-timer EEPROM2

System boards in the Intel® Server D50TNP chassis contain components used to store data. A list of components for the system boards in the chassis is included in the following table. For server board components and Intel® D50TNP Module components, see the sections above.

Table 61. Intel® Server D50TNP Chassis Components

Component Type	Size	Board Location	User Data	Name
Non-Volatile	256 B	U25	No	Power distribution board FRU
Non-Volatile	128 K + 3 Kb (boot)	U30	No	Power distribution board PIC MCU
Non-Volatile	4 Kb	U18	No	Ethernet Management Port SW EEPROM
Non-Volatile	256 B	U25	No	Ethernet Management Port FRU

Appendix J. Product Regulatory Compliance

This product has been evaluated and certified as Information Technology Equipment (ITE) that may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product certification categories and/or environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, and so on), other than an ITE application, will require further evaluation and may require additional regulatory approvals.

Intel has verified that all L3, L6, and L9 server products¹ <u>as configured and sold by Intel</u> to its customers comply with the requirements for all regulatory certifications defined in the following table. <u>It is the Intel customer's responsibility to ensure that their final server system configurations are tested and certified to meet the regulatory requirements for the countries to which they plan to ship and or deploy server systems into.</u>

	Intel® Server Board D50TNP1SB Family "Tenessee Pass"	Intel® Server System D50TNP Family "Tenessee Pass"	Notes Intel Project Code Name
	L3 Board	L6/L9 System	Product integration level
	D50TNP	FC2H	Product family identified on certification
Regulatory Certification			
RCM DoC Australia & New Zealand	✓	✓	
CB Certification & Report (International - report to include all CB country national deviations)	✓	✓	
China CCC Certification	0		Out of CCC Scope (PSU > 1300 W)
CU Certification (Russia/Belarus/Kazakhstan)	0	✓	
Europe CE Declaration of Conformity	✓	✓	
FCC Part 15 Emissions Verification (USA & Canada)	✓	✓	
Germany GS Certification	0	✓	
India BIS Certification	0	✓	Only L9 at MSL
International Compliance – CISPR32 & CISPR24	✓	✓	
Japan VCCI Certification	0	✓	
Korea KC Certification	✓	✓	
Mexico Certification	0	✓	
NRTL Certification (USA&Canada)	√	✓	
South Africa Certification	0	✓	
Taiwan BSMI Certification	✓	✓	
Ukraine Certification	0	✓	

Table Key

Not Tested / Not Certified

Tested / Certified – Limited OEM SKUs only

Testing / Certification (Planned) (Date)

Tested / Certified ✓

¹ An L9 system configuration is a power-on ready server system with NO operating system installed. An L6 system configuration requires additional components to be installed to make it power-on ready. L3 are component building block options that require integration into a chassis to create a functional server system.

EU Directive 2019/424 (Lot 9)

Beginning on March 1, 2020, an additional component of the European Union (EU) regulatory CE marking scheme, identified as EU Directive 2019/424 (Lot 9), will go into effect. After this date, all new server systems shipped into or deployed within the EU must meet the full CE marking requirements including those defined by the additional EU Lot 9 regulations.

Intel has verified that all L3, L6, and L9 server products² **as configured and sold by Intel** to its customers comply with the full CE regulatory requirements for the given product type, including those defined by EU Lot 9. It is the Intel customer's responsibility to ensure that their final server system configurations are SPEC SERT* tested and meet the new CE regulatory requirements.

Visit the following website for additional EU Directive 2019/424 (Lot9) information:

https://eur-lex.europa.eu/legal-content/EN/TXT/?uri=CELEX:32019R0424

In compliance with the EU Directive 2019/424 (Lot 9) materials efficiency requirements, Intel makes available all necessary product collaterals as identified below:

• System Disassembly Instructions

- Intel® Server D50TNP Family Integration and Service Guide
- See Section 1.2 for link to document.

Product Specifications

- Intel® Server D50TNP Family Technical Product Specification (TPS)
- See Section 1.2 for link to document.

System BIOS/Firmware and Security Updates – Intel® Server D50TNP Family

- System Update Package (SUP) UEFI only
- See Section 1.2.

Intel® Solid State Drive (SSD) Secure Data Deletion and Firmware Updates

- o Note: for system configurations that may be configured with an Intel SSD
- The Intel® Memory and Storage Tool (Intel® MAS)
- https://downloadcenter.intel.com/product/35125/Memory-and-Storage

Intel® RAID Controller Firmware Updates and other support collaterals

- Note: for system configurations that may be configured with an Intel® RAID Controller
- https://www.intel.com/content/www/us/en/support/products/43732/server-products/raidproducts.html

² An L9 system configuration is a power-on ready server system with NO operating system installed. An L6 system configuration requires additional components to be installed to make it power-on ready. L3 are component building block options that require integration into a chassis to create a functional server system. 200

EU Lot9 Support Summary - FC2H - Intel® Server System D50TNP

DISCLAIMER – The information contained within the following tables is for reference purposes only and is intended to provide Intel customers with a template to report product information necessary for (EU) 2019/424 (Lot 9) server conformity assessment. The information provided herein does not represent any final shipping server system test results, and customer's actual test results for shipping server configurations may differ from the information provided. Use of this information is at the sole risk of the user, and Intel assumes no responsibility for customers server system level regulation compliance to EU 2019/424 (Lot 9).

Product Information					
Product Type	Server				
Manufacturer Name	Intel Corporation				
Registered trade name and address	Intel 2200 Mission Colle	ge Blvd, Sa	nta Clara,	CA 95054	I-1594, USA
Product model number and model numbers for low end performance and high-end performance configure if applicable	FC2H				
Year Of Manufacture	2021				
PSU efficiency at 10%, 20%, 50%, and 100% of rated output power	1600W PSU AXX160 2100W PSU AXX210	_	-		
Tated output power	Model	10%	20%	50%	100%
	AXX1600TCRPS	90%	94%	96%	91%
	AXX2100TCRPS	90%	94%	96%	91%
PSU factor at 50% of rated load level	AXX1600TCRPS	0.95			
	AXX2100TCRPS	0.95			
PSU Rated Power Output	AXX1600TCRPS	1600 Wa	atts		
(Server Only)	AXX2100TCRPS	CRPS 2100 Watts			
Idle state power (Server only) (Watts)	Refer to the following table				
List of all components for additional idle power allowances (server only)	Refer to the following table				
Maximum power (Server only)	Refer to the following	ng table			
Declared operating condition class	ASHRAE Class A2-Continuous Operation 10 °C to 35 °C with the maximum rate of change not to exceed 10 °C per hour				
Idle State Power (watts) at the higher boundary temp (Server Only)	Refer to the following table				
the active state efficiency and the performance in active state of the server (server only)	Refer to the following table				
Information on the secure data deletion functionality	Refer to the following table				
for blade server, a list of recommended combinations with compatible chassis (Server only)	Not Applicable				
If Product Model Is Part Of A Server Product Family, a list of all model configurations that are represented by the model shall be supplied (Server only)	Not Applicable				

ig.	2 CPUs High-end Config.	2 CPUs Low-end Config.	Configuration			
	FC2HFAC16W3	FC2HFAC16W3	Model	Chassis		
	1	1	Quantity	No do /MD		
	D50TNP1SB	D50TNP1SB	Model	Node/MB		
	2	2	Quantity	CPU		
3P	Intel® Xeon® Platinum 8358P	Intel® Xeon® Gold 5317 Processor	Model	CPU		
	16	16	Quantity			
	128	8	Capacity per DIMM (GB)	Memory		
	2,048	128	Total Memory Amount (GB)		Details	
	2	2	SSD Quantity	SSD		
	3	3	Quantity	PSU		
	FCXX2100CRPS	AXX1600TCRPS	Model	F30		
R config	BIOS: SE5C620.86B.01.01.0002(00. BMC: 2.80.d8286de7 FRU SDR: 0.35 CYP FSC SDR of sheet - Mitac_rev0.51.xlsm	BIOS: SE5C620.86B.01.01.0002(0020P24) BMC: 2.80.d8286de7 FRU SDR: 0.35 CYP FSC SDR config sheet - Mitac_rev0.51.xlsm	FW			
	38.0	38.0	P Base			
	159.8	92.0	CPU	Additional		
	10.0	10.0	Power Supply	Additional	Measured	
	10.0	10.0	evices	Storage De	and Calculated	
	183.60	22.32	Memory	Additional	Server	
	0.0	0.0	Additional I/O Device (10Gx		Allowance	
	22.83	13.14		Perf _{cpu}		
	401.4	172.3	dle power allowances (W) 172.3			
	215.5	171.1	Idle power tested (W) Per node		Limits/ Results	
	9.5	9.5	Minimum Eff _{ACTIVE}			
	40.0	31.0				
	251.5	185.9	Idle Power at Higher Temp. (per Node) at 35 °C		Other test	
					result	
	sheet - Mitac_rev0.51.xlsm 38.0 159.8 10.0 10.0 183.60 0.0 22.83 401.4 215.5 9.5 40.0	sheet - Mitac_rev0.51.xlsm 38.0 92.0 10.0 10.0 22.32 0.0 13.14 172.3 171.1 9.5 31.0	P Base Additional CPU Additional Power Supply Storage Devices Additional Memory Additional I/O Device (10Gx 15W/2Port on MB) Perf _{cpu} Idle power allowances (W) Idle power tested (W) Per node Minimum Eff _{ACTIVE} Eff _{ACTIVE} tested Idle Power at Higher Temp. (per		and Calculated Server Allowance Limits/ Results Other test	

Other Information:

Chemical Declaration

- Neodymium Not Applicable. (No HDD offered by Intel)
- Cobalt Not Applicable. (No BBUs. Coin battery is out of scope)

Appendix K. Glossary

Term	Definition
ACPI	Advanced Configuration and Power Interface
Intel® AES-NI	Intel® Advanced Encryption Standard New Instructions. See also AES.
Al	Artificial Intelligence
ASHRAE	American Society of Heating, Refrigerating, and Air Conditioning Engineers
Intel® AVX-512	Intel® Advanced Vector Extensions 512
BBS	BIOS Boot Selection
вмс	Baseboard Management Controller
BIOS	Basic Input/Output System
Intel® CBnT	Converged Intel® Boot Guard and Trusted Execution Technology (Intel® TXT)
CFM	Cubic Feet per Minute
CLST	Closed Loop System Throttling
CMOS	Complementary Metal-Oxide-Semiconductor
DDR4	Double Data Rate 4
DIMM	Dual In-line Memory Module
DMI	Direct Media Interface
DPC	DIMMs per Channel
DR	Dual Rank
ECC	Error Correction Code
EFI	Extensible Firmware Interface
EMP	Ethernet Management Port
EPS	External Product Specification
FRB	Fault Resilient Boot
FRU	Field Replaceable Unit
GPIO	General Purpose Input/Output
GUI	Graphical User Interface
HPC	High-Performance Computing
Intel® HT Technology	Intel® Hyper-Threading Technology
IDE	Integrated Drive Electronics
IMC	Integrated Memory Controller
IIO	Integrated Input/Output
iPC	Intel Product Code
ІРМВ	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
ISTA	International Safe Transit Association
KVM	Keyboard, Video, and Mouse
KVM-r	Keyboard/Video/Mouse Redirection
JRE	Java Runtime Environment
LFM	Linear Feet per Minute (airflow measurement)
LLC	Last Level Cache
LRDIMM	Load Reduced DIMM
LSB	Least Significant Bit
Intel® ME	Intel® Management Engine
MKTME	Multi-Key Total Memory Encryption

Term	Definition
MLE	Measured Launch Environment
ММ	Memory Mode
MRC	Memory Reference Code
MSB	Most Significant Bit
NAT	Network Address Translation
NIC	Network Interface Controller
NMI	Non-maskable Interrupt
NTB	Non-Transparent Bridge
OCuLink	Optical Copper Link
ОЕМ	Original Equipment Manufacturer
OR	Oct (8) Rank
ОТР	Over Temperature Protection
OVP	Over-voltage Protection
PCH	Peripheral Controller Hub
PCI	Peripheral Component Interconnect
PCIe*	Peripheral Component Interconnect Express*
PDB	Power Distribution Board
PECI	Platform Environment Control Interface
Intel® PFR	Intel® Platform Firmware Resilience
РНМ	Processor Heat sink Module
PMBus*	Power Management Bus
PMem	Persistent Memory
POST	Power-on self-test
PSU	Power Supply Unit
PWM	Pulse Width Modulation
QR	Quad (8) Rank
RAID	Redundant Array of Independent Disks
RAS	Reliability, Availability, and Serviceability
RCiEP	Root Complex Integrated Endpoint
RDIMM	Registered DIMM
RMCP	Remote Management Control Protocol
ROC	RAID On Chip
SATA	Serial Advanced Technology Attachment
SEL	System Event Log
SDR	Sensor Data Record
SmaRT	Smart Ride Through
Intel® SGX	Intel® Software Guard Extensions
SMBus*	System Management Bus
SMM	Server Management Mode
SMP	Server Management Processor
SMS	System Management Software
SMTP	Simple Mail Transfer Protocol
SNMP	Simple Network Management Protocol
SOL	Serial-Over-LAN
SR	Single Rank
SSD	Solid State Device

Term	Definition
SSL	Secure Sockets Layer
TCG	Trusted Computing Group
TDP	Thermal Design Power
TIM	Thermal Interface Material
Intel® TME	Intel® Total Memory Encryption
TPM	Trusted Platform Module
Intel® TXT	Intel® Trusted Execution Technology
UEFI	Unified Extensible Firmware Interface
Intel® UPI	Intel® Ultra Path Interconnect
Intel® VMD	Intel® Volume Management Device
VNNI	Vector Neural Network Instructions
Intel® VROC	Intel® Virtual RAID on CPU
VSB	Voltage Standby
Intel® VT-d	Intel® Virtualization Technology for Directed I/O
Intel® VT-x	Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture