

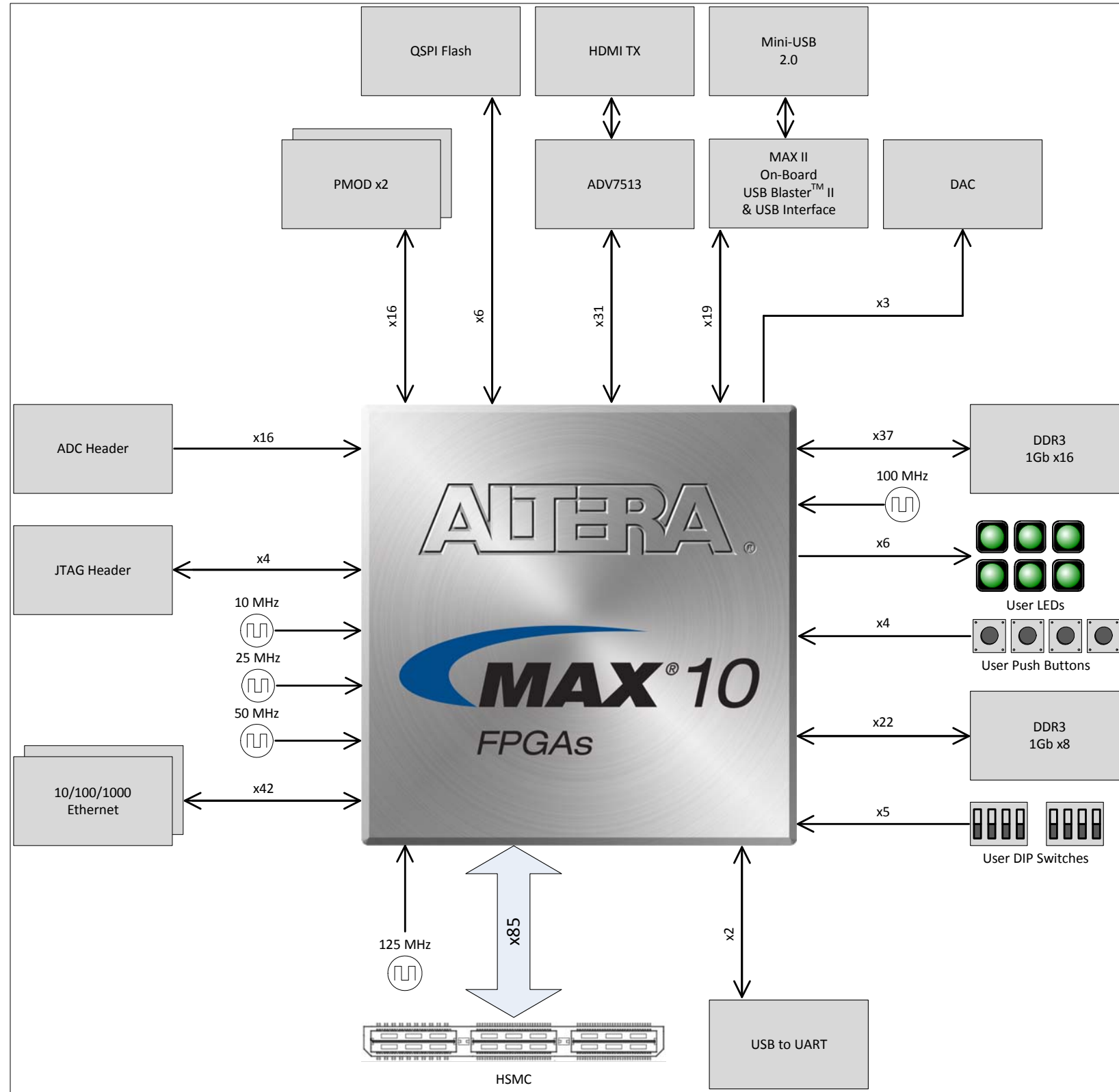
**NOTES:**

1. Project Drawing Numbers:
- Raw PCB 100-0321401- C1
  - Gerber Files 110-0321401- C1
  - PCB Design Files 120-0321401- C1
  - Assembly Drawing 130-0321401- C1
  - Fab Drawing 140-0321401- C1
  - Schematic Drawing 150-0321401- C1
  - PCB Film 160-0321401- C1
  - Bill of Materials 170-0321401- C1
  - Schematic Design Files 180-0321401- C1
  - Functional Specification 210-0321401- C1
  - PCB Layout Guidelines 220-0321401- C1
  - Assembly Rework 320-0321401- C1

# Pre-Release Schematic

## DO NOT COPY

### MAX 10 Development Kit Board



REV	DATE	PAGES	DESCRIPTION
A	20 May 2014	All	INITIAL REVISION A RELEASE
B	2 Sep 2014	6	Swap pin AA21 with AA22
		7	Swap pin D5 with C3, and E8 with C6
		23	Change resistor value, R44 to 10K, R106 to 1K, R99 to 2K, R100 to 1K, R104 to 1K
		24	SW3 pin number change
		26 27	Add DNI capacitor, C70 and C166
	24 Sep 2014	1	Add functional diagram
		24	Change resistor value, R169 to 10K
	26 Jan 2015	All	Update notes for release version
C	17 Mar 2015	6	Swap pin F20 with D19, F21 with C20, F18 with A21, and E19 with B20
		10	Add resistors R303, R304, R305, R306, R80, R81, C355
		13	Add resistors R307
		9 & 23	Update the net name from BOOT_SEL to CONFIG_SEL
		22 & 23	Update the net name from MAX10_BYPASSn to VTAP_BYPASSn

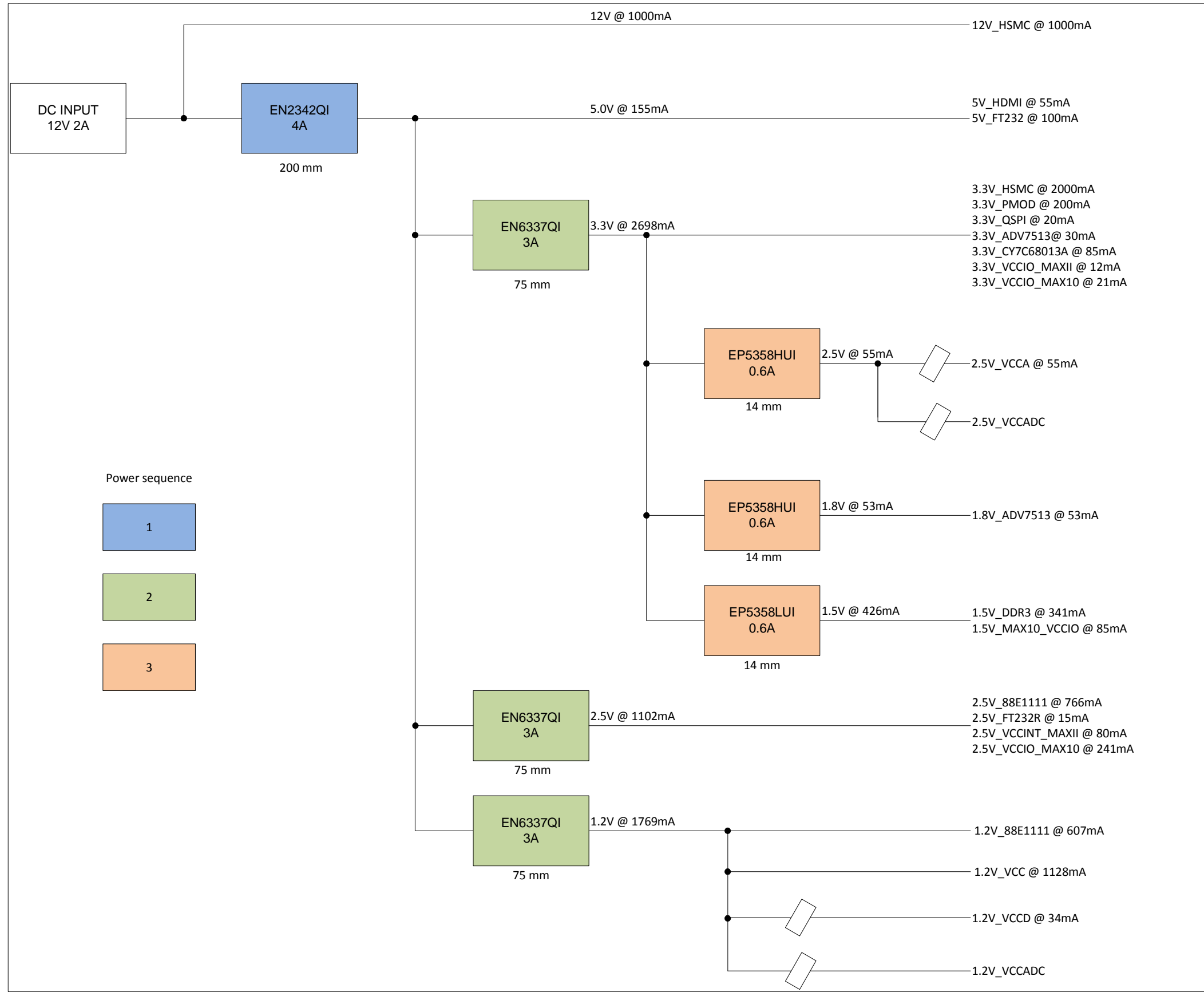
PAGE	DESCRIPTION	PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Rev. History	30	MAX10 Ground
2	Power Tree	31	Decoupling
3	Clock Tree		
4	MAX10 Bank 1 & 2		
5	MAX10 Bank 3 & 4		
6	MAX10 Bank 5 & 6		
7	MAX10 Bank 7 & 8		
8	MAX10 Configuration		
9	MAX10 Clocks		
10	PLL		
11	ADC Filter		
12	DAC		
13	DDR3 SDRAM		
14	QSPI FLASH		
15	HSMC Port		
16	GPIO, PMOD		
17	HDMI		
18	10/100/1000 Ethernet A		
19	10/100/1000 Ethernet B		
20	USB to UART		
21	On-Board USB Blaster II-1		
22	On-Board USB Blaster II-2		
23	LED, User IO, Connector		
24	Power1		
25	Power2		
26	Power3		
27	Power4		
28	Power5		
29	MAX10 Power		



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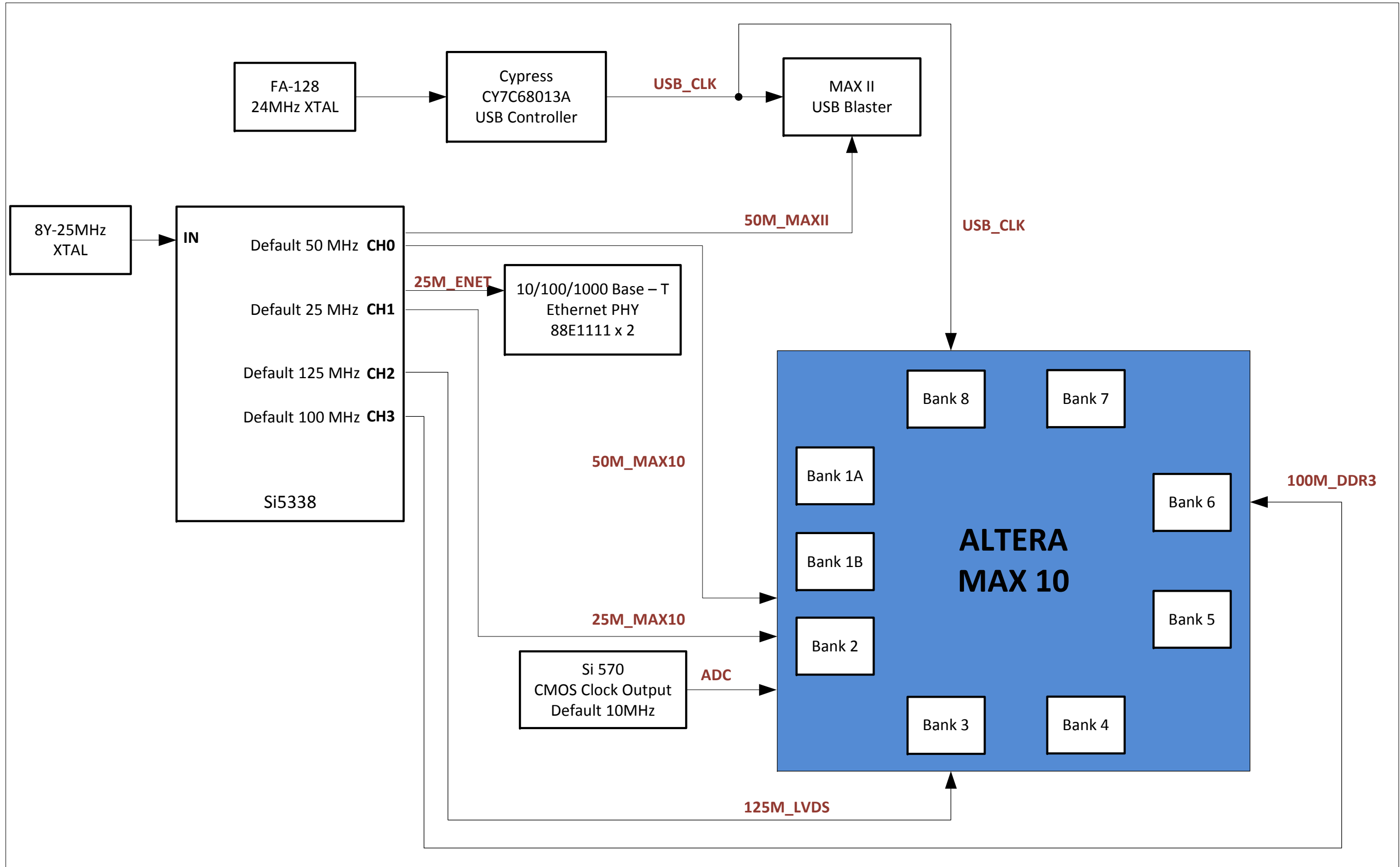
Title MAX10 FPGA Development Kit (6XX-44292R)		
Size B	Document Number 150-0321401-C1	Rev C1
Date: Wednesday, March 18, 2015	Sheet 1	of 31

# Power Tree



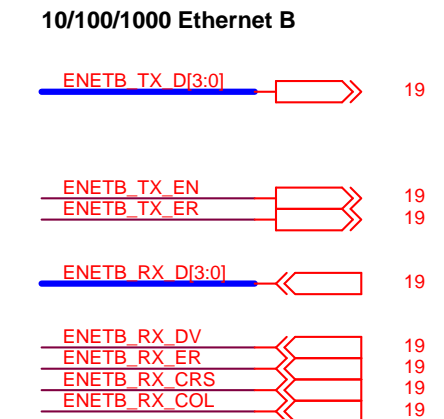
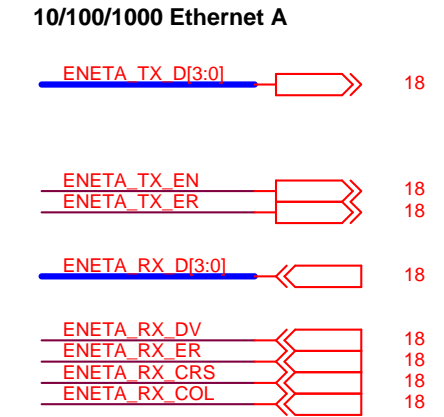
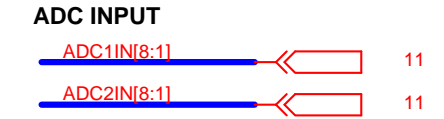
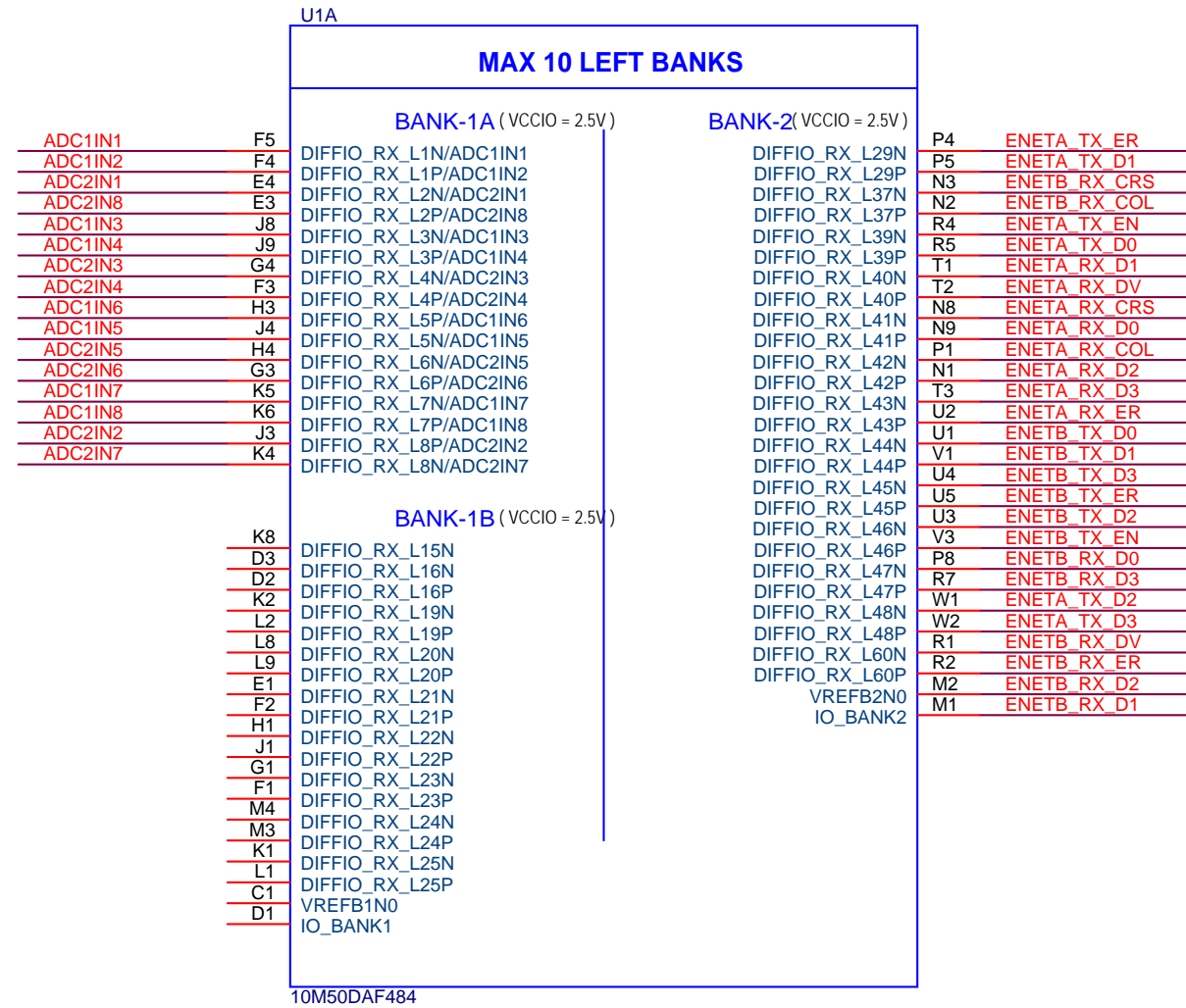
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Date: Wednesday, March 18, 2015	Sheet 2	of 31

# Clock Tree

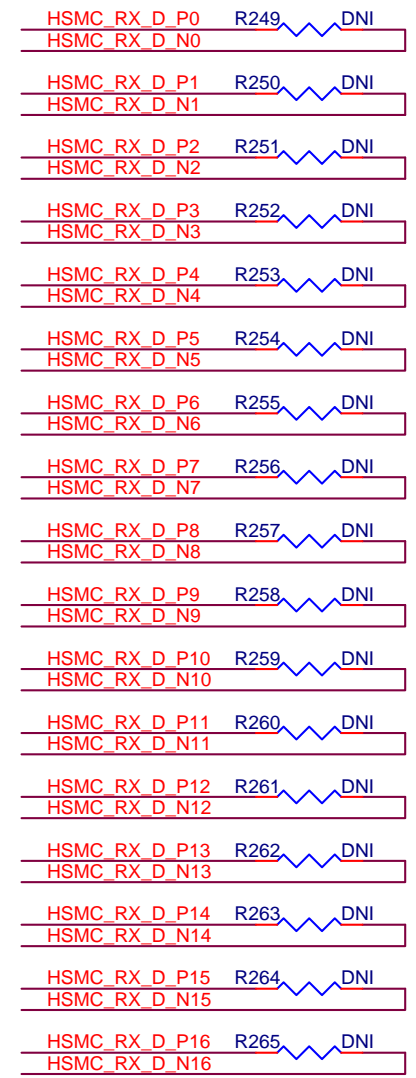
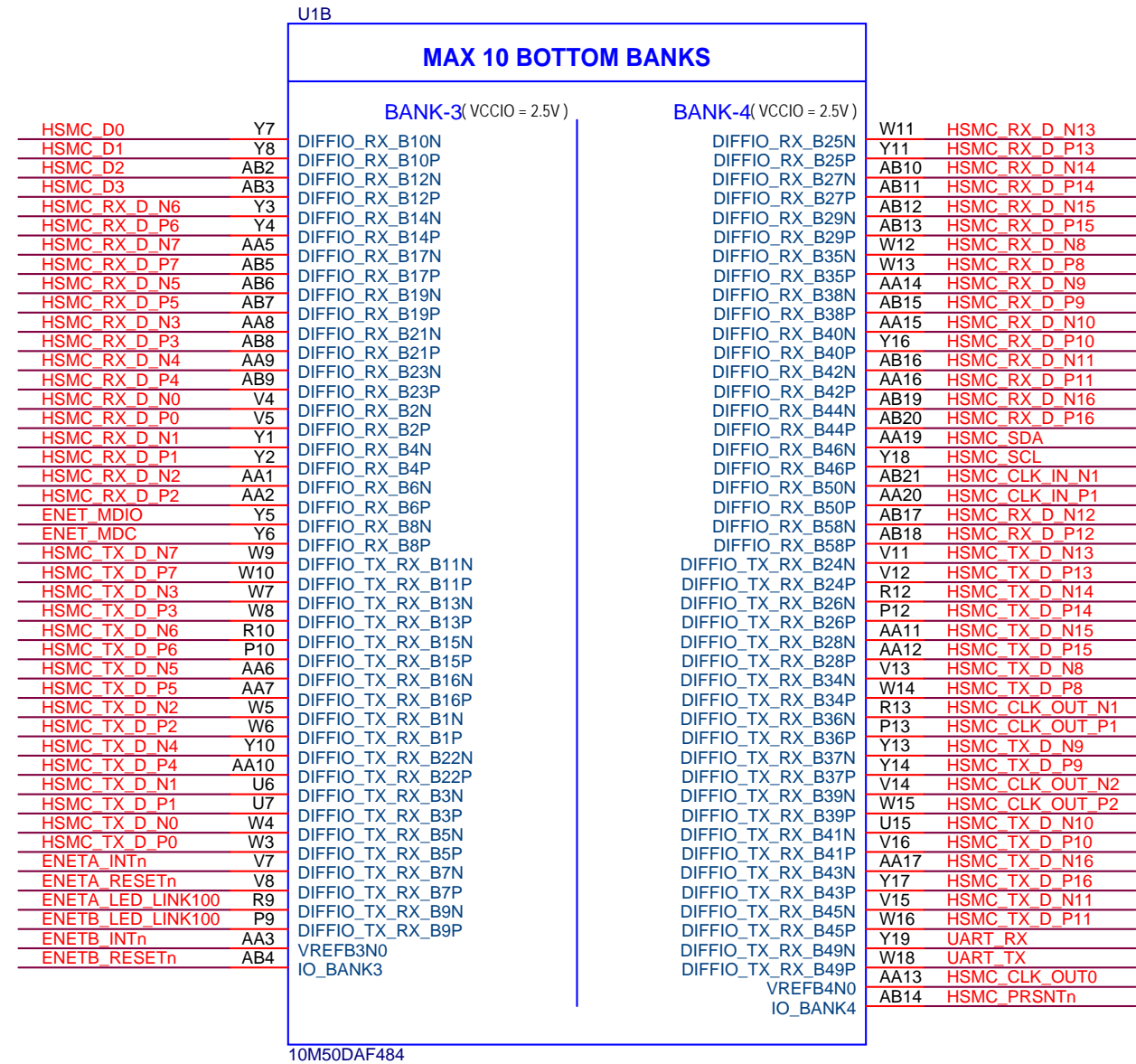


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Title MAX10 FPGA Development Kit (6XX-44292R)		
Size B	Document Number 150-0321401-C1	Rev C1
Date:	Wednesday, March 18, 2015	Sheet 3 of 31

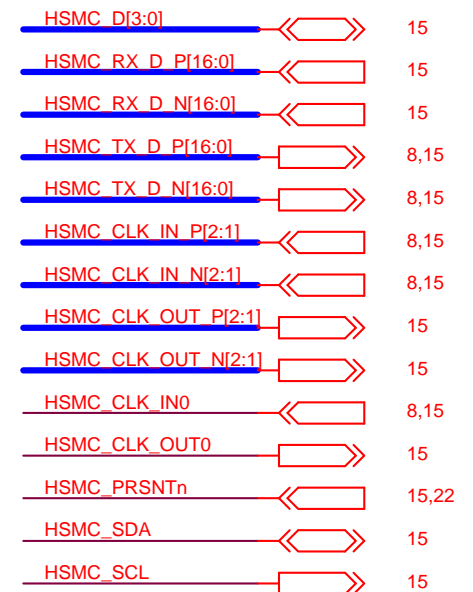
# MAX10 Bank 1 & 2



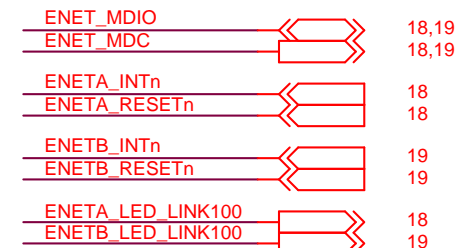
# MAX10 Bank 3 & 4



## HSMC Interface



## Ethernet



## UART

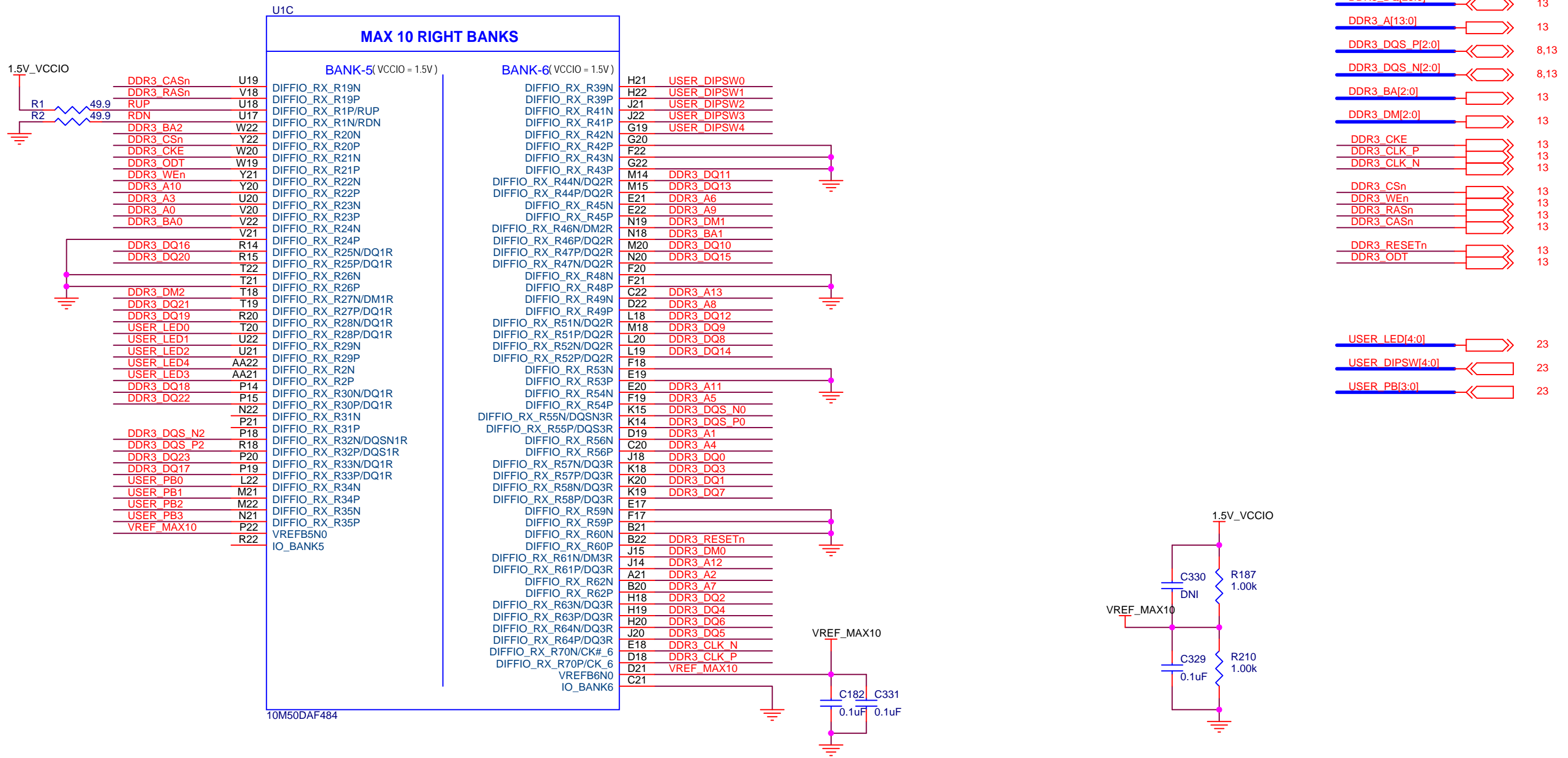


Notes:  
R249-R265 are 100 ohm termination resistors for LVDS RX.



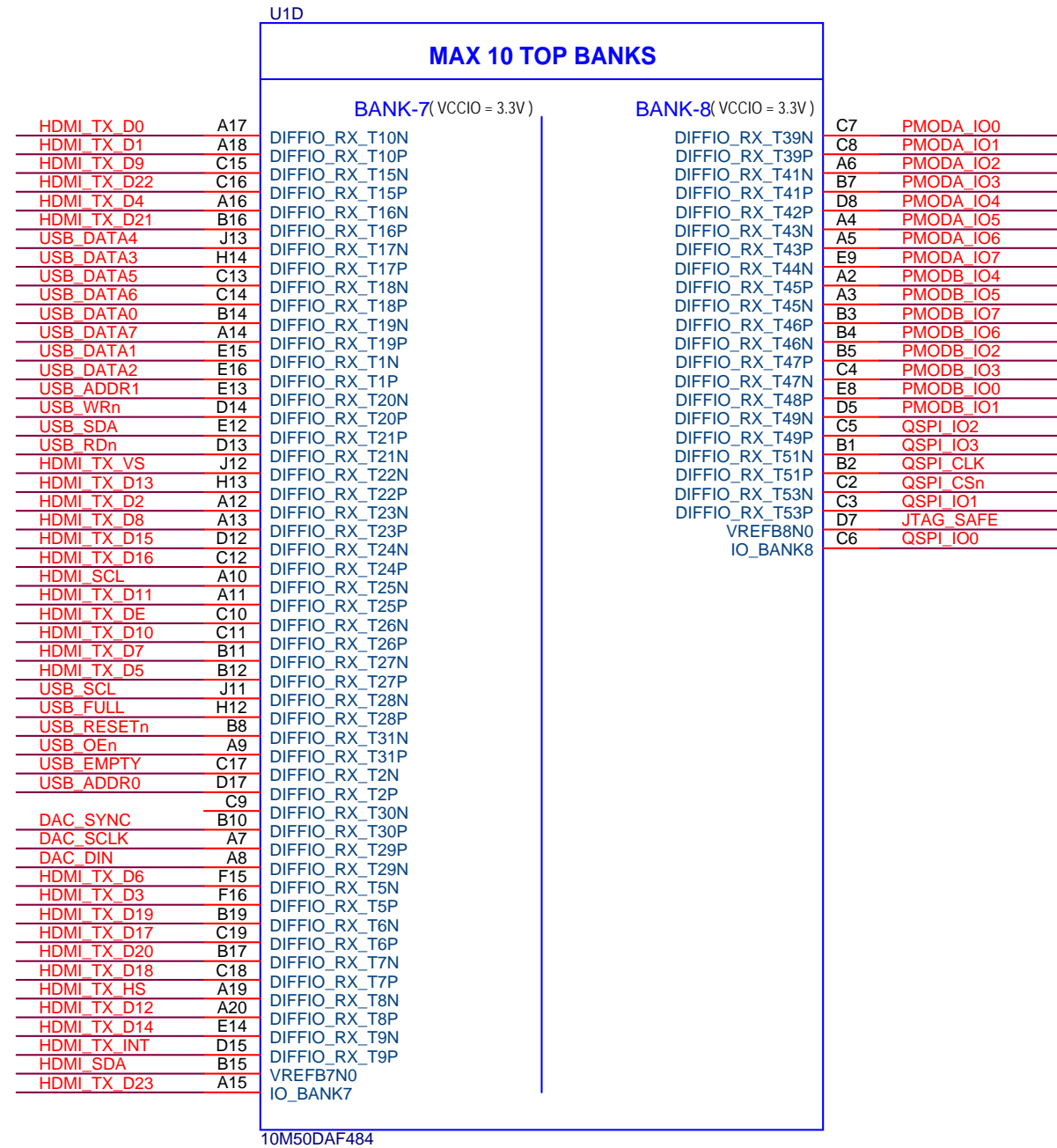
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Date:	Thursday, March 19, 2015	Sheet 5 of 31

# MAX10 Bank 5 & 6

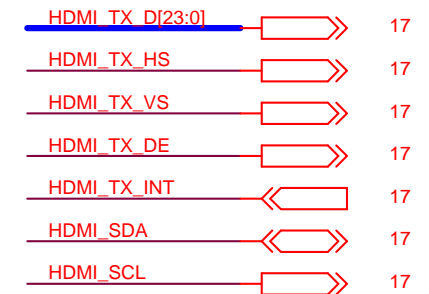


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Size B	Document Number 150-0321401-C1	Rev C1
Date: Friday, March 20, 2015	Sheet 6	of 31

# MAX10 Bank 7 & 8



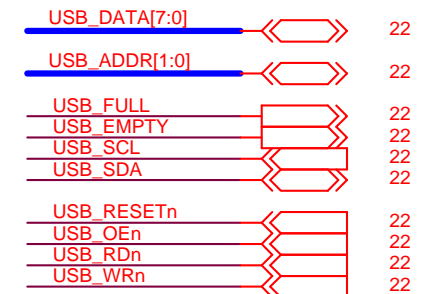
## HDMI TX



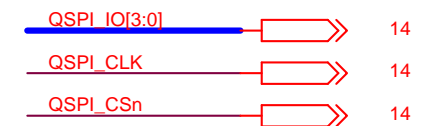
## PMOD



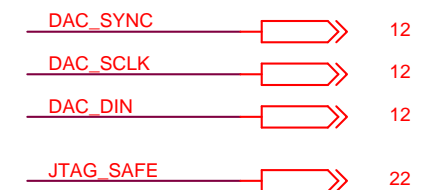
## MAX10 USB INTERFACE



## QSPI FLASH

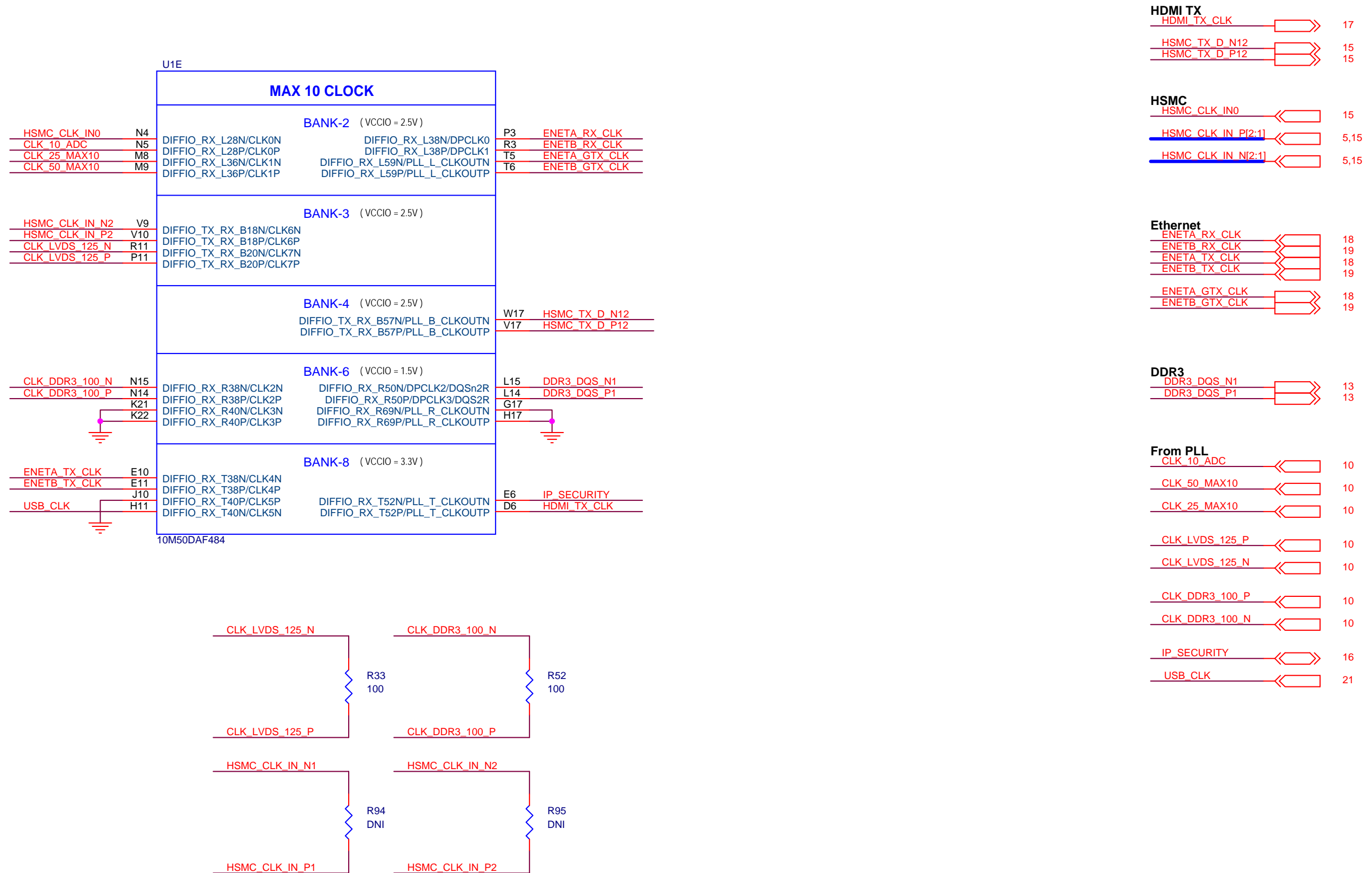


## DAC



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Size B	Document Number 150-0321401-C1	Rev C1
Date:	Wednesday, March 18, 2015	Sheet 7 of 31

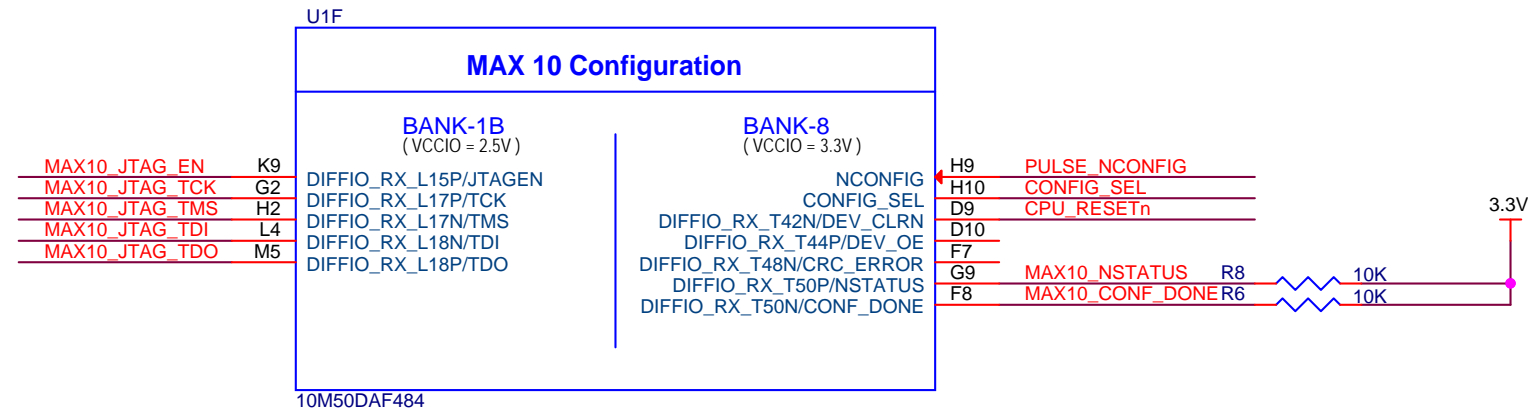
# MAX10 Clock



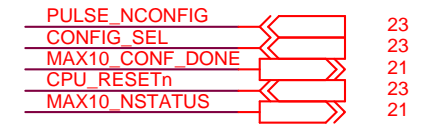
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Size B	Document Number 150-0321401-C1	Rev C1
Date: Thursday, March 19, 2015	Sheet 8	of 31



# MAX10 Configuration



## Configuration

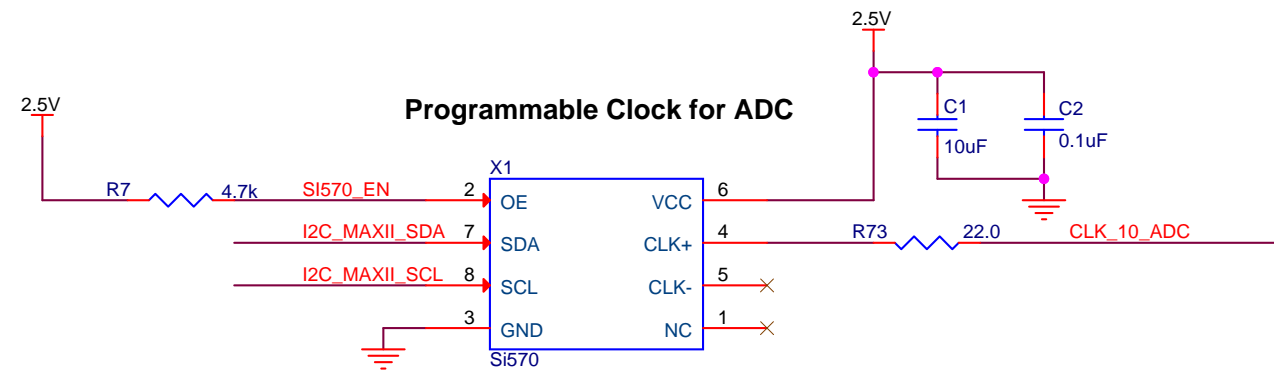


## JTAG



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Size B	Document Number 150-0321401-C1	Rev C1
Date: Wednesday, March 18, 2015	Sheet 9	of 31

# PLL



**Programmable Clock for ADC**

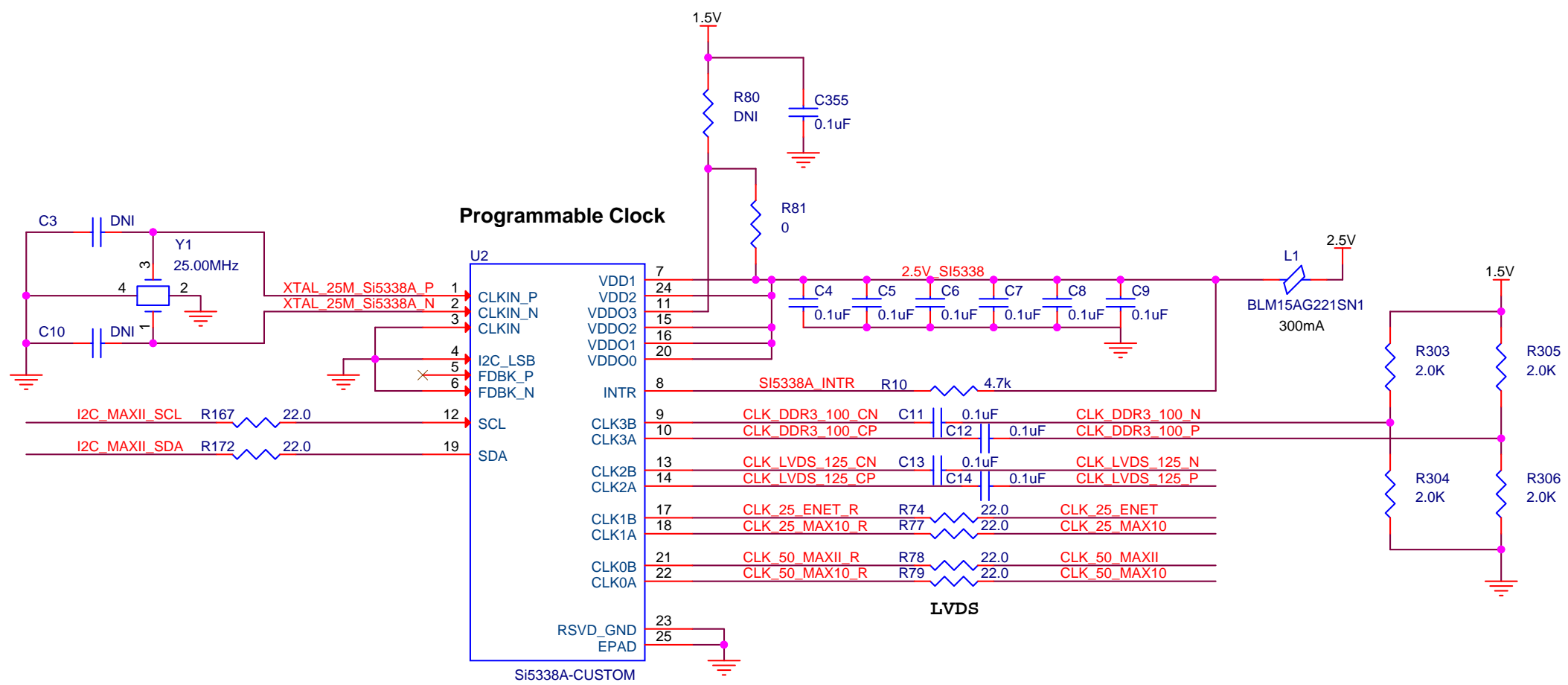
Notes:  
Use Clock Control GUI  
Default 10MHz  
I2C Address 55 HEX

### Clock control

I2C_MAXII_SCL	22,28
I2C_MAXII_SDA	22,28
SI5338A_INTR	22
SI570_EN	22

### Clock out

CLK_10_ADC	8
CLK_50_MAX10	8
CLK_50_MAXII	21
CLK_25_ENET	18,19
CLK_25_MAX10	8
CLK_LVDS_125_P	8
CLK_LVDS_125_N	8
CLK_DDR3_100_P	8
CLK_DDR3_100_N	8



**Programmable Clock**

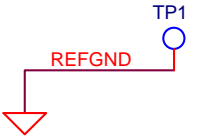
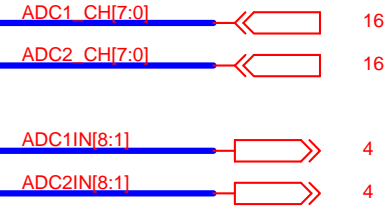
Notes:  
SI5338 Programmable Oscillator Use Clock Control GUI  
(Defaults 50MHz, 25MHz, 125MHz, 100MHz)  
I2C Address 70 HEX

### LVDS

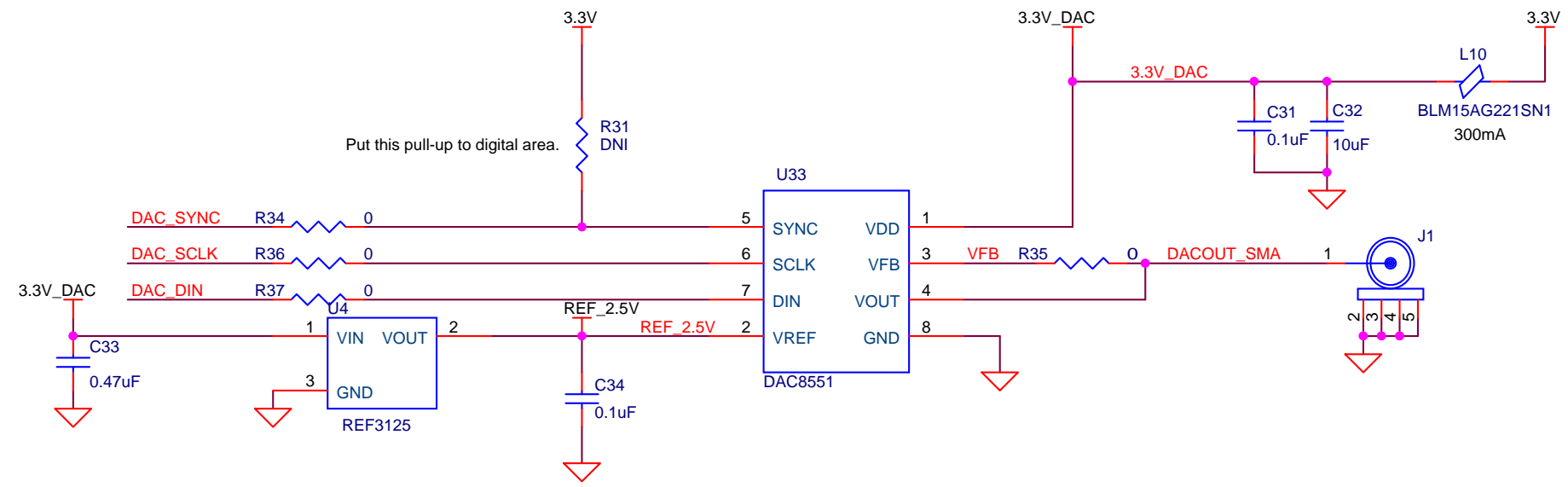
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Size B	Document Number 150-0321401-C1	Rev C1
Date:	Wednesday, March 18, 2015	Sheet 10 of 31

# ADC Filter

Notes:  
Put the 1pF capacitors close to each MAX10 analog pin.



# DAC



- Notes:
1. Put 0.1uF capacitor close to VREF pin.
  2. Everything related to this DAC should be connected to analog ground.
  3. For better DC accuracy, VFB should be connected to VOUT at loadpoints.
  4. Thermal pad should be connected to GND.

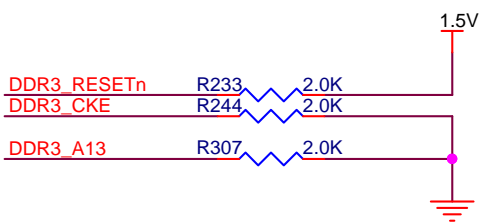
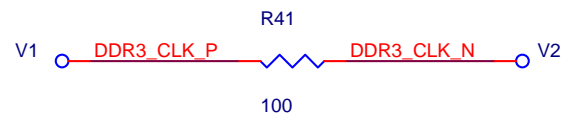
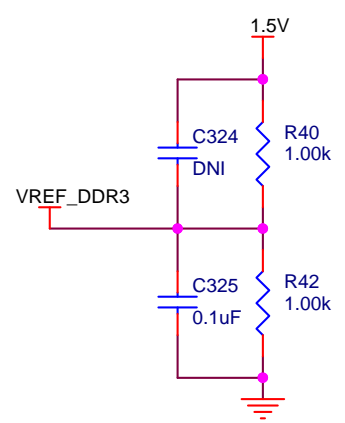
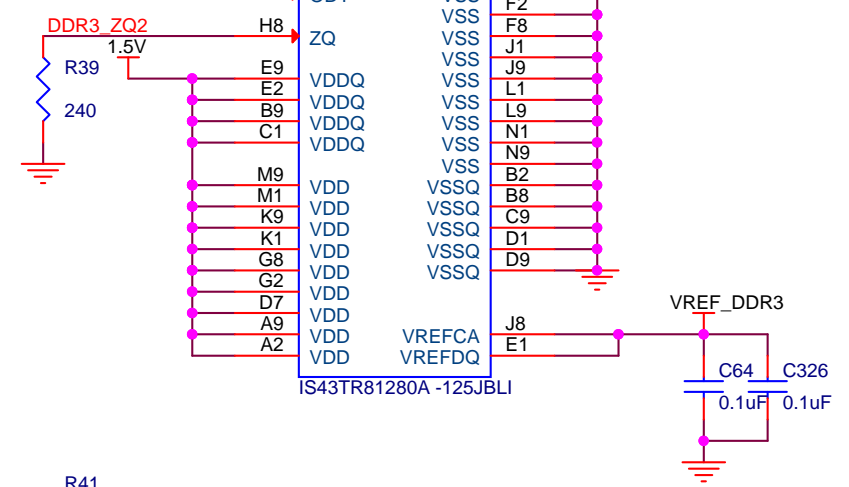
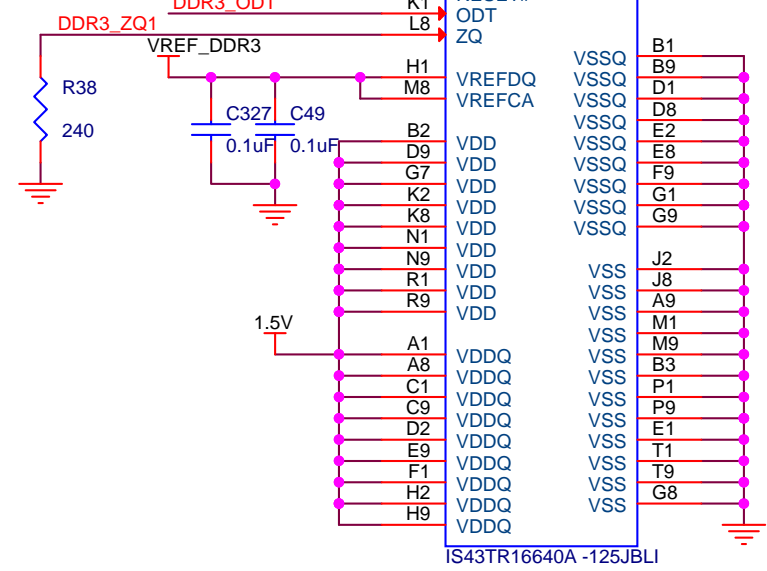
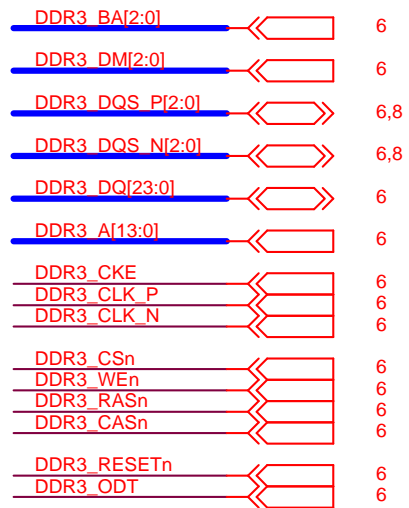
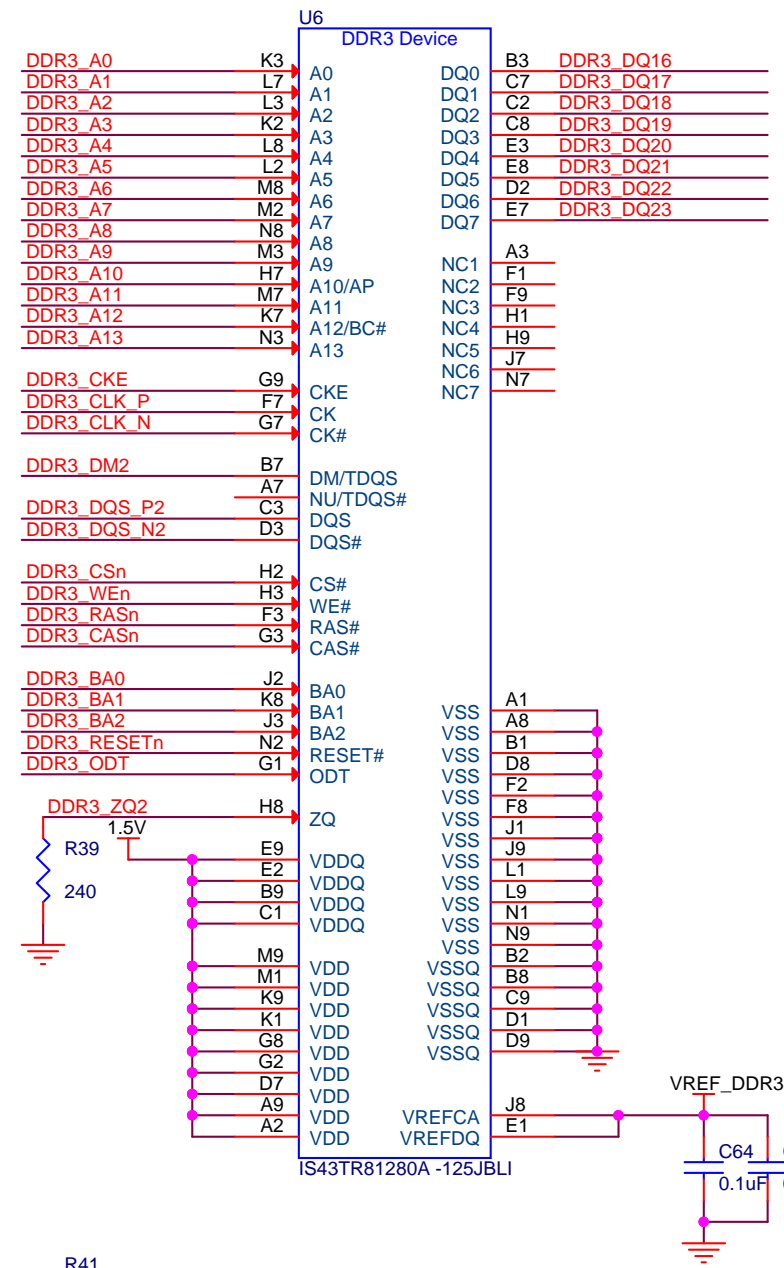
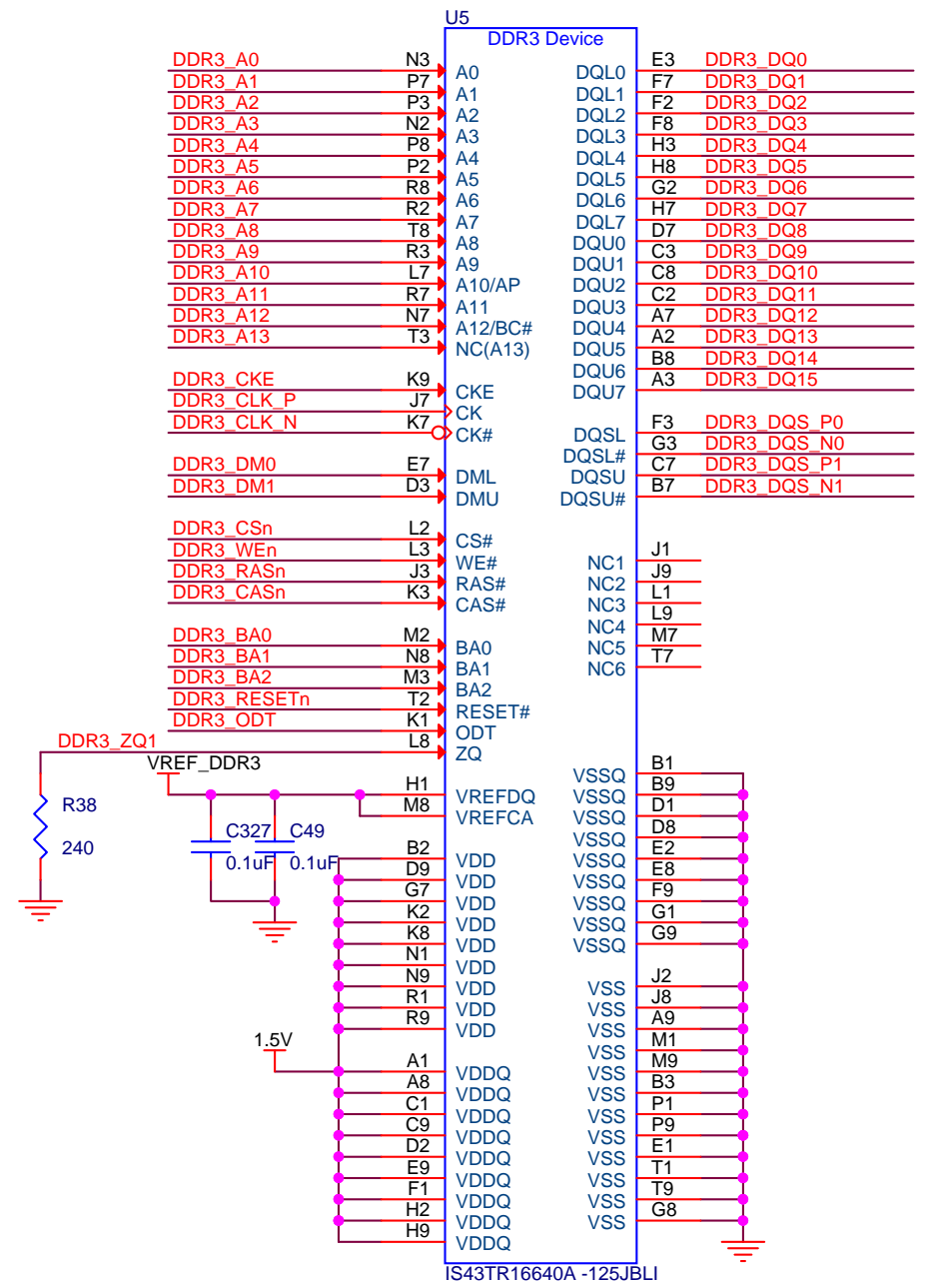
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Title MAX10 FPGA Development Kit (6XX-44292R)		
Size B	Document Number 150-0321401-C1	Rev C1
Date:	Wednesday, March 18, 2015	Sheet 12 of 31

# DDR3 SDRAM

DDR3 SDRAM A (64Mx16)

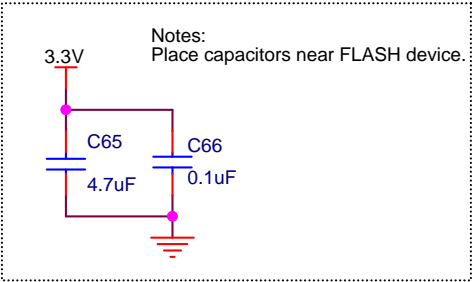
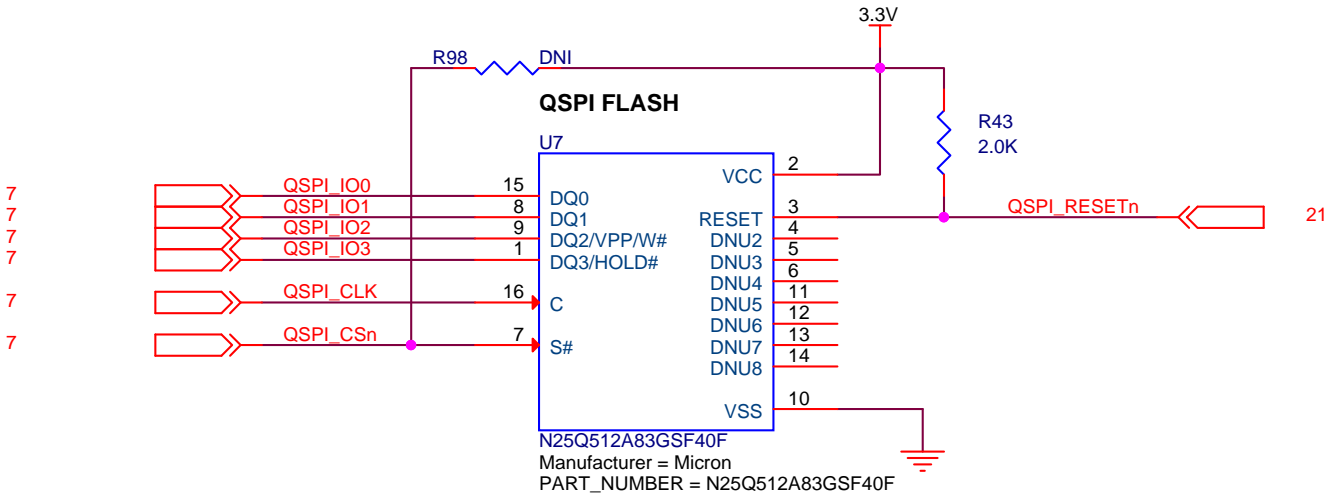
DDR3 SDRAM B (128Mx8)

FPGA Interface



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Size B	Document Number: 150-0321401-C1	Rev C1
Date: Wednesday, March 18, 2015	Sheet 13 of 31	

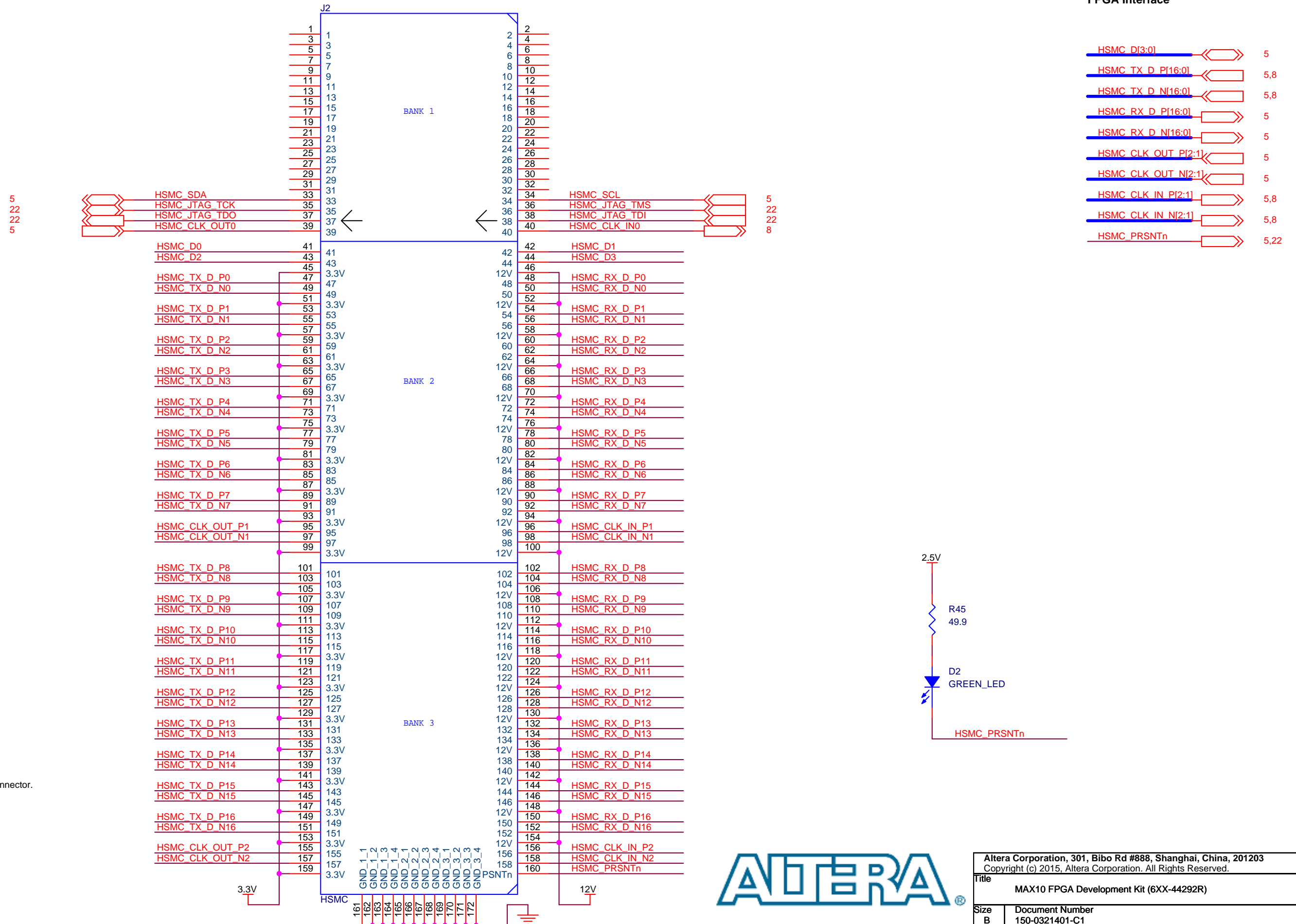
# QSPI FLASH



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Size B	Document Number 150-0321401-C1	Rev C1
Date: Wednesday, March 18, 2015	Sheet 14	of 31

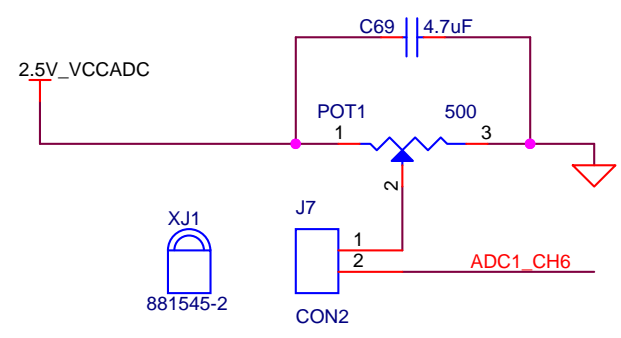
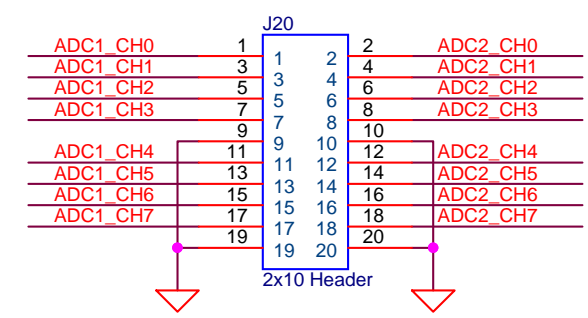
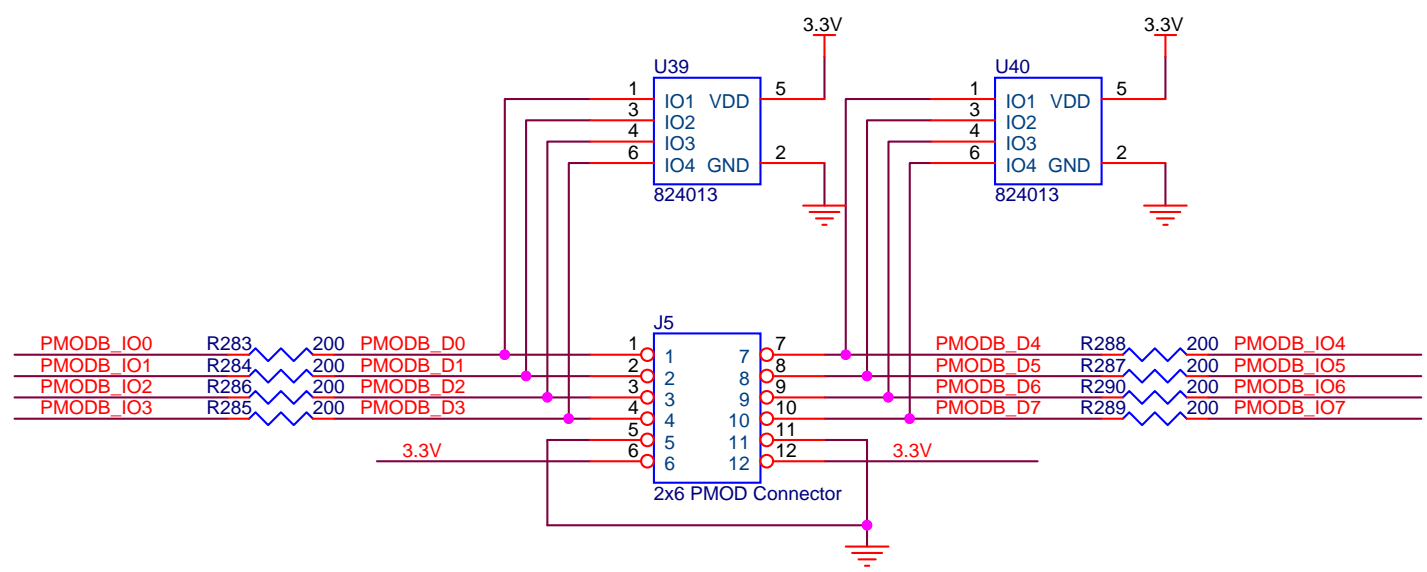
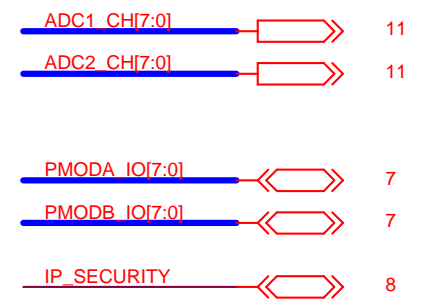
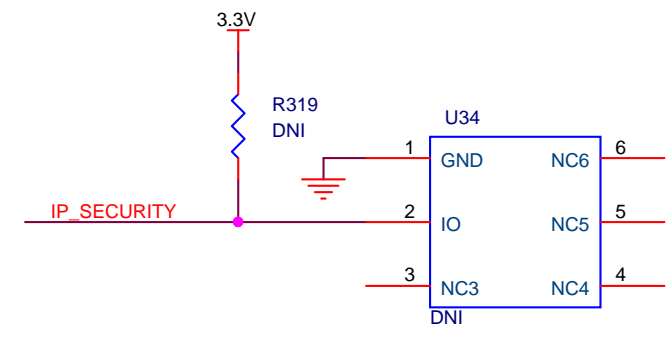
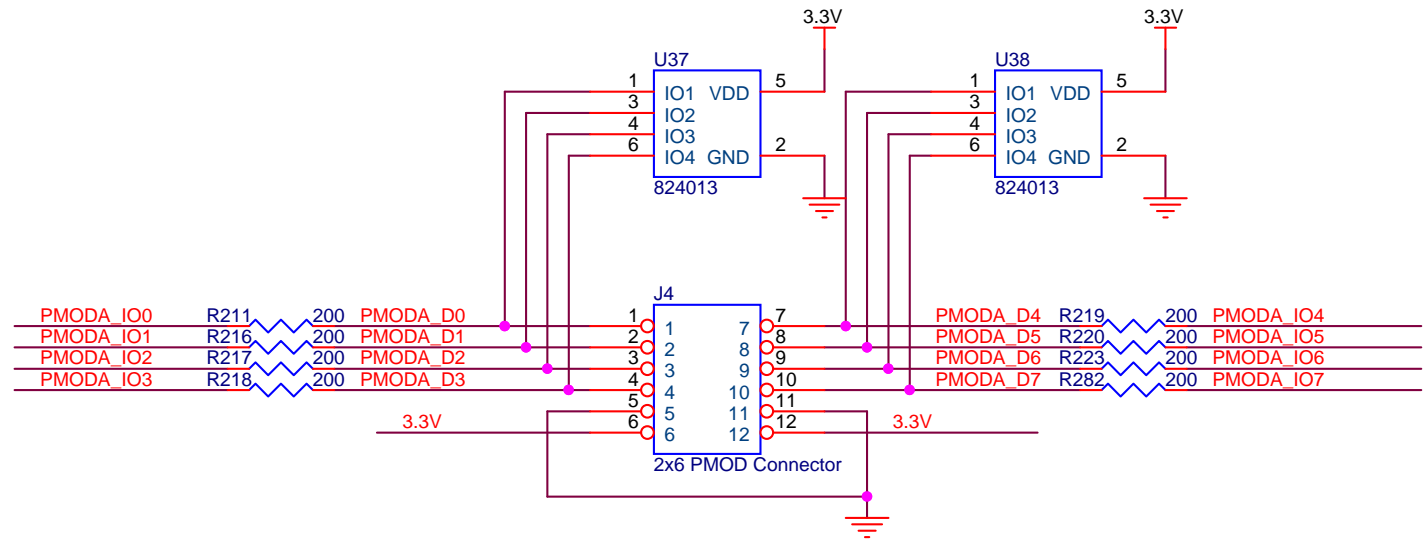
# HSMC Port

## FPGA Interface



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Size B	Document Number: 150-0321401-C1	Rev C1
Date: Thursday, March 19, 2015	Sheet 15 of 31	

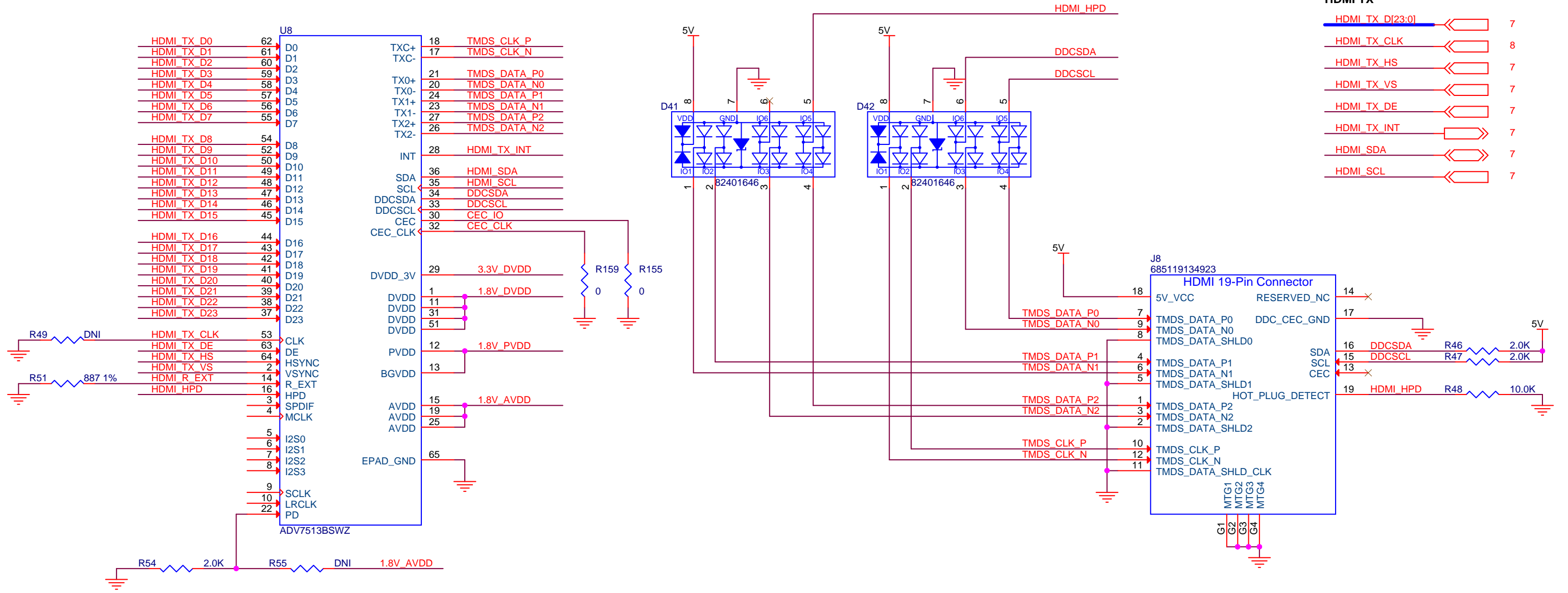
# GPIO, PMOD



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Date: Wednesday, March 18, 2015		Sheet 16 of 31

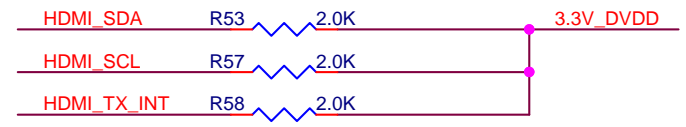
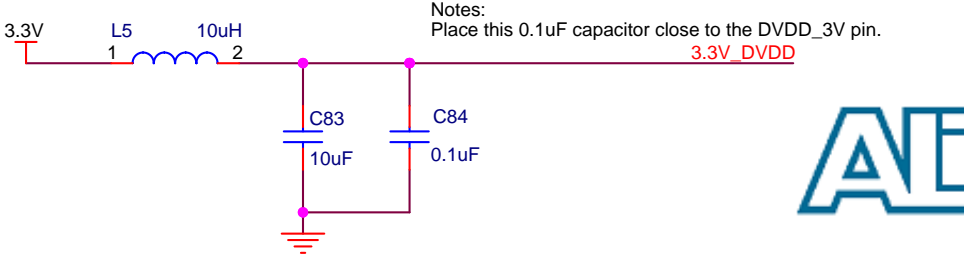
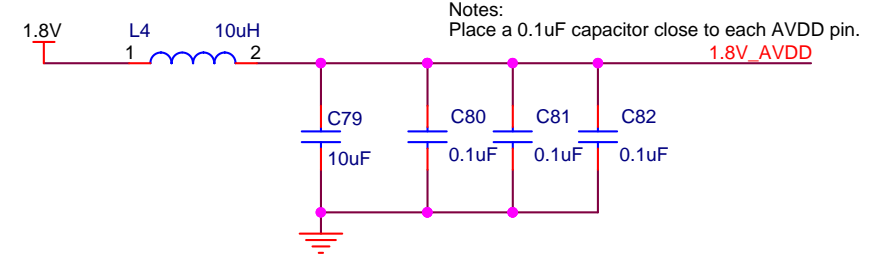
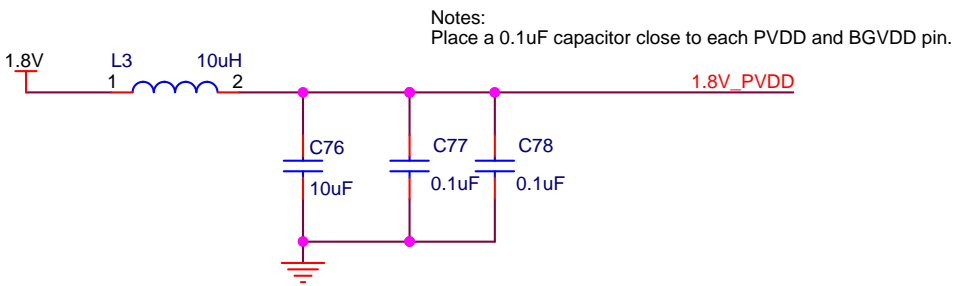
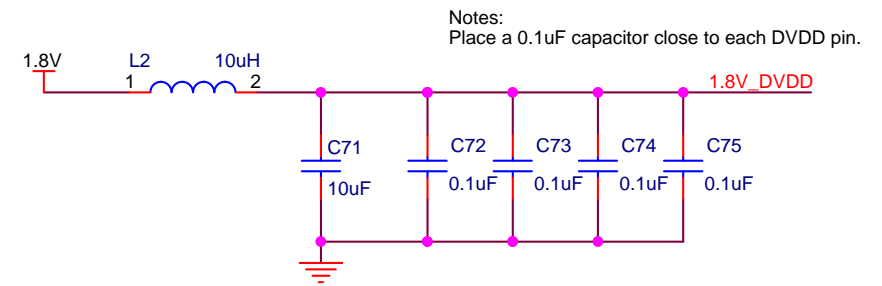


# HDMI



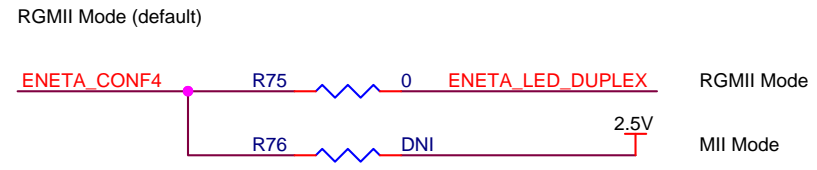
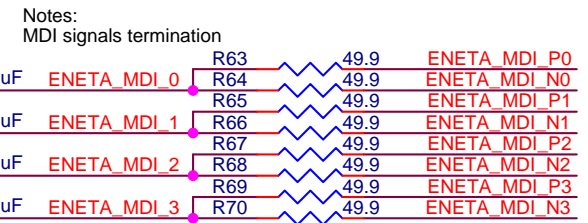
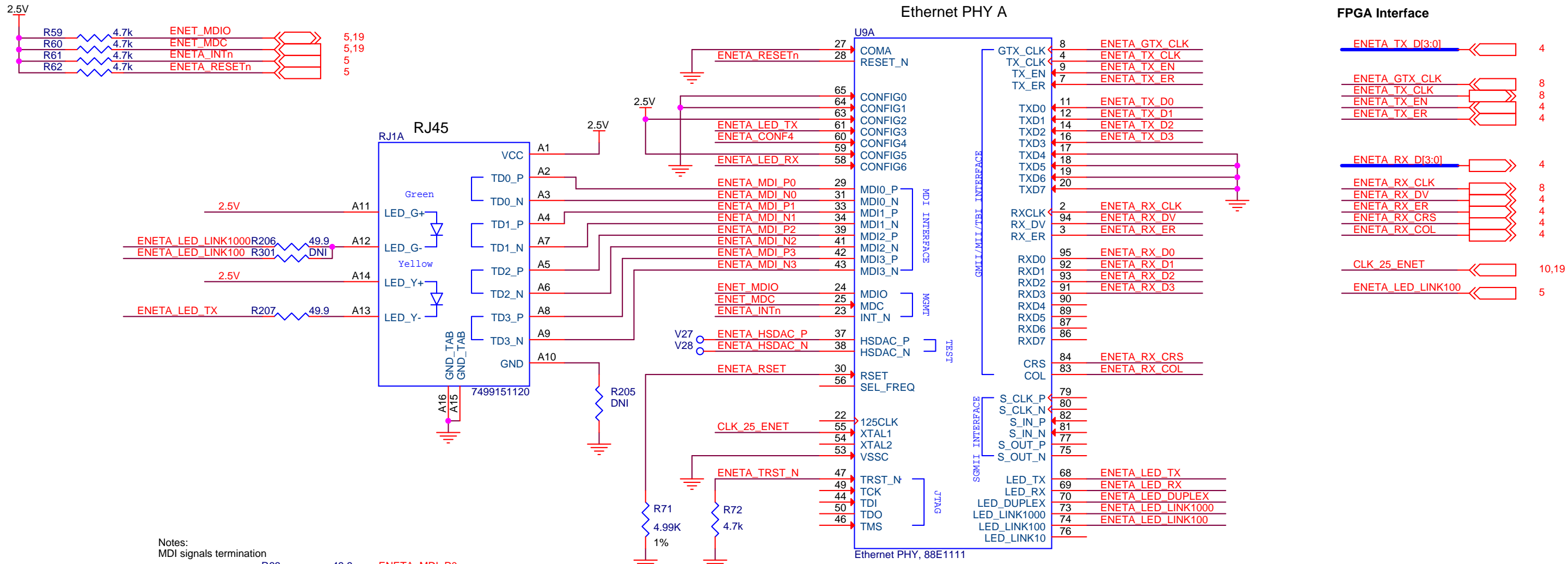
**HDMI TX**

HDMI_TX_D[23:0]	7
HDMI_TX_CLK	8
HDMI_TX_HS	7
HDMI_TX_VS	7
HDMI_TX_DE	7
HDMI_TX_INT	7
HDMI_SDA	7
HDMI_SCL	7

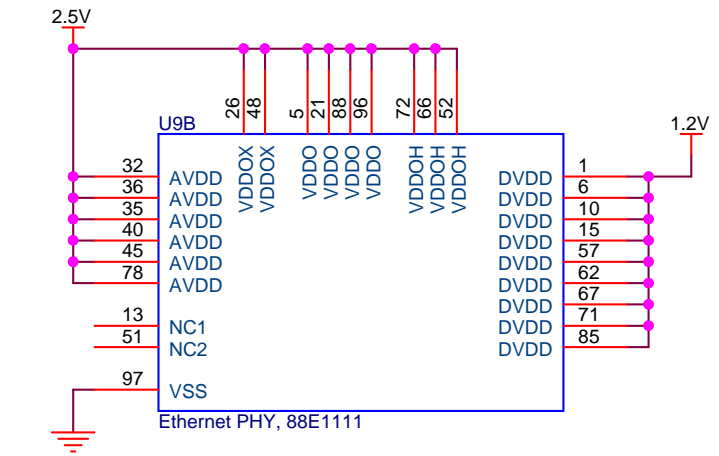
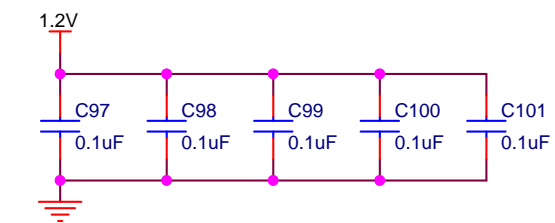
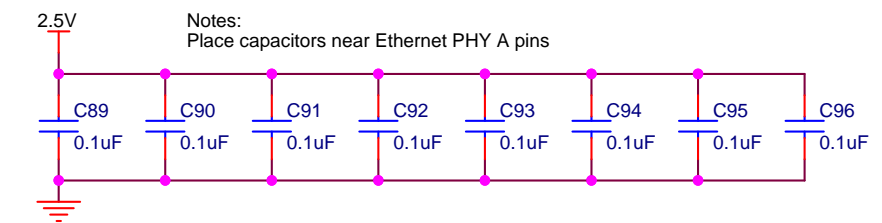


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Size B	Document Number 150-0321401-C1	Rev C1
Date: Wednesday, March 18, 2015	Sheet 17	of 31

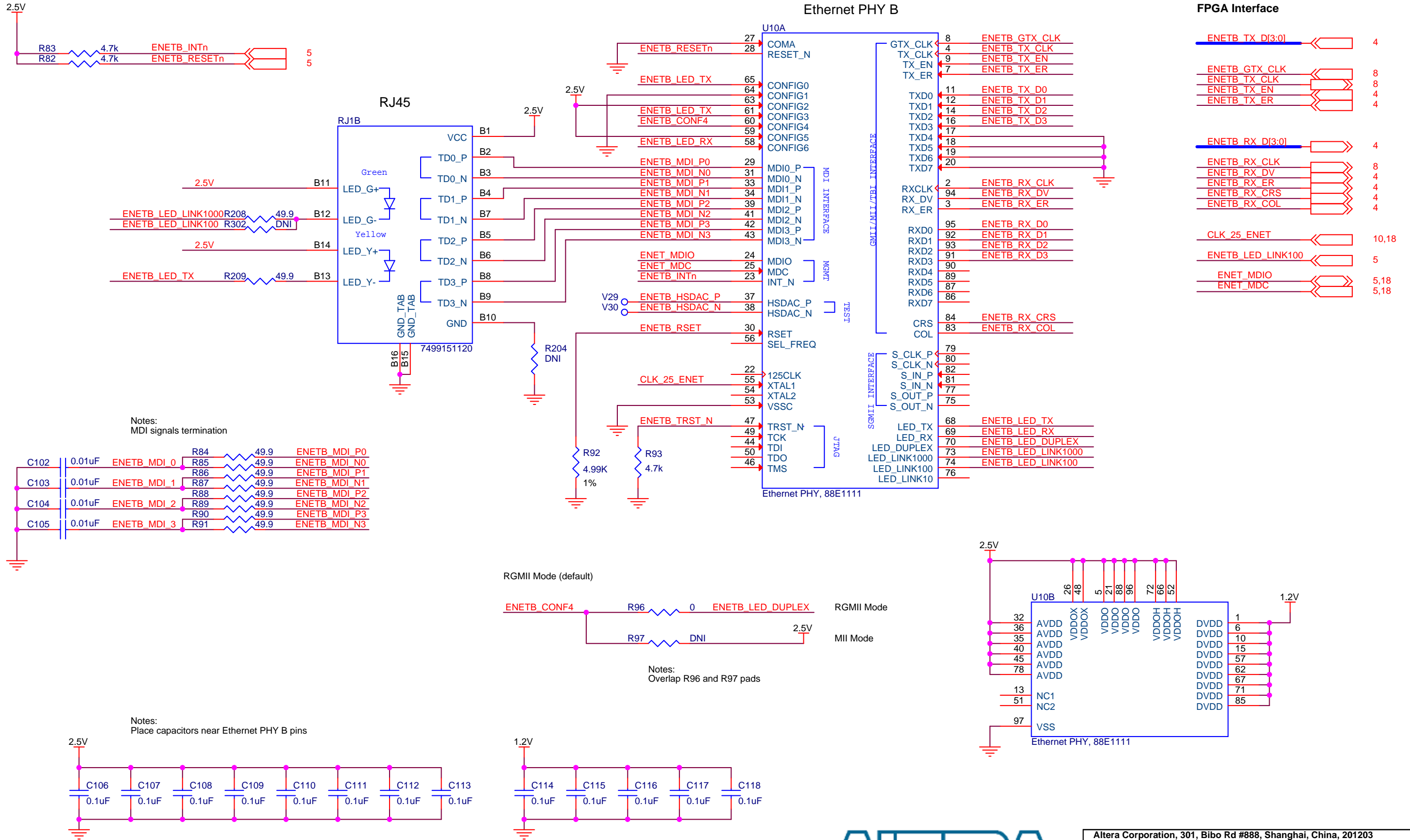
# 10/100/1000 Ethernet A



Notes:  
Overlap R75 and R76 pads

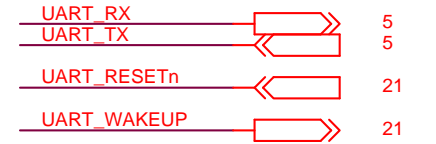


# 10/100/1000 Ethernet B

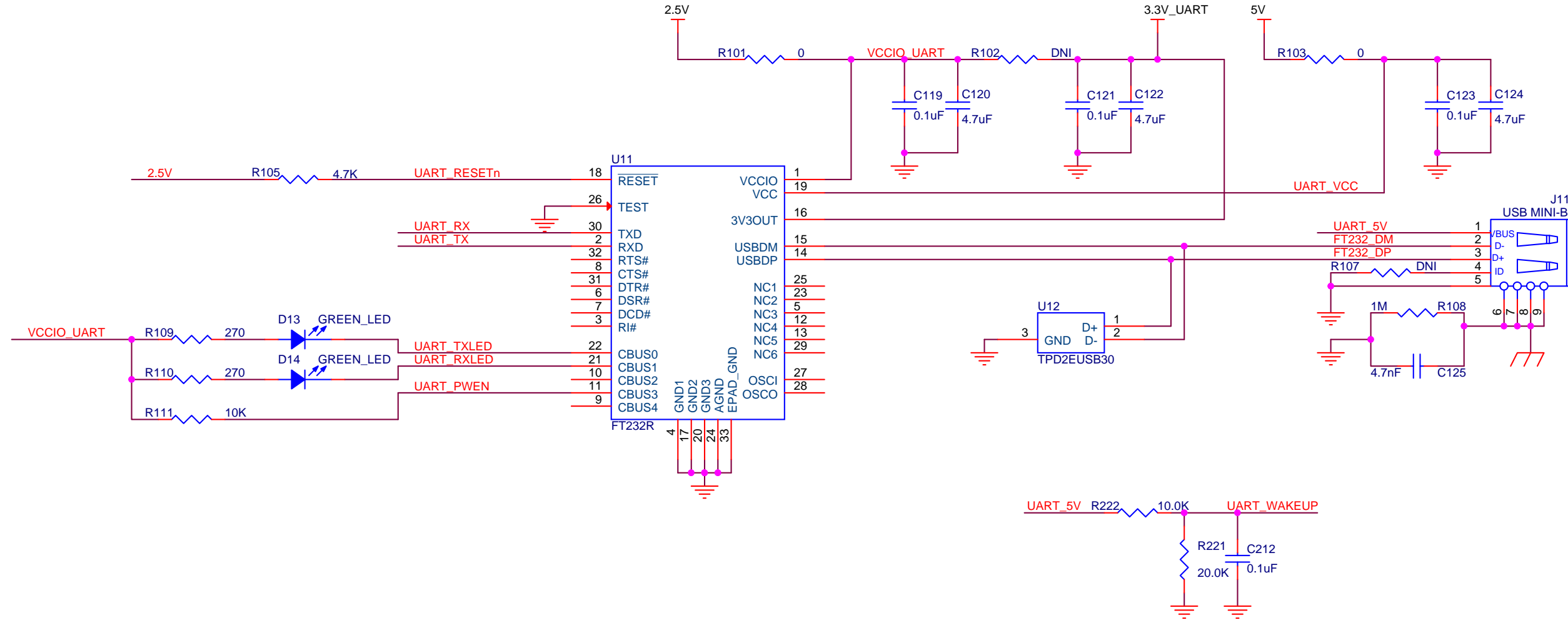


# USB to UART

## FPGA Interface

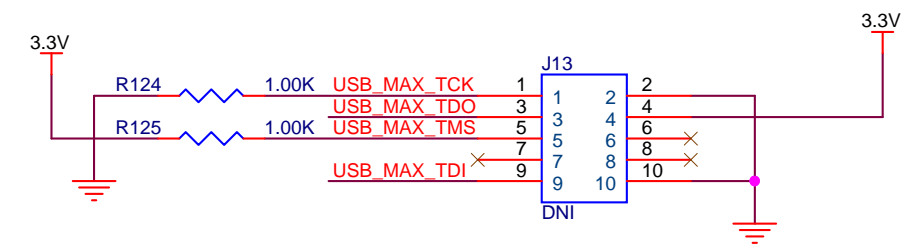
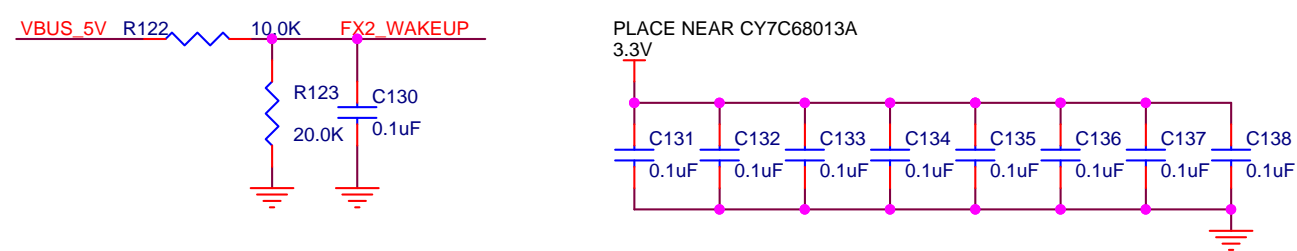
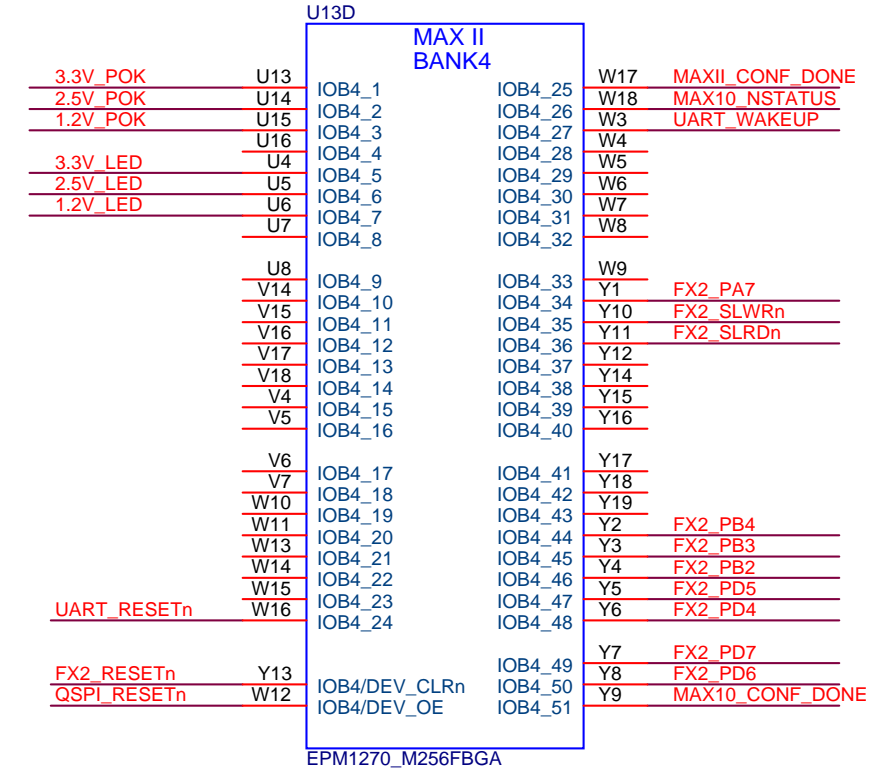
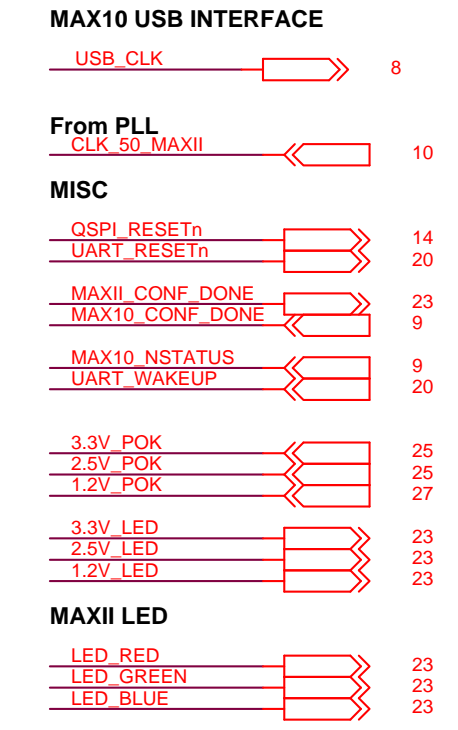
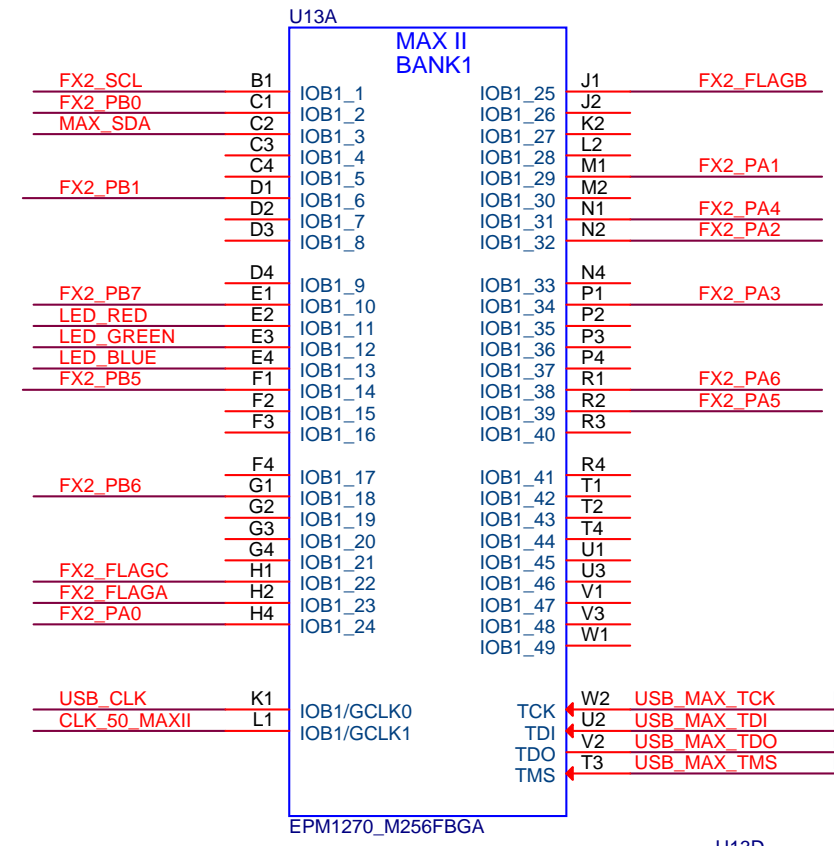
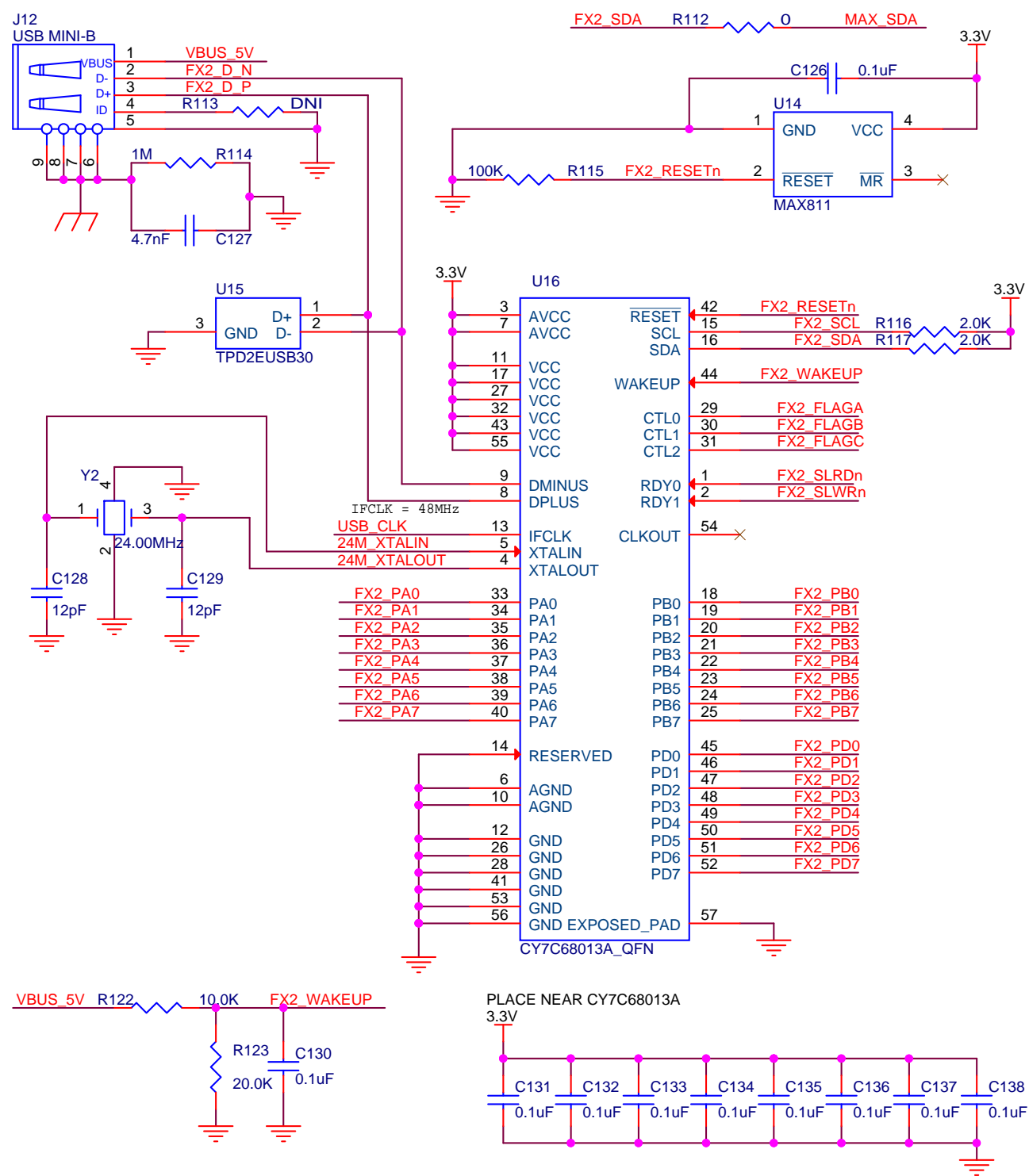


2.5V default 3.3V optional



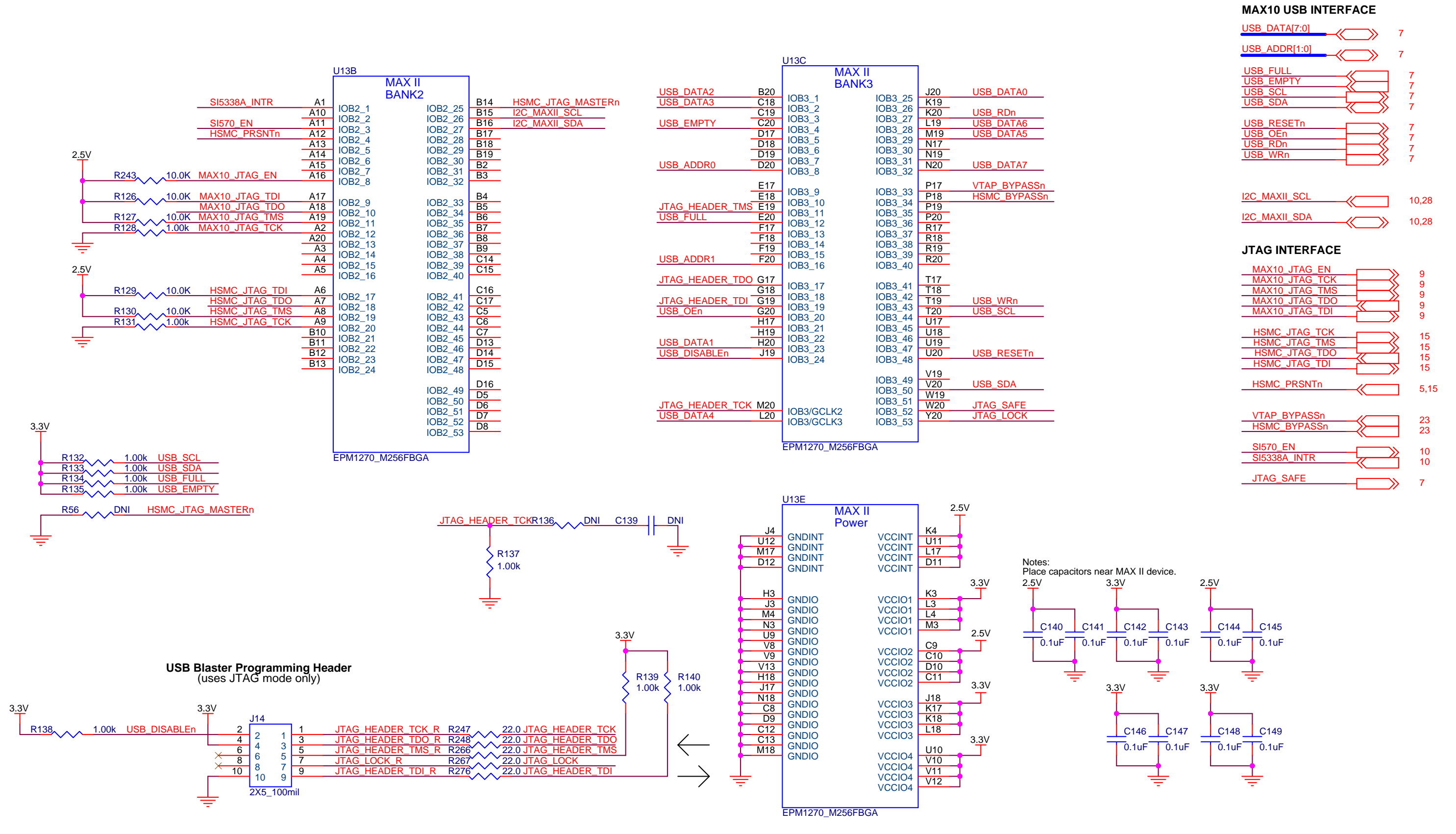
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Title MAX10 FPGA Development Kit (6XX-44292R)		
Size B	Document Number 150-0321401-C1	Rev C1
Date:	Wednesday, March 18, 2015	Sheet 20 of 31

# On-Board USB Blaster II-1



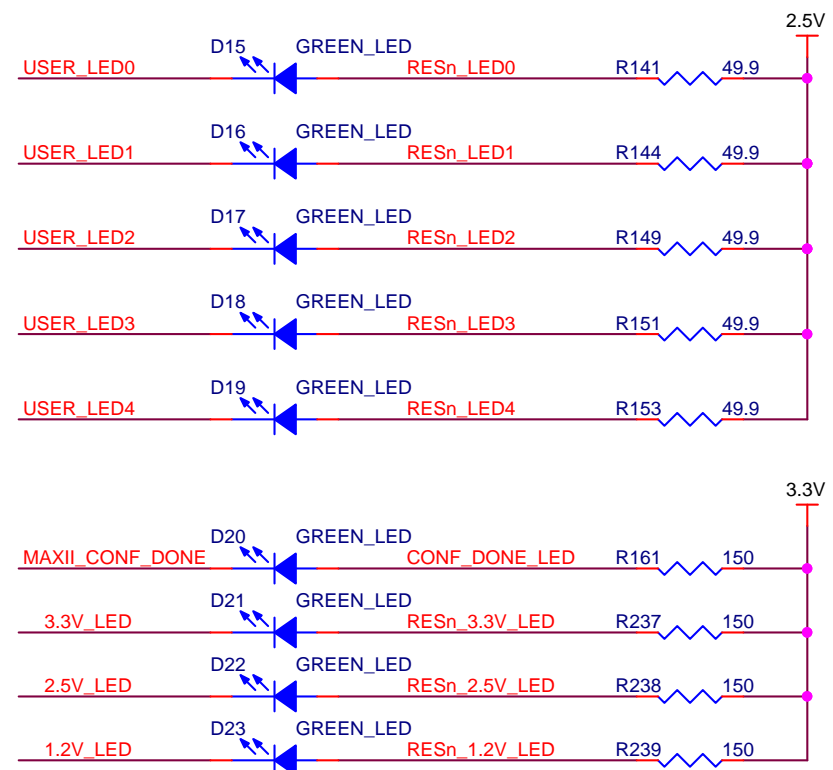
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Title: MAX10 FPGA Development Kit (6XX-44292R)		
Size: B	Document Number: 150-0321401-C1	Rev: C1
Date: Wednesday, March 18, 2015	Sheet: 21	of 31

# On-Board USB Blaster II-2

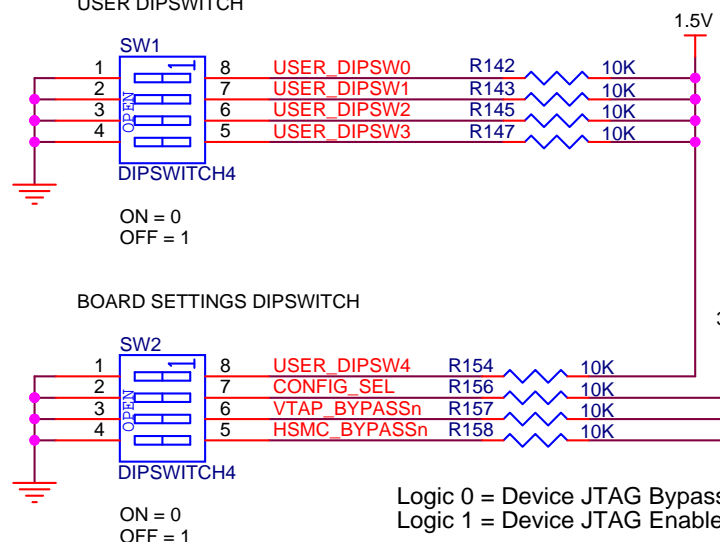


# LED, User IO, Connector

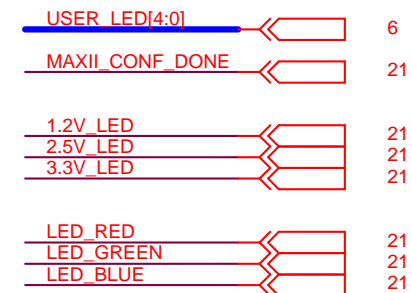
## LED



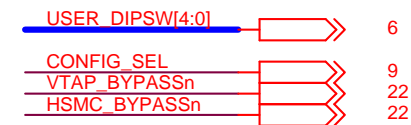
## USER DIPSWITCH



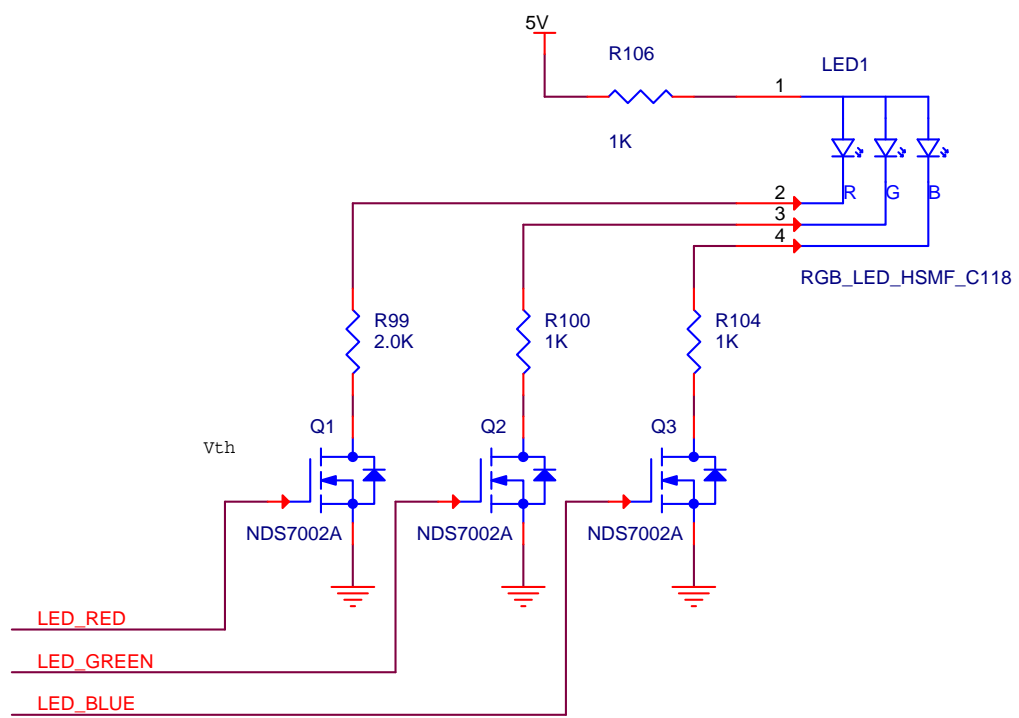
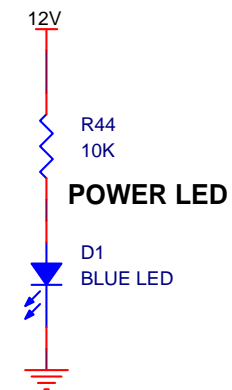
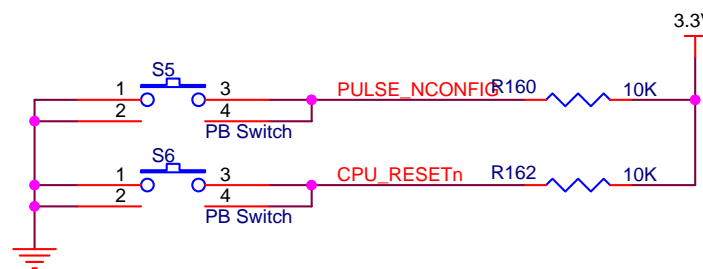
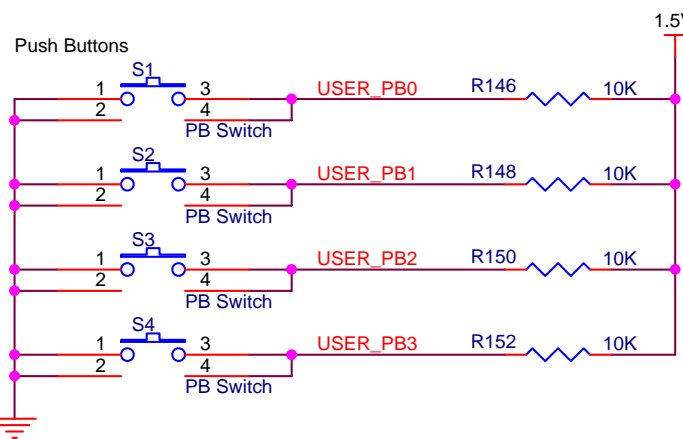
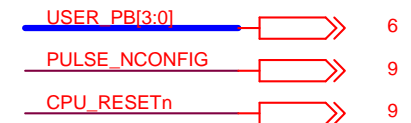
## LED



## Switches



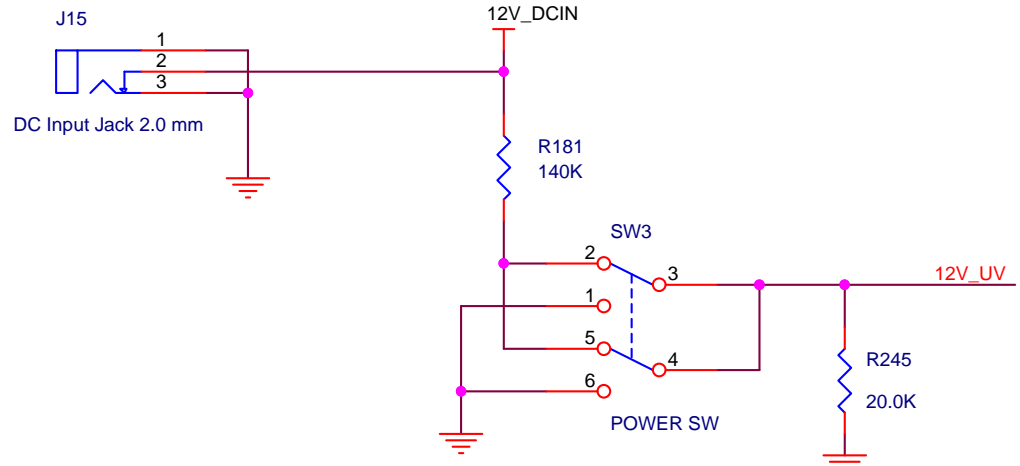
## Buttons



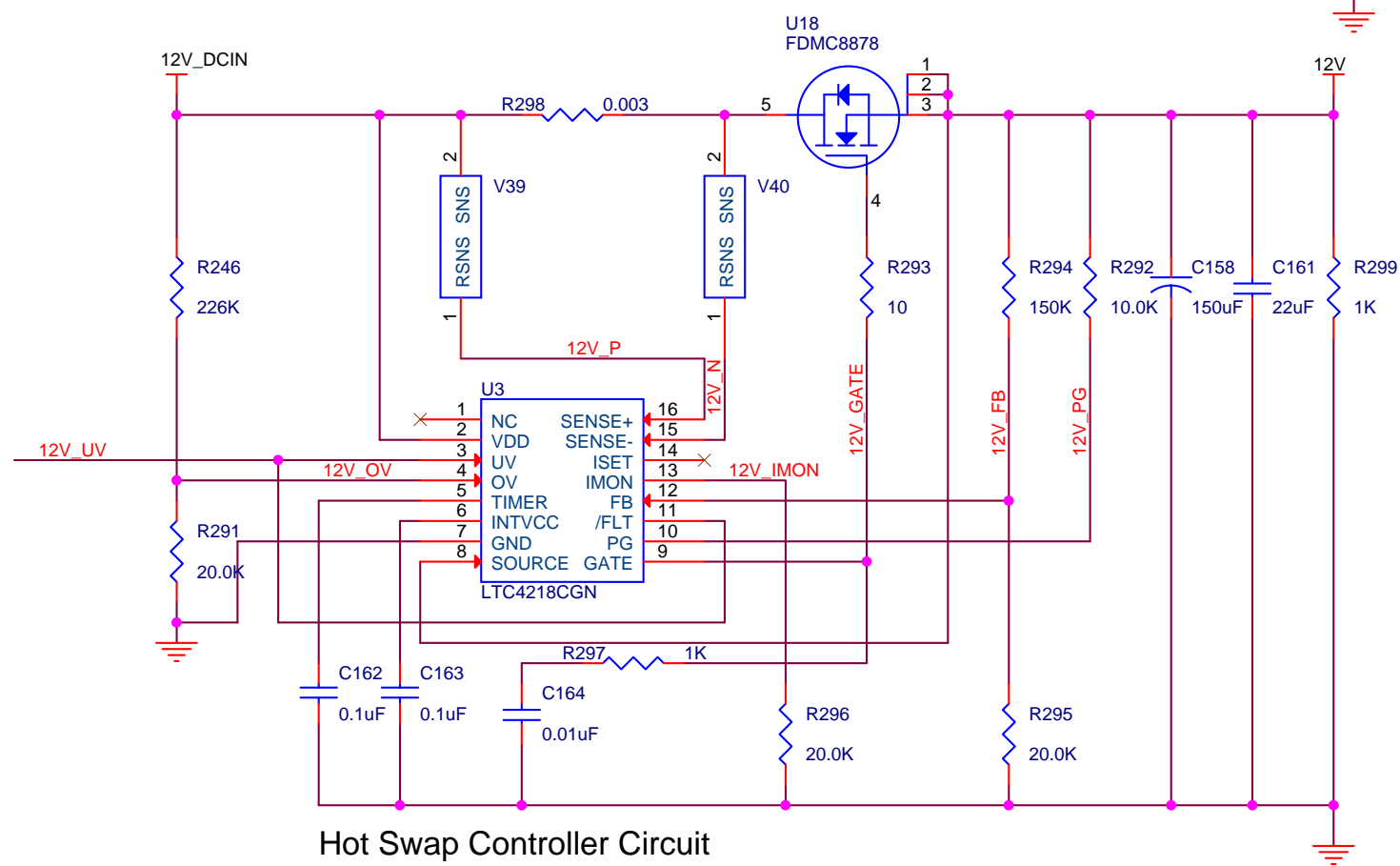
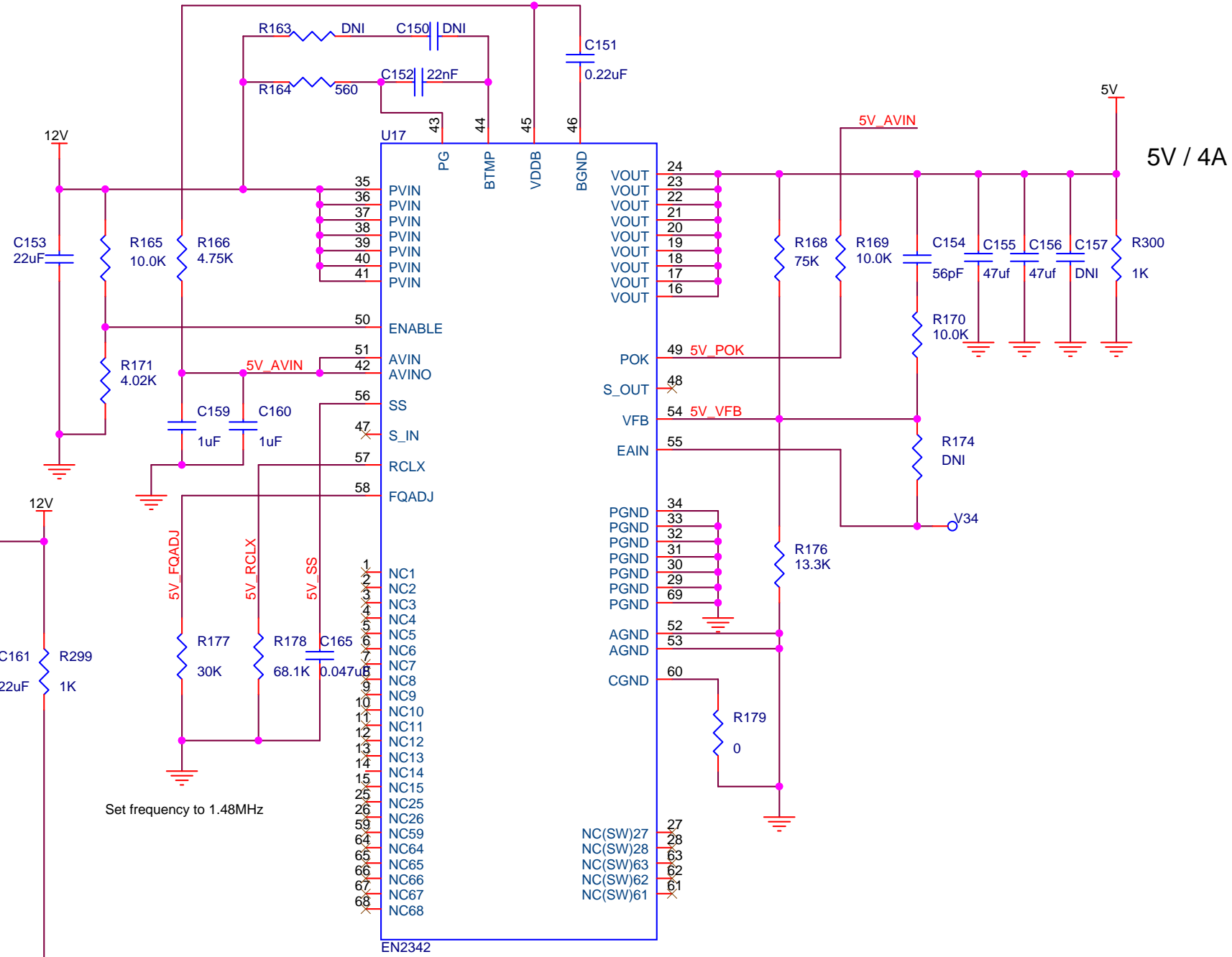
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Title MAX10 FPGA Development Kit (6XX-44292R)		
Size B	Document Number 150-0321401-C1	Rev C1
Date:	Wednesday, March 18, 2015	Sheet 23 of 31

# Power - 12V\_DCIN / 5V

## 12V DC Input



5V\_POK → 25,27



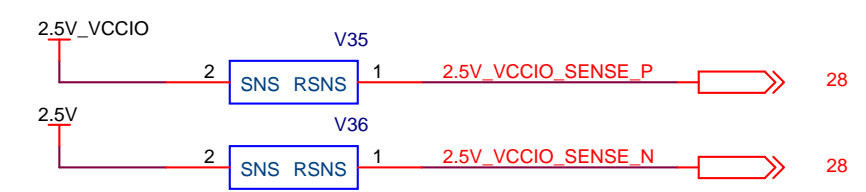
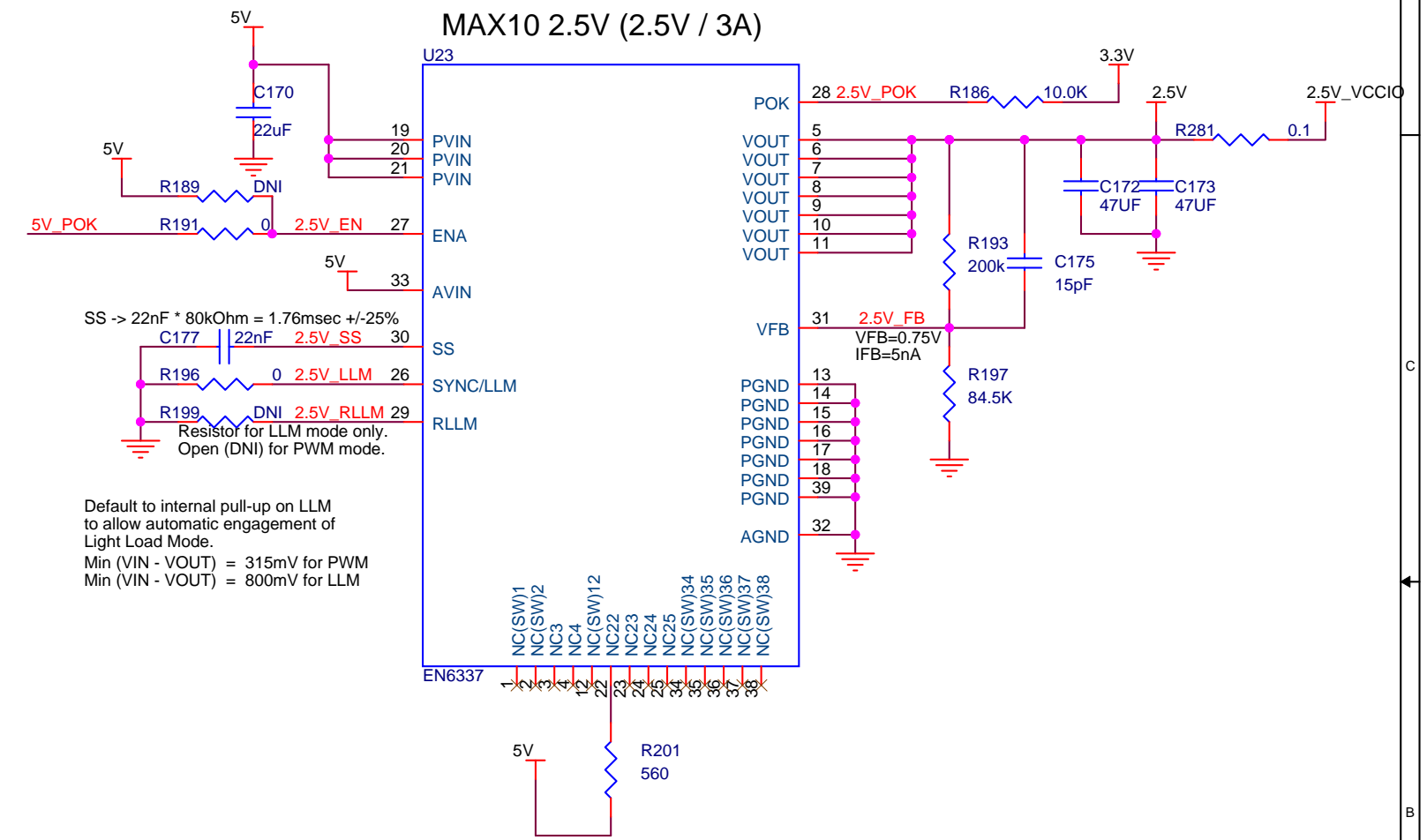
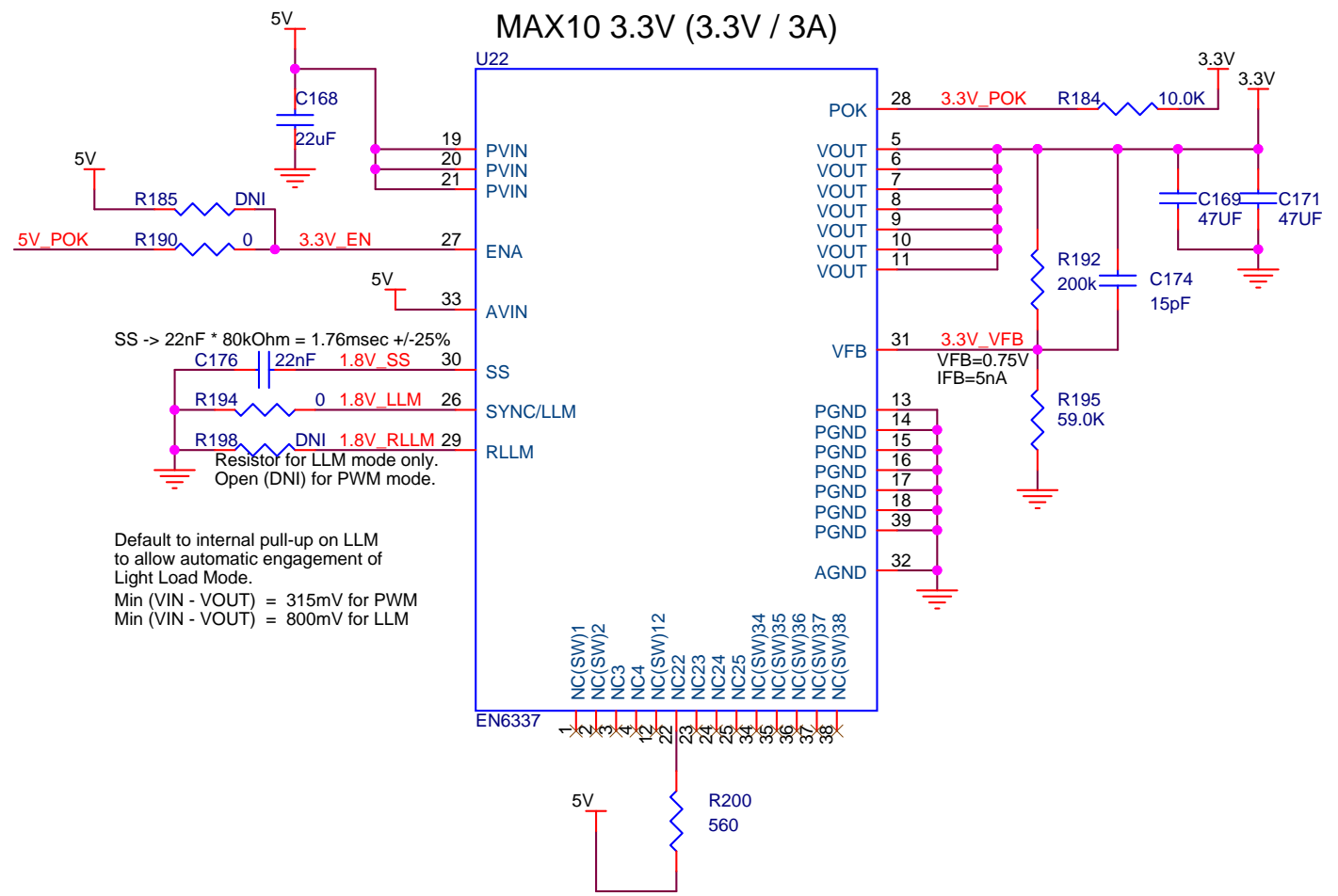
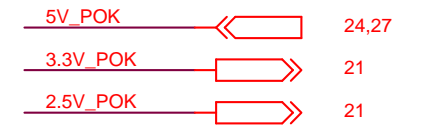
Hot Swap Controller Circuit



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Title MAX10 FPGA Development Kit (6XX-44292R)		
Size B	Document Number 150-0321401-C1	Rev C1
Date:	Tuesday, March 24, 2015	Sheet 24 of 31

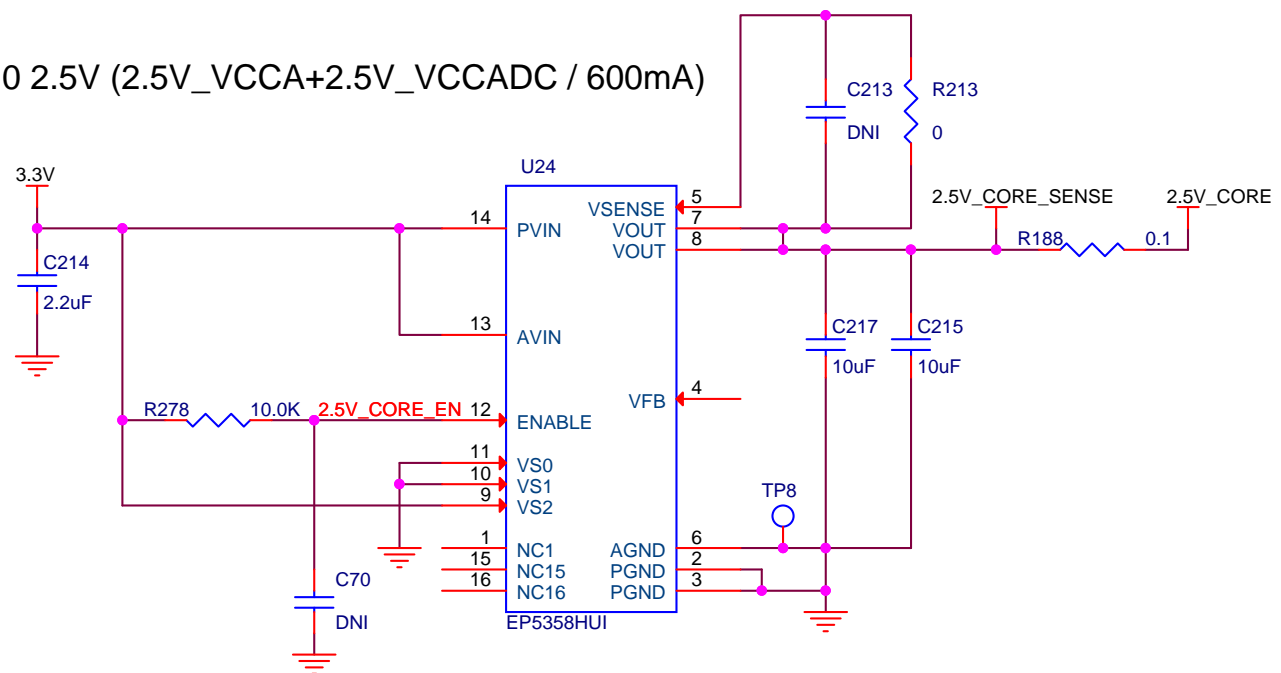


# Power - 3.3V / 2.5V

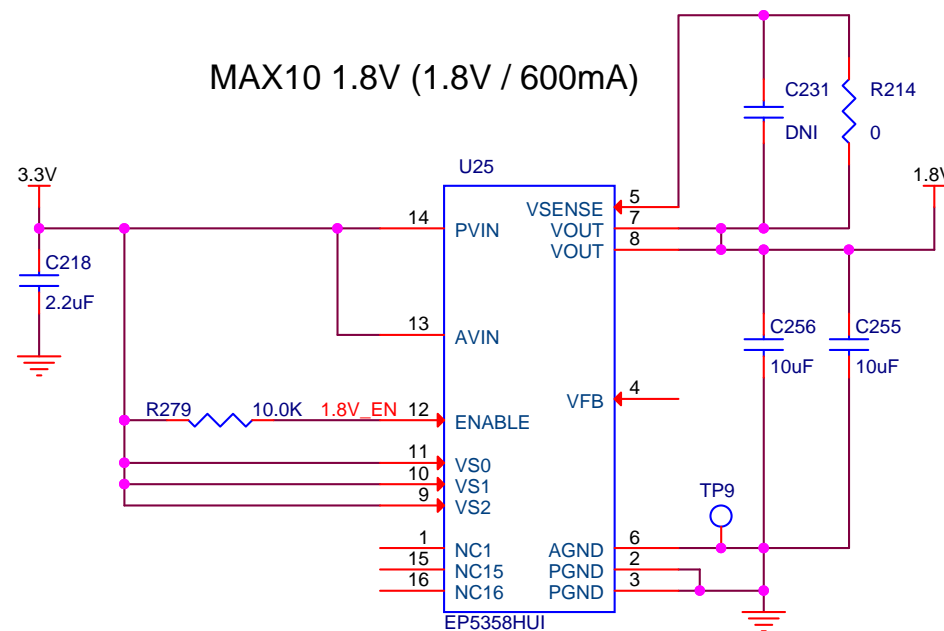


# Power - 2.5V\_VCC / 1.2V

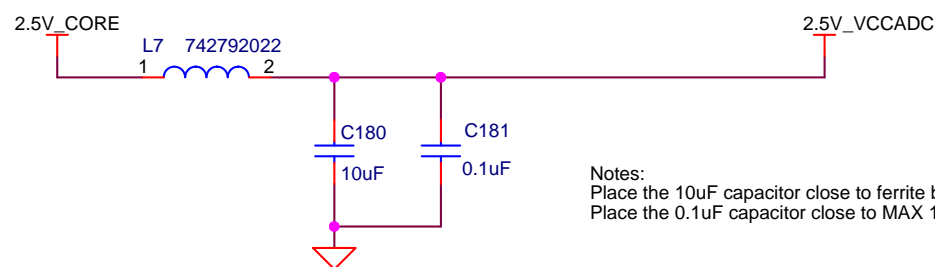
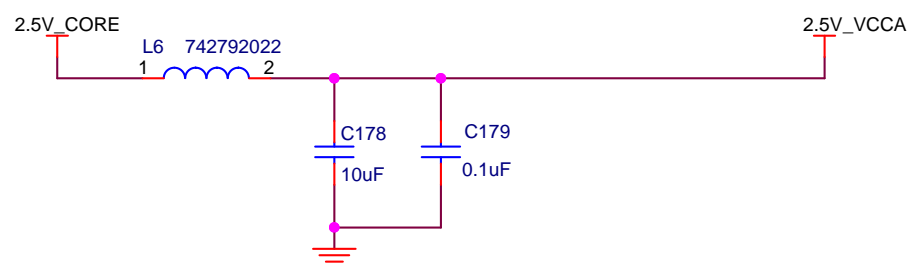
MAX10 2.5V (2.5V\_VCCA+2.5V\_VCCADC / 600mA)



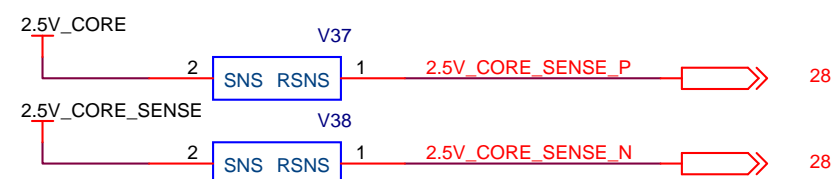
MAX10 1.8V (1.8V / 600mA)



1.2V\_POK → 21,27

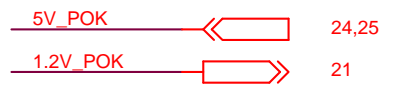
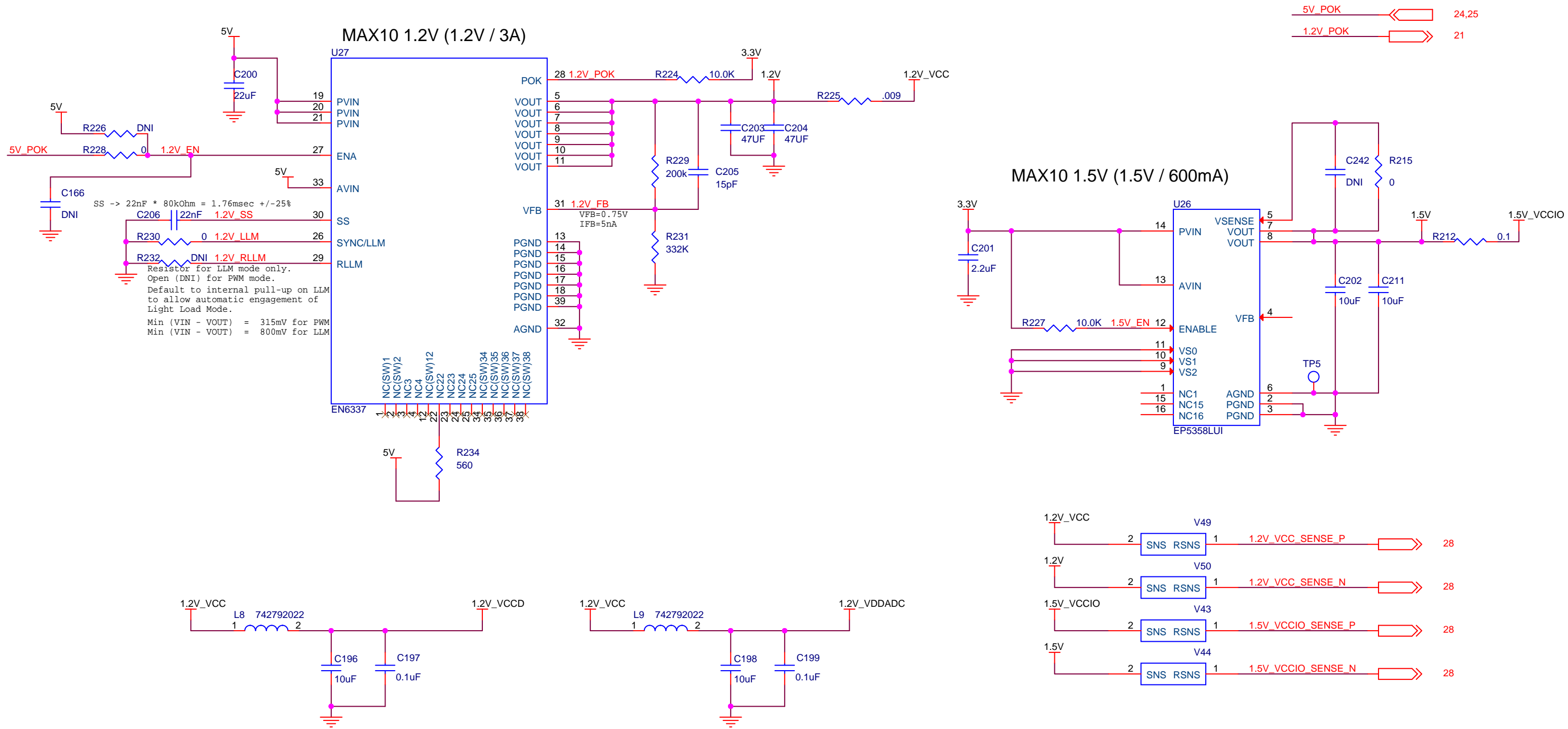


Notes:  
Place the 10uF capacitor close to ferrite bead.  
Place the 0.1uF capacitor close to MAX 10 pin.



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Title MAX10 FPGA Development Kit (6XX-44292R)		
Size B	Document Number 150-0321401-C1	Rev C1
Date: Tuesday, March 24, 2015	Sheet 26	of 31

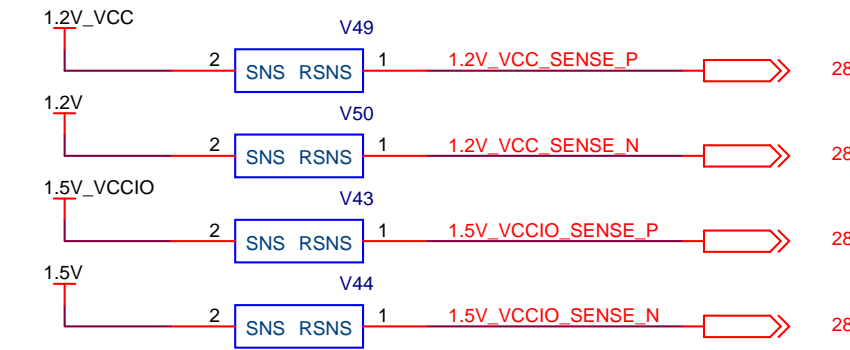
# Power - 1.5V / 1.2V



SS ->  $22nF * 80k\Omega = 1.76msec \pm 25\%$

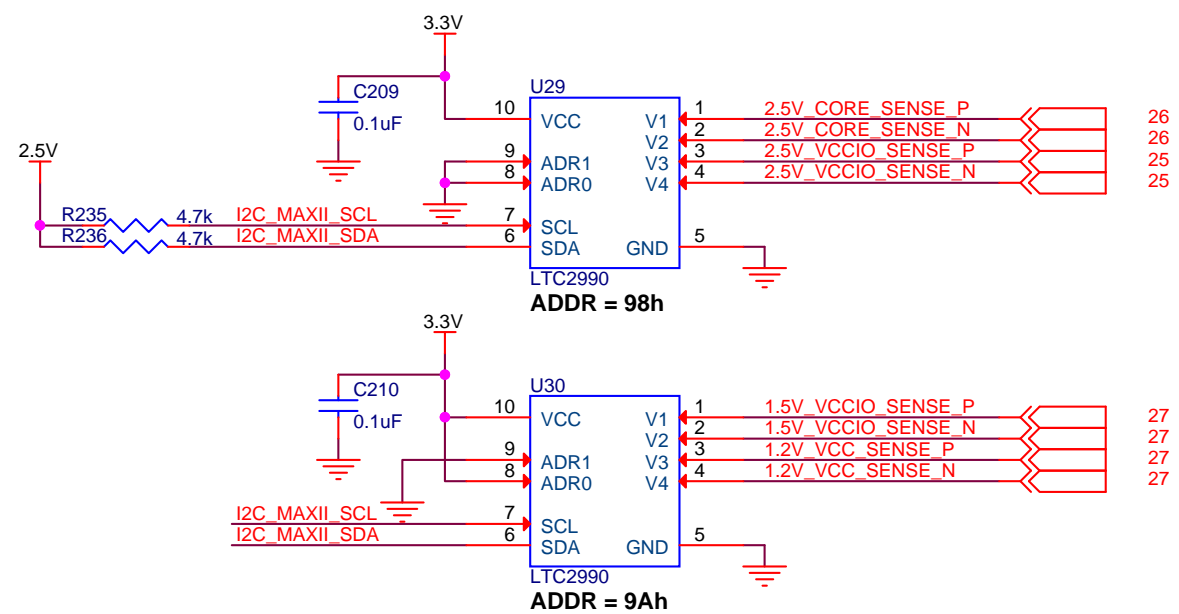
Resistor for LLM mode only.  
Open (DNI) for PWM mode.  
Default to internal pull-up on LLM  
to allow automatic engagement of  
Light Load Mode.  
Min (VIN - VOUT) = 315mV for PWM  
Min (VIN - VOUT) = 800mV for LLM

Notes:  
Place the 10uF capacitor close to ferrite bead.  
Place the 0.1uF capacitor close to MAX 10 pin.

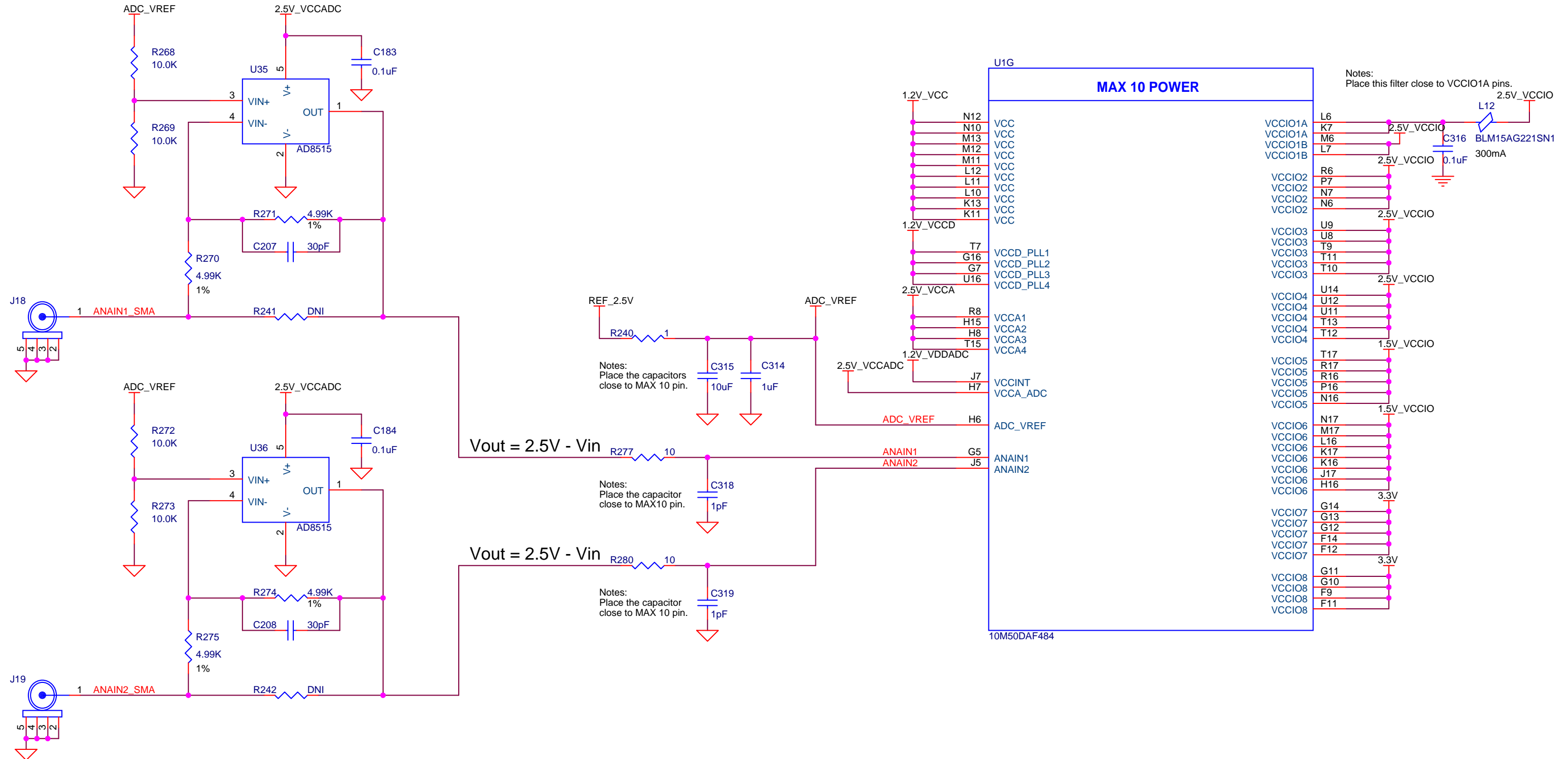


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Title MAX10 FPGA Development Kit (6XX-44292R)		
Size B	Document Number 150-0321401-C1	Rev C1
Date: Tuesday, March 24, 2015	Sheet 27	of 31

# Power - Power Monitor



# MAX10 Power



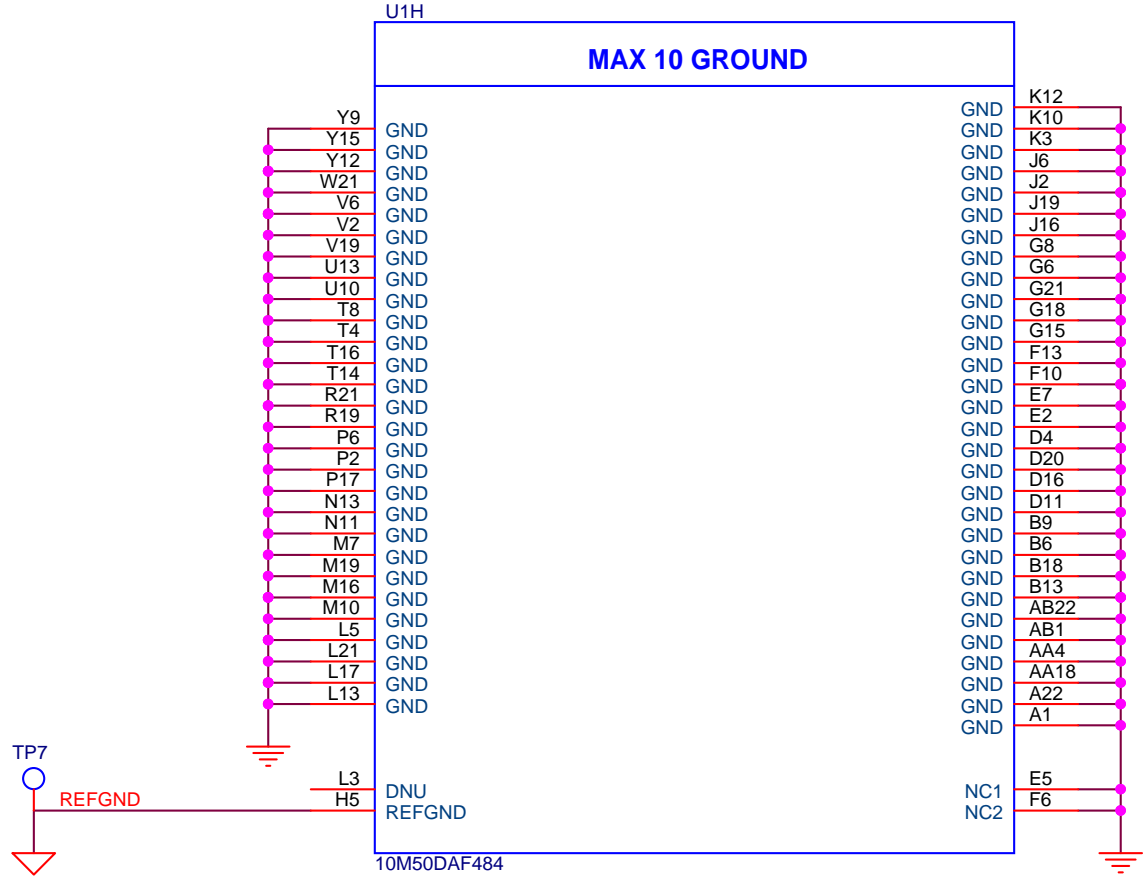
$$V_{out} = 2.5V - V_{in}$$

$$V_{out} = 2.5V - V_{in}$$



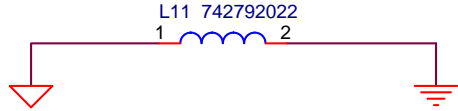
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Title MAX10 FPGA Development Kit (6XX-44292R)		
Size B	Document Number 150-0321401-C1	Rev C1
Date: Tuesday, March 24, 2015	Sheet 29	of 31

# MAX10 Ground



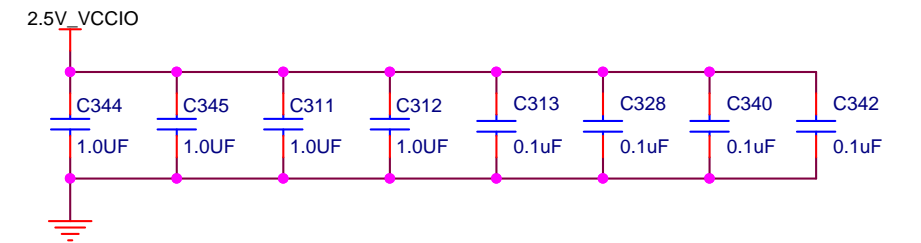
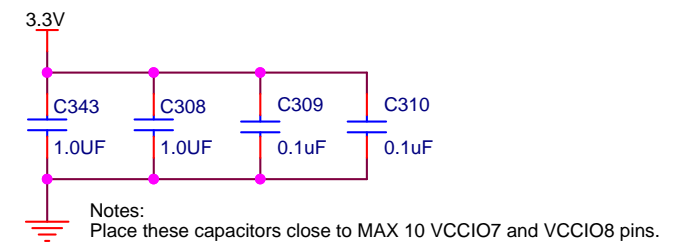
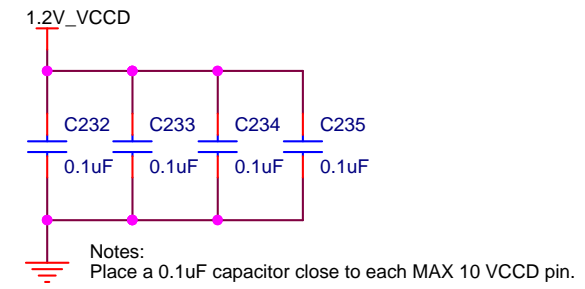
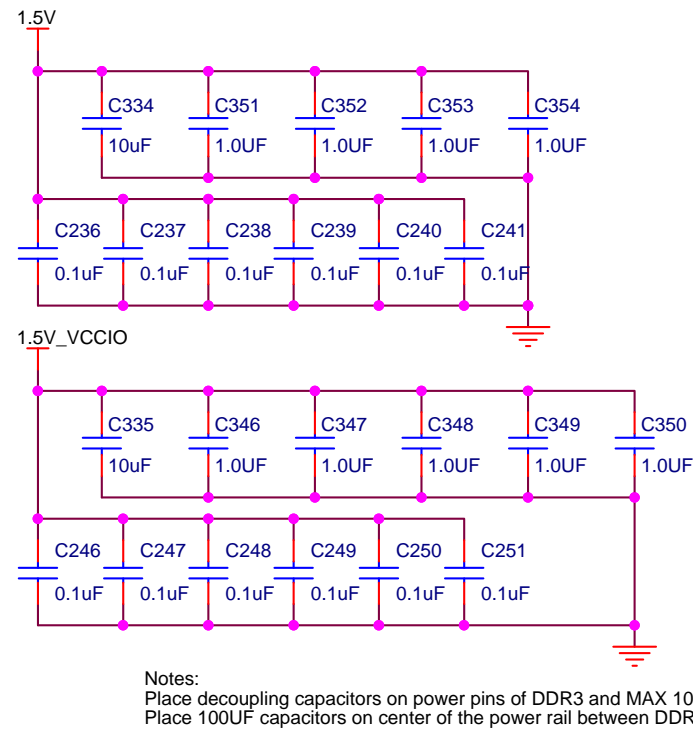
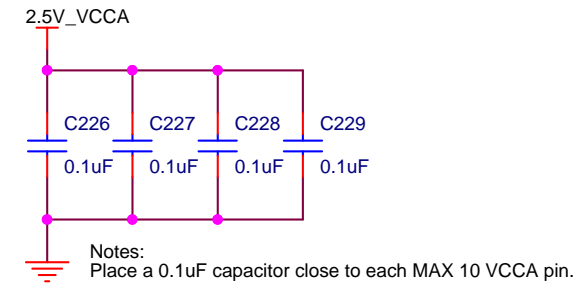
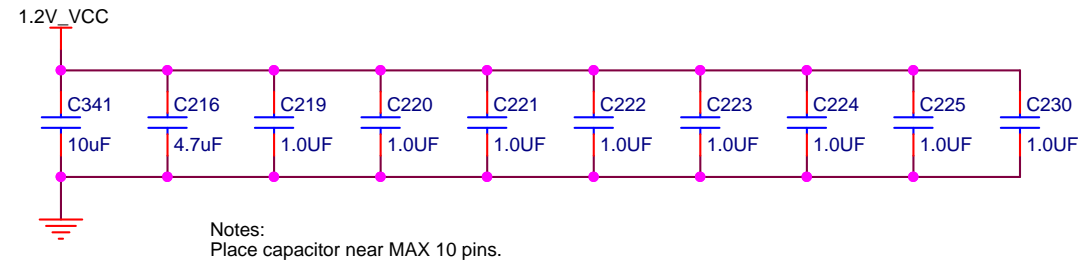
- Notes:
1. Use REFGND as ground reference.
  2. Route analog input signal adjacent to AVSSREF as possible.

Notes:  
Place this FB close to MAX 10 ADC\_VREF.



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Title MAX10 FPGA Development Kit (6XX-44292R)		
Size B	Document Number 150-0321401-C1	Rev C1
Date: Wednesday, March 18, 2015	Sheet 30	of 31

# MAX10 Decoupling



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Title MAX10 FPGA Development Kit (6XX-44292R)		
Size B	Document Number 150-0321401-C1	Rev C1
Date:	Wednesday, March 18, 2015	Sheet 31 of 31