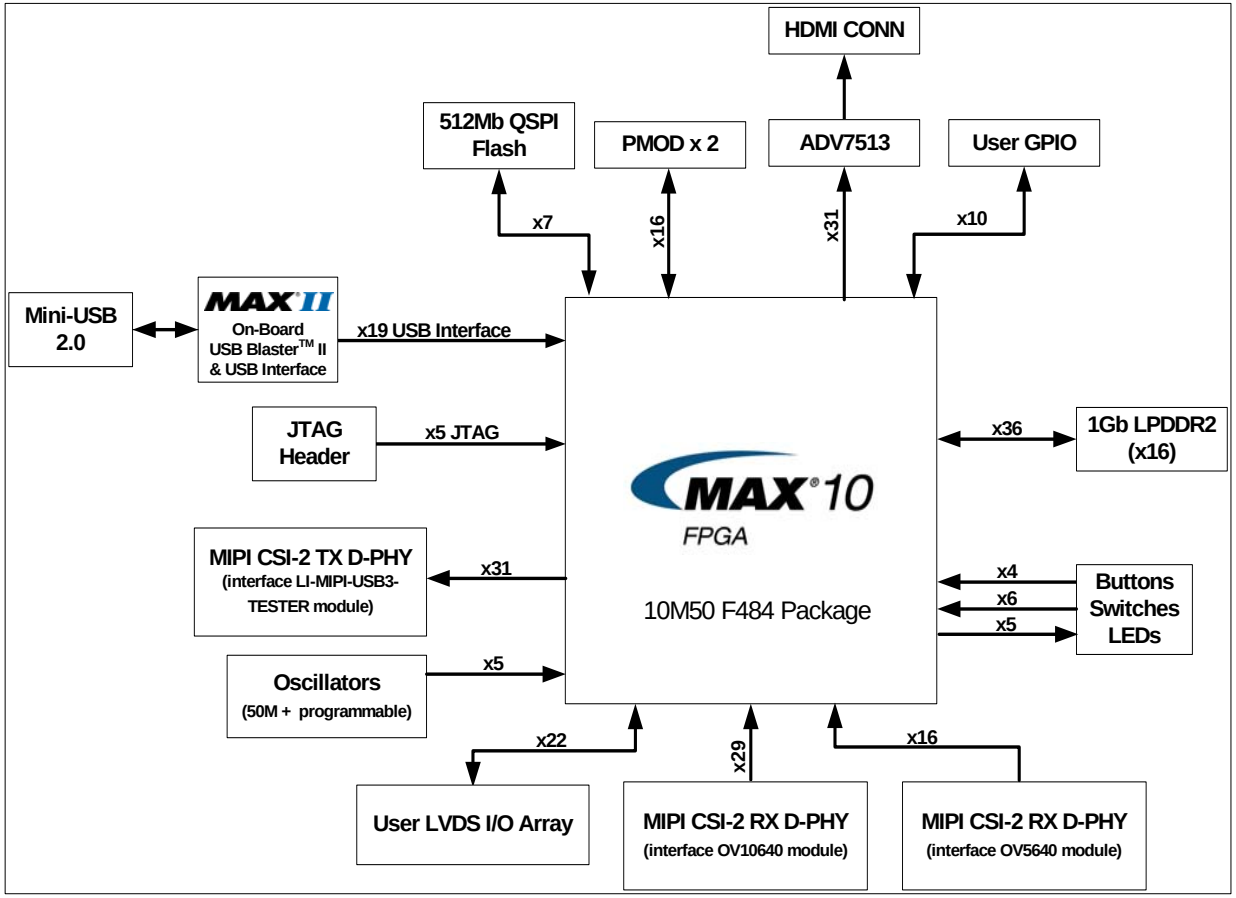
NOTES:

1. Project Drawing Numbers:

Raw PCB	100-0321404-A1.1
Gerber Files	110-0321404-A1.1
PCB Design Files	120-0321404-A1.1
Assembly Drawing	130-0321404-A1.1
Fab Drawing	140-0321404-A1.1
Schematic Drawing	150-0321404-A1.1
PCB Film	160-0321404-A1.1
Bill of Materials	170-0321404-A1.1
Schematic Design Files	180-0321404-A1.1
Functional Specification	210-0321404-A1.1
PCB Layout Guidelines	220-0321404-A1.1
Assembly Rework	320-0321404-A1.1

REV	DATE	PAGES	DESCRIPTION
A1	Jun 19 2015	All	Initial Revision A Release.
A1.1	Sep 15 2015	1	Update block diagram.
		2	Update power tree.
		10	Delete C12.
		18	Add note for SW2.4 MAX10_BYPASSn.
		22	Change the value of C219 from DNI to 47uF.
		23	Add R315 to 1.2V_VCCIO.
		25	Change the value of C232 from 100uF to DNI.
A1.2	Dec 23 2015	10	Change LPDDR2_IS43LD16640A-3BL(333MHz part) to IS43LD16640A-25BL (400MHz part) due to Altera IP recommendation.

MAX 10 FPGA 10M50 Evaluation Kit Board



PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Rev. History
2	Power Tree
3	Clock Tree
4	MAX10 Banks 1 & 2
5	MAX10 Banks 3 & 4
6	MAX10 Banks 5 & 6
7	MAX10 Banks 7 & 8
8	MAX10 Clocks
9	MAX10 Configuration
10	LPDDR2 SDRAM
11	MIPI CSI-2 Tx D-PHY LI-USB3
12	MIPI CSI-2 Rx D-PHY OV10640
13	MIPI CSI-2 Rx D-PHY OV5640
14	HDMI (VIDEO ONLY)
15	On-Board USB Blaster II -1
16	On-Board USB Blaster II -2
17	PMOD, GPIO, LVDS UserIO
18	Pushbutton, Switch, LED
19	Clocking
20	QSPI Flash
21	Hot Swap and Power 3.3 V
22	Power 2.5 V & 1.8V
23	Power 1.2V
24	MAX 10 Power & Ground
25	Decoupling

Altera Corporation, 301, Bibo Rd #888, Shanghai, China, 201203

Title: MAX 10 FPGA 10M50 Evaluation Kit (6XX-44364R)

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B	<Doc>	A1.1

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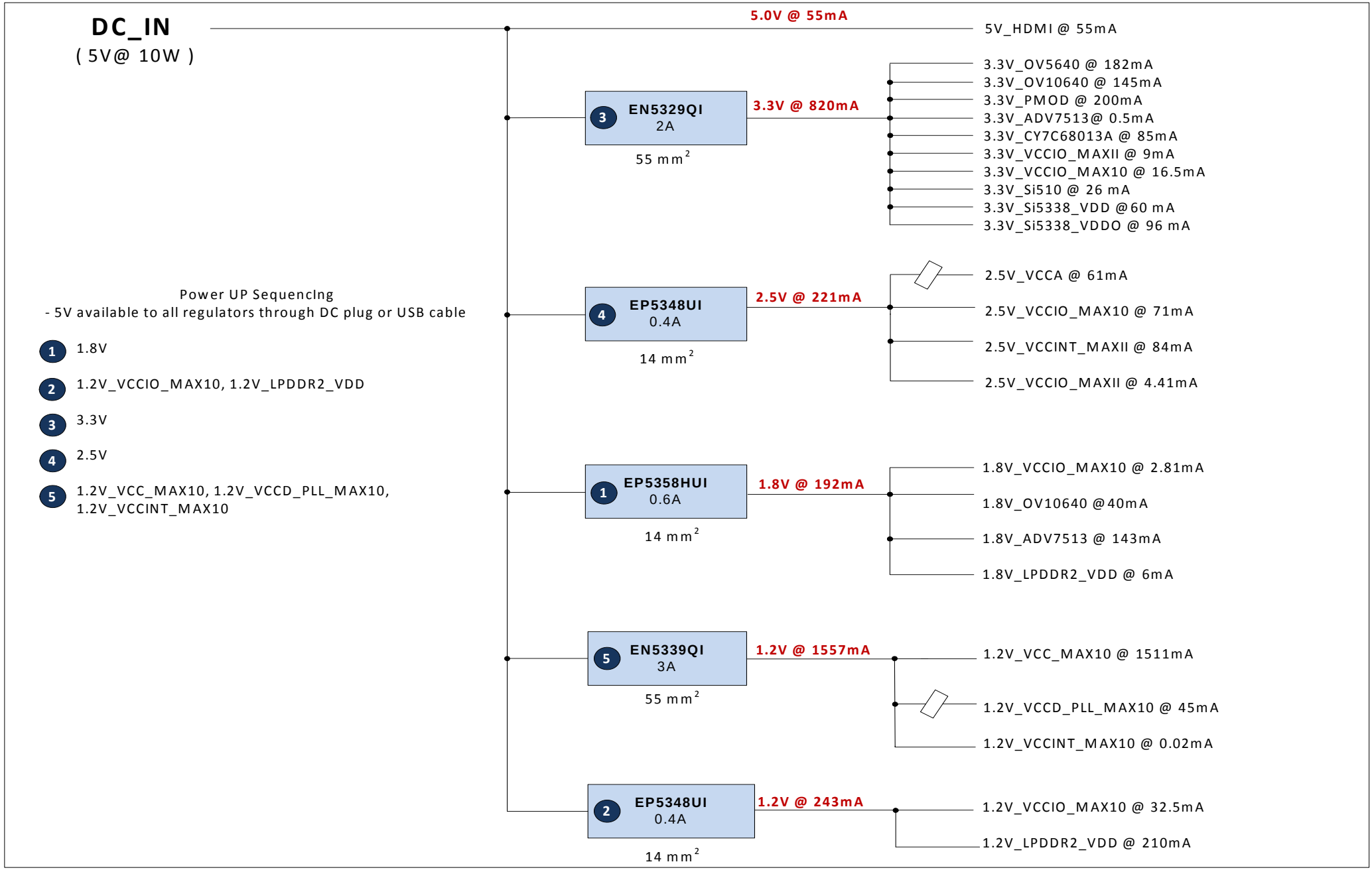
POWER TREE



Power UP Sequencing
- 5V available to all regulators through DC plug or USB cable

1. 1.8V
2. 1.2V_VCCIO_MAX10, 1.2V_LPDDR2_VDD
3. 3.3V
4. 2.5V
5. 1.2V_VCC_MAX10, 1.2V_VCCD_PLL_MAX10, 1.2V_VCCINT_MAX10

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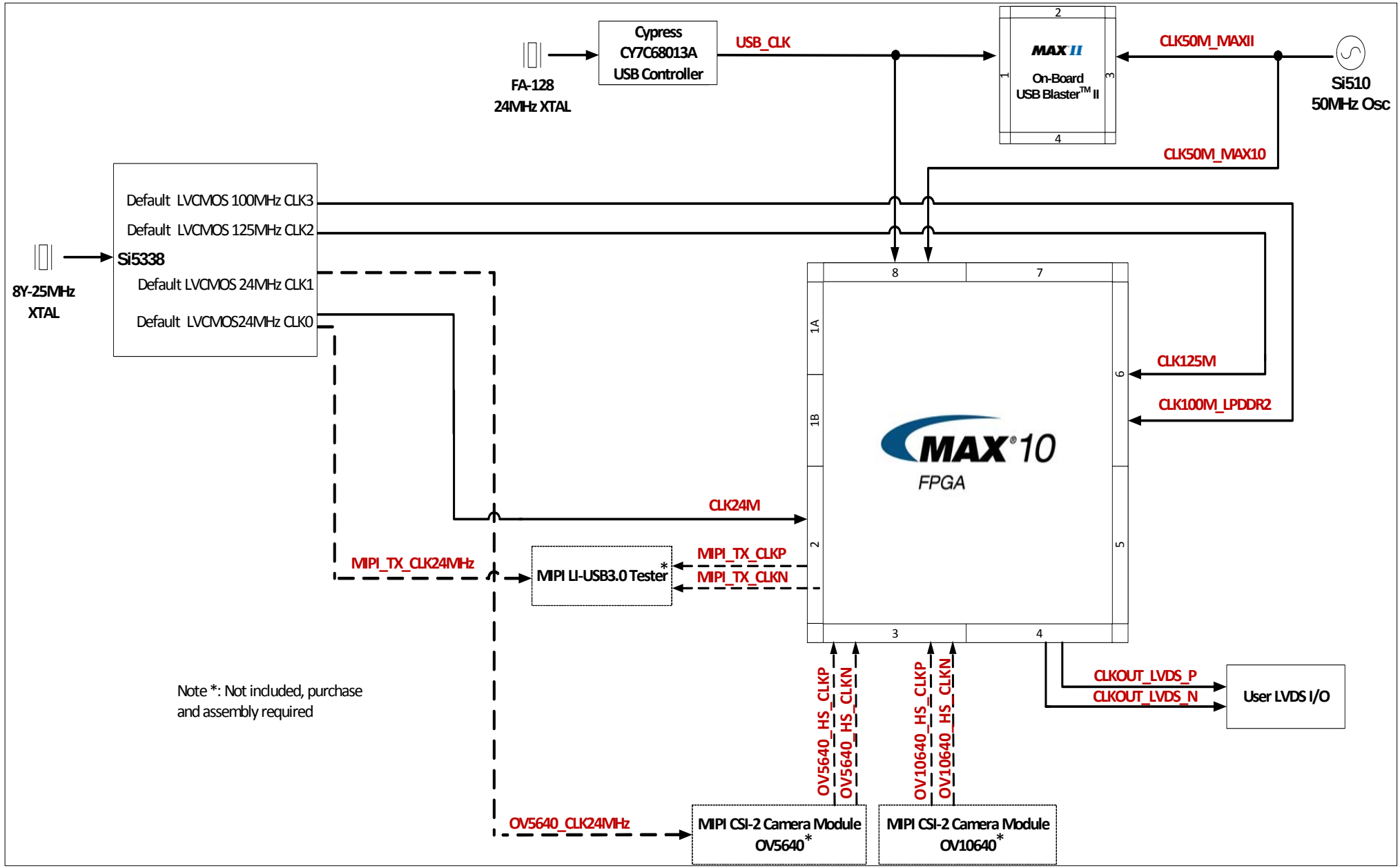
CLOCK TREE



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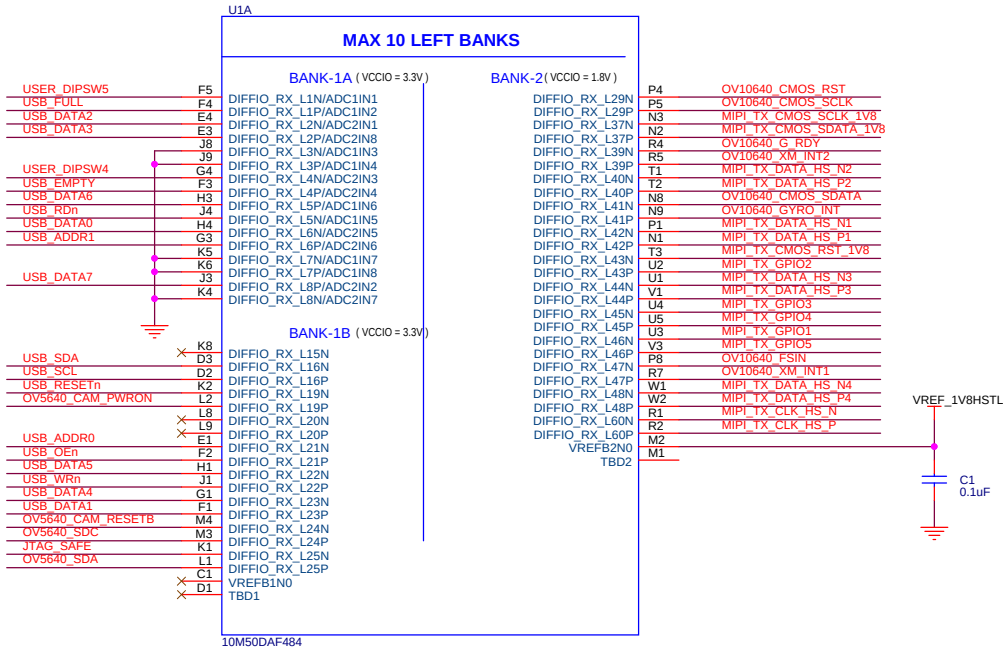
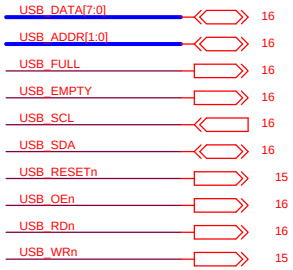
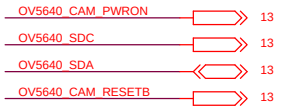
MAX10 BANKS 1 & 2



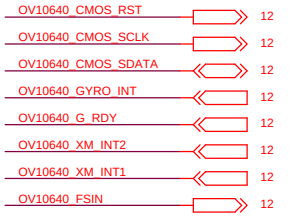
MAX10 USB Interface



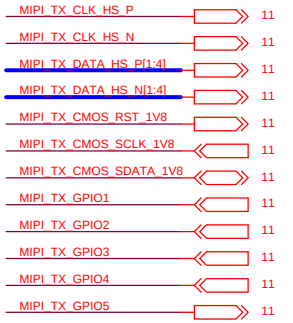
OV5640 CSI-2 RX Interface



OV10640 CSI-2 RX Interface



LI-USB3 CSI-2 TX Interface



Misc

User DIP Switch

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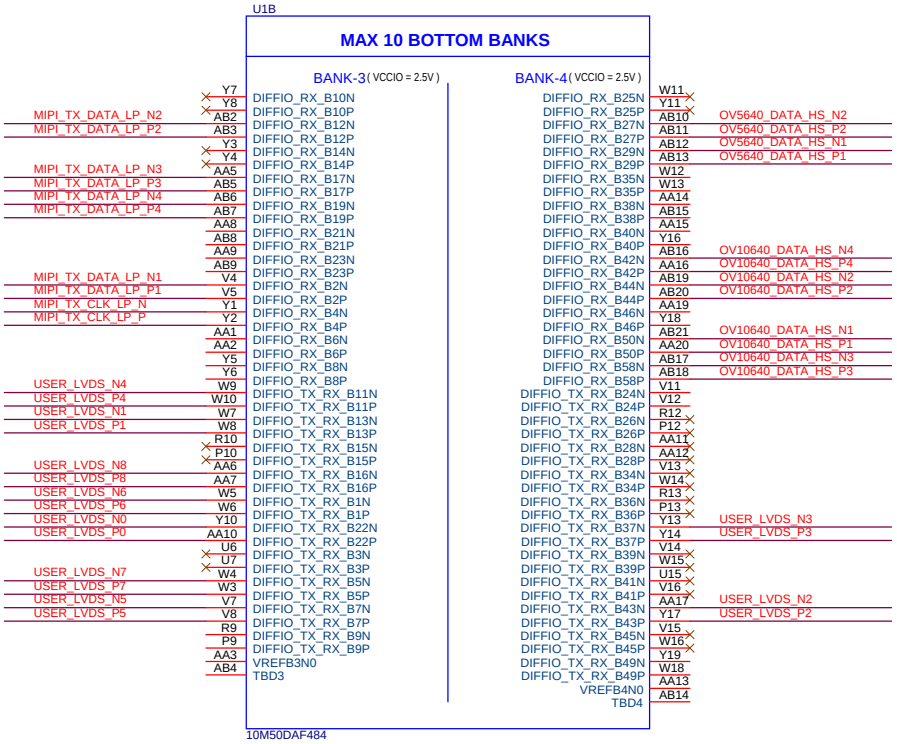
MAX10 BANKS 3 & 4



User LVDS IO

USER_LVDS_P[0:8] 17
USER_LVDS_N[0:8] 17

OV10640 Interface

OV10640_DATA_HS_P[1:4] 12
OV10640_DATA_HS_N[1:4] 12

OV5640 Interface

OV5640_DATA_HS_P[1:2] 13
OV5640_DATA_HS_N[1:2] 13

LI-USB3 CSI-2 TX Interface

MIPI_TX_CLK_LP_P 11
MIPI_TX_CLK_LP_N 11
MIPI_TX_DATA_LP_P[1:4] 11
MIPI_TX_DATA_LP_N[1:4] 11

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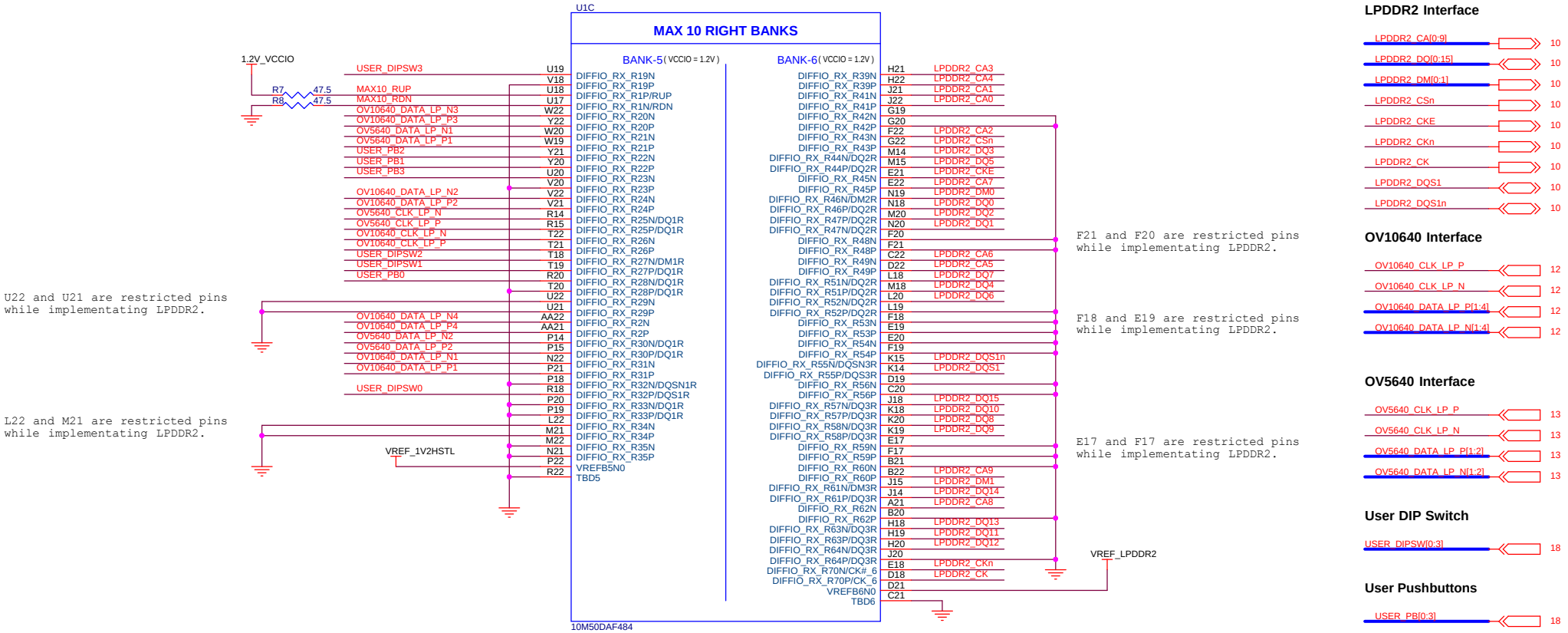
MAX10 BANKS 5 & 6



LPDDR2 Interface

LPDDR2_CA[0:9] 10
LPDDR2_DQ[0:15] 10
LPDDR2_DM[0:1] 10
LPDDR2_CSn 10
LPDDR2_CKE 10
LPDDR2_CKn 10
LPDDR2_CK 10
LPDDR2_DQS1 10
LPDDR2_DQS1n 10

OV10640 Interface

OV10640_CLK_LP_P 12
OV10640_CLK_LP_N 12
OV10640_DATA_LP_P[1:4] 12
OV10640_DATA_LP_N[1:4] 12

OV5640 Interface

OV5640_CLK_LP_P 13
OV5640_CLK_LP_N 13
OV5640_DATA_LP_P[1:2] 13
OV5640_DATA_LP_N[1:2] 13

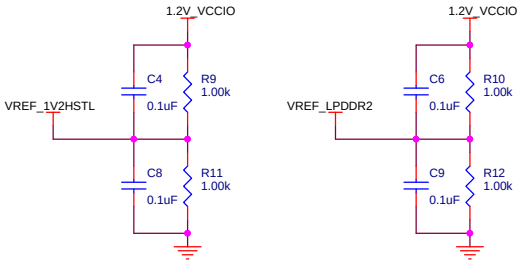
User DIP Switch

USER_DIPSW[0:3] 18

User Pushbuttons

USER_PB[0:3] 18

Reference Voltages of 1.2V HSTL and LPDDR2



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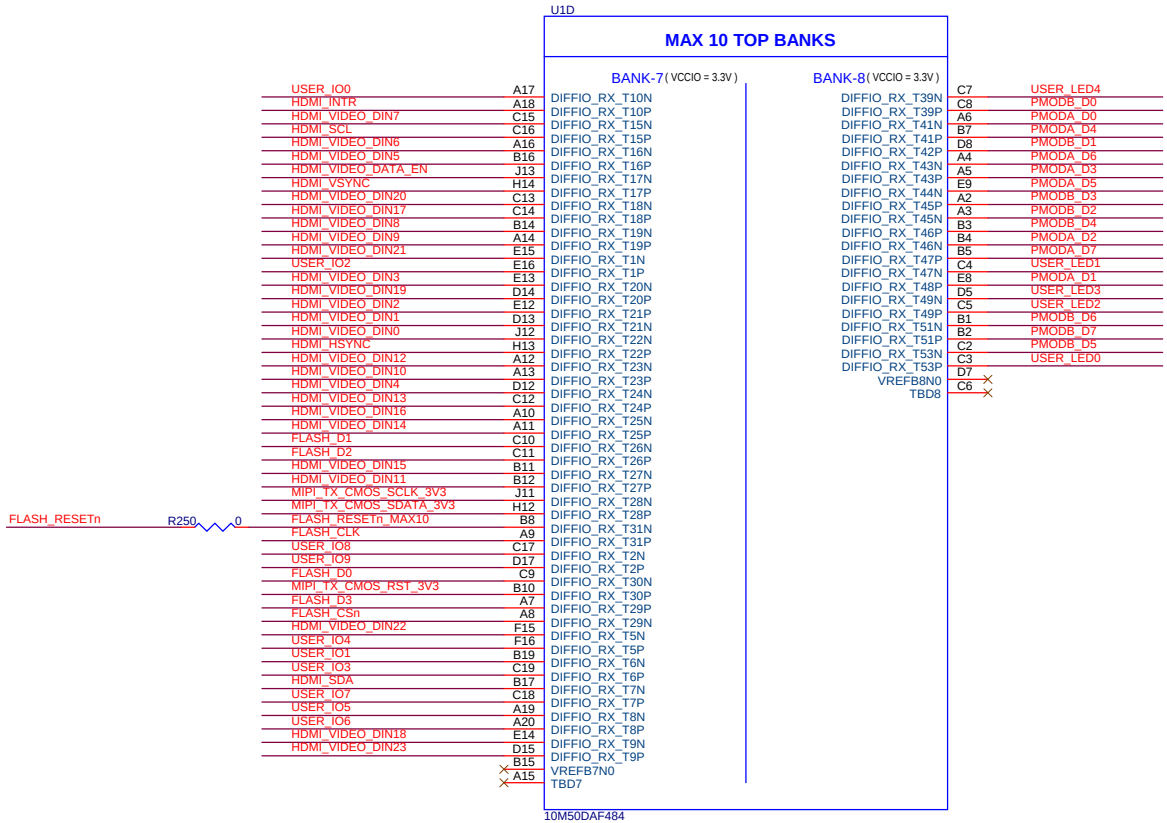
MAX10 BANKS 7 & 8



User IO

USER_IO[0:9] — 17

PMOD

PMODA_D[7:0] — 17

PMODB_D[7:0] — 17

HDMI TX

HDMI_VIDEO_DIN[23:0] — 14

HDMI_HSYNC — 14

HDMI_VSYNC — 14

HDMI_VIDEO_DATA_EN — 14

HDMI_INTR — 14

HDMI_SDA — 14

HDMI_SCL — 14

Flash

FLASH_RESETn — 15,25

FLASH_CSn — 25

FLASH_CLK — 25

FLASH_D[0:3] — 25

LI-USB3 CSI-2 TX Interface

MIPI_TX_CMOS_SCLK_3V3 — 11

MIPI_TX_CMOS_SDATA_3V3 — 11

MIPI_TX_CMOS_RST_3V3 — 11

User LED

USER_LED[0:4] — 18

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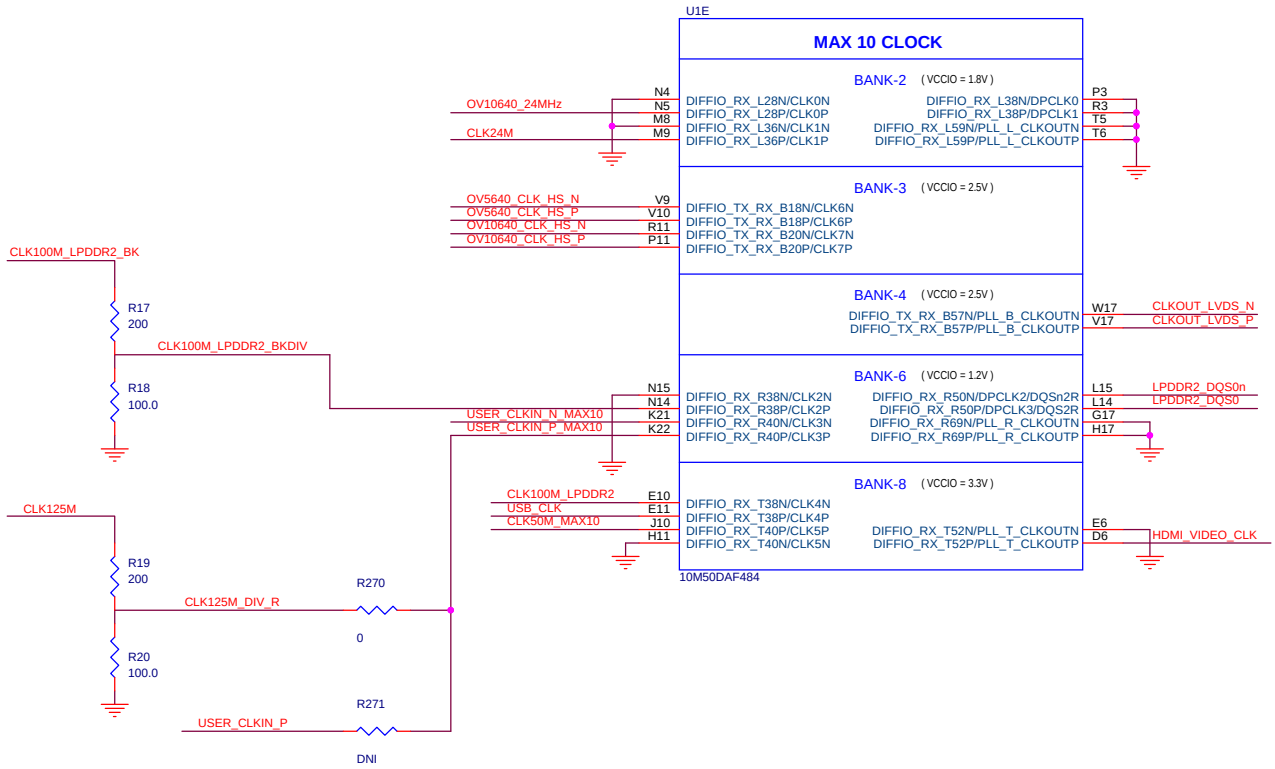
MAX10 CLOCKS



Note: CLK125M_LVDS is the clock source provided to external LVDS user interface.
USER_CLKIN_P is used for external sigle-ended clock input.
USER_CLKIN_P/N is used for external differential clock input.

LPDDR2 Interface
- LPDDR2_DQS0 — 10
- LPDDR2_DQS0n — 10

OV5640 Interface
- OV5640_CLK_HS_P — 13
- OV5640_CLK_HS_N — 13

OV10640 Interface
- OV10640_CLK_HS_P — 12
- OV10640_CLK_HS_N — 12
- OV10640_24MHz — 12

Si5338
- CLK50M_MAX10 — 19
- CLK24M — 19
- CLK125M — 19
- CLK100M_LPDDR2 — 19
- CLK100M_LPDDR2_BK — 19

USB Blaster II
- USB_CLK — 15

User LVDS
- USER_CLKIN_P — 17
- USER_CLKIN_N_MAX10 — 17
- CLKOUT_LVDS_P — 17
- CLKOUT_LVDS_N — 17

HDMI
- HDMI_VIDEO_CLK — 14

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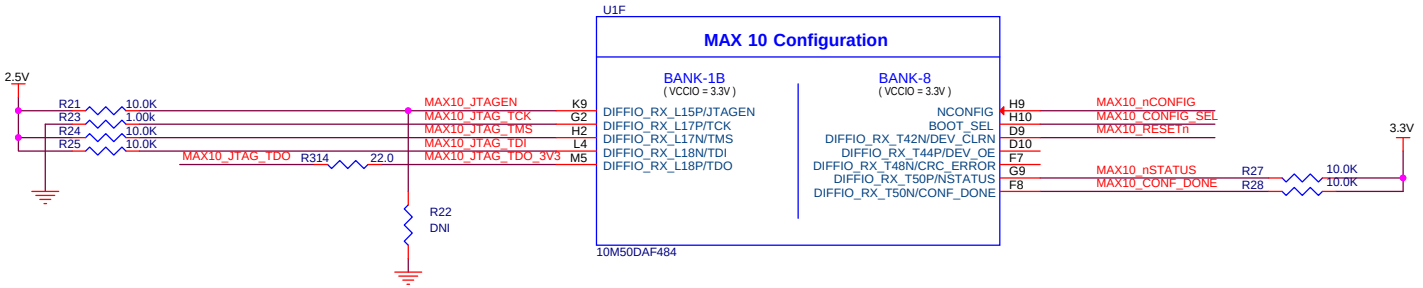
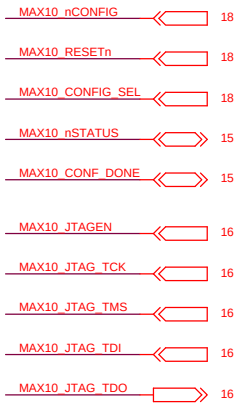
MAX10 CONFIGURATION



Configuration



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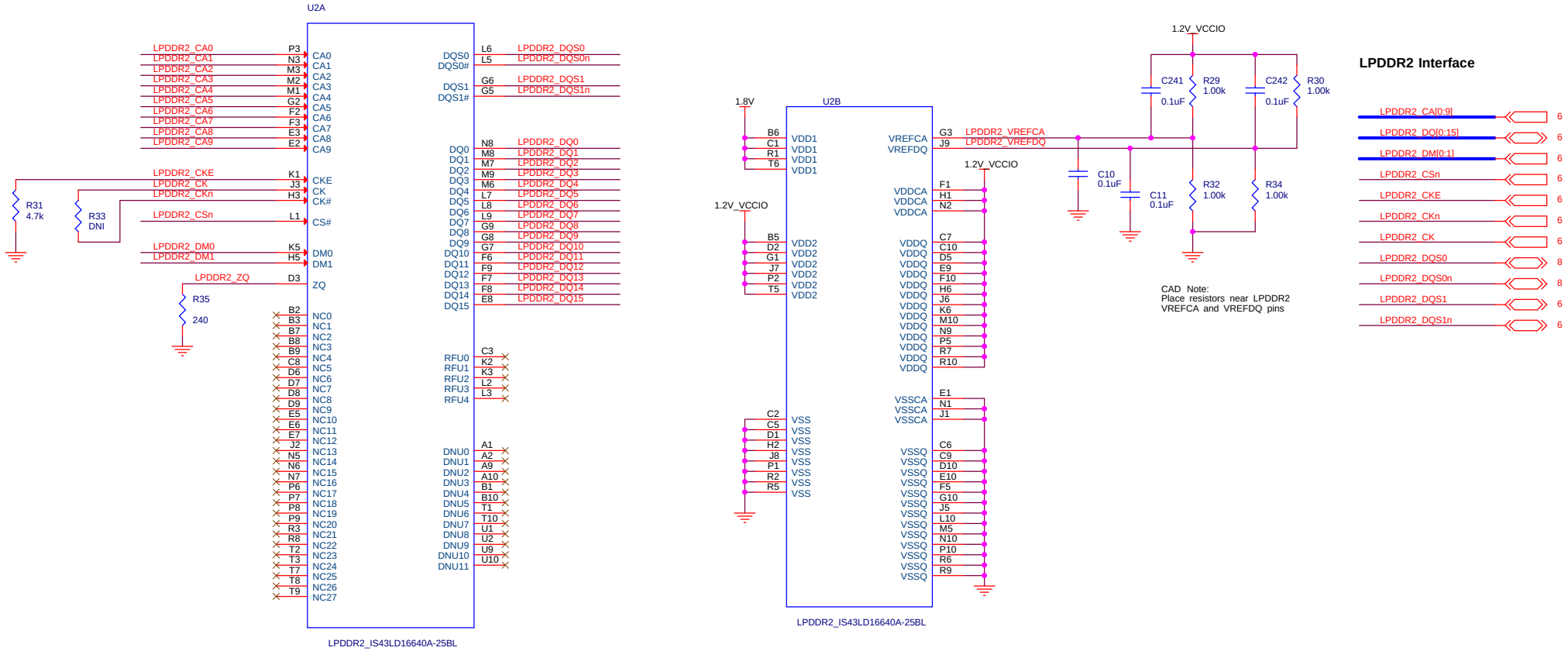
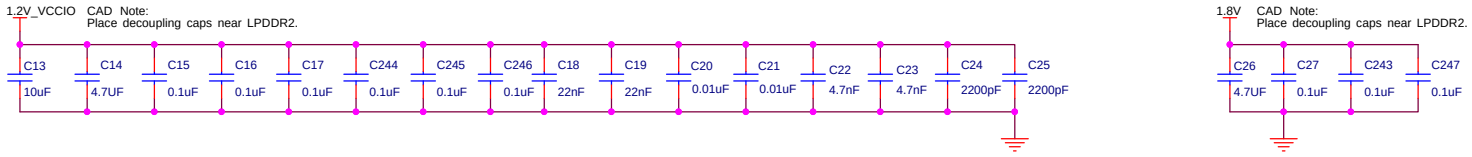
LPDDR2 SDRAM x 16



LPDDR2 Power Decoupling



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MIPI CSI-2 TX D-PHY

CAD Note:
Place resistors near FPGA side.

TP7 TP8 TP10 TP11
MIPI_TX_CLK_LP_P
MIPI_TX_CLK_HS_P
MIPI_TX_CLK_HS_N
MIPI_TX_CLK_LP_N
R37 100.0
R41 150
R42 150
R47 100.0
R38 100.0
R43 100.0
MIPI_TX_CLKP
MIPI_TX_CLKN

CAD Note:
Place resistors near FPGA side.

TP13 TP14 TP15 TP16
MIPI_TX_DATA_LP_P1
MIPI_TX_DATA_HS_P1
MIPI_TX_DATA_HS_N1
MIPI_TX_DATA_LP_N1
R48 100.0
R50 150
R54 150
R58 100.0
R51 100.0
R55 100.0
MIPI_TX_DATA1P
MIPI_TX_DATA1N

CAD Note:
Place resistors near FPGA side.

TP19 TP20 TP21 TP22
MIPI_TX_DATA_LP_P2
MIPI_TX_DATA_HS_P2
MIPI_TX_DATA_HS_N2
MIPI_TX_DATA_LP_N2
R60 100.0
R62 150
R65 150
R67 100.0
R63 100.0
R66 100.0
MIPI_TX_DATA2P
MIPI_TX_DATA2N

CAD Note:
Place resistors near FPGA side.

TP25 TP26 TP27 TP28
MIPI_TX_DATA_LP_P3
MIPI_TX_DATA_HS_P3
MIPI_TX_DATA_HS_N3
MIPI_TX_DATA_LP_N3
R36 100.0
R40 150
R44 150
R46 100.0
R39 100.0
R45 100.0
MIPI_TX_DATA3P
MIPI_TX_DATA3N

CAD Note:
Place resistors near FPGA side.

TP31 TP32 TP33 TP34
MIPI_TX_DATA_LP_P4
MIPI_TX_DATA_HS_P4
MIPI_TX_DATA_HS_N4
MIPI_TX_DATA_LP_N4
R49 100.0
R53 150
R56 150
R59 100.0
R52 100.0
R57 100.0
MIPI_TX_DATA4P
MIPI_TX_DATA4N

Pull-up Options for MIPI TX

1.8V 3.3V
R68 DNI R303 DNI
MIPI_TX_CMOS_SCLK_1V8
MIPI_TX_CMOS_SCLK_3V3
R294 DNI
R302 DNI
MIPI_TX_CMOS_SCLK

1.8V 3.3V
R305 DNI R306 DNI
MIPI_TX_CMOS_SDATA_1V8
MIPI_TX_CMOS_SDATA_3V3
R307 DNI
R304 DNI
MIPI_TX_CMOS_SDATA

1.8V 3.3V
R308 DNI R309 DNI
MIPI_TX_CMOS_RST_1V8
MIPI_TX_CMOS_RST_3V3
R312 DNI
R313 DNI
MIPI_TX_CMOS_RST_IO
C28 DNI

LI-USB3 CSI-2 TX Interface

MIPI_TX_CLK_HS_P 4
MIPI_TX_CLK_HS_N 4
MIPI_TX_DATA_HS_P[1:4] 4
MIPI_TX_DATA_HS_N[1:4] 4
MIPI_TX_CLK_LP_P 5
MIPI_TX_CLK_LP_N 5
MIPI_TX_DATA_LP_P[1:4] 5
MIPI_TX_DATA_LP_N[1:4] 5
MIPI_TX_CMOS_RST_1V8 4
MIPI_TX_CMOS_RST_3V3 7
MIPI_TX_CMOS_SCLK_1V8 4
MIPI_TX_CMOS_SCLK_3V3 7
MIPI_TX_CMOS_SDATA_1V8 4
MIPI_TX_CMOS_SDATA_3V3 7
MIPI_TX_CLK24MHz 19
MIPI_TX_GPIO1 4
MIPI_TX_GPIO2 4
MIPI_TX_GPIO3 4
MIPI_TX_GPIO4 4
MIPI_TX_GPIO5 4

3.3V R61 DNI 3.3V_MIPITX
1.8V R64 DNI 1.8V_MIPITX
C30 DNI
C29 DNI

CAD Note:
Place C29 and C30 near J1 connector.

J1
SP4 G4 SP3 G3 SP2 G2 SP1 G1
MIPI_TX_DATA1P MIPI_TX_DATA1N
MIPI_TX_CLKP MIPI_TX_CLKN
MIPI_TX_DATA2P MIPI_TX_DATA2N
MIPI_TX_DATA3P MIPI_TX_DATA3N
MIPI_TX_DATA4P MIPI_TX_DATA4N
MIPI_TX_CMOS_RST_IO
MIPI_TX_CMOS_SDATA
MIPI_TX_CMOS_SCLK
MIPI_TX_CLK24MHz
MIPI_TX_GPIO1_IO
MIPI_TX_GPIO2_IO
MIPI_TX_GPIO3_IO
MIPI_TX_GPIO4_IO
MIPI_TX_GPIO5_IO
MIPI_TX_GPIO1 R273 DNI
MIPI_TX_GPIO2 R274 DNI
MIPI_TX_GPIO3 R275 DNI
MIPI_TX_GPIO4 R276 DNI
MIPI_TX_GPIO5 R277 DNI
FFC_CONN_1x36

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MIPI CSI-2 RX D-PHY OV10640

CAD Note:
Place resistors near FPGA side.

R71 100.0 TP67 OV10640_CLK_LP_P
OV10640_CLK_HS_P
R73 200
R75 200 C31 100 pF
OV10640_CLK_HS_N
TP68
R77 100.0 OV10640_CLK_LP_N

CAD Note:
Place resistors near FPGA side.

R72 100.0 TP57 OV10640_DATA_LP_P3
OV10640_DATA_HS_P3
R74 200
R76 200 C32 100 pF
OV10640_DATA_HS_N3
TP60
R78 100.0 OV10640_DATA_LP_N3

CAD Note:
Place resistors near FPGA side.

R79 100.0 TP45 OV10640_DATA_LP_P1
OV10640_DATA_HS_P1
R81 200
R83 200 C33 100 pF
OV10640_DATA_HS_N1
TP48
R86 100.0 OV10640_DATA_LP_N1

CAD Note:
Place resistors near FPGA side.

R80 100.0 TP63 OV10640_DATA_LP_P4
OV10640_DATA_HS_P4
R82 200
R84 200 C34 100 pF
OV10640_DATA_HS_N4
TP66
R85 100.0 OV10640_DATA_LP_N4

CAD Note:
Place resistors near FPGA side.

R87 100.0 TP50 OV10640_DATA_LP_P2
OV10640_DATA_HS_P2
R88 200
R90 200 C35 100 pF
OV10640_DATA_HS_N2
TP54
R93 100.0 OV10640_DATA_LP_N2

1.8V
R91 2.0K
R92 2.0K
R89 2.0K
OV10640_CMOS_SDATA
OV10640_CMOS_SCLK
OV10640_CMOS_RST
C36 DNI

OV10640_24MHz R94 DNI

1.8V R246 0 C171 10uF
3.3V R247 0 C172 10uF

CAD Note:
Place capacitors near J2 connector.

OV10640 CSI-2 RX Interface

OV10640_CLK_HS_P 8
OV10640_CLK_HS_N 8
OV10640_DATA_HS_P[1:4] 5
OV10640_DATA_HS_N[1:4] 5
OV10640_CLK_LP_P 6
OV10640_CLK_LP_N 6
OV10640_DATA_LP_P[1:4] 6
OV10640_DATA_LP_N[1:4] 6
OV10640_CMOS_RST 4
OV10640_CMOS_SCLK 4
OV10640_CMOS_SDATA 4
OV10640_24MHz 8
OV10640_GYRO_INT 4
OV10640_G_RDY 4
OV10640_XM_INT2 4
OV10640_XM_INT1 4
OV10640_FSIN 4

J2
SP4 G4
SP3 G3
SP2 G2
SP1 G1
1.8V_OV10640
3.3V_OV10640
FFC_CONN_1x36

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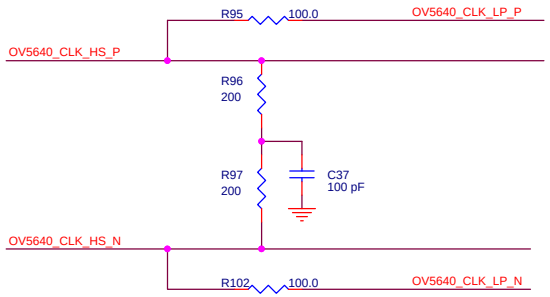
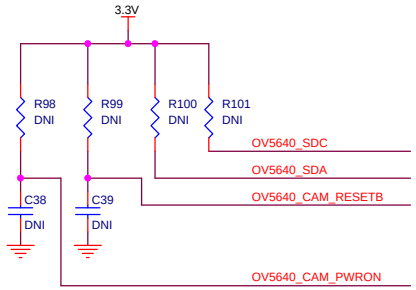
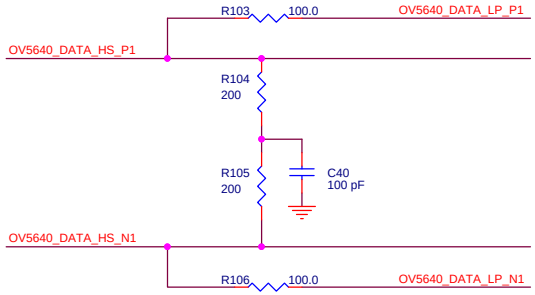
MIPI CSI-2 RX D-PHY OV5640

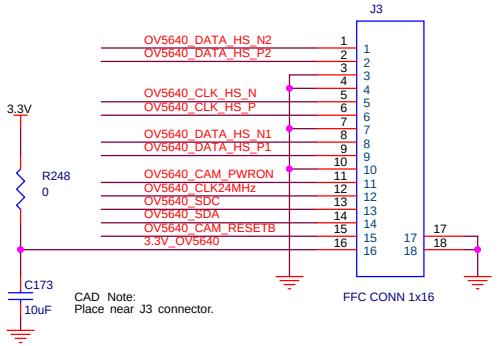
CAD Note:
Place resistors near FPGA side.





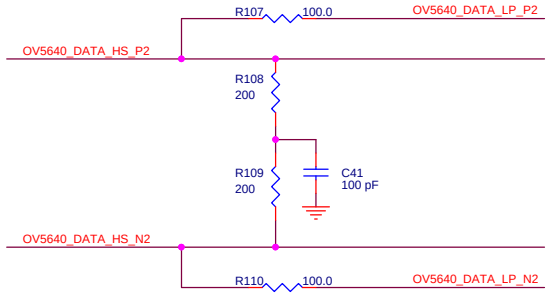
CAD Note:
Place resistors near FPGA side.



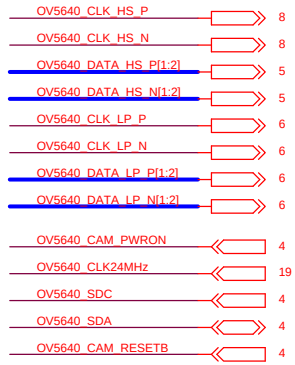


CAD Note:
Place near J3 connector.

CAD Note:
Place resistors near FPGA side.



OV5640 CSI-2 RX Interface



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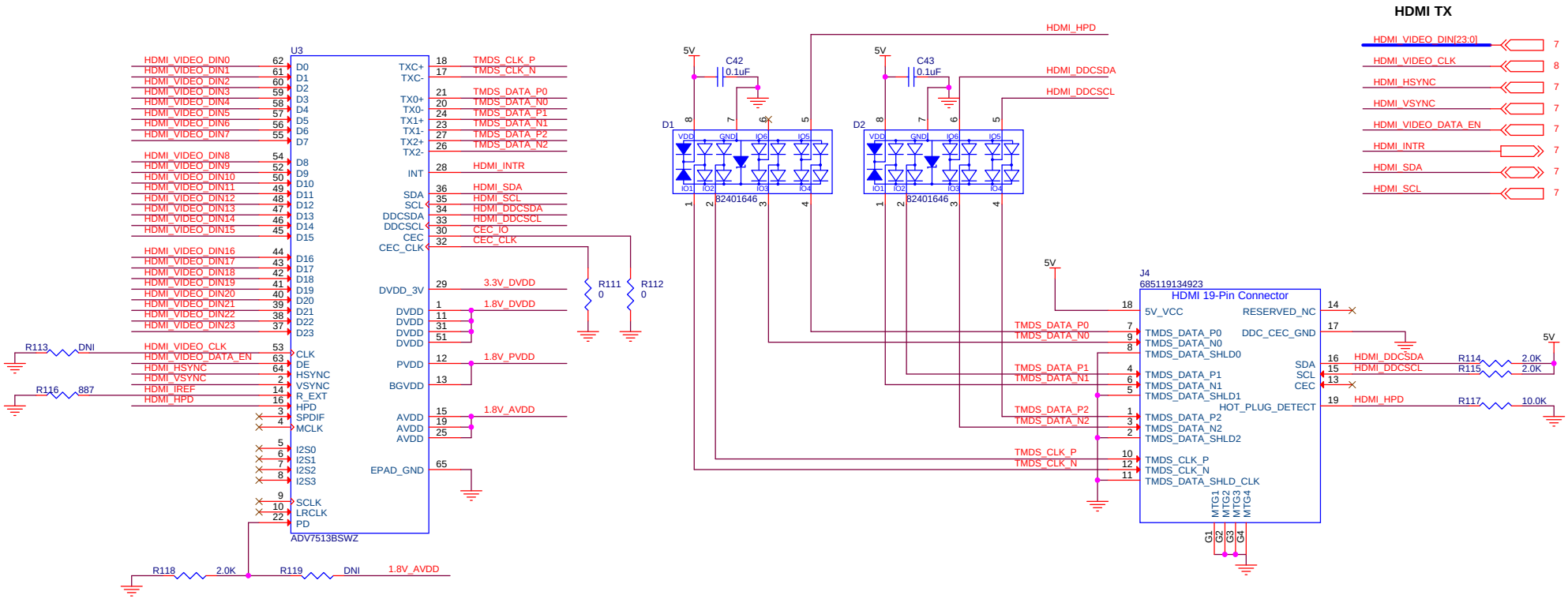
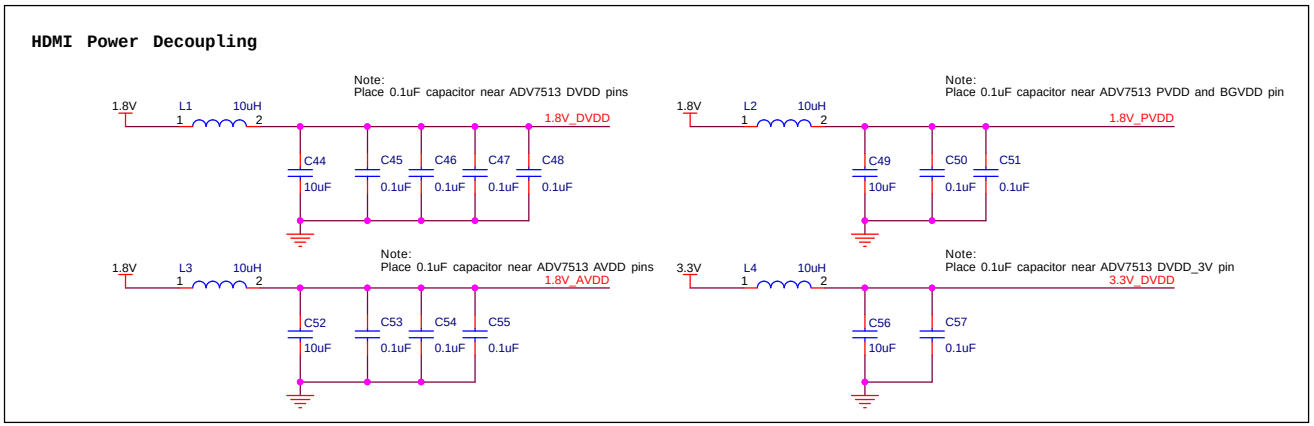
HDMI (VIDEO ONLY)



HDMI Power Decoupling



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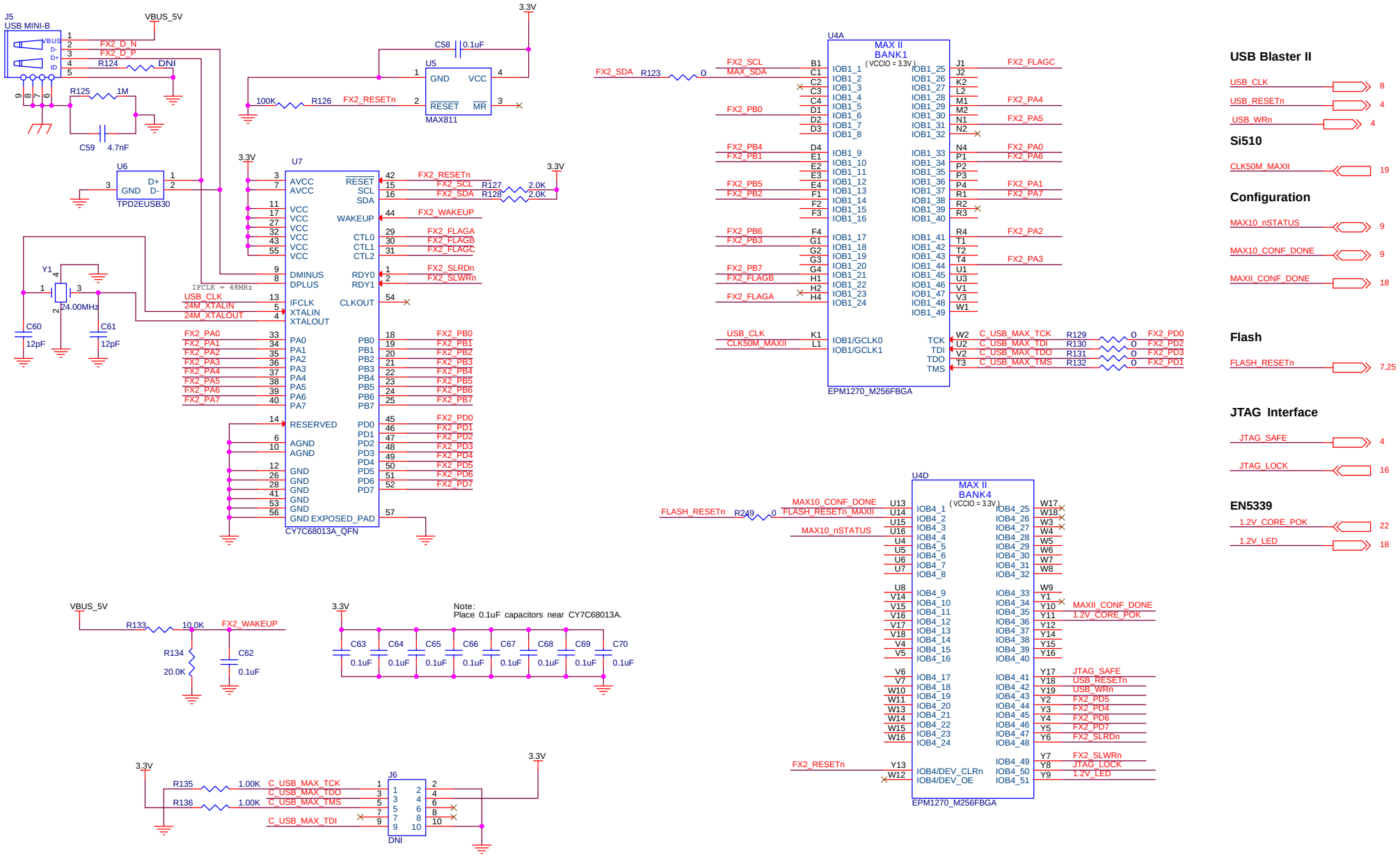
ON-BOARD USB BLASTER II-1



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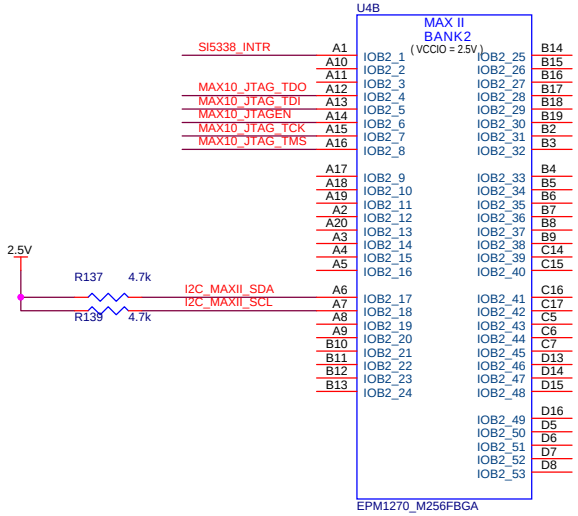
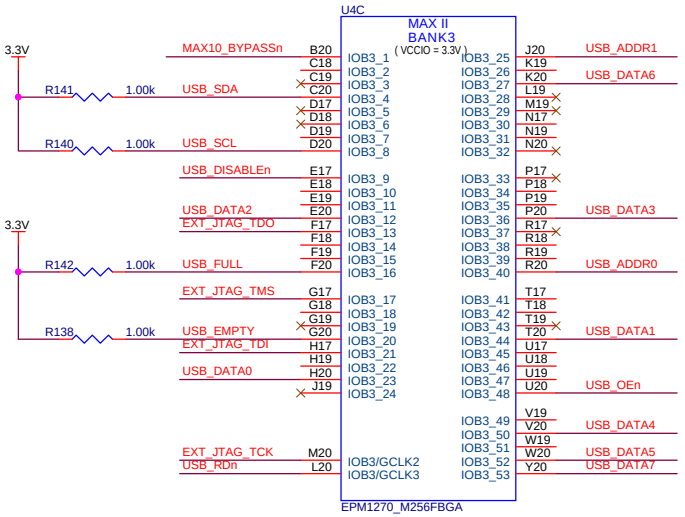
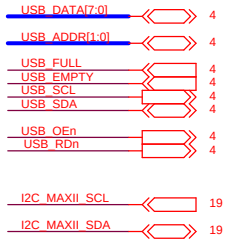
ON-BOARD USB BLASTER II-2

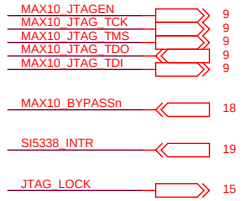


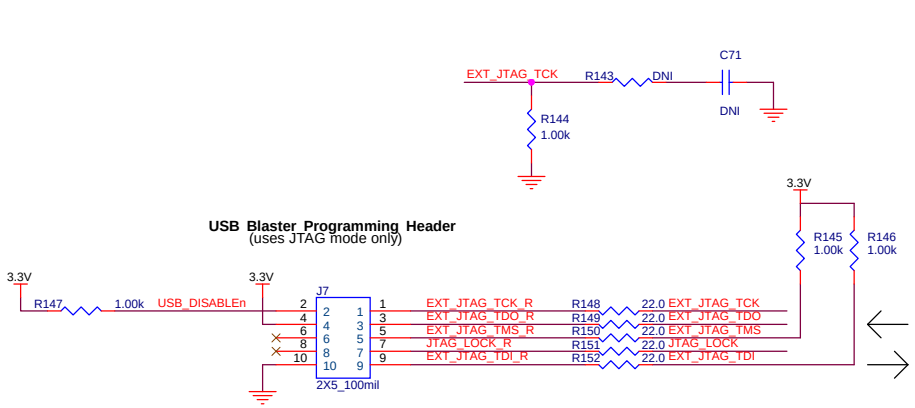


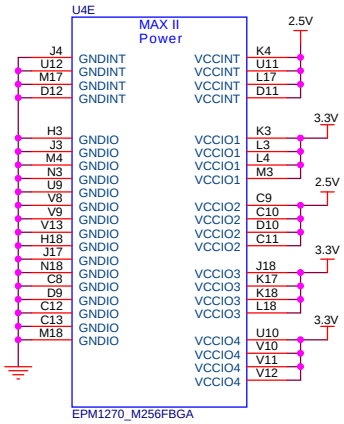
MAX10 USB Interface



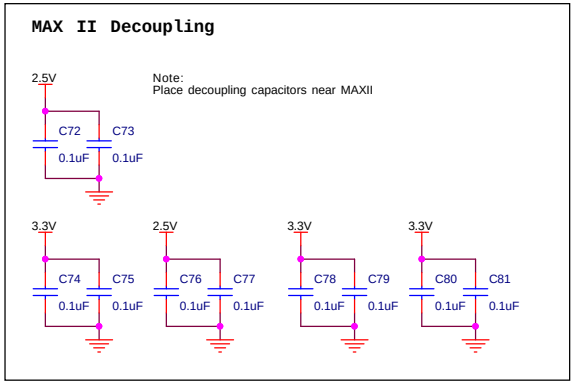
JTAG Interface







MAX II Decoupling



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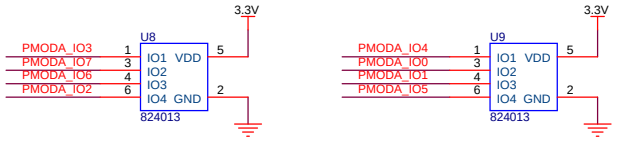
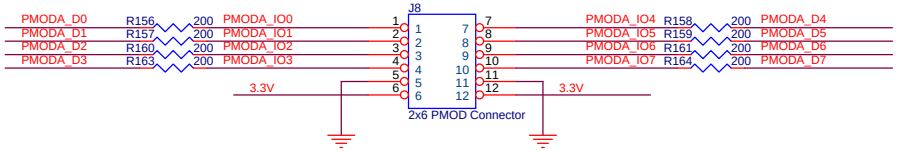
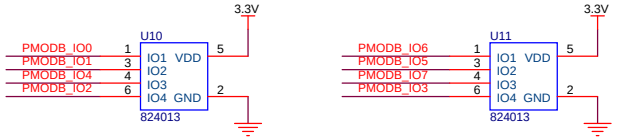
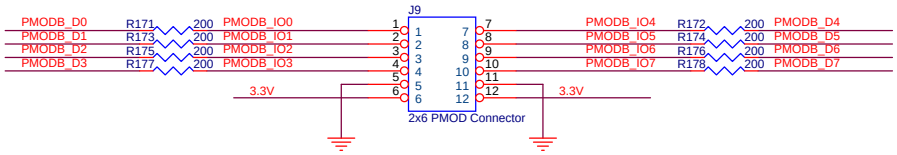
PMOD, GPIO, LVDS USER IO

PMOD

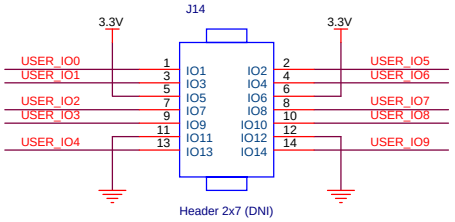






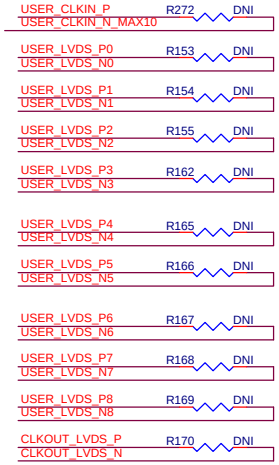


User GPIO

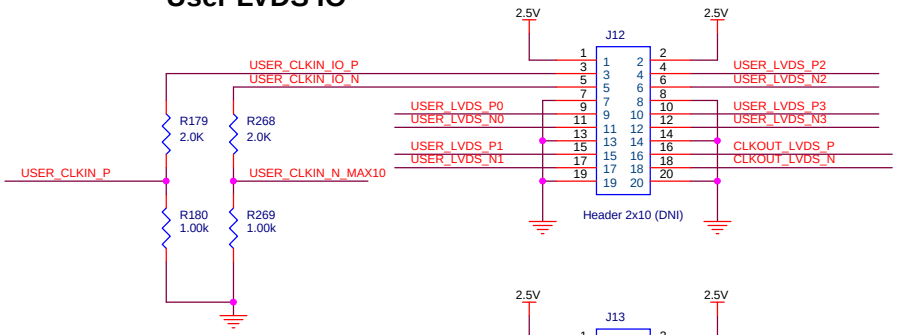


LVDS Termination

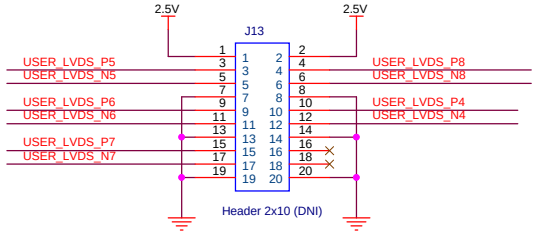
Note: Place near MAX 10 side.

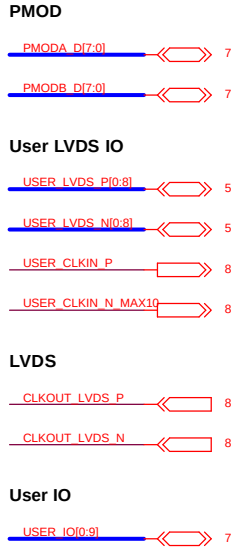


User LVDS IO



Note: USER_CLKIN_IO_P is used if external single-ended clk needs to use on-chip PLL resource. USER_CLKIN_IO_P/N is used for external differential clk input. Values of R179,R180,R268, and R269 might be adjusted according to user input voltage.





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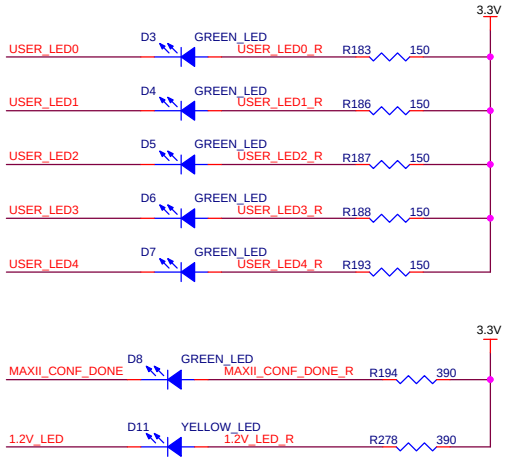
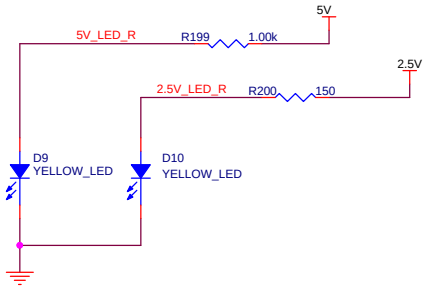
PUSHBUTTON, SWITCH, LED

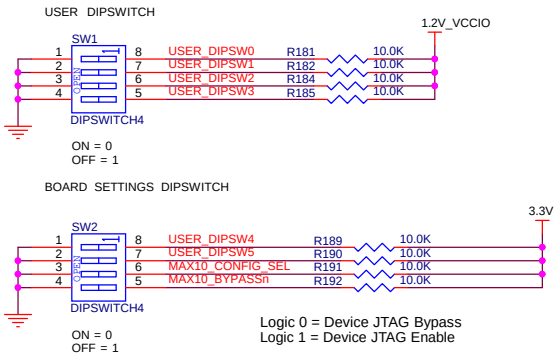
User LED



Power LED



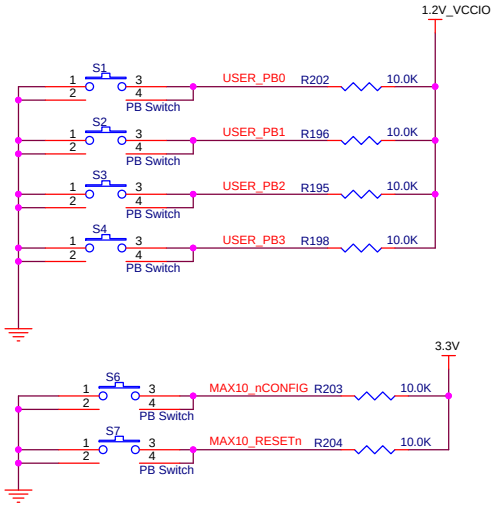
User DIP Switch



Logic 0 = Device JTAG Bypass
Logic 1 = Device JTAG Enable

Note: MAX10_BYPASSn is used to bypass the virtual JTAG device provided within the On-Board USB-Blaster II.

User Pushbutton



MAXII

MAXII_CONF_DONE 15
1.2V_LED 15

User LED

USER_LED[0:4] 7

User Pushbutton

USER_PB[0:3] 6
MAX10_nCONFIG 9
MAX10_RESETn 9

User DIP Switch

USER_DIPSW[0:3] 6
USER_DIPSW[4:5] 4
MAX10_CONFIG_SEL 9
MAX10_BYPASSn 16

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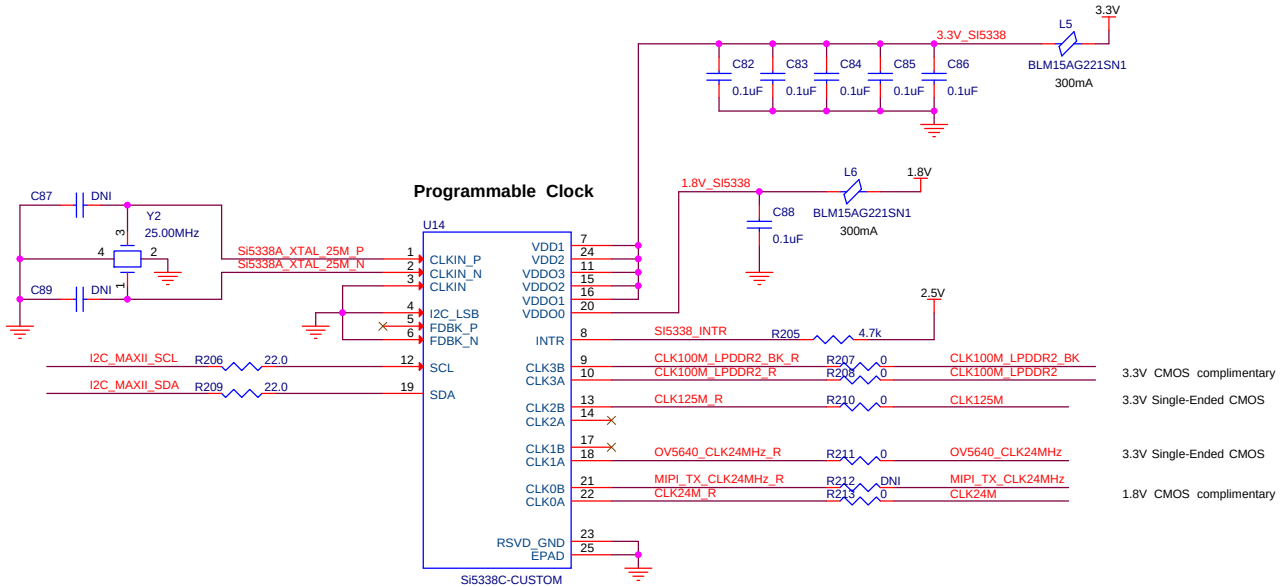
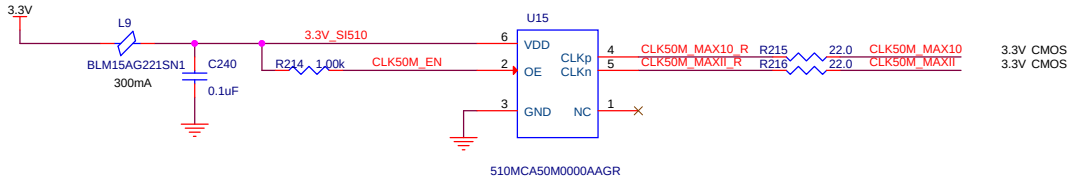
CLOCKING



Notes:
Use Clock Control GUI to program Si5338 oscillator outputs.
(Defaults 100MHz, 125MHz, 24MHz, 24MHz)

I2C Address 70 HEX



MAX 10

CLK50M_MAX10 8
CLK24M 8
CLK125M 8
CLK100M_LPDDR2 8
CLK100M_LPDDR2_BK 8
SI5338_INTR 16

MAXII

CLK50M_MAXII 15
I2C_MAXII_SCL 16
I2C_MAXII_SDA 16

DM385 CSI-2 TX Interface

OV5640_CLK24MHz 13
MIPI_TX_CLK24MHz 11

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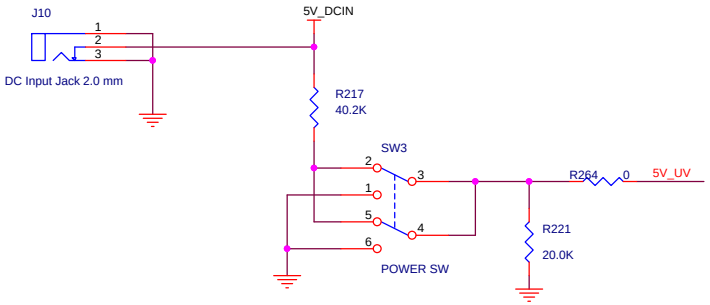
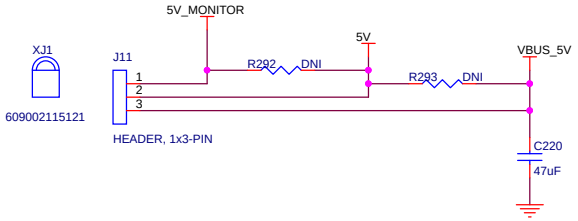
HOT SWAP and POWER 3.3V

5V
DC Input

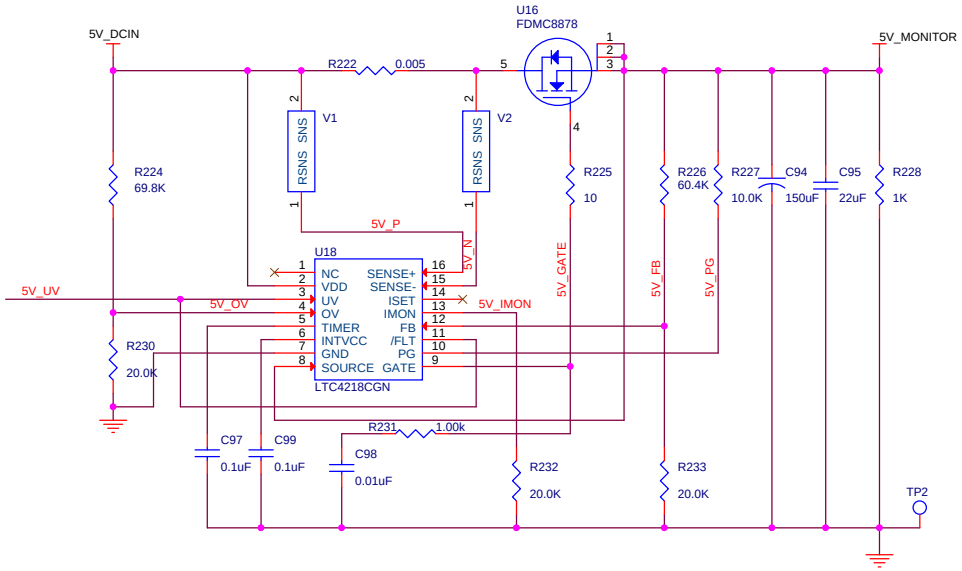




CAUTION:
When NOT using jumpers,
solder R292 for power input from DC Jack,
or solder R293 for USB power.
SOLDER ONLY ONE POWER OPTION,
AND SUGGEST NOT TO USE WITH JUMPER.

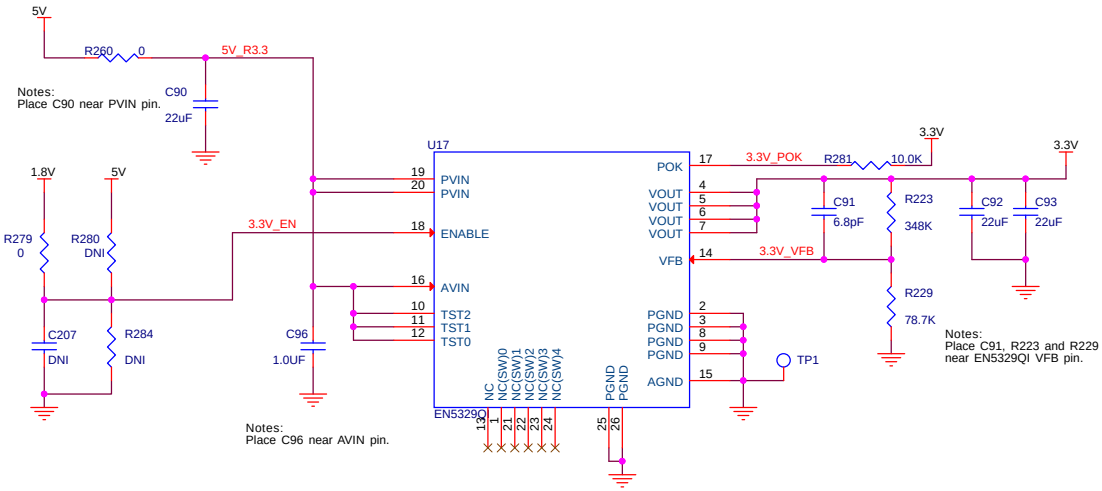
EN5329

Hot Swap for DC Plug



Hot Swap Controller Circuit

POWER 3.3V



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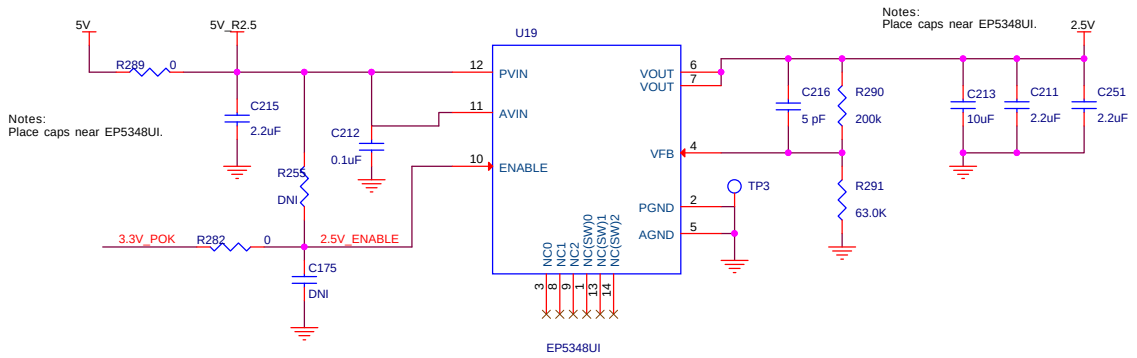
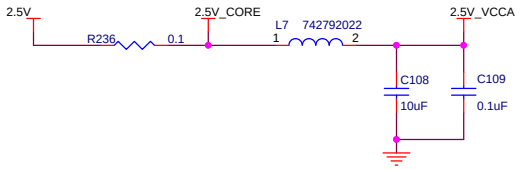
POWER 2.5V & 1.8V

POWER 2.5V

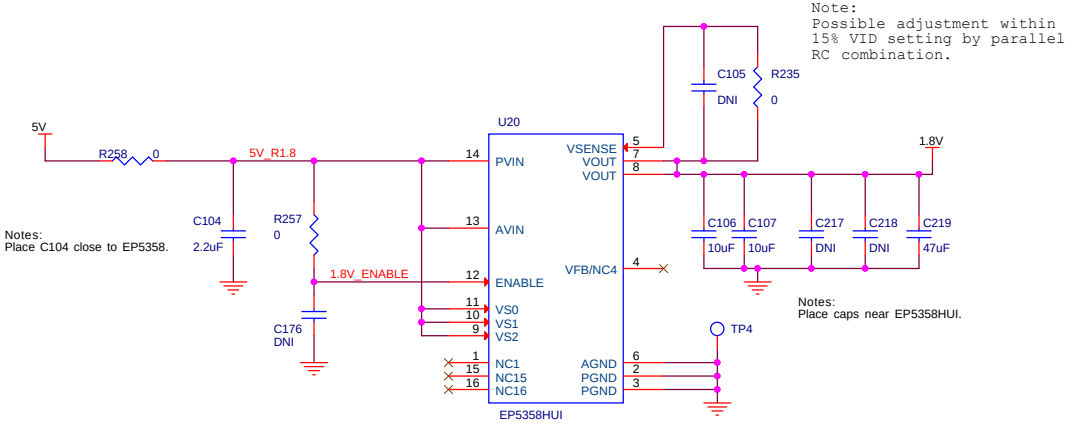


EN5329

POWER 2.5V_VCCA



POWER 1.8V



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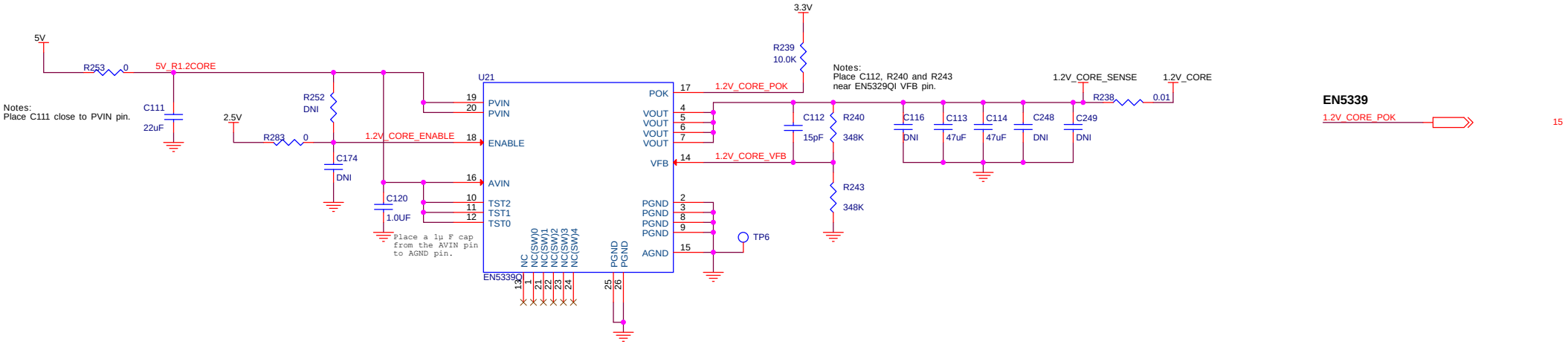
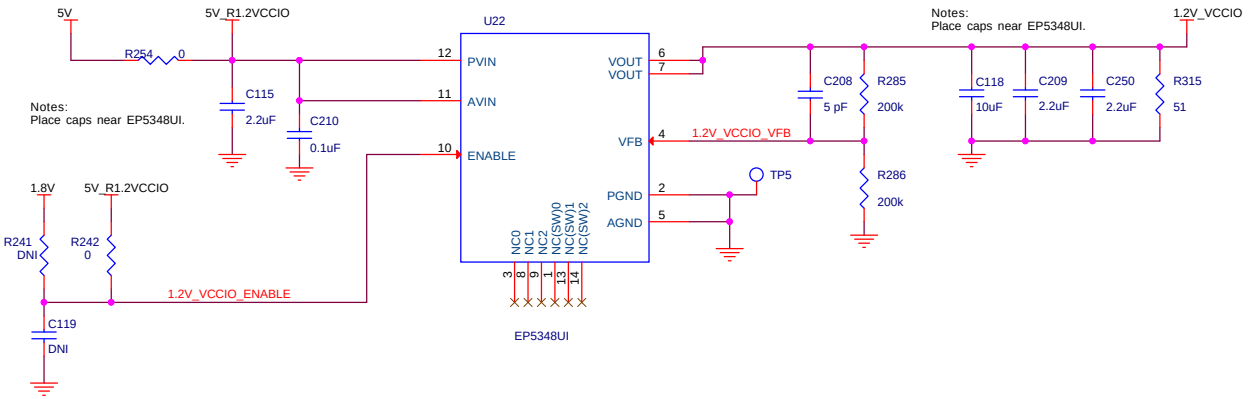
POWER 1.2V

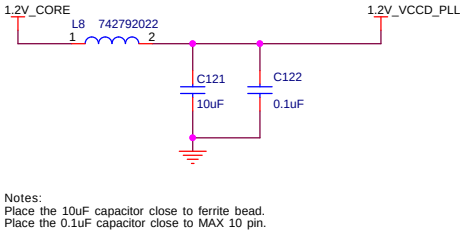
POWER 1.2V_CORE



POWER 1.2V_VCCIO



POWER 1.2V_VCCD_PLL



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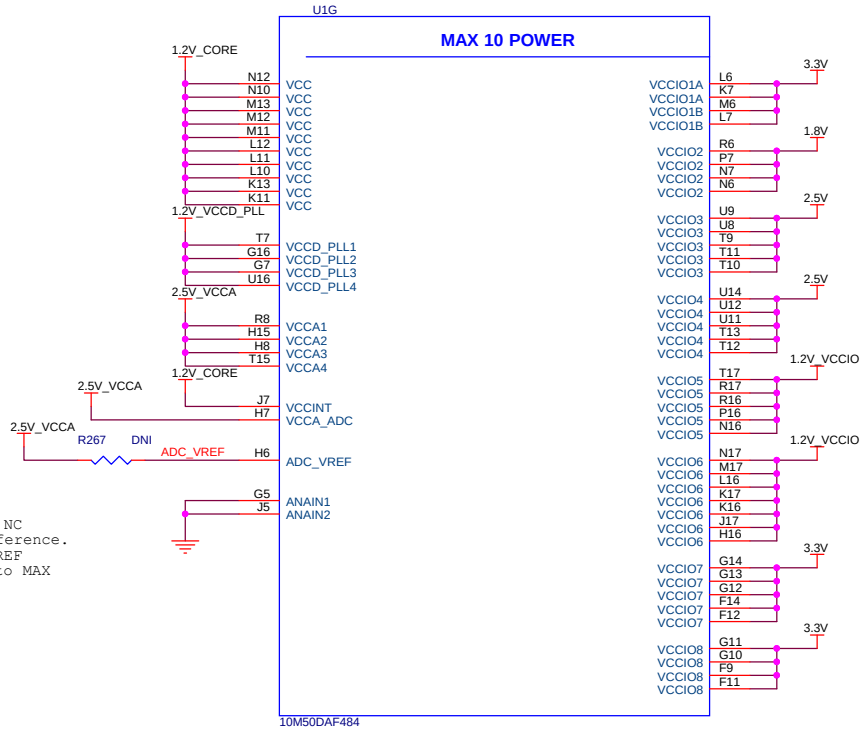
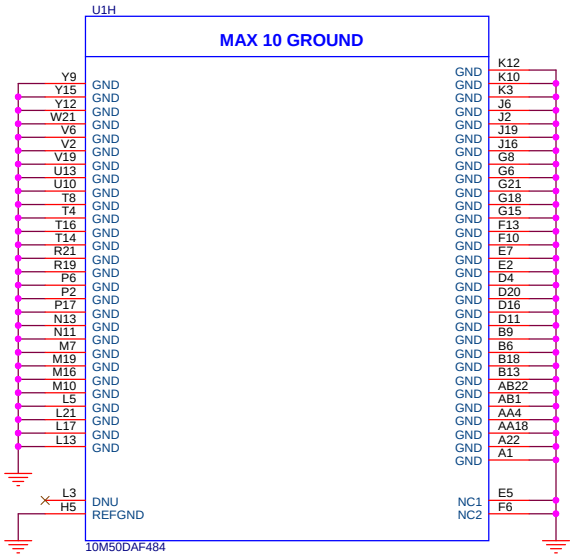
MAX 10 POWER & GROUND

Note:
According to MAX 10 pin connection guideline PCG-01018-1.2, "Tie the VCCINT pin to any 1.2V power domain if you are not using ADC." Therefore, connect VCCINT to 1.2V_CORE for DC or DF production device migration.

Note:
According to MAX 10 pin connection guideline PCG-01018-1.2, "Tie the VCCA_ADC pin to any 2.5V power domain if you are not using ADC, and do not tie the VCCA_ADC pin to GND." Therefore, connect VCCA_ADC to 2.5V_CORE for DC or DF production device migration.

Note:
For ES device, connect ADC_VREF to NC when not using external voltage reference. For DC/DF production device, ADC_VREF pin is migrated to VCCA according to MAX 10 Errata.





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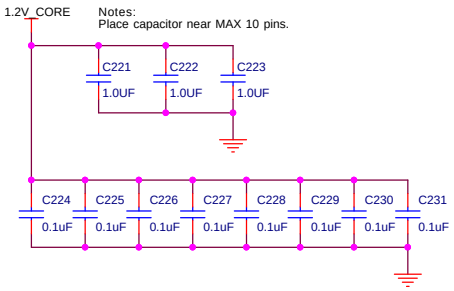
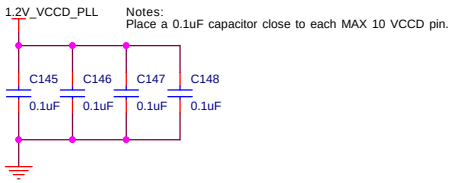
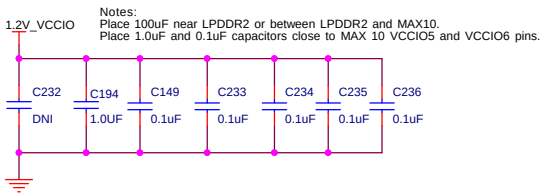
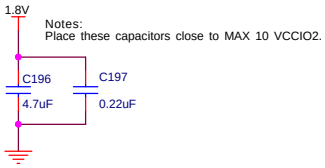
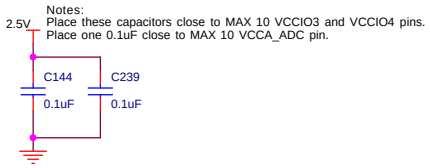
DECOUPLING

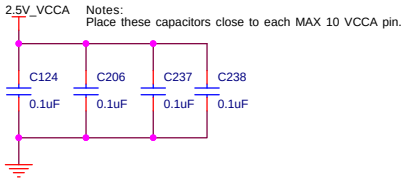


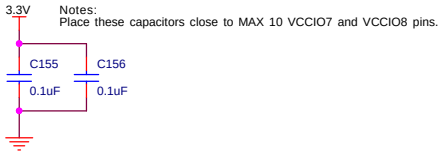












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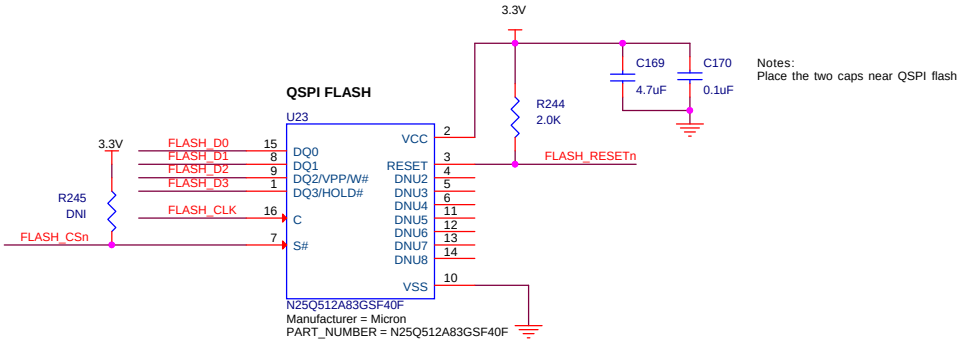
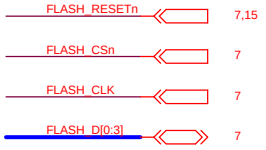
QSPI FLASH





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