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NOTES UNLESS OTHERWISE SPECIFIED:

1. PCB VENDOR MUST NOTIFY RESPONSIBLE INTEL PCB CONTACT OF ANY DISCREPANCIES FOUND BETWEEN FABRICATION DATA AND FABRICATION DRAWING NOTES.
2. THIS DRAWING IS VIEWED FROM THE PRIMARY OR TOP SIDE OF THE PCB.
3. FABRICATION OF THIS PCB SHALL BE IN CONFORMANCE WITH THE FOLLOWING SPECIFICATIONS: IPC-6012 CLASS 2 (LATEST REVISION).
4. FABRICATION OF THIS PCB TO BE ACCEPTABLE TO IPC-A-600 CLASS 2 (LATEST REVISION).
5. ALL MATERIALS USED MUST BE RoHS COMPLIANT.
6. ALL DIMENSIONAL LIMITS APPLY AFTER PLATING OR PROCESSING.
7. TOLERANCES OF DATUM HOLE TO: BOARD EDGE LOCATIONS +/- 0.010

   V-SCORE LOCATIONS +/- 0.010
8. MATERIALS TO BE HIGH PERFORMANCE FR4 GLASS EPOXY PANASONIC R 5775K MEGTRON 6 & DUPONT HK-4 WITH SVLP/HVLP COPPER FOIL. MIN. Tg OF 210 DEGREES C.
9. FLAME CLASS: UL 94V-0 & MUST MEET REQUIREMENTS OF UL796.
10. MANUFACTURER MUST BE UL RECOGNIZED TO PRODUCE THIS PRODUCT SUCH THAT IT MEETS 170 DEGREES CELSIUS MAXIMUM OPERATING TEMPERATURE (MOT).
11. THE FOLLOWING MUST BE MARKED OR ETCHED ON SECONDARY SIDE OF PCB IN AREA SHOWN:
    a) DATE CODE.
    b) UL RECOGNIZED VENDOR ID, UL TYPE DESIGNATION AND/OR MARKINGS WHICH REFLECT THE SPECIFIED FLAME CLASS AND MAXIMUM OPERATING TEMPERATURE RATINGS.
12. PCB VENDOR TO ENSURE ALL UNCONNECTED (NON-FUNCTIONAL) INTERNAL SIGNAL LAYER PADS AND VIAS ARE REMOVED.
13. HOLE/SLOT PLATING = 0.001 MIN. AVERAGE / 0.0008 ABSOLUTE MIN. UNLESS OTHERWISE SPECIFIED, ALL DRILL TABLE DIAMETERS ARE FINISHED HOLE SIZE.
14. A. THESE HOLES MUST BE FILLED USING NON-CONDUCTIVE FILL
    B. THESE HOLES MUST BE SOLID COPPER FILLED AND PLANARIZED.
    C. VIA IN PAD : MUST BE SOLID COPPER FILLED AND PLANARIZED.
15. PLEASE REFERENCE ATTACHED DOCUMENT FOR SPECIFIC THIEVING GUIDELINES.
16. SMEAR REMOVAL SHALL NOT ETCHBACK GREATER THAN 0.001.
17. FINISHED CONDUCTOR WIDTH NOT TO BE REDUCED MORE THAN 20% OF MINIMUM WIDTH FROM ARTWORK SUPPLIED. FINISHED CONDUCTOR SPACING NOT TO BE REDUCED MORE THAN 20% OF MINIMUM SPACING FROM ARTWORK SUPPLIED.
18. CONTACT FINGERS SHALL BE GOLD PLATED 30 MICRO INCHES OVER 200 MICRO INCHES NICKEL. EDGES AT CONTACT FINGERS ARE TO BE BEVELED BOTH SIDES 20 X .051.
19. SOLDER MASK IS LIQUID PHOTO IMAGEABLE AND IN ACCORDANCE WITH IPC-SM-840C CLASS T. FINISH MUST BE GREEN AND GLOSSY. REGISTRATION TO BE WITHIN +/- 0.003 OF ITS RESPECTIVE OUTER CIRCUIT LAYERS. VENDOR MAY ADJUST SOLDERMASK WHEREVER SOLDERMASK PADS ARE THE SAME SIZE (1:1) TO PROVIDE UP TO .003 MAXIMUM CLEARANCE FROM MASK TO PAD PROVIDED NO ADJACENT COPPER IS EXPOSED. NO "VIA TENTING/PLUGGING IS ALLOWED WITHOUT PRIOR CONSENT OF INTEL.
20. PCB VENDOR TO ENSURE ALL VIAS ARE COMPLETELY FREE OF SOLDERMASK ON BOTTOM SIDE OF PCB WITH THE EXCEPTION OF VIAS UNDER COMPONENTS ON BOTTOM SIDE.
21. PCB FINISH BOTH SIDES TO BE ELECTROLESS NICKEL (Ni) FOLLOWED BY IMMERSION GOLD (AU) (ENIG) ACCEPTABLE TO IPC-4552.
22. REMOVE ALL SHARP EDGES AND BURRS 0.003" MAXIMUM.
23. SILKSCREEN USING WHITE NONCONDUCTIVE INK. NO INK TO APPEAR ON EXPOSED COPPER SUCH AS PLATED THROUGH HOLE PADS AND SURFACE MOUNT LANDS. INK ON SOLDER MASK COVERED PADS IS PERMISSIBLE. CLIPPING OF SILKSCREEN 0.008 MAX. FROM PADS IS PERMITTED.
24. BOW & TWIST SHALL BE DETERMINED BY PHYSICAL MEASUREMENT AND PERCENTAGE CALCULATION IN ACCORDANCE WITH IPC-TM-650, METHOD 2.4.22. BOW AND TWIST MAY NOT EXCEED 0.7%
25. 100% CONTINUITY AND ISOLATION ELECTRICAL TESTING PER CURRENT IPC TEST METHODS REQUIRED FOR EVERY PCB. FINAL PCB TEST DATA MUST BE CROSS-REFERENCED TO IPC-D-356 FILE, NEUTRAL FILE OR NETLIST PROVIDED.
26. CONTROLLED IMPEDANCE TRACES ARE AS FOLLOWS. DESIGNATED WIDTHS ARE DEFINED FOR ALL LAYERS, BUT MAY NOT ACTUALLY EXIST ON STATED LAYERS.
    a) TOLERANCE ON ALL LINES, UNLESS OTHERWISE SPECIFIED +/-8%.
    b) SINGLE ENDED TRACES (.00625) -LYRS 1 & 18 TO BE 50 OHMS.
    c) SINGLE ENDED TRACES (.0031) -LYRS 3 & 16 TO BE 50 OHMS.
    d) SINGLE ENDED TRACES (.0044) -LYRS 6, 7, 12 & 13 TO BE 50 OHMS
    e) SINGLE ENDED TRACES (.0105) -LYR 1 TO BE 75 OHMS.
    f) EDGE COUPLED TRACES (.006 -.011 CENTERS), LYR 1 & 18 TO BE 85 OHMS.
    g) EDGE COUPLED TRACES (.0040 -.011 CENTERS), LYR 3 TO BE 85 OHMS.
    h) EDGE COUPLED TRACES (.0040 -.009 CENTERS), LYR 1 & 18 TO BE 100 OHMS.
    i) EDGE COUPLED TRACES (.0030 -.011 CENTERS), LYR 3 & 16 TO BE 100 OHMS.
    j) EDGE COUPLED TRACES (.0040 -.011 CENTERS), LYR 6, 7, 12, 13 TO BE 100 OHMS.
27. PCB VENDOR TO PROVIDE ONE TEST COUPON AND ONE CROSS SECTION PER LOT WITH SHIPMENT.
28. PCB VENDOR TO PROVIDE 2 SOLDER SAMPLES WITH FIRST SHIPMENT. SOLDER SAMPLE MARKINGS OR STICKERS CAN NOT BE ON PCB. A HANG TAG IS ACCEPTABLE.
29. VENDOR TO KEEP QUALITY CONTROL INK STAMPINGS AND VENDOR ETCH/SILK LOGOS ON BOTTOM OF PCB IN AREA SPECIFIED.
30. DETAILS NOT SPECIFIED ARE AT MANUFACTURER'S OPTION, HOWEVER FINAL APPROVAL MUST BE OBTAINED FROM INTEL.

DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

	FIGURE	SIZE	TOLERANCE	PLATED	QTY
14-B	•	9.0	+2.0/-9.0	PLATED	3243
14-A	·	10.0	+3.0/-10.0	PLATED	2826
14-A	•	12.0	+3.0/-12.0	PLATED	2032
	⊕	20.0	+3.0/-3.0	PLATED	7
	⊕	22.0	+3.0/-3.0	PLATED	20
	⊕	30.0	+3.0/-3.0	PLATED	2
	′	31.0	+3.0/-3.0	PLATED	6
	G	31.496	+3.0/-3.0	PLATED	16
	"	35.0	+3.0/-3.0	PLATED	10
	⊕	40.0	+3.0/-3.0	PLATED	4
	⊕	41.339	+1.969/-1.969	PLATED	11
	K	47.0	+3.0/-3.0	PLATED	2
	L	62.0	+3.0/-3.0	PLATED	2
	⊠	67.0	+3.0/-3.0	PLATED	8
	⊠	70.0	+3.0/-3.0	PLATED	6
	⊠	71.0	+3.0/-3.0	PLATED	8
	P	106.0	+3.0/-3.0	PLATED	2
	ⓟ	125.0	+3.0/-3.0	PLATED	1
	ⓣ	149.606	+3.937/-3.937	PLATED	2
	ⓘ	165.354	+3.937/-3.937	PLATED	4
	ⓖ	188.976	+3.937/-3.937	PLATED	4
	*	40.0	+2.0/-2.0	NON-PLATED	4
	*	42.0	+2.0/-2.0	NON-PLATED	2
	*	49.0	+2.0/-2.0	NON-PLATED	1
	·	51.0	+2.0/-2.0	NON-PLATED	2
	*	61.0	+2.0/-2.0	NON-PLATED	2
	⊬	118.0	+2.0/-2.0	NON-PLATED	4
	⊬	128.0	+2.0/-2.0	NON-PLATED	2
	•	33.46x25.59	+3.0/-3.0	PLATED	2
	▪	51.181x23.622	+3.0/-3.0	PLATED	2
	∞	69.0x28.0	+3.0/-3.0	PLATED	2
	∞	93.0x36.0	+3.0/-3.0	PLATED	2

DRILL CHART: TOP to L2_GND
ALL UNITS ARE IN MILS

	FIGURE	SIZE	TOLERANCE	PLATED	QTY
14-B	·	5.0	+3.0/-5.0	PLATED	129

DRILL CHART: TOP to L3_SIG1
ALL UNITS ARE IN MILS

	FIGURE	SIZE	TOLERANCE	PLATED	QTY
14-B	·	5.0	+3.0/-5.0	PLATED	316

DRILL CHART: L2_GND to L17_GND
ALL UNITS ARE IN MILS

	FIGURE	SIZE	TOLERANCE	PLATED	QTY
14-B	·	8.0	+3.0/-8.0	PLATED	123

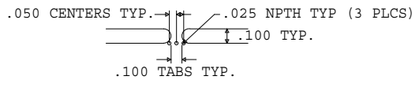
DRILL CHART: L17_GND to BOTTOM
ALL UNITS ARE IN MILS

	FIGURE	SIZE	TOLERANCE	PLATED	QTY
14-B	·	5.0	+3.0/-5.0	PLATED	126

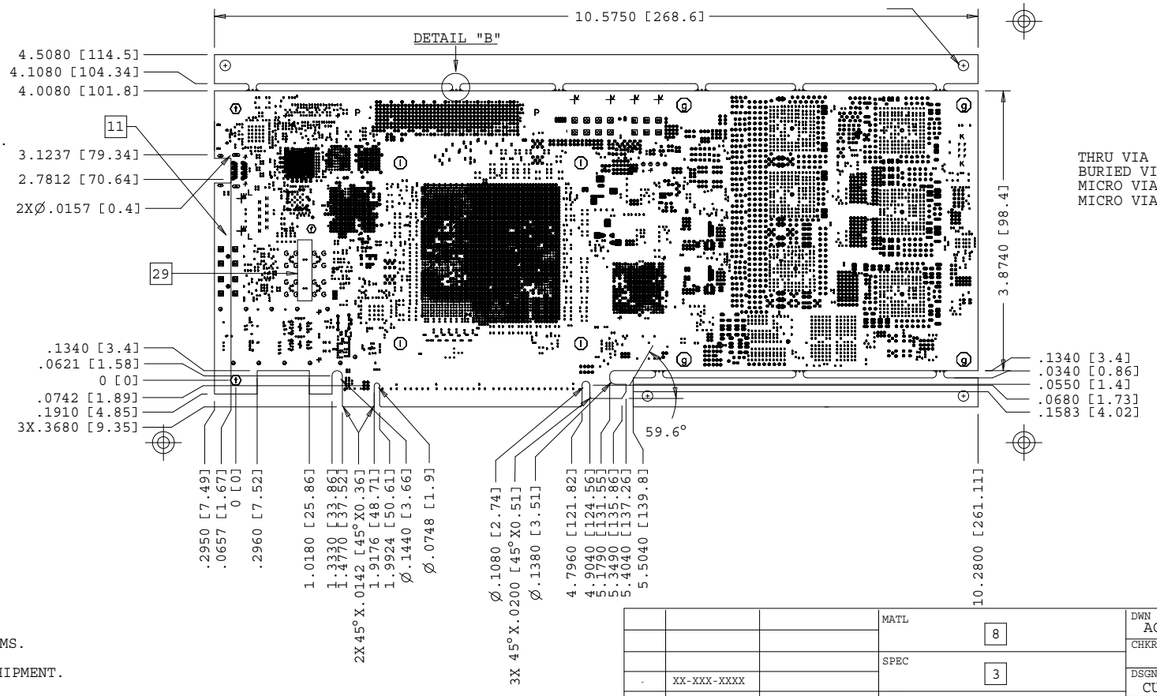
DRILL CHART: L16_SIG6 to BOTTOM
ALL UNITS ARE IN MILS

	FIGURE	SIZE	TOLERANCE	PLATED	QTY
14-B	·	5.0	+3.0/-5.0	PLATED	29

DETAIL B
SCALE: NONE



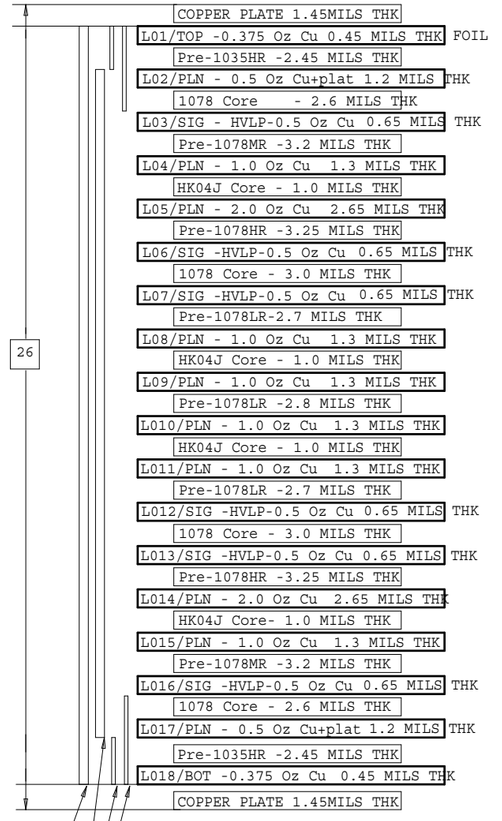
TOOLING HOLE SIZE/LOCATION DETERMINED BY FAB VENDOR (4 PLCS)



PRIMARY SIDE SHOWN

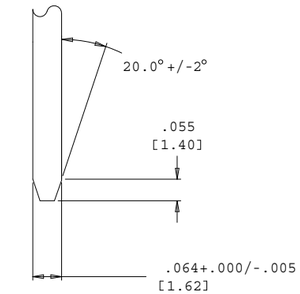
REVISIONS

REV	DESCRIPTION	DATE	APPROVED



DETAIL A
SCALE: NONE
(CROSS SECTION)

Thickness After plating .0644 +/-.005
(not including solder mask)



CHAMFER EDGE CONNECTOR
SCALE: NONE

			MATL 8
			SPEC 3
-	XX-XXX-XXXX		
DASH	NEXT ASSY	USED ON	FNSH 19 21 23
APPLICATION			

THIRD ANGLE PROJECTION

TOLERANCES: UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES IN ACCORDANCE WITH ANSI Y14.5. DRILL TOLERANCES ARE PER 10387
DEC .X ± —
DEC .XX ± .01
DEC .XXX ± .005
DEC .XXXX ± .002
FRACTIONS ± —
ANGLES ± 1°

DWN ACRONICS 07-MAR-17
CHKR
DSGN ENGR CUONG
RELEASE
CONTRACT NO. XXXXXXXX

(c) 2017 INTEL Corporation

TITLE
PCB FABRICATION
STRATIX 10 GX
FPGA DEVELOPMENT KIT

SIZE	CAGE CODE	DWG NO.	REV
D	N/A	140-0321309-D1	D1

SCALE: 1/1 SHEET 1 OF 2

REV D1 DWG NO. 140-0321309-D1