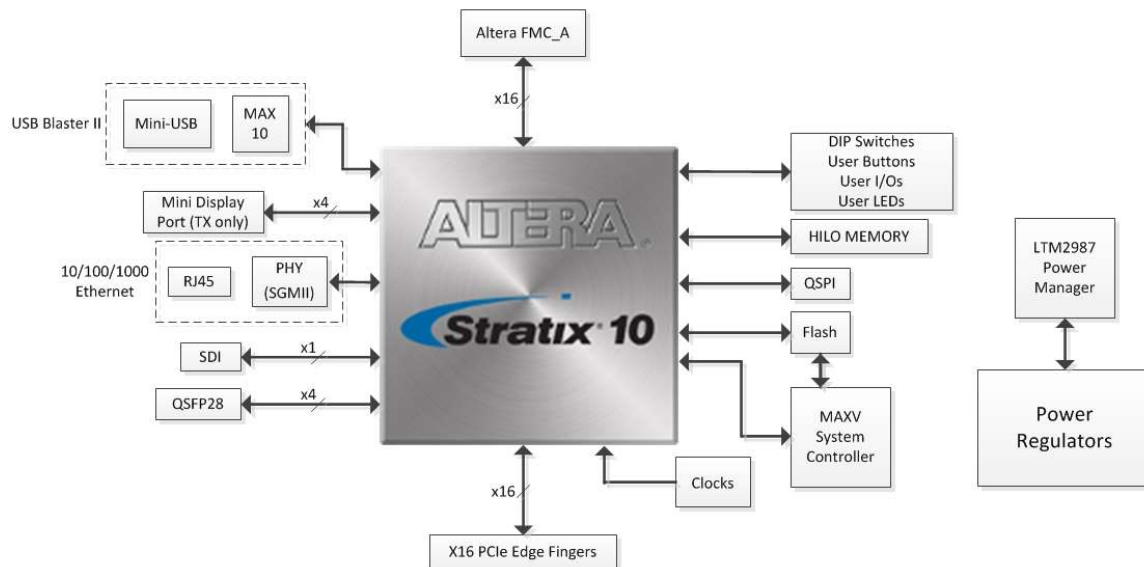


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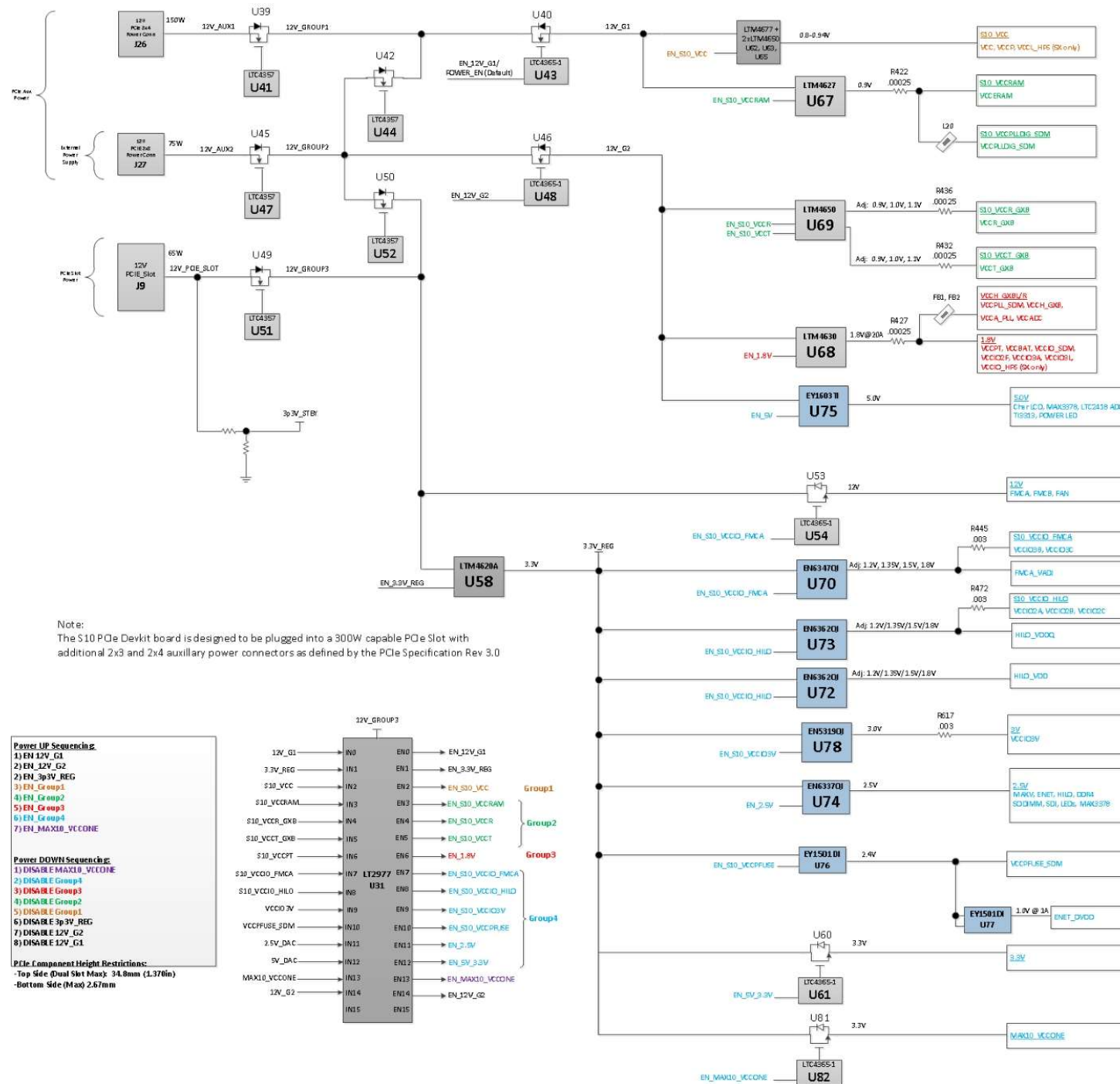
1. Project Drawing Numbers:
Raw PCB 100-0321309-D1
Gerber Files 110-0321309-D1
PCB Design Files 120-0321309-D1
Assembly Drawing 130-0321309-D1
Fab Drawing 140-0321309-D1
Schematic Drawing 150-0321309-D1
PCB Film 160-0321309-D1
Bill of Materials 170-0321309-D1
Schematic Design Files 180-0321309-D1
Functional Specification 210-0321309-D1
PCB Layout Guidelines 220-0321309-D1
Assembly Rework 320-0321309-D1



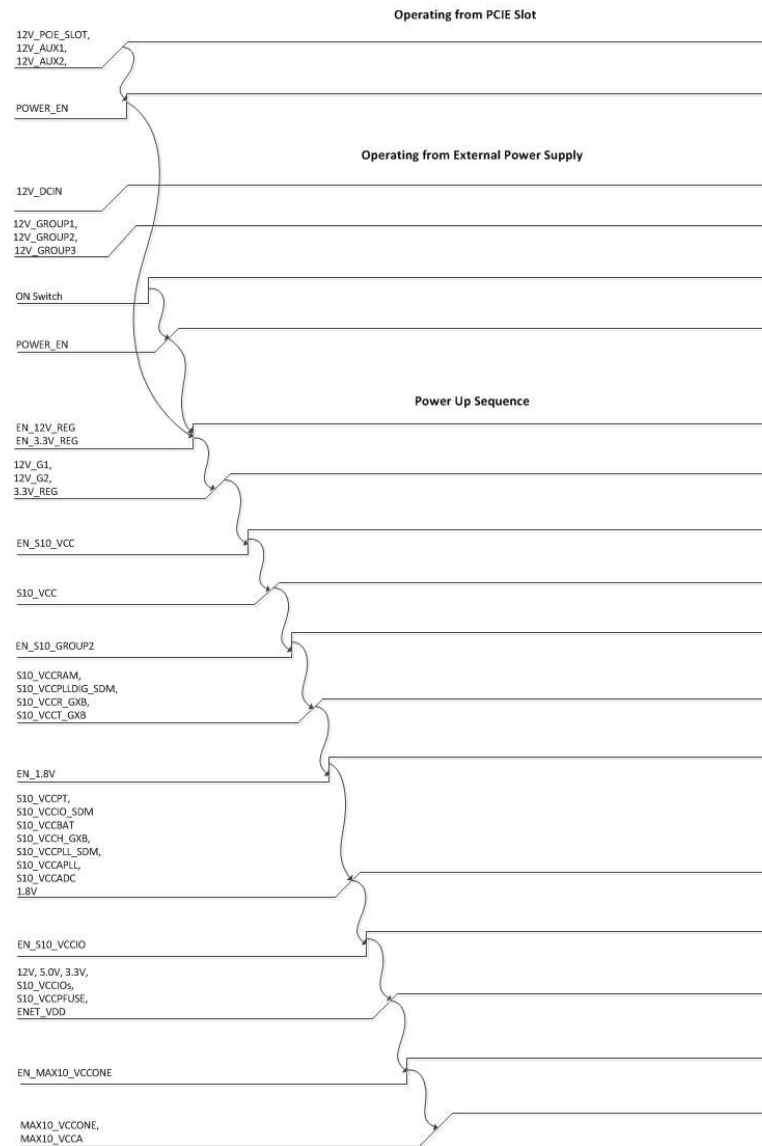
| REV | DATE | PAGES | DESCRIPTION |
|-----|------------|--------|---|
| A1 | 03/11/2016 | All | Initial Release |
| B1 | 06/15/2016 | 06 | Fix MSEL1 unconnection |
| C1 | 12/1/2016 | 06 | Remove R5372 and change R5373 to 0-ohm |
| | | 19 | Add U86. Move I2C-SCL/SDA from U85 to U86 |
| | | 28 | Update SDI BOM stuffing options for 12Gbps. Replace R164 and R165 with C873 and C874. |
| | | 30 | Add R5382, R5383 to source USB_MAX5_CLK and USB_FPGA_CLK from U23 instead of U27 |
| | | 31 | Add C372 to I2C-SCL signal near SW3.2 to GND to clean glitch |
| | | 33 | Remove power-on switch SW7.6 connection to GND |
| | | 38 | Change C428 to Conflict Mineral Free part |
| | | 40 | Add C869-C868 (100uF) for VCCT_GXB & move C454-C456 before R432 |
| | | 40 | Add C869-C871 (100uF) for VCCR_GXB & move C458-C460 before R436 |
| | | 40 | Change R437 to 180K for 700KHz switching frequency |
| | | 15, 32 | Connect core TEMPDIODE to MAX1619 |
| | | 32 | Add dedicated LDO (U87) for MAX1619 power |
| | | 32 | Connect MAX1619 OVERTEMPn to LT2987 CTRL1 to power off when overtemp occurs. |
| D1 | 3/2/2017 | | |

| PAGE | DESCRIPTION | PAGE | DESCRIPTION |
|------|----------------------------|------|----------------------------|
| 1 | Title, Note, Block Diagram | 37 | Power - VCC part 3 |
| 2 | Power Tree Diagram | 38 | Power - VCCRAM |
| 3 | Power Sequence Diagram | 39 | Power - VCCPT & 1.8V |
| 4 | I2C & JTAG Diagram | 40 | Power - VCCR_GXB, VCCT_GXB |
| 5 | Clock Diagram | 41 | Power - FMCA, FMCB |
| 6 | S10 GX Configuration | 42 | Power - HILO MEMORY |
| 7 | S10 GX Bank 2A,B,C | 43 | Power - 5V, 2.5V, 2.4V, 1V |
| 8 | S10 GX Bank 2F,L,M,N | 44 | Power - VCCIO3V |
| 9 | S10 GX Bank 3A,B,C | 45 | S10 Decoupling |
| 10 | S10 GX Bank 3I,J,K,L | 46 | Fast Power-Down Discharge |
| 11 | S10 GX Xcvr GXBL 1C,D,E,F | 47 | |
| 12 | S10 GX Xcvr GXBL 1K,L,M,N | 48 | |
| 13 | S10 GX Xcvr GXBR 4C,D,E,F | 49 | |
| 14 | S10 GX Xcvr GXBR 4K,L,M,N | 50 | |
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Power Tree Diagram



Power Sequence Diagram



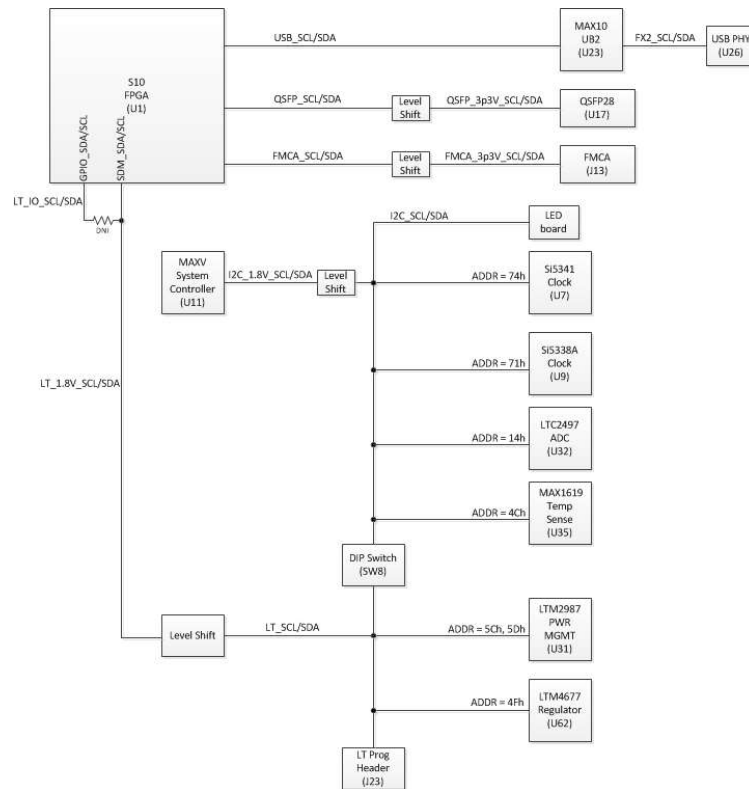
*Power-down sequence is the reverse of power-up sequence



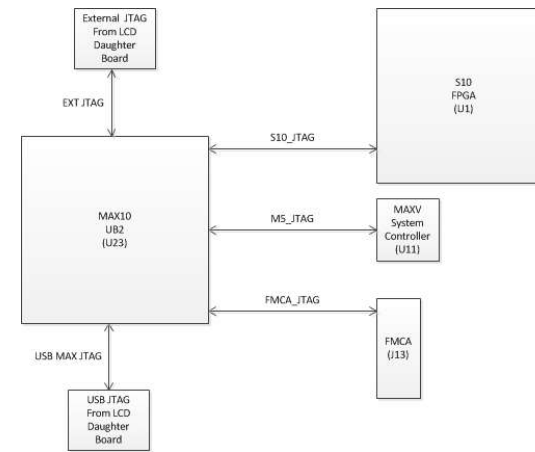
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| Size | Document Number | | Rev |
| C | 150-0321309-D1 | (6XX-44484R) | D1 |
| Date: | Friday, March 17, 2017 | Sheet | 3 of 46 |

I2C & JTAG Diagram

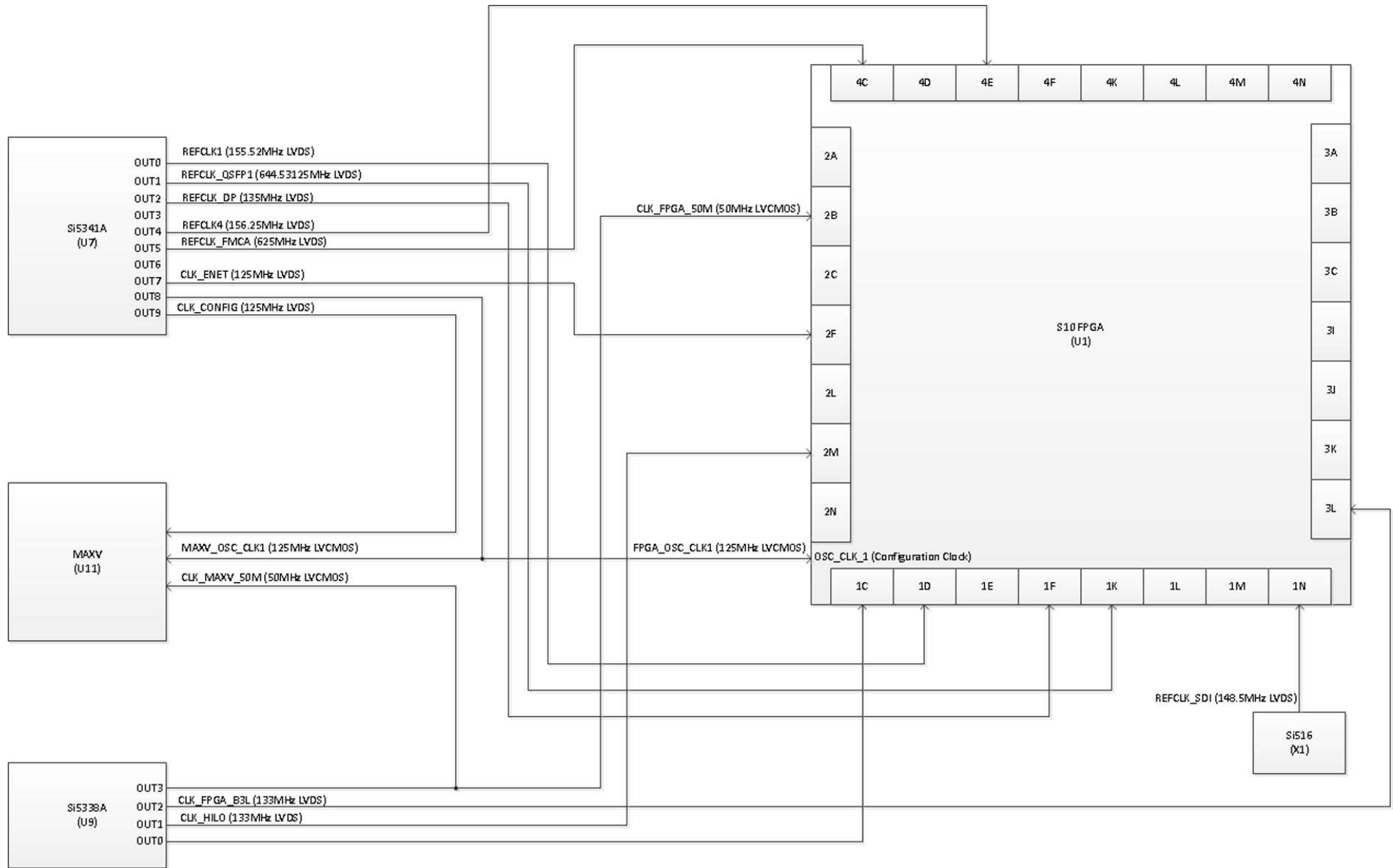
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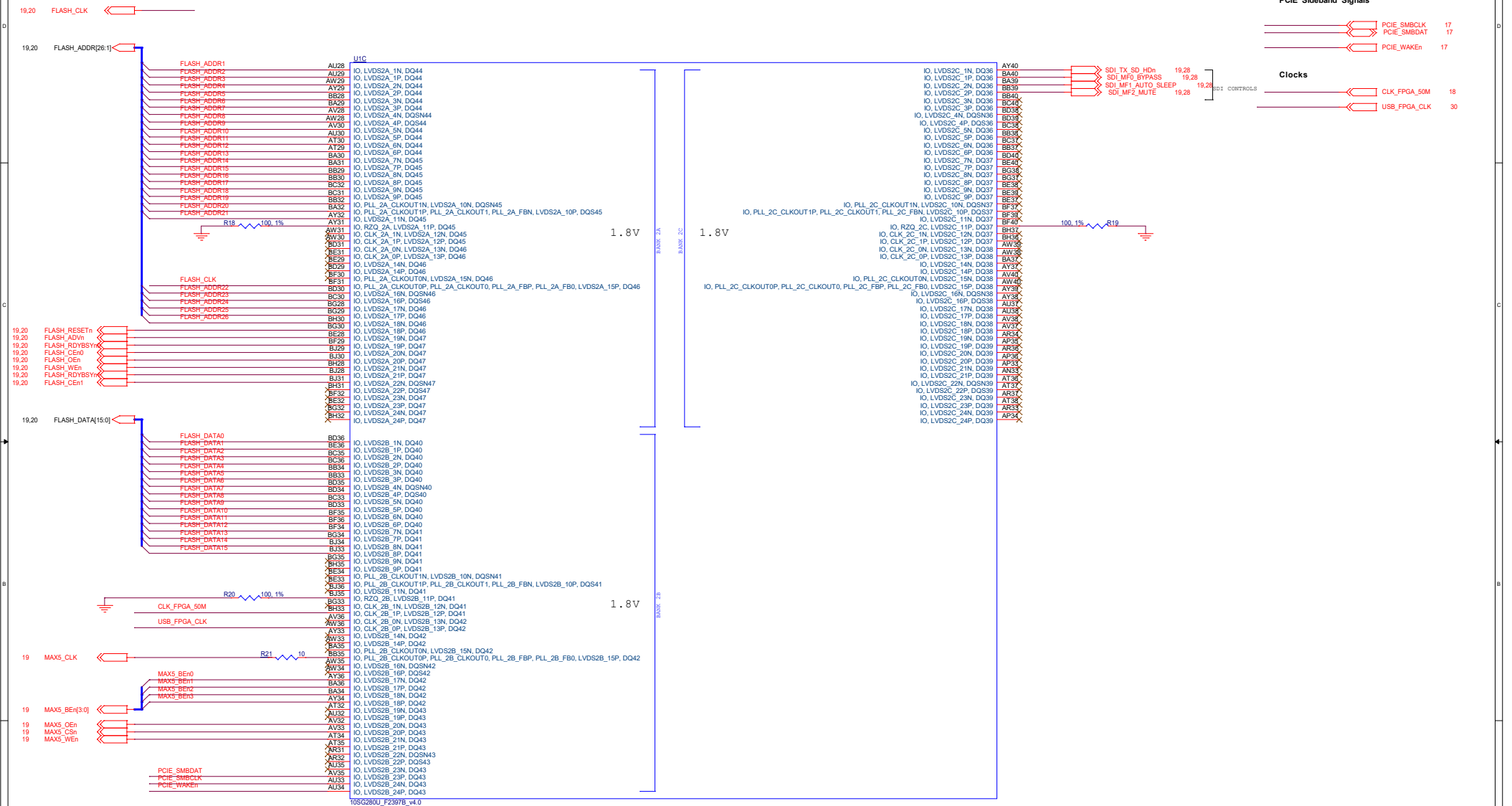
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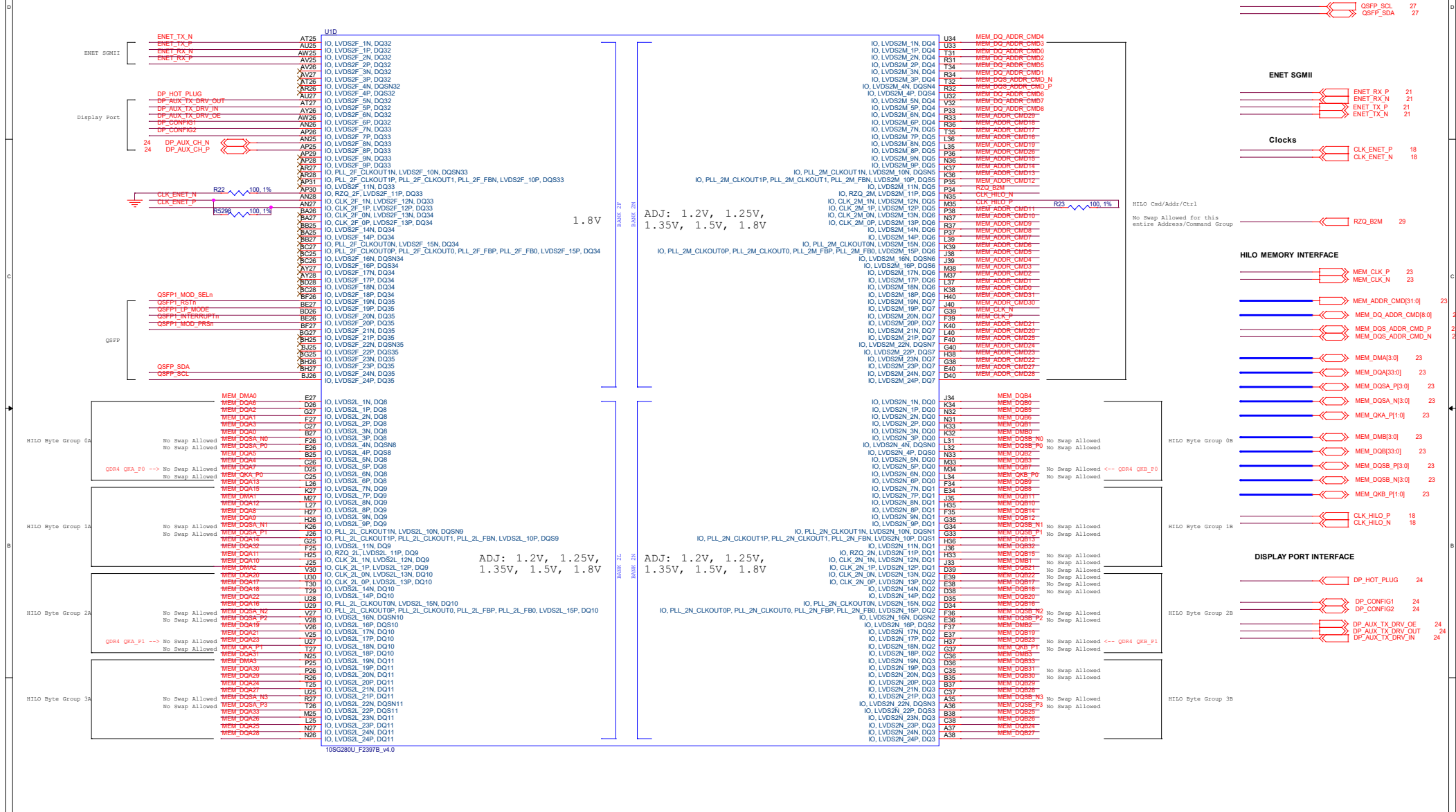
Clock Diagram



S10 GX Bank 2A, B, C

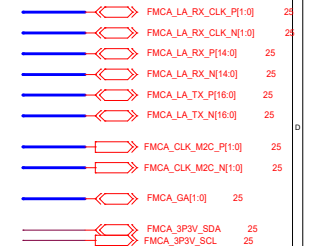
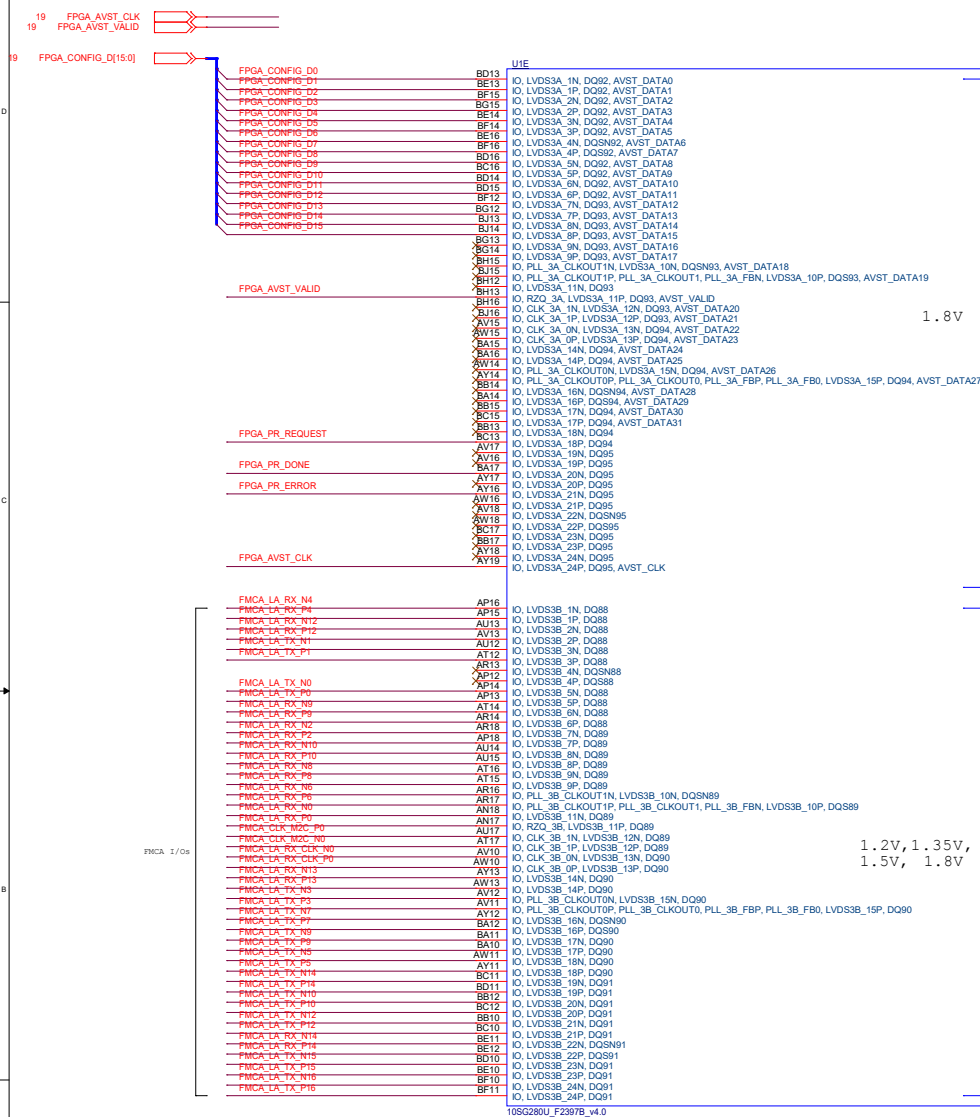


| | |
|--------------------------------|--|
| 3 | |
| S10 GX Bank 2F, L, M, N | |

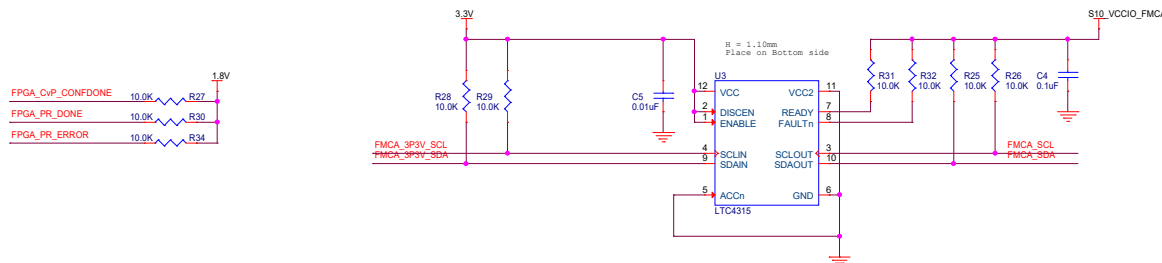


S10 GX Bank 3A, B, C

AVSTx32 CONFIG DATA INTERFACE

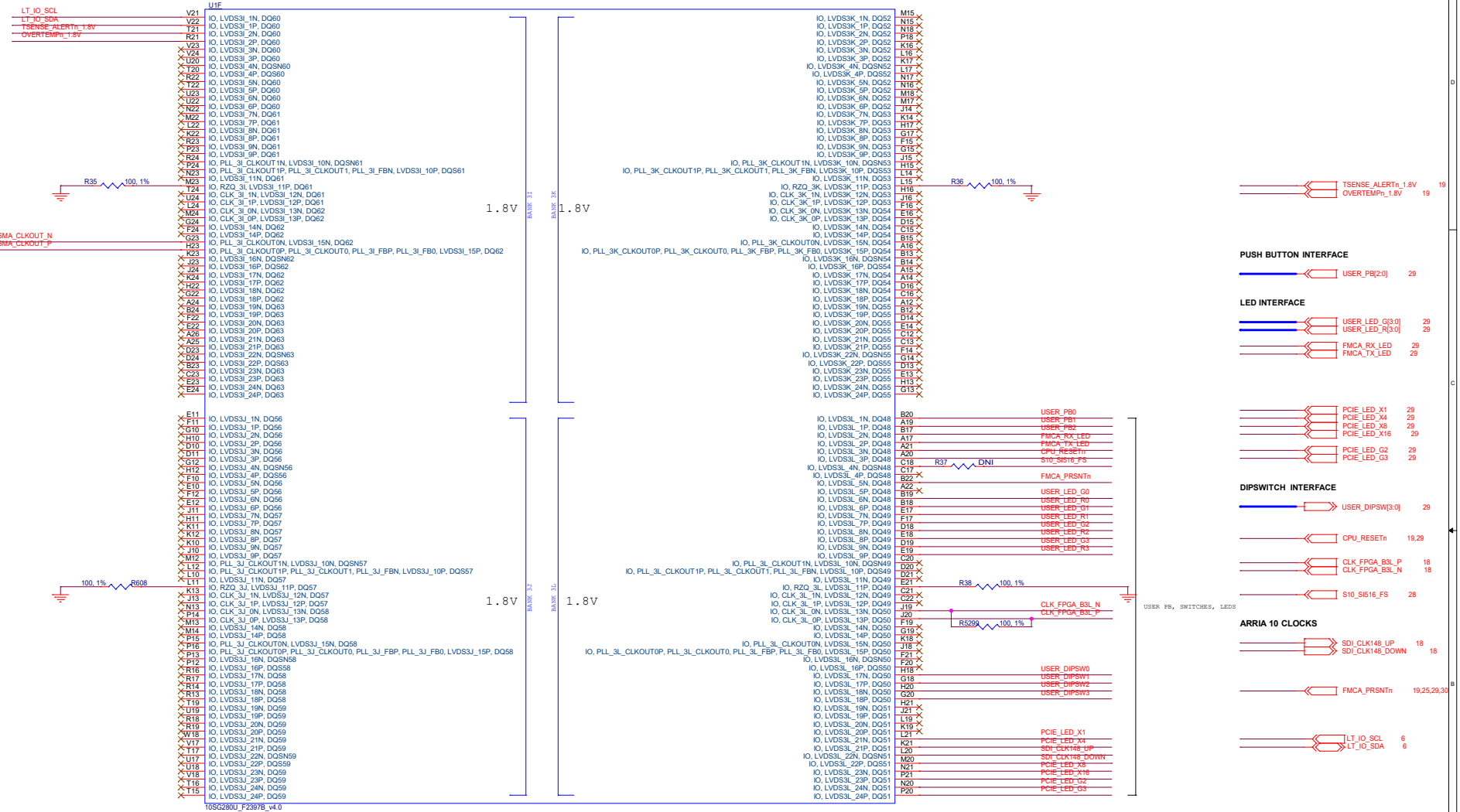


PARTIAL RECONFIG SIGNALS



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| Size C | Document Number 150-0321309-D1 | | (6XX-44484R) |
| Date: | Friday, March 17, 2017 | Sheet | 9 of 49 |

S10 GX Bank 3I, J, K, L



[illegible]

PCIE x16

PCIE x16

DISPLAY PORT



S10 GX Xcvr GXBL 1K,L,M,N



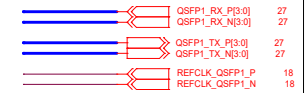
TX1 and TX3 Channels swapped to uncross layout routing

RX1 and RX3 Channels swapped to uncross layout routing

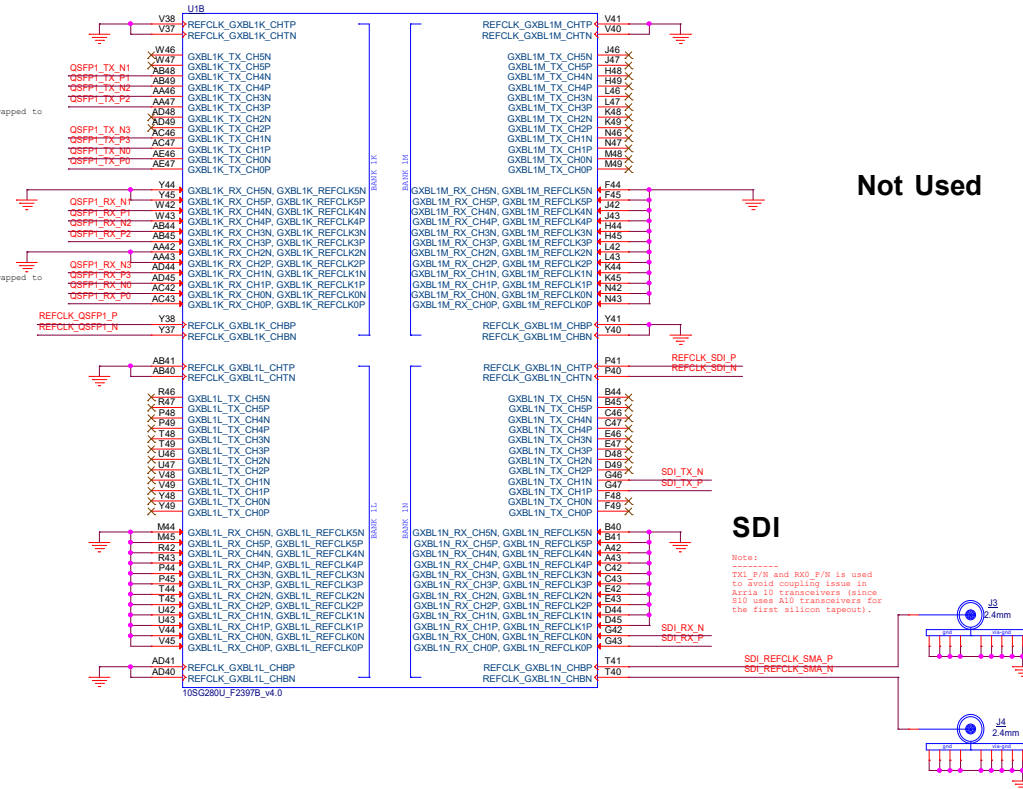
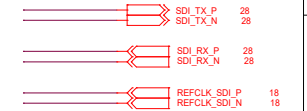
Not Used

Not Used

QSFP1 INTERFACE



SDI INTERFACE



S10 GX Xcvr GXBR 4C,D,E,F



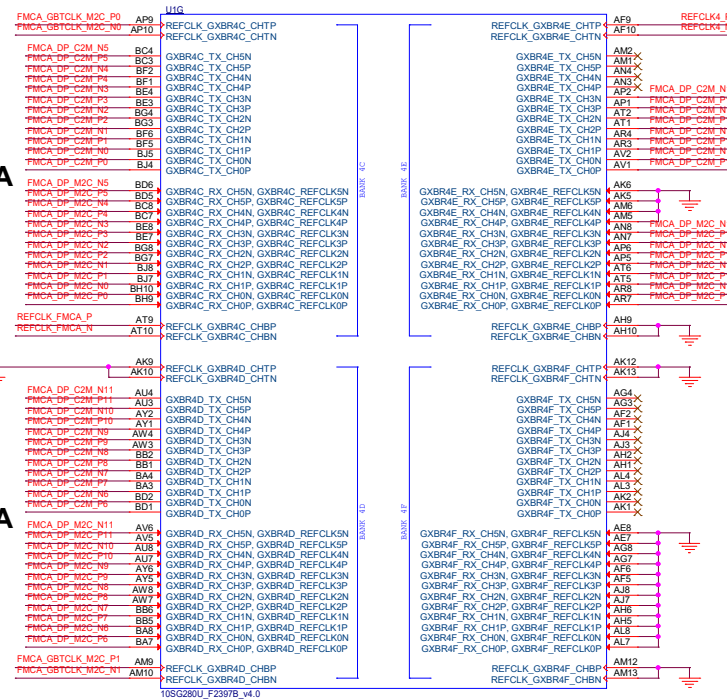
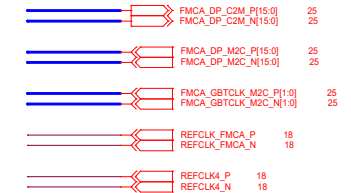
FMCA

FMCA

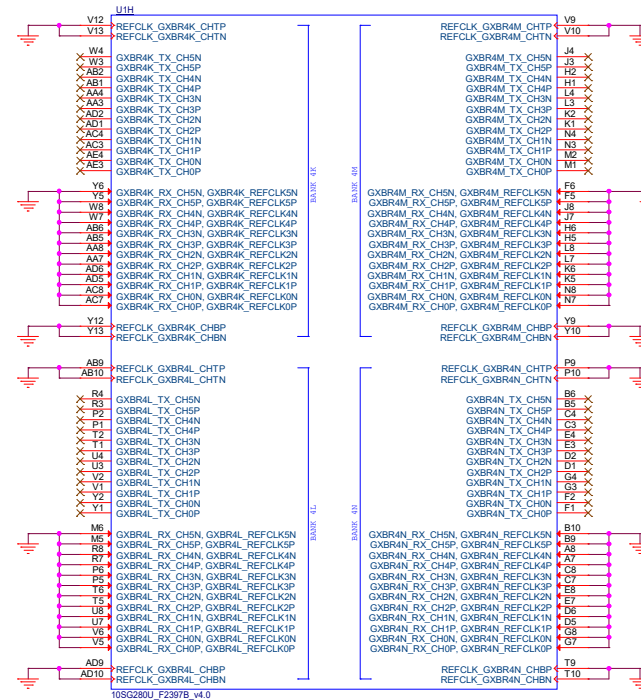
FMCA

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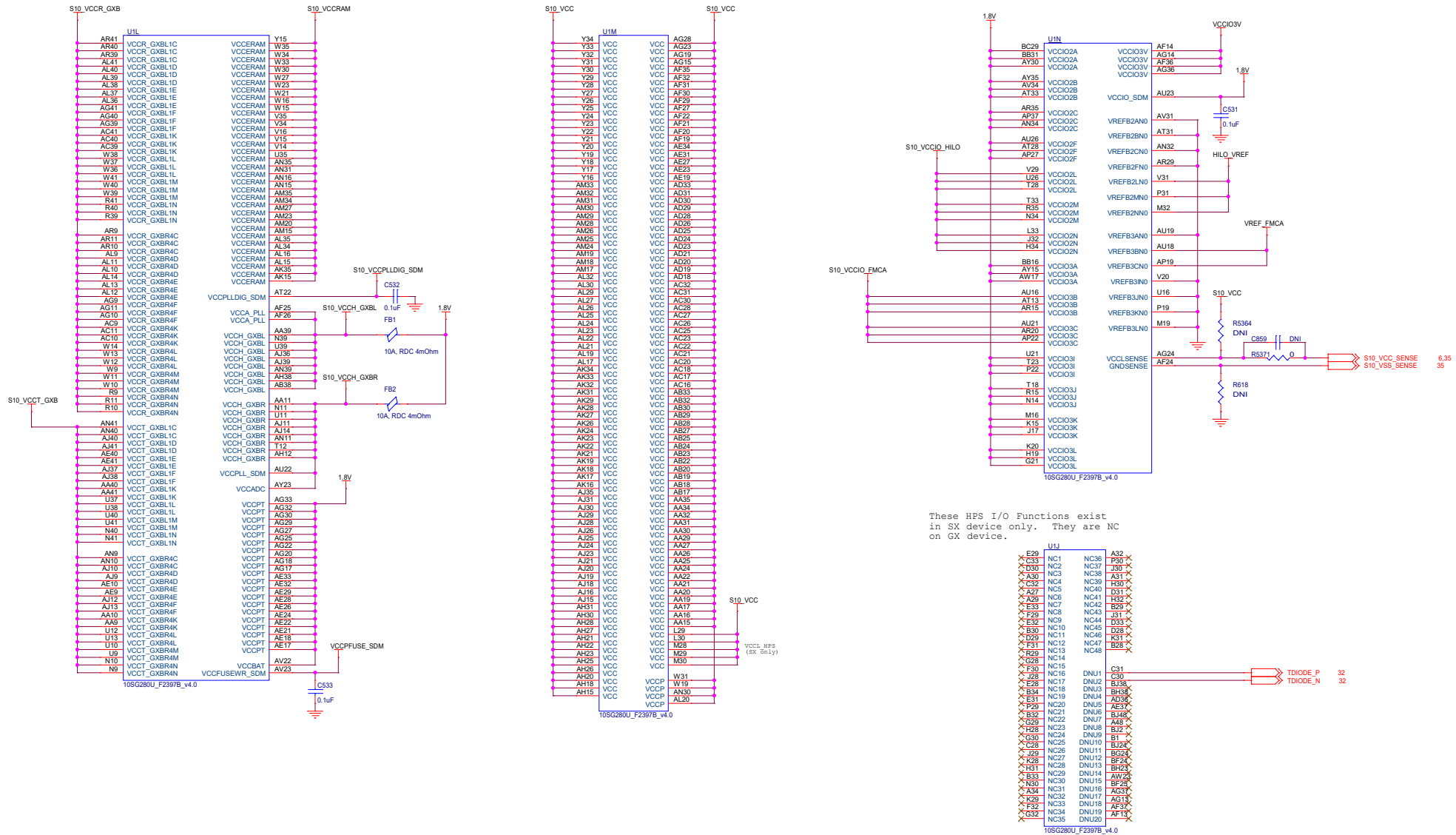
FMCA INTERFACE



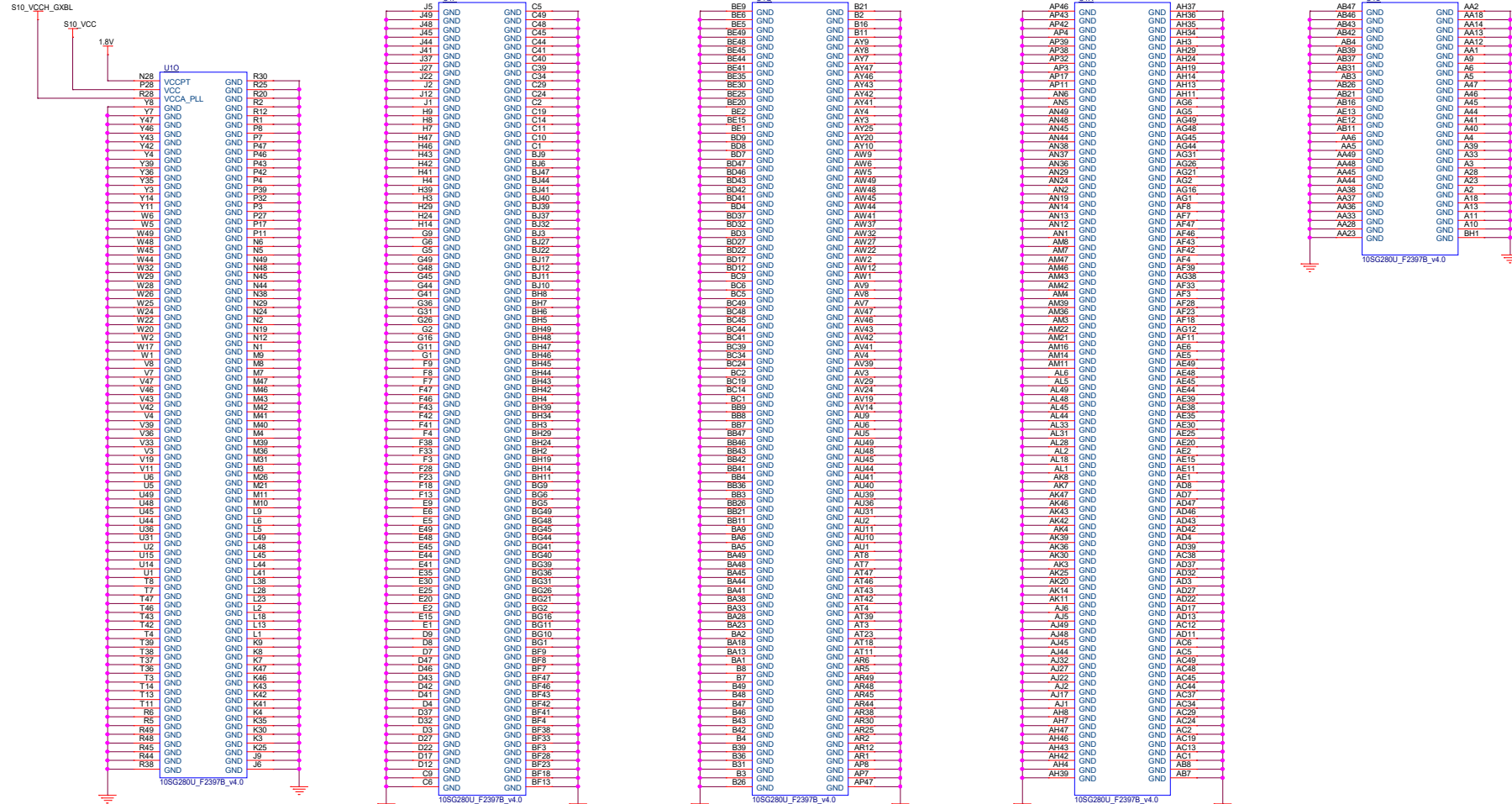
S10 GX Xcvr GXBR 4K,L,M,N



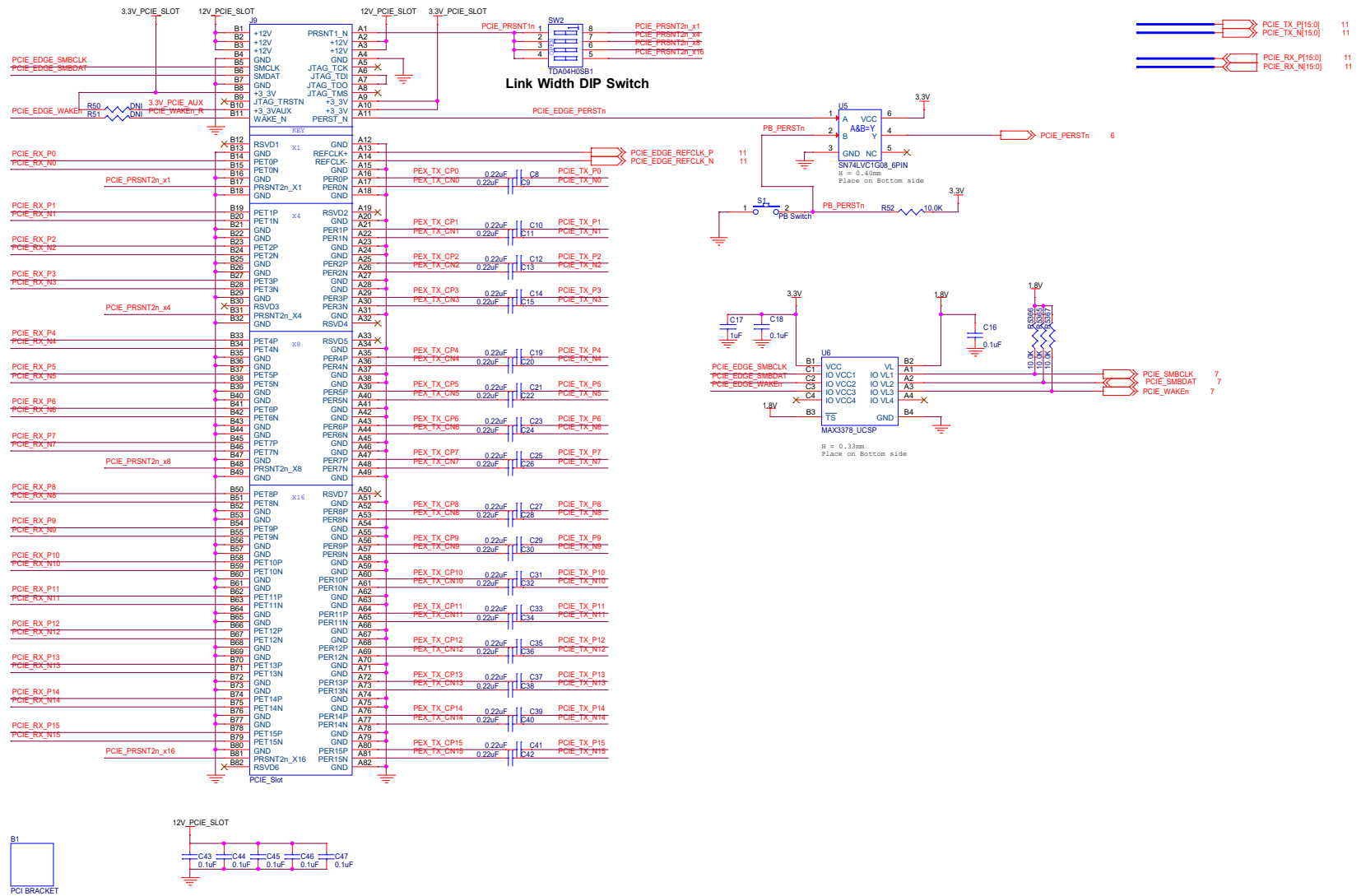
S10 GX Power



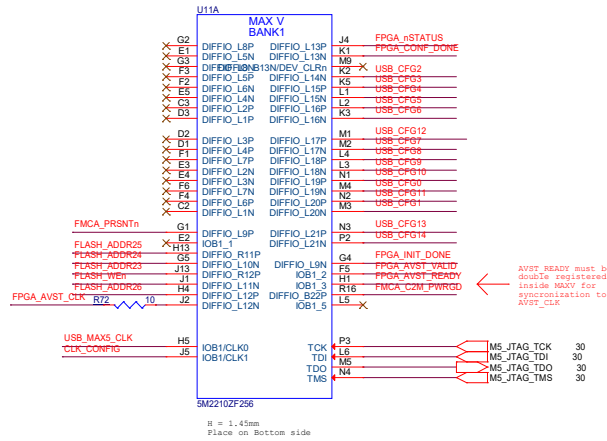
S10 GX Ground



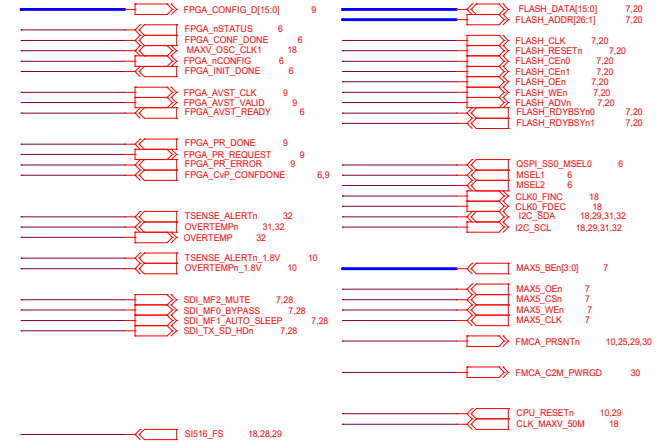
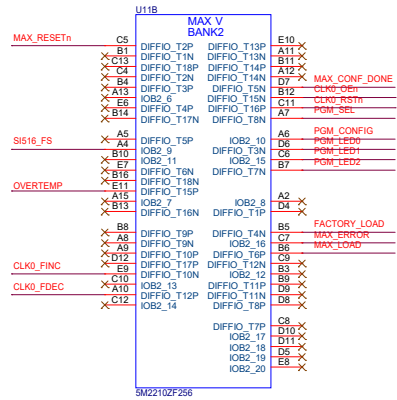
PCIe Edge x16 Gold Fingers



Max V System Controller



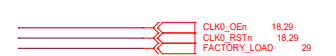
- AVST_READY must be double registered inside MAXV for synchronization to AVST_CLK



ON-BOARD USB BLASTER II



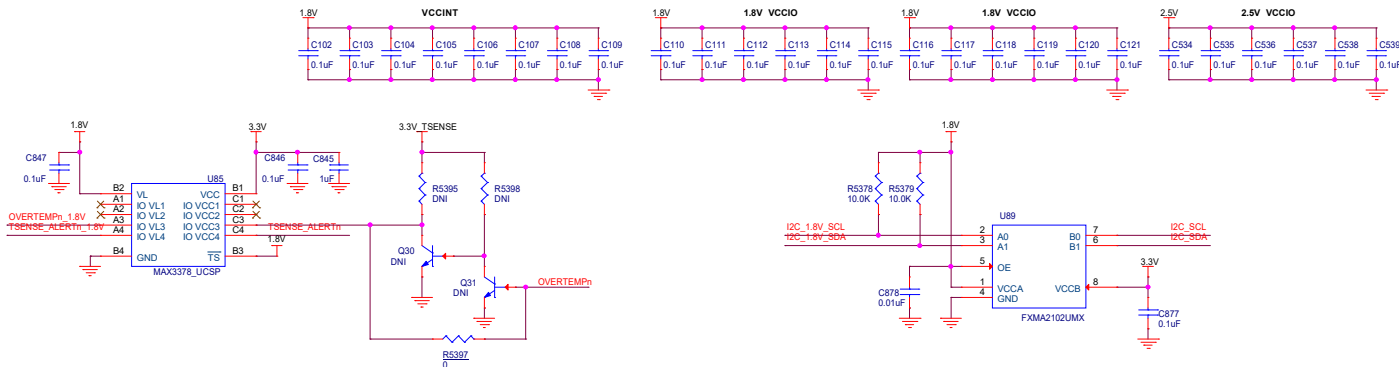
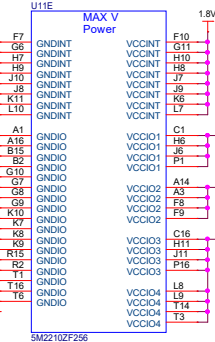
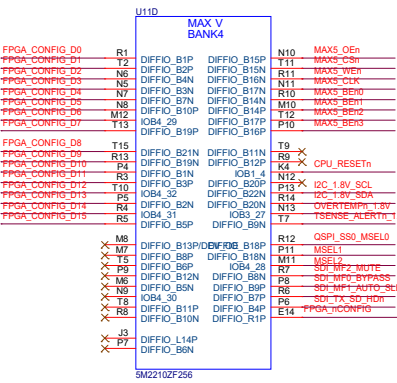
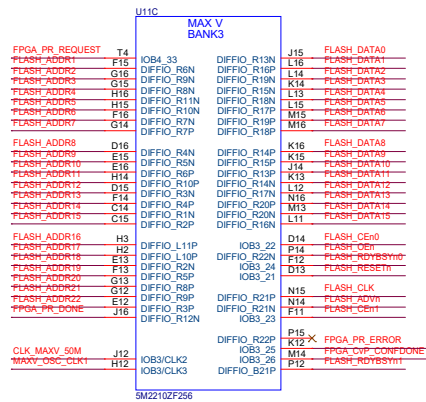
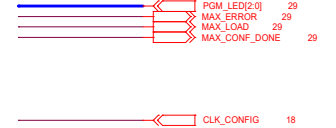
MAXV DIPSWITCH



PUSH BUTTON INTERFACE

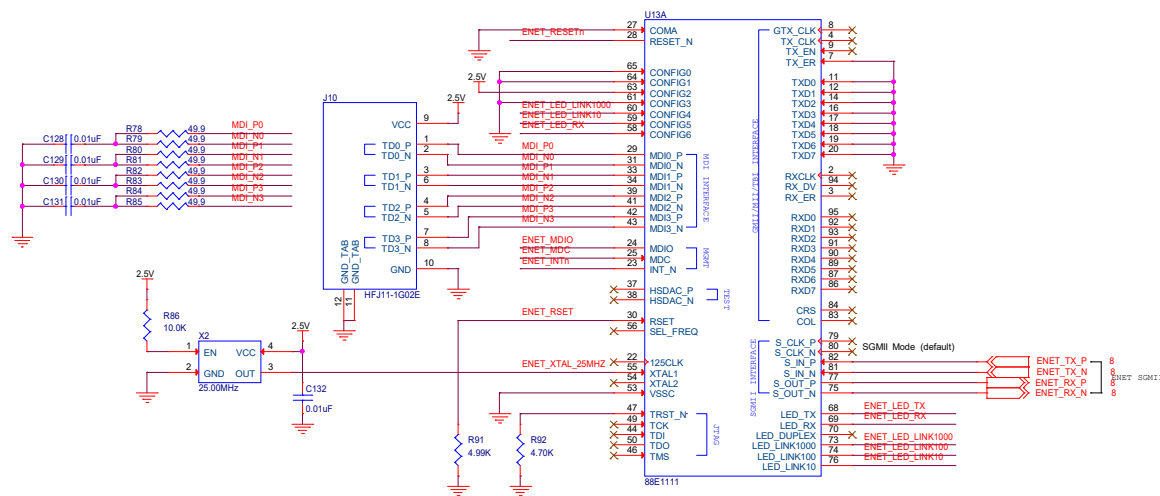


LED INTERFACE

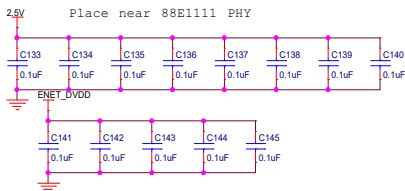
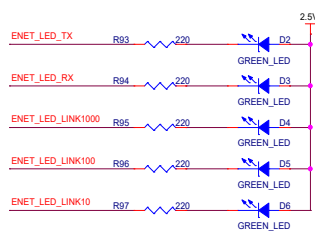
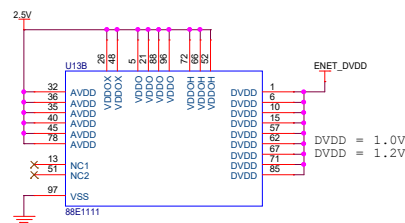




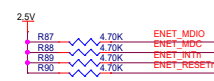
10/100/1000 Ethernet Phy



88E1111-B2-CAA1C000 EOL
88E1111-B2-NDC2C000 Pin Compatible Replacement



| Pin | Pin Connection | Setting Bit[2:0] | Definition |
|---------|---------------------|------------------|---|
| CONFIG0 | GND | 000 | MDIO PHY Address bit (2:0) = 000 |
| CONFIG1 | GND | 000 | Enable Pause, PHY Address bits (4:3) = 00 |
| CONFIG2 | VDDO (2.5V or 3.3V) | 111 | 1110 = Auto-negotiate, advertise all capabilities, prefer Master 100BASE-X FULL-DUPLEX-Auto-Negotiation enabled, 100BASE-X half-duplex |
| CONFIG3 | GND | 000 | Disable crossover, Enable 125kCL |
| CONFIG4 | LED_LINK1000 | 100 | Hardware Config Mode Reg (2:0) = 100 SGMII without Clock with SGMII Auto-Neg to copper |
| CONFIG5 | LED_LINK10 | 110 | Disable fiber/copper auto-sense, disable sleep mode (enable energy detect), Hardware Config Mode Reg (3) = 0 |
| CONFIG6 | LED_RX | 010 | Select MDIO (over 2-wire serial), interrupt polarity = active low, 50-ohm termination for fiber |



ENET RGMII INTERFACE



HILO Connector Map

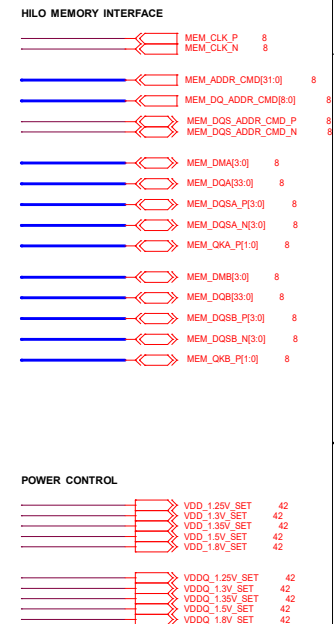
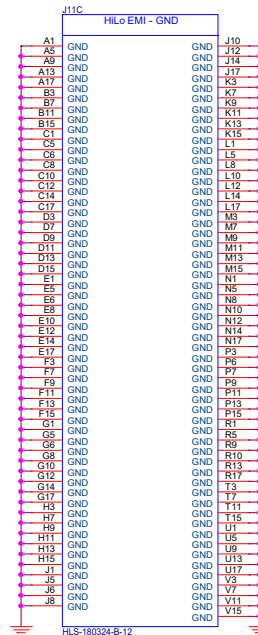
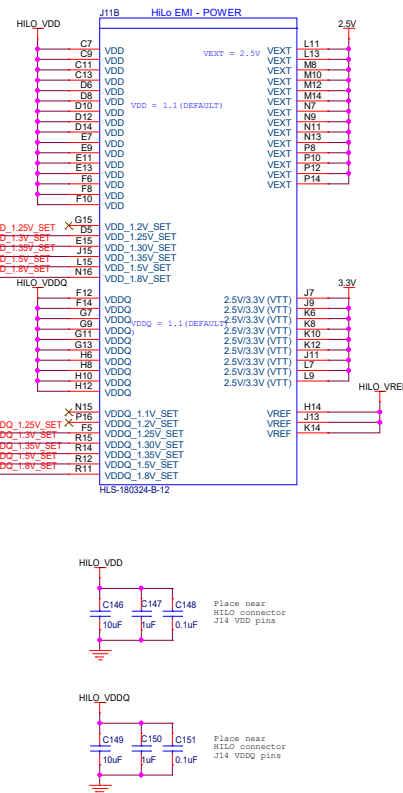
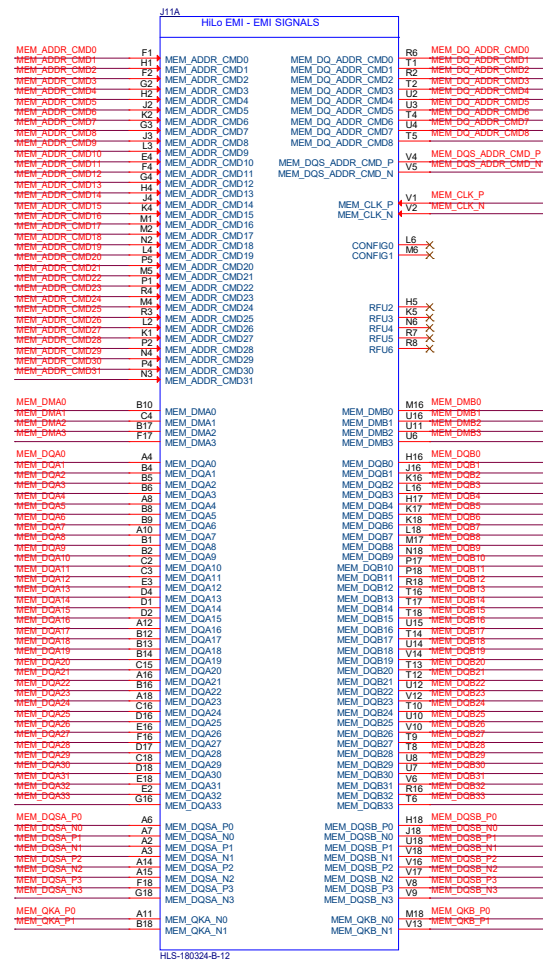
| DDR3 x72 (DQ5 x8) | DDR4 x72 (DQ5 x8 Groups) | RLDRAM3 x36 (DQ5 x8/x9 Groups) | QDR IV x36 (DQ5 x18 Groups) | Hilo Pin Name | Hilo Pin Number |
|----------------------|--------------------------------|--------------------------------------|-----------------------------------|--------------------|--------------------|
| | | | | CONFIG0 | L6 |
| | | | | CONFIG1 | M6 |
| A0 | A0 | A0 | A1 | MEM_ADDR_CMD[0] | F1 |
| A1 | A1 | A1 | A2 | MEM_ADDR_CMD[1] | H1 |
| A10 | A10 | A10 | A11 | MEM_ADDR_CMD[10] | E4 |
| A11 | A11 | A11 | A12 | MEM_ADDR_CMD[11] | F4 |
| A12 | A12 | A12 | A13 | MEM_ADDR_CMD[12] | G4 |
| A13 | A13 | A13 | A14 | MEM_ADDR_CMD[13] | H4 |
| A14 | A14 | A14 | A15 | MEM_ADDR_CMD[14] | J4 |
| A15 | A15 | A15 | A16 | MEM_ADDR_CMD[15] | K4 |
| BA0 | BA0 | BA0 | A19 | MEM_ADDR_CMD[16] | M1 |
| BA1 | BA1 | BA1 | A20 | MEM_ADDR_CMD[17] | M2 |
| BA2 | BA0 | BA2 | A21 | MEM_ADDR_CMD[18] | N2 |
| CA5n | A17 | A17 | A18 | MEM_ADDR_CMD[19] | L4 |
| A2 | A2 | A2 | A3 | MEM_ADDR_CMD[2] | F2 |
| CKE0 | CKE0 | A20 | RWAn | MEM_ADDR_CMD[20] | P5 |
| CKE1 | CKE1 | WEEn | RWBn | MEM_ADDR_CMD[21] | M5 |
| CSn0 | CSn0 | CSn0 | LBKn | MEM_ADDR_CMD[22] | P1 |
| CSn1 | ACTn | CSn1 | LBKn | MEM_ADDR_CMD[23] | R4 |
| ODT0 | ODT0 | A18 | LDAn | MEM_ADDR_CMD[24] | M4 |
| ODT1 | ODT1 | A19 | LDBn | MEM_ADDR_CMD[25] | R3 |
| RA5n | A16 | A16 | A17 | MEM_ADDR_CMD[26] | L2 |
| RESETn | RESETn | RESETn | RESETn | MEM_ADDR_CMD[27] | K1 |
| WEEn | BG1 | BA3 | CFGn | MEM_ADDR_CMD[28] | P2 |
| | ALERTn | CSn3 | A22 | MEM_ADDR_CMD[29] | N4 |
| A3 | A3 | A3 | A4 | MEM_ADDR_CMD[3] | G2 |
| | CSn1 | CSn2 | AINV | MEM_ADDR_CMD[30] | P4 |
| | PAR | REFn | A0 | MEM_ADDR_CMD[31] | N3 |
| A4 | A4 | A4 | A5 | MEM_ADDR_CMD[4] | H2 |
| A5 | A5 | A5 | A6 | MEM_ADDR_CMD[5] | J2 |
| A6 | A6 | A6 | A7 | MEM_ADDR_CMD[6] | K2 |
| A7 | A7 | A7 | A8 | MEM_ADDR_CMD[7] | G3 |
| A8 | A8 | A8 | A9 | MEM_ADDR_CMD[8] | J3 |
| A9 | A9 | A9 | A10 | MEM_ADDR_CMD[9] | L3 |
| CK_NO | CK_NO | CK_N | CK_N | MEM_CLK_N | V2 |
| CK_P0 | CK_P0 | CK_P | CK_P | MEM_CLK_P | V1 |
| DM0 | LDM_n0 | | DINVAD | MEM_DMA[0] | B10 |
| DM1 | UDM_n0 | DM1 | QVLDAD | MEM_DMA[1] | C4 |
| DM2 | LDM_n1 | | DINVAI | MEM_DMA[2] | B17 |
| DM3 | UDM_n1 | | QVLDAI | MEM_DMA[3] | F17 |
| DM4 | LDM_n2 | DQ18 | DINVBO | MEM_DMB[0] | M16 |
| DM5 | UDM_n2 | | QVLD80 | MEM_DMB[1] | U16 |
| DM6 | LDM_n3 | DQ0 | DINVB1 | MEM_DMB[2] | U11 |
| DM7 | UDM_n3 | | QVLD81 | MEM_DMB[3] | U6 |
| DM8 | LDM_n4 | | | MEM_DQ_ADDR_CMD[0] | R6 |
| DQ64 | DQ64 | | | MEM_DQ_ADDR_CMD[1] | T1 |
| DQ65 | DQ65 | | | MEM_DQ_ADDR_CMD[2] | R2 |
| DQ66 | DQ66 | | | MEM_DQ_ADDR_CMD[3] | T2 |

| DDR3 x72 (DQ5 x8) | DDR4 x72 (DQ5 x8 Groups) | RLDRAM3 x36 (DQ5 x8/x9 Groups) | QDR IV x36 (DQ5 x18 Groups) | Hilo Pin Name | Hilo Pin Number |
|----------------------|--------------------------------|--------------------------------------|-----------------------------------|--------------------|--------------------|
| DQ67 | DQ67 | | | MEM_DQ_ADDR_CMD[4] | U2 |
| DQ68 | DQ68 | | | MEM_DQ_ADDR_CMD[5] | U3 |
| DQ69 | DQ69 | | AP | MEM_DQ_ADDR_CMD[6] | T4 |
| DQ70 | DQ70 | | A24 | MEM_DQ_ADDR_CMD[7] | U4 |
| DQ71 | DQ71 | | A23 | MEM_DQ_ADDR_CMD[8] | T5 |
| DQ0 | DQ0 | | DQA0 | MEM_DQA[0] | A4 |
| DQ1 | DQ1 | | DQA1 | MEM_DQA[1] | B4 |
| DQ10 | DQ10 | DQ11 | DQA9 | MEM_DQA[10] | C2 |
| DQ11 | DQ11 | DQ12 | DQA10 | MEM_DQA[11] | C3 |
| DQ12 | DQ12 | DQ13 | DQA11 | MEM_DQA[12] | E3 |
| DQ13 | DQ13 | DQ14 | DQA12 | MEM_DQA[13] | D4 |
| DQ14 | DQ14 | DQ15 | DQA13 | MEM_DQA[14] | D1 |
| DQ15 | DQ15 | DQ16 | DQA14 | MEM_DQA[15] | D2 |
| DQ16 | DQ16 | QVLD1 | DQA18 | MEM_DQA[16] | A12 |
| DQ17 | DQ17 | | DQA19 | MEM_DQA[17] | B12 |
| DQ18 | DQ18 | | DQA20 | MEM_DQA[18] | B13 |
| DQ19 | DQ19 | | DQA21 | MEM_DQA[19] | B14 |
| DQ2 | DQ2 | | DQA2 | MEM_DQA[2] | B5 |
| DQ20 | DQ20 | | DQA22 | MEM_DQA[20] | C15 |
| DQ21 | DQ21 | | DQA23 | MEM_DQA[21] | A16 |
| DQ22 | DQ22 | | DQA24 | MEM_DQA[22] | B16 |
| DQ23 | DQ23 | | QKA_N1 | MEM_DQA[23] | A18 |
| DQ24 | DQ24 | DQ27 | DQA25 | MEM_DQA[24] | C16 |
| DQ25 | DQ25 | DQ28 | DQA26 | MEM_DQA[25] | D16 |
| DQ26 | DQ26 | DQ29 | DQA27 | MEM_DQA[26] | F16 |
| DQ27 | DQ27 | DQ30 | DQA28 | MEM_DQA[27] | F16 |
| DQ28 | DQ28 | DQ31 | DQA29 | MEM_DQA[28] | D17 |
| DQ29 | DQ29 | DQ32 | DQA30 | MEM_DQA[29] | C18 |
| DQ3 | DQ3 | | DQA3 | MEM_DQA[3] | B6 |
| DQ30 | DQ30 | DQ33 | DQA31 | MEM_DQA[30] | D18 |
| DQ31 | DQ31 | DQ34 | DQA32 | MEM_DQA[31] | E18 |
| | | DQ17 | DQA15 | MEM_DQA[32] | E2 |
| | | DQ35 | DQA33 | MEM_DQA[33] | G16 |
| DQ4 | DQ4 | | DQA4 | MEM_DQA[4] | A8 |
| DQ5 | DQ5 | | DQA5 | MEM_DQA[5] | B8 |
| DQ6 | DQ6 | | DQA6 | MEM_DQA[6] | B9 |
| DQ7 | DQ7 | | QKA_NO | MEM_DQA[7] | A10 |
| DQ8 | DQ8 | DQ9 | DQA7 | MEM_DQA[8] | B1 |
| DQ9 | DQ9 | DQ10 | DQA8 | MEM_DQA[9] | B2 |
| DQ32 | DQ32 | DQ19 | DQ80 | MEM_DQB[0] | H16 |
| DQ33 | DQ33 | DQ20 | DQ81 | MEM_DQB[1] | J16 |
| DQ42 | DQ42 | | DQ89 | MEM_DQB[10] | P17 |
| DQ43 | DQ43 | | DQ810 | MEM_DQB[11] | P18 |
| DQ44 | DQ44 | | DQ811 | MEM_DQB[12] | R18 |
| DQ45 | DQ45 | | DQ812 | MEM_DQB[13] | T16 |
| DQ46 | DQ46 | | DQ813 | MEM_DQB[14] | T17 |
| DQ47 | DQ47 | | DQ814 | MEM_DQB[15] | T18 |
| DQ48 | DQ48 | DQ1 | DQ818 | MEM_DQB[16] | U15 |

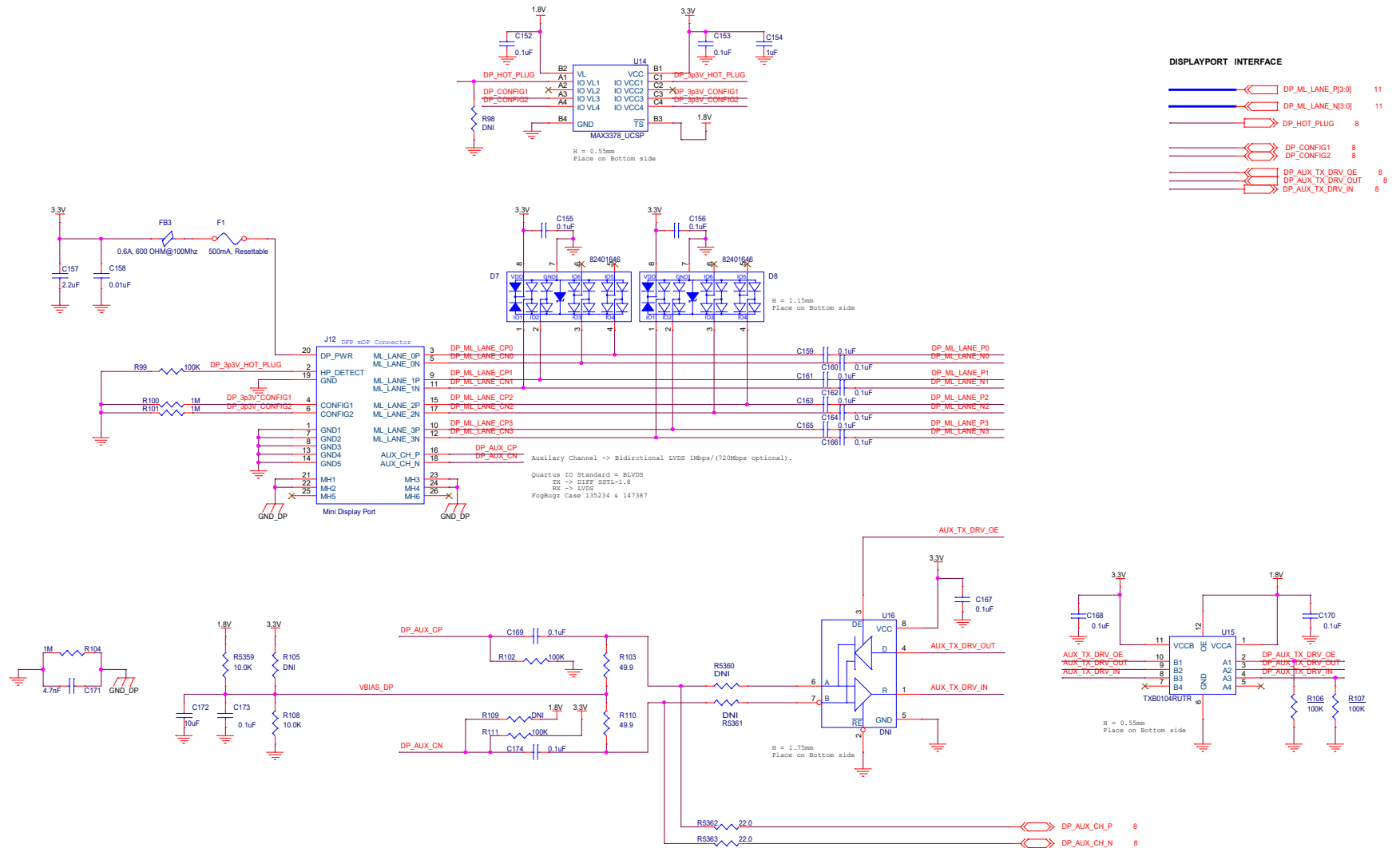
| DDR3 x72 (DQ5 x8) | DDR4 x72 (DQ5 x8 Groups) | RLDRAM3 x36 (DQ5 x8/x9 Groups) | QDR IV x36 (DQ5 x18 Groups) | Hilo Pin Name | Hilo Pin Number |
|----------------------|--------------------------------|--------------------------------------|-----------------------------------|--------------------|--------------------|
| DQ49 | DQ49 | DQ2 | DQ819 | MEM_DQB[17] | T14 |
| DQ50 | DQ50 | DQ3 | DQ820 | MEM_DQB[18] | U14 |
| DQ51 | DQ51 | DQ4 | DQ821 | MEM_DQB[19] | V14 |
| DQ34 | DQ34 | DQ21 | DQ82 | MEM_DQB[2] | K16 |
| DQ52 | DQ52 | DQ5 | DQ822 | MEM_DQB[20] | T13 |
| DQ53 | DQ53 | DQ6 | DQ823 | MEM_DQB[21] | T12 |
| DQ54 | DQ54 | DQ7 | DQ824 | MEM_DQB[22] | U12 |
| DQ55 | DQ55 | DQ8 | QKB_N1 | MEM_DQB[23] | V12 |
| DQ56 | DQ56 | | DQ825 | MEM_DQB[24] | T10 |
| DQ57 | DQ57 | | DQ826 | MEM_DQB[25] | U10 |
| DQ58 | DQ58 | | DQ827 | MEM_DQB[26] | V10 |
| DQ59 | DQ59 | | DQ828 | MEM_DQB[27] | T9 |
| DQ60 | DQ60 | | DQ829 | MEM_DQB[28] | T8 |
| DQ61 | DQ61 | | DQ830 | MEM_DQB[29] | U8 |
| DQ35 | DQ35 | DQ22 | DQ83 | MEM_DQB[3] | L16 |
| DQ62 | DQ62 | | DQ831 | MEM_DQB[30] | U7 |
| DQ63 | DQ63 | | DQ832 | MEM_DQB[31] | V6 |
| | | | DQ815 | MEM_DQB[32] | R16 |
| | | | DQ833 | MEM_DQB[33] | T6 |
| DQ36 | DQ36 | DQ23 | DQ84 | MEM_DQB[4] | H17 |
| DQ37 | DQ37 | DQ24 | DQ85 | MEM_DQB[5] | K17 |
| DQ38 | DQ38 | DQ25 | DQ86 | MEM_DQB[6] | K18 |
| DQ39 | DQ39 | DQ26 | QKB_NO | MEM_DQB[7] | L18 |
| DQ40 | DQ40 | QVLD0 | DQ87 | MEM_DQB[8] | M17 |
| DQ41 | DQ41 | | DQ88 | MEM_DQB[9] | N18 |
| DQS_N8 | DQSL_N4 | | | MEM_DQS_ADDR_CMD_N | V5 |
| DQS_P8 | DQSL_P4 | | PEn | MEM_DQS_ADDR_CMD_P | V4 |
| DQS_NO | DQSL_NO | | DQA17 | MEM_DQSA_N[0] | A7 |
| DQS_N1 | DQSU_N0 | QK1# | DKA_NO | MEM_DQSA_N[1] | A3 |
| DQS_N2 | DQSL_N1 | DK1# | DQA35 | MEM_DQSA_N[2] | A15 |
| DQS_N3 | DQSU_N1 | QK3# | DKA_N1 | MEM_DQSA_N[3] | G18 |
| DQS_P0 | DQSL_P0 | | DQA16 | MEM_DQSA_P[0] | A6 |
| DQS_P1 | DQSU_P0 | QK1 | DKA_P0 | MEM_DQSA_P[1] | A2 |
| DQS_P2 | DQSL_P1 | DK1 | DQA34 | MEM_DQSA_P[2] | A14 |
| DQS_P3 | DQSU_P1 | QK3 | DKA_P1 | MEM_DQSA_P[3] | F18 |
| DQS_N4 | DQSL_N2 | QK2# | DQ817 | MEM_DQSB_N[0] | J18 |
| DQS_N5 | DQSU_N2 | DK0# | DK8_NO | MEM_DQSB_N[1] | V18 |
| DQS_N6 | DQSL_N3 | QK0# | DQ835 | MEM_DQSB_N[2] | V17 |
| DQS_N7 | DQSU_N3 | | DK8_N1 | MEM_DQSB_N[3] | V9 |
| DQS_P4 | DQSL_P2 | QK2 | DQ816 | MEM_DQSB_P[0] | H18 |
| DQS_P5 | DQSU_P2 | DK0 | DK8_P0 | MEM_DQSB_P[1] | U18 |
| DQS_P6 | DQSL_P3 | QK0 | DQ834 | MEM_DQSB_P[2] | V16 |
| DQS_P7 | DQSU_P3 | | DK8_P1 | MEM_DQSB_P[3] | V8 |
| | | | QKA_P0 | MEM_QKA_P[0] | A11 |
| | | | QKA_P1 | MEM_QKA_P[1] | B18 |
| | | | QKB_P0 | MEM_QKB_P[0] | M18 |
| | | DM0 | QKB_P1 | MEM_QKB_P[1] | V13 |



HILO Memory Interface



Display Port (x4)

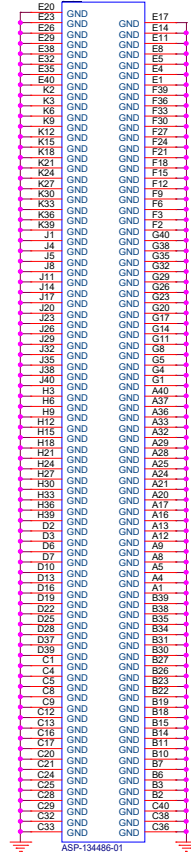
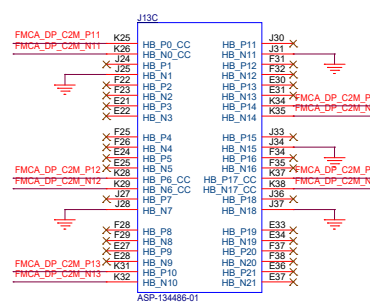
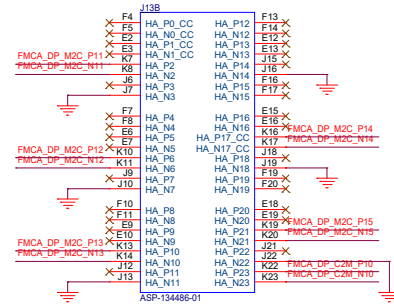
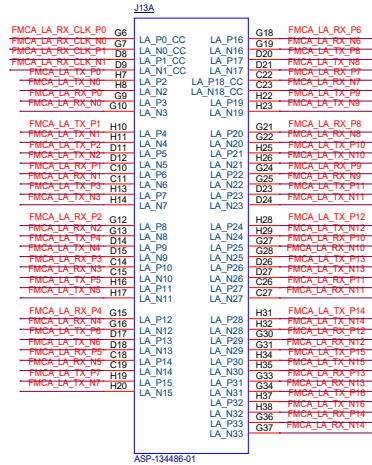


- TX uses diff satll8 configuration, which is able to meet peak-to-peak differential voltage and common mode voltage spec for DP.
- RX uses LVDS input, but user need to ensure pin voltage at NF receiver end is <1.9V.
 - If the channel is AC couple, then user need to choose the correct Vbias RX so that Vpin < 1.9v. The spec is 0 - 2v, which is quite wide. Selecting Vbias RX at 2v region will cause NF device to have reliability issue.
 - If the channel is DC couple, user need to make sure TX common mode voltage + ground reference differences between Tx and Rx will not cause Vpin for NF to be higher than 1.9v.

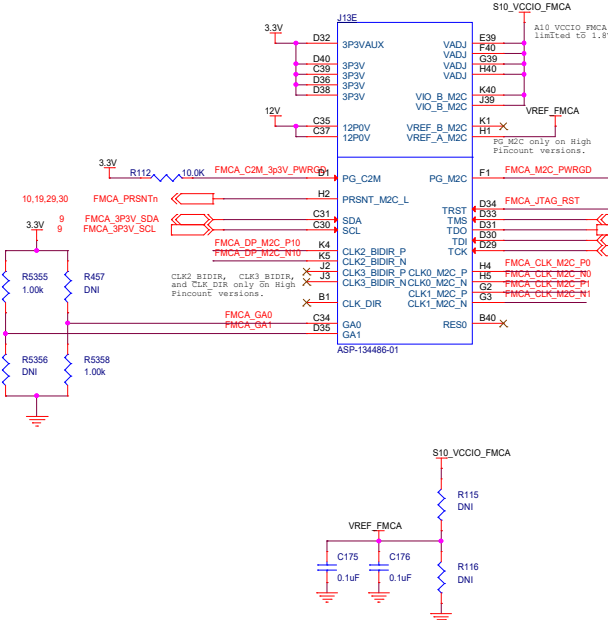
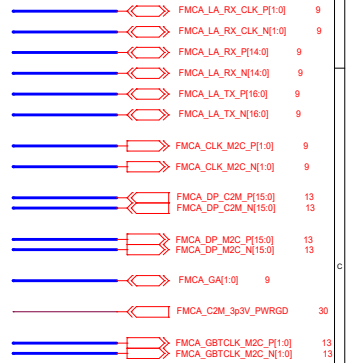


FMC Port A

LVDS P/N NEED TO BE MATCHED BY +/-10ps WITH COMPENSATION ON BOARD FOR PACKAGE DELAYS.



FMCA INTERFACE



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| | | | |
|---|-----------------------------|-------|----------|
| Intel Corporation, 101 Innovation Dr., San Jose CA 95134 | | | |
| Copyright (c) 2016, Intel Corporation. All Rights Reserved. | | | |
| Title Stratix 10 GX FPGA Development Kit | | | |
| PRE-RELEASED SCHEMATIC DO NOT COPY | | | |
| Size | Document Number | | Rev |
| C | 150-0321309-D1 (6XX-44484R) | | D1 |
| Date: | Friday, March 17, 2017 | Sheet | 26 of 46 |

3
QSFP

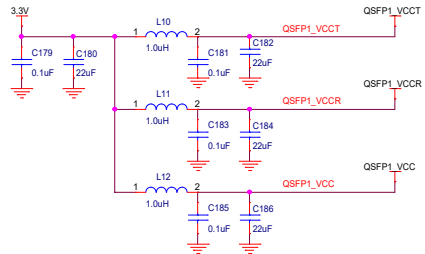
Quad Small Form-factor Pluggable (QSFP) Interface

NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

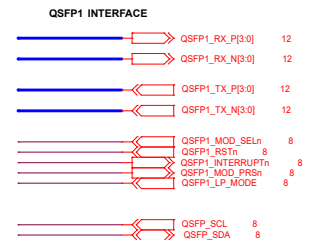
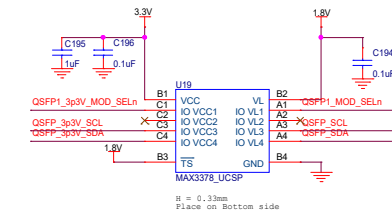
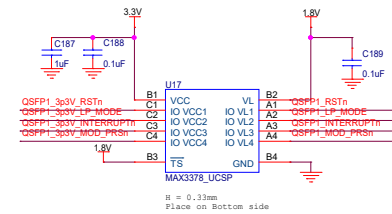
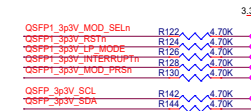
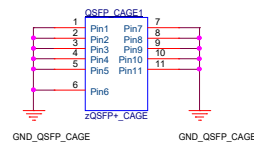
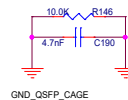
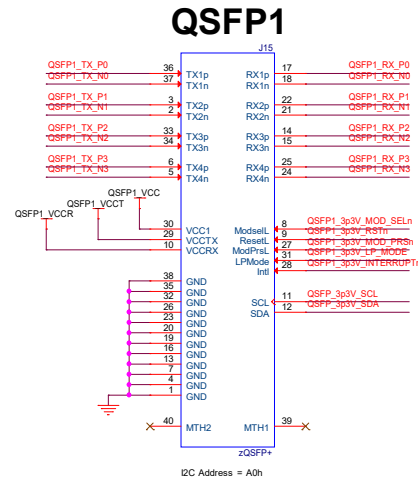
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

NOTE 3: DC blocking capacitors are in the module for RX and TX.

NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



Maximum power is $\leq 3.5\text{W}$ (1.06 A)
Maximum inrush current = 1.3A



NEW CHIPSET AVAILABLE - CHECK WITH MACOM

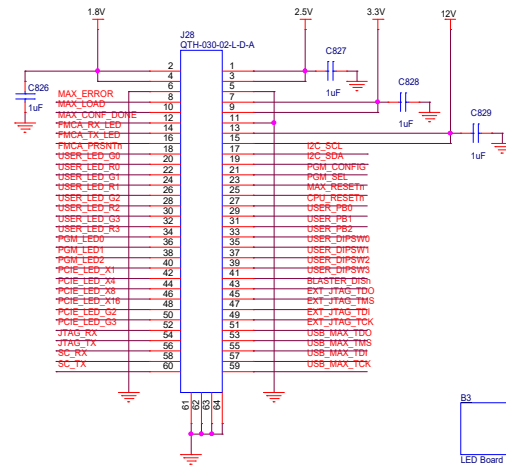
Layout Notes (M22468) SDI Cable Driver:

- The RSET resistor should be located close to pin 5.
- Remove GND under pin 5 and the RSET resistor.
- The 49.9-ohm resistors should be placed close to device pins 16 and 1 (SDIP/SDIN).

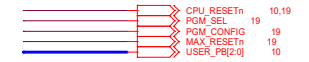
Layout Notes (M22544) SDI Cable Equalizer:

- The AGC 33nF capacitor should be located close to the device pins 8 and 9 (AGC+/AGC-).
- Clear GND under the AGC 33nF capacitor.

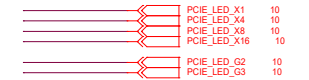
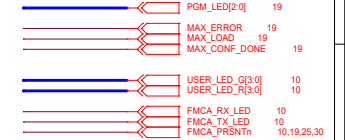
LCD, User PB, SW, I/Os



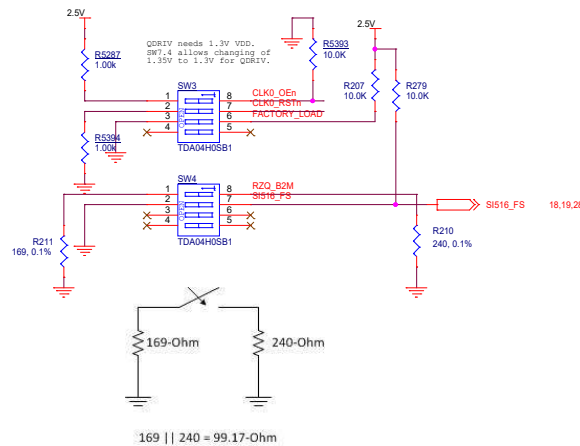
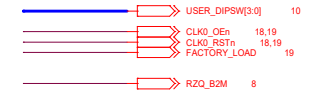
PUSH BUTTON INTERFACE



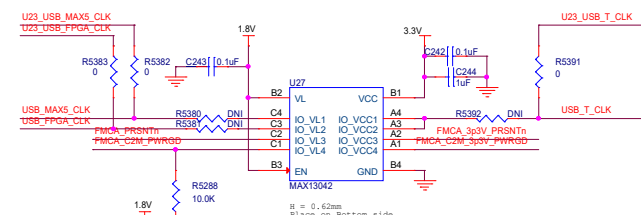
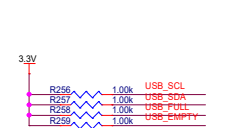
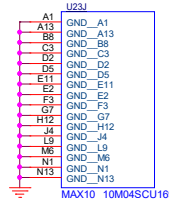
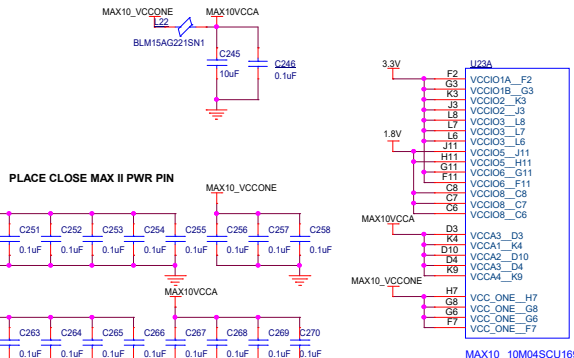
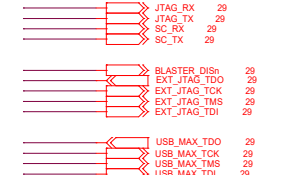
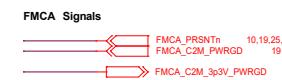
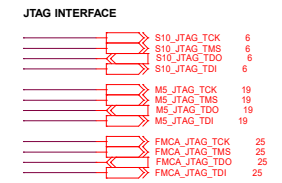
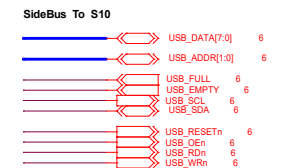
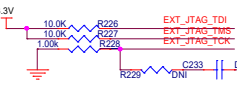
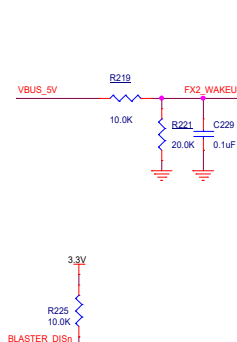
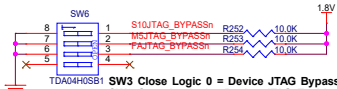
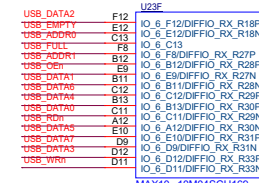
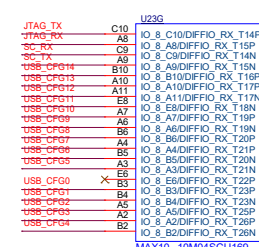
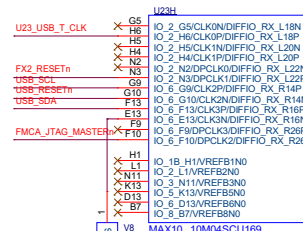
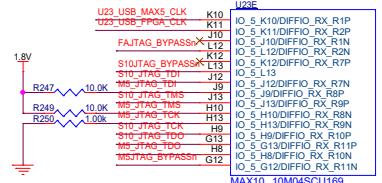
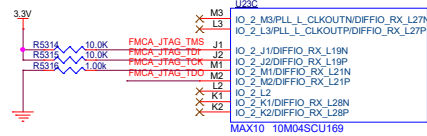
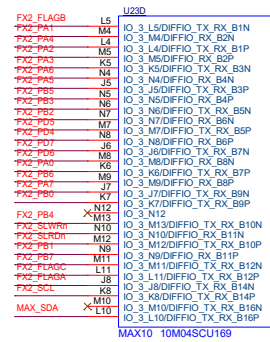
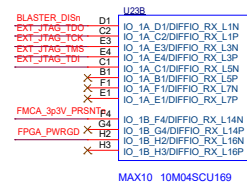
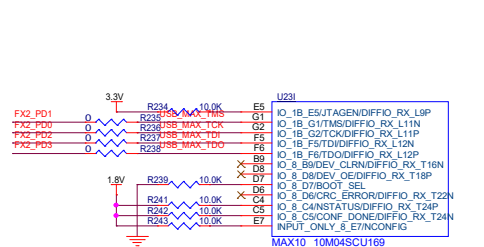
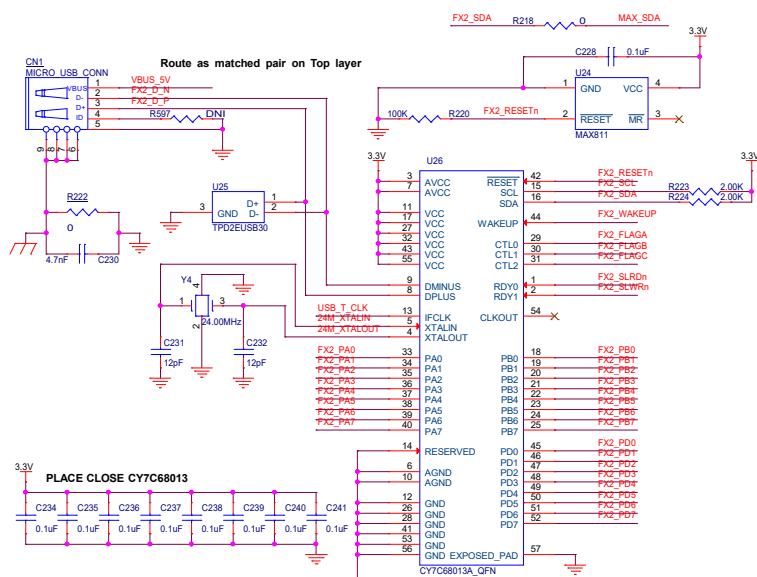
LED INTERFACE



DIPSWITCH INTERFACE



Max10 USB Blaster II

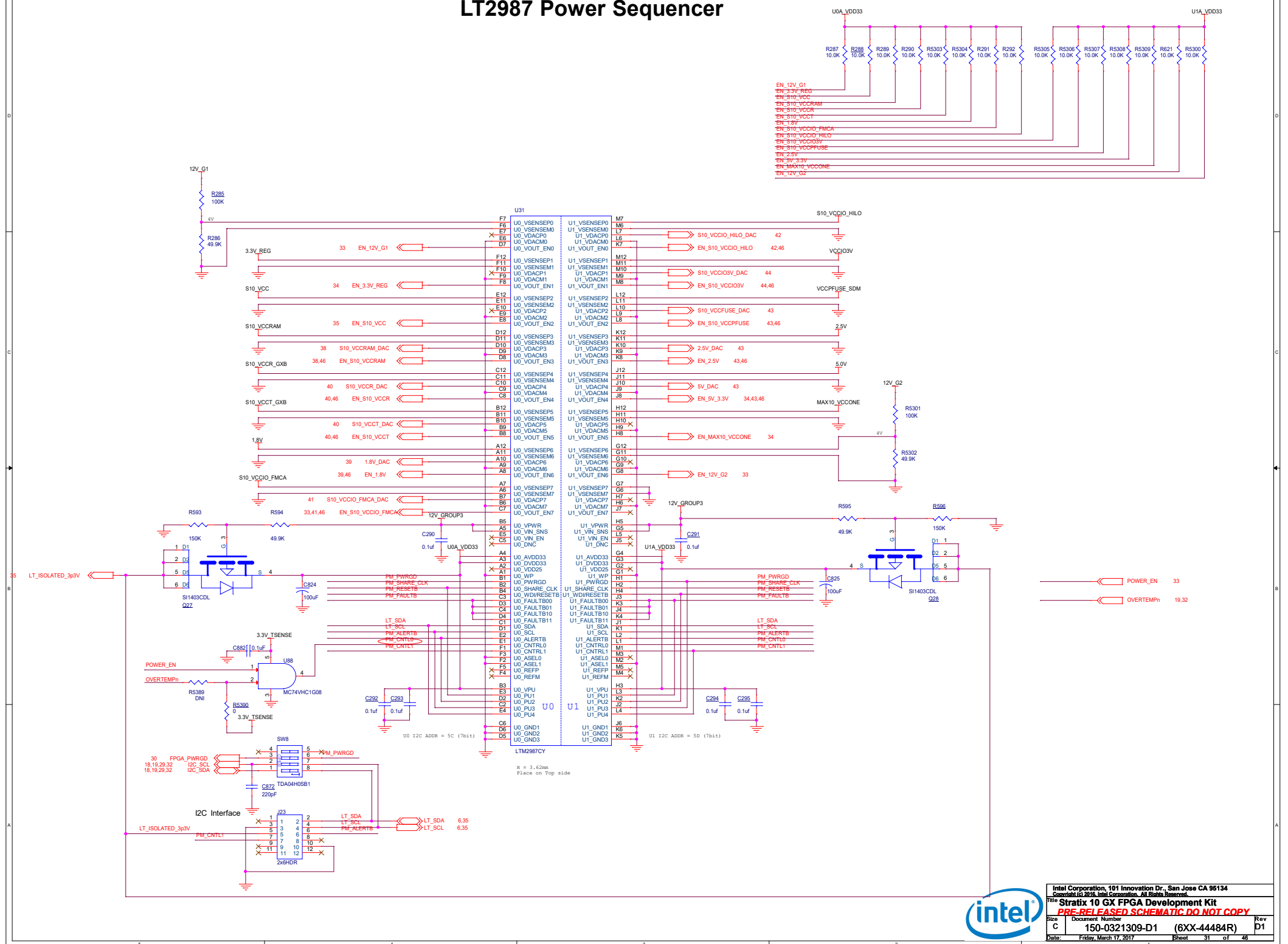


```
To reduce stub, route:
R5383 shares one pad with R5381
R5382 shares one pad with R5380
R5391 shares one pad with R5392
```

SW3 Close Logic 0 = Device JTAG Bypass
SW3 Open Logic 1 = Device JTAG Enable

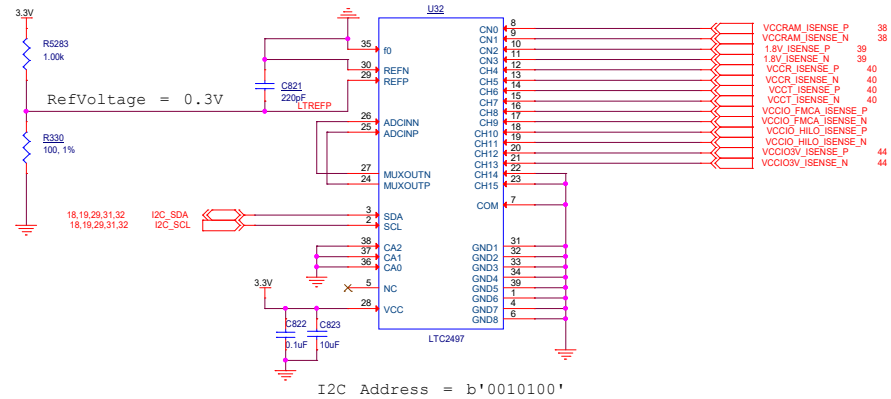
H = 0.62mm
 Flange on Bottom side

LT2987 Power Sequencer

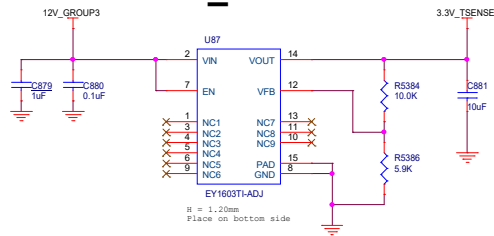


Current & Temp Sense

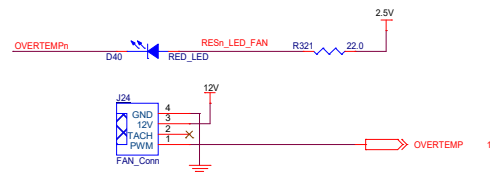
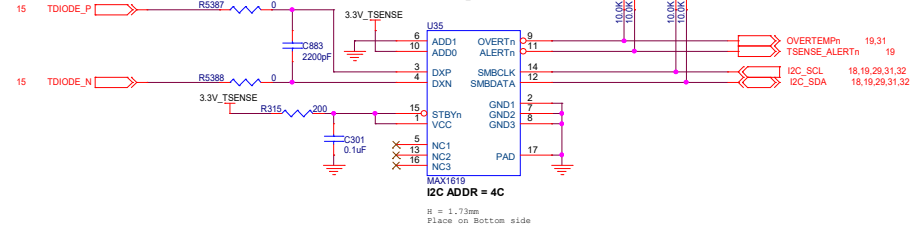
Current Monitor



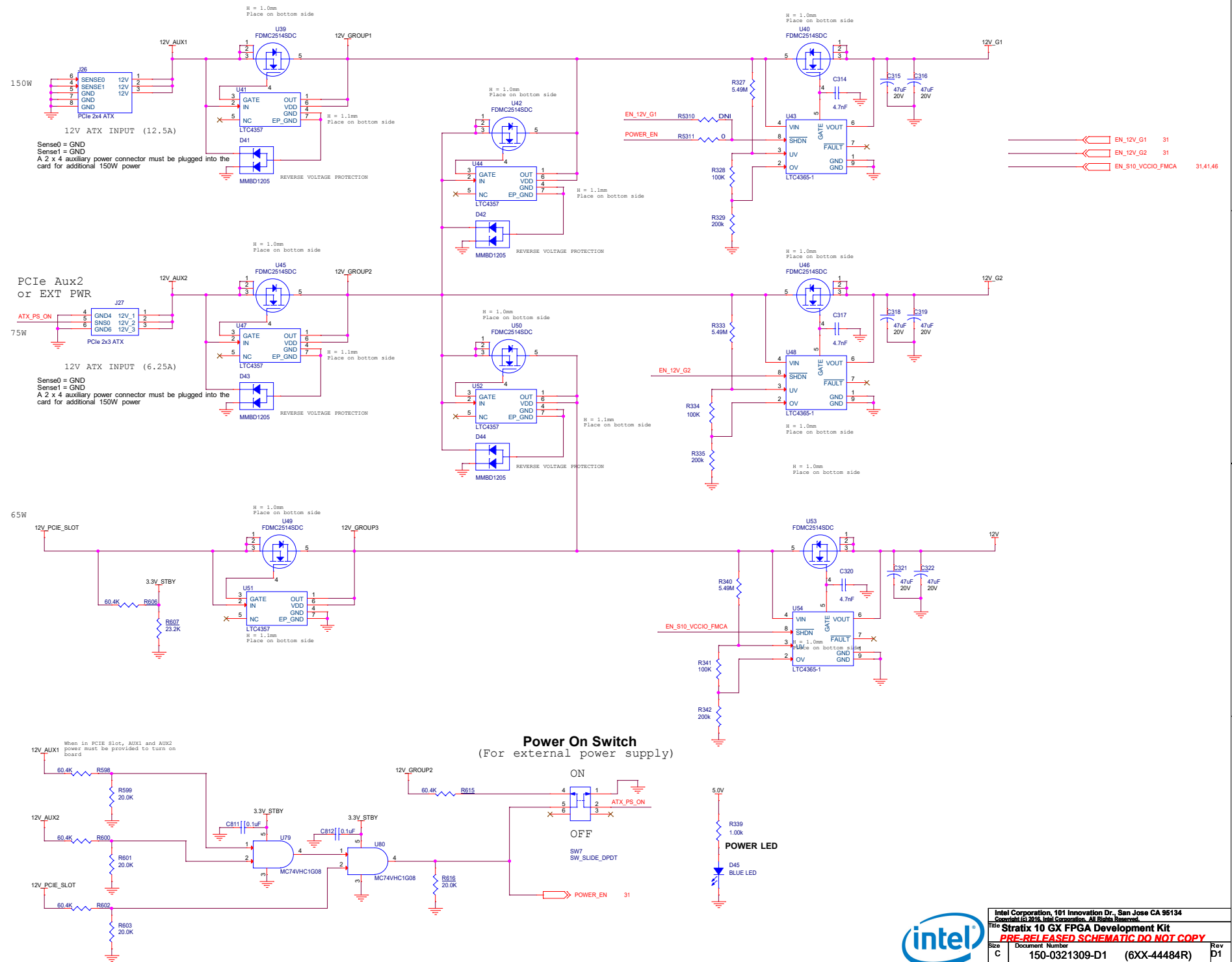
3.3V_TSENSE



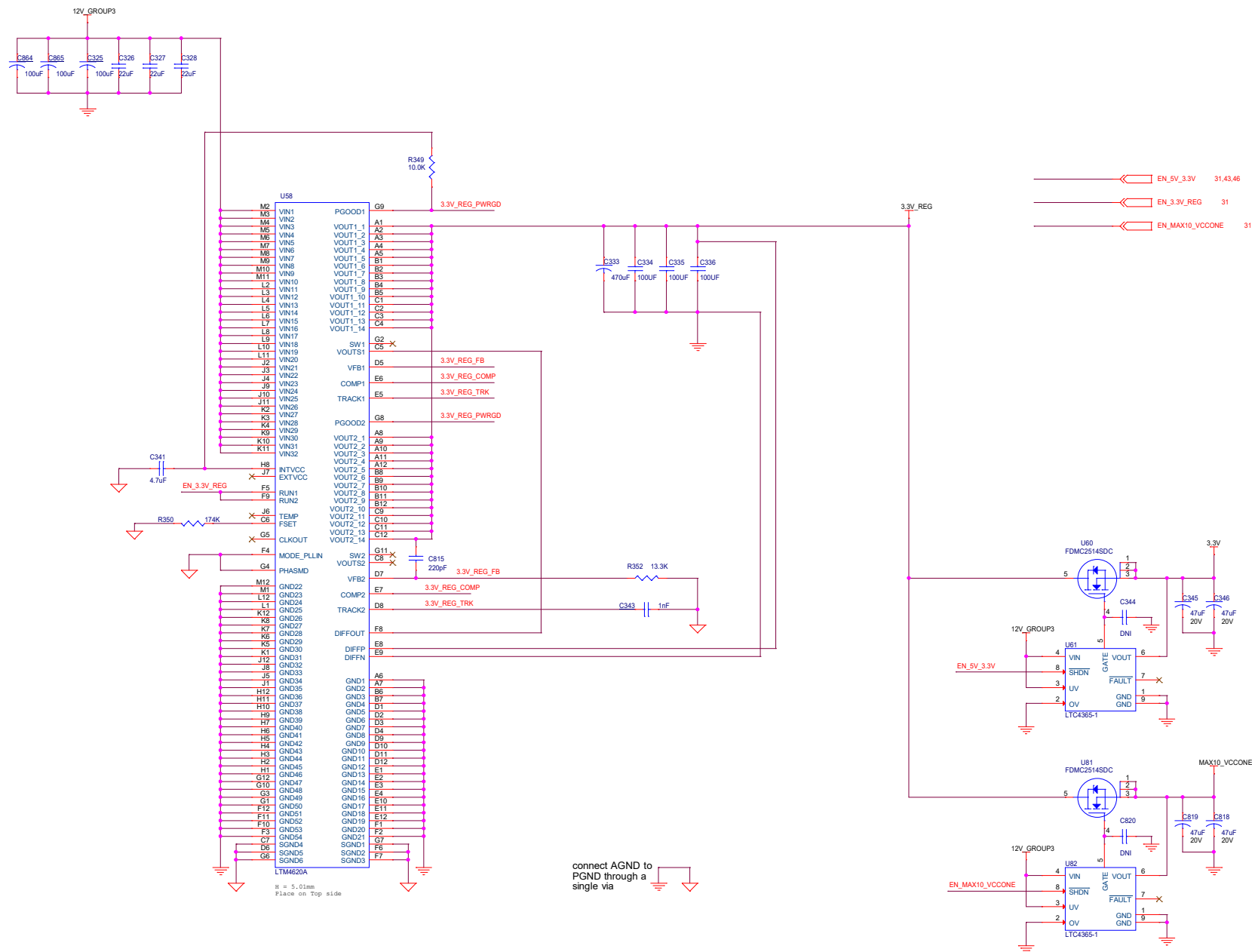
Board Temp Sensor



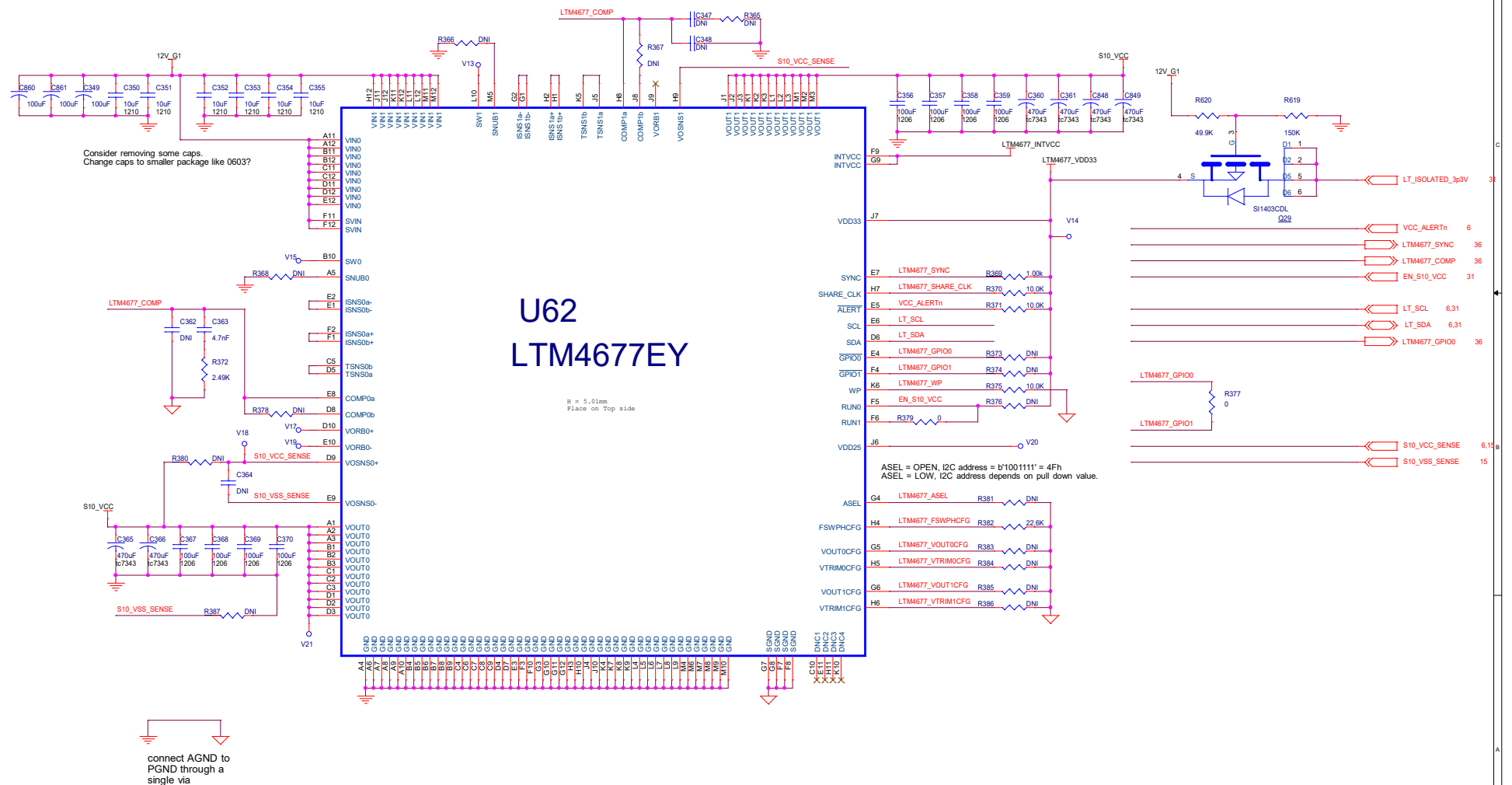
Power - Select Power Input



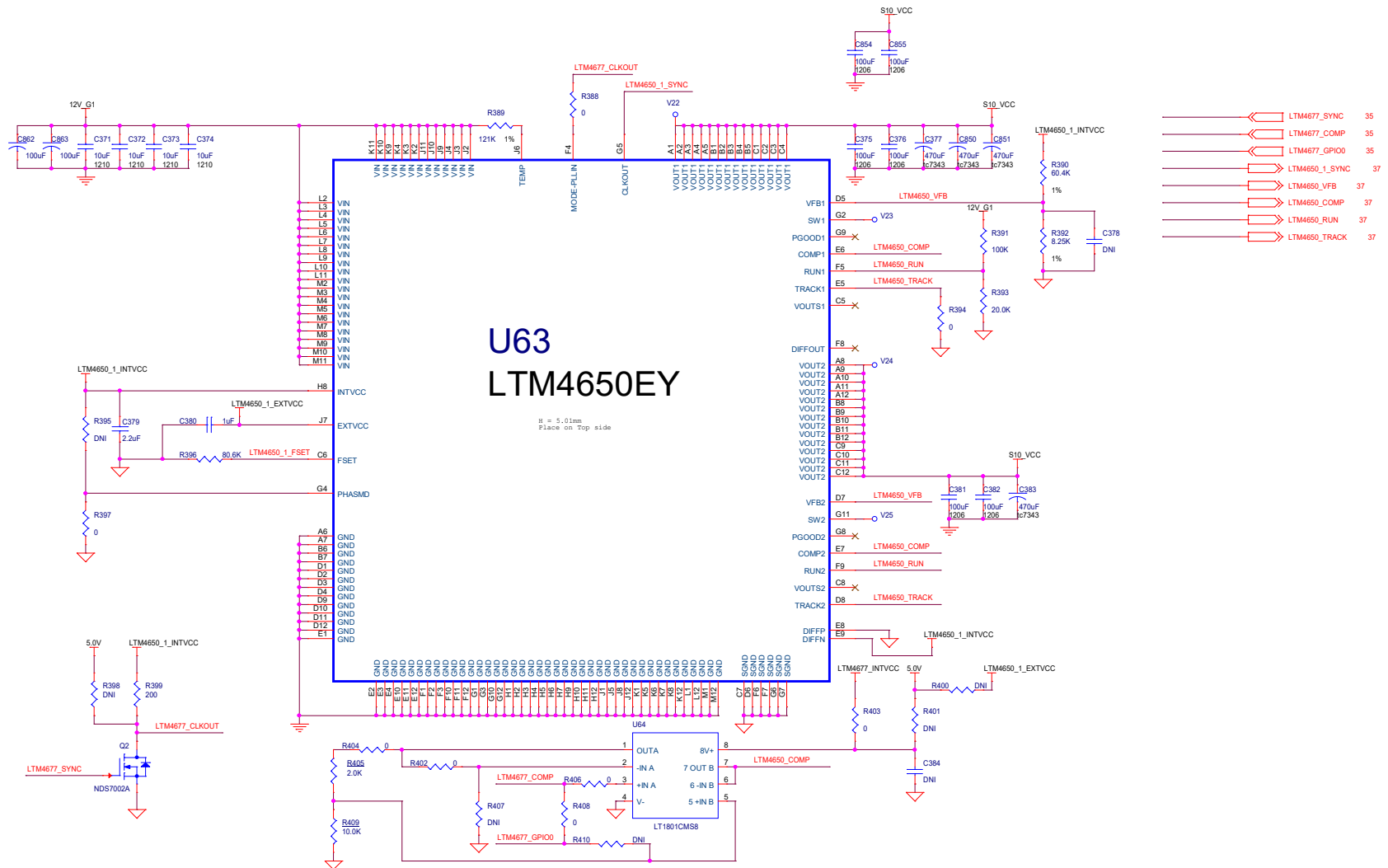
Power - 12V_REG to 3.3V_REG



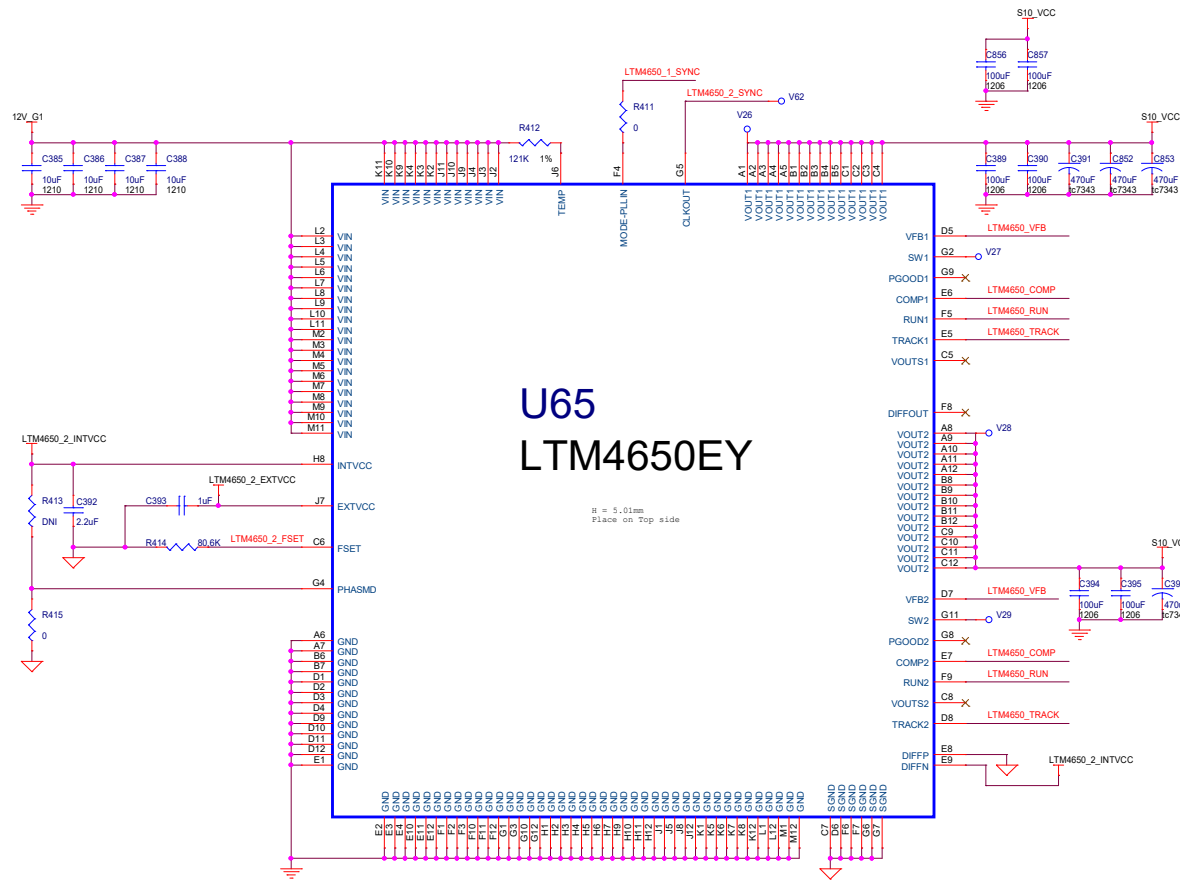
Power - S10 VCC Part 1



Power - S10 VCC Part 2



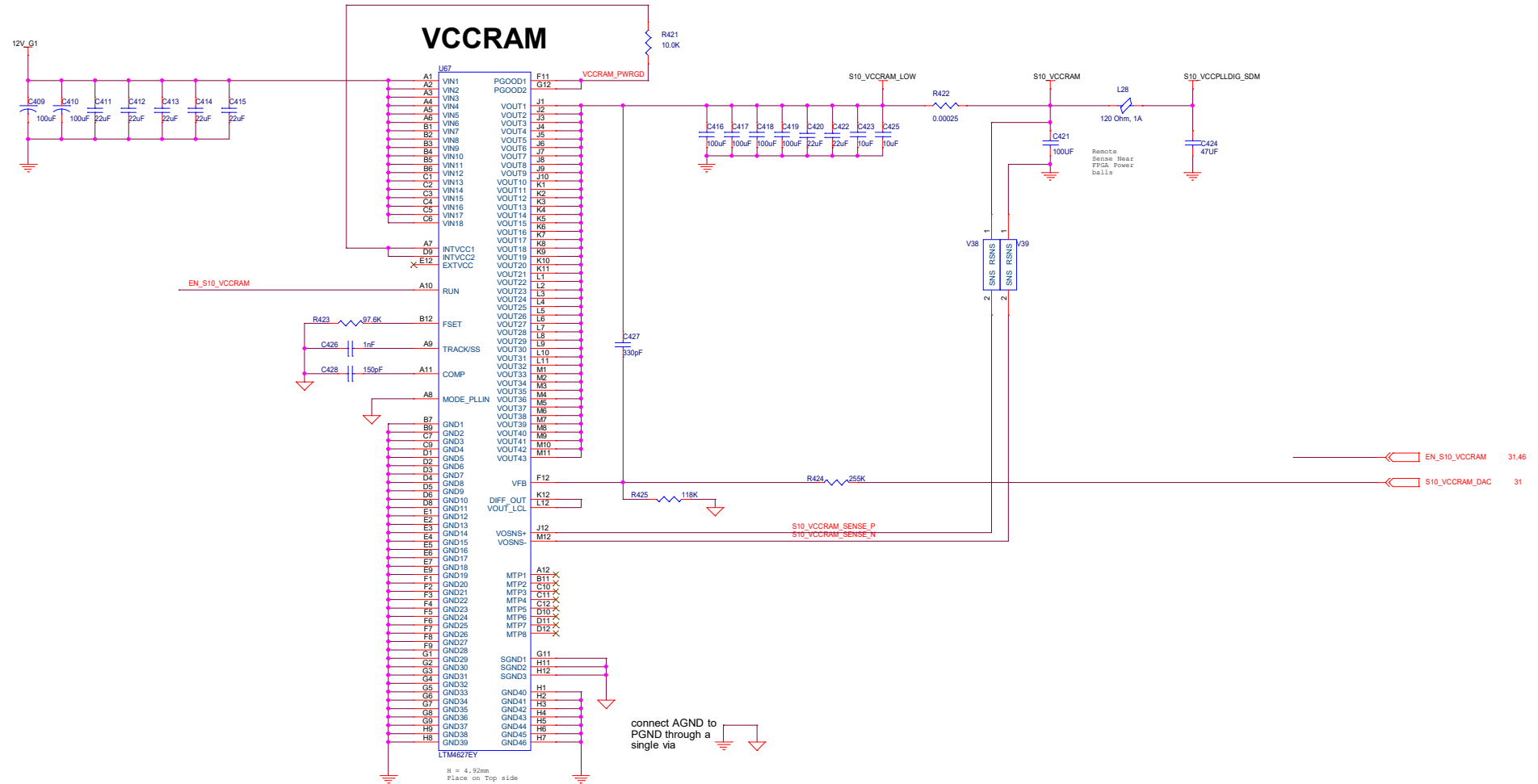
Power - S10 VCC Part 3



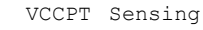
- LTM4650_1_SYNC 36
- LTM4650_VFB 36
- LTM4650_COMP 36
- LTM4650_RUN 36
- LTM4650_TRACK 36



Power - S10 VCCRAM



VCCPT



Power - S10 VCCR_GXB, VCCT_GXB

VCCT_GXB Current Sensing

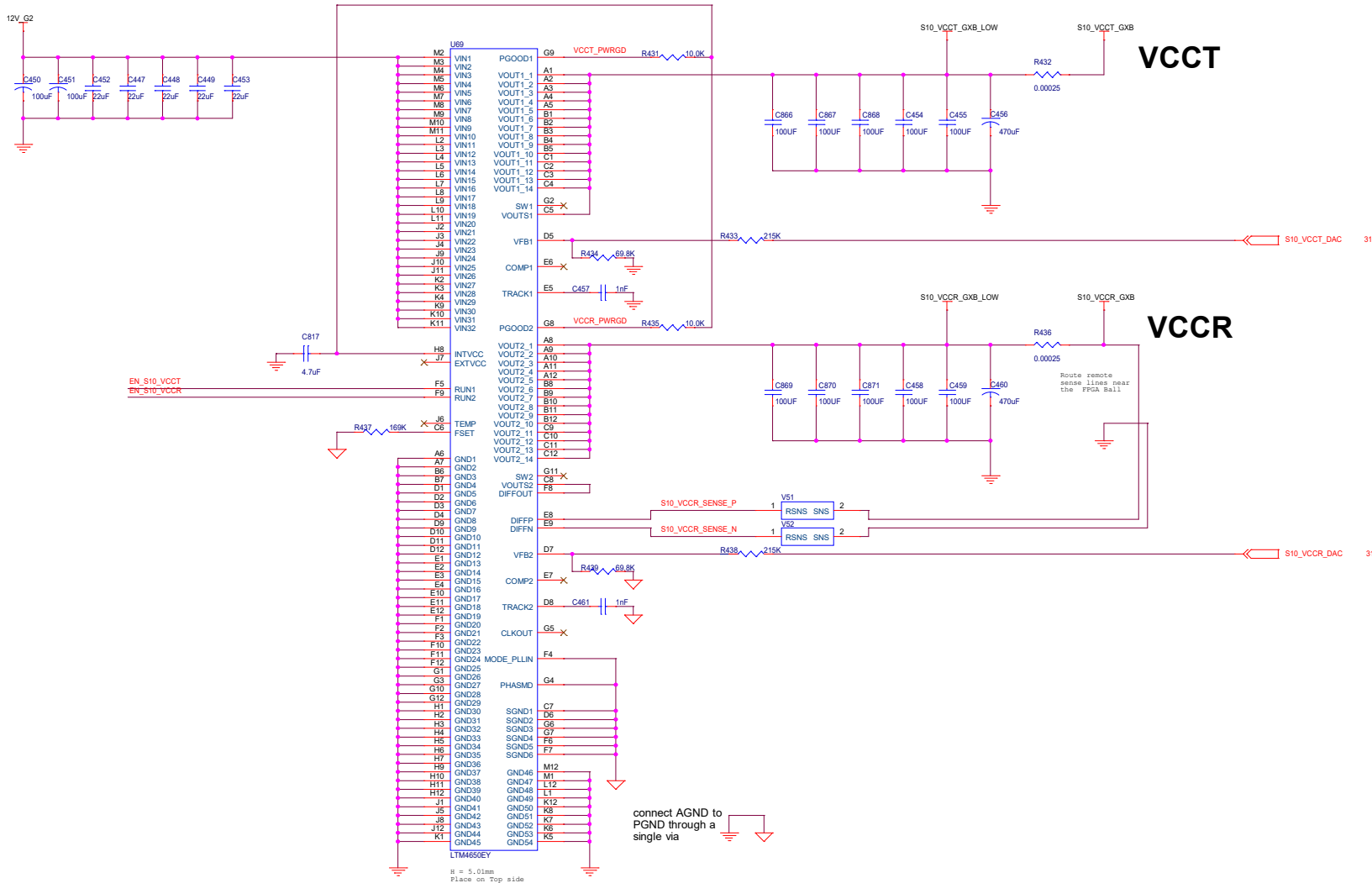


VCCR_GXB Current Sensing



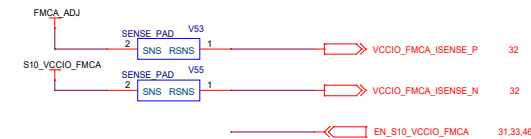
VCCT

VCCR

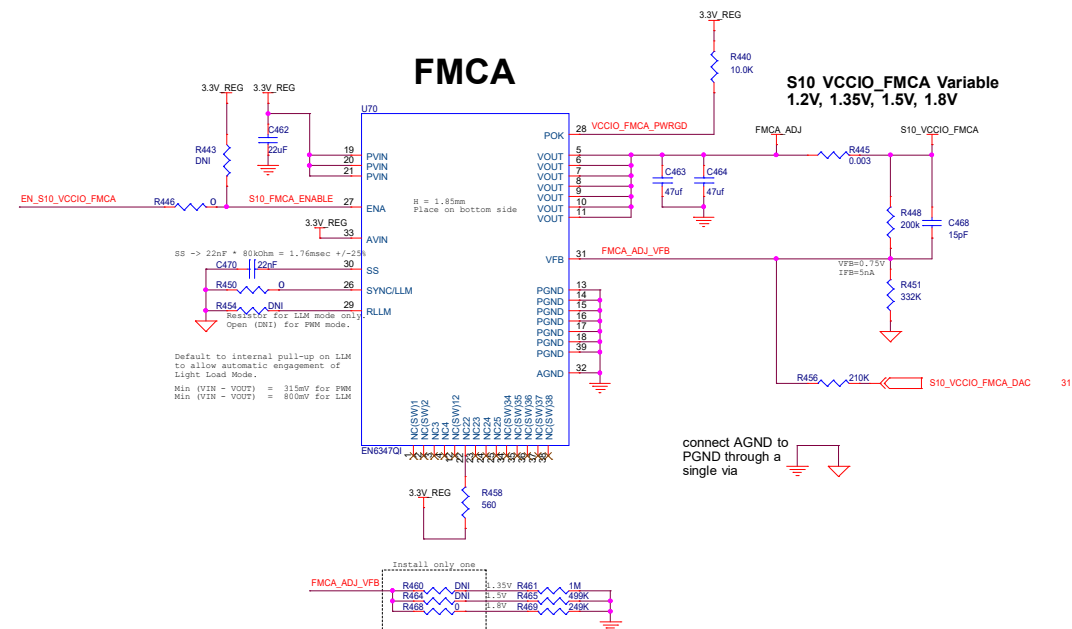


Power - S10 VCCIO FMCA, FMCB

VCCIO_FMCA Current Sensing



FMCA



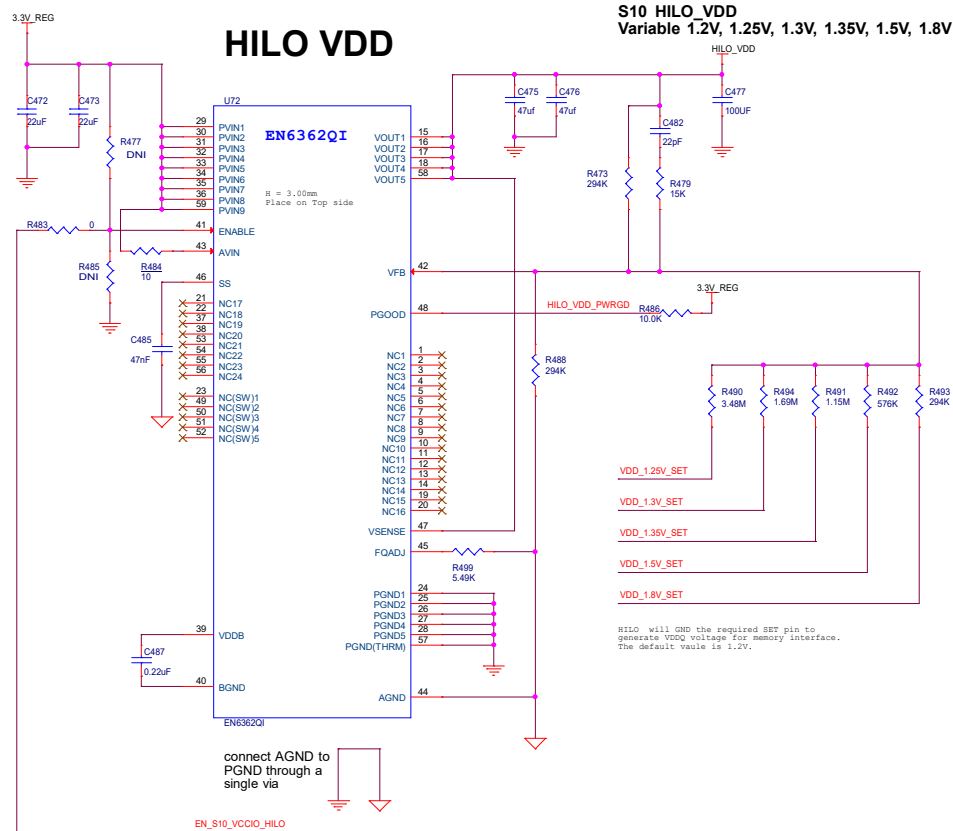
FMCA Voltage

| | |
|-------------------|-----------------|
| Installed | WCCIO FMCA SELE |
| NCNE | 1.2V |
| R460 | 1.35V |
| R464 | 1.5V |
| R468 (Default) | 1.8V |

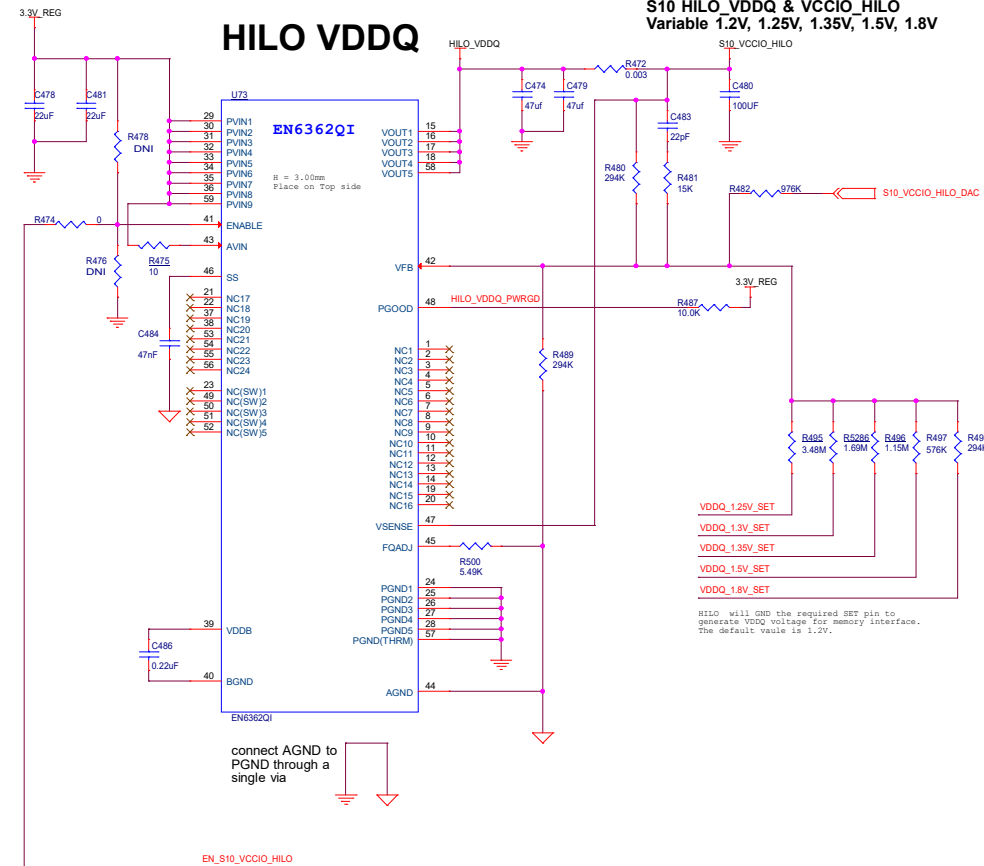


Power - HILO Memory

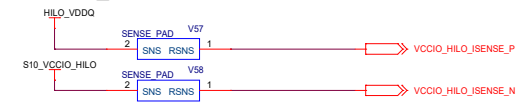
HILO VDD



HILO VDDQ

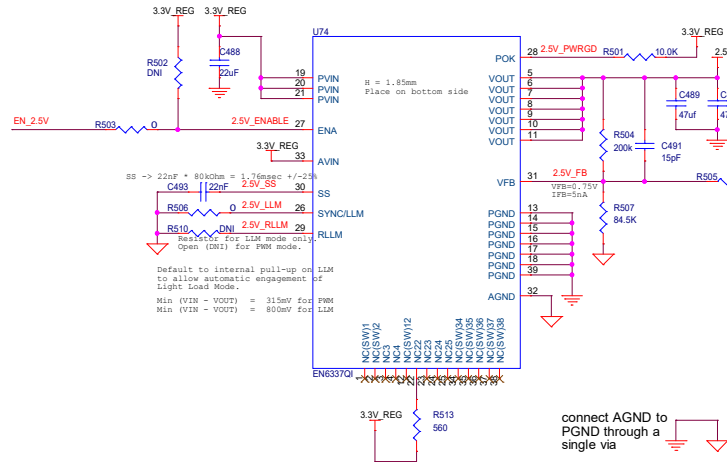


HILO_VCCIO Current Sensing

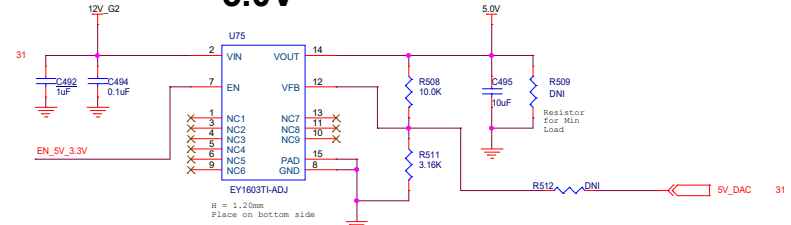


50 - Power - LDO 5.0V, 2.5V, 2.4V, 1.0V

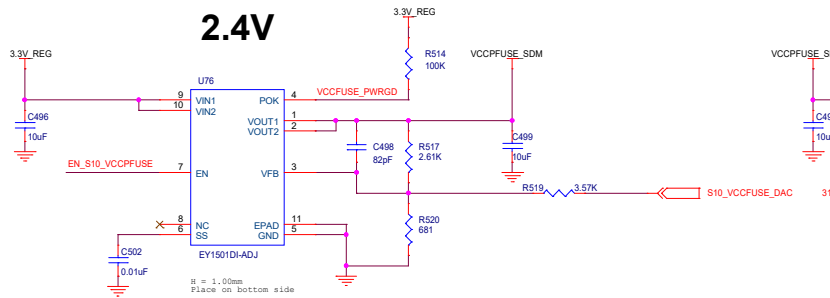
2.5V



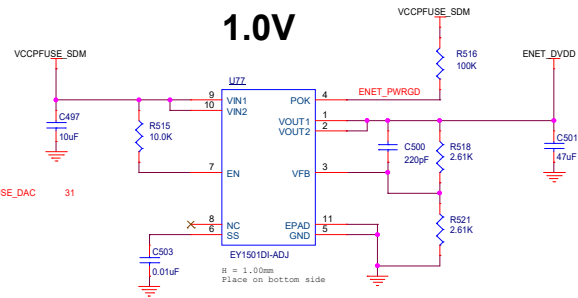
5.0V



2.4V



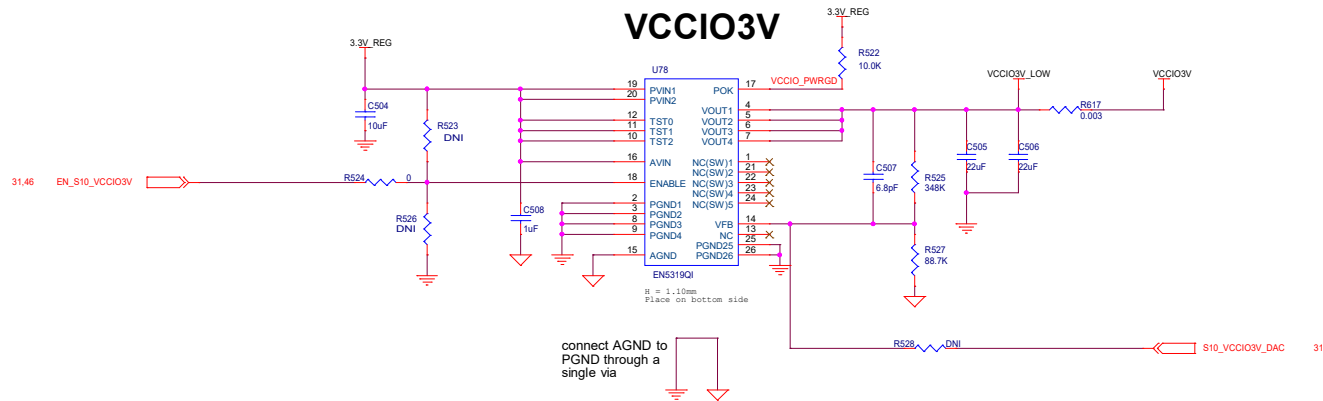
1.0V



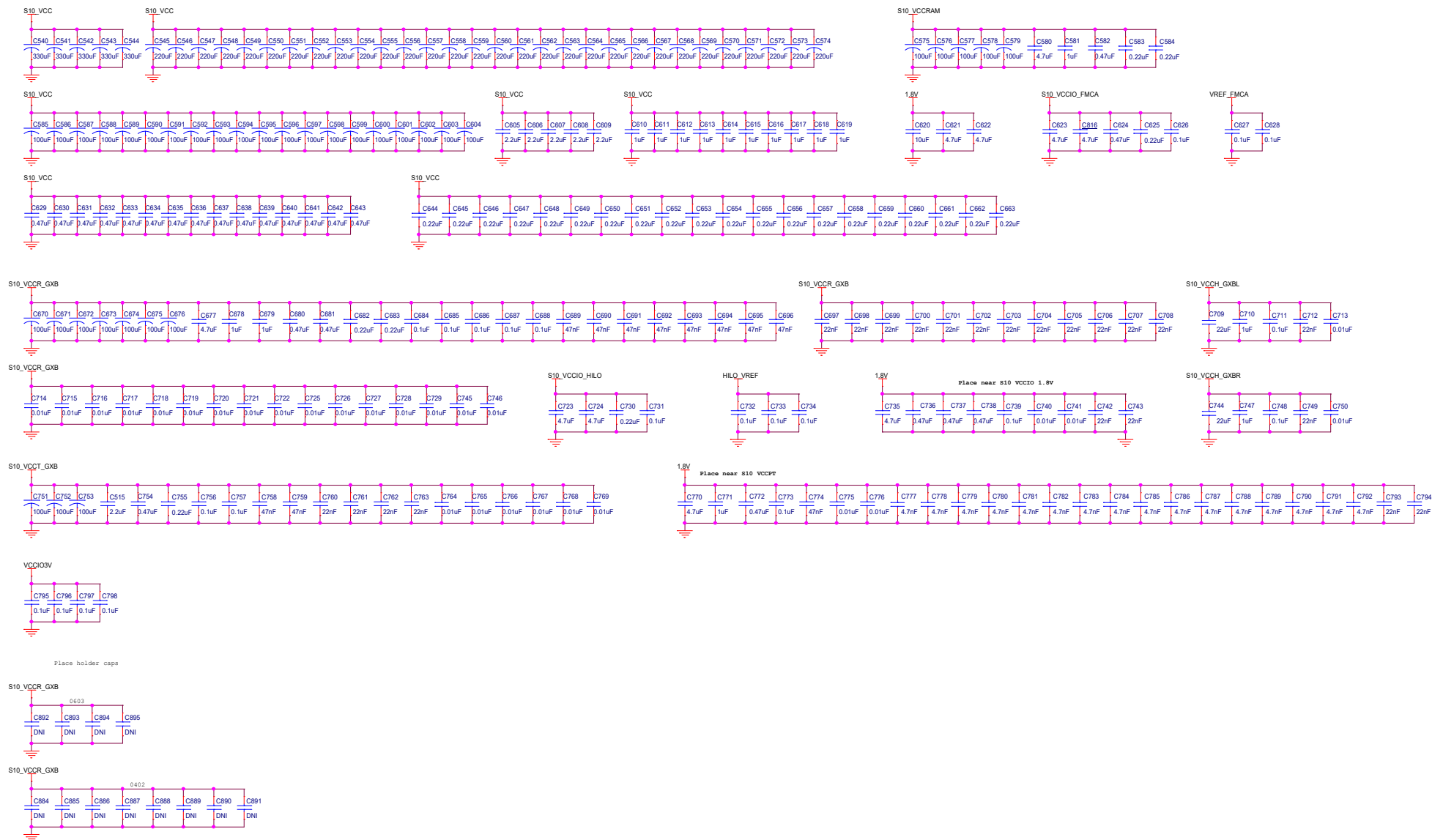
| | |
|-----------------|----------|
| EN_S10_VCCPFUSE | 31,46 |
| EN_2.5V | 31,46 |
| EN_5V_3.3V | 31,34,46 |

VCCIO3V

VCCIO3V Current Sensing



S10 Decoupling



Fast Power-Down Discharge

31.38 EN_S10_VCCRAM
31.40 EN_S10_VCCR
31.40 EN_S10_VCCIO
31.39 EN_1.8V
31.33,41 EN_S10_VCCIO_FMCA

31.42 EN_S10_VCCIO_HILO
31.44 EN_S10_VCCIO3V
31.43 EN_S10_VCCPFUSE
31.43 EN_2.5V
31.34,43 EN_5V_3.3V

