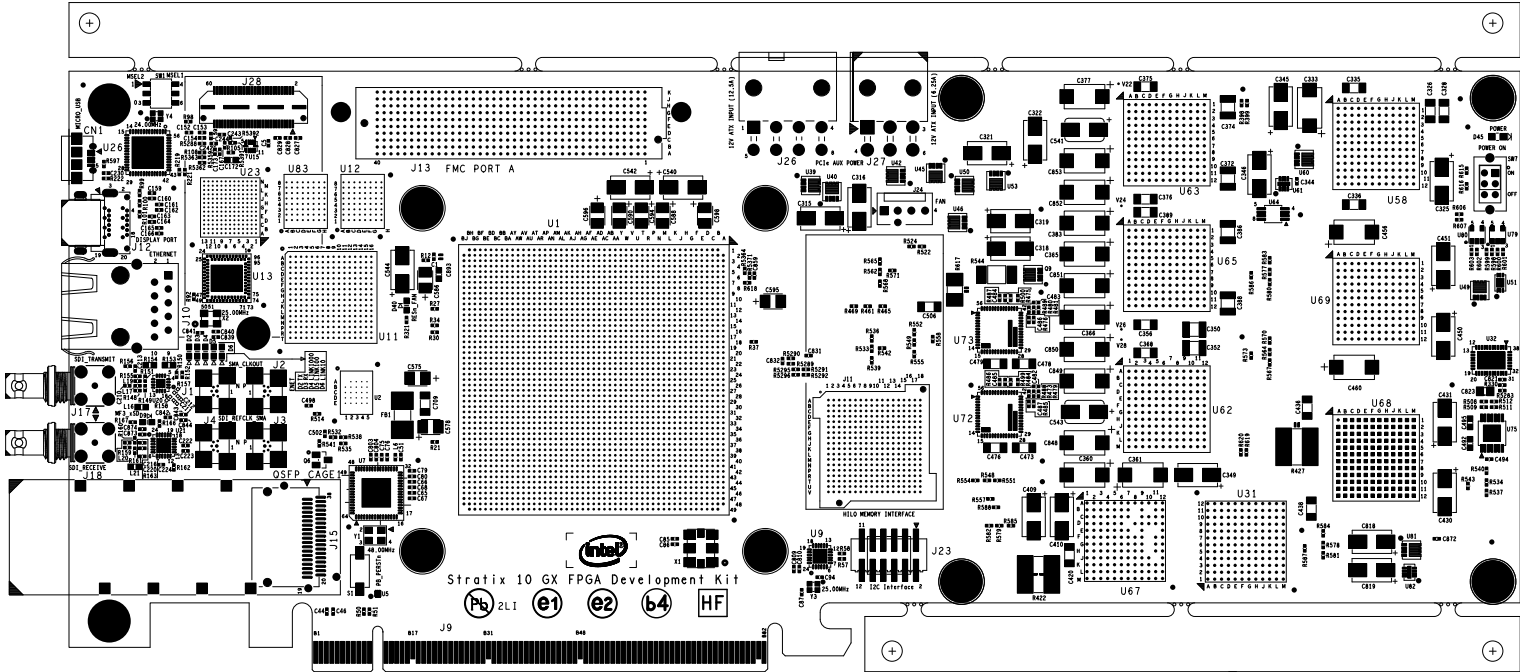


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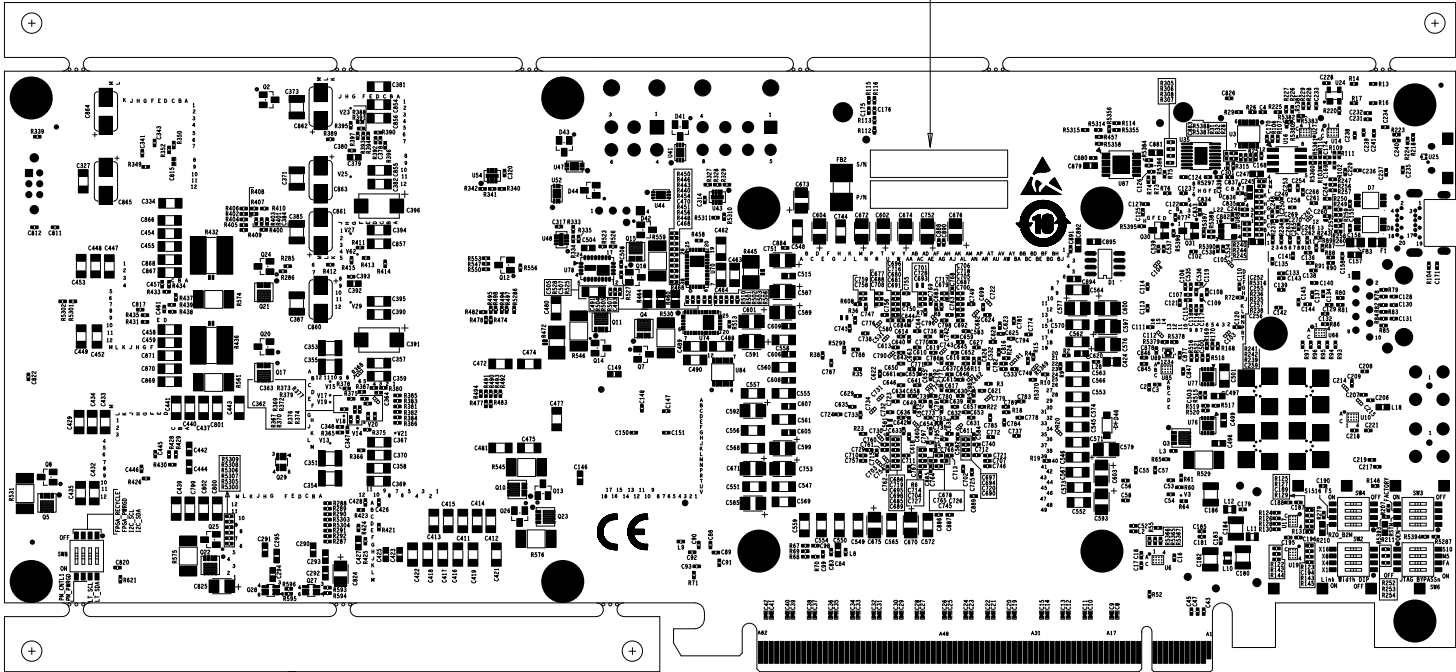
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

NOTES: UNLESS OTHERWISE SPECIFIED


1. ASSEMBLY HOUSE TO VISUALLY VERIFY BOARD BEING ASSEMBLED HAS INTEL P/N 100-0321309-D1 REV D1 IN ETCH ON BOTTOM SIDE.
2. BOARDS MUST BE BAKED FOR A DURATION OF 8 HOURS AT 250 DEGREES FARENHEIT IMMEDIATELY PRIOR TO ASSEMBLY.
3. ASSEMBLE BOARD PER IPC-A-610 (LATEST REVISION) STANDARD.
4. ALL MATERIALS USED MUST BE ROHS COMPLIANT.
5. HANDLE MOISTURE SENSITIVE DEVICES (MSD) PER MANUFACTURE'S CALL OUT ON MSD LABEL. IF MSD LABEL IS MISSING OR NOT LEGIBLE THEN ALL PLASTIC PACKAGED COMPONENTS ARE TO BE CONSIDERED MSD LEVEL 6 AND USE EIA/JEP 113-A FOR HANDLING.
6. SQUARE PIN PAD DENOTE PIN 1 OF ICs/CONNECTORS, POSITIVE END FOR CAPACITORS OR CATHODE END FOR DIODES.
7. REWORK MUST BE APPROVED BY CUSTOMER BEFORE BEING ACCEPTIBLE USE IPC-R-700 (LATEST REVISION) FOR ALL PCA REWORK APPROVED.
8. INSTALL BAR CODE LABEL APPROX WHERE SHOWN, INCLUDING S/N.
9. VENDOR TO KEEP QUALITY CONTROL INK STAMPINGS OFF SIGNAL TRACES AND PADS EVEN IF COVERED BY SOLDERMASK.



TOP SIDE SHOWN



BOTTOM SIDE SHOWN

				MATL		DWN ACRONICS 07-MAR-2017		<div>intel®</div> <div>(c) 2017 INTEL Corporation</div>			
				SPEC		CHKR					
- XX-XXX-XXXX						DSGN ENGR CUONG					
DASH NEXT ASSY		USED ON		FNSH		RELEASE					
APPLICATION								TITLE PCB ASSEMBLY STRATIX 10 GX FPGA DEVELOPMENT KIT			
THIRD ANGLE PROJECTION 		UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES IN ACCORDANCE WITH ANSI Y14.5. DRILL TOLERANCES ARE PER 10387		TOLERANCES: DEC .X ± DEC .XX ± .01 DEC .XXX ± .005 DEC .XXXX ± .002 FRACTIONS ± ANGLES ± 1°		CONTRACT NO. XXXXXX					
						SIZE D		CAGE CODE N/A	DWG NO. 130-0321309-D1	REV D1	
								SCALE: 1/1		SHEET 1 OF 1	