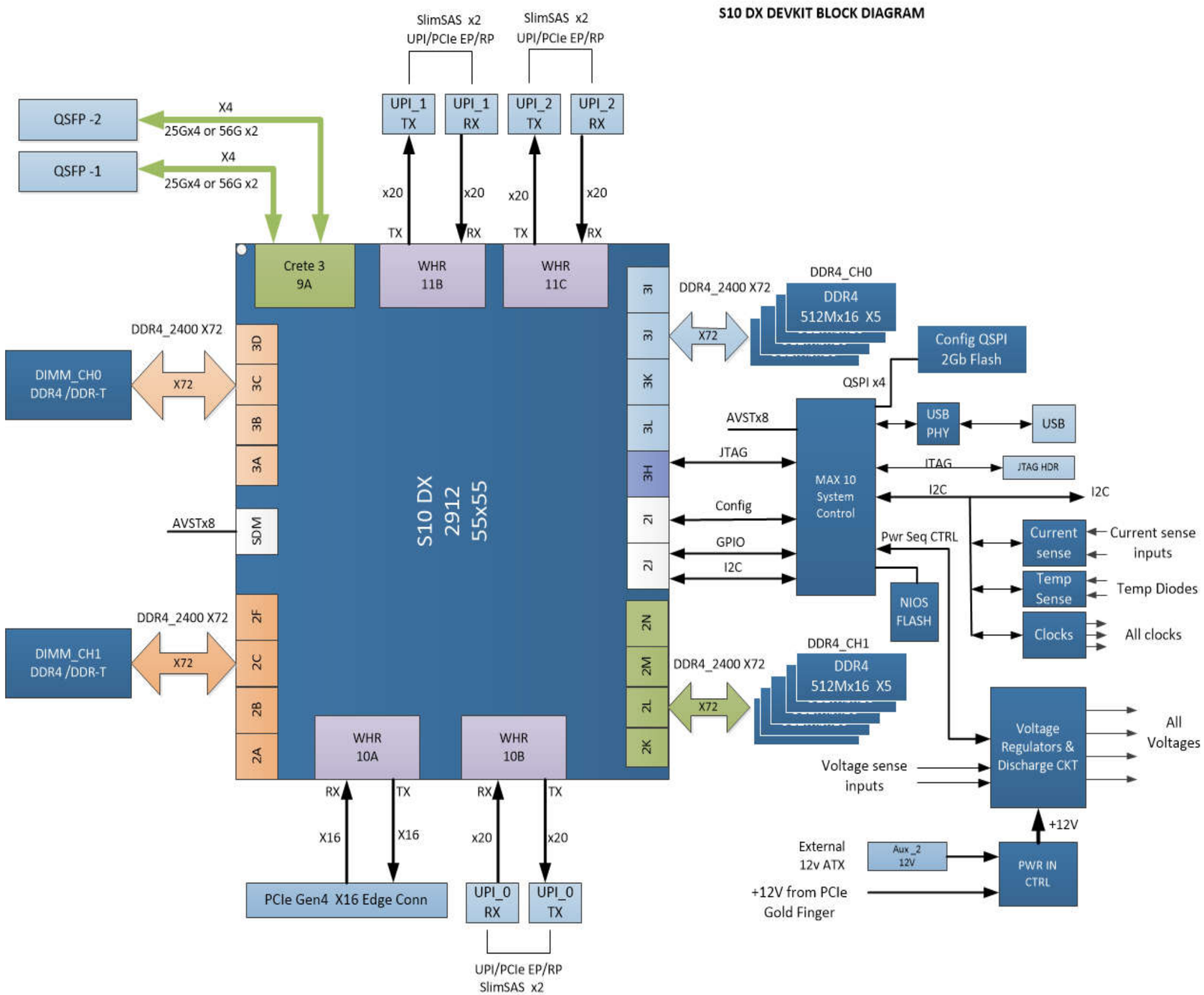
Title, Note, Block Diagram



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3	Diag - Power Sequence
4	Diag - I2C
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8	S10 DX Bank 2J
9	S10 DX Bank 2K,L,M,N
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12	S10 DX Bank 3H,L
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44	Power-S10_VCCH_GXE
45	Power-S10_VCCH_GXP
46	Power-S10_VCCCLK_GXE
47	Blank
48	Blank
49	12V AUX 2 Hotswap
50	Power- S10 VCCPT_1.8V
51	Power-1.8V
52	S10 Decoupling
53	Fast Power-Down Discharge
54	12V_AUX 1 Hotswap
55	12V_PCIE Hotswap
56	Power - Max10 BMC
57	Power - 5V
58	Power - VCCcore part1
59	Power - VCCcore part2
60	Power - VCCcore part3
61	Power - VCCcore part4
62	Power - VCCERAM
63	Power - 3.3V_REG_INST
64	Power - 2.4V VCCPFUSE_SDM
65	Power - 2V5_DDR4, DDR4_VTT
66	Power-1V2_DDR4_CH11
67	Power-1V2_DDR4_CH00
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69	Level Translators 2

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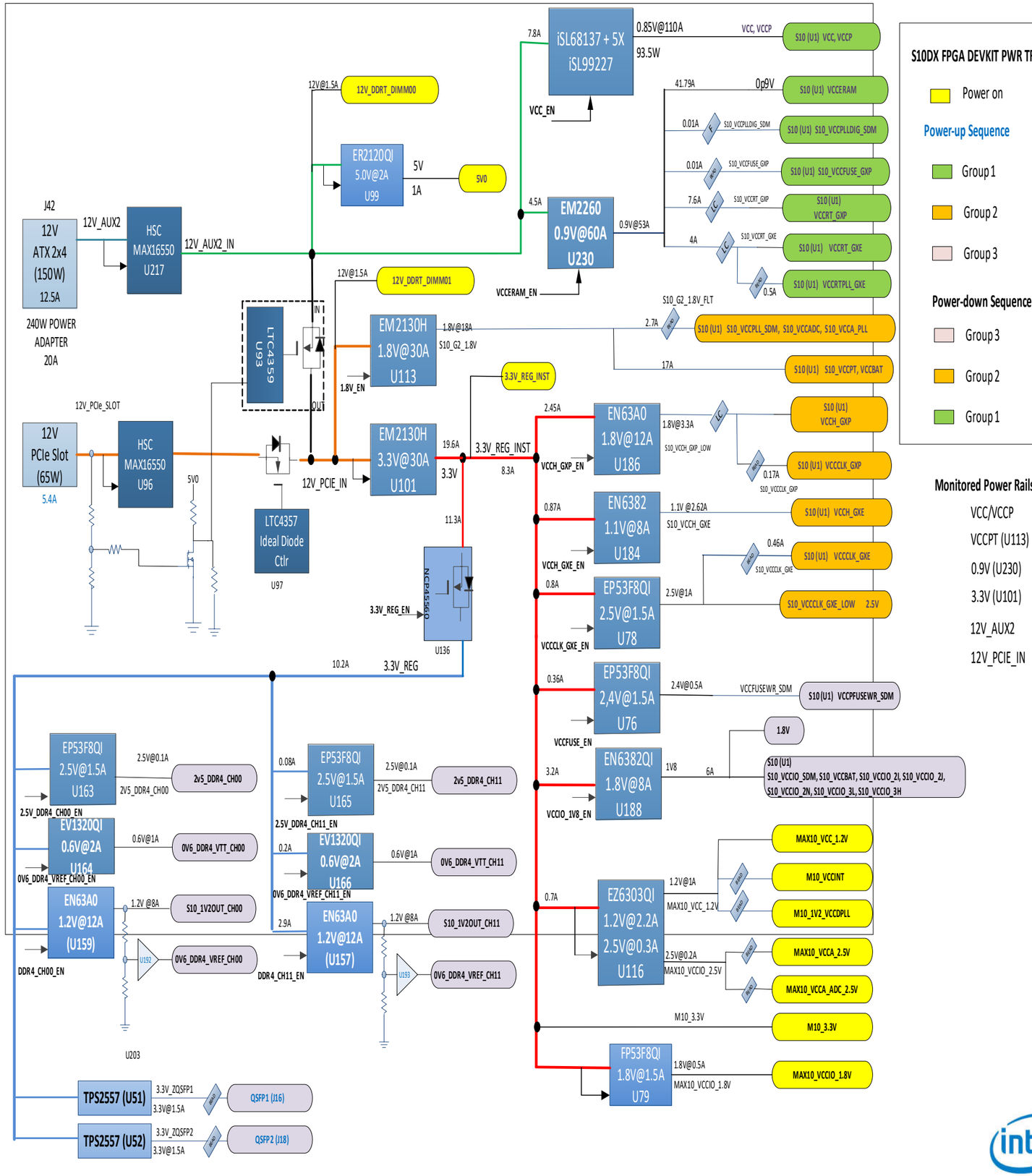

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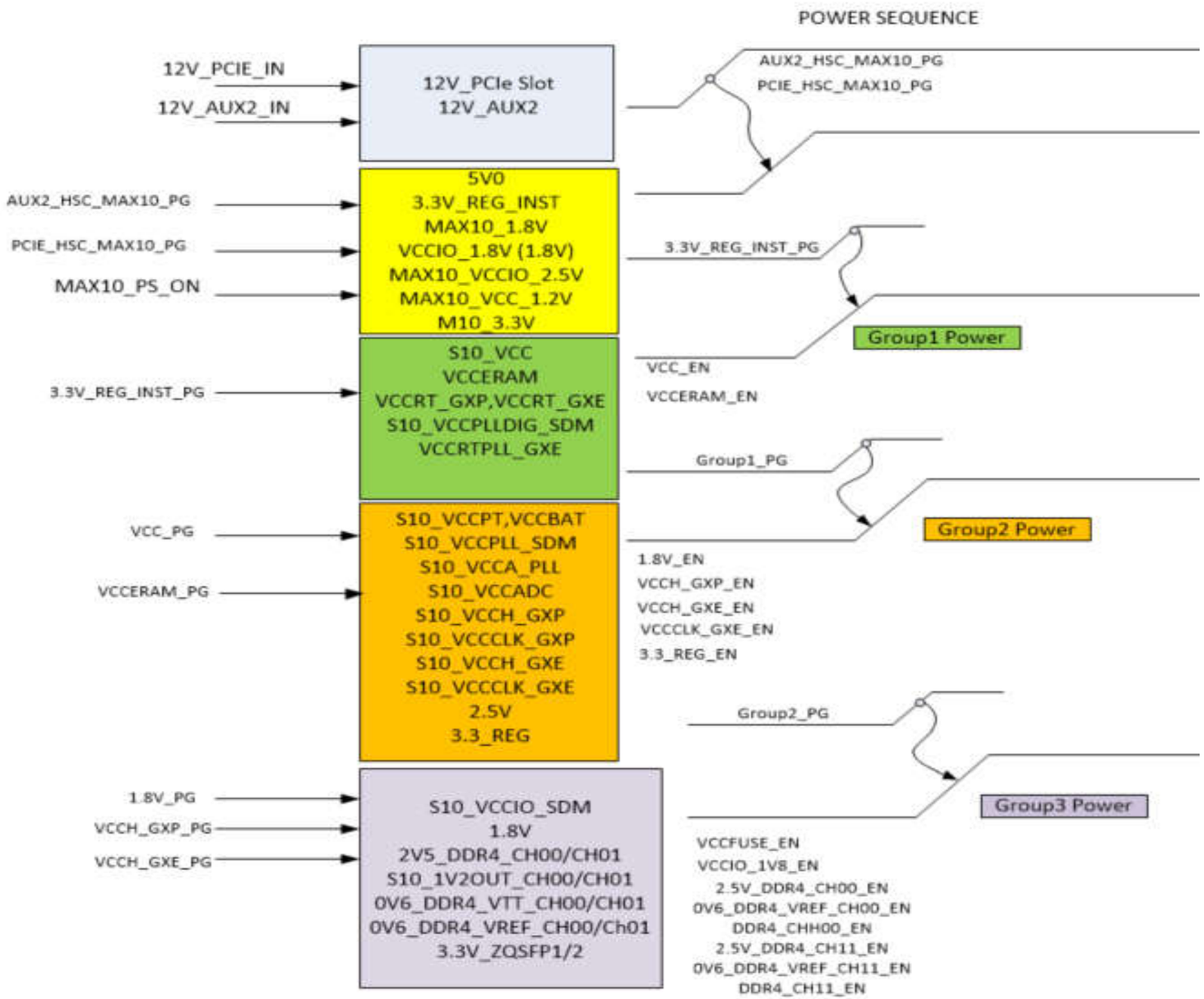
Power Sequence Diagram



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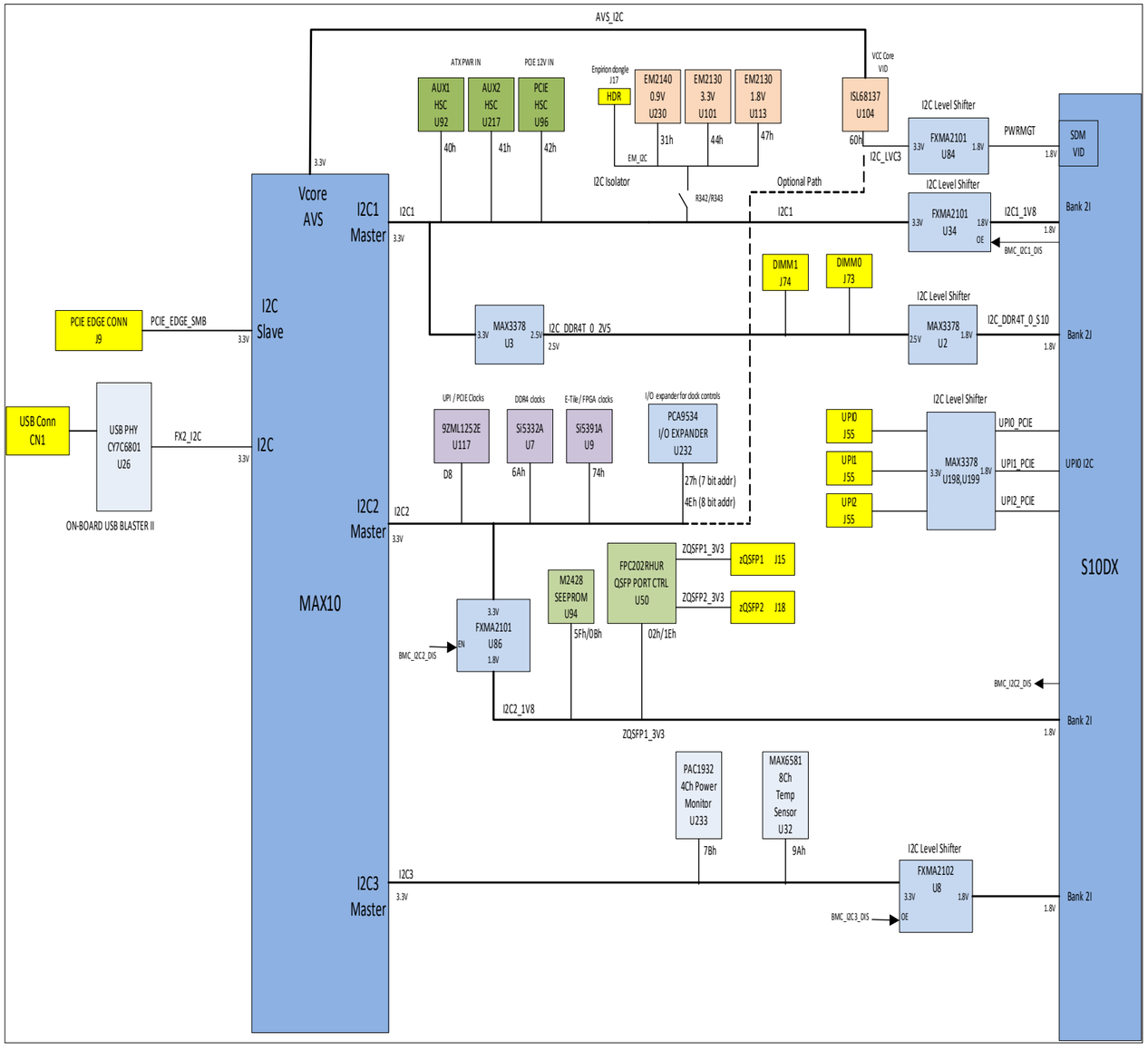
I2C & JTAG DIAGRAM



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Title	Stratix 10 DX FPGA DEVKIT Board	
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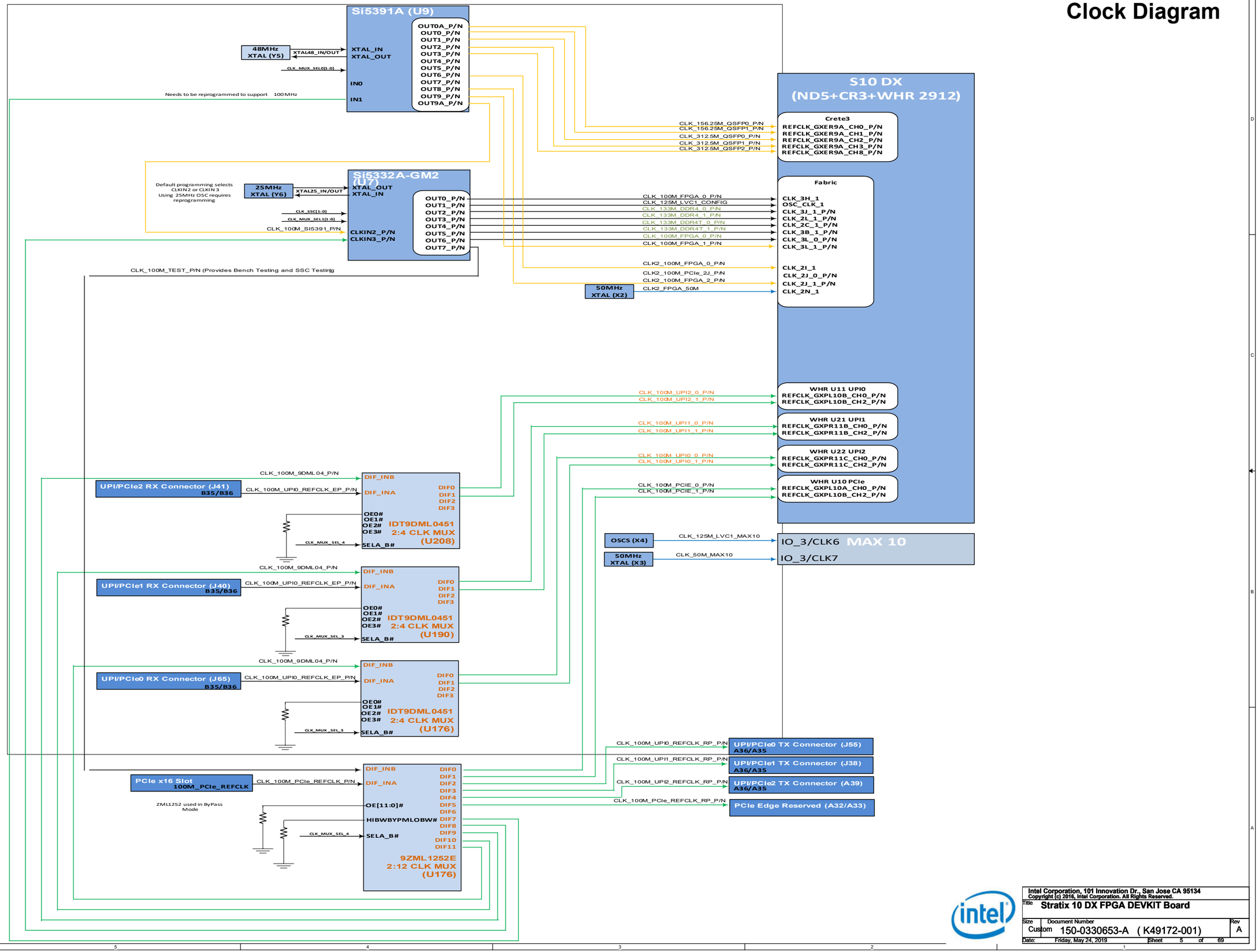
Clock Diagram



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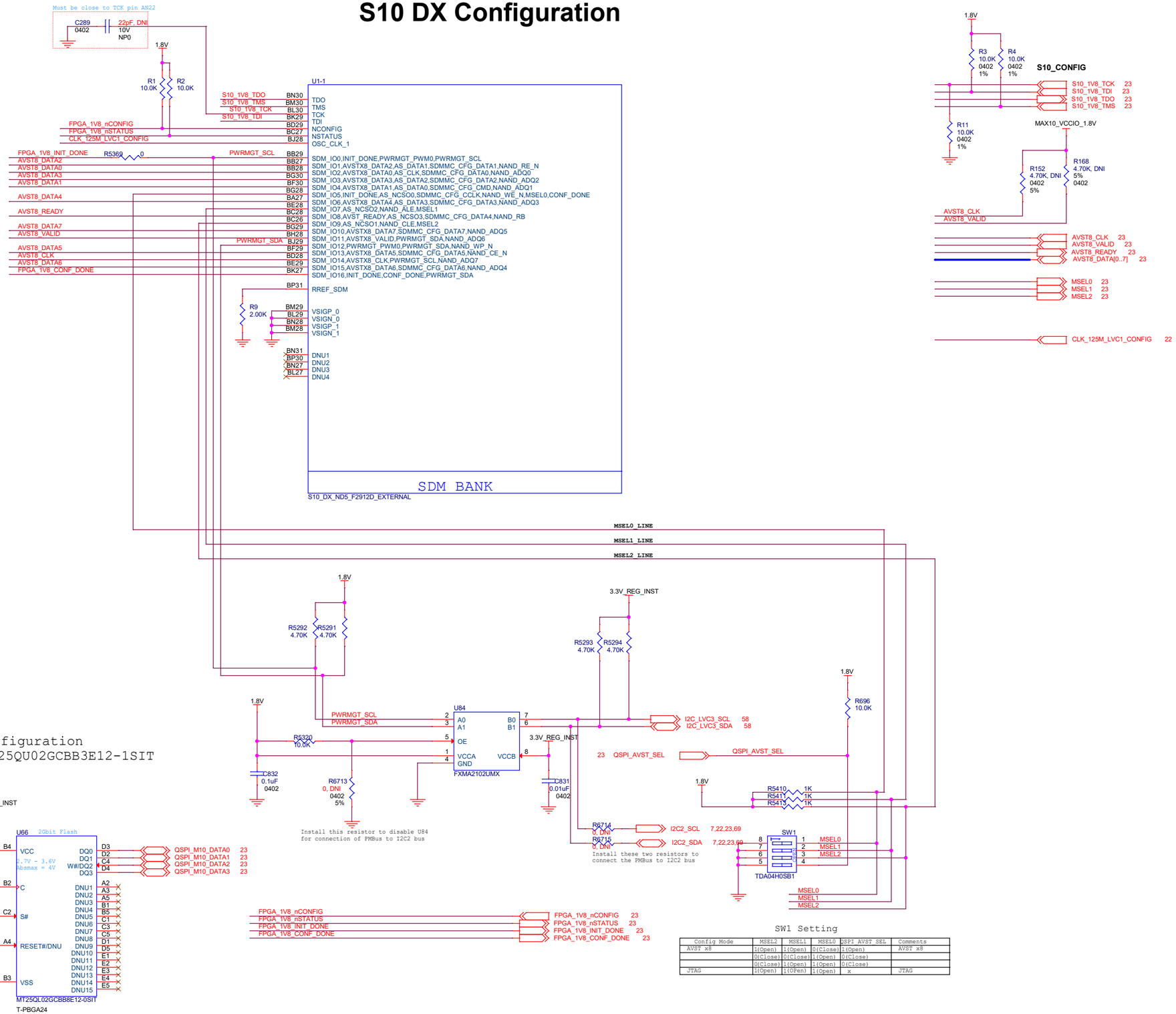
S10 DX Configuration



SW1 Setting

Config Mode	MSEL2	MSEL1	MSEL0	QSPI AVST SEL	Comments
AVST x8	1(Open)	1(Open)	0(Close)	1(Open)	AVST x8
	0(Close)	0(Close)	1(Open)	0(Close)	
	0(Close)	1(Open)	1(Open)	0(Close)	
JTAG	1(Open)	1(OPen)	1(Open)	x	JTAG

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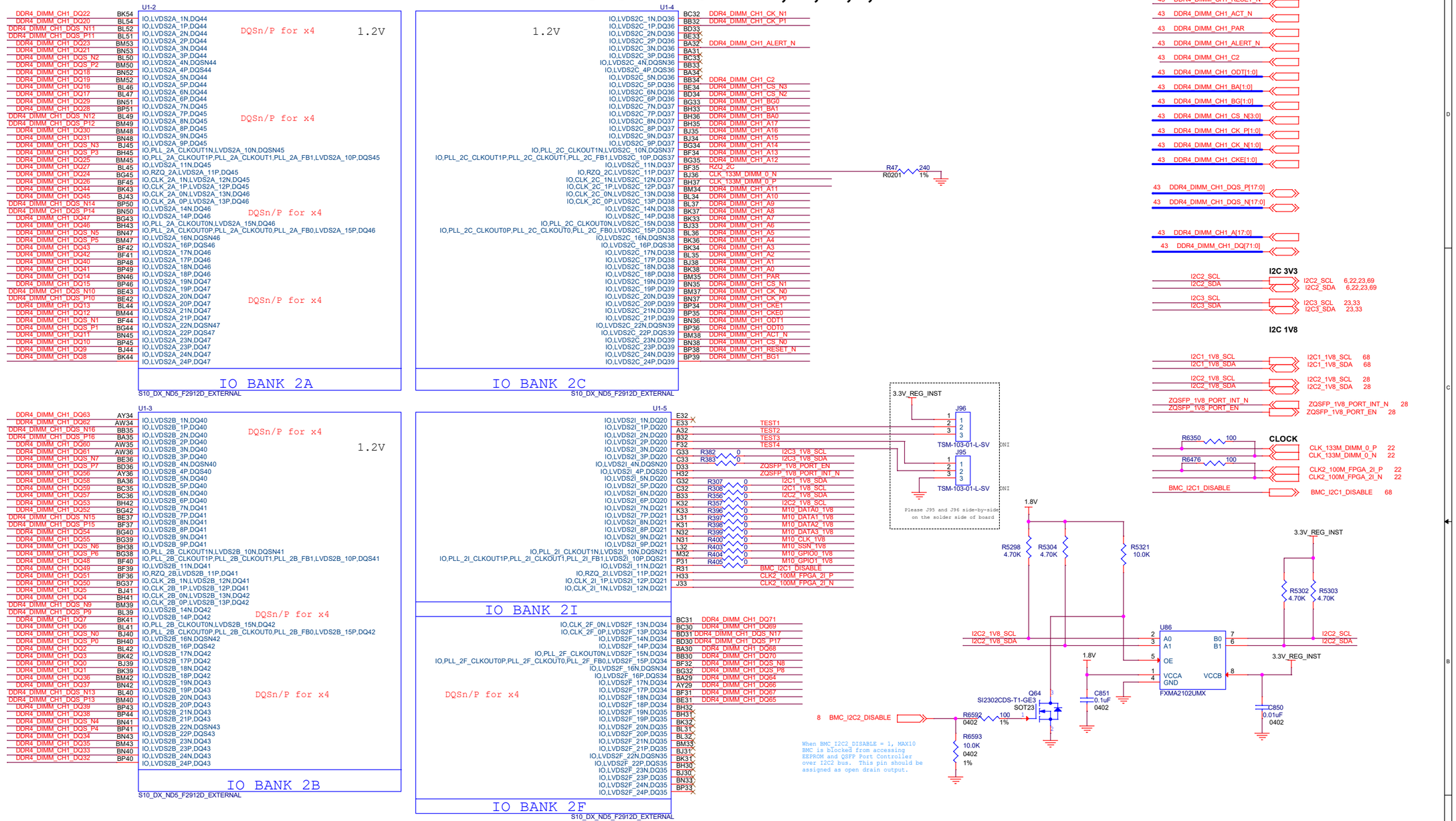
S10 DX Bank 2A, B, C, I, F



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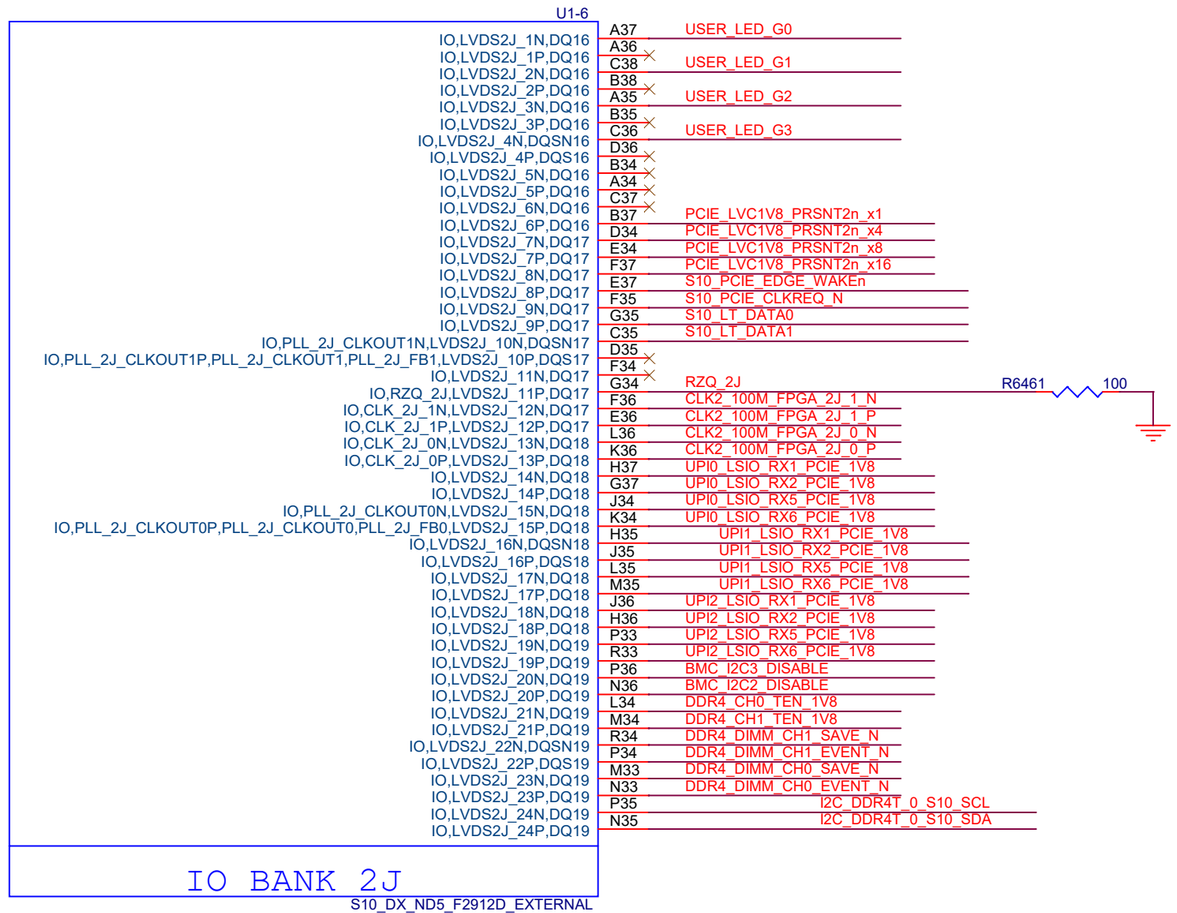
S10 DX Bank 2J



R6461 100

S10_LT_DATA0 68
S10_LT_DATA1 68

S10_PCIE_CLKREQ_N 68
S10_PCIE_EDGE_WAKEn 68

PCIE_LVC1V8_PRSNT2n_x1 68
PCIE_LVC1V8_PRSNT2n_x4 68
PCIE_LVC1V8_PRSNT2n_x8 68
PCIE_LVC1V8_PRSNT2n_x16 68

DDRT DIMM

DDR4_DIMM_CH0_SAVE_N 42
DDR4_DIMM_CH0_EVENT_N 42

DDR4_DIMM_CH1_EVENT_N 43
DDR4_DIMM_CH1_SAVE_N 43

DDR COMP

DDR4_CH0_TEN_1V8 36
DDR4_CH1_TEN_1V8 40

I2C_DDR4T_0_S10_SCL 42
I2C_DDR4T_0_S10_SDA 42

1.8V

I2C_DDR4T_0_S10_SCL R5722 10.0K
I2C_DDR4T_0_S10_SDA R5723 10.0K

DDR4_DIMM_CH0_SAVE_N R5729 10.0K
DDR4_DIMM_CH0_EVENT_N R5730 10.0K

DDR4_DIMM_CH1_SAVE_N R5737 10.0K
DDR4_DIMM_CH1_EVENT_N R5738 10.0K

LED INTERFACE

USER_LED_G[3:0] 31

CLOCK

R6351 DNI

CLK2_100M_FPGA_2J_1_N 22
CLK2_100M_FPGA_2J_1_P 22

R6394 100

CLK2_100M_FPGA_2J_0_N 22
CLK2_100M_FPGA_2J_0_P 22

BMC_I2C3_DISABLE 7
BMC_I2C2_DISABLE 7

UPI0_LSIO_RX1_PCIE_1V8 69
UPI0_LSIO_RX2_PCIE_1V8 69
UPI0_LSIO_RX5_PCIE_1V8 69
UPI0_LSIO_RX6_PCIE_1V8 69
UPI1_LSIO_RX1_PCIE_1V8 69
UPI1_LSIO_RX2_PCIE_1V8 69
UPI1_LSIO_RX5_PCIE_1V8 69
UPI1_LSIO_RX6_PCIE_1V8 69
UPI2_LSIO_RX1_PCIE_1V8 69
UPI2_LSIO_RX2_PCIE_1V8 69
UPI2_LSIO_RX5_PCIE_1V8 69
UPI2_LSIO_RX6_PCIE_1V8 69

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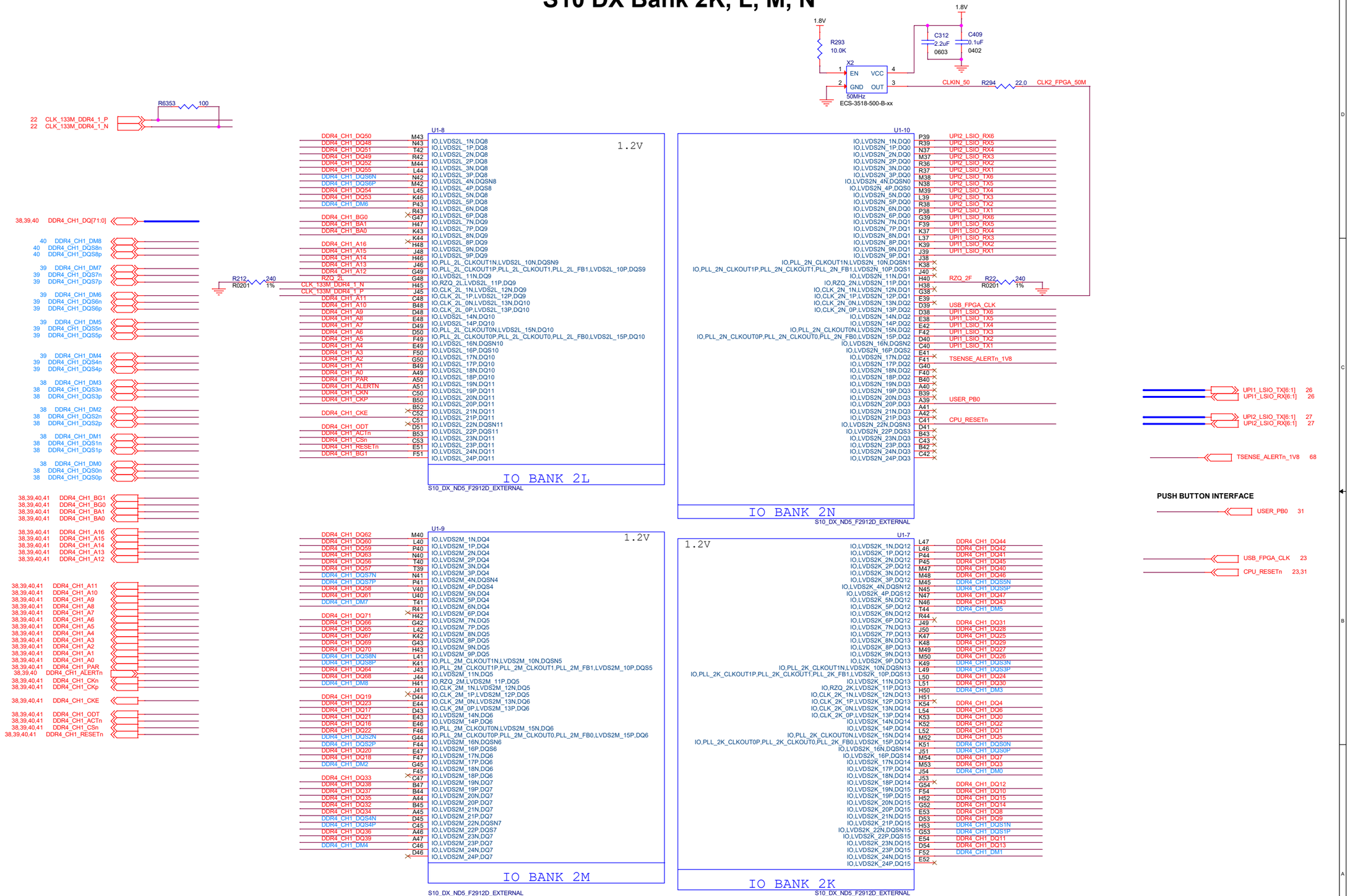
S10 DX Bank 2K, L, M, N



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Title: **Stratix 10 DX FPGA DEVKIT Board**

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S10 DX Bank 3A, B, C, D

U1-11

1.2V

DDR4_DIMM_CH0_DQ12	BP24	IO,LVDS3A_1n,DQ92,AVST_DATA0	
DDR4_DIMM_CH0_DQ13	BP23	IO,LVDS3A_1p,DQ92,AVST_DATA1	
DDR4_DIMM_CH0_DQS_N10	BP26	IO,LVDS3A_2n,DQ92,AVST_DATA2	DQSn/P for x4
DDR4_DIMM_CH0_DQS_P10	BN26	IO,LVDS3A_2p,DQ92,AVST_DATA3	
DDR4_DIMM_CH0_DQ14	BN22	IO,LVDS3A_3n,DQ92,AVST_DATA4	
DDR4_DIMM_CH0_DQ15	BN23	IO,LVDS3A_3p,DQ92,AVST_DATA5	
DDR4_DIMM_CH0_DQS_N1	BP25	IO,LVDS3A_4n,DQSn92,AVST_DATA6	
DDR4_DIMM_CH0_DQS_P1	BN25	IO,LVDS3A_4p,DQS92,AVST_DATA7	
DDR4_DIMM_CH0_DQ11	BM24	IO,LVDS3A_5n,DQ92,AVST_DATA8	
DDR4_DIMM_CH0_DQ10	BM23	IO,LVDS3A_5p,DQ92,AVST_DATA9	
DDR4_DIMM_CH0_DQ8	BL25	IO,LVDS3A_6n,DQ92,AVST_DATA10	
DDR4_DIMM_CH0_DQ9	BM25	IO,LVDS3A_6p,DQ92,AVST_DATA11	
DDR4_DIMM_CH0_DQ21	BK26	IO,LVDS3A_7n,DQ93,AVST_DATA12	
DDR4_DIMM_CH0_DQ20	BL26	IO,LVDS3A_7p,DQ93,AVST_DATA13	DQSn/P for x4
DDR4_DIMM_CH0_DQS_N11	BH26	IO,LVDS3A_8n,DQ93,AVST_DATA14	
DDR4_DIMM_CH0_DQS_P11	BJ26	IO,LVDS3A_8p,DQ93,AVST_DATA15	
DDR4_DIMM_CH0_DQ23	BK23	IO,LVDS3A_9n,DQ93,AVST_DATA16	
DDR4_DIMM_CH0_DQ22	BJ23	IO,LVDS3A_9p,DQ93,AVST_DATA17	
DDR4_DIMM_CH0_DQS_N2	BL24	IO,PLL_3A_CLKOUT1n,LVDS3A_10n,DQSn93,AVST_DATA18	
DDR4_DIMM_CH0_DQS_P2	BK24	IO,PLL_3A_CLKOUT1p,PLL_3A_CLKOUT1,PLL_3A_FB1,LVDS3A_10p,DQS93,AVST_DATA19	
DDR4_DIMM_CH0_DQ16	BH23	IO,LVDS3A_11n,DQ93	
DDR4_DIMM_CH0_DQ18	BG23	IO,RZQ_3A,LVDS3A_11p,DQ93,AVST_VALID,AVST_VALID	
DDR4_DIMM_CH0_DQ19	BJ25	IO,CLK_3A_1n,LVDS3A_12n,DQ93,AVST_DATA20	
DDR4_DIMM_CH0_DQ17	BJ24	IO,CLK_3A_1p,LVDS3A_12p,DQ93,AVST_DATA21	
DDR4_DIMM_CH0_DQ7	BG24	IO,CLK_3A_0n,LVDS3A_13n,DQ94,AVST_DATA22	
DDR4_DIMM_CH0_DQ5	BH25	IO,CLK_3A_0p,LVDS3A_13p,DQ94,AVST_DATA23	
DDR4_DIMM_CH0_DQS_N9	BF27	IO,LVDS3A_14n,DQ94,AVST_DATA24	DQSn/P for x4
DDR4_DIMM_CH0_DQS_P9	BE27	IO,LVDS3A_14p,DQ94,AVST_DATA25	
DDR4_DIMM_CH0_DQ4	BF25	IO,PLL_3A_CLKOUT0n,LVDS3A_15n,DQ94,AVST_DATA26	
DDR4_DIMM_CH0_DQ6	BG25	IO,PLL_3A_CLKOUT0p,PLL_3A_CLKOUT0,PLL_3A_FB0,LVDS3A_15p,DQ94,AVST_DATA27	
DDR4_DIMM_CH0_DQS_N0	BE26	IO,LVDS3A_16n,DQSn94,AVST_DATA28	
DDR4_DIMM_CH0_DQS_P0	BF26	IO,LVDS3A_16p,DQS94,AVST_DATA29	
DDR4_DIMM_CH0_DQ0	BF24	IO,LVDS3A_17n,DQ94,AVST_DATA30	
DDR4_DIMM_CH0_DQ1	BE24	IO,LVDS3A_17p,DQ94,AVST_DATA31	
DDR4_DIMM_CH0_DQ2	BH27	IO,LVDS3A_18n,DQ94	
DDR4_DIMM_CH0_DQ3	BG27	IO,LVDS3A_18p,DQ94	
DDR4_DIMM_CH0_DQ61	BD23	IO,LVDS3A_19n,DQ95	
DDR4_DIMM_CH0_DQ60	BE23	IO,LVDS3A_19p,DQ95	
DDR4_DIMM_CH0_DQS_N16	BB25	IO,LVDS3A_20n,DQ95	DQSn/P for x4
DDR4_DIMM_CH0_DQS_P16	BC25	IO,LVDS3A_20p,DQ95	
DDR4_DIMM_CH0_DQ63	BC23	IO,LVDS3A_21n,DQ95	
DDR4_DIMM_CH0_DQ62	BB23	IO,LVDS3A_21p,DQ95	
DDR4_DIMM_CH0_DQS_N7	BA24	IO,LVDS3A_22n,DQSn95	
DDR4_DIMM_CH0_DQS_P7	BB24	IO,LVDS3A_22p,DQS95	
DDR4_DIMM_CH0_DQ59	AW24	IO,LVDS3A_23n,DQ95	
DDR4_DIMM_CH0_DQ58	AY24	IO,LVDS3A_23p,DQ95	
DDR4_DIMM_CH0_DQ56	BD25	IO,LVDS3A_24n,DQ95	
DDR4_DIMM_CH0_DQ57	BD26	IO,LVDS3A_24p,DQ95,AVST_CLK	

IO BANK 3A

S10_DX_ND5_F2912D_EXTERNAL

U1-13

1.2V

BD18	DDR4_DIMM_CH0_DQ55	IO,LVDS3C_1N,DQ84	
BE17	DDR4_DIMM_CH0_DQ54	IO,LVDS3C_1P,DQ84	
BC18	DDR4_DIMM_CH0_DQS_N15	IO,LVDS3C_2N,DQ84	DQSn/P for x4
BC17	DDR4_DIMM_CH0_DQS_P15	IO,LVDS3C_2P,DQ84	
BF15	DDR4_DIMM_CH0_DQ53	IO,LVDS3C_3N,DQ84	
BF16	DDR4_DIMM_CH0_DQ52	IO,LVDS3C_3P,DQ84	
BD16	DDR4_DIMM_CH0_DQS_N6	IO,LVDS3C_4N,DQSN84	
BE16	DDR4_DIMM_CH0_DQS_P6	IO,LVDS3C_4P,DQS84	
BG17	DDR4_DIMM_CH0_DQ51	IO,LVDS3C_5N,DQ84	
BF17	DDR4_DIMM_CH0_DQ50	IO,LVDS3C_5P,DQ84	
BC16	DDR4_DIMM_CH0_DQ48	IO,LVDS3C_6N,DQ84	
BD15	DDR4_DIMM_CH0_DQ49	IO,LVDS3C_6P,DQ84	
BF14	DDR4_DIMM_CH0_DQ38	IO,LVDS3C_7N,DQ85	
BG14	DDR4_DIMM_CH0_DQ36	IO,LVDS3C_7P,DQ85	DQSn/P for x4
BH12	DDR4_DIMM_CH0_DQS_N13	IO,LVDS3C_8N,DQ85	
BH13	DDR4_DIMM_CH0_DQS_P13	IO,LVDS3C_8P,DQ85	
BH16	DDR4_DIMM_CH0_DQ37	IO,LVDS3C_9N,DQ85	
BH17	DDR4_DIMM_CH0_DQ39	IO,LVDS3C_9P,DQ85	
BG15	DDR4_DIMM_CH0_DQS_N4	IO,PLL_3C_CLKOUT1N,LVDS3C_10N,DQSN85	
BH15	DDR4_DIMM_CH0_DQS_P4	IO,PLL_3C_CLKOUT1P,PLL_3C_CLKOUT1,PLL_3C_FB1,LVDS3C_10P,DQS85	
BJ15	DDR4_DIMM_CH0_DQ33	IO,LVDS3C_11N,DQ85	
BJ16	DDR4_DIMM_CH0_DQ34	IO,RZQ_3C,LVDS3C_11P,DQ85	
BJ13	DDR4_DIMM_CH0_DQ35	IO,CLK_3C_1N,LVDS3C_12N,DQ85	
BJ14	DDR4_DIMM_CH0_DQ32	IO,CLK_3C_1P,LVDS3C_12P,DQ85	
BL15	DDR4_DIMM_CH0_DQ68	IO,CLK_3C_0N,LVDS3C_13N,DQ86	
BL16	DDR4_DIMM_CH0_DQ70	IO,CLK_3C_0P,LVDS3C_13P,DQ86	
BK13	DDR4_DIMM_CH0_DQS_N17	IO,LVDS3C_14N,DQ86	
BK12	DDR4_DIMM_CH0_DQS_P17	IO,LVDS3C_14P,DQ86	DQSn/P for x4
BK16	DDR4_DIMM_CH0_DQ71	IO,PLL_3C_CLKOUT0N,LVDS3C_15N,DQ86	
BK17	DDR4_DIMM_CH0_DQ69	IO,PLL_3C_CLKOUT0P,PLL_3C_CLKOUT0,PLL_3C_FB0,LVDS3C_15P,DQ86	
BL14	DDR4_DIMM_CH0_DQS_N8	IO,LVDS3C_16N,DQSN86	
BK14	DDR4_DIMM_CH0_DQS_P8	IO,LVDS3C_16P,DQS86	
BL17	DDR4_DIMM_CH0_DQ66	IO,LVDS3C_17N,DQ86	
BM17	DDR4_DIMM_CH0_DQ65	IO,LVDS3C_17P,DQ86	
BM12	DDR4_DIMM_CH0_DQ64	IO,LVDS3C_18N,DQ86	
BL12	DDR4_DIMM_CH0_DQ67	IO,LVDS3C_18P,DQ86	
BN13	DDR4_DIMM_CH0_DQ30	IO,LVDS3C_19N,DQ87	
BN12	DDR4_DIMM_CH0_DQ31	IO,LVDS3C_19P,DQ87	
BM13	DDR4_DIMM_CH0_DQS_N12	IO,LVDS3C_20N,DQ87	DQSn/P for x4
BM14	DDR4_DIMM_CH0_DQS_P12	IO,LVDS3C_20P,DQ87	
BN16	DDR4_DIMM_CH0_DQ29	IO,LVDS3C_21N,DQ87	
BN17	DDR4_DIMM_CH0_DQ28	IO,LVDS3C_21P,DQ87	
BN15	DDR4_DIMM_CH0_DQS_N3	IO,LVDS3C_22N,DQSN87	
BM15	DDR4_DIMM_CH0_DQS_P3	IO,LVDS3C_22P,DQS87	
BP15	DDR4_DIMM_CH0_DQ24	IO,LVDS3C_23N,DQ87	
BP16	DDR4_DIMM_CH0_DQ25	IO,LVDS3C_23P,DQ87	
BP13	DDR4_DIMM_CH0_DQ26	IO,LVDS3C_24N,DQ87	
BP14	DDR4_DIMM_CH0_DQ27	IO,LVDS3C_24P,DQ87	

IO BANK 3C

S10_DX_ND5_F2912D_EXTERNAL

DDR4 DIMM CH0 IF

42	DDR4_DIMM_CH0_C2	
42	DDR4_DIMM_CH0_RESET_N	
42	DDR4_DIMM_CH0_ACT_N	
42	DDR4_DIMM_CH0_PAR	
42	DDR4_DIMM_CH0_ALERT_N	
42	DDR4_DIMM_CH0_CK_P[1:0]	
42	DDR4_DIMM_CH0_CK_N[1:0]	
42	DDR4_DIMM_CH0_CKE[1:0]	
42	DDR4_DIMM_CH0_ODT[1:0]	
42	DDR4_DIMM_CH0_BG[1:0]	
42	DDR4_DIMM_CH0_BA[1:0]	
42	DDR4_DIMM_CH0_CS_N[3:0]	
42	DDR4_DIMM_CH0_DQS_P[17:0]	
42	DDR4_DIMM_CH0_DQS_N[17:0]	
42	DDR4_DIMM_CH0_A[17:0]	
42	DDR4_DIMM_CH0_DQ[71:0]	

CLOCK

R6354 100

CLK_133M_DIMM_1_P	22	
CLK_133M_DIMM_1_N	22	

U1-12

1.2V

DDR4_DIMM_CH0_CK_N1	BA22	IO,LVDS3B_1N,DQ88	
DDR4_DIMM_CH0_CK_P1	BB22	IO,LVDS3B_1P,DQ88	
	BE18	IO,LVDS3B_2N,DQ88	
	BE19	IO,LVDS3B_2P,DQ88	
DDR4_DIMM_CH0_ALERT_N	BC20	IO,LVDS3B_3N,DQ88	
	BC21	IO,LVDS3B_3P,DQ88	
	BA20	IO,LVDS3B_4N,DQSN88	
	BB20	IO,LVDS3B_4P,DQS88	
	BC22	IO,LVDS3B_5N,DQ88	
DDR4_DIMM_CH0_C2	BD21	IO,LVDS3B_5P,DQ88	
DDR4_DIMM_CH0_CS_N3	BD20	IO,LVDS3B_6N,DQ88	
DDR4_DIMM_CH0_CS_N2	BD19	IO,LVDS3B_6P,DQ88	
DDR4_DIMM_CH0_BG0	BE21	IO,LVDS3B_7N,DQ89	
DDR4_DIMM_CH0_BA1	BF21	IO,LVDS3B_7P,DQ89	
DDR4_DIMM_CH0_BA0	BG18	IO,LVDS3B_8N,DQ89	
DDR4_DIMM_CH0_A17	BH18	IO,LVDS3B_8P,DQ89	
DDR4_DIMM_CH0_A16	BF22	IO,LVDS3B_9N,DQ89	
DDR4_DIMM_CH0_A15	BG22	IO,LVDS3B_9P,DQ89	
DDR4_DIMM_CH0_A14	BF20	IO,PLL_3B_CLKOUT1N,LVDS3B_10N,DQSN89	
DDR4_DIMM_CH0_A13	BG20	IO,PLL_3B_CLKOUT1P,PLL_3B_CLKOUT1,PLL_3B_FB1,LVDS3B_10P,DQS89	
DDR4_DIMM_CH0_A12	BH22	IO,LVDS3B_11N,DQ89	
RZQ_3B	BH21	IO,RZQ_3B,LVDS3B_11P,DQ89	
CLK_133M_DIMM_1_N	BG19	IO,CLK_3B_1N,LVDS3B_12N,DQ89	
CLK_133M_DIMM_1_P	BF19	IO,CLK_3B_1P,LVDS3B_12P,DQ89	
DDR4_DIMM_CH0_A11	BJ21	IO,CLK_3B_0N,LVDS3B_13N,DQ90	
DDR4_DIMM_CH0_A10	BK21	IO,CLK_3B_0P,LVDS3B_13P,DQ90	
DDR4_DIMM_CH0_A9	BK18	IO,LVDS3B_14N,DQ90	
DDR4_DIMM_CH0_A8	BJ18	IO,LVDS3B_14P,DQ90	
DDR4_DIMM_CH0_A7	BL19	IO,PLL_3B_CLKOUT0N,LVDS3B_15N,DQ90	
DDR4_DIMM_CH0_A6	BL20	IO,PLL_3B_CLKOUT0P,PLL_3B_CLKOUT0,PLL_3B_FB0,LVDS3B_15P,DQ90	
DDR4_DIMM_CH0_A5	BJ20	IO,LVDS3B_16N,DQSN90	
DDR4_DIMM_CH0_A4	BH20	IO,LVDS3B_16P,DQS90	
DDR4_DIMM_CH0_A3	BK22	IO,LVDS3B_17N,DQ90	
DDR4_DIMM_CH0_A2	BL22	IO,LVDS3B_17P,DQ90	
DDR4_DIMM_CH0_A1	BK19	IO,LVDS3B_18N,DQ90	
DDR4_DIMM_CH0_A0	BJ19	IO,LVDS3B_18P,DQ90	
DDR4_DIMM_CH0_PAR	BL21	IO,LVDS3B_19N,DQ91	
DDR4_DIMM_CH0_CS_N1	BM22	IO,LVDS3B_19P,DQ91	
DDR4_DIMM_CH0_CK_N0	BM19	IO,LVDS3B_20N,DQ91	
DDR4_DIMM_CH0_CK_P0	BM18	IO,LVDS3B_20P,DQ91	
DDR4_DIMM_CH0_CKE1	BN18	IO,LVDS3B_21N,DQ91	
DDR4_DIMM_CH0_CKE0	BP18	IO,LVDS3B_21P,DQ91	
DDR4_DIMM_CH0_ODT1	BM20	IO,LVDS3B_22N,DQSN91	
DDR4_DIMM_CH0_ODT0	BN20	IO,LVDS3B_22P,DQS91	
DDR4_DIMM_CH0_ACT_N	BN21	IO,LVDS3B_23N,DQ91	
DDR4_DIMM_CH0_CS_N0	BP21	IO,LVDS3B_23P,DQ91	
DDR4_DIMM_CH0_RESET_N	BP19	IO,LVDS3B_24N,DQ91	
DDR4_DIMM_CH0_BG1	BP20	IO,LVDS3B_24P,DQ91	

240 1% R28 R0201

IO BANK 3B

S10_DX_ND5_F2912D_EXTERNAL

U1-14

1.2V

BD13	DDR4_DIMM_CH0_DQ46	IO,CLK_3D_0N,LVDS3D_13N,DQ82	
BE13	DDR4_DIMM_CH0_DQ44	IO,CLK_3D_0P,LVDS3D_13P,DQ82	
BG10	DDR4_DIMM_CH0_DQS_N14	IO,LVDS3D_14N,DQ82	DQSn/P for x4
BF10	DDR4_DIMM_CH0_DQS_P14	IO,LVDS3D_14P,DQ82	
BD14	DDR4_DIMM_CH0_DQ45	IO,PLL_3D_CLKOUT0N,LVDS3D_15N,DQ82	
BE14	DDR4_DIMM_CH0_DQ47	IO,PLL_3D_CLKOUT0P,PLL_3D_CLKOUT0,PLL_3D_FB0,LVDS3D_15P,DQ82	
BE12	DDR4_DIMM_CH0_DQS_N5	IO,LVDS3D_16N,DQSN82	
BF12	DDR4_DIMM_CH0_DQS_P5	IO,LVDS3D_16P,DQS82	
BG12	DDR4_DIMM_CH0_DQ40	IO,LVDS3D_17N,DQ82	
BG13	DDR4_DIMM_CH0_DQ42	IO,LVDS3D_17P,DQ82	
BF11	DDR4_DIMM_CH0_DQ41	IO,LVDS3D_18N,DQ82	
BE11	DDR4_DIMM_CH0_DQ43	IO,LVDS3D_18P,DQ82	
BL10		IO,LVDS3D_19N,DQ83	
BM10		IO,LVDS3D_19P,DQ83	
BH10		IO,LVDS3D_20N,DQ83	
BJ10		IO,LVDS3D_20P,DQ83	
BN10		IO,LVDS3D_21N,DQ83	
BP10		IO,LVDS3D_21P,DQ83	
BH11		IO,LVDS3D_22N,DQSN83	
BJ11		IO,LVDS3D_22P,DQS83	
BN11		IO,LVDS3D_23N,DQ83	
BP11		IO,LVDS3D_23P,DQ83	
BK11		IO,LVDS3D_24N,DQ83	
BL11		IO,LVDS3D_24P,DQ83	

IO BANK 3D

S10_DX_ND5_F2912D_EXTERNAL

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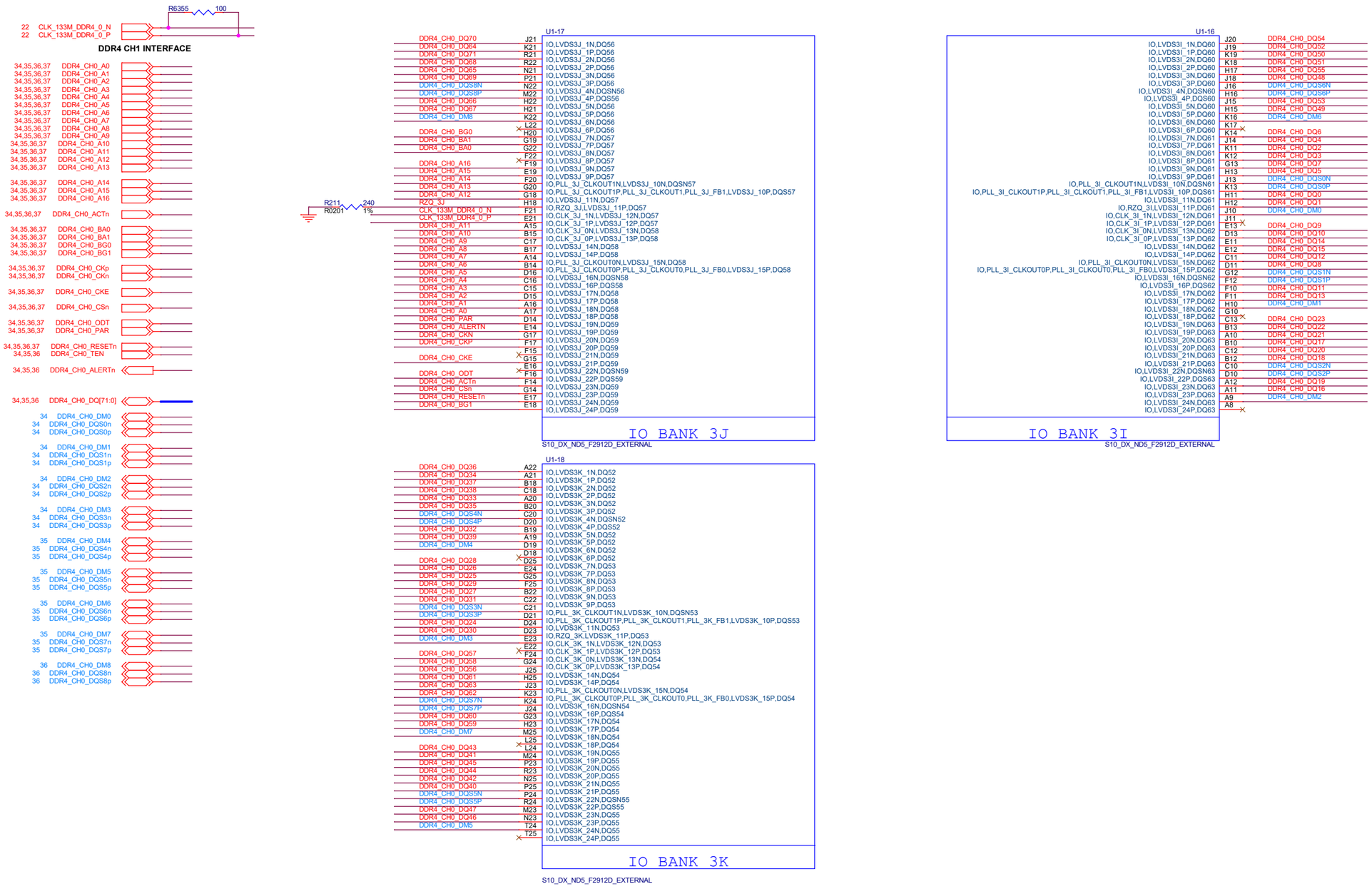
Title: Stratix 10 DX FPGA DEVKIT Board

Size	Document Number	Rev
C	150-0330653-A (K49172-001)	A

Date: Friday, May 24, 2019 Sheet 10 of 69

S10 DX Bank 3I,J,K



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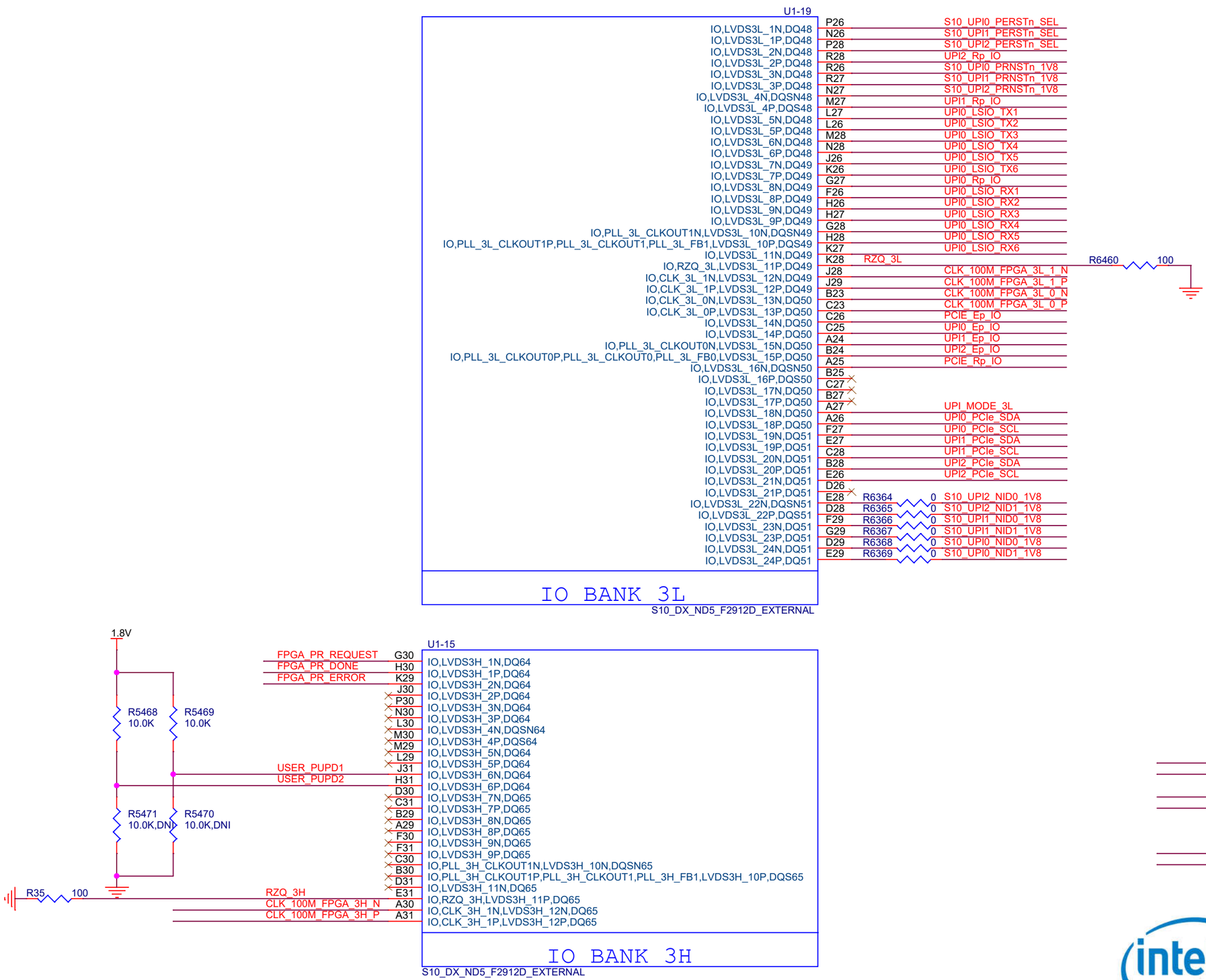
Title: Stratix 10 DX FPGA DEVKIT Board

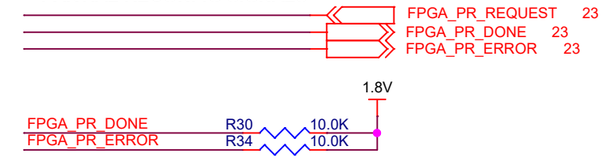
Size	Document Number	Rev
C	150-0330653-A (K49172-001)	A

Date: Friday, May 24, 2019 Sheet 11 of 69

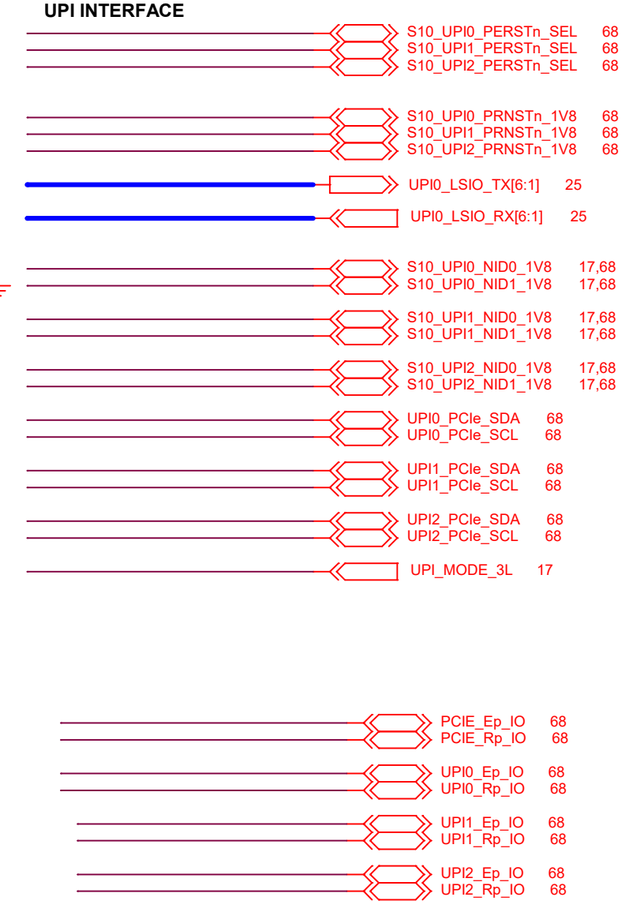
S10 DX Bank 3H, L



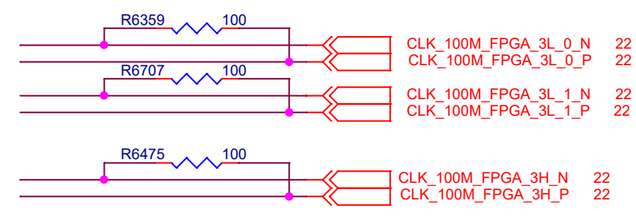
PARTIAL RECONFIG SIGNALS



UPI INTERFACE



CLOCK



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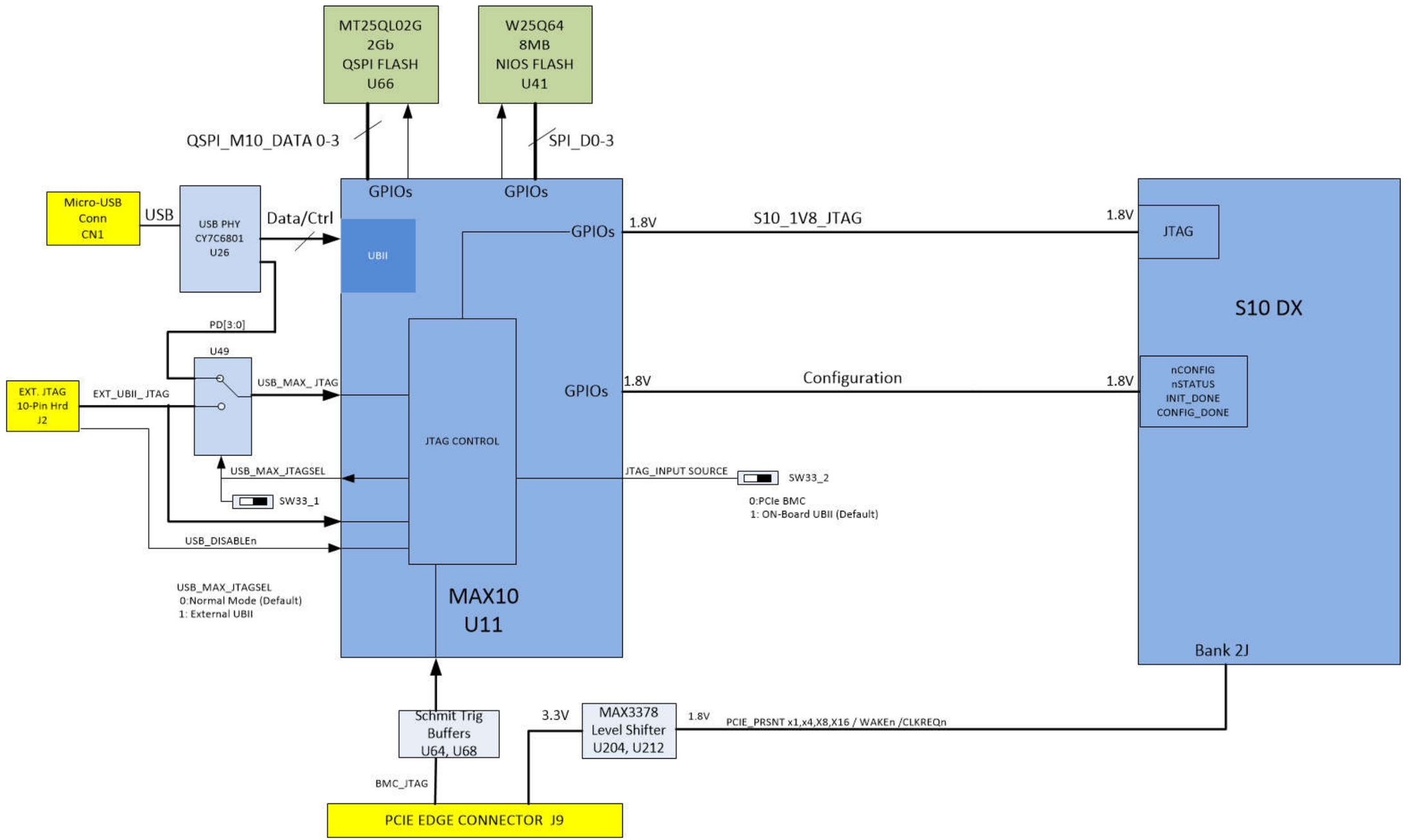
Title: **Stratix 10 DX FPGA DEVKIT Board**

Size	Document Number	Rev
B	150-0330653-A (K49172-001)	A

Date: Friday, May 24, 2019 Sheet 12 of 69

JTAG /Configuration/Flash Interface Diagram



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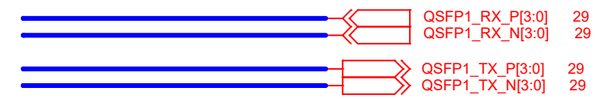
S10 DX Xcvr GXER 9A

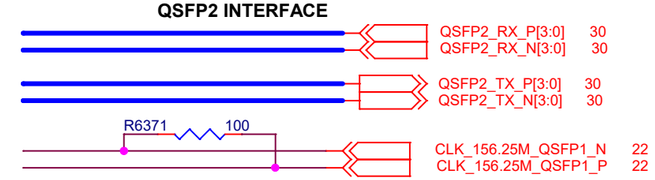
QSFP1

QSFP1 INTERFACE

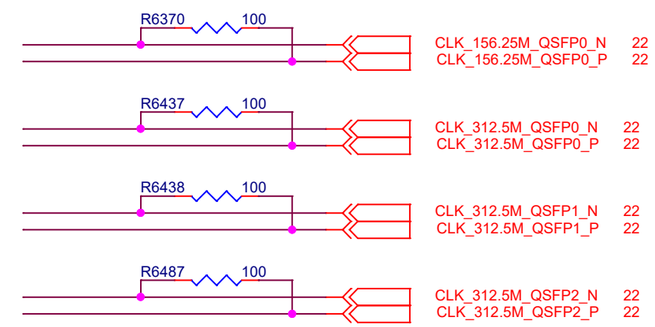


QSFP2

QSFP2 INTERFACE



CLOCK



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Title	Stratix 10 DX FPGA DEVKIT Board	
Size B	Document Number 150-0330653-A (K49172-001)	Rev A
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S10 DX Xcvr GXPL 10A,10B

PCIE x16

U1-21

PCIE_RX_N0	BJ51	GXPL10A_RX_CH0N	GXPL10A_TX_CH0N	BJ47	PCIE_TX_N0
PCIE_RX_P0	BJ52	GXPL10A_RX_CH0P	GXPL10A_TX_CH0P	BJ48	PCIE_TX_P0
PCIE_RX_N1	BH53	GXPL10A_RX_CH1N	GXPL10A_TX_CH1N	BH49	PCIE_TX_N1
PCIE_RX_P1	BH54	GXPL10A_RX_CH1P	GXPL10A_TX_CH1P	BH50	PCIE_TX_P1
PCIE_RX_N2	BG51	GXPL10A_RX_CH2N	GXPL10A_TX_CH2N	BG47	PCIE_TX_N2
PCIE_RX_P2	BG52	GXPL10A_RX_CH2P	GXPL10A_TX_CH2P	BG48	PCIE_TX_P2
PCIE_RX_N3	BF53	GXPL10A_RX_CH3N	GXPL10A_TX_CH3N	BF49	PCIE_TX_N3
PCIE_RX_P3	BF54	GXPL10A_RX_CH3P	GXPL10A_TX_CH3P	BF50	PCIE_TX_P3
PCIE_RX_N4	BE51	GXPL10A_RX_CH4N	GXPL10A_TX_CH4N	BE47	PCIE_TX_N4
PCIE_RX_P4	BE52	GXPL10A_RX_CH4P	GXPL10A_TX_CH4P	BE48	PCIE_TX_P4
PCIE_RX_N5	BD53	GXPL10A_RX_CH5N	GXPL10A_TX_CH5N	BD49	PCIE_TX_N5
PCIE_RX_P5	BD54	GXPL10A_RX_CH5P	GXPL10A_TX_CH5P	BD50	PCIE_TX_P5
PCIE_RX_N6	BC51	GXPL10A_RX_CH6N	GXPL10A_TX_CH6N	BC47	PCIE_TX_N6
PCIE_RX_P6	BC52	GXPL10A_RX_CH6P	GXPL10A_TX_CH6P	BC48	PCIE_TX_P6
PCIE_RX_N7	BB53	GXPL10A_RX_CH7N	GXPL10A_TX_CH7N	BB49	PCIE_TX_N7
PCIE_RX_P7	BB54	GXPL10A_RX_CH7P	GXPL10A_TX_CH7P	BB50	PCIE_TX_P7
PCIE_RX_N8	BA51	GXPL10A_RX_CH8N	GXPL10A_TX_CH8N	BA47	PCIE_TX_N8
PCIE_RX_P8	BA52	GXPL10A_RX_CH8P	GXPL10A_TX_CH8P	BA48	PCIE_TX_P8
PCIE_RX_N9	AY53	GXPL10A_RX_CH9N	GXPL10A_TX_CH9N	AY49	PCIE_TX_N9
PCIE_RX_P9	AY54	GXPL10A_RX_CH9P	GXPL10A_TX_CH9P	AY50	PCIE_TX_P9
PCIE_RX_N10	AW51	GXPL10A_RX_CH10N	GXPL10A_TX_CH10N	AW47	PCIE_TX_N10
PCIE_RX_P10	AW52	GXPL10A_RX_CH10P	GXPL10A_TX_CH10P	AW48	PCIE_TX_P10
PCIE_RX_N11	AV53	GXPL10A_RX_CH11N	GXPL10A_TX_CH11N	AV49	PCIE_TX_N11
PCIE_RX_P11	AV54	GXPL10A_RX_CH11P	GXPL10A_TX_CH11P	AV50	PCIE_TX_P11
PCIE_RX_N12	AU51	GXPL10A_RX_CH12N	GXPL10A_TX_CH12N	AU47	PCIE_TX_N12
PCIE_RX_P12	AU52	GXPL10A_RX_CH12P	GXPL10A_TX_CH12P	AU48	PCIE_TX_P12
PCIE_RX_N13	AT53	GXPL10A_RX_CH13N	GXPL10A_TX_CH13N	AT49	PCIE_TX_N13
PCIE_RX_P13	AT54	GXPL10A_RX_CH13P	GXPL10A_TX_CH13P	AT50	PCIE_TX_P13
PCIE_RX_N14	AR51	GXPL10A_RX_CH14N	GXPL10A_TX_CH14N	AR47	PCIE_TX_N14
PCIE_RX_P14	AR52	GXPL10A_RX_CH14P	GXPL10A_TX_CH14P	AR48	PCIE_TX_P14
PCIE_RX_N15	AP53	GXPL10A_RX_CH15N	GXPL10A_TX_CH15N	AP49	PCIE_TX_N15
PCIE_RX_P15	AP54	GXPL10A_RX_CH15P	GXPL10A_TX_CH15P	AP50	PCIE_TX_P15

RESREF = 169 Ohm for 85 Ohm UPI/PCIe or 200 Ohm for 100 Ohm UPI/PCIe

R6464 169,0.1% AN41 — U10_P_IO_RESREF_0

CLK_100M_PCIE_0_N	AT44	REFCLK_GXPL10A_CH0N	
CLK_100M_PCIE_0_P	AT45	REFCLK_GXPL10A_CH0P	
CLK_100M_PCIE_1_N	AP44	REFCLK_GXPL10A_CH2N	
CLK_100M_PCIE_1_P	AP45	REFCLK_GXPL10A_CH2P	

XCVR BANK 10A

S10_DX_ND5_F2912D_EXTERNAL

PCIE x16

PCIE x16 INTERFACE

PCIE_TX_P[15:0]	21	
PCIE_TX_N[15:0]	21	
PCIE_RX_P[15:0]	21	
PCIE_RX_N[15:0]	21	

UPI0 INTERFACE

UPI0_FPGA_CPU_DN[19:0]	25
UPI0_FPGA_CPU_DP[19:0]	25
UPI0_CPU_FPGA_DN[19:0]	25
UPI0_CPU_FPGA_DP[19:0]	25

CLOCKs

R6417	100	CLK_100M_UPI0_0_P	22
		CLK_100M_UPI0_0_N	22
R6418	100	CLK_100M_UPI0_1_P	22
		CLK_100M_UPI0_1_N	22
R6423	100	CLK_100M_PCIE_0_P	22
		CLK_100M_PCIE_0_N	22
R6424	100	CLK_100M_PCIE_1_P	22
		CLK_100M_PCIE_1_N	22

U1-22

UPI0_CPU_FPGA_DN0	AN51	GXPL10B_RX_CH0N	GXPL10B_TX_CH0N	AN47	UPI0_FPGA_CPU_DN0
UPI0_CPU_FPGA_DP0	AN52	GXPL10B_RX_CH0P	GXPL10B_TX_CH0P	AN48	UPI0_FPGA_CPU_DP0
UPI0_CPU_FPGA_DN1	AM53	GXPL10B_RX_CH1N	GXPL10B_TX_CH1N	AM49	UPI0_FPGA_CPU_DN1
UPI0_CPU_FPGA_DP1	AM54	GXPL10B_RX_CH1P	GXPL10B_TX_CH1P	AM50	UPI0_FPGA_CPU_DP1
UPI0_CPU_FPGA_DN2	AL51	GXPL10B_RX_CH2N	GXPL10B_TX_CH2N	AL47	UPI0_FPGA_CPU_DN2
UPI0_CPU_FPGA_DP2	AL52	GXPL10B_RX_CH2P	GXPL10B_TX_CH2P	AL48	UPI0_FPGA_CPU_DP2
UPI0_CPU_FPGA_DN3	AK53	GXPL10B_RX_CH3N	GXPL10B_TX_CH3N	AK49	UPI0_FPGA_CPU_DN3
UPI0_CPU_FPGA_DP3	AK54	GXPL10B_RX_CH3P	GXPL10B_TX_CH3P	AK50	UPI0_FPGA_CPU_DP3
UPI0_CPU_FPGA_DN4	AJ51	GXPL10B_RX_CH4N	GXPL10B_TX_CH4N	AJ47	UPI0_FPGA_CPU_DN4
UPI0_CPU_FPGA_DP4	AJ52	GXPL10B_RX_CH4P	GXPL10B_TX_CH4P	AJ48	UPI0_FPGA_CPU_DP4
UPI0_CPU_FPGA_DN5	AH53	GXPL10B_RX_CH5N	GXPL10B_TX_CH5N	AH49	UPI0_FPGA_CPU_DN5
UPI0_CPU_FPGA_DP5	AH54	GXPL10B_RX_CH5P	GXPL10B_TX_CH5P	AH50	UPI0_FPGA_CPU_DP5
UPI0_CPU_FPGA_DN6	AG51	GXPL10B_RX_CH6N	GXPL10B_TX_CH6N	AG47	UPI0_FPGA_CPU_DN6
UPI0_CPU_FPGA_DP6	AG52	GXPL10B_RX_CH6P	GXPL10B_TX_CH6P	AG48	UPI0_FPGA_CPU_DP6
UPI0_CPU_FPGA_DN7	AF53	GXPL10B_RX_CH7N	GXPL10B_TX_CH7N	AF49	UPI0_FPGA_CPU_DN7
UPI0_CPU_FPGA_DP7	AF54	GXPL10B_RX_CH7P	GXPL10B_TX_CH7P	AF50	UPI0_FPGA_CPU_DP7
UPI0_CPU_FPGA_DN8	AE51	GXPL10B_RX_CH8N	GXPL10B_TX_CH8N	AE47	UPI0_FPGA_CPU_DN8
UPI0_CPU_FPGA_DP8	AE52	GXPL10B_RX_CH8P	GXPL10B_TX_CH8P	AE48	UPI0_FPGA_CPU_DP8
UPI0_CPU_FPGA_DN9	AD53	GXPL10B_RX_CH9N	GXPL10B_TX_CH9N	AD49	UPI0_FPGA_CPU_DN9
UPI0_CPU_FPGA_DP9	AD54	GXPL10B_RX_CH9P	GXPL10B_TX_CH9P	AD50	UPI0_FPGA_CPU_DP9
UPI0_CPU_FPGA_DN10	AC51	GXPL10B_RX_CH10N	GXPL10B_TX_CH10N	AC47	UPI0_FPGA_CPU_DN10
UPI0_CPU_FPGA_DP10	AC52	GXPL10B_RX_CH10P	GXPL10B_TX_CH10P	AC48	UPI0_FPGA_CPU_DP10
UPI0_CPU_FPGA_DN11	AB53	GXPL10B_RX_CH11N	GXPL10B_TX_CH11N	AB49	UPI0_FPGA_CPU_DN11
UPI0_CPU_FPGA_DP11	AB54	GXPL10B_RX_CH11P	GXPL10B_TX_CH11P	AB50	UPI0_FPGA_CPU_DP11
UPI0_CPU_FPGA_DN12	AA51	GXPL10B_RX_CH12N	GXPL10B_TX_CH12N	AA47	UPI0_FPGA_CPU_DN12
UPI0_CPU_FPGA_DP12	AA52	GXPL10B_RX_CH12P	GXPL10B_TX_CH12P	AA48	UPI0_FPGA_CPU_DP12
UPI0_CPU_FPGA_DN13	Y53	GXPL10B_RX_CH13N	GXPL10B_TX_CH13N	Y49	UPI0_FPGA_CPU_DN13
UPI0_CPU_FPGA_DP13	Y54	GXPL10B_RX_CH13P	GXPL10B_TX_CH13P	Y50	UPI0_FPGA_CPU_DP13
UPI0_CPU_FPGA_DN14	W51	GXPL10B_RX_CH14N	GXPL10B_TX_CH14N	W47	UPI0_FPGA_CPU_DN14
UPI0_CPU_FPGA_DP14	W52	GXPL10B_RX_CH14P	GXPL10B_TX_CH14P	W48	UPI0_FPGA_CPU_DP14
UPI0_CPU_FPGA_DN15	V53	GXPL10B_RX_CH15N	GXPL10B_TX_CH15N	V49	UPI0_FPGA_CPU_DN15
UPI0_CPU_FPGA_DP15	V54	GXPL10B_RX_CH15P	GXPL10B_TX_CH15P	V50	UPI0_FPGA_CPU_DP15
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UPI0_CPU_FPGA_DP16	U52	GXPL10B_RX_CH16P	GXPL10B_TX_CH16P	U48	UPI0_FPGA_CPU_DP16
UPI0_CPU_FPGA_DN17	T53	GXPL10B_RX_CH17N	GXPL10B_TX_CH17N	T49	UPI0_FPGA_CPU_DN17
UPI0_CPU_FPGA_DP17	T54	GXPL10B_RX_CH17P	GXPL10B_TX_CH17P	T50	UPI0_FPGA_CPU_DP17
UPI0_CPU_FPGA_DN18	R51	GXPL10B_RX_CH18N	GXPL10B_TX_CH18N	R47	UPI0_FPGA_CPU_DN18
UPI0_CPU_FPGA_DP18	R52	GXPL10B_RX_CH18P	GXPL10B_TX_CH18P	R48	UPI0_FPGA_CPU_DP18
UPI0_CPU_FPGA_DN19	P53	GXPL10B_RX_CH19N	GXPL10B_TX_CH19N	P49	UPI0_FPGA_CPU_DN19
UPI0_CPU_FPGA_DP19	P54	GXPL10B_RX_CH19P	GXPL10B_TX_CH19P	P50	UPI0_FPGA_CPU_DP19

RESREF = 169 Ohm for 85 Ohm UPI/PCIe or 200 Ohm for 100 Ohm UPI/PCIe

R6465 169,0.1% AC41 — U11_P_IO_RESREF_0

CLK_100M_UPI0_0_N	AJ44	REFCLK_GXPL10B_CH0N	
CLK_100M_UPI0_0_P	AJ45	REFCLK_GXPL10B_CH0P	
CLK_100M_UPI0_1_N	AG44	REFCLK_GXPL10B_CH2N	
CLK_100M_UPI0_1_P	AG45	REFCLK_GXPL10B_CH2P	

XCVR BANK 10B

S10_DX_ND5_F2912D_EXTERNAL

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S10 DX Xcvr GXPR 11B, 11C

UPI_1 CPU->FPGA

UPI_1 FPGA->CPU

U1-23

UPI1_CPU_FPGA_DN0	BB2	GXPR11B_RX_CH0N	GXPR11B_TX_CH0N	BA8	UPI1_FPGA_CPU_DN0
UPI1_CPU_FPGA_DP0	BB1	GXPR11B_RX_CH0P	GXPR11B_TX_CH0P	BA7	UPI1_FPGA_CPU_DP0
UPI1_CPU_FPGA_DN1	BA4	GXPR11B_RX_CH1N	GXPR11B_TX_CH1N	AY6	UPI1_FPGA_CPU_DN1
UPI1_CPU_FPGA_DP1	BA3	GXPR11B_RX_CH1P	GXPR11B_TX_CH1P	AY5	UPI1_FPGA_CPU_DP1
UPI1_CPU_FPGA_DN2	AY2	GXPR11B_RX_CH2N	GXPR11B_TX_CH2N	AW8	UPI1_FPGA_CPU_DN2
UPI1_CPU_FPGA_DP2	AY1	GXPR11B_RX_CH2P	GXPR11B_TX_CH2P	AW7	UPI1_FPGA_CPU_DP2
UPI1_CPU_FPGA_DN3	AW4	GXPR11B_RX_CH3N	GXPR11B_TX_CH3N	AV6	UPI1_FPGA_CPU_DN3
UPI1_CPU_FPGA_DP3	AW3	GXPR11B_RX_CH3P	GXPR11B_TX_CH3P	AV5	UPI1_FPGA_CPU_DP3
UPI1_CPU_FPGA_DN4	AV2	GXPR11B_RX_CH4N	GXPR11B_TX_CH4N	AU8	UPI1_FPGA_CPU_DN4
UPI1_CPU_FPGA_DP4	AV1	GXPR11B_RX_CH4P	GXPR11B_TX_CH4P	AU7	UPI1_FPGA_CPU_DP4
UPI1_CPU_FPGA_DN5	AU4	GXPR11B_RX_CH5N	GXPR11B_TX_CH5N	AT6	UPI1_FPGA_CPU_DN5
UPI1_CPU_FPGA_DP5	AU3	GXPR11B_RX_CH5P	GXPR11B_TX_CH5P	AT5	UPI1_FPGA_CPU_DP5
UPI1_CPU_FPGA_DN6	AT2	GXPR11B_RX_CH6N	GXPR11B_TX_CH6N	AR8	UPI1_FPGA_CPU_DN6
UPI1_CPU_FPGA_DP6	AT1	GXPR11B_RX_CH6P	GXPR11B_TX_CH6P	AR7	UPI1_FPGA_CPU_DP6
UPI1_CPU_FPGA_DN7	AR4	GXPR11B_RX_CH7N	GXPR11B_TX_CH7N	AP6	UPI1_FPGA_CPU_DN7
UPI1_CPU_FPGA_DP7	AR3	GXPR11B_RX_CH7P	GXPR11B_TX_CH7P	AP5	UPI1_FPGA_CPU_DP7
UPI1_CPU_FPGA_DN8	AP2	GXPR11B_RX_CH8N	GXPR11B_TX_CH8N	AN8	UPI1_FPGA_CPU_DN8
UPI1_CPU_FPGA_DP8	AP1	GXPR11B_RX_CH8P	GXPR11B_TX_CH8P	AN7	UPI1_FPGA_CPU_DP8
UPI1_CPU_FPGA_DN9	AN4	GXPR11B_RX_CH9N	GXPR11B_TX_CH9N	AM6	UPI1_FPGA_CPU_DN9
UPI1_CPU_FPGA_DP9	AN3	GXPR11B_RX_CH9P	GXPR11B_TX_CH9P	AM5	UPI1_FPGA_CPU_DP9
UPI1_CPU_FPGA_DN10	AM2	GXPR11B_RX_CH10N	GXPR11B_TX_CH10N	AL8	UPI1_FPGA_CPU_DN10
UPI1_CPU_FPGA_DP10	AM1	GXPR11B_RX_CH10P	GXPR11B_TX_CH10P	AL7	UPI1_FPGA_CPU_DP10
UPI1_CPU_FPGA_DN11	AL4	GXPR11B_RX_CH11N	GXPR11B_TX_CH11N	AK6	UPI1_FPGA_CPU_DN11
UPI1_CPU_FPGA_DP11	AL3	GXPR11B_RX_CH11P	GXPR11B_TX_CH11P	AK5	UPI1_FPGA_CPU_DP11
UPI1_CPU_FPGA_DN12	AK2	GXPR11B_RX_CH12N	GXPR11B_TX_CH12N	AJ8	UPI1_FPGA_CPU_DN12
UPI1_CPU_FPGA_DP12	AK1	GXPR11B_RX_CH12P	GXPR11B_TX_CH12P	AJ7	UPI1_FPGA_CPU_DP12
UPI1_CPU_FPGA_DN13	AJ4	GXPR11B_RX_CH13N	GXPR11B_TX_CH13N	AH6	UPI1_FPGA_CPU_DN13
UPI1_CPU_FPGA_DP13	AJ3	GXPR11B_RX_CH13P	GXPR11B_TX_CH13P	AH5	UPI1_FPGA_CPU_DP13
UPI1_CPU_FPGA_DN14	AH2	GXPR11B_RX_CH14N	GXPR11B_TX_CH14N	AG8	UPI1_FPGA_CPU_DN14
UPI1_CPU_FPGA_DP14	AH1	GXPR11B_RX_CH14P	GXPR11B_TX_CH14P	AG7	UPI1_FPGA_CPU_DP14
UPI1_CPU_FPGA_DN15	AG4	GXPR11B_RX_CH15N	GXPR11B_TX_CH15N	AF6	UPI1_FPGA_CPU_DN15
UPI1_CPU_FPGA_DP15	AG3	GXPR11B_RX_CH15P	GXPR11B_TX_CH15P	AF5	UPI1_FPGA_CPU_DP15
UPI1_CPU_FPGA_DN16	AF2	GXPR11B_RX_CH16N	GXPR11B_TX_CH16N	AE8	UPI1_FPGA_CPU_DN16
UPI1_CPU_FPGA_DP16	AF1	GXPR11B_RX_CH16P	GXPR11B_TX_CH16P	AE7	UPI1_FPGA_CPU_DP16
UPI1_CPU_FPGA_DN17	AE4	GXPR11B_RX_CH17N	GXPR11B_TX_CH17N	AD6	UPI1_FPGA_CPU_DN17
UPI1_CPU_FPGA_DP17	AE3	GXPR11B_RX_CH17P	GXPR11B_TX_CH17P	AD5	UPI1_FPGA_CPU_DP17
UPI1_CPU_FPGA_DN18	AD2	GXPR11B_RX_CH18N	GXPR11B_TX_CH18N	AC8	UPI1_FPGA_CPU_DN18
UPI1_CPU_FPGA_DP18	AD1	GXPR11B_RX_CH18P	GXPR11B_TX_CH18P	AC7	UPI1_FPGA_CPU_DP18
UPI1_CPU_FPGA_DN19	AC4	GXPR11B_RX_CH19N	GXPR11B_TX_CH19N	AB6	UPI1_FPGA_CPU_DN19
UPI1_CPU_FPGA_DP19	AC3	GXPR11B_RX_CH19P	GXPR11B_TX_CH19P	AB5	UPI1_FPGA_CPU_DP19

RESREF = 169 Ohm for 85 Ohm UPI/PCIe or 200 Ohm for 100 Ohm UPI/PCIe

R6462 169.0.1%

	AL14	U21_P_IO_RESREF_0
CLK_100M_UPI1_0_N	AH11	REFCLK_GXPR11B_CH0N
CLK_100M_UPI1_0_P	AH10	REFCLK_GXPR11B_CH0P
CLK_100M_UPI1_1_N	AF11	REFCLK_GXPR11B_CH2N
CLK_100M_UPI1_1_P	AF10	REFCLK_GXPR11B_CH2P

XCVR BANK 11B

S10_DX_ND5_F2912D_EXTERNAL

UPI_2 CPU->FPGA

UPI_2 FPGA->CPU

U1-24

UPI2_CPU_FPGA_DN0	AB2	GXPR11C_RX_CH0N	GXPR11C_TX_CH0N	AA8	UPI2_FPGA_CPU_DN0
UPI2_CPU_FPGA_DP0	AB1	GXPR11C_RX_CH0P	GXPR11C_TX_CH0P	AA7	UPI2_FPGA_CPU_DP0
UPI2_CPU_FPGA_DN1	AA4	GXPR11C_RX_CH1N	GXPR11C_TX_CH1N	Y6	UPI2_FPGA_CPU_DN1
UPI2_CPU_FPGA_DP1	AA3	GXPR11C_RX_CH1P	GXPR11C_TX_CH1P	Y5	UPI2_FPGA_CPU_DP1
UPI2_CPU_FPGA_DN2	Y2	GXPR11C_RX_CH2N	GXPR11C_TX_CH2N	W8	UPI2_FPGA_CPU_DN2
UPI2_CPU_FPGA_DP2	Y1	GXPR11C_RX_CH2P	GXPR11C_TX_CH2P	W7	UPI2_FPGA_CPU_DP2
UPI2_CPU_FPGA_DN3	W4	GXPR11C_RX_CH3N	GXPR11C_TX_CH3N	V6	UPI2_FPGA_CPU_DN3
UPI2_CPU_FPGA_DP3	W3	GXPR11C_RX_CH3P	GXPR11C_TX_CH3P	V5	UPI2_FPGA_CPU_DP3
UPI2_CPU_FPGA_DN4	V2	GXPR11C_RX_CH4N	GXPR11C_TX_CH4N	U8	UPI2_FPGA_CPU_DN4
UPI2_CPU_FPGA_DP4	V1	GXPR11C_RX_CH4P	GXPR11C_TX_CH4P	U7	UPI2_FPGA_CPU_DP4
UPI2_CPU_FPGA_DN5	U4	GXPR11C_RX_CH5N	GXPR11C_TX_CH5N	T6	UPI2_FPGA_CPU_DN5
UPI2_CPU_FPGA_DP5	U3	GXPR11C_RX_CH5P	GXPR11C_TX_CH5P	T5	UPI2_FPGA_CPU_DP5
UPI2_CPU_FPGA_DN6	T2	GXPR11C_RX_CH6N	GXPR11C_TX_CH6N	R8	UPI2_FPGA_CPU_DN6
UPI2_CPU_FPGA_DP6	T1	GXPR11C_RX_CH6P	GXPR11C_TX_CH6P	R7	UPI2_FPGA_CPU_DP6
UPI2_CPU_FPGA_DN7	R4	GXPR11C_RX_CH7N	GXPR11C_TX_CH7N	P6	UPI2_FPGA_CPU_DN7
UPI2_CPU_FPGA_DP7	R3	GXPR11C_RX_CH7P	GXPR11C_TX_CH7P	P5	UPI2_FPGA_CPU_DP7
UPI2_CPU_FPGA_DN8	P2	GXPR11C_RX_CH8N	GXPR11C_TX_CH8N	N8	UPI2_FPGA_CPU_DN8
UPI2_CPU_FPGA_DP8	P1	GXPR11C_RX_CH8P	GXPR11C_TX_CH8P	N7	UPI2_FPGA_CPU_DP8
UPI2_CPU_FPGA_DN9	N4	GXPR11C_RX_CH9N	GXPR11C_TX_CH9N	M6	UPI2_FPGA_CPU_DN9
UPI2_CPU_FPGA_DP9	N3	GXPR11C_RX_CH9P	GXPR11C_TX_CH9P	M5	UPI2_FPGA_CPU_DP9
UPI2_CPU_FPGA_DN10	M2	GXPR11C_RX_CH10N	GXPR11C_TX_CH10N	L8	UPI2_FPGA_CPU_DN10
UPI2_CPU_FPGA_DP10	M1	GXPR11C_RX_CH10P	GXPR11C_TX_CH10P	L7	UPI2_FPGA_CPU_DP10
UPI2_CPU_FPGA_DN11	L4	GXPR11C_RX_CH11N	GXPR11C_TX_CH11N	K6	UPI2_FPGA_CPU_DN11
UPI2_CPU_FPGA_DP11	L3	GXPR11C_RX_CH11P	GXPR11C_TX_CH11P	K5	UPI2_FPGA_CPU_DP11
UPI2_CPU_FPGA_DN12	K2	GXPR11C_RX_CH12N	GXPR11C_TX_CH12N	J8	UPI2_FPGA_CPU_DN12
UPI2_CPU_FPGA_DP12	K1	GXPR11C_RX_CH12P	GXPR11C_TX_CH12P	J7	UPI2_FPGA_CPU_DP12
UPI2_CPU_FPGA_DN13	J4	GXPR11C_RX_CH13N	GXPR11C_TX_CH13N	H6	UPI2_FPGA_CPU_DN13
UPI2_CPU_FPGA_DP13	J3	GXPR11C_RX_CH13P	GXPR11C_TX_CH13P	H5	UPI2_FPGA_CPU_DP13
UPI2_CPU_FPGA_DN14	H2	GXPR11C_RX_CH14N	GXPR11C_TX_CH14N	G8	UPI2_FPGA_CPU_DN14
UPI2_CPU_FPGA_DP14	H1	GXPR11C_RX_CH14P	GXPR11C_TX_CH14P	G7	UPI2_FPGA_CPU_DP14
UPI2_CPU_FPGA_DN15	G4	GXPR11C_RX_CH15N	GXPR11C_TX_CH15N	F6	UPI2_FPGA_CPU_DN15
UPI2_CPU_FPGA_DP15	G3	GXPR11C_RX_CH15P	GXPR11C_TX_CH15P	F5	UPI2_FPGA_CPU_DP15
UPI2_CPU_FPGA_DN16	F2	GXPR11C_RX_CH16N	GXPR11C_TX_CH16N	E8	UPI2_FPGA_CPU_DN16
UPI2_CPU_FPGA_DP16	F1	GXPR11C_RX_CH16P	GXPR11C_TX_CH16P	E7	UPI2_FPGA_CPU_DP16
UPI2_CPU_FPGA_DN17	E4	GXPR11C_RX_CH17N	GXPR11C_TX_CH17N	D6	UPI2_FPGA_CPU_DN17
UPI2_CPU_FPGA_DP17	E3	GXPR11C_RX_CH17P	GXPR11C_TX_CH17P	D5	UPI2_FPGA_CPU_DP17
UPI2_CPU_FPGA_DN18	D2	GXPR11C_RX_CH18N	GXPR11C_TX_CH18N	C8	UPI2_FPGA_CPU_DN18
UPI2_CPU_FPGA_DP18	D1	GXPR11C_RX_CH18P	GXPR11C_TX_CH18P	C7	UPI2_FPGA_CPU_DP18
UPI2_CPU_FPGA_DN19	C4	GXPR11C_RX_CH19N	GXPR11C_TX_CH19N	B6	UPI2_FPGA_CPU_DN19
UPI2_CPU_FPGA_DP19	C3	GXPR11C_RX_CH19P	GXPR11C_TX_CH19P	B5	UPI2_FPGA_CPU_DP19

RESREF = 169 Ohm for 85 Ohm UPI/PCIe or 200 Ohm for 100 Ohm UPI/PCIe

R6463 169.0.1%

	AB12	U22_P_IO_RESREF_0
CLK_100M_UPI2_0_N	V11	REFCLK_GXPR11C_CH0N
CLK_100M_UPI2_0_P	V10	REFCLK_GXPR11C_CH0P
CLK_100M_UPI2_1_N	T11	REFCLK_GXPR11C_CH2N
CLK_100M_UPI2_1_P	T10	REFCLK_GXPR11C_CH2P

XCVR BANK 11C

S10_DX_ND5_F2912D_EXTERNAL

UPI2 INTERFACE

UPI2_FPGA_CPU_DN[19:0]	27	
UPI2_FPGA_CPU_DP[19:0]	27	
UPI2_CPU_FPGA_DN[19:0]	27	
UPI2_CPU_FPGA_DP[19:0]	27	

UPI1 INTERFACE

UPI1_FPGA_CPU_DN[19:0]	26	
UPI1_FPGA_CPU_DP[19:0]	26	
UPI1_CPU_FPGA_DN[19:0]	26	
UPI1_CPU_FPGA_DP[19:0]	26	

CLOCK

CLK_100M_UPI1_0_P	22	R6419 100	
CLK_100M_UPI1_0_N	22		
CLK_100M_UPI1_1_P	22	R6420 100	
CLK_100M_UPI1_1_N	22		
CLK_100M_UPI2_0_P	22	R6421 100	
CLK_100M_UPI2_0_N	22		
CLK_100M_UPI2_1_P	22	R6422 100	
CLK_100M_UPI2_1_N	22		

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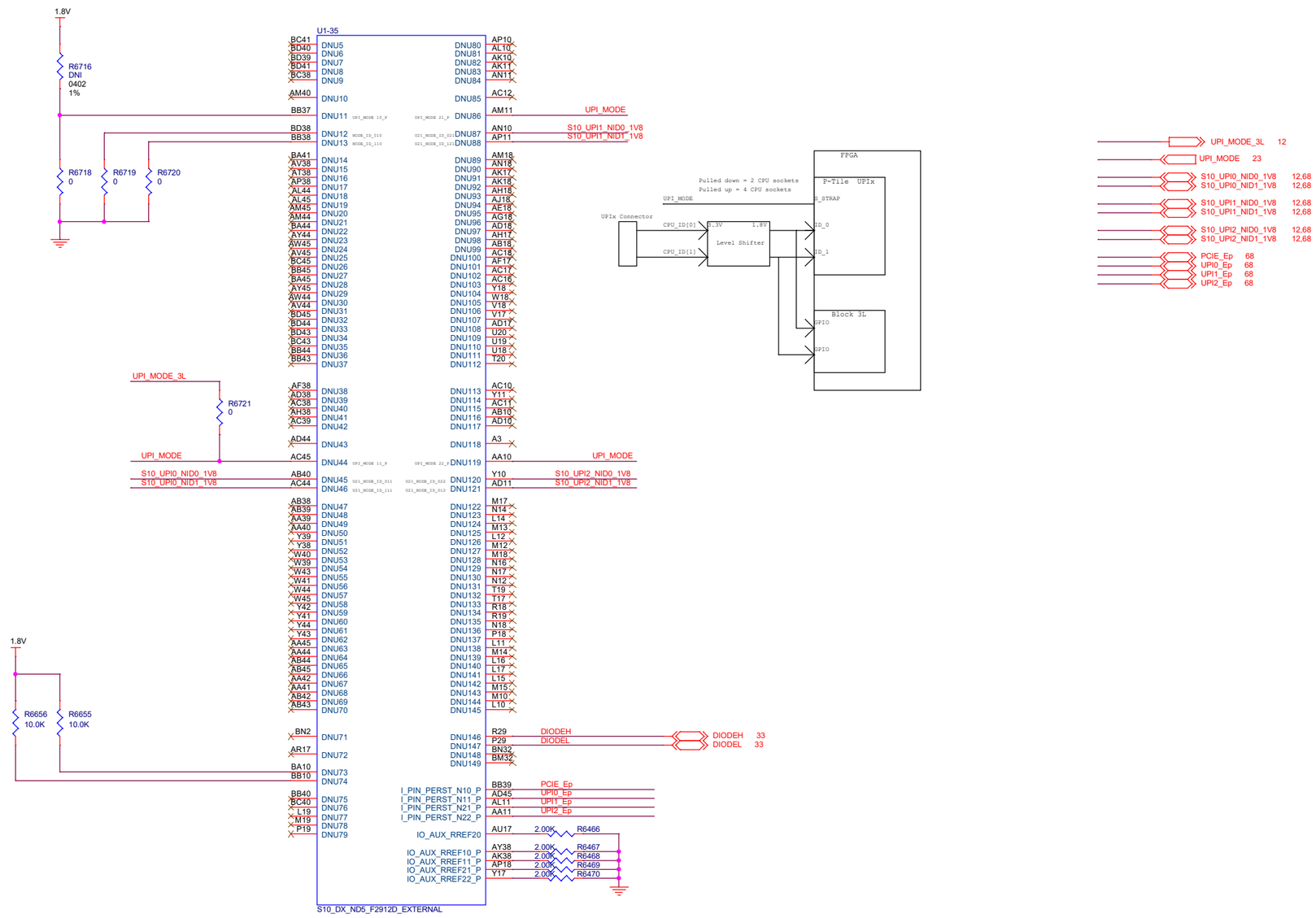
S10 DX Bank WHR



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Title: **Stratix 10 DX FPGA DEVKIT Board**

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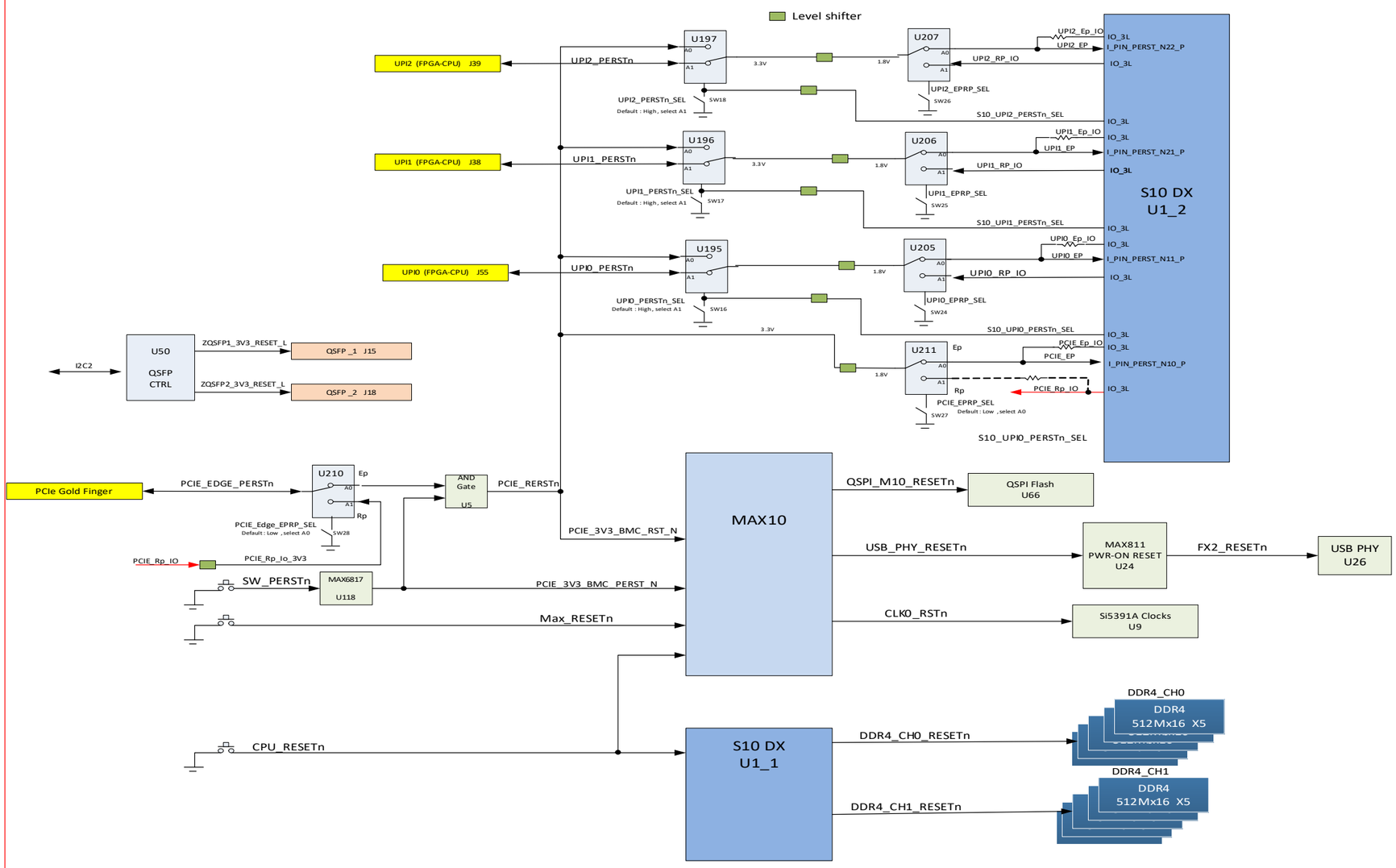
Reset Tree



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Title	Stratix 10 DX FPGA DEVKIT Board	
Size B	Document Number 150-0330653-A (K49172-001)	Rev A
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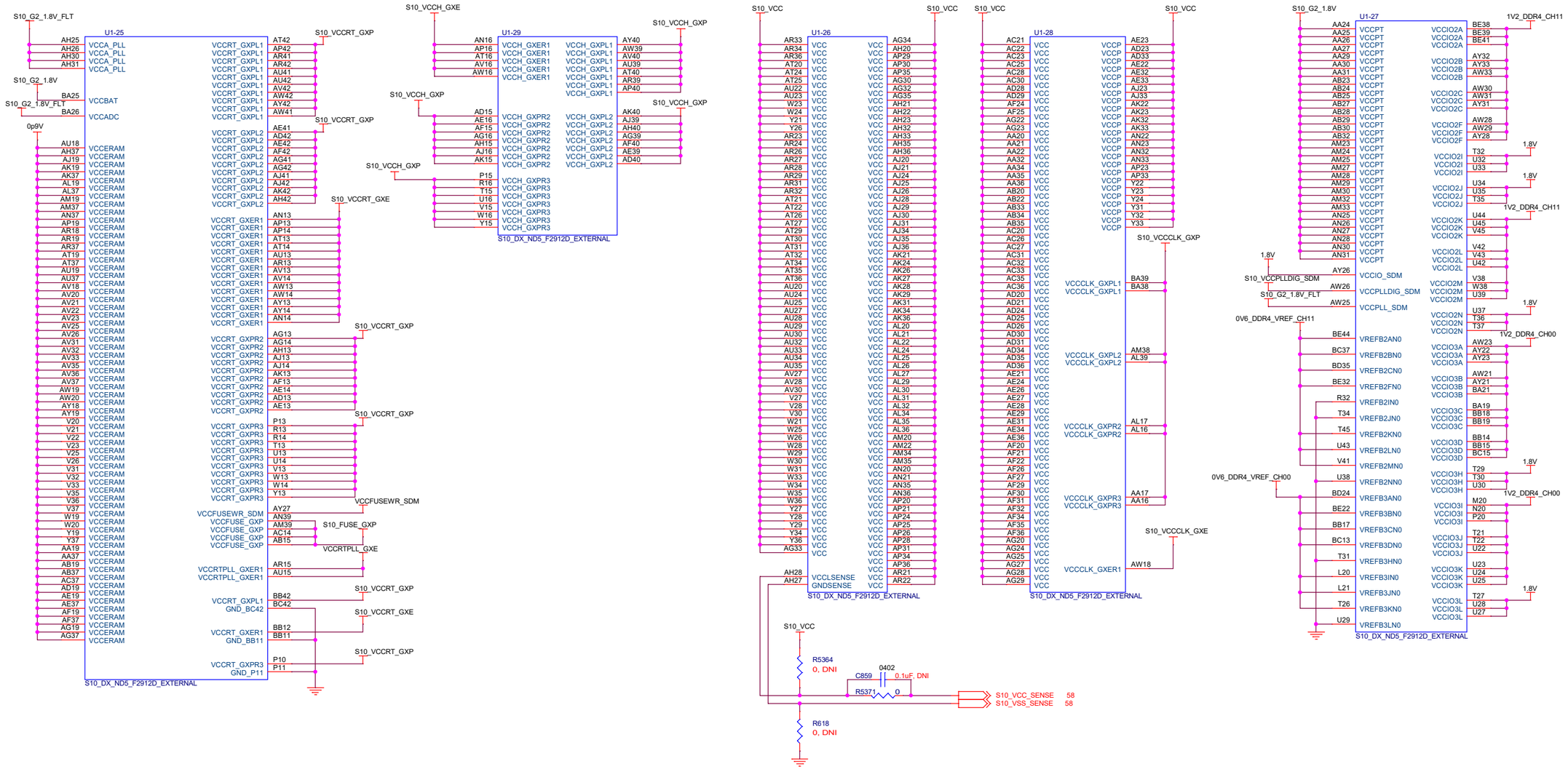
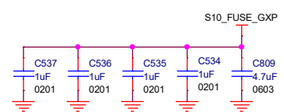
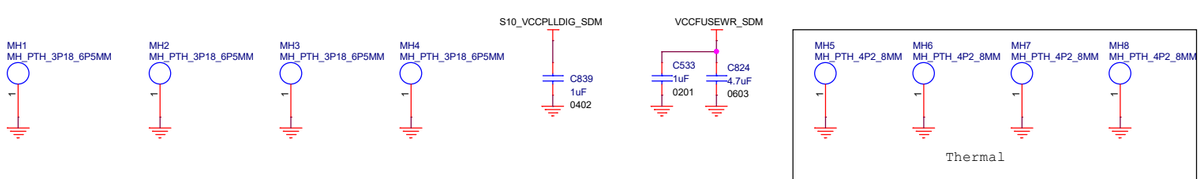
S10 DX Power







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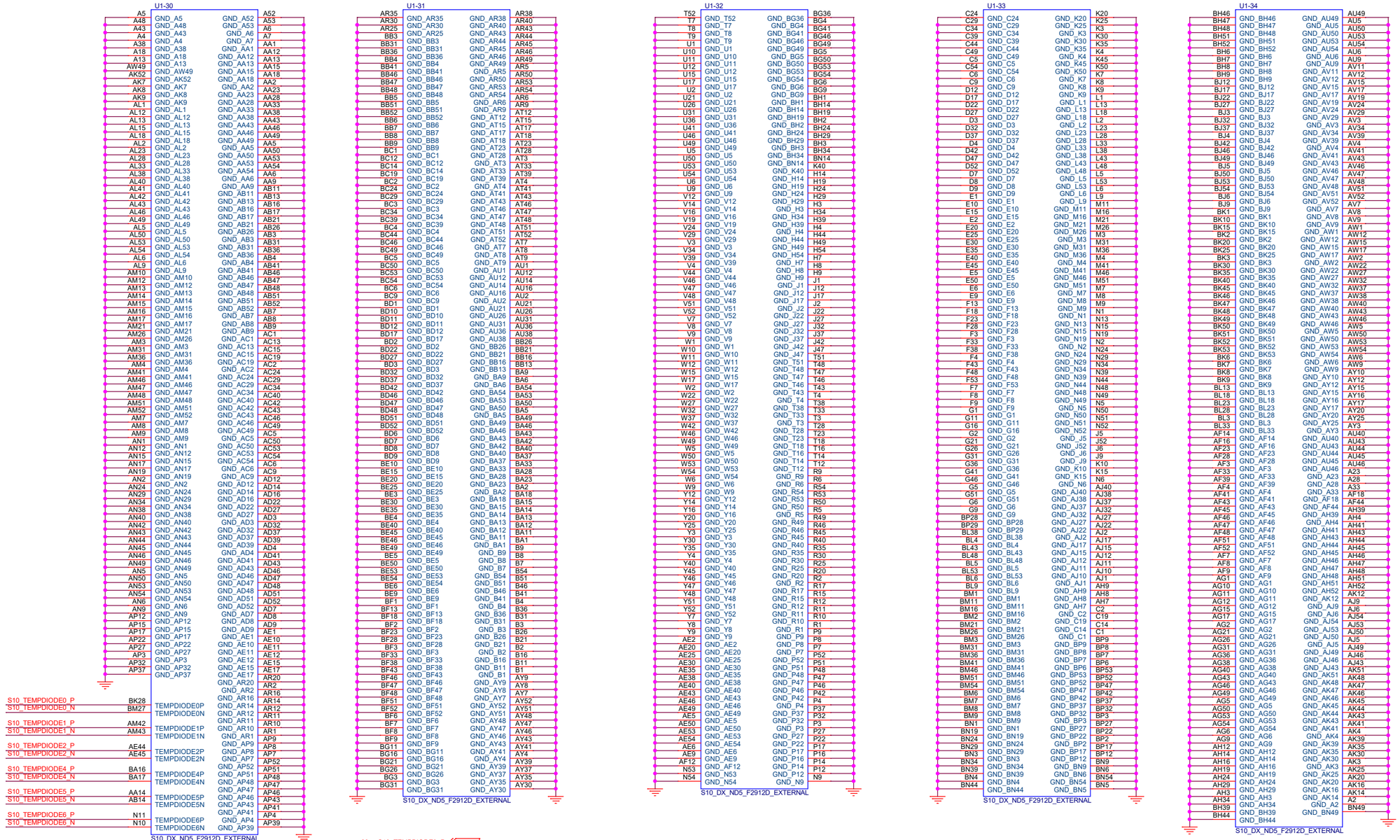
S10 DX Ground



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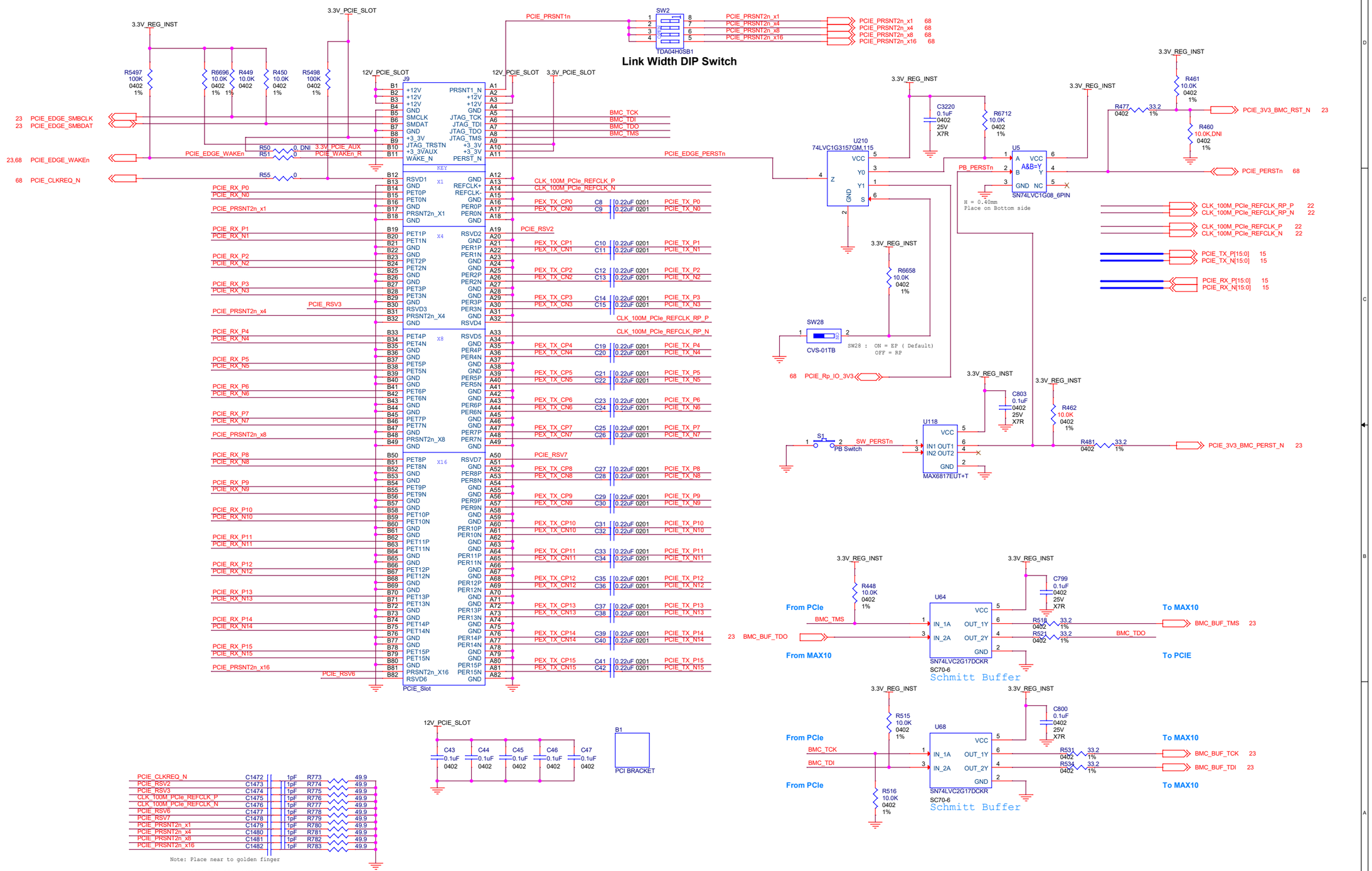
PCIe Edge x16 Gold Fingers



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Title: Stratix 10 DX FPGA DEVKIT Board

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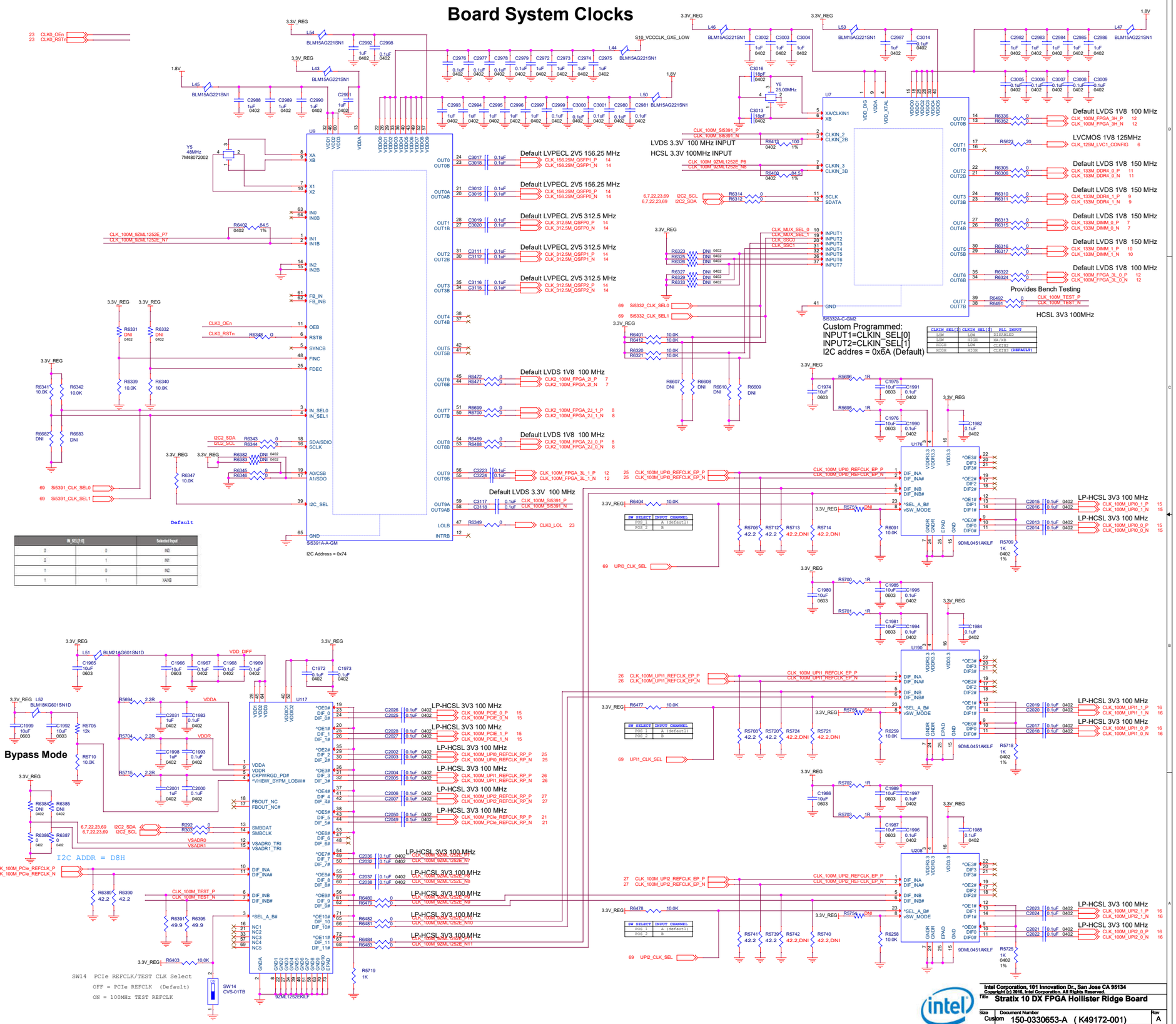
Board System Clocks



IN_SEL[1:0]		Selected Input
0	0	IN0
0	1	IN1
1	0	IN2
1	1	XA/XB

Default

CLKIN_SEL[1]	CLKIN_SEL[0]	PLL INPUT
LOW	LOW	DISABLED
LOW	HIGH	XA/XB
HIGH	LOW	CLKIN2
HIGH	HIGH	CLKIN1 (DEFAULT)

SW SELECT	INPUT CHANNEL
POS 1	A (default)
POS 2	B

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Title: Stratix 10 DX FPGA Hollister Ridge Board

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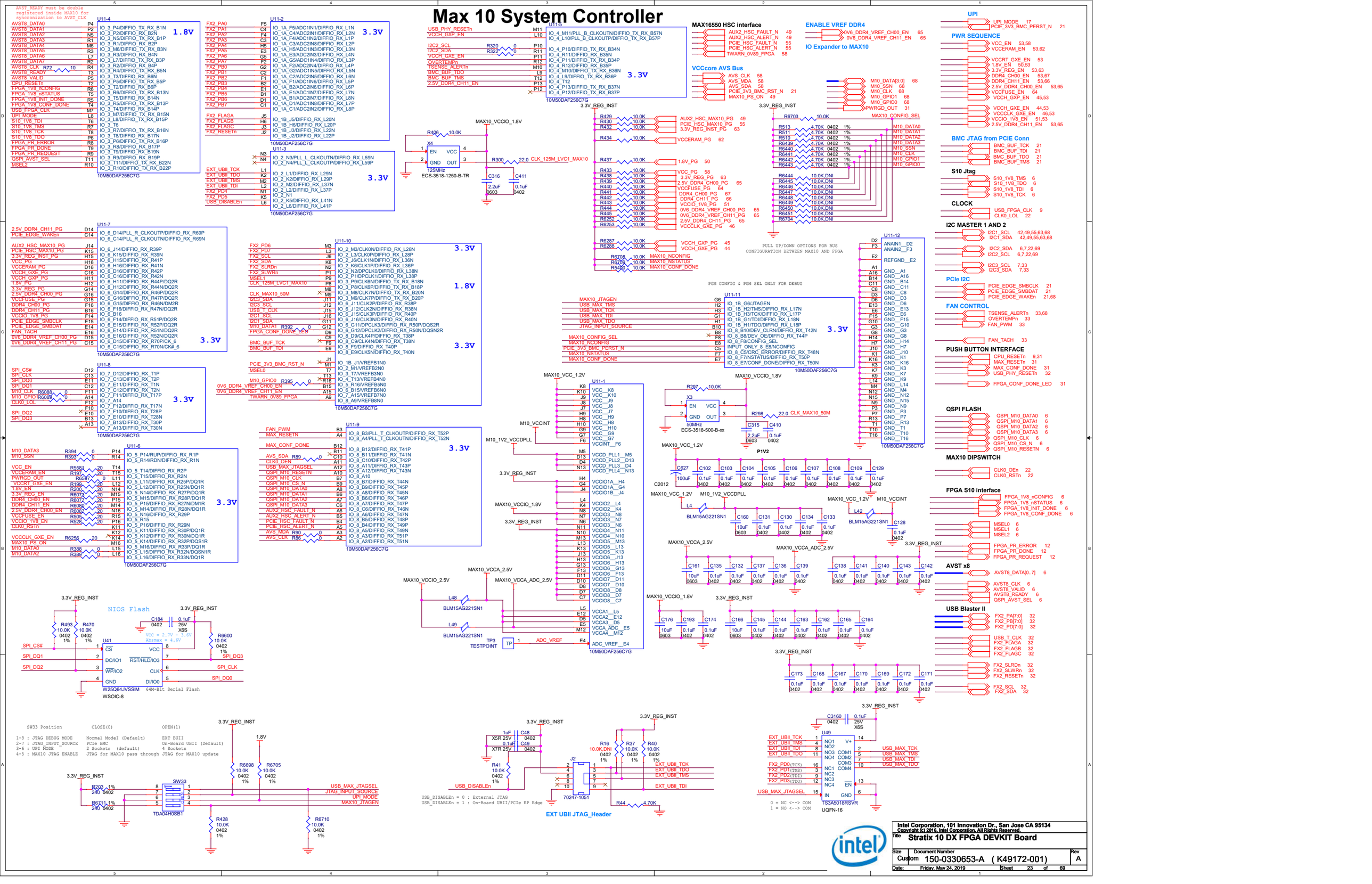
Max 10 System Controller



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Title: Stratix 10 DX FPGA DEVKIT Board

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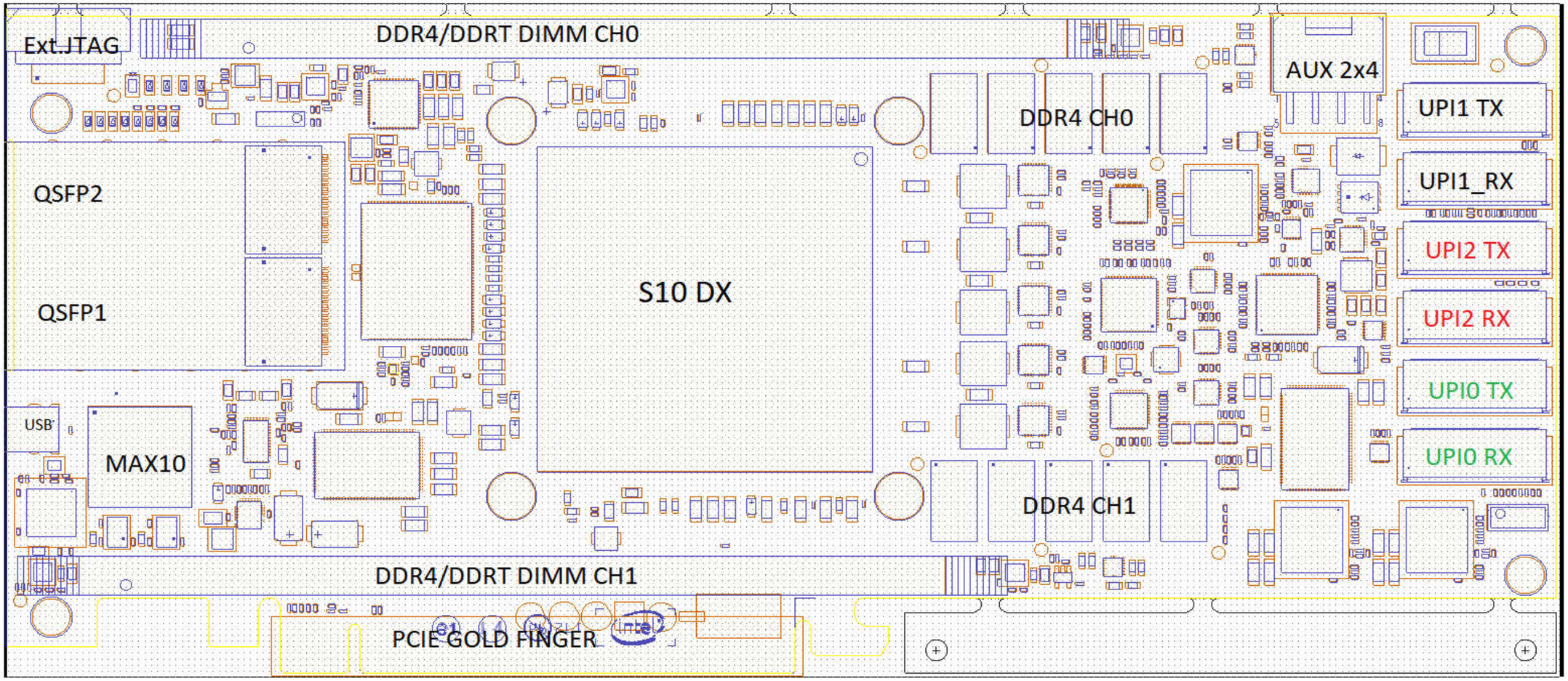
S10DX Devkit Board Diagram



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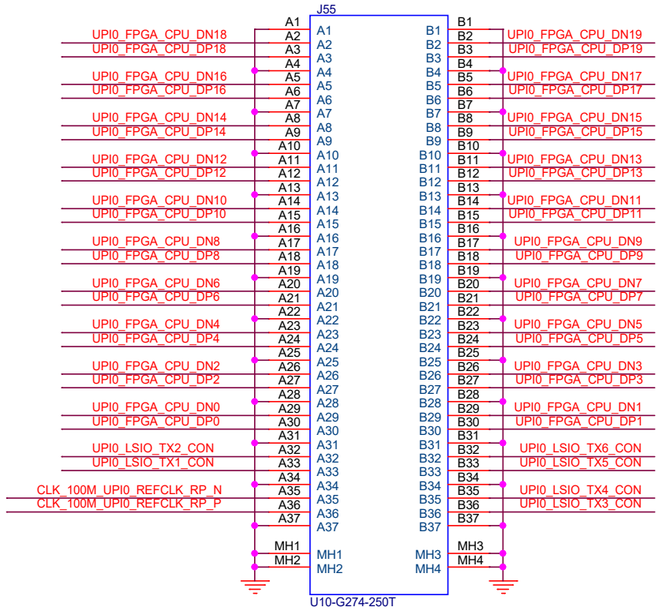
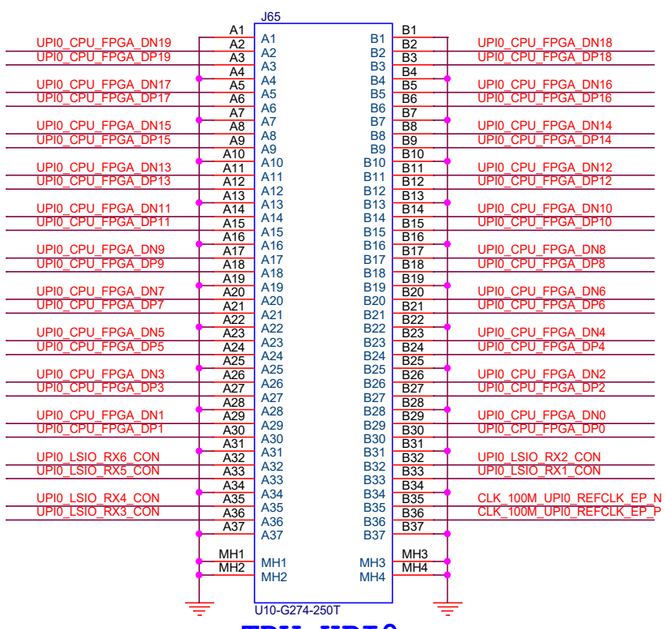
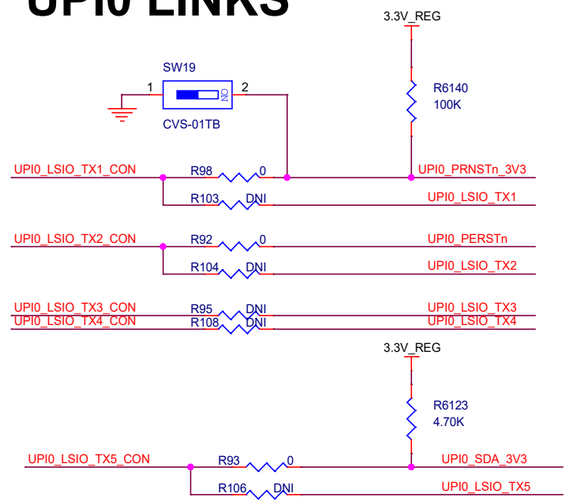
UPI0 LINKS

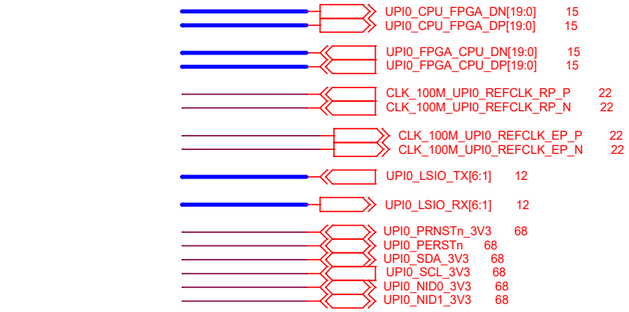


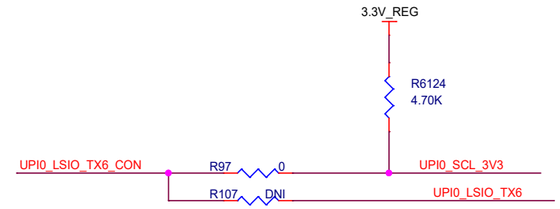
Note:
LSIO signals carry 3.3V in PCIe mode
or 1.8V in UPI mode.
Default mode is PCIe

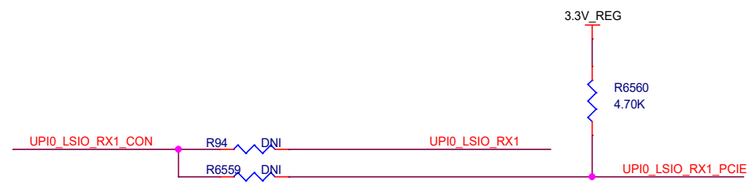


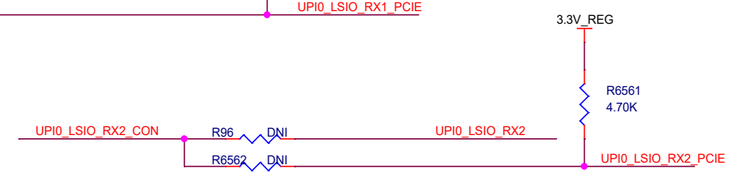
TDV UPI0

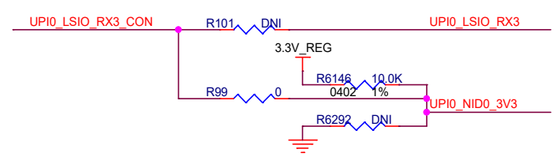


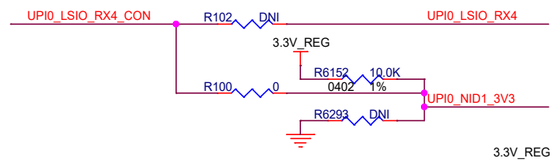


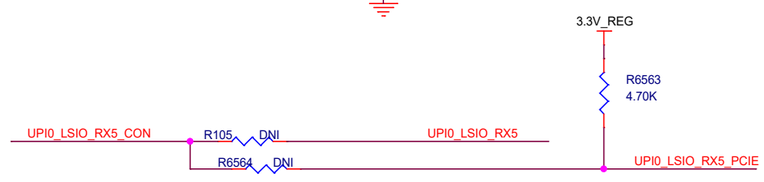


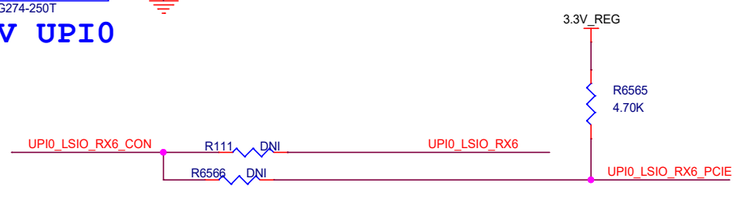












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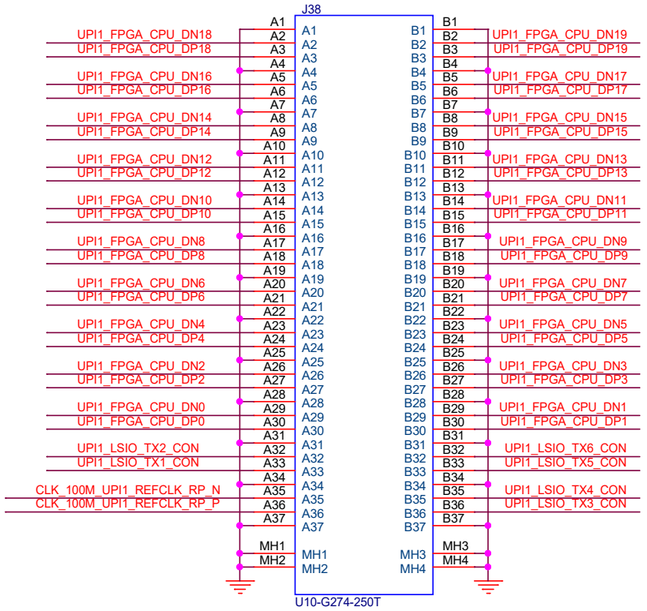
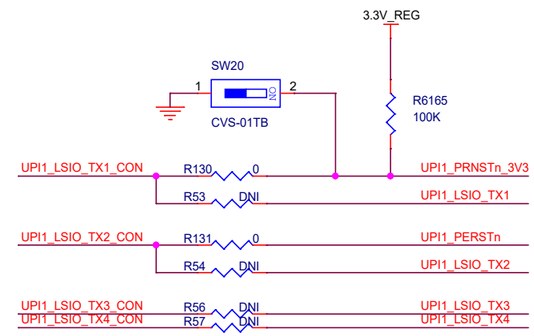
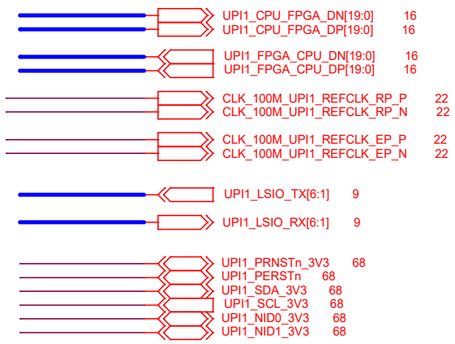
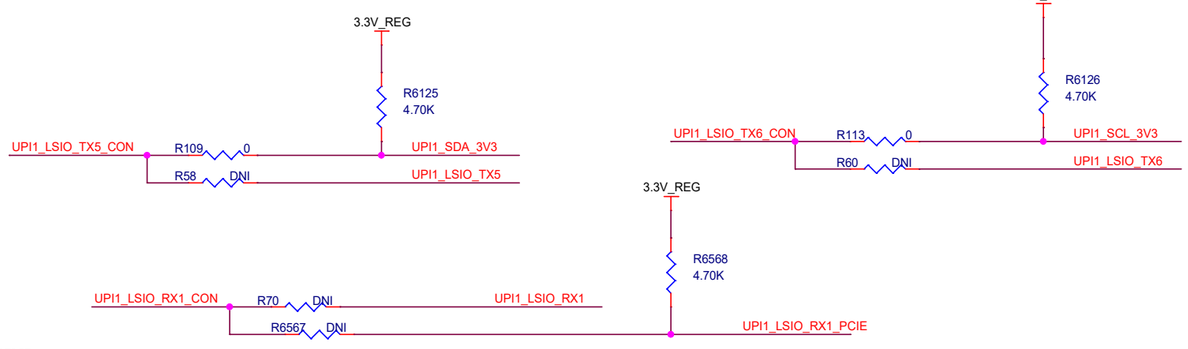
UPI1 LINK



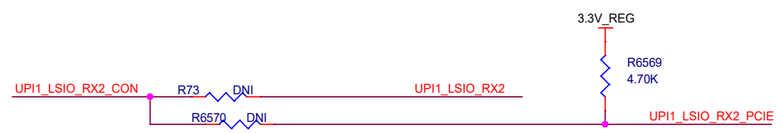


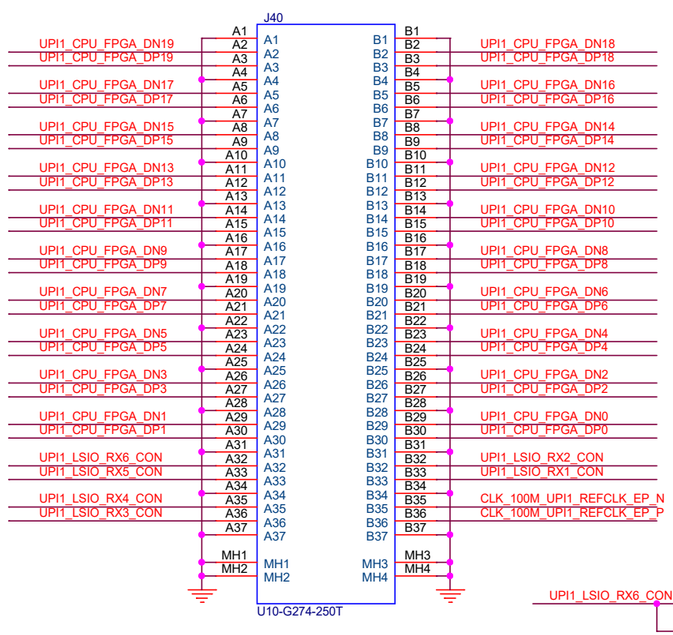


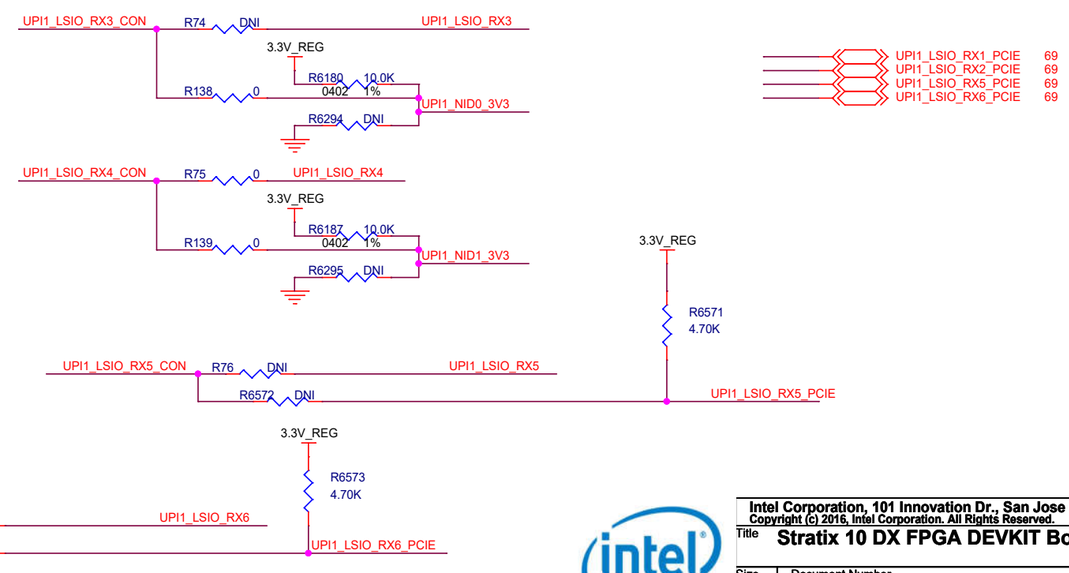


Note:
LSIO signals carry 3.3V in PCIe mode
or 1.8V in UPI mode.
Default mode is PCIe

UPI1 ONLY SUPPOR SLAVE EP PCIE OR UPI SLAVE MODE ON FPGA INTERFACE







TDV UPI1

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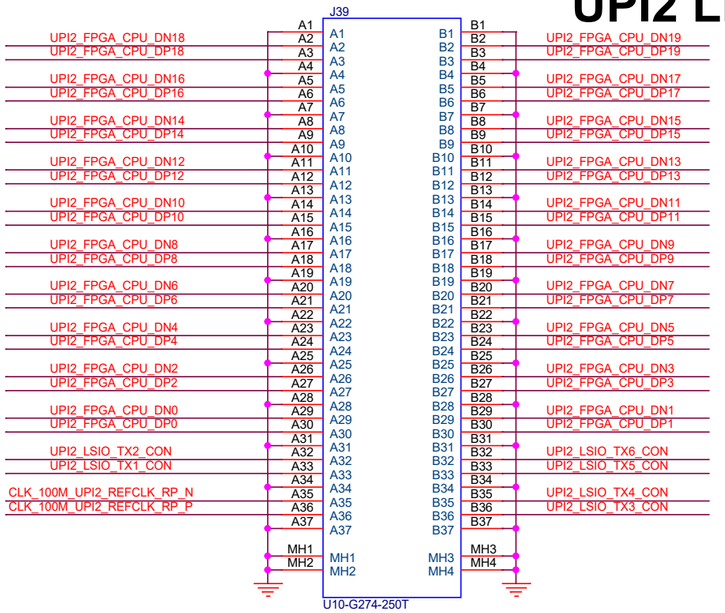
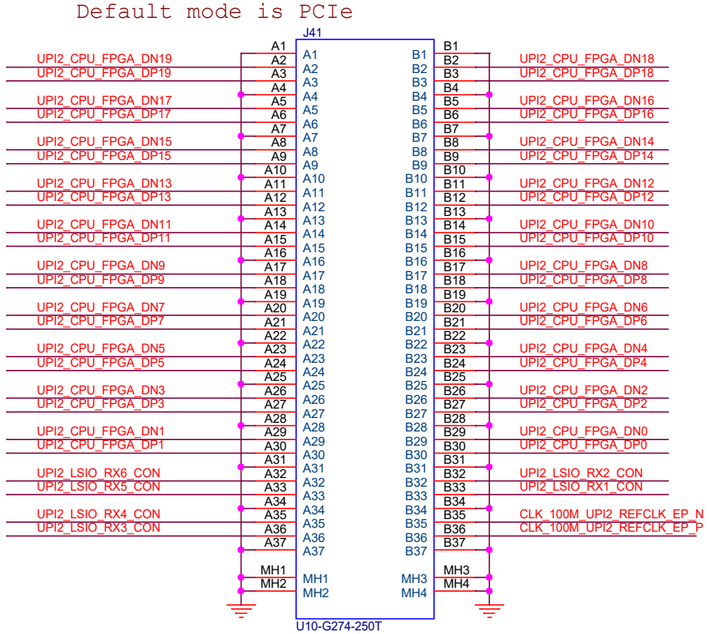
UPI2 LINK

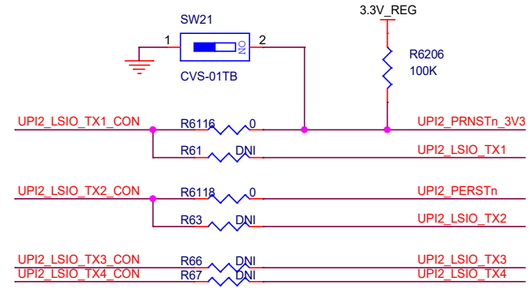


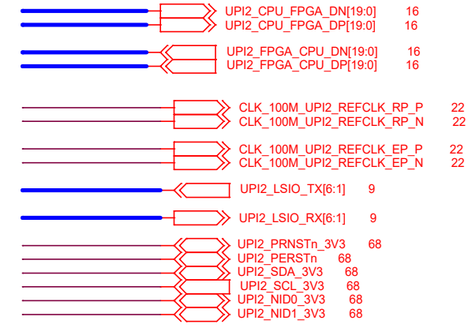
UPI1 ONLY SUPPOR SLAVE EP PCIE OR UPI SLAVE MODE ON FPGA INTERFACE

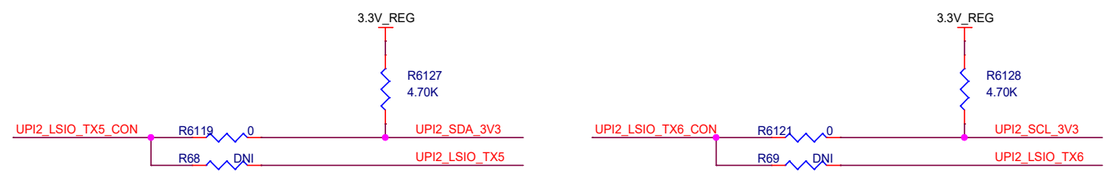
Note:
LSIO signals carry 3.3V in PCIe mode
or 1.8V in UPI mode.
Default mode is PCIe

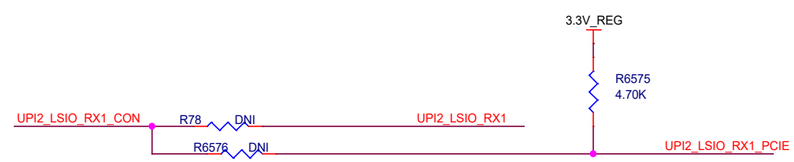


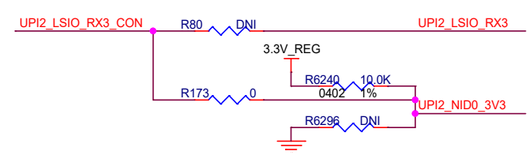
TDV UPI2

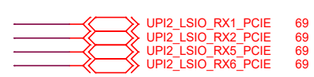


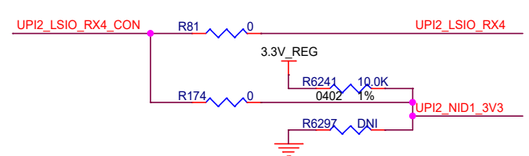


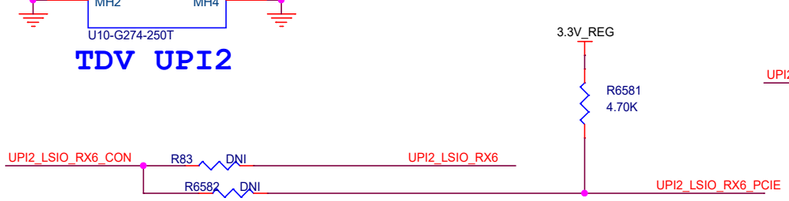












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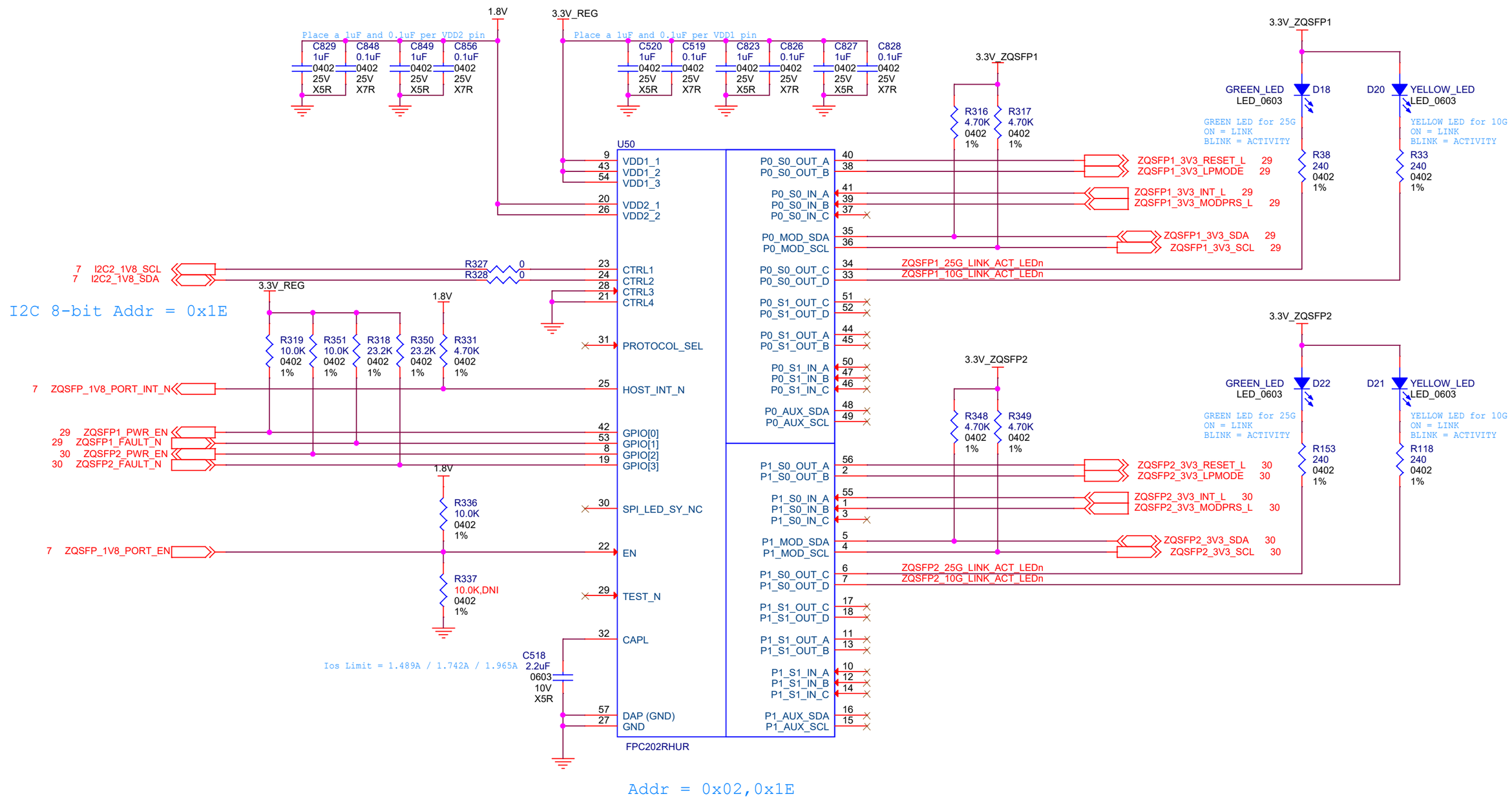
zQSFP Controller



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QSFP1

Quad Small Form-factor Pluggable (QSFP) Interface

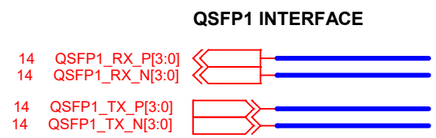
NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

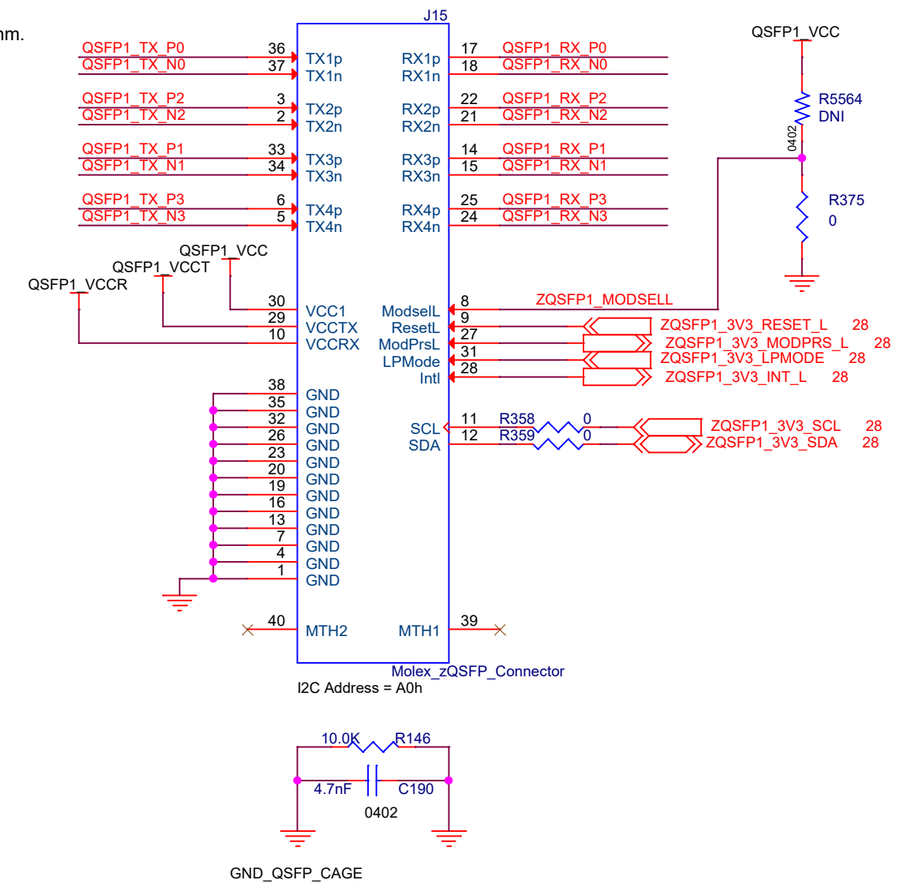
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

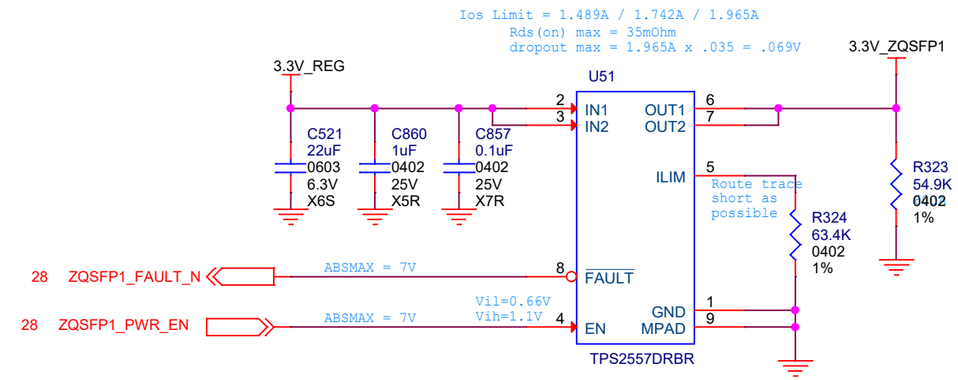
NOTE 3: DC blocking capacitors are in the module for RX and TX.

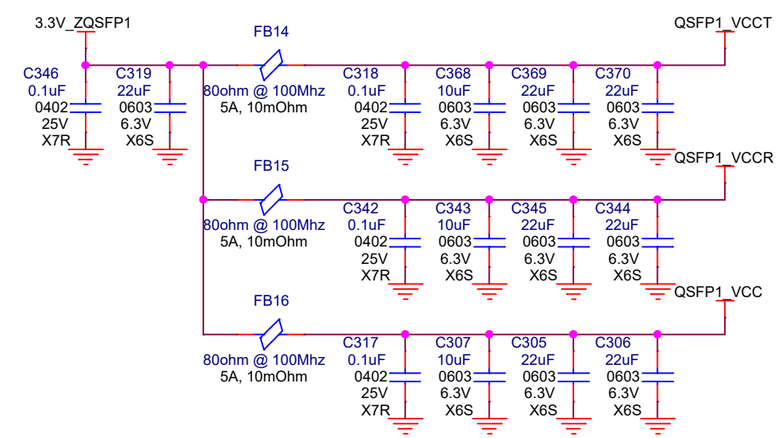
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.

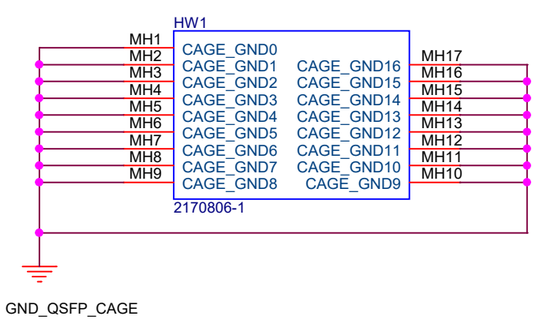
Support both CAUI2 and 4x25G ethernet











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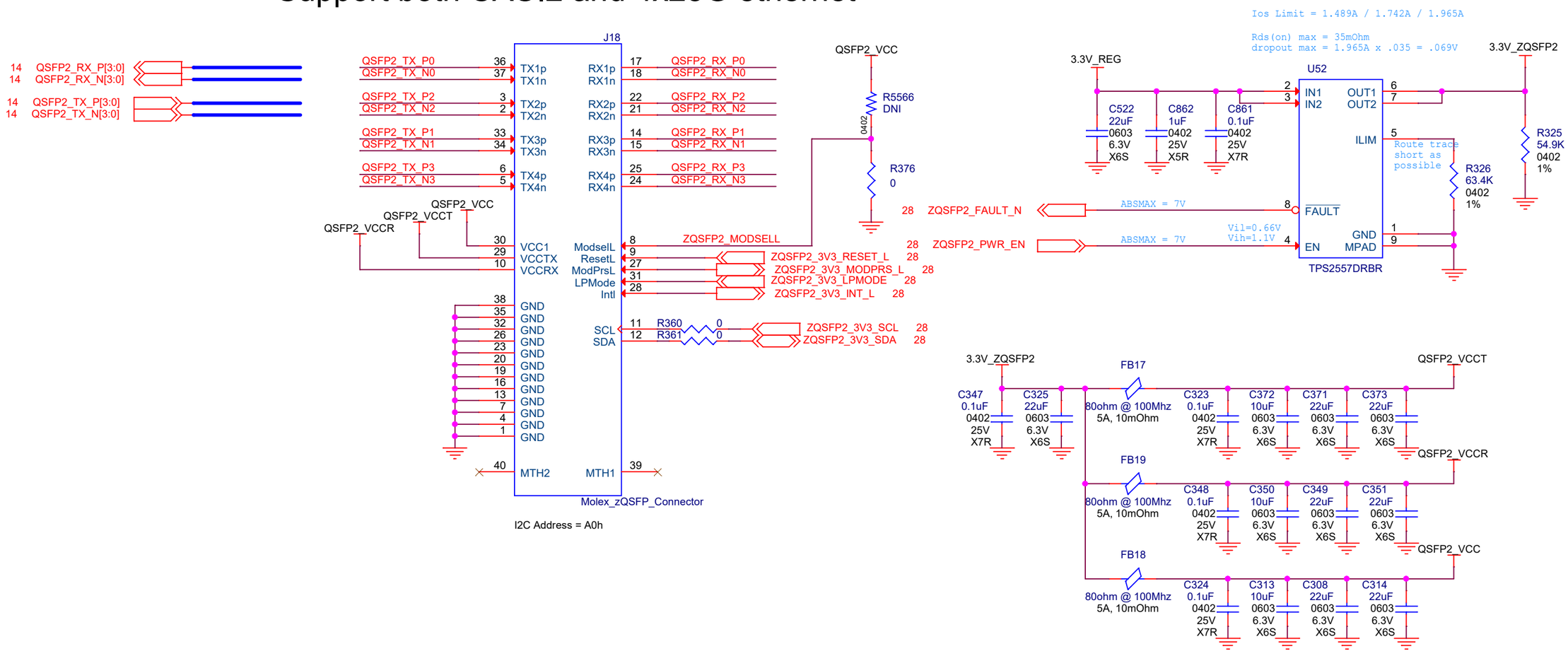
QSFP2

Support both CAUI2 and 4x25G ethernet



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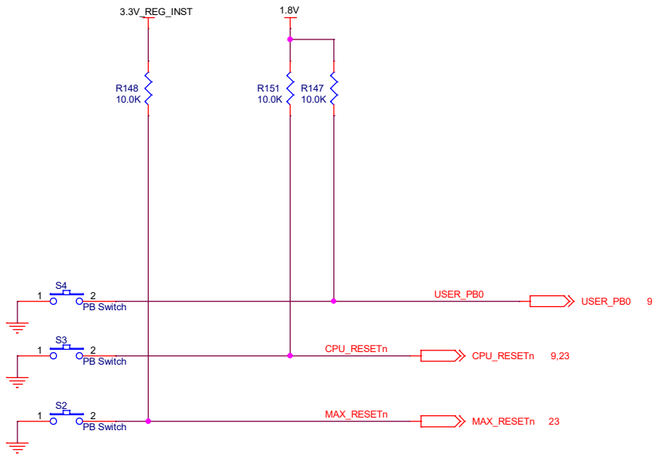
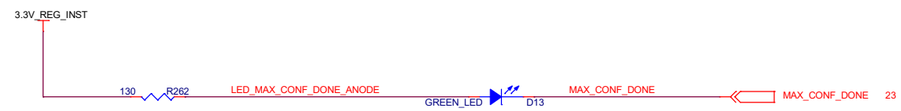
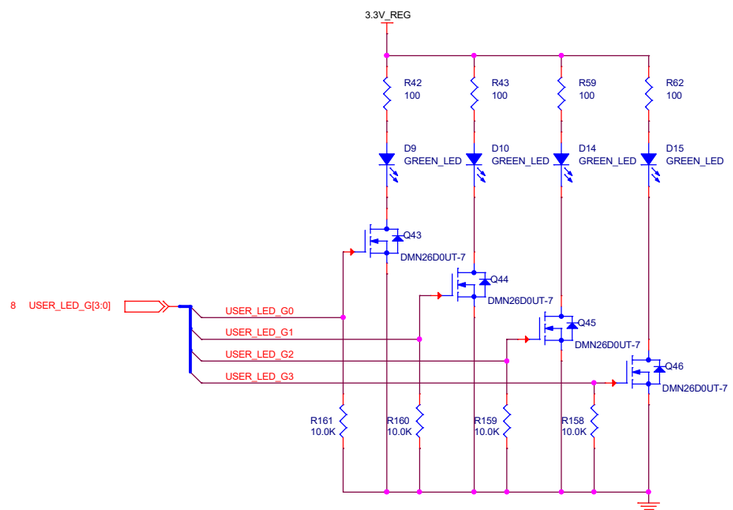
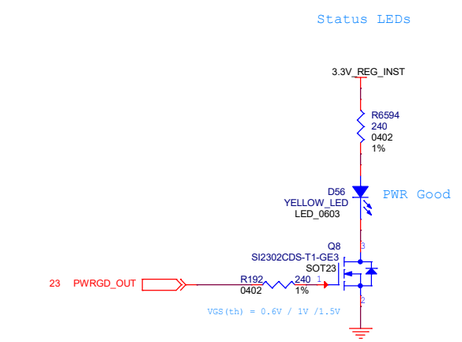
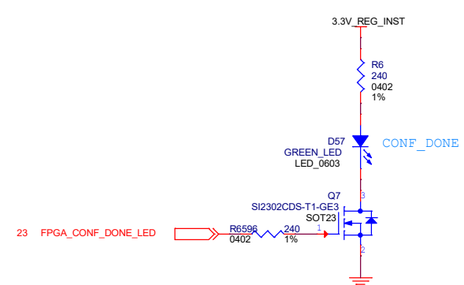
User PB, SW, I/Os











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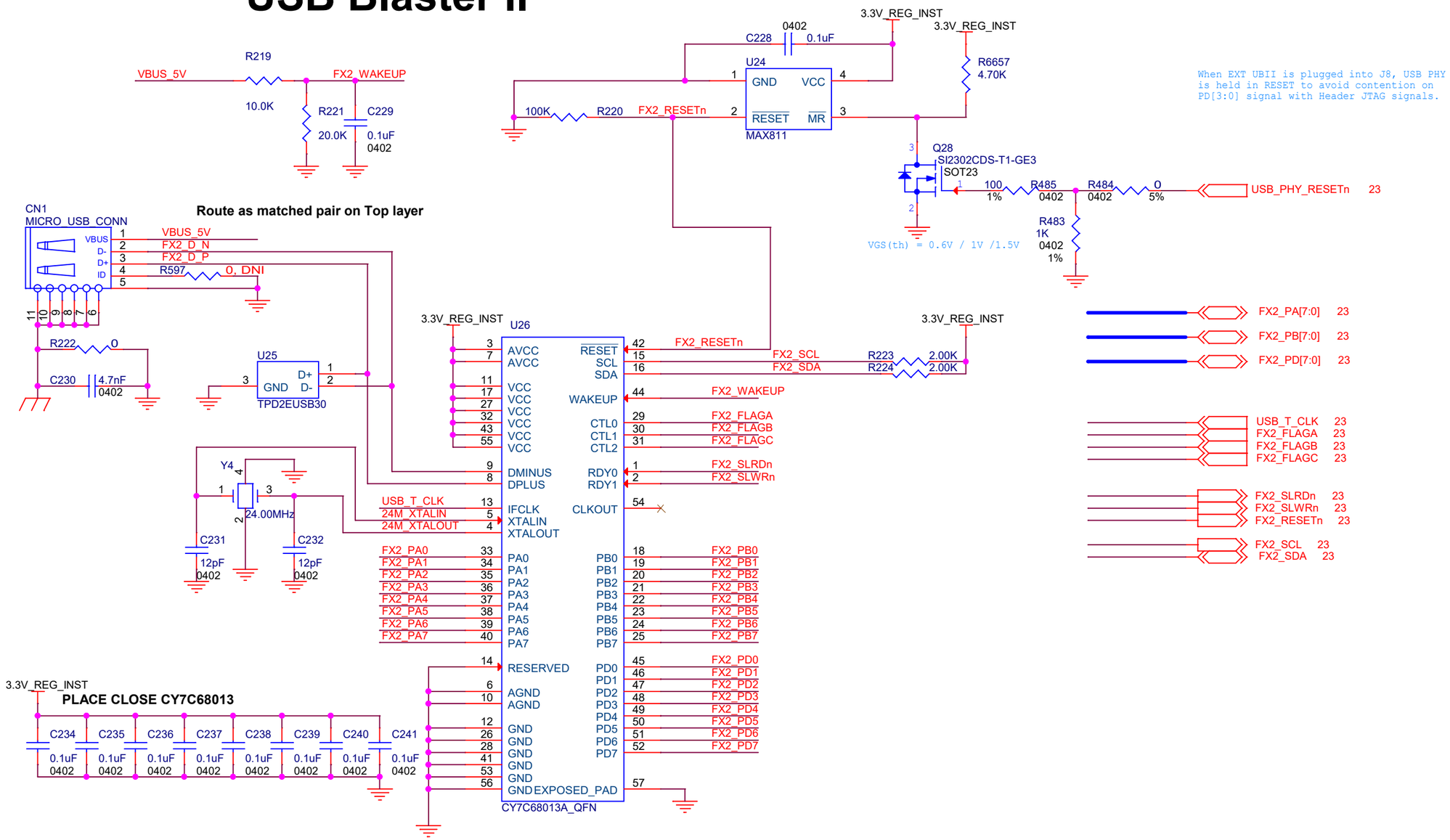
USB Blaster II



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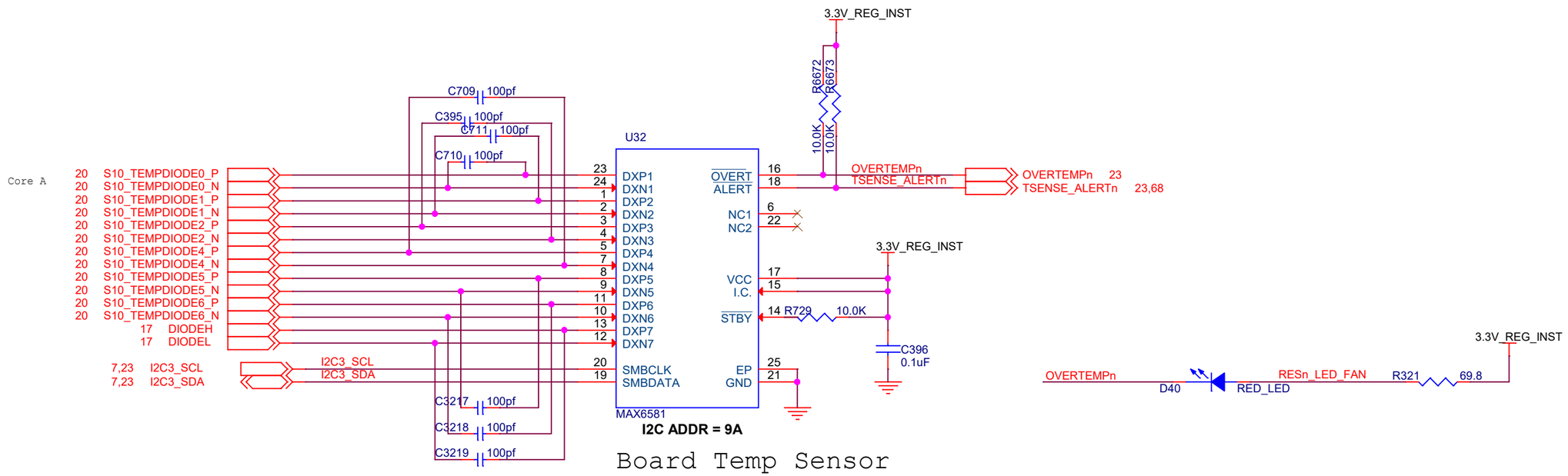
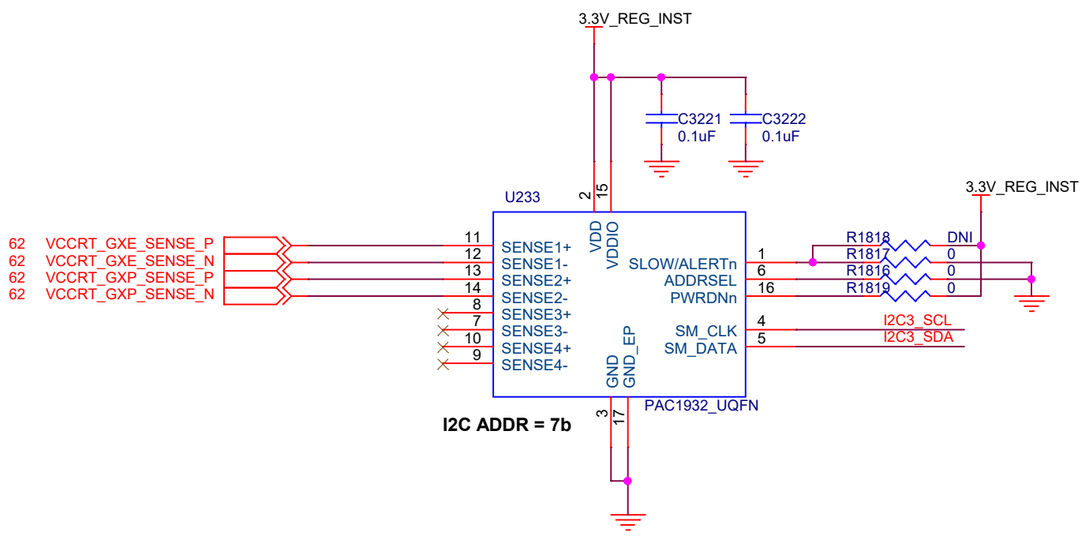
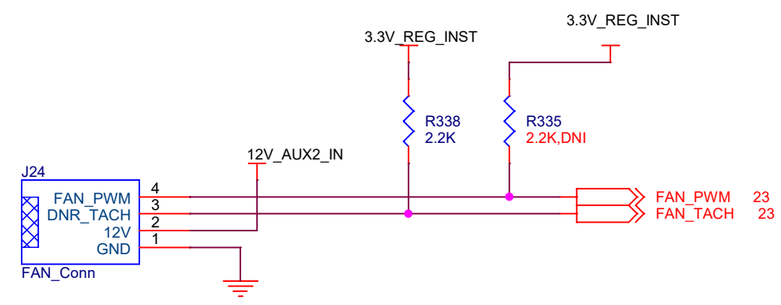
Temp Sense, fan connector







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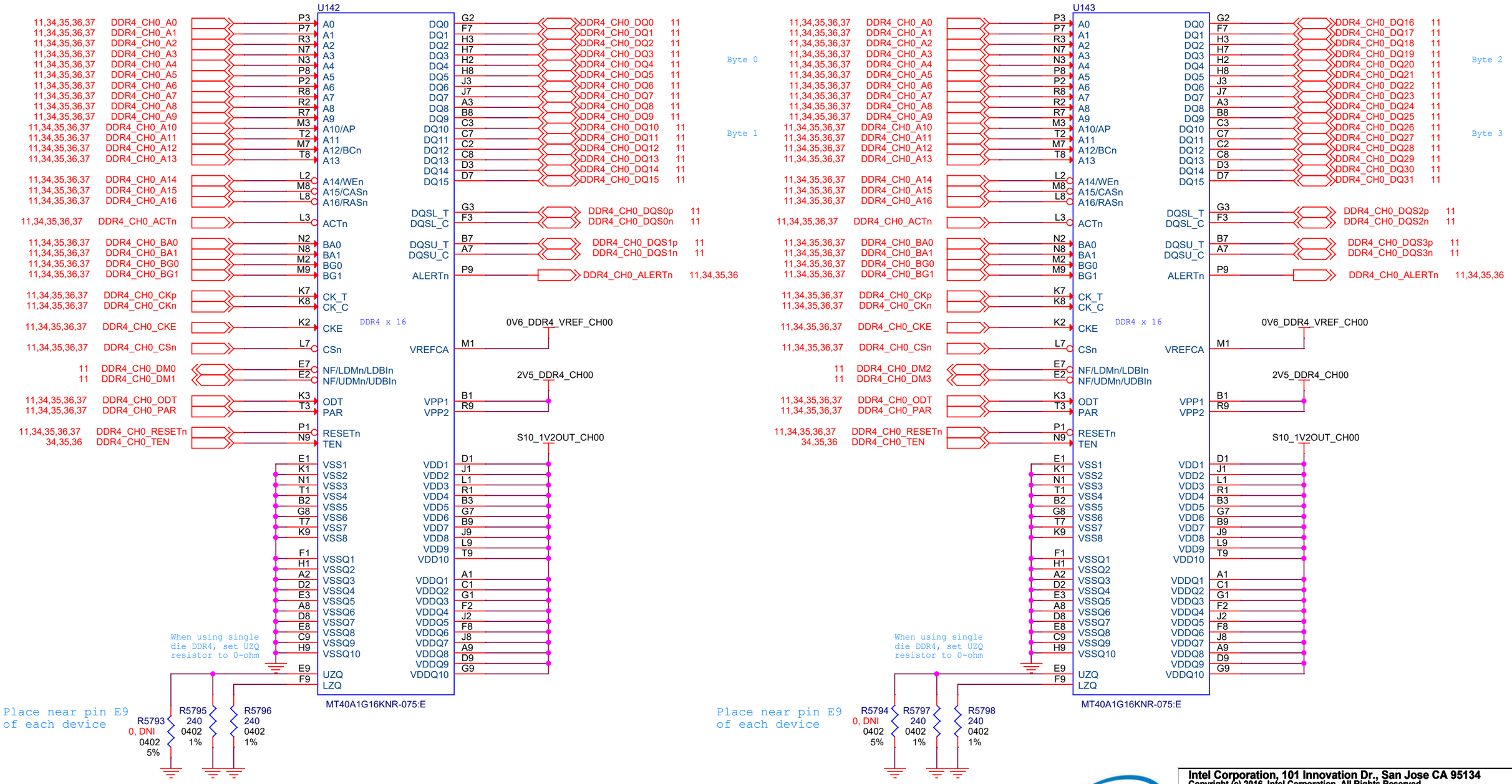
DDR4 CH0 Part1



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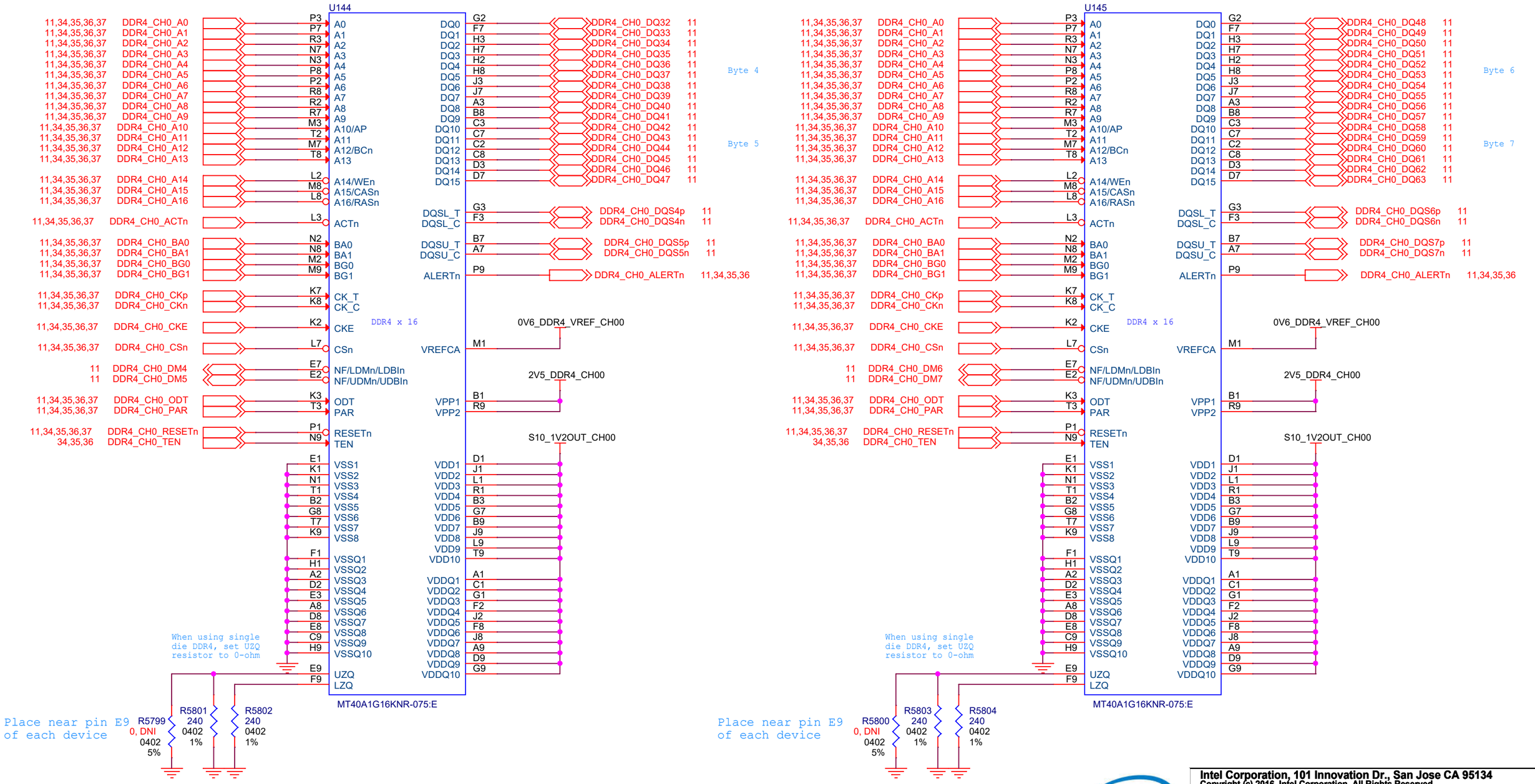
DDR4 CH0 Part2



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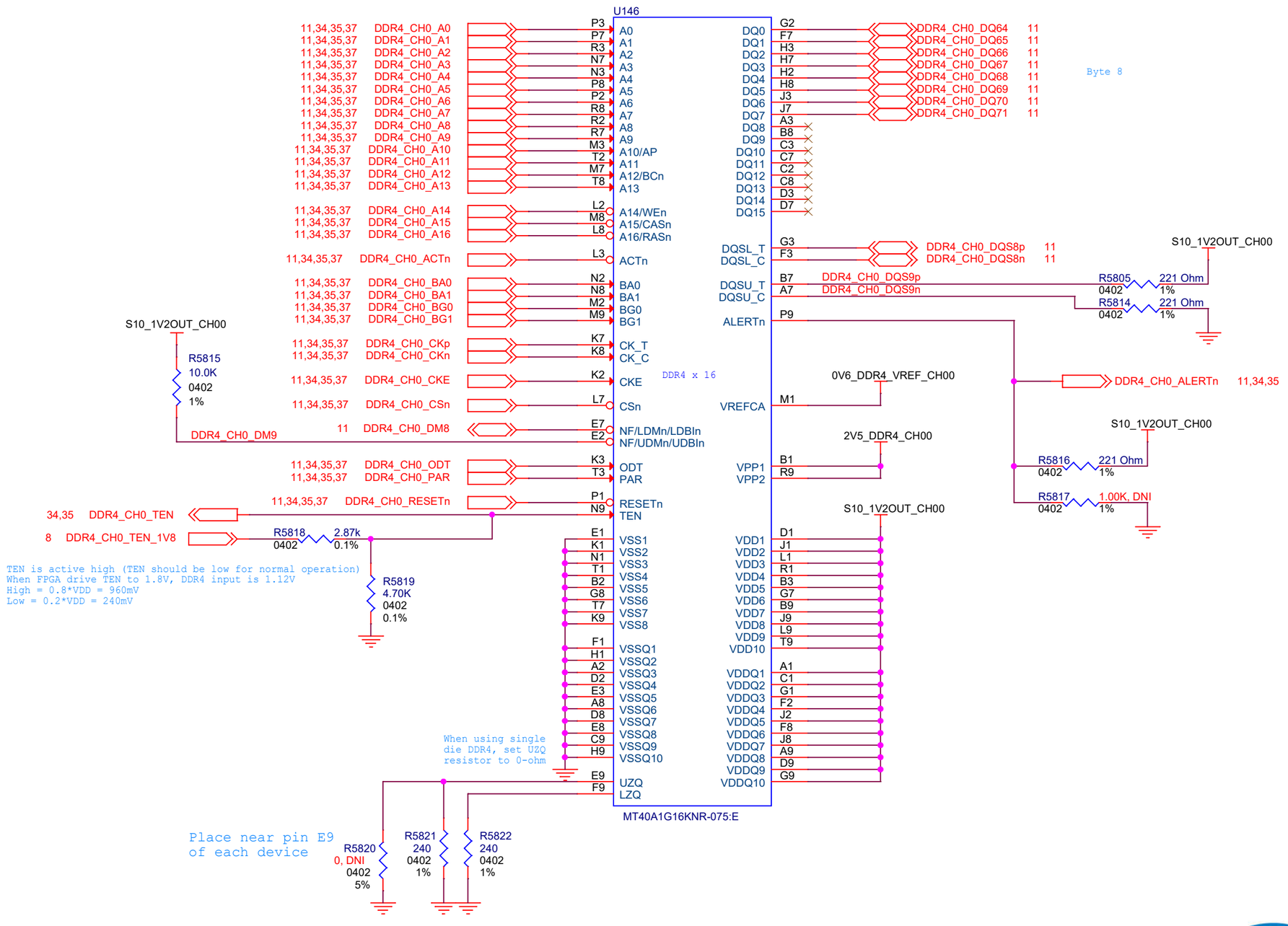
DDR4 CH0 Part3



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DDR4 CH0 Part4

0V6_DDR4_VTT_CH00

11,34,35,36	DDR4_CH0_A0	R5823	39	0402 1%
11,34,35,36	DDR4_CH0_A1	R5824	39	0402 1%
11,34,35,36	DDR4_CH0_A2	R5825	39	0402 1%
11,34,35,36	DDR4_CH0_A3	R5826	39	0402 1%
11,34,35,36	DDR4_CH0_A4	R5827	39	0402 1%
11,34,35,36	DDR4_CH0_A5	R5828	39	0402 1%
11,34,35,36	DDR4_CH0_A6	R5829	39	0402 1%
11,34,35,36	DDR4_CH0_A7	R5830	39	0402 1%
11,34,35,36	DDR4_CH0_A8	R5831	39	0402 1%
11,34,35,36	DDR4_CH0_A9	R5832	39	0402 1%
11,34,35,36	DDR4_CH0_A10	R5833	39	0402 1%
11,34,35,36	DDR4_CH0_A11	R5834	39	0402 1%
11,34,35,36	DDR4_CH0_A12	R5835	39	0402 1%
11,34,35,36	DDR4_CH0_A13	R5836	39	0402 1%
11,34,35,36	DDR4_CH0_A14	R5837	39	0402 1%
11,34,35,36	DDR4_CH0_A15	R5838	39	0402 1%
11,34,35,36	DDR4_CH0_A16	R5839	39	0402 1%
11,34,35,36	DDR4_CH0_BA0	R5840	39	0402 1%
11,34,35,36	DDR4_CH0_BA1	R5841	39	0402 1%
11,34,35,36	DDR4_CH0_CSn	R5842	39	0402 1%
11,34,35,36	DDR4_CH0_ACTn	R5843	39	0402 1%
11,34,35,36	DDR4_CH0_ODT	R5844	39	0402 1%
11,34,35,36	DDR4_CH0_PAR	R5845	39	0402 1%
11,34,35,36	DDR4_CH0_BG0	R5846	39	0402 1%
11,34,35,36	DDR4_CH0_BG1	R5847	39	0402 1%
11,34,35,36	DDR4_CH0_CKE	R5848	39	0402 1%

S10_1V2OUT_CH00

11,34,35,36	DDR4_CH0_RESETn	R5849	1K	0402 1%
		R5850	1.00K, DNI	0402 1%

11,34,35,36	DDR4_CH0_CKp	R5851	36.5 Ohm	0402 1%
11,34,35,36	DDR4_CH0_CKn	R5852	36.5 Ohm	0402 1%

C2159 10nF 0402 50V X7R

0V6_DDR4_VTT_CH00 S10_1V2OUT_CH00

C2090	0.1uF	0402 25V X7R
C2094	0.1uF	0402 25V X7R
C2098	0.1uF	0402 25V X7R
C2101	0.1uF	0402 25V X7R
C2104	0.1uF	0402 25V X7R
C2108	0.1uF	0402 25V X7R
C2112	0.1uF	0402 25V X7R
C2116	0.1uF	0402 25V X7R
C2119	0.1uF	0402 25V X7R
C2122	0.1uF	0402 25V X7R

2V5_DDR4_CH00

C2132	0.1uF	0402 25V X7R
C2135	0.1uF	0402 25V X7R
C2138	0.1uF	0402 25V X7R
C2140	0.1uF	0402 25V X7R
C2142	0.1uF	0402 25V X7R
C2144	0.1uF	0402 25V X7R
C2146	0.1uF	0402 25V X7R
C2148	0.1uF	0402 25V X7R
C2150	0.1uF	0402 25V X7R
C2152	0.1uF	0402 25V X7R

2V5_DDR4_CH00

C3225 4.7uF

S10_1V2OUT_CH00

C2091	0.1uF	0402 25V X7R
C2095	0.1uF	0402 25V X7R
C2099	0.1uF	0402 25V X7R
C2102	0.1uF	0402 25V X7R
C2105	0.1uF	0402 25V X7R
C2109	0.1uF	0402 25V X7R
C2113	0.1uF	0402 25V X7R
C2117	0.1uF	0402 25V X7R
C2120	0.1uF	0402 25V X7R
C2123	0.1uF	0402 25V X7R
C2126	0.1uF	0402 25V X7R
C2129	0.1uF	0402 25V X7R
C2133	0.1uF	0402 25V X7R
C2136	0.1uF	0402 25V X7R
C2139	0.1uF	0402 25V X7R
C2141	0.1uF	0402 25V X7R
C2143	0.1uF	0402 25V X7R
C2145	0.1uF	0402 25V X7R
C2147	0.1uF	0402 25V X7R
C2149	0.1uF	0402 25V X7R
C2151	0.1uF	0402 25V X7R
C2153	0.1uF	0402 25V X7R
C2154	0.1uF	0402 25V X7R
C2155	0.1uF	0402 25V X7R
C2157	0.1uF	0402 25V X7R
C2158	0.1uF	0402 25V X7R
C2160	0.1uF	0402 25V X7R
C2161	0.1uF	0402 25V X7R

S10_1V2OUT_CH00

C2092	0.1uF	0402 25V X7R
C2096	0.1uF	0402 25V X7R
C2100	0.1uF	0402 25V X7R
C2103	0.1uF	0402 25V X7R
C2106	0.1uF	0402 25V X7R
C2110	0.1uF	0402 25V X7R
C2114	0.1uF	0402 25V X7R
C2118	0.1uF	0402 25V X7R
C2121	0.1uF	0402 25V X7R
C2124	0.1uF	0402 25V X7R
C2127	0.1uF	0402 25V X7R
C2130	0.1uF	0402 25V X7R

S10_1V2OUT_CH00

C2093	4.7uF	0402 6.3V X5R
C2097	4.7uF	0402 6.3V X5R

0V6_DDR4_VTT_CH00 S10_1V2OUT_CH00

C2107	0.1uF	0402 25V X7R
C2111	0.1uF	0402 25V X7R
C2115	0.1uF	0402 25V X7R

0V6_DDR4_VREF_CH00 S10_1V2OUT_CH00

C2125	0.1uF	0402 25V X7R
C2128	0.1uF	0402 25V X7R
C2131	0.1uF	0402 25V X7R
C2134	0.1uF	0402 25V X7R
C2137	0.1uF	0402 25V X7R

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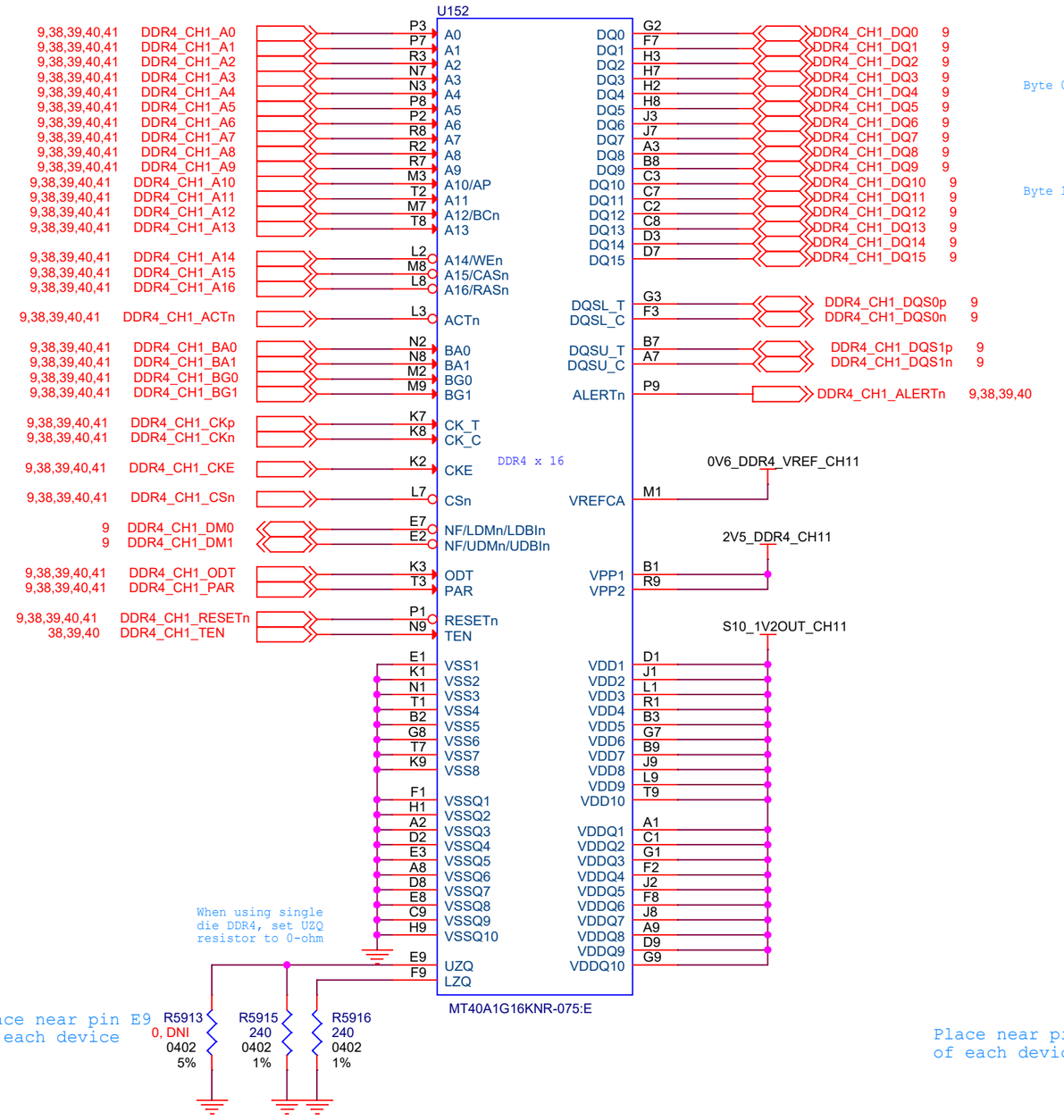
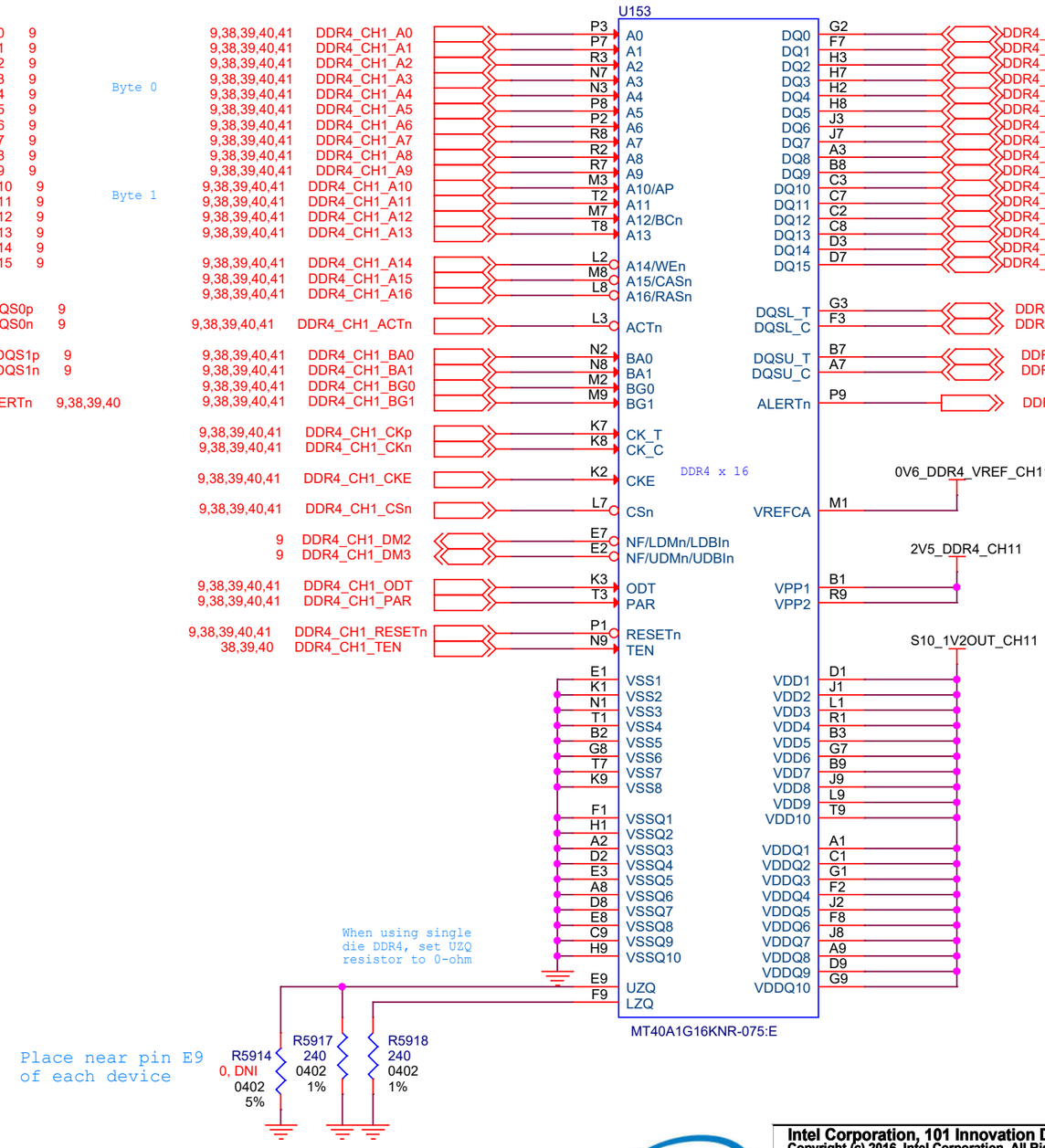
DDR4 CH1 Part1





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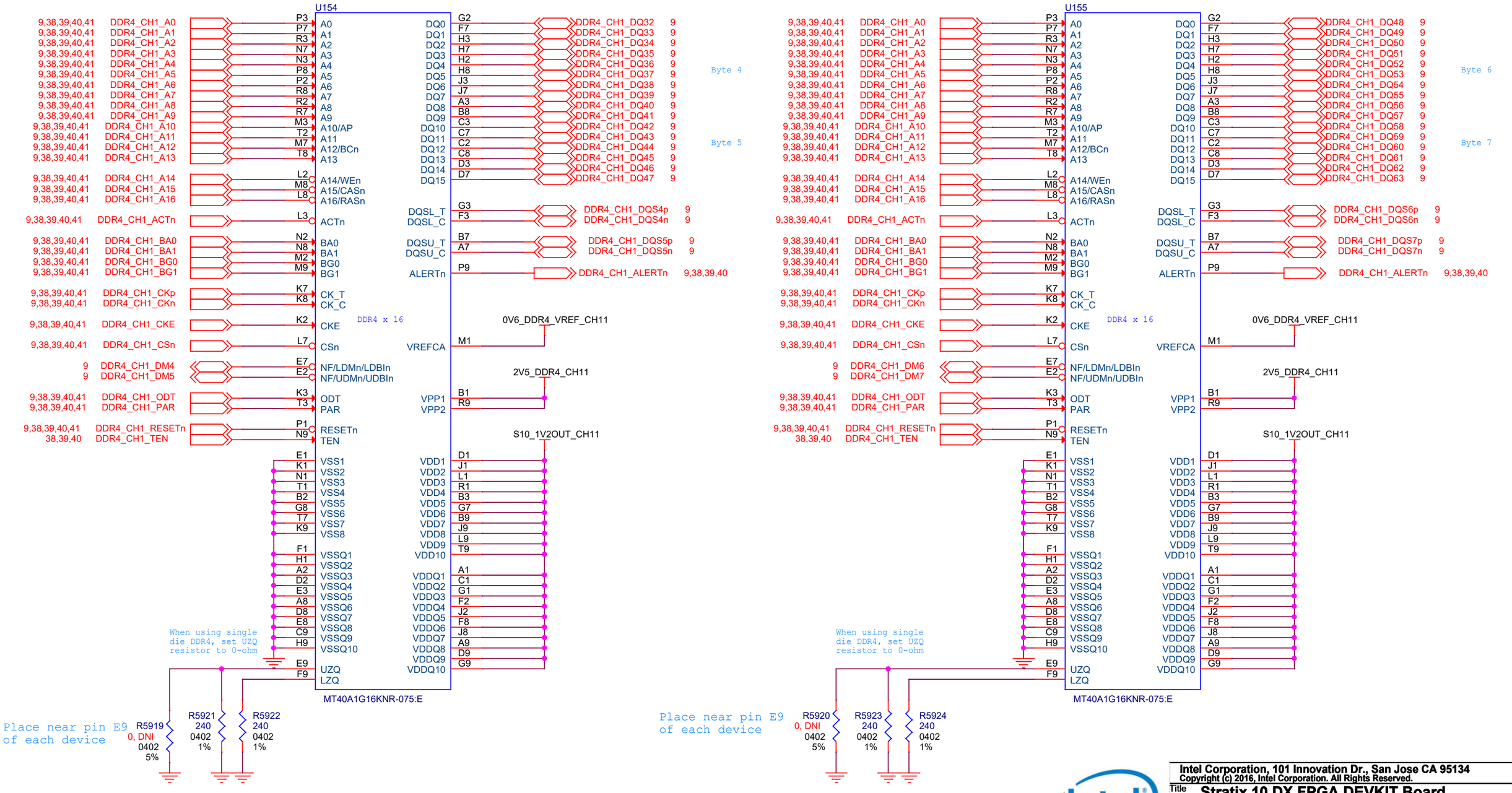
DDR4 CH1 Part2



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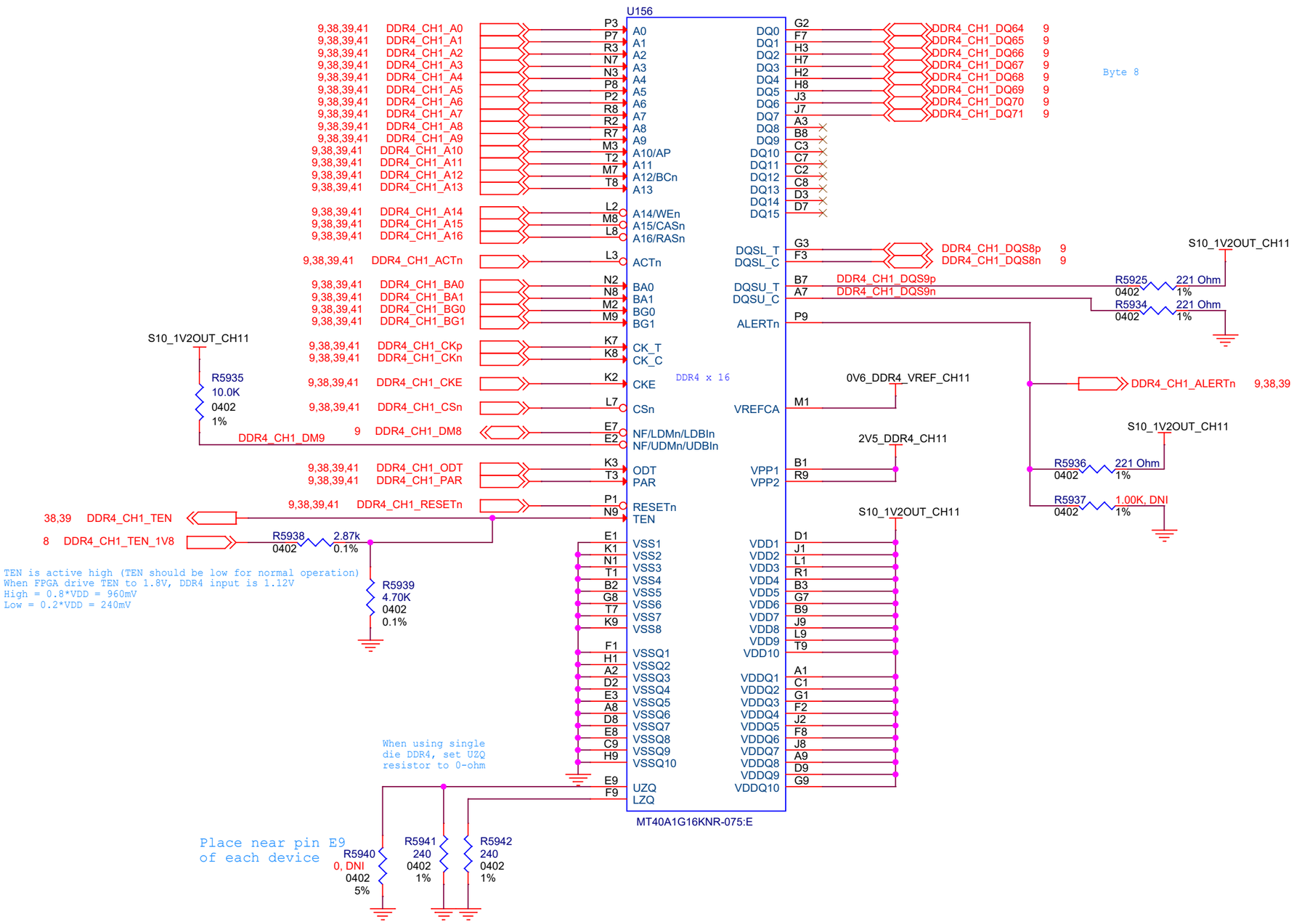
DDR4 CH1 Part3



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DDR4 CH1 Part4

0V6_DDR4_VTT_CH11

9,38,39,40	DDR4_CH1_A0	R5943	39	0402 1%
9,38,39,40	DDR4_CH1_A1	R5944	39	0402 1%
9,38,39,40	DDR4_CH1_A2	R5945	39	0402 1%
9,38,39,40	DDR4_CH1_A3	R5946	39	0402 1%
9,38,39,40	DDR4_CH1_A4	R5947	39	0402 1%
9,38,39,40	DDR4_CH1_A5	R5948	39	0402 1%
9,38,39,40	DDR4_CH1_A6	R5949	39	0402 1%
9,38,39,40	DDR4_CH1_A7	R5950	39	0402 1%
9,38,39,40	DDR4_CH1_A8	R5951	39	0402 1%
9,38,39,40	DDR4_CH1_A9	R5952	39	0402 1%
9,38,39,40	DDR4_CH1_A10	R5953	39	0402 1%
9,38,39,40	DDR4_CH1_A11	R5954	39	0402 1%
9,38,39,40	DDR4_CH1_A12	R5955	39	0402 1%
9,38,39,40	DDR4_CH1_A13	R5956	39	0402 1%
9,38,39,40	DDR4_CH1_A14	R5957	39	0402 1%
9,38,39,40	DDR4_CH1_A15	R5958	39	0402 1%
9,38,39,40	DDR4_CH1_A16	R5959	39	0402 1%
9,38,39,40	DDR4_CH1_BA0	R5960	39	0402 1%
9,38,39,40	DDR4_CH1_BA1	R5961	39	0402 1%
9,38,39,40	DDR4_CH1_CSn	R5962	39	0402 1%
9,38,39,40	DDR4_CH1_ACTn	R5963	39	0402 1%
9,38,39,40	DDR4_CH1_ODT	R5964	39	0402 1%
9,38,39,40	DDR4_CH1_PAR	R5965	39	0402 1%
9,38,39,40	DDR4_CH1_BG0	R5966	39	0402 1%
9,38,39,40	DDR4_CH1_BG1	R5967	39	0402 1%
9,38,39,40	DDR4_CH1_CKE	R5968	39	0402 1%

S10_1V2OUT_CH11

9,38,39,40	DDR4_CH1_RESETn	R5969 1K 0402 1%
		R5970 1.00K, DNI 0402 1%

2V5_DDR4_CH11

9,38,39,40	DDR4_CH1_CKp	R5971 36.5 Ohm 0402 1%
9,38,39,40	DDR4_CH1_CKn	R5972 36.5 Ohm 0402 1%

C2304 10nF 0402 50V X7R

0V6_DDR4_VTT_CH11 S10_1V2OUT_CH11

C2234	0.1uF 0402 25V X7R
C2238	0.1uF 0402 25V X7R
C2242	0.1uF 0402 25V X7R
C2245	0.1uF 0402 25V X7R
C2248	0.1uF 0402 25V X7R
C2252	0.1uF 0402 25V X7R
C2256	0.1uF 0402 25V X7R
C2260	0.1uF 0402 25V X7R
C2263	0.1uF 0402 25V X7R
C2266	0.1uF 0402 25V X7R

2V5_DDR4_CH11

C2276	0.1uF 0402 25V X7R
C2279	0.1uF 0402 25V X7R
C2282	0.1uF 0402 25V X7R
C2284	0.1uF 0402 25V X7R
C2286	0.1uF 0402 25V X7R
C2288	0.1uF 0402 25V X7R
C2290	0.1uF 0402 25V X7R
C2292	0.1uF 0402 25V X7R
C2294	0.1uF 0402 25V X7R
C2296	0.1uF 0402 25V X7R

2V5_DDR4_CH11

C1647 4.7uF

S10_1V2OUT_CH11

C2235	0.1uF 0402 25V X7R
C2239	0.1uF 0402 25V X7R
C2243	0.1uF 0402 25V X7R
C2246	0.1uF 0402 25V X7R
C2249	0.1uF 0402 25V X7R
C2253	0.1uF 0402 25V X7R
C2257	0.1uF 0402 25V X7R
C2261	0.1uF 0402 25V X7R
C2264	0.1uF 0402 25V X7R
C2267	0.1uF 0402 25V X7R
C2270	0.1uF 0402 25V X7R
C2273	0.1uF 0402 25V X7R
C2277	0.1uF 0402 25V X7R
C2280	0.1uF 0402 25V X7R
C2283	0.1uF 0402 25V X7R
C2285	0.1uF 0402 25V X7R
C2287	0.1uF 0402 25V X7R
C2289	0.1uF 0402 25V X7R
C2291	0.1uF 0402 25V X7R
C2293	0.1uF 0402 25V X7R
C2295	0.1uF 0402 25V X7R
C2297	0.1uF 0402 25V X7R
C2298	0.1uF 0402 25V X7R
C2299	0.1uF 0402 25V X7R
C2301	0.1uF 0402 25V X7R
C2302	0.1uF 0402 25V X7R
C2303	0.1uF 0402 25V X7R
C2305	0.1uF 0402 25V X7R

S10_1V2OUT_CH11

C2236	0.1uF 0402 25V X7R
C2240	0.1uF 0402 25V X7R
C2244	0.1uF 0402 25V X7R
C2247	0.1uF 0402 25V X7R
C2250	0.1uF 0402 25V X7R
C2254	0.1uF 0402 25V X7R
C2258	0.1uF 0402 25V X7R
C2262	0.1uF 0402 25V X7R
C2265	0.1uF 0402 25V X7R
C2268	0.1uF 0402 25V X7R
C2271	0.1uF 0402 25V X7R
C2274	0.1uF 0402 25V X7R

S10_1V2OUT_CH11

C2237	4.7uF 0402 6.3V X5R
C2241	4.7uF 0402 6.3V X5R

0V6_DDR4_VTT_CH11 S10_1V2OUT_CH11

C2251	0.1uF 0402 25V X7R
C2255	0.1uF 0402 25V X7R
C2259	0.1uF 0402 25V X7R

0V6_DDR4_VREF_CH11 S10_1V2OUT_CH11

C2269	0.1uF 0402 25V X7R
C2272	0.1uF 0402 25V X7R
C2275	0.1uF 0402 25V X7R
C2278	0.1uF 0402 25V X7R
C2281	0.1uF 0402 25V X7R

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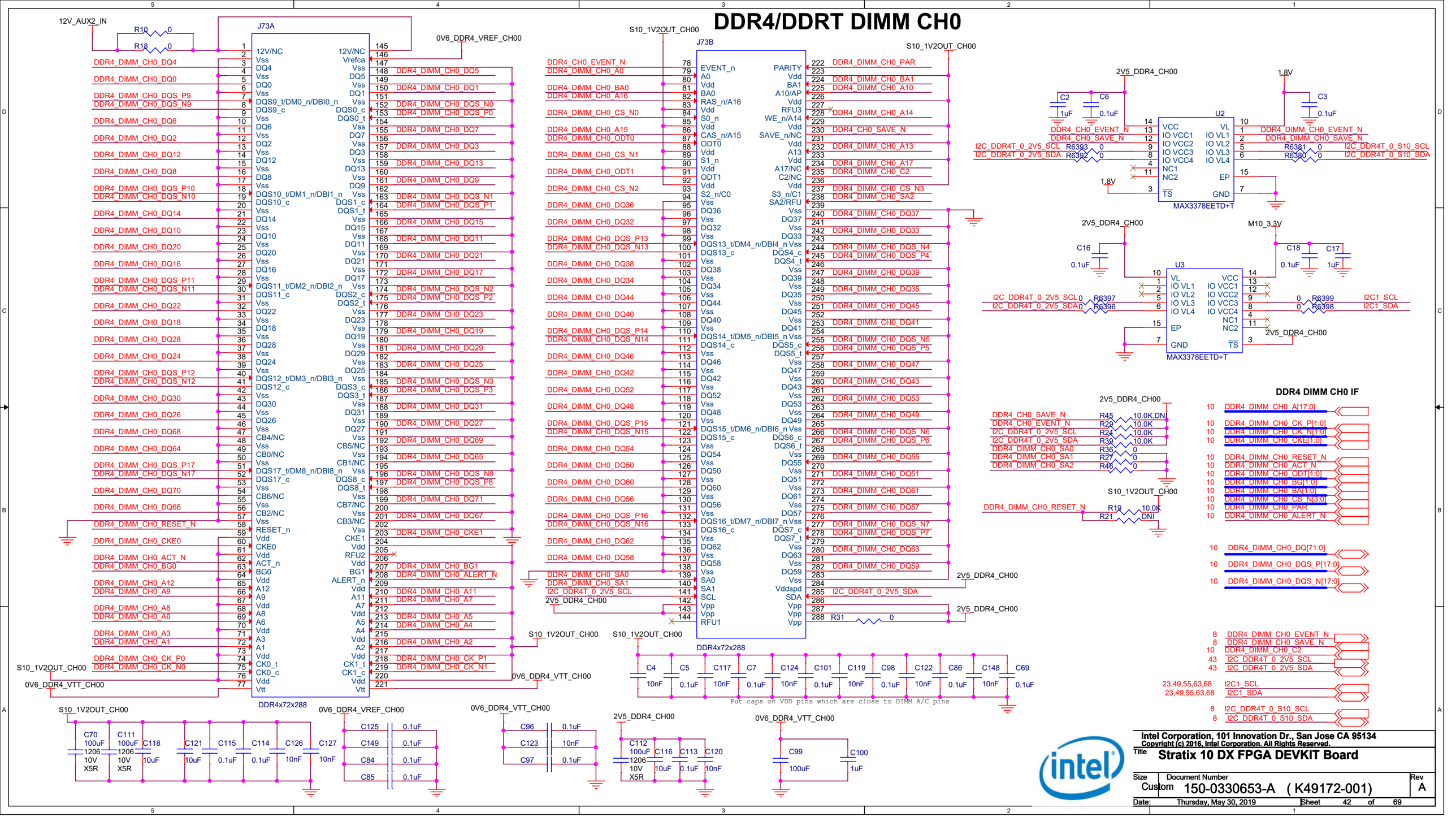
DDR4/DDRT DIMM CH0



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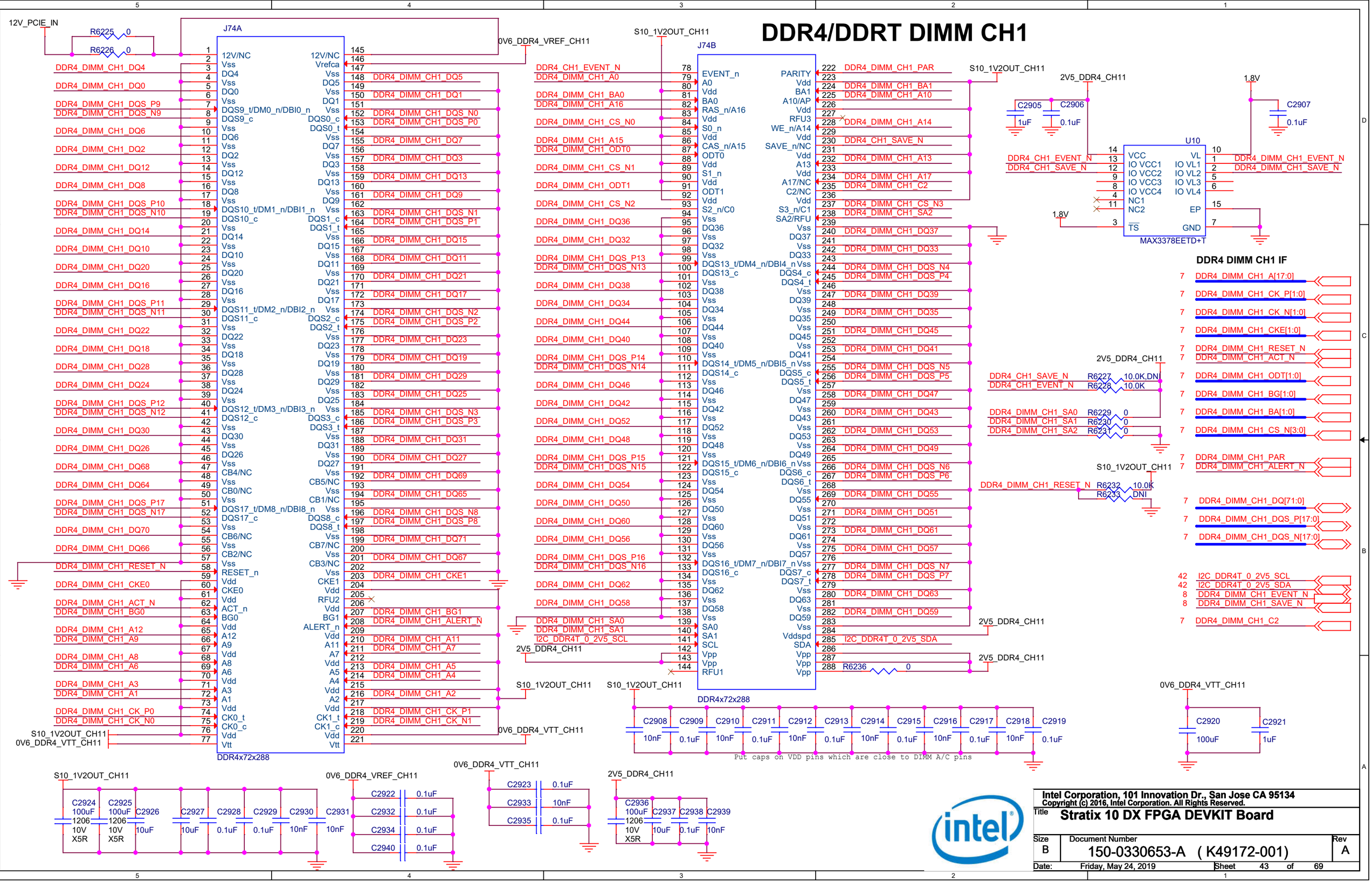
DDR4/DDRT DIMM CH1



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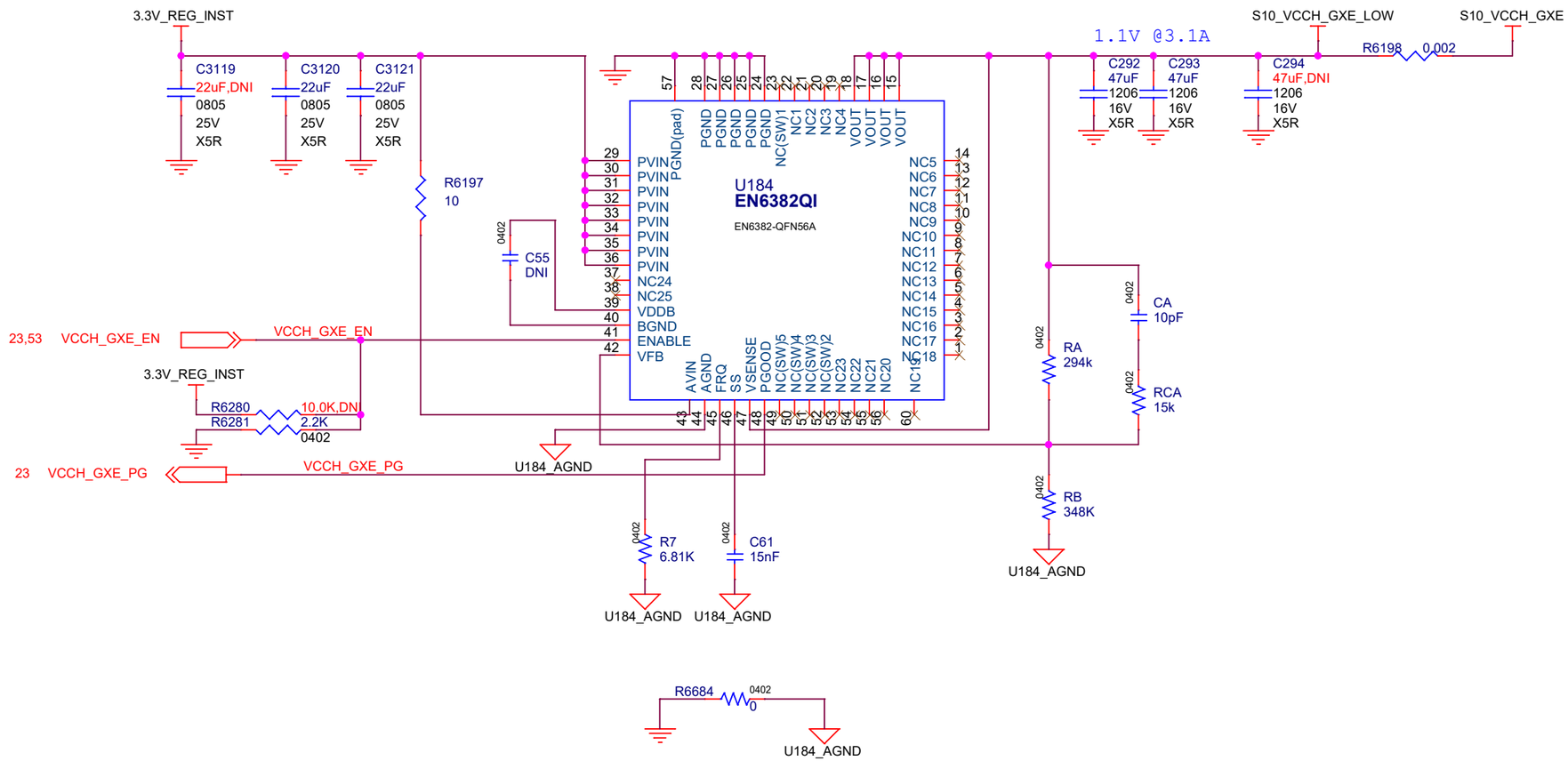
Power S10_VCCH_GXE



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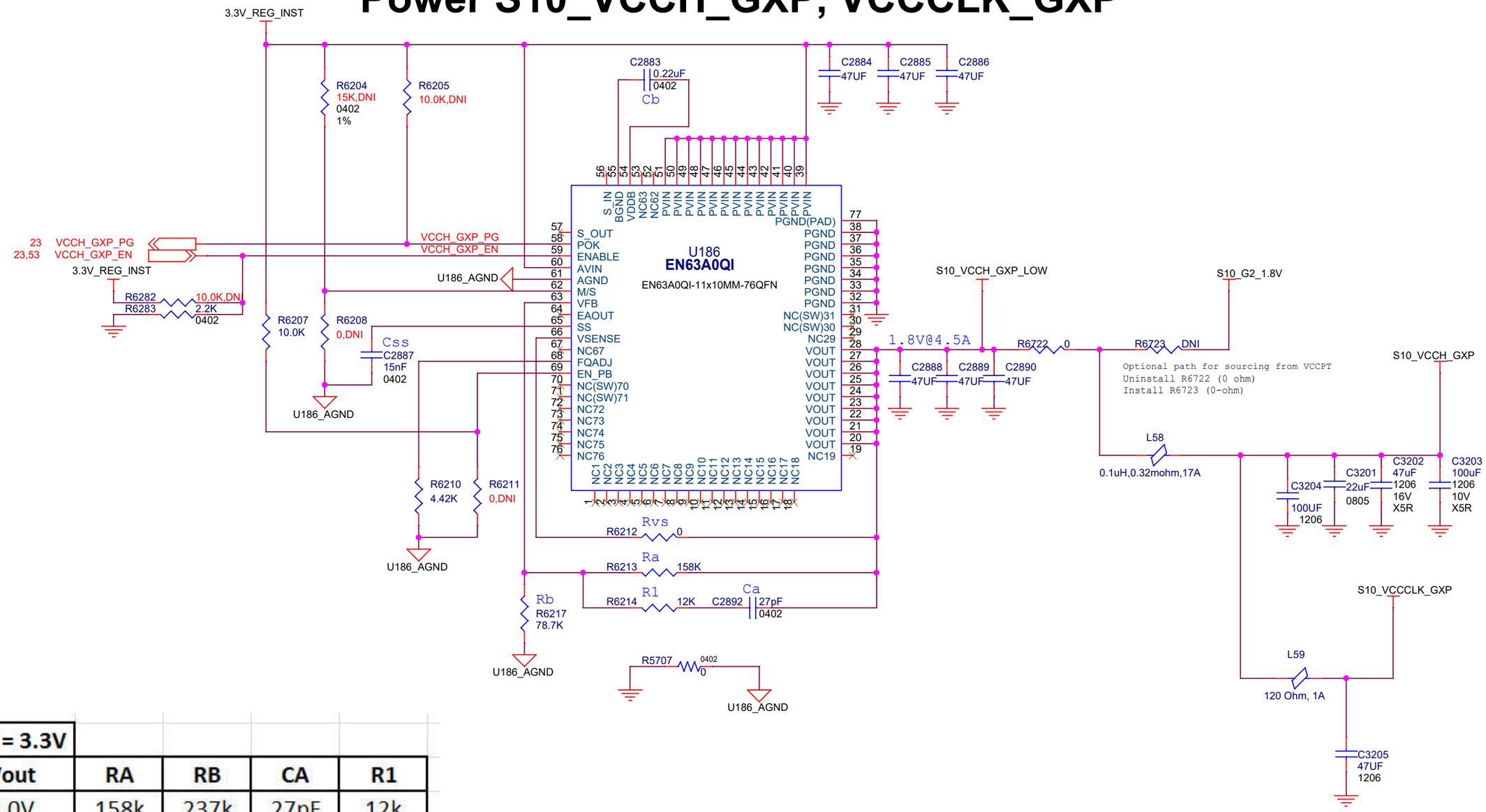
Power S10_VCCH_GXP, VCCCLK_GXP



VIN = 3.3V				
Vout	RA	RB	CA	R1
1.0V	158k	237k	27pF	12k
1.2V	158k	158k	27pF	12k
1.5V	158k	105k	27pF	12k
1.8V	158k	78.7K	27pF	12k
2.5V	158k	49.9K	27pF	12k

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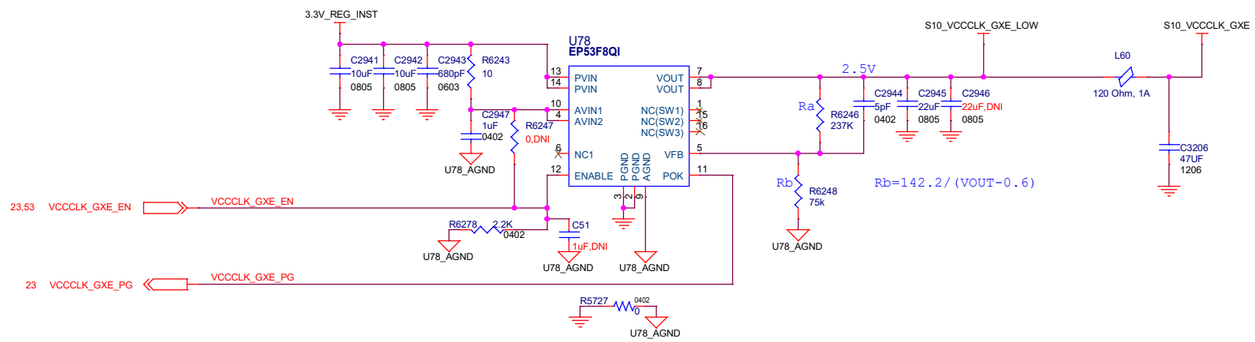
Power - S10_VCCCLK_GXE



V_{FB} = 0.6V, R_A (R2) = 237k

$$R_B = \frac{V_{FB} \times R_A}{V_{OUT} - V_{FB}}$$

VOUT	RA (R2)	RB (R4)
1.0V	237k	357k
1.2V	237k	237k
1.5V	237k	158k
1.8V	237k	118k
2.5V	237k	75k
3.3V	237k	52.3k

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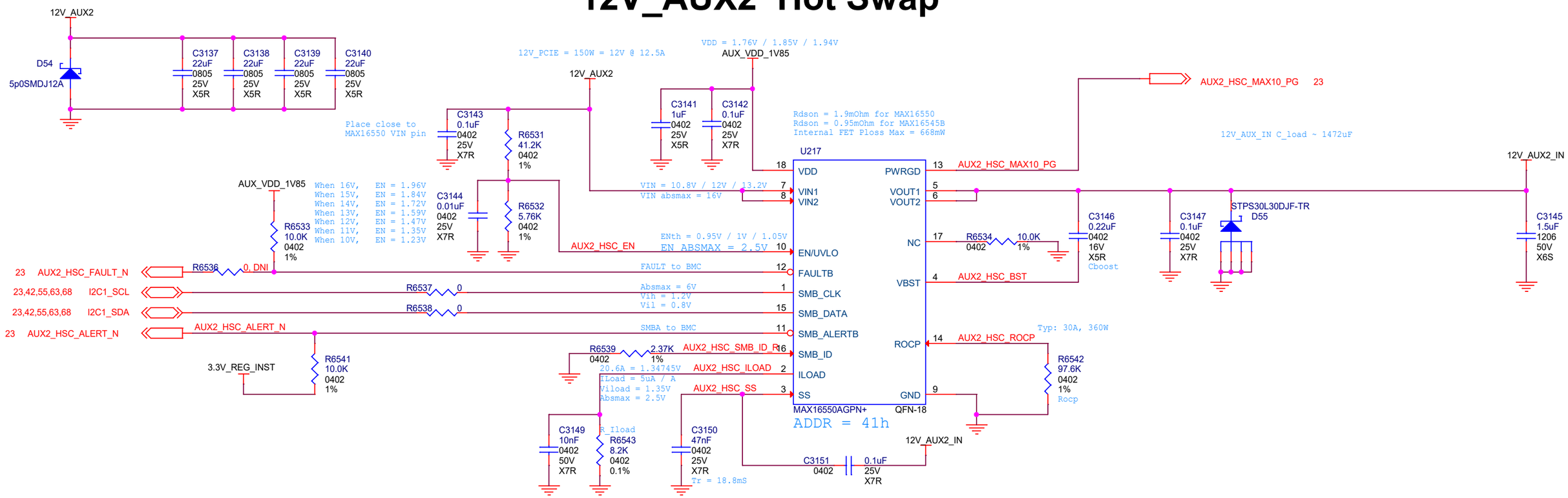
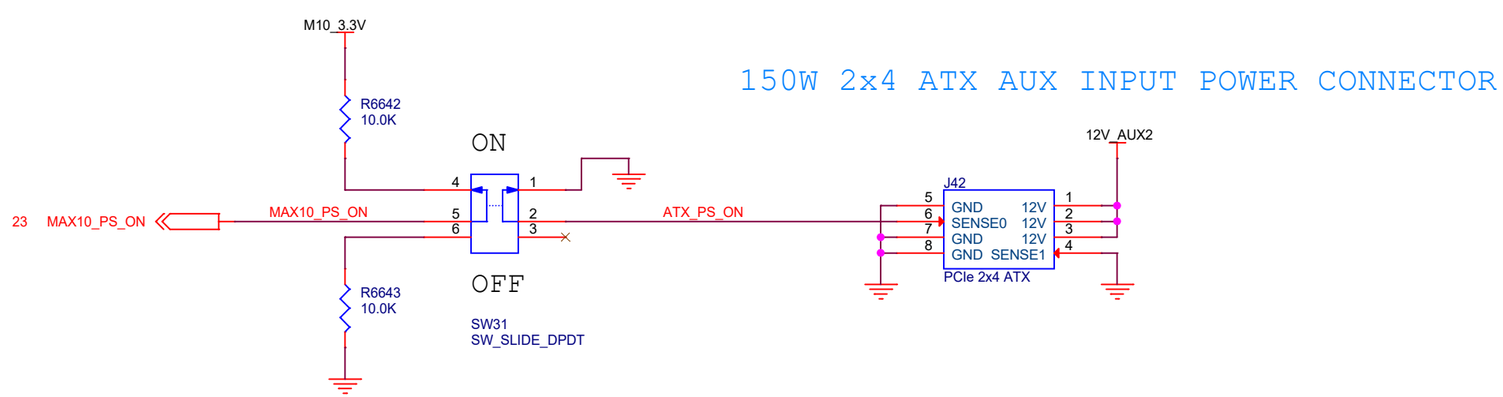
12V_AUX2 Hot Swap



Power On Switch
(For external power supply)



150W 2x4 ATX AUX INPUT POWER CONNECTOR

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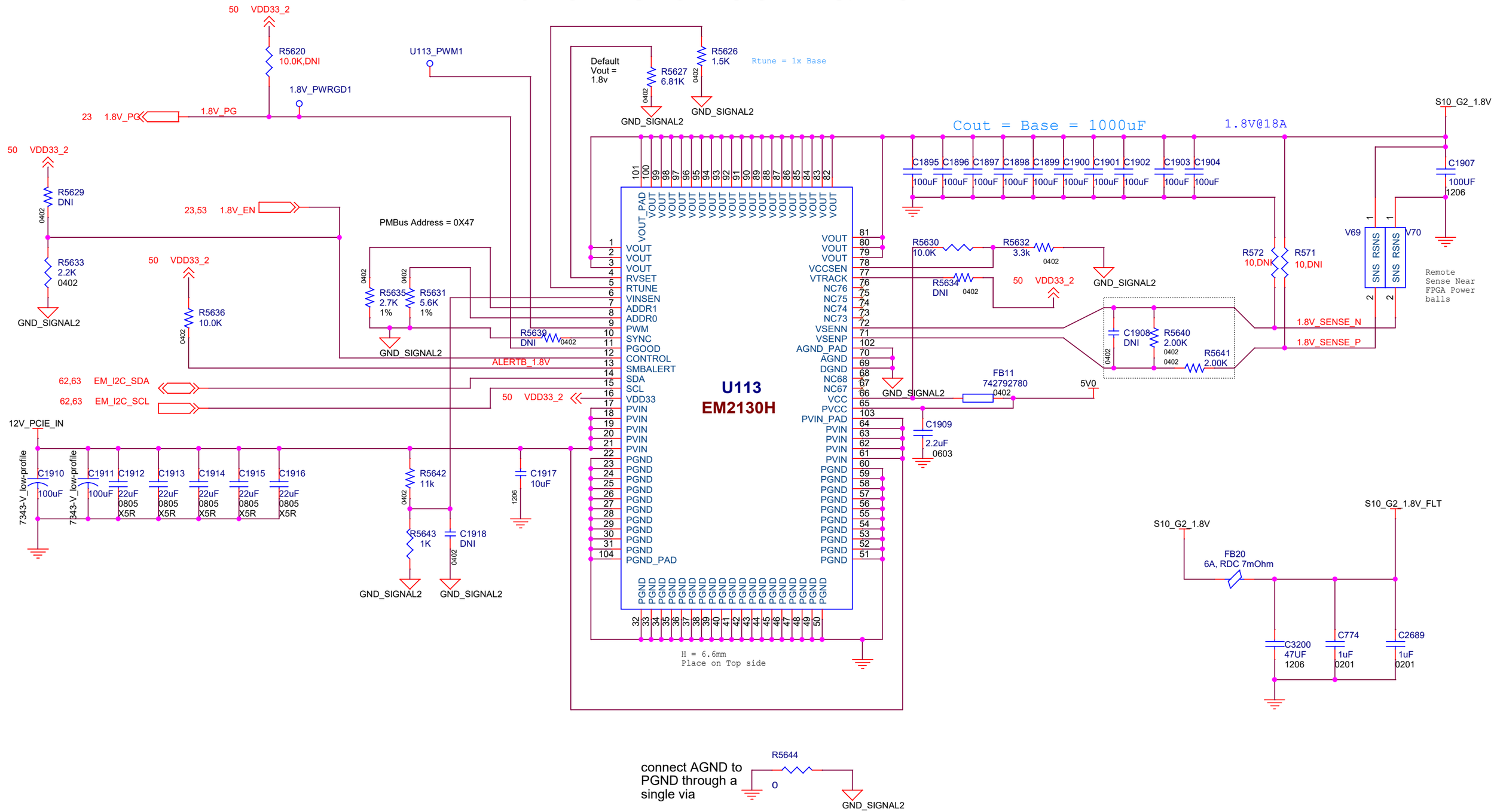
Power - S10 VCCPT & 1.8V



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Power S10_VCCIO_1V8

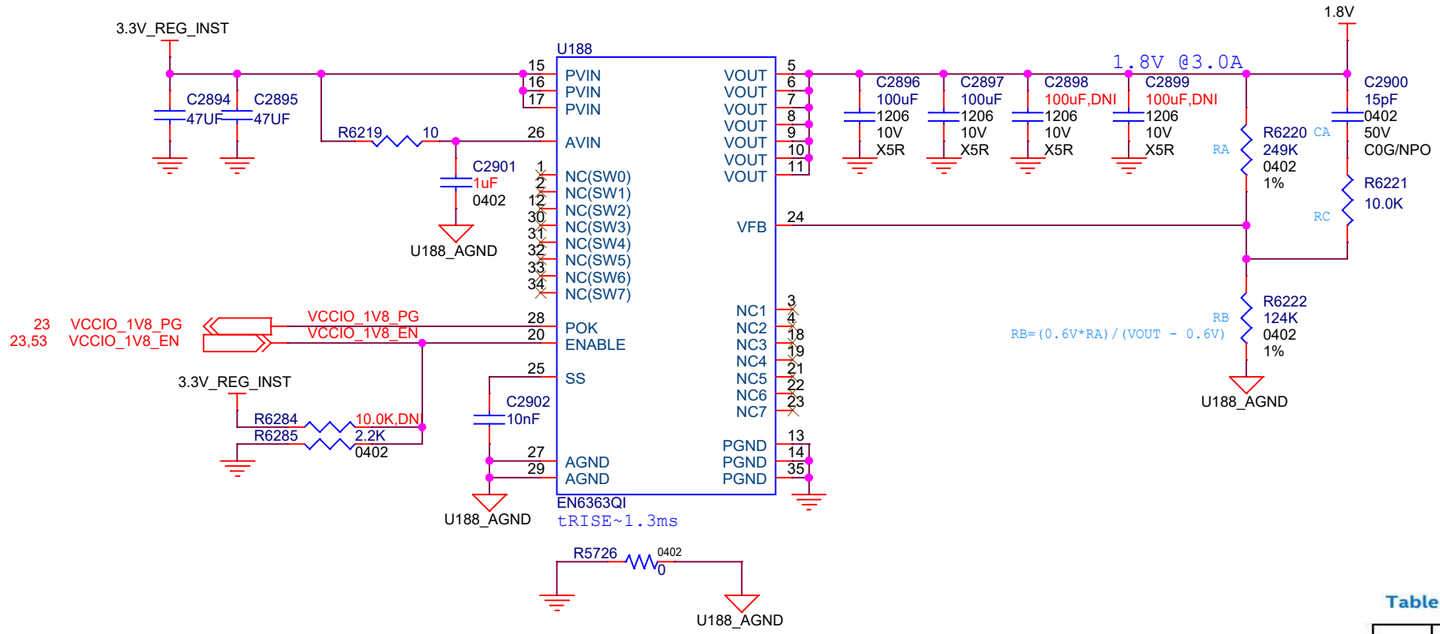

Table 1: External Compensation Recommendations

VIN	VOUT	RB	CA	RA	RC	COUT (0805)
3.3V	1.0V	374kΩ	18pF	249kΩ	10kΩ	2 x 100µF
	1.2V	249kΩ	15pF			
	1.5V	165kΩ	15pF			
	1.8V	124kΩ	15pF			
	2.5V	78.7kΩ	12pF			
5V	1.0V	374kΩ	15pF	249kΩ	10kΩ	2 x 100µF
	1.2V	249kΩ	15pF			
	1.5V	165kΩ	15pF			
	1.8V	124kΩ	12pF			
	2.5V	78.7kΩ	12pF			
	3.3V	54.9kΩ	10pF			

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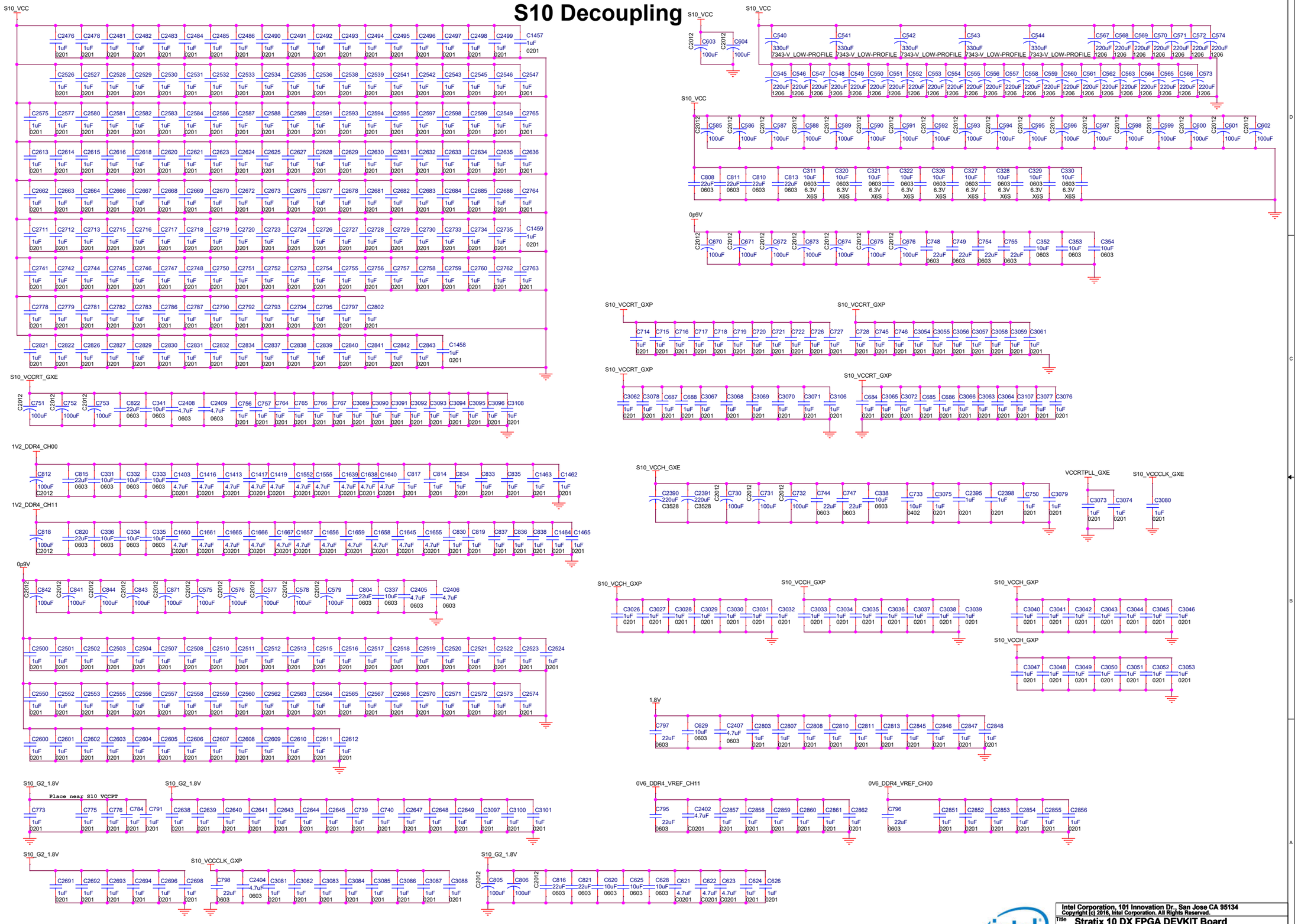
S10 Decoupling



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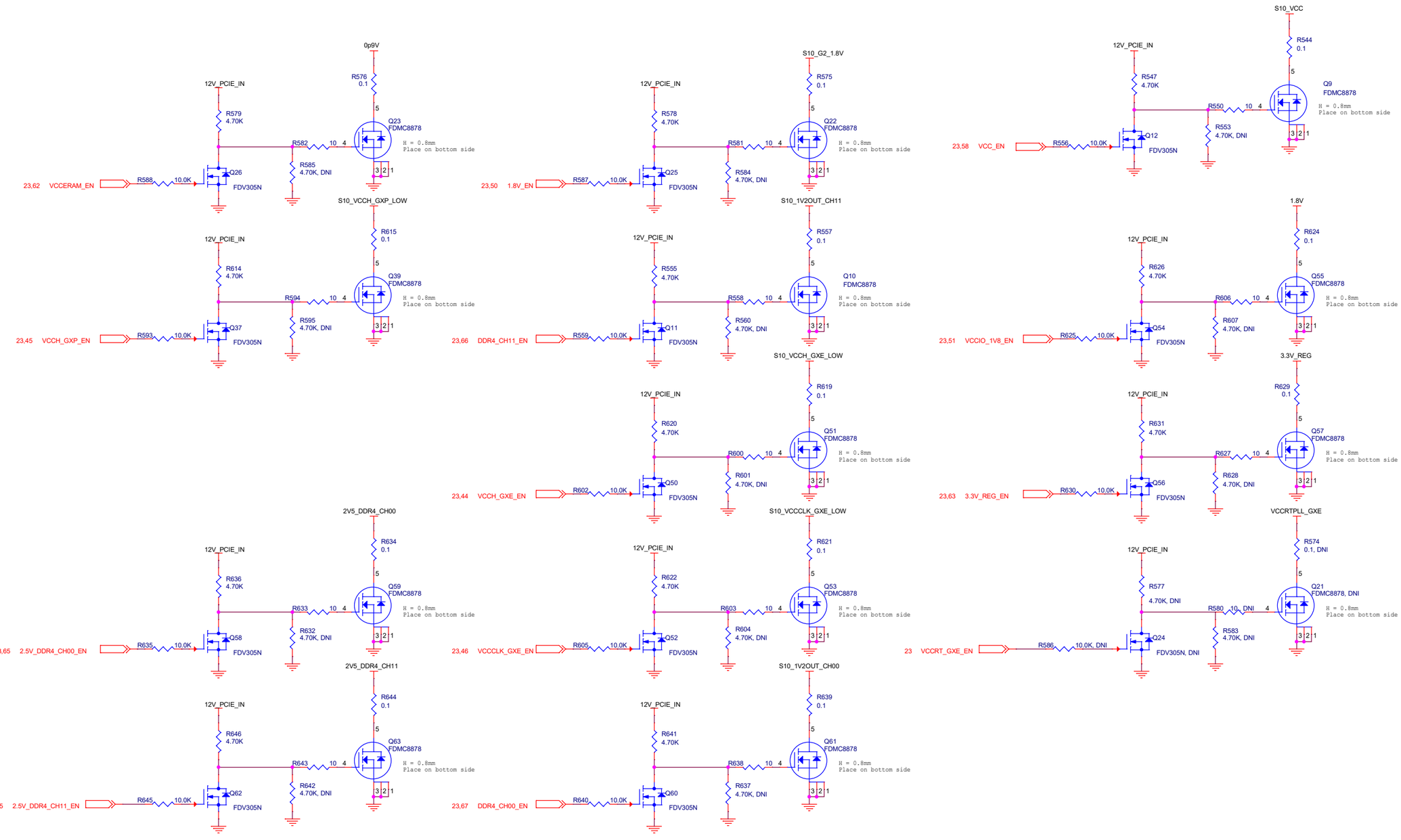
Fast Power-Down Discharge



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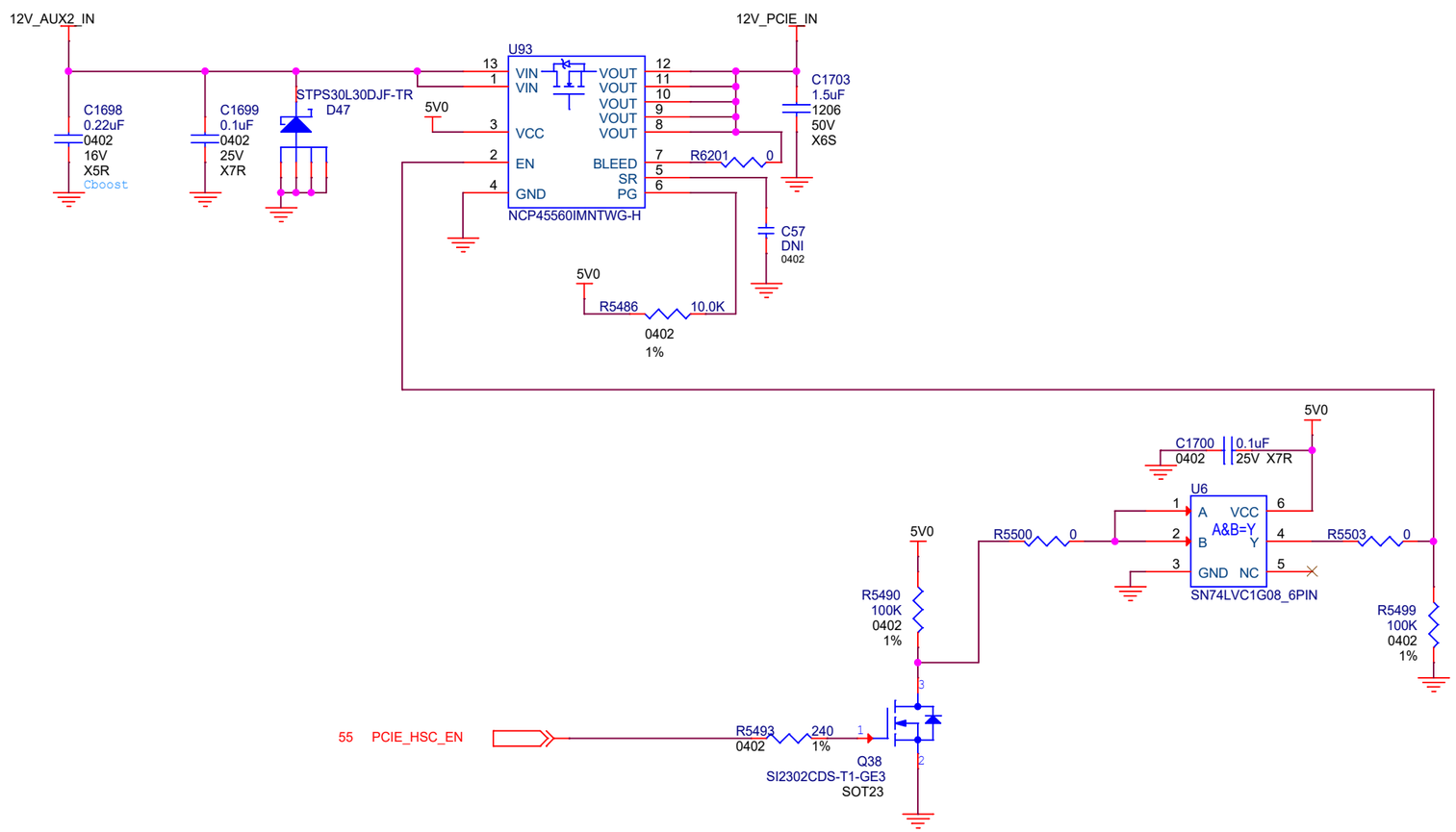
PCIE_12V to AUX_12V Power Bridge



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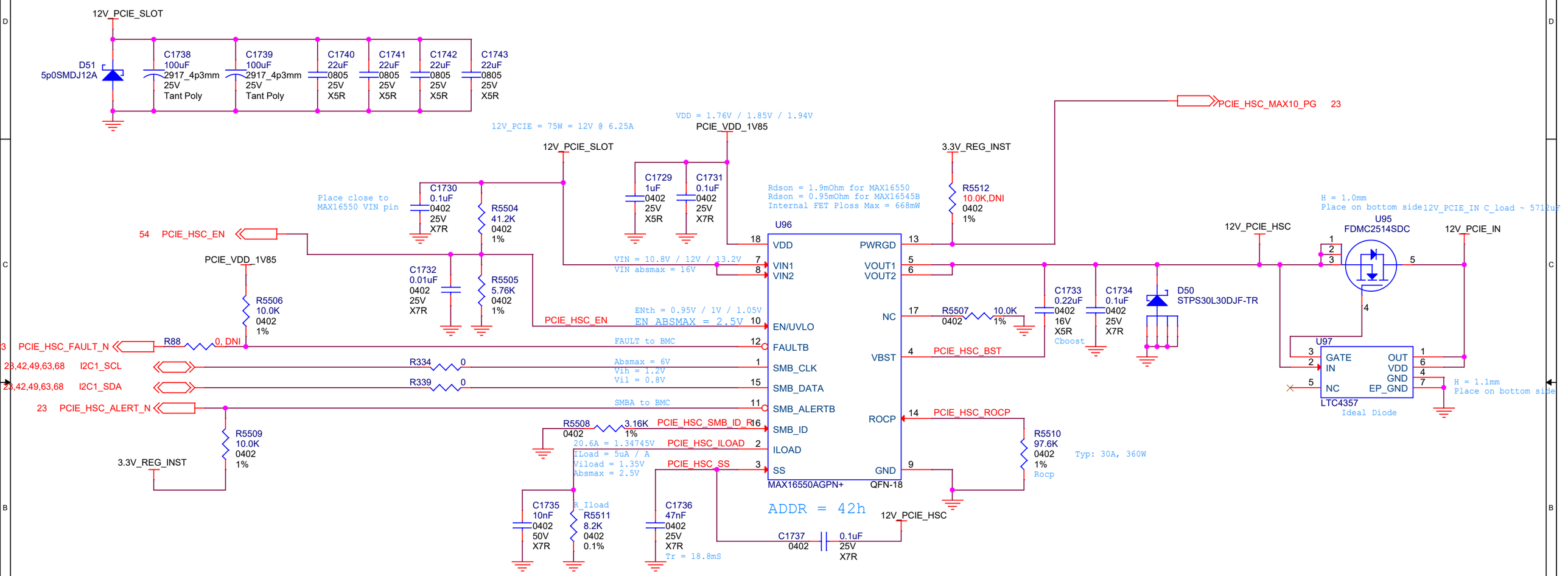
12V_PCIE Hotswap



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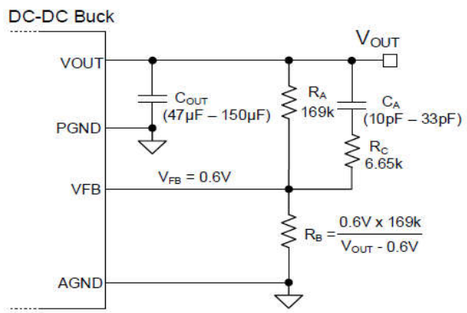
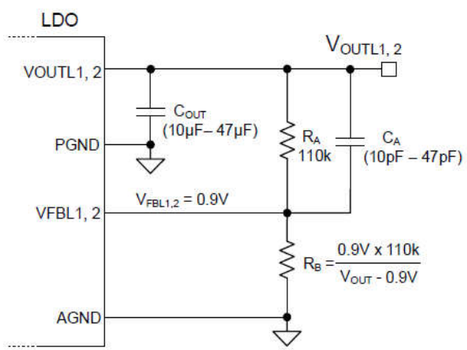
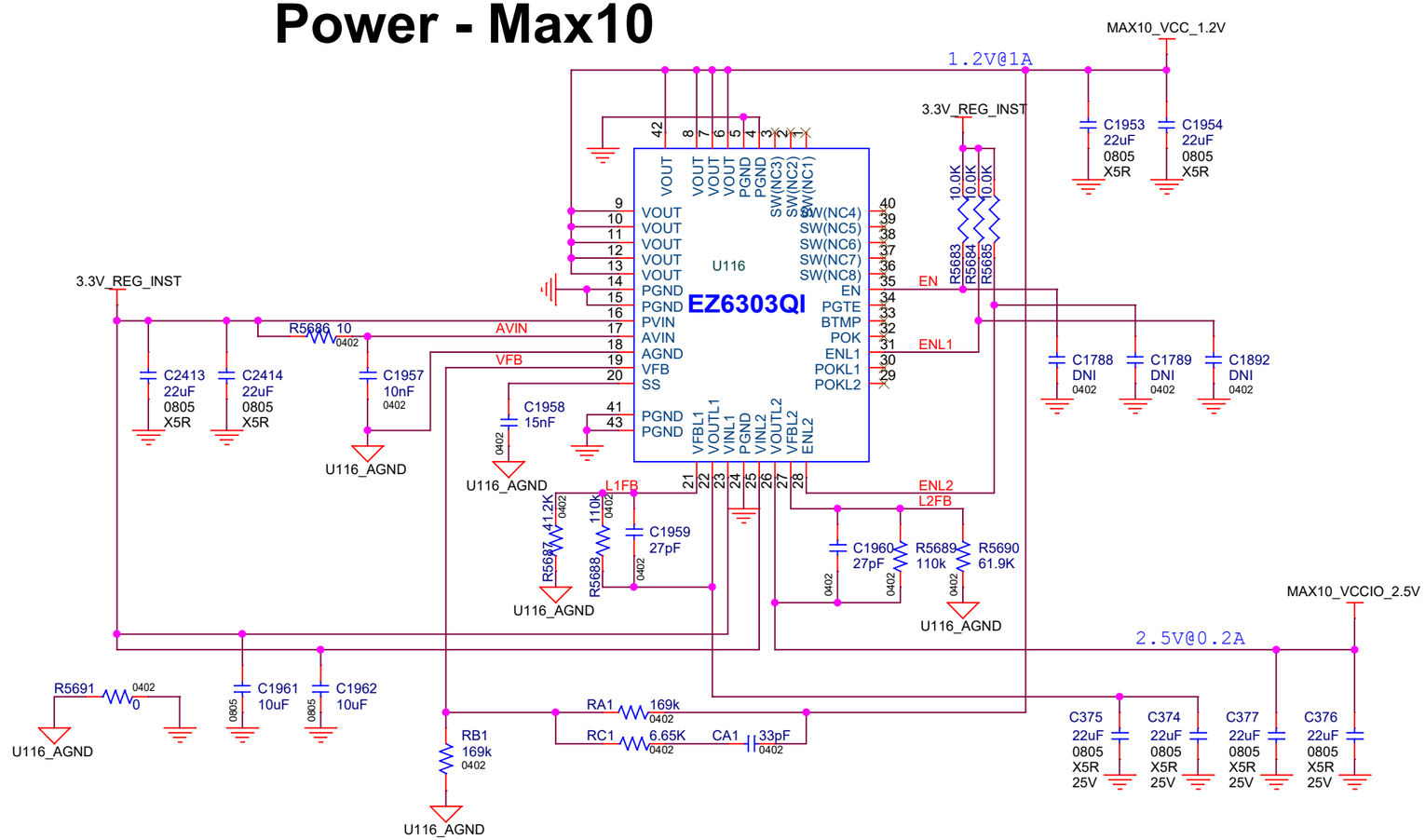
Power - Max10

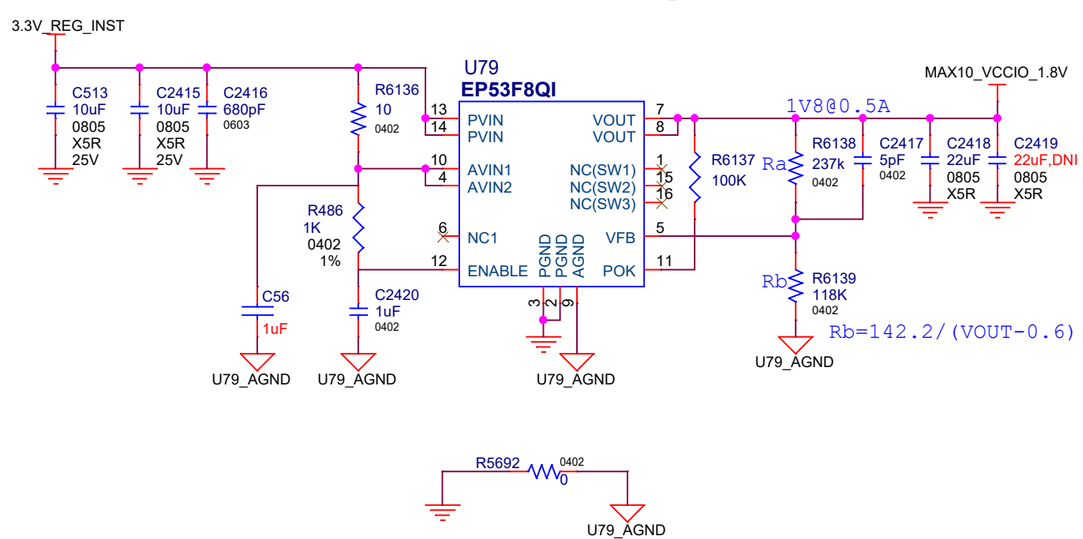
***VOUT CALCULATION**



***VOUTL1/2 CALCULATION**







V_{FB} = 0.6V, R_A (R2) = 237k

$$R_B = \frac{V_{FB} \times R_A}{V_{OUT} - V_{FB}}$$

VOUT	RA (R2)	RB (R4)
1.0V	237k	357k
1.2V	237k	237k
1.5V	237k	158k
1.8V	237k	118k
2.5V	237k	75k
3.3V	237k	52.3k

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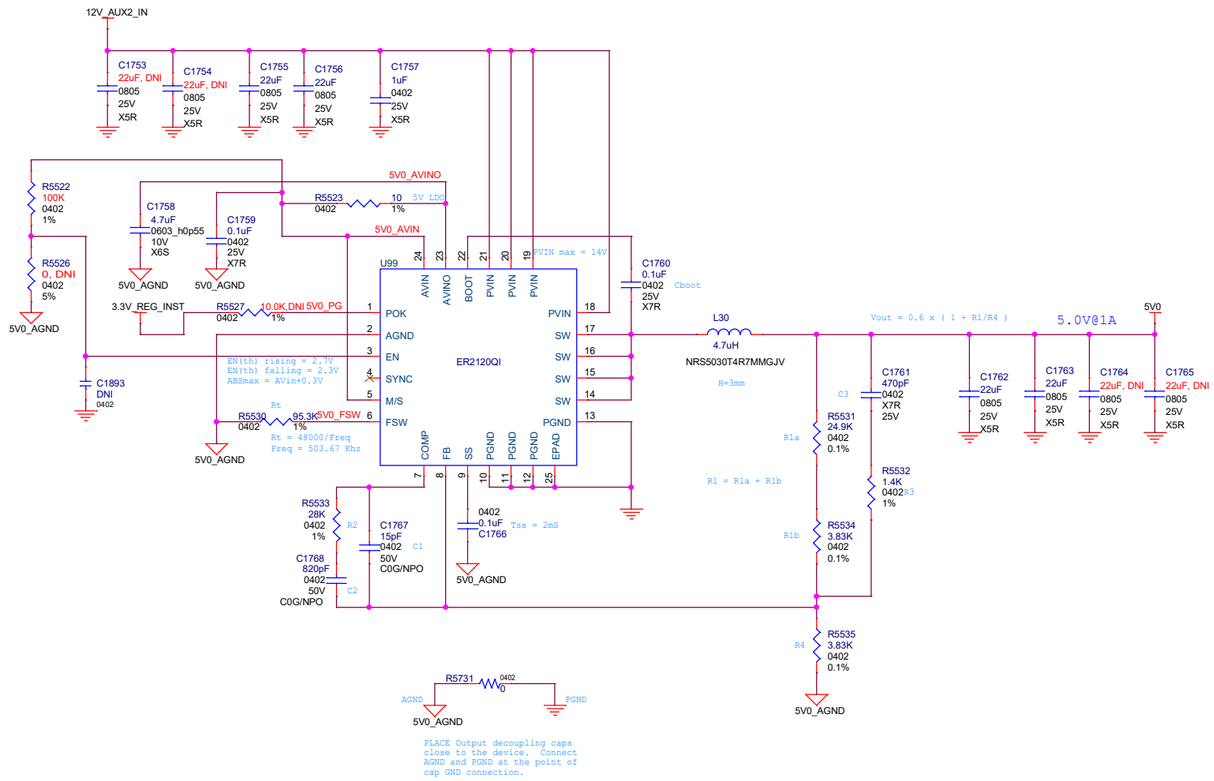
Power - 5V



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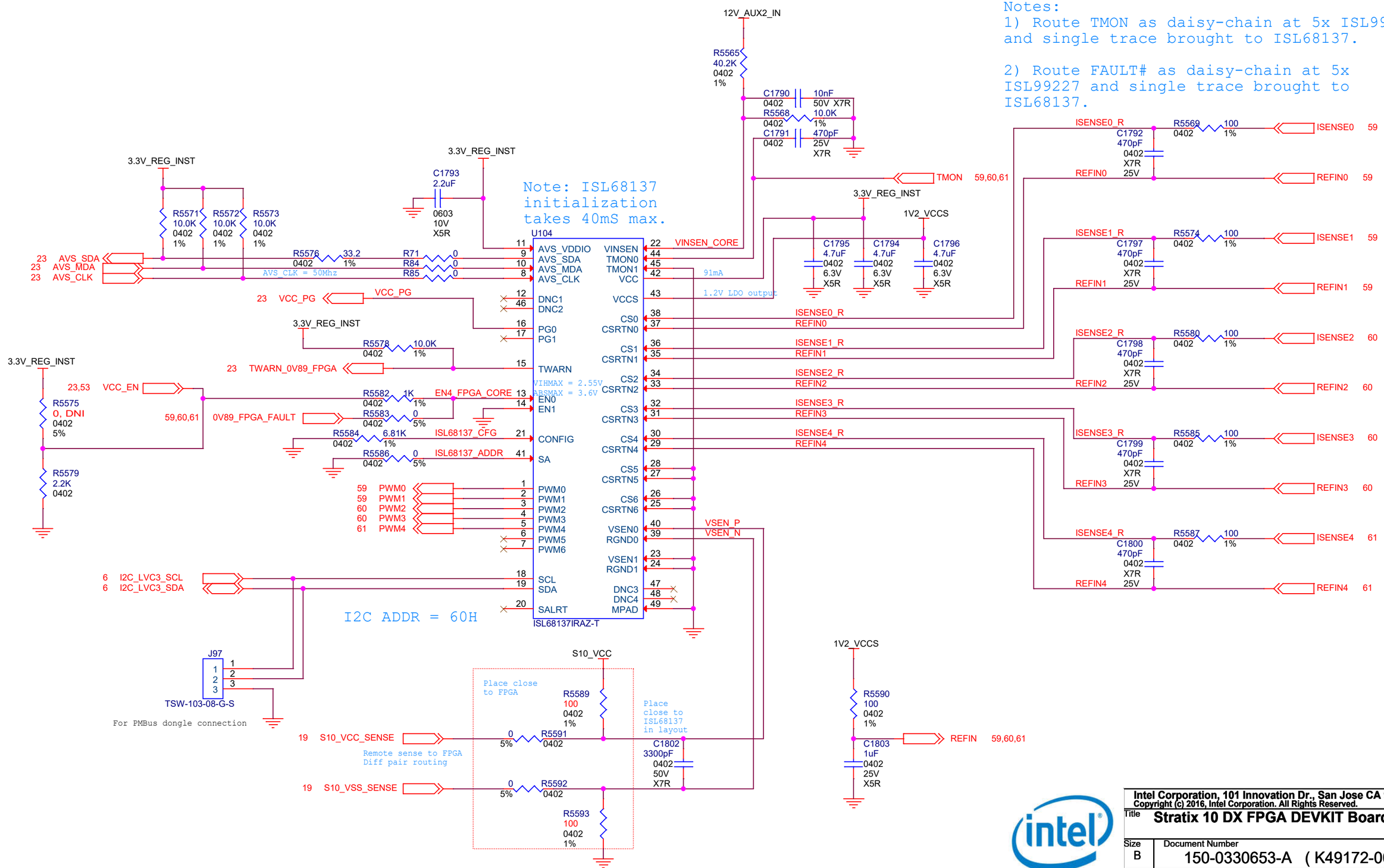
Power - VCCcore part1

Notes:
1) Route TMON as daisy-chain at 5x ISL99227 and single trace brought to ISL68137.

2) Route FAULT# as daisy-chain at 5x ISL99227 and single trace brought to ISL68137.

Note: ISL68137 initialization takes 40mS max.



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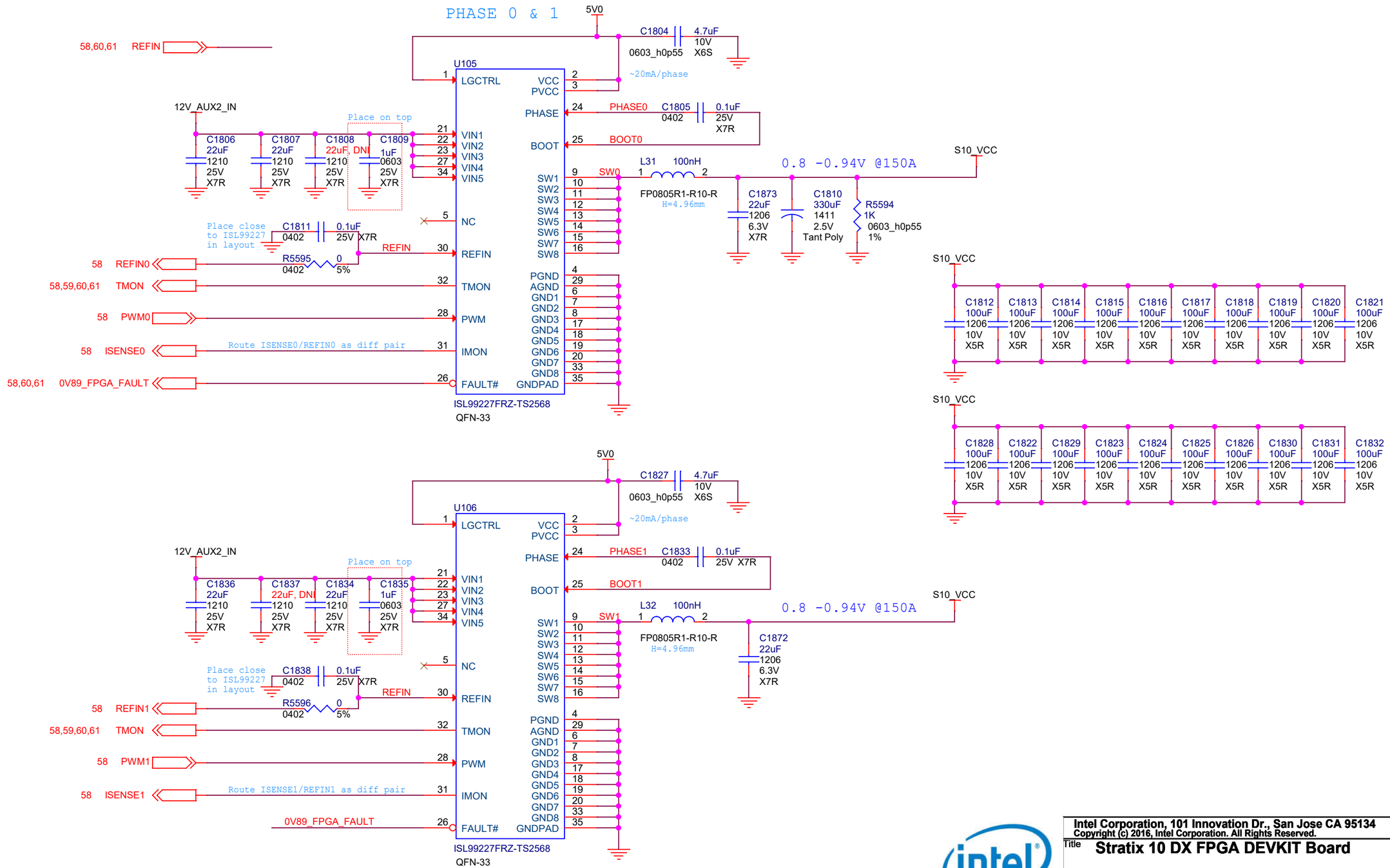
Power - VCCcore part2



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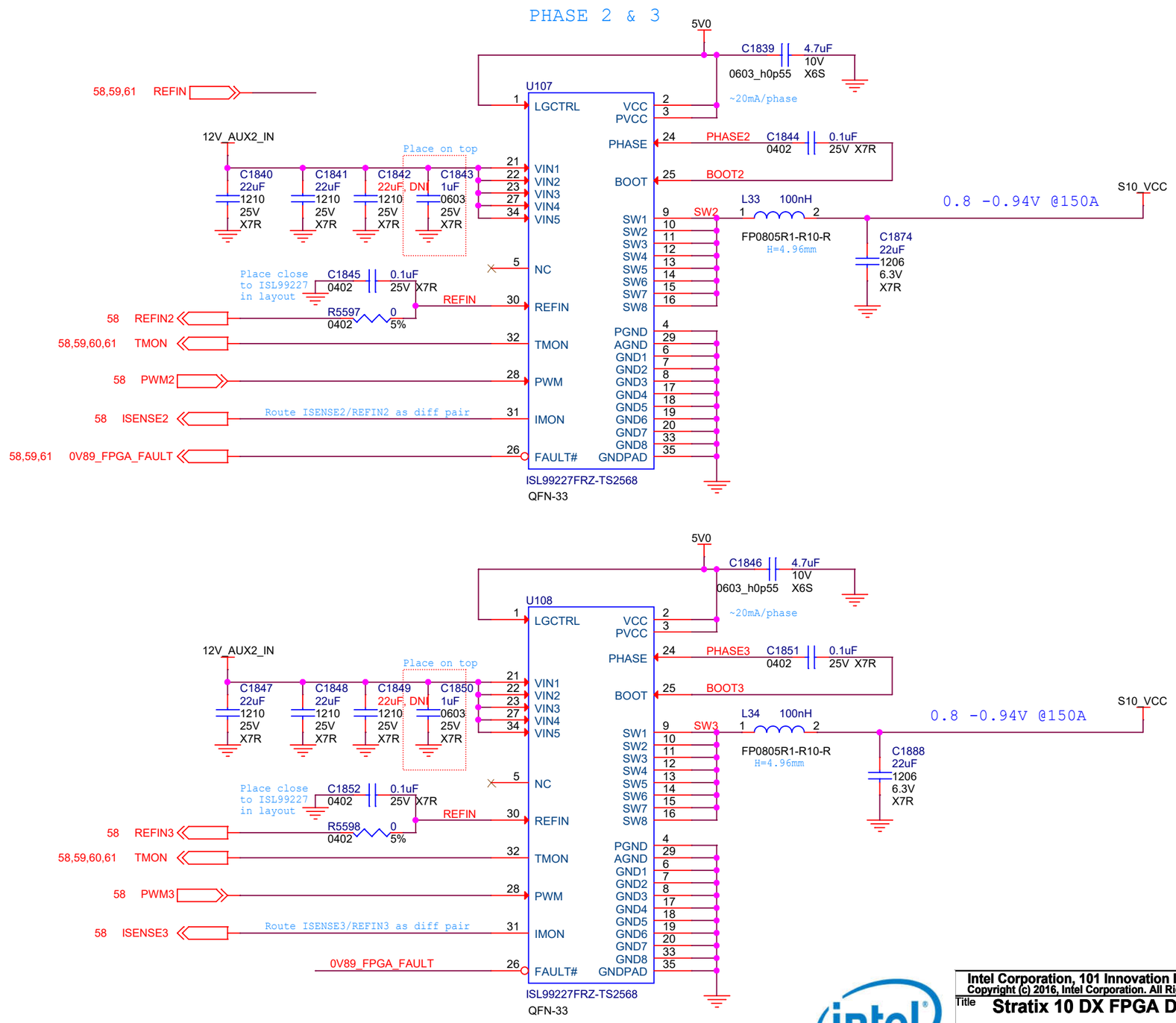
Power - VCCcore part3



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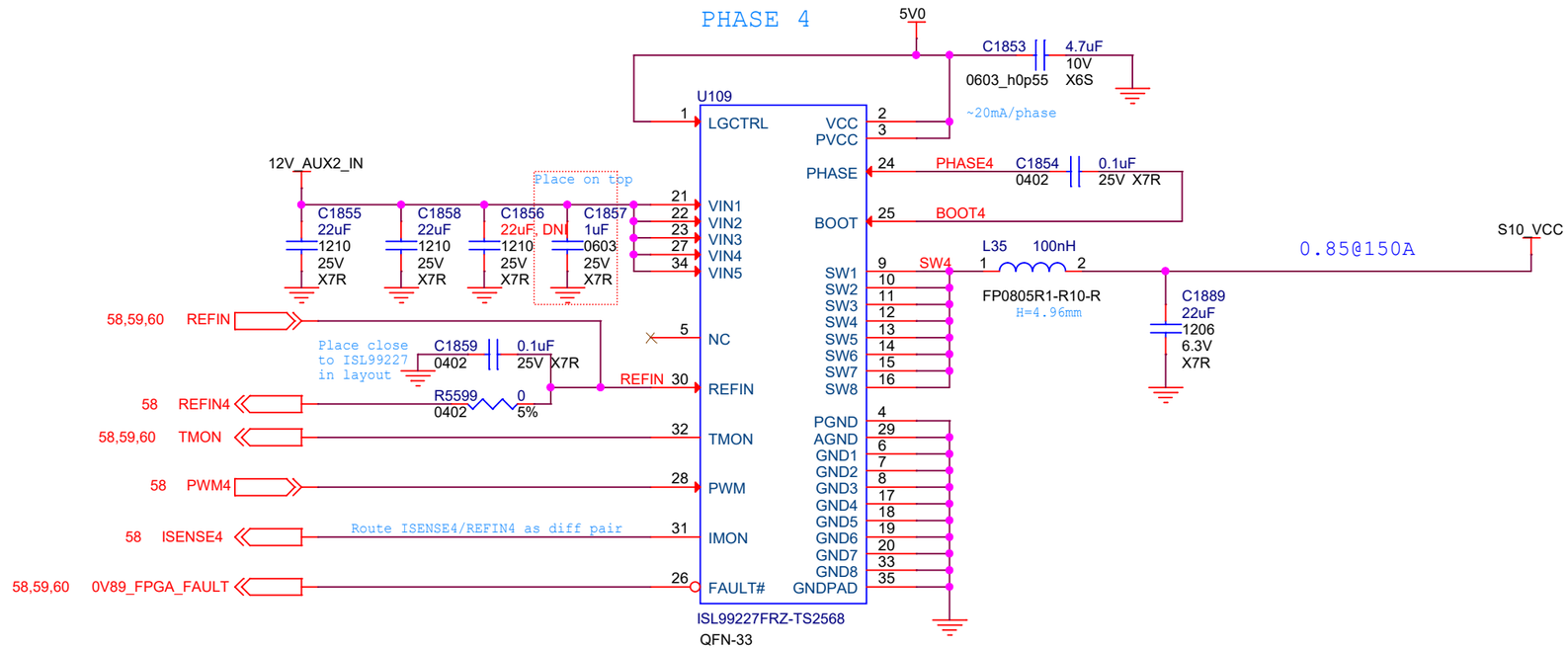
Power - VCCcore part4



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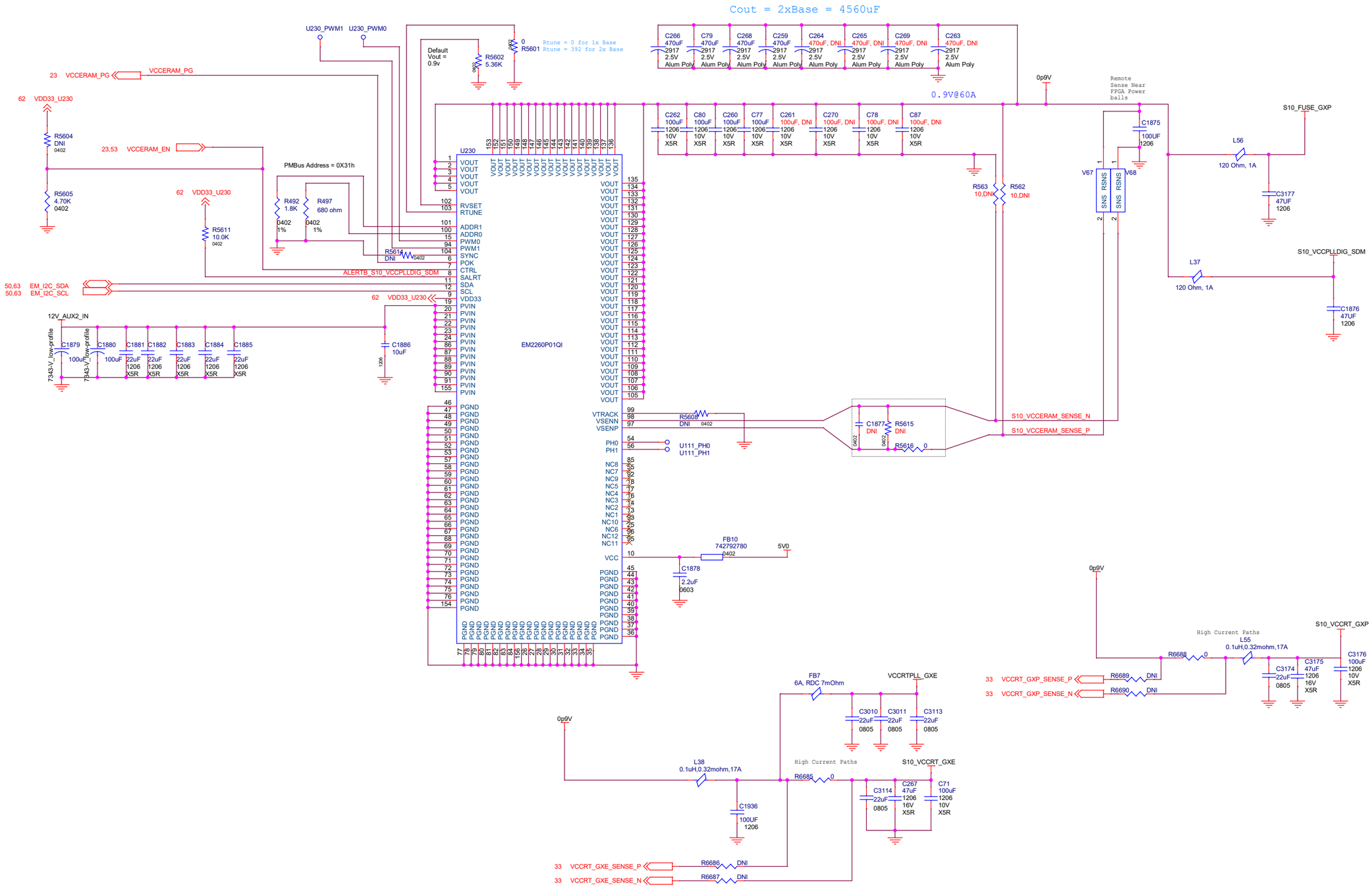
Power - VCCERAM, VCCRT_GXP, VCCRT_GXE
VCCPLLDIG_SDM, VCCRTPLL_GXE, VCCFUSE_GXP



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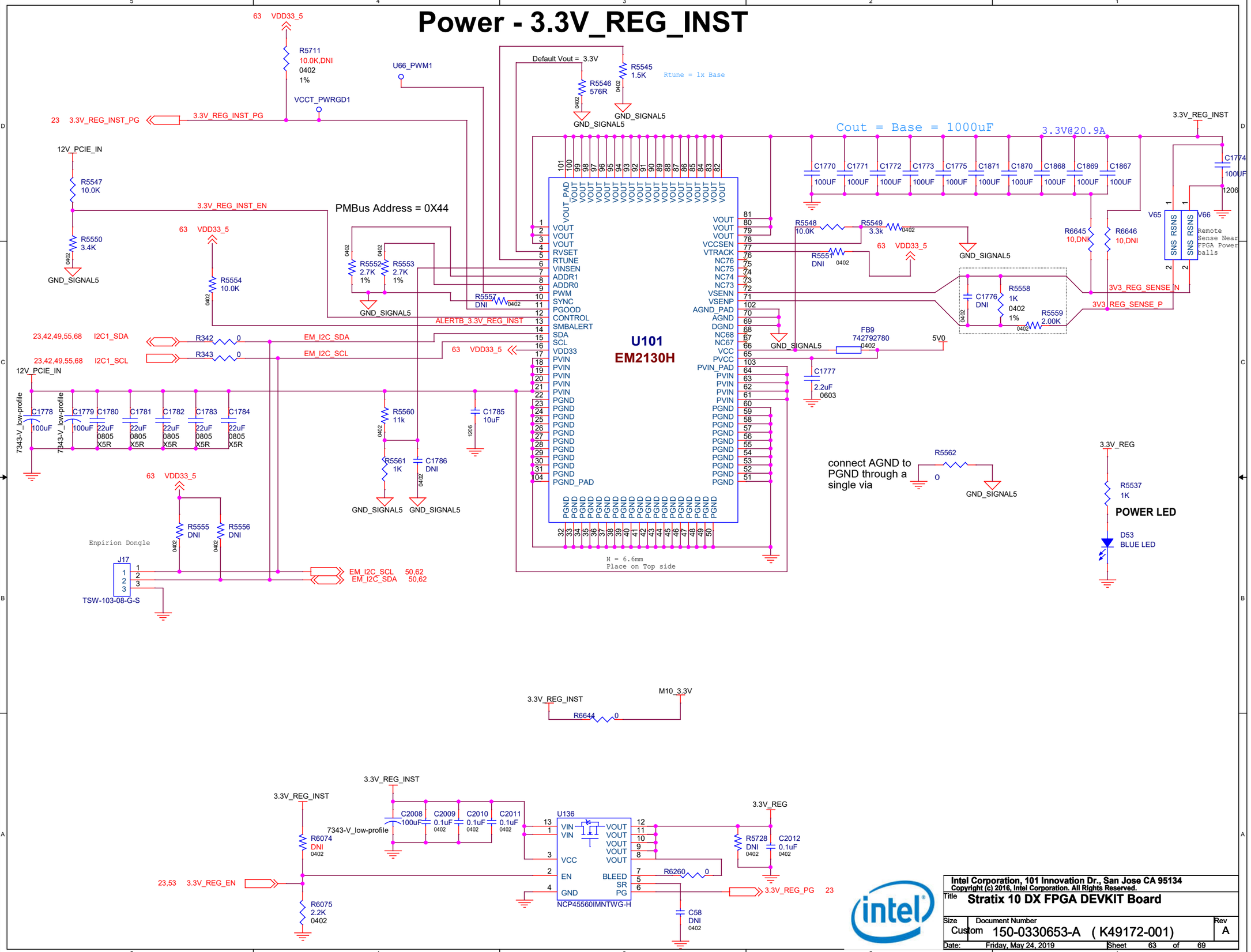
Power - 3.3V_REG_INST



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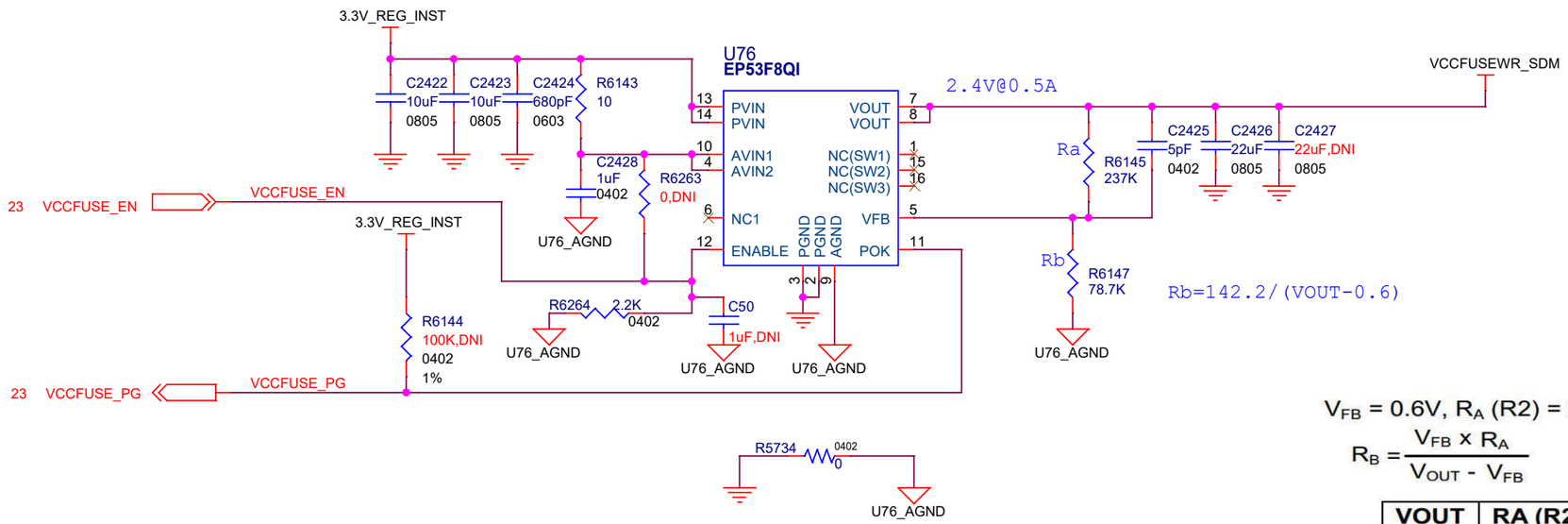
Power - 2.4V VCCFUSE_PWRGD



V_{FB} = 0.6V, R_A (R2) = 237k

$$R_B = \frac{V_{FB} \times R_A}{V_{OUT} - V_{FB}}$$

VOUT	RA (R2)	RB (R4)
1.0V	237k	357k
1.2V	237k	237k
1.5V	237k	158k
1.8V	237k	118k
2.5V	237k	75k
3.3V	237k	52.3k

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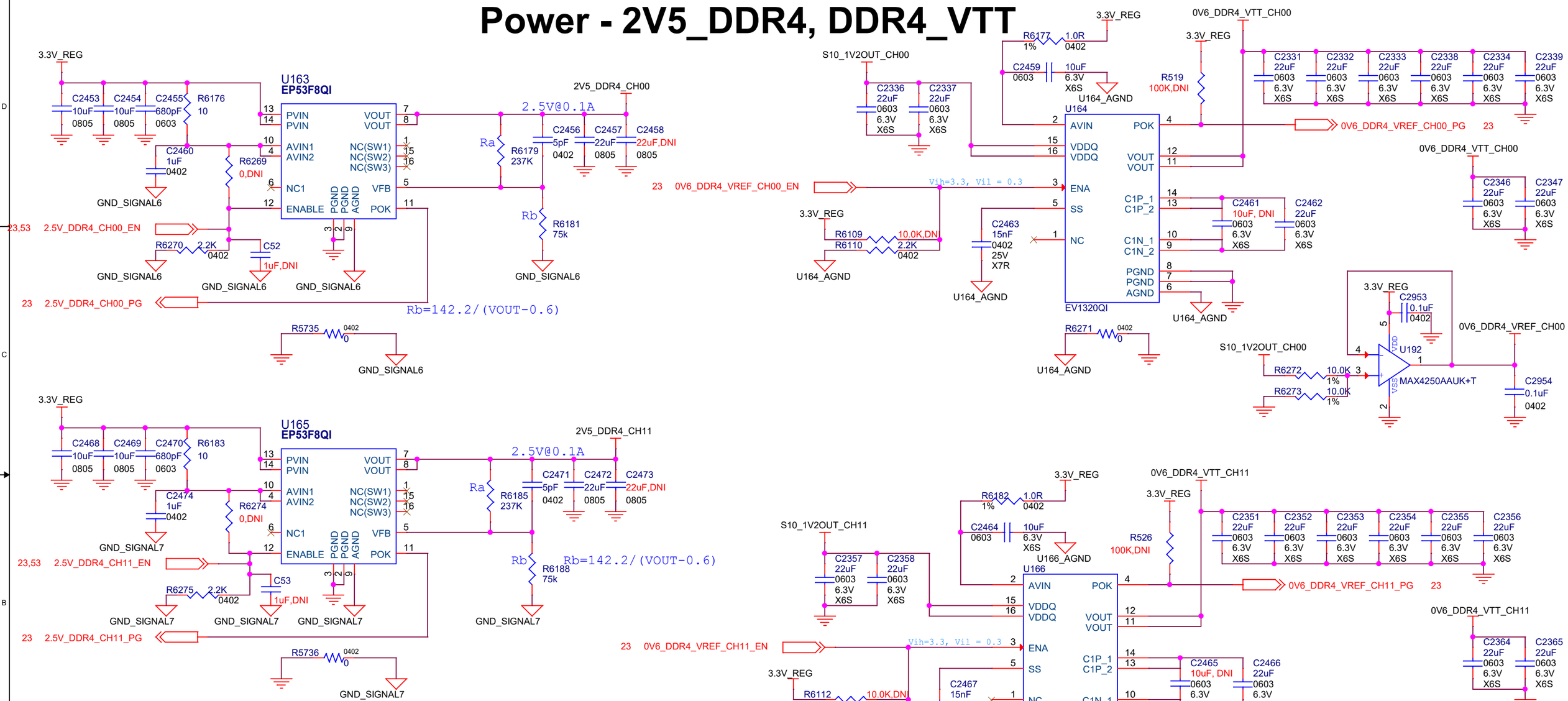
Power - 2V5_DDR4, DDR4_VTT



$$V_{FB} = 0.6V,\ R_A\ (R2) = 237k$$

$$R_B = \frac{V_{FB} \times R_A}{V_{OUT} - V_{FB}}$$

VOUT	RA (R2)	RB (R4)
1.0V	237k	357k
1.2V	237k	237k
1.5V	237k	158k
1.8V	237k	118k
2.5V	237k	75k
3.3V	237k	52.3k

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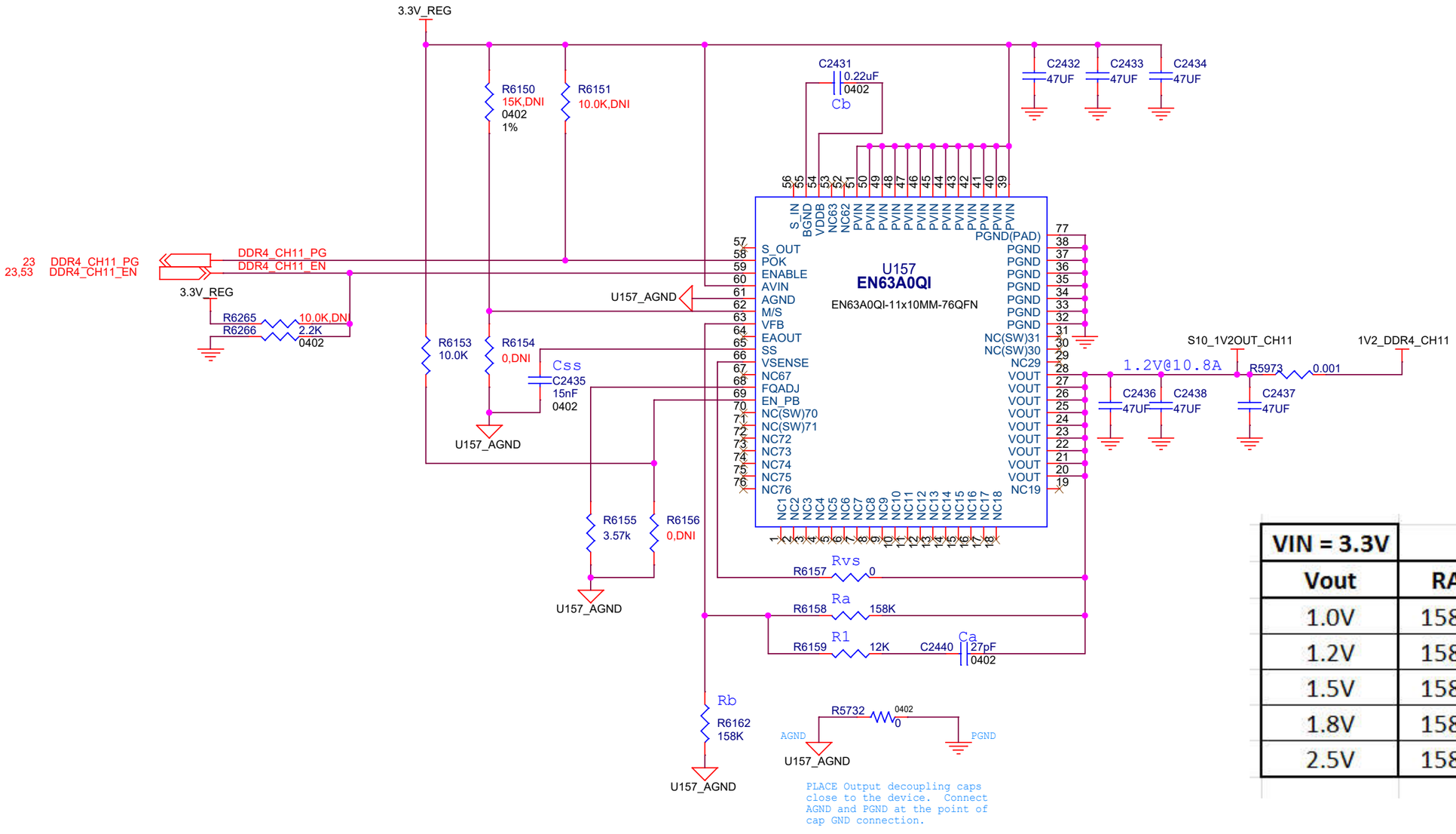
Power-1V2_DDR4_CH11



VIN = 3.3V				
Vout	RA	RB	CA	R1
1.0V	158k	237k	27pF	12k
1.2V	158k	158k	27pF	12k
1.5V	158k	105k	27pF	12k
1.8V	158k	78.7K	27pF	12k
2.5V	158k	49.9K	27pF	12k

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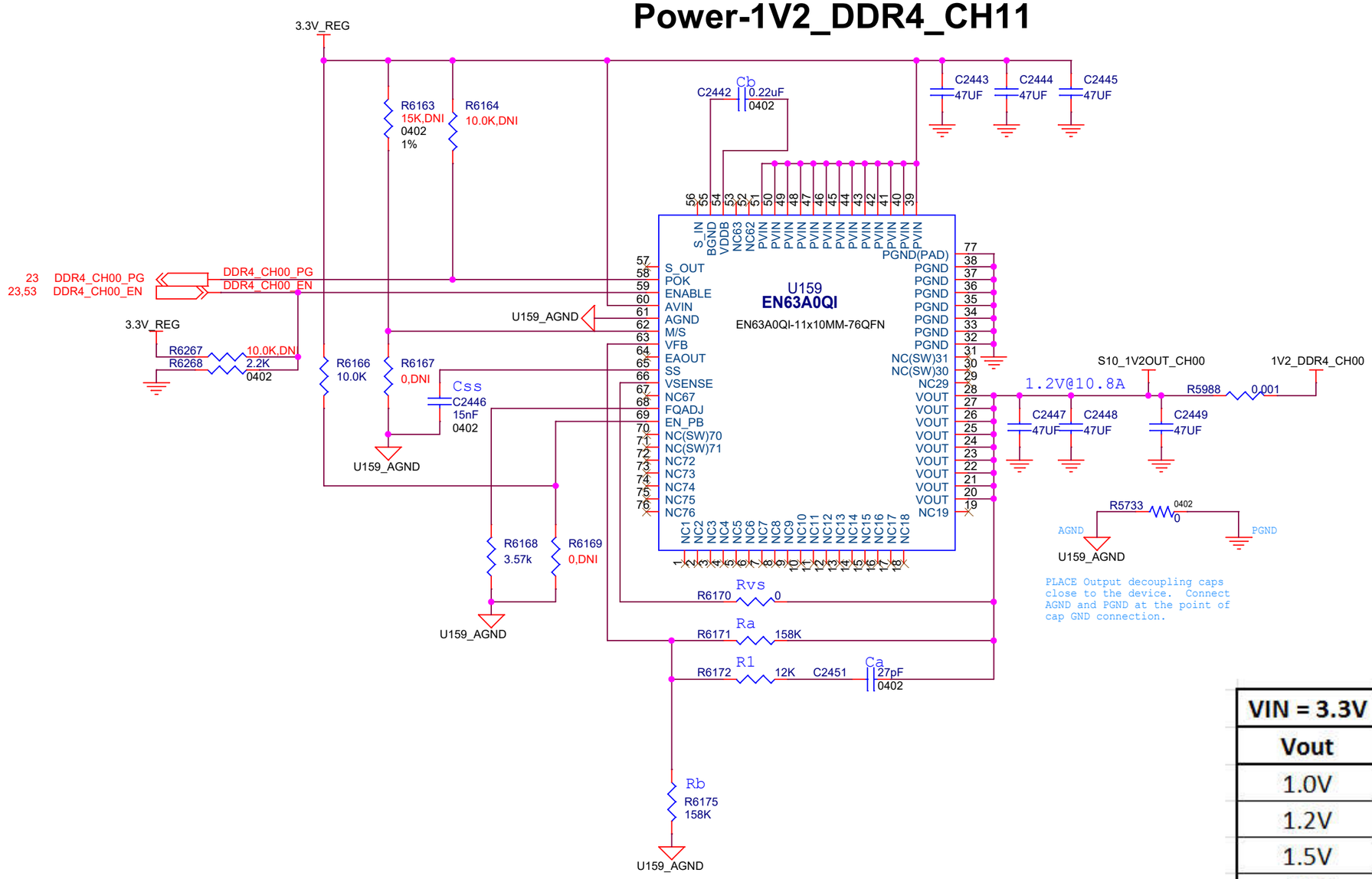
Power-1V2_DDR4_CH11



VIN = 3.3V				
Vout	RA	RB	CA	R1
1.0V	158k	237k	27pF	12k
1.2V	158k	158k	27pF	12k
1.5V	158k	105k	27pF	12k
1.8V	158k	78.7K	27pF	12k
2.5V	158k	49.9K	27pF	12k

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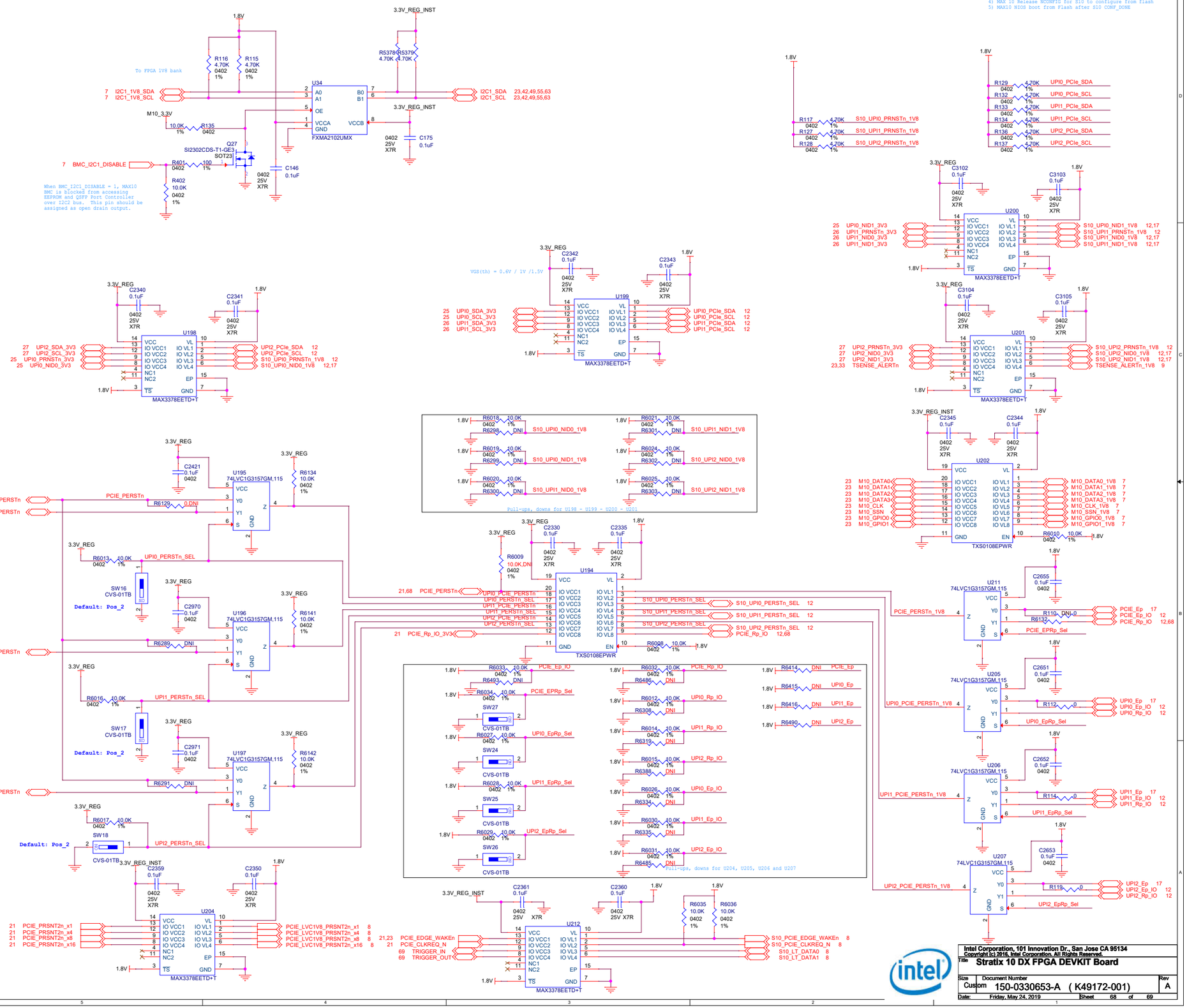
Level Translators, IOexp

1) M10_2V5 power good
2) MAX10 configures itself from CFM
3) MAX10 Initiate Power Up Sequence
4) MAX 10 Release NCONFIG for S10 to configure from flash
5) MAX10 NIOS boot from Flash after S10 CONF_DONE



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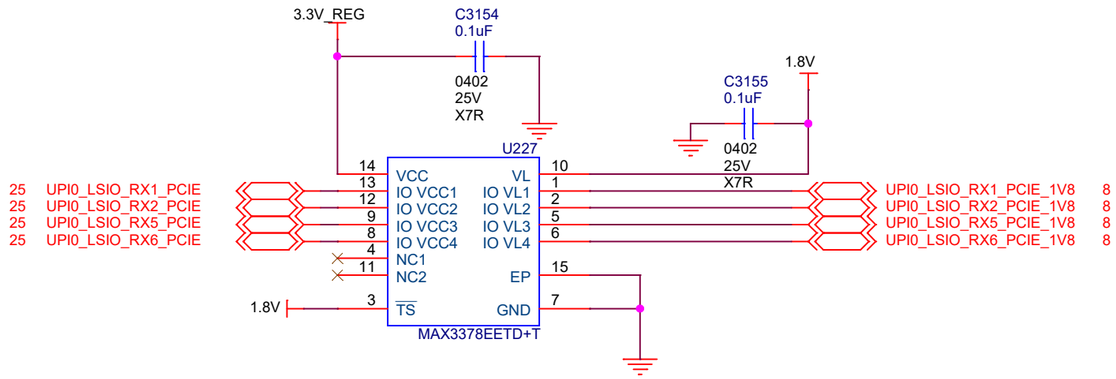
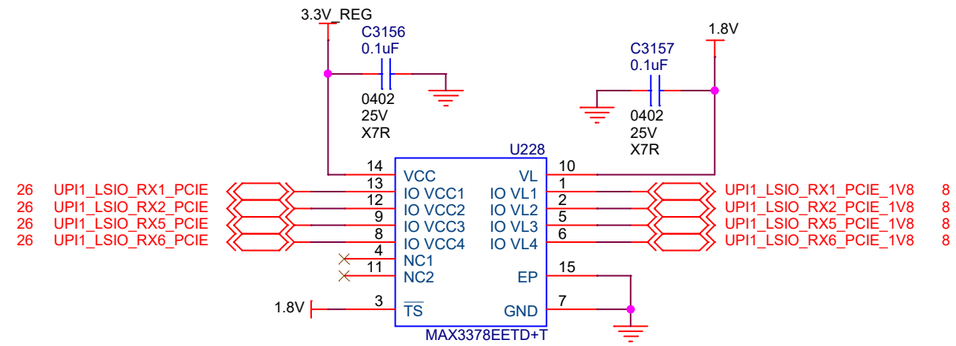
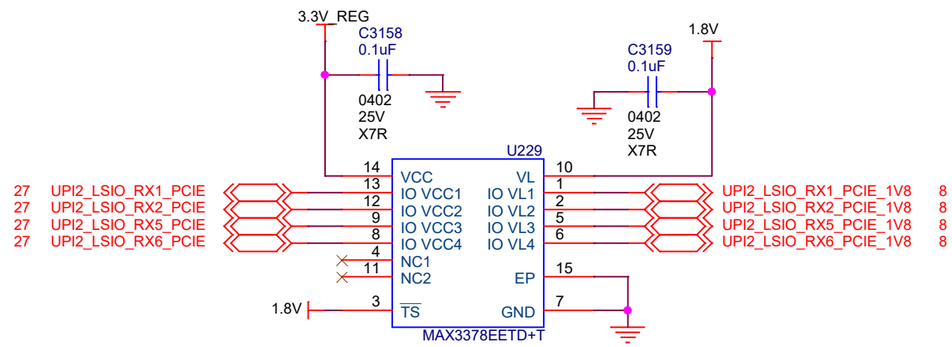
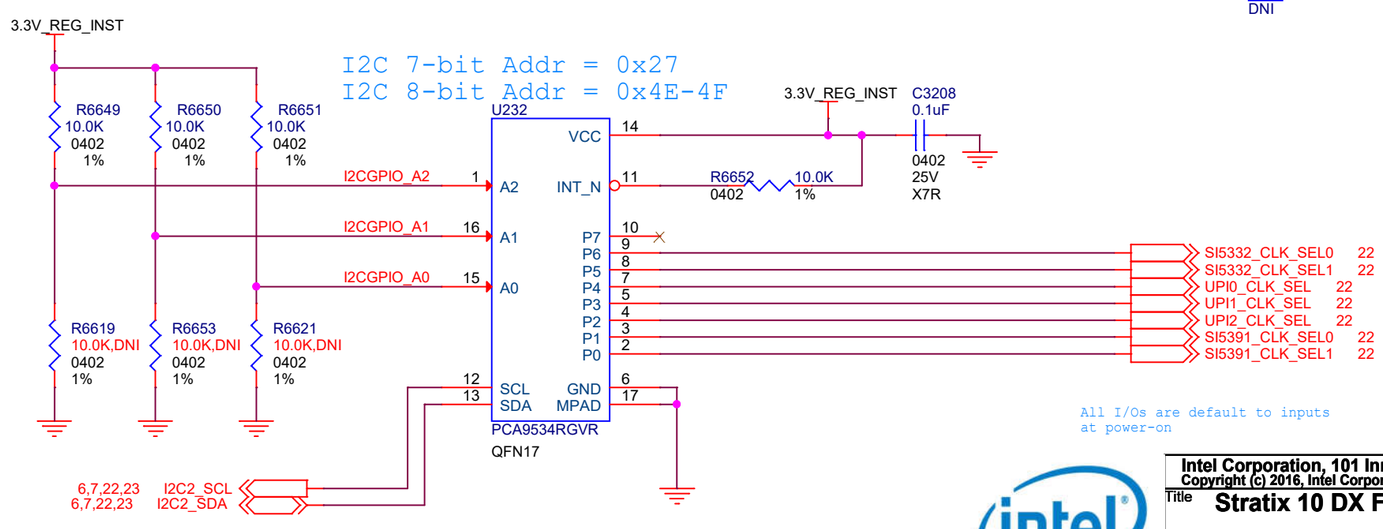
Level translator









All I/Os are default to inputs
at power-on

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