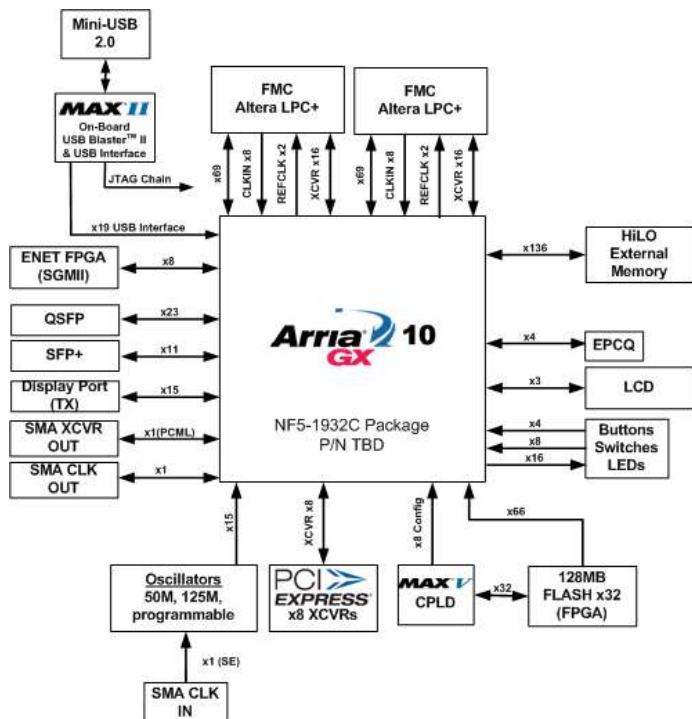


NOTES:

1. Project Drawing Numbers:

PB M88283-002
 PSA M88349-002
 MPN 100-0330700-B1
 TA M88350-002
 MMID 99C5L5

Arria® 10 FPGA Development Kit (Non-ENP)



Note: Design database is leveraged from MMID: 979983, TA-J99940-001, PBA-K11695-001, PB-K15395-001

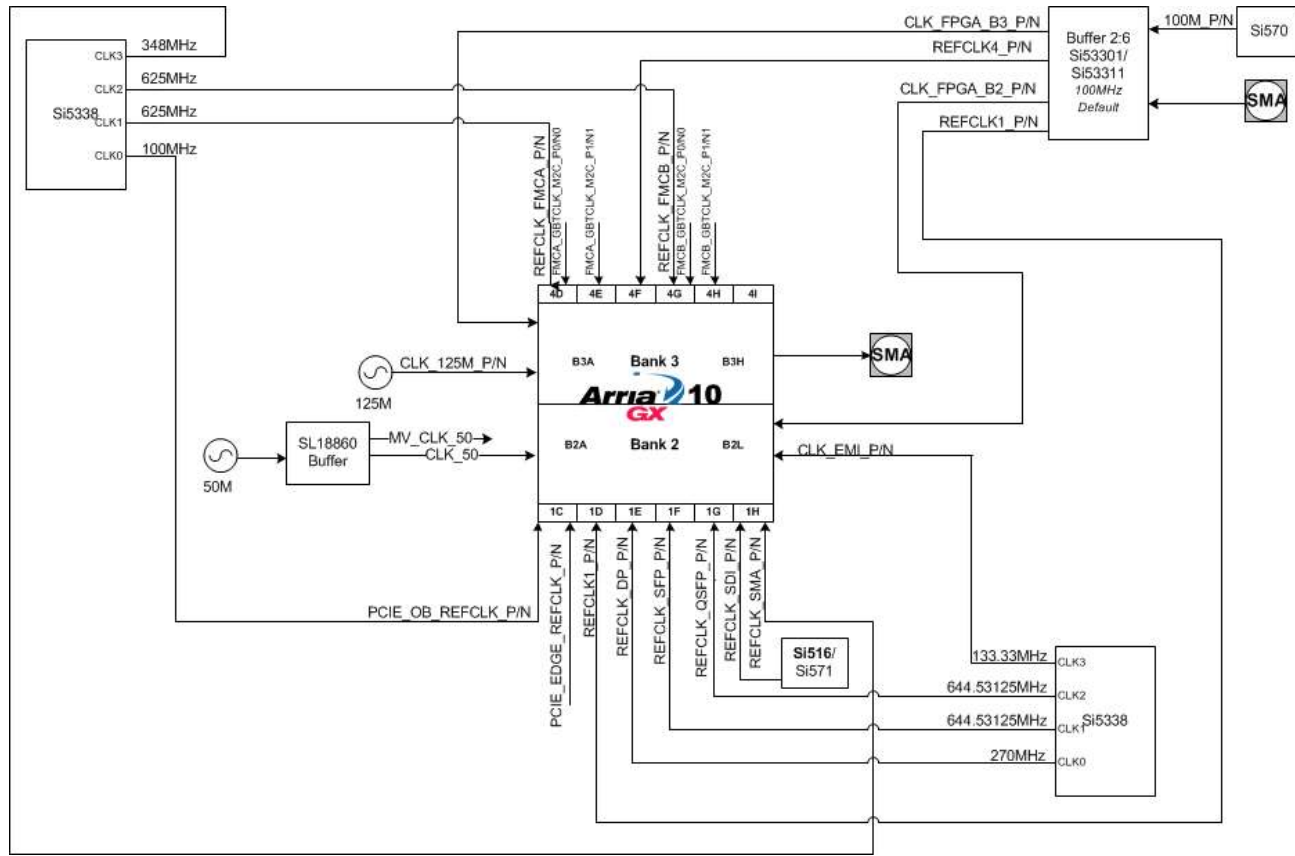
REV	DATE	PAGES	DESCRIPTION	DONE BY
A	30-Aug-2022	1 to 49	Initial release	Yaseen
B	10-Aug-2023	1 to 49	Test points at SW pins and BST pins of VRs are removed	Bhaskara

PAGE	DESCRIPTION	PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Rev. History	37	Power1 A10 VCC ET4040 (2)
2	Clock Diagram	38	Power2 - A10 VCCRAM
3	PCI Express Edge Connector	39	Power2 - A10 VCCR GXB
4	Arria® 10 GX Bank 2	40	Blank Page
5	Arria® 10 GX Bank 3A-3D	41	Power3 - A10 VCCPT/1.8V
6	Arria® 10 GX Bank 3E-3H	42	Power4 - A10 VCCIO 1.8V
7	Arria® 10 Configuration	43	Power4 - A10 VCCIO FMCA
8	Arria® 10 Clocks	44	Power4 - A10 VCCIO FMCB
9	PLL	45	Power4 - A10 VCCIO MEM
10	PLL2	46	Arria 10 Power
11	Arria® 10 XCVR Left (B1)	47	Arria 10 Ground
12	Arria® 10 XCVR Right (B4)	48	Decoupling
13	5M2210 System Controller	49	Power-Down Discharge
14	Flash	50	
15	10/100/1000 Ethernet PHY	51	
16	EMI Connector Map	52	
17	External Memory Interface	53	
18	DisplayPort (x4)	54	
19	FMC Port A	55	
20	FMC Port B	56	
21	QSFP	57	
22	SFP+	58	
23	SDI Transmit/Receive	59	
24	User IO	60	
25	On-Board USB Blaster II -1	61	
26	On-Board USB Blaster II -2	62	
27	Power Tree	63	
28	Power Sequence Diagram	64	
29	Voltage & Temperature Sense	65	
30	Power Sequence Control	66	
31	Power - Select Power Input	67	
32	Power - DCin to 3.3V	68	
33	Power - 3.3V & 5.0V		
34	Power - MEM_VDD & 2.5V		
35	Power1 - A10 VCC		
36	Power1 A10 VCC ET4040 (1)		



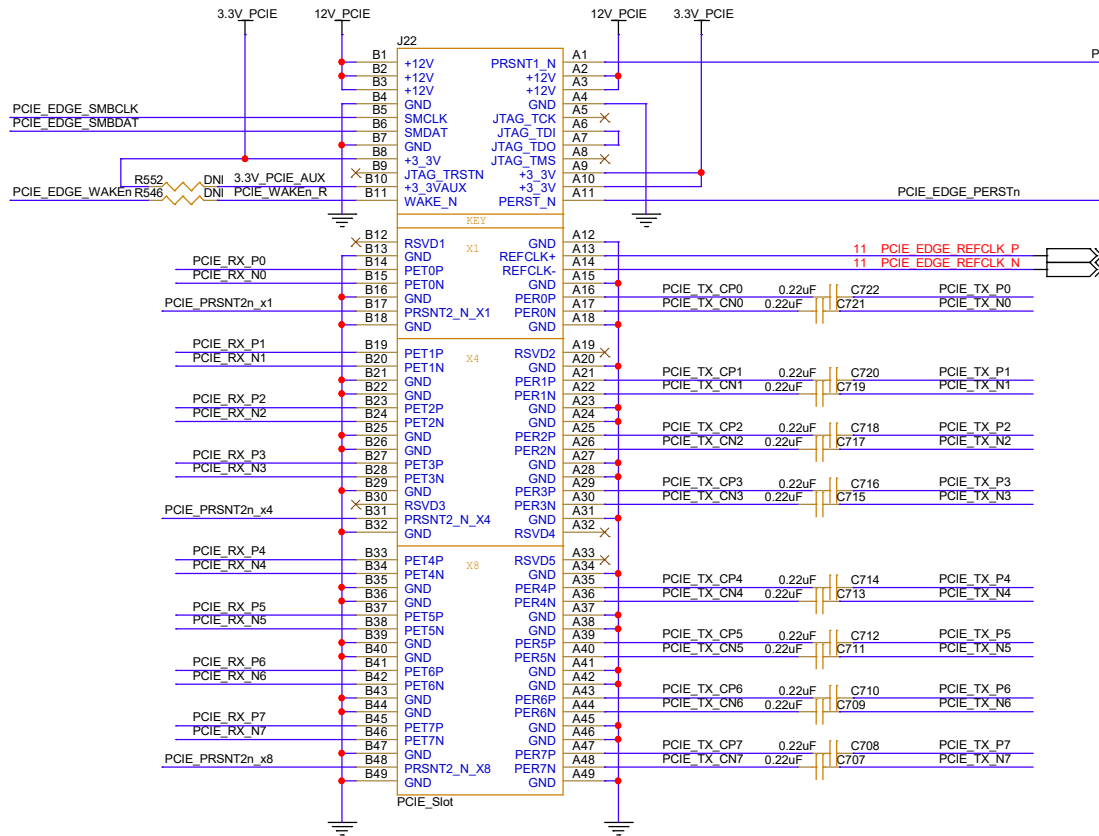
Altera Corporation, 101 innovation Dr, San Jose, CA 95134
 © 2024 Altera Corporation. All Rights Reserved.
Title Arria® 10 GX FPGA Development Kit (Non-ENP)
Size B **Document Number** M88349-002 (100-0330700-B1) **Rev** B
Date: Wednesday, December 11, 2024 **Sheet** 1 of 49

Clock Diagram

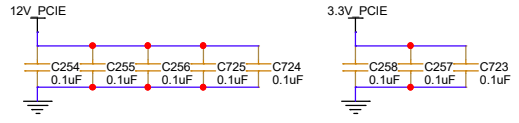


Altera Corporation, 101 innovation Dr, San Jose, CA 95134 © 2024 Altera Corporation. All Rights Reserved.		
Title Arria® 10 GX FPGA Development Kit (Non-ENP)		
Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
Date: Wednesday, December 11, 2024	Sheet 2	of 49

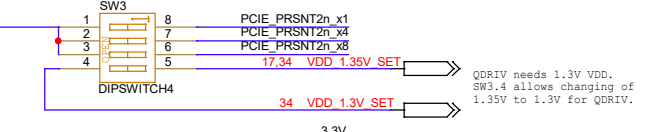
PCI Express Edge Connector



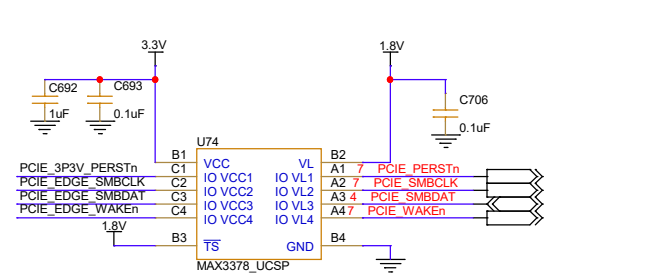
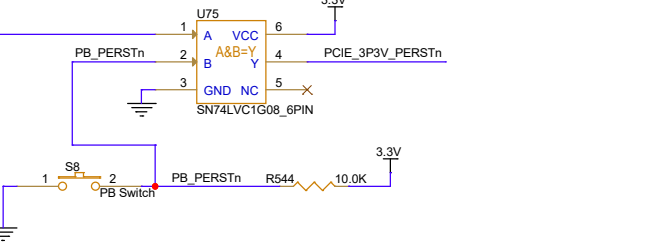
75-ohm to 100-ohm XCVR traces.



Link Width DIP Switch



QDRIV needs 1.35V VDD. SW3.4 allows changing of 1.35V to 1.3V for QDRIV.



Altera Corporation, 101 Innovation Dr., San Jose, CA 95134 © 2024 Altera Corporation. All Rights Reserved.			
Title: Arria® 10 GX FPGA Development Kit (Non-ENP)			
Size: B	Document Number: M88349-002 (100-0330700-B1)	Rev: B	
Date: Wednesday, December 11, 2024	Sheet: 3	of 49	

Arria® 10 GX Bank 2

U28C

ARRIA 10 - BANK 2I-2L

OSFP_LP_MODE	AK34	IO.LVDS2I_1P.DQ12L	IO.LVDS2K_1P.DQ04L
OSFP_INTERRUPTn	AL34	IO.LVDS2I_1N.DQ12L	IO.LVDS2K_1N.DQ04L
DP_HOT_PLUG	AM30	IO.LVDS2I_2P.DQ12L	IO.LVDS2K_2P.DQ04L
CLOCK_SDA	AN30	IO.LVDS2I_2N.DQ12L	IO.LVDS2K_2N.DQ04L
DP_RETURN	AL32	IO.LVDS2I_3P.DQ12L	IO.LVDS2K_3P.DQ04L
DP_CONFIG2	AK32	IO.LVDS2I_3N.DQ12L	IO.LVDS2K_3N.DQ04L
DP_CONFIG1	AK31	IO.LVDS2I_5P.DQ12L	IO.LVDS2K_5P.DQ04L
	AM31	IO.LVDS2I_5N.DQ12L	IO.LVDS2K_5N.DQ04L
DP_AUX_CH_P	AM32	IO.LVDS2I_6N.DQ12L	IO.LVDS2K_6N.DQ04L
DP_AUX_CH_N	AN34	IO.LVDS2I_4P.DQS12L	IO.LVDS2K_4P.DQS04L
	AM35	IO.LVDS2I_4N.DQSN12L	IO.LVDS2K_4N.DQSN04L
	AR32	IO.LVDS2I_7P.DQ13L	IO.LVDS2K_7P.DQ05L
	AP32	IO.LVDS2I_7N.DQ13L	IO.LVDS2K_7N.DQ05L
	AT37	IO.LVDS2I_8P.DQ13L	IO.LVDS2K_8P.DQ05L
PCIE_SMBDAT	AU37	IO.LVDS2I_8N.DQ13L	IO.LVDS2K_8N.DQ05L
	AP34	IO.LVDS2I_9P.DQ13L	IO.LVDS2K_9P.DQ05L
	AP33	IO.LVDS2I_9N.DQ13L	IO.LVDS2K_9N.DQ05L
	AR34	IO.RZQ_2I.LVDS2I_11P.DQ13L	IO.RZQ_2K.LVDS2K_11P.DQ05L
	AR35	IO.LVDS2I_11N.DQ13L	IO.LVDS2K_11N.DQ05L
SFP_MOD0_PRSNTn	AT30	IO.LVDS2I_14P.DQ14L	IO.LVDS2K_14P.DQ06L
SFP_MOD2_SDA	AR31	IO.LVDS2I_14N.DQ14L	IO.LVDS2K_14N.DQ06L
SFP_RST	AT34	IO.LVDS2I_16P.DQS14L	IO.LVDS2K_17P.DQ06L
SFP_TX_FAULT	AT35	IO.LVDS2I_16N.DQSN14L	IO.LVDS2K_17N.DQ06L
SFP_RS0	AR30	IO.LVDS2I_17P.DQ14L	IO.LVDS2K_18P.DQ06L
SFP_MOD1_SCL	AP31	IO.LVDS2I_17N.DQ14L	IO.LVDS2K_18N.DQ06L
OSFP_SDA	AU31	IO.LVDS2I_18P.DQ14L	IO.LVDS2K_16P.DQS6L
SFP_RX_LOS	AU30	IO.LVDS2I_18N.DQ14L	IO.LVDS2K_16N.DQSN6L
OSFP_MOD_PRSn	AU36	IO.LVDS2I_19P.DQ15L	IO.LVDS2K_19P.DQ07L
OSFP_MOD_SELn	AU35	IO.LVDS2I_19N.DQ15L	IO.LVDS2K_19N.DQ07L
OSFP_RSTn	AV34	IO.LVDS2I_20P.DQ15L	IO.LVDS2K_20P.DQ07L
SDI_MF2_MUTE	AY35	IO.LVDS2I_20N.DQ15L	IO.LVDS2K_20N.DQ07L
SDI_TX_SD_HDn	AW34	IO.LVDS2I_21P.DQ15L	IO.LVDS2K_21P.DQ07L
DISP_I2C_SCL	AW33	IO.LVDS2I_21N.DQ15L	IO.LVDS2K_21N.DQ07L
CLOCK_SCL	AV33	IO.LVDS2I_23P.DQ15L	IO.LVDS2K_23P.DQ07L
DISP_I2C_SDA	AY34	IO.LVDS2I_24P.DQ15L	IO.LVDS2K_24P.DQ07L
DISP_SPISS	BA35	IO.LVDS2I_24N.DQ15L	IO.LVDS2K_24N.DQ07L
SDI_MF0_BYPASS	AW32	IO.LVDS2I_22P.DQS15L	IO.LVDS2K_22P.DQS07L
SDI_MF1_AUTO_SLEEP	AY32	IO.LVDS2I_22N.DQSN15L	IO.LVDS2K_22N.DQSN07L
MEM_DQB0	AC31	IO.LVDS2I_1P.DQ08L	IO.LVDS2L_1P.DQ00L
MEM_DQB4	AD31	IO.LVDS2I_1N.DQ08L	IO.LVDS2L_1N.DQ00L
MEM_DQB6	AD33	IO.LVDS2I_2P.DQ08L	IO.LVDS2L_2P.DQ00L
MEM_DQB5	AD32	IO.LVDS2I_2N.DQ08L	IO.LVDS2L_2N.DQ00L
MEM_DNB0	AB31	IO.LVDS2I_3P.DQ08L	IO.LVDS2L_3P.DQ00L
MEM_DQB1	AB31	IO.LVDS2I_3N.DQ08L	IO.LVDS2L_3N.DQ00L
MEM_DQB3	Y31	IO.LVDS2I_5P.DQ08L	IO.LVDS2L_5P.DQ00L
MEM_DQB2	W31	IO.LVDS2I_5N.DQ08L	IO.LVDS2L_5N.DQ00L
MEM_QKB_P0	Y30	IO.LVDS2I_6P.DQ08L	IO.LVDS2L_6P.DQ00L
MEM_DQB7	AA30	IO.LVDS2I_6N.DQ08L	IO.LVDS2L_6N.DQ00L
MEM_DQSB_P0	Y32	IO.LVDS2I_4P.DQS08L	IO.LVDS2L_4P.DQS00L
MEM_DQSB_N0	AA32	IO.LVDS2I_4N.DQSN08L	IO.LVDS2L_4N.DQSN00L
MEM_DQB8	AE31	IO.LVDS2I_7P.DQ09L	IO.LVDS2L_7P.DQ01L
MEM_DQB9	AE32	IO.LVDS2I_7N.DQ09L	IO.LVDS2L_7N.DQ01L
MEM_DQB10	AE30	IO.LVDS2I_8P.DQ09L	IO.LVDS2L_8P.DQ01L
MEM_DQB11	AF30	IO.LVDS2I_8N.DQ09L	IO.LVDS2L_8N.DQ01L
MEM_DQB12	AG33	IO.LVDS2I_9P.DQ09L	IO.LVDS2L_9P.DQ01L
MEM_DQB14	AH33	IO.LVDS2I_9N.DQ09L	IO.LVDS2L_9N.DQ01L
MEM_DQB32	AF32	IO.RZQ_2I.LVDS2I_11P.DQ09L	IO.RZQ_2L.LVDS2L_11P.DQ01L
MEM_DQB13	AG32	IO.LVDS2I_11N.DQ09L	IO.LVDS2L_11N.DQ01L
MEM_DQB18	W32	IO.LVDS2I_14P.DQ10L	IO.LVDS2L_14P.DQ02L
MEM_DQB17	W33	IO.LVDS2I_14N.DQ10L	IO.LVDS2L_14N.DQ02L
MEM_DQB21	W36	IO.LVDS2I_17P.DQ10L	IO.LVDS2L_17P.DQ02L
MEM_DMB2	Y35	IO.LVDS2I_17N.DQ10L	IO.LVDS2L_17N.DQ02L
MEM_QKB_P1	AF33	IO.LVDS2I_18P.DQ10L	IO.LVDS2L_18P.DQ02L
MEM_DQB23	V34	IO.LVDS2I_18N.DQ10L	IO.LVDS2L_18N.DQ02L
MEM_DQSB_P2	AA34	IO.LVDS2I_16P.DQS10L	IO.LVDS2L_16P.DQS02L
MEM_DQSB_N2	AA33	IO.LVDS2I_16N.DQSN10L	IO.LVDS2L_16N.DQSN02L
MEM_DQB31	AD34	IO.LVDS2I_19P.DQ11L	IO.LVDS2L_19P.DQ03L
MEM_DMB3	AC34	IO.LVDS2I_19N.DQ11L	IO.LVDS2L_19N.DQ03L
MEM_DQB33	AB33	IO.LVDS2I_20P.DQ11L	IO.LVDS2L_20P.DQ03L
MEM_DQB30	AC33	IO.LVDS2I_20N.DQ11L	IO.LVDS2L_20N.DQ03L
MEM_DQB28	AD35	IO.LVDS2I_21P.DQ11L	IO.LVDS2L_21P.DQ03L
MEM_DQB29	AE34	IO.LVDS2I_21N.DQ11L	IO.LVDS2L_21N.DQ03L
MEM_DQB26	AJ33	IO.LVDS2I_23P.DQ11L	IO.LVDS2L_23P.DQ03L
MEM_DQB25	AJ34	IO.LVDS2I_23N.DQ11L	IO.LVDS2L_23N.DQ03L
MEM_DQB27	AH34	IO.LVDS2I_24P.DQ11L	IO.LVDS2L_24P.DQ03L
MEM_DQB24	AH35	IO.LVDS2I_24N.DQ11L	IO.LVDS2L_24N.DQ03L
MEM_DQSB_P3	AF33	IO.LVDS2I_22P.DQS11L	IO.LVDS2L_22P.DQS03L
MEM_DQSB_N3	AF34	IO.LVDS2I_22N.DQSN11L	IO.LVDS2L_22N.DQSN03L

10AX115F1932C

BANK-2K

VARIABLE EMI VCCIO (1.2V, 1.35V, 1.5V)

BANK-2L

VARIABLE EMI VCCIO (1.2V, 1.35V, 1.5V)

D32	MEM_DQ_ADDR_CMD3
C33	MEM_DQ_ADDR_CMD4
B32	MEM_DQ_ADDR_CMD2
A32	MEM_DQ_ADDR_CMD0
B33	MEM_DQ_ADDR_CMD5
A33	MEM_DQ_ADDR_CMD1
C35	MEM_DQ_ADDR_CMD7
D34	MEM_DQ_ADDR_CMD6
E35	MEM_ADDR_CMD29
E34	MEM_DQ_ADDR_CMD8
D33	MEM_DQS_ADDR_CMD_P
C34	MEM_DQS_ADDR_CMD_N
G35	MEM_ADDR_CMD17
H35	MEM_ADDR_CMD18
G33	MEM_ADDR_CMD19
F33	MEM_ADDR_CMD16
E32	MEM_ADDR_CMD15
F32	MEM_ADDR_CMD28
H34	MEM_ADDR_CMD12
H34	MEM_ADDR_CMD12
J33	MEM_ADDR_CMD8
J32	MEM_ADDR_CMD9
N34	MEM_ADDR_CMD2
M35	MEM_ADDR_CMD3
M32	MEM_ADDR_CMD4
L32	MEM_ADDR_CMD1
L34	MEM_ADDR_CMD4
K34	MEM_ADDR_CMD5
U32	MEM_ADDR_CMD30
T32	MEM_ADDR_CMD31
R30	MEM_CLK_P
R31	MEM_CLK_N
U33	MEM_ADDR_CMD20
T33	MEM_ADDR_CMD21
R34	MEM_ADDR_CMD22
P34	MEM_ADDR_CMD23
T34	MEM_ADDR_CMD28
T35	MEM_ADDR_CMD27
N33	MEM_ADDR_CMD24
P33	MEM_ADDR_CMD25
D26	MEM_DQA6
E26	MEM_DMA0
A28	MEM_DQA1
A27	MEM_DQA2
B28	MEM_DQA0
B27	MEM_DQA3
D27	MEM_DQA4
E27	MEM_DQA5
C28	MEM_QKA_P0
D28	MEM_DQA7
B26	MEM_DQSA_P0
C26	MEM_DQSA_N0
F28	MEM_DQA15
F27	MEM_DQA13
G28	MEM_DQA12
G27	MEM_DMA1
H25	MEM_DQA9
G25	MEM_DQA8
J28	MEM_DQA32
K27	MEM_DQA14
D31	MEM_DQA16
C31	MEM_DQA19
E30	MEM_DQA21
E31	MEM_DQA17
E29	MEM_QKA_P1
D29	MEM_DQA23
C30	MEM_DQSA_P2
C29	MEM_DQSA_N2
F30	MEM_DMA3
F29	MEM_DQA31
K29	MEM_DQA29
J29	MEM_DQA30
K31	MEM_DQA27
K30	MEM_DQA24
G30	MEM_DQA26
G31	MEM_DQA33
H29	MEM_DQA28
H30	MEM_DQA25
L30	MEM_DQSA_P3
L29	MEM_DQSA_N3

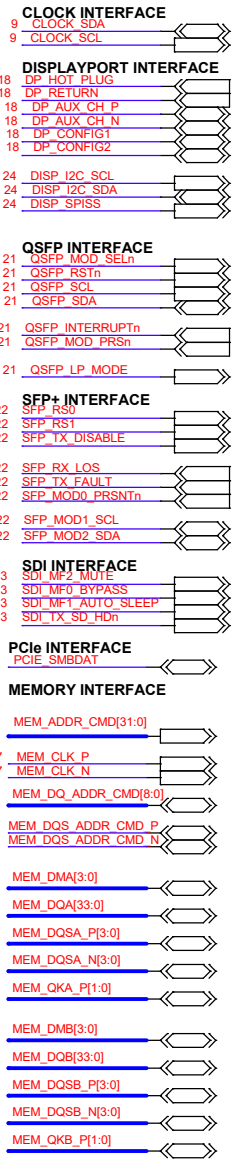
Stratix 5 RZQ 100-ohm for 50-ohm RT or 25-ohm RS.

QDR4 QKB_P0

QDR4 QKA_P0

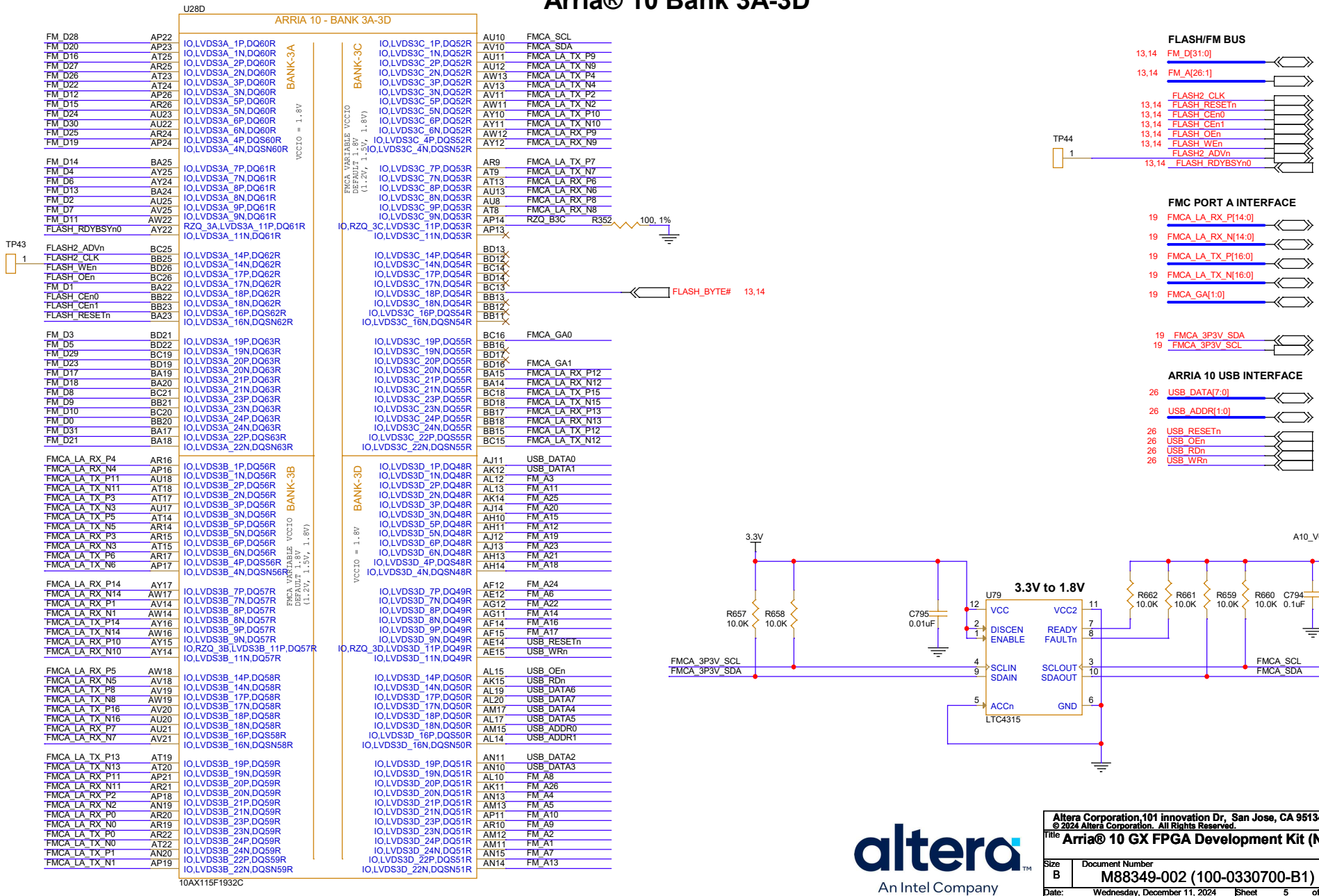
QDR4 QKB_P1

QDR4 QKA_P1

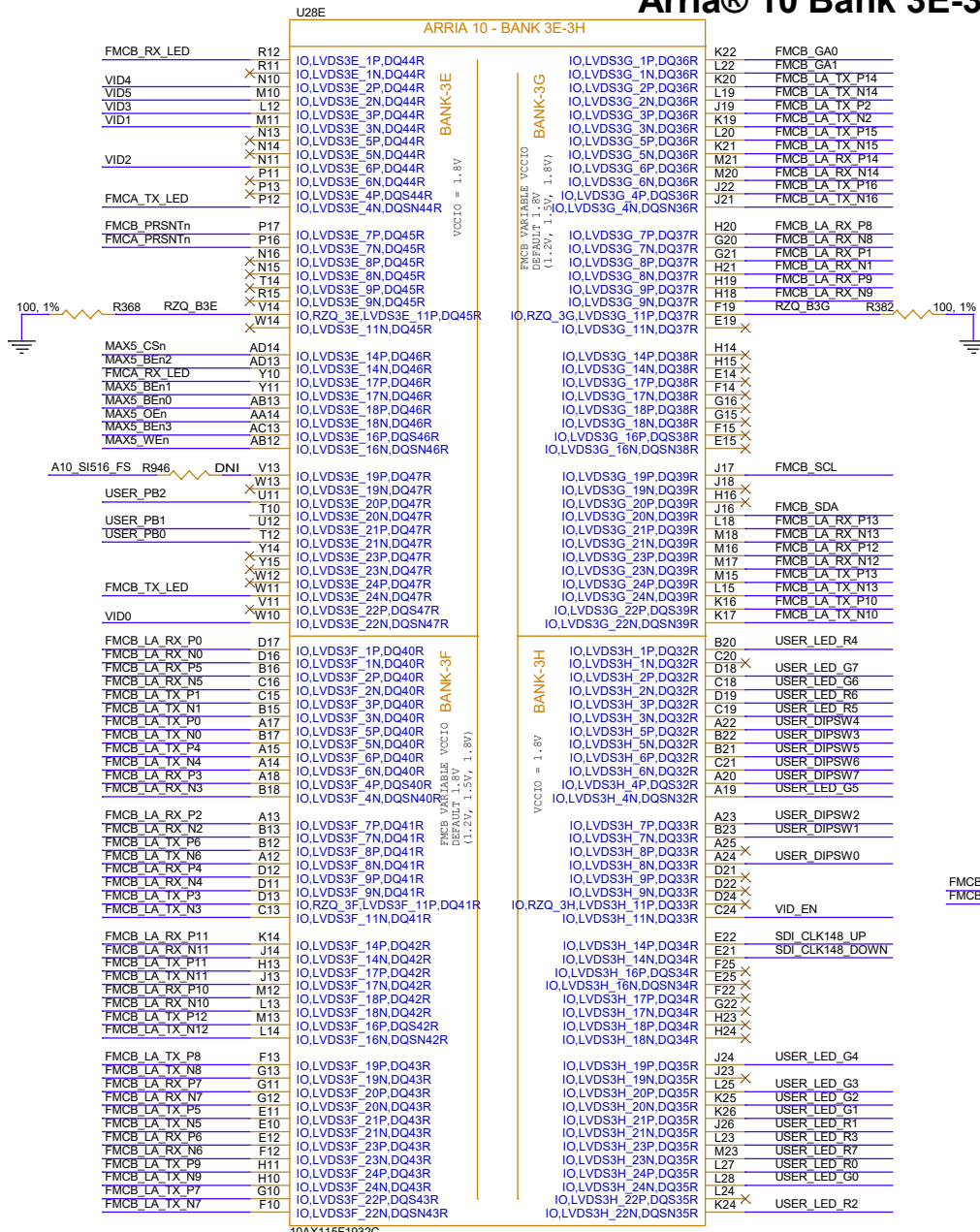


Altera Corporation, 101 innovation Dr, San Jose, CA 95134
 © 2024 Altera Corporation. All Rights Reserved.
Title Arria® 10 GX FPGA Development Kit (Non-ENP)
 Size B Document Number M88349-002 (100-0330700-B1) Rev B
 Date: Wednesday, December 11, 2024 Sheet 4 of 49

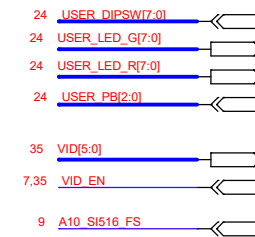
Arria® 10 Bank 3A-3D



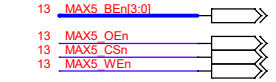
Arria® 10 Bank 3E-3H



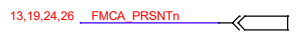
USER IO INTERFACE



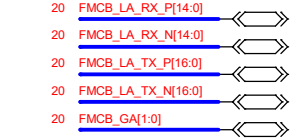
MAX5 INTERFACE



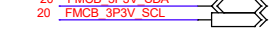
FMC PORT A INTERFACE



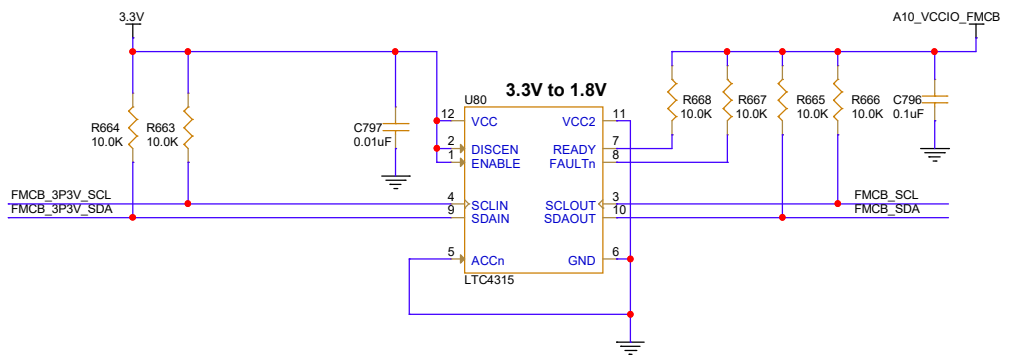
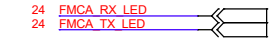
FMC PORT B INTERFACE



USER I/O INTERFACE

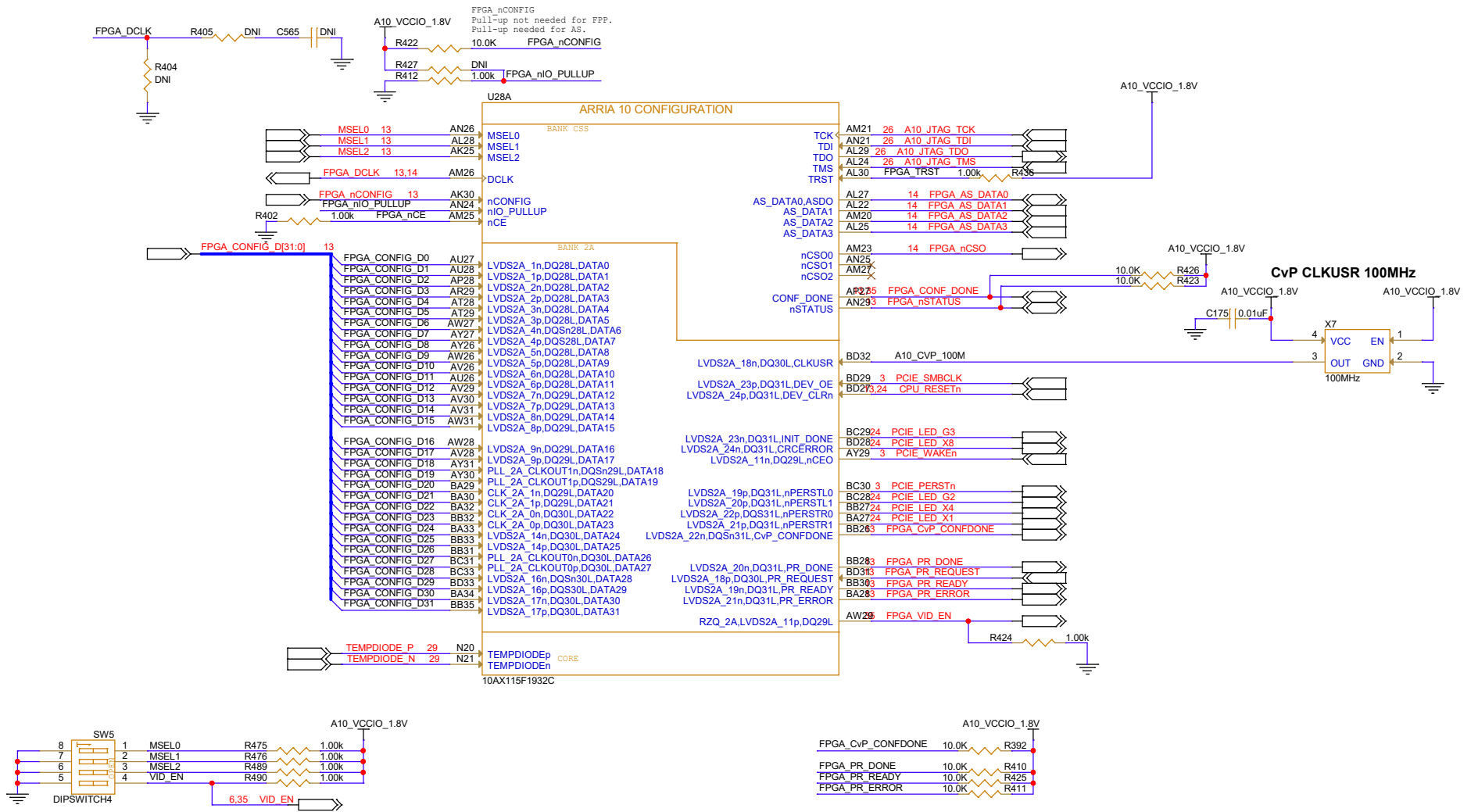


ARRIA 10 CLOCKS

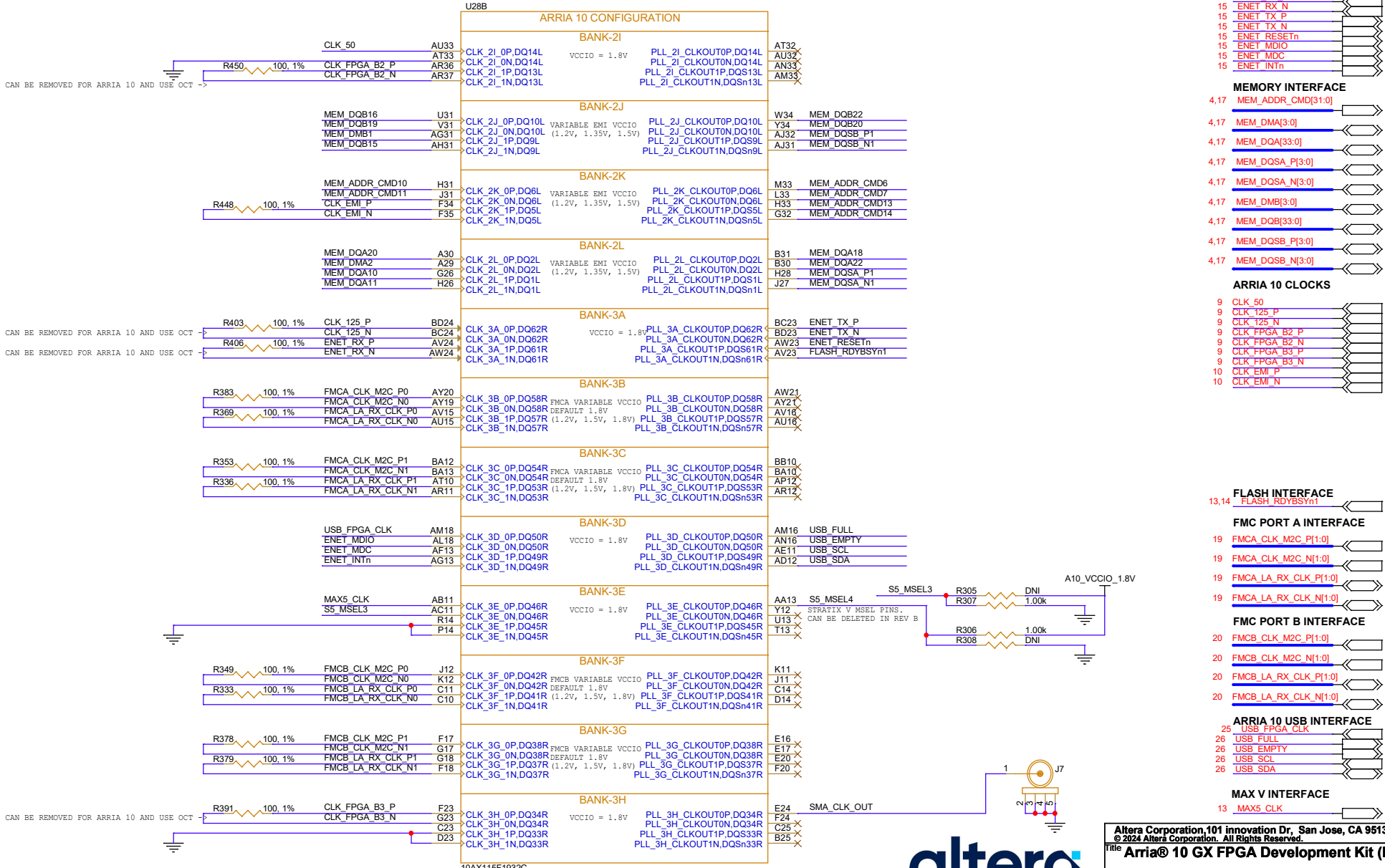


Altera Corporation, 101 Innovation Dr., San Jose, CA 95134
 © 2024 Altera Corporation. All Rights Reserved.
Title Arria® 10 GX FPGA Development Kit (Non-ENP)
Size B **Document Number** M88349-002 (100-0330700-B1) **Rev** B
Date: Wednesday, December 11, 2024 **Sheet** 6 **of** 49

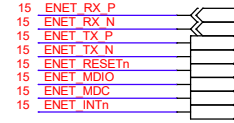
Arria® 10 Configuration



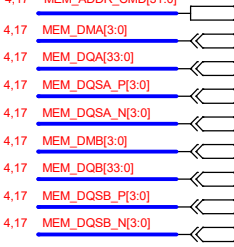
Arria® 10 Clocks



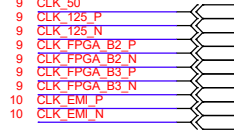
ETHERNET INTERFACE



MEMORY INTERFACE



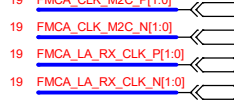
ARRIA 10 CLOCKS



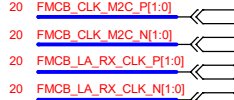
FLASH INTERFACE



FMC PORT A INTERFACE



FMC PORT B INTERFACE



ARRIA 10 USB INTERFACE



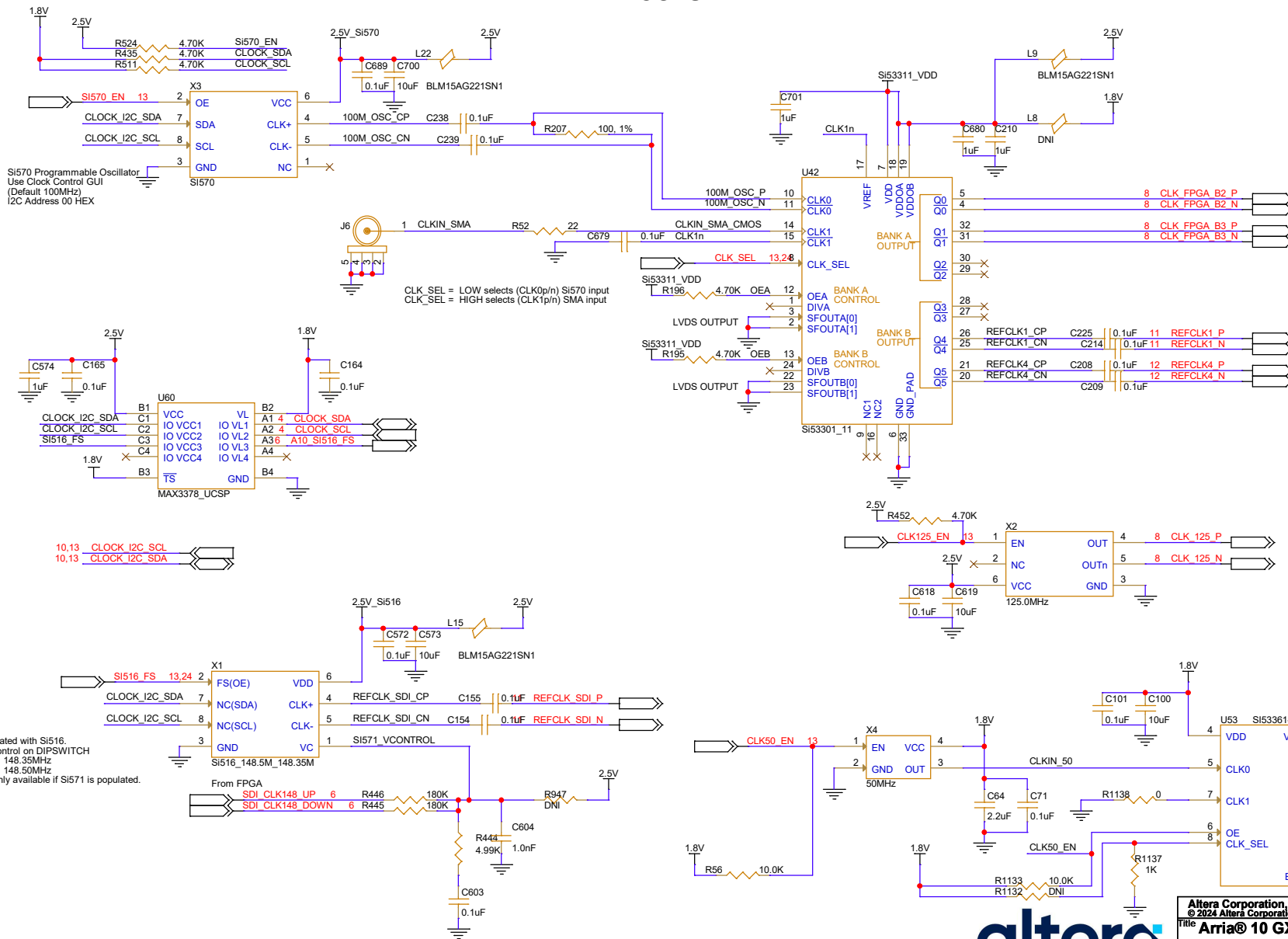
MAX V INTERFACE



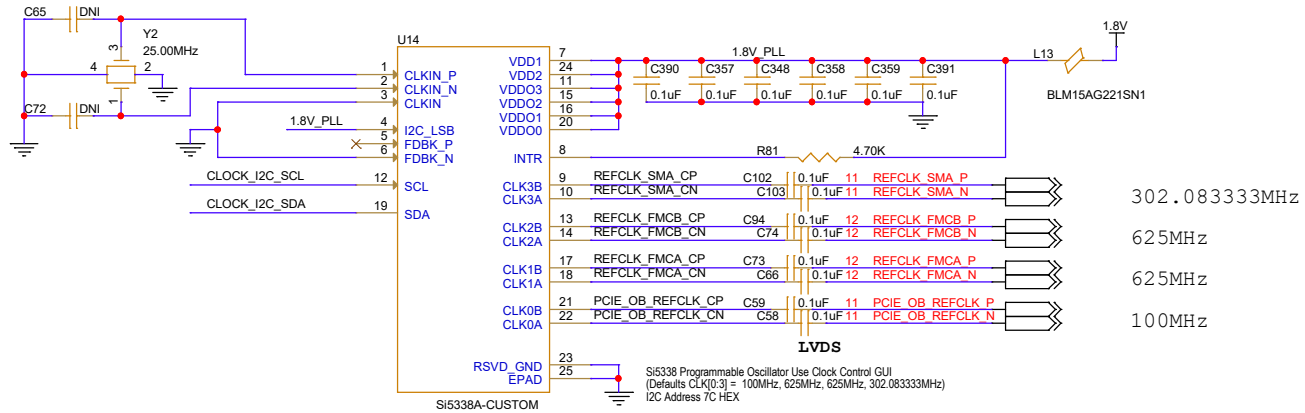
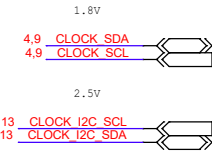
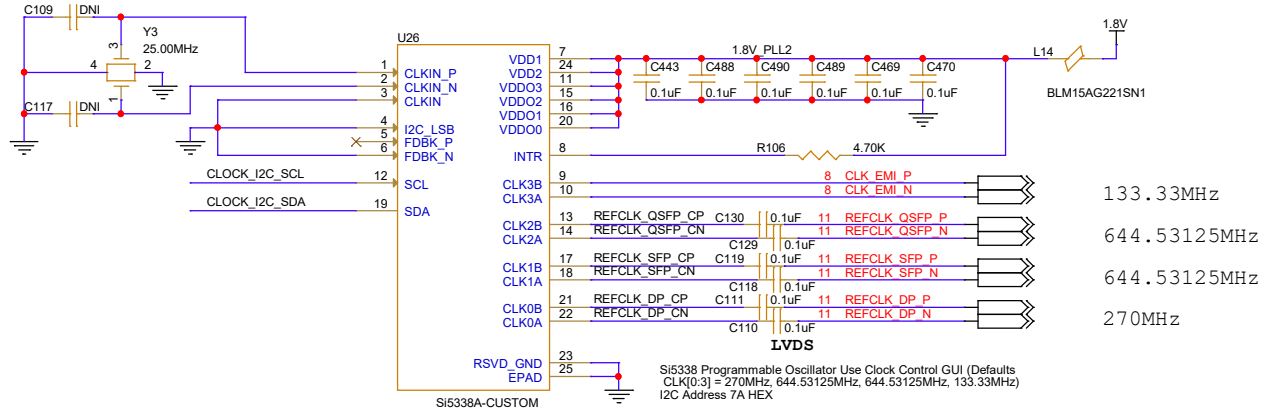
Altera Corporation, 101 innovation Dr, San Jose, CA 95134
 © 2024 Altera Corporation. All Rights Reserved.
Title Arria® 10 GX FPGA Development Kit (Non-ENP)

Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
Date: Wednesday, December 11, 2024	Sheet 8	of 49

Clocks

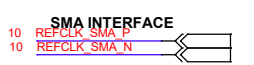
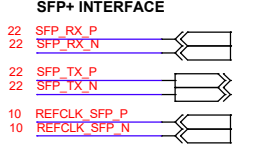
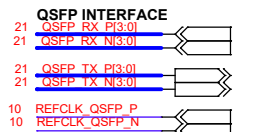
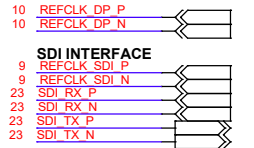
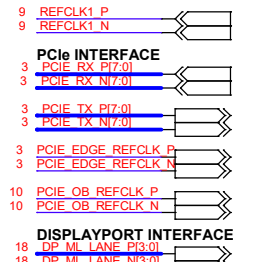
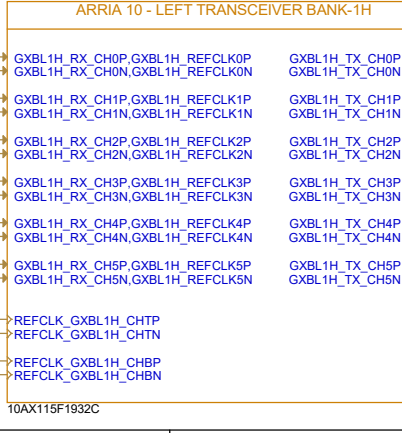
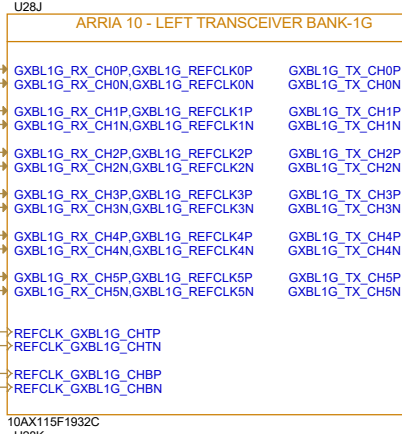
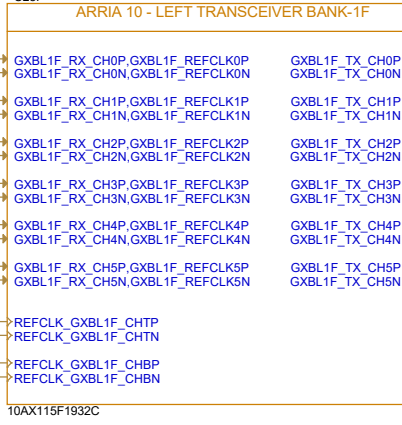
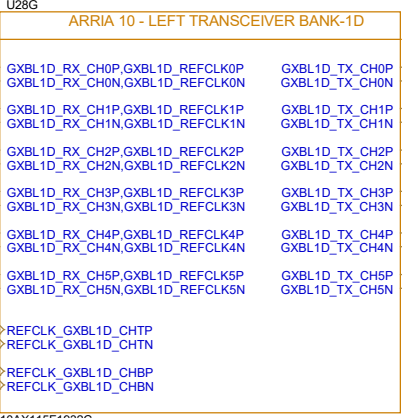
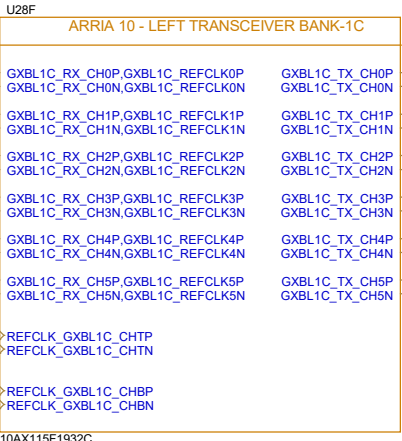


PLL (2)



Altera Corporation, 101 innovation Dr., San Jose, CA 95134 © 2024 Altera Corporation. All Rights Reserved.		
Title Arria® 10 GX FPGA Development Kit (Non-ENP)		
Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
Date: Wednesday, December 11, 2024	Sheet 10	of 49

Arria® 10 Transceivers Left

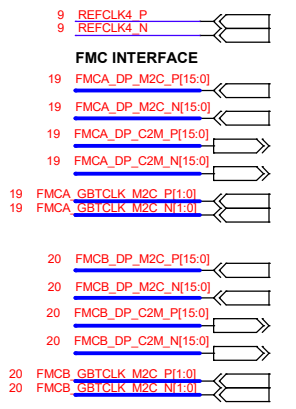
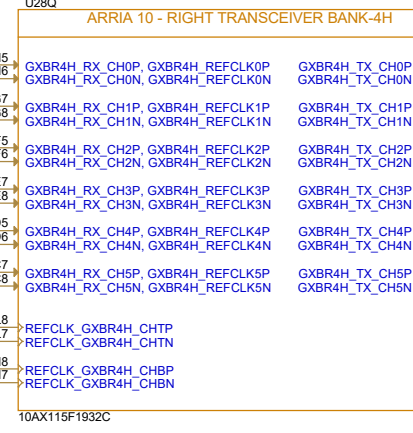
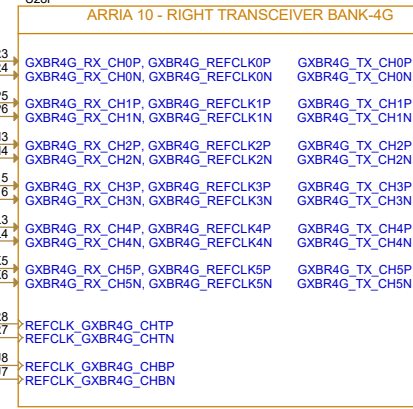
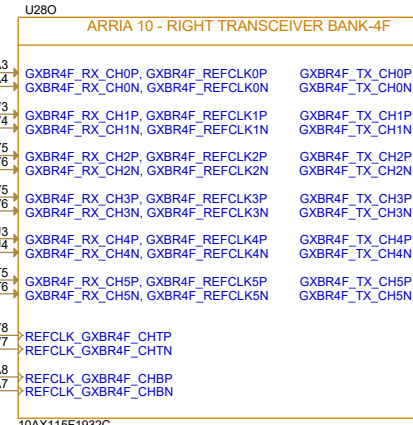
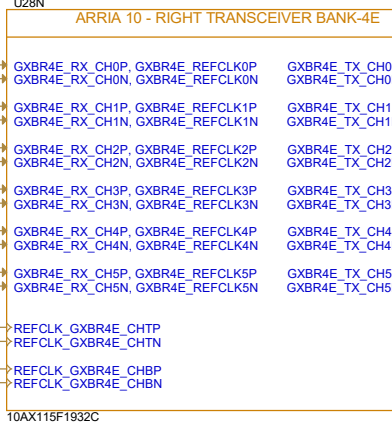
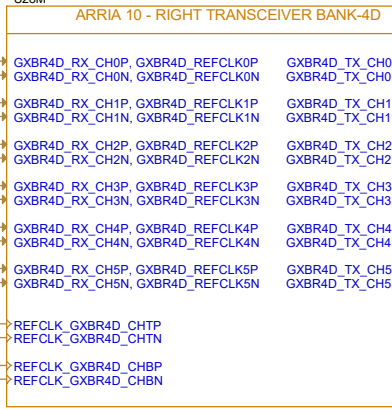
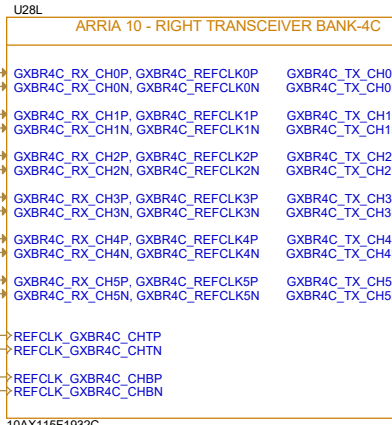


Altera Corporation, 101 Innovation Dr., San Jose, CA 95134
 © 2024 Altera Corporation. All Rights Reserved.

Title Arria® 10 GX FPGA Development Kit (Non-ENP)

Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
Date: Wednesday, December 11, 2024	Sheet 11	of 49

Arria® 10 Transceivers Right

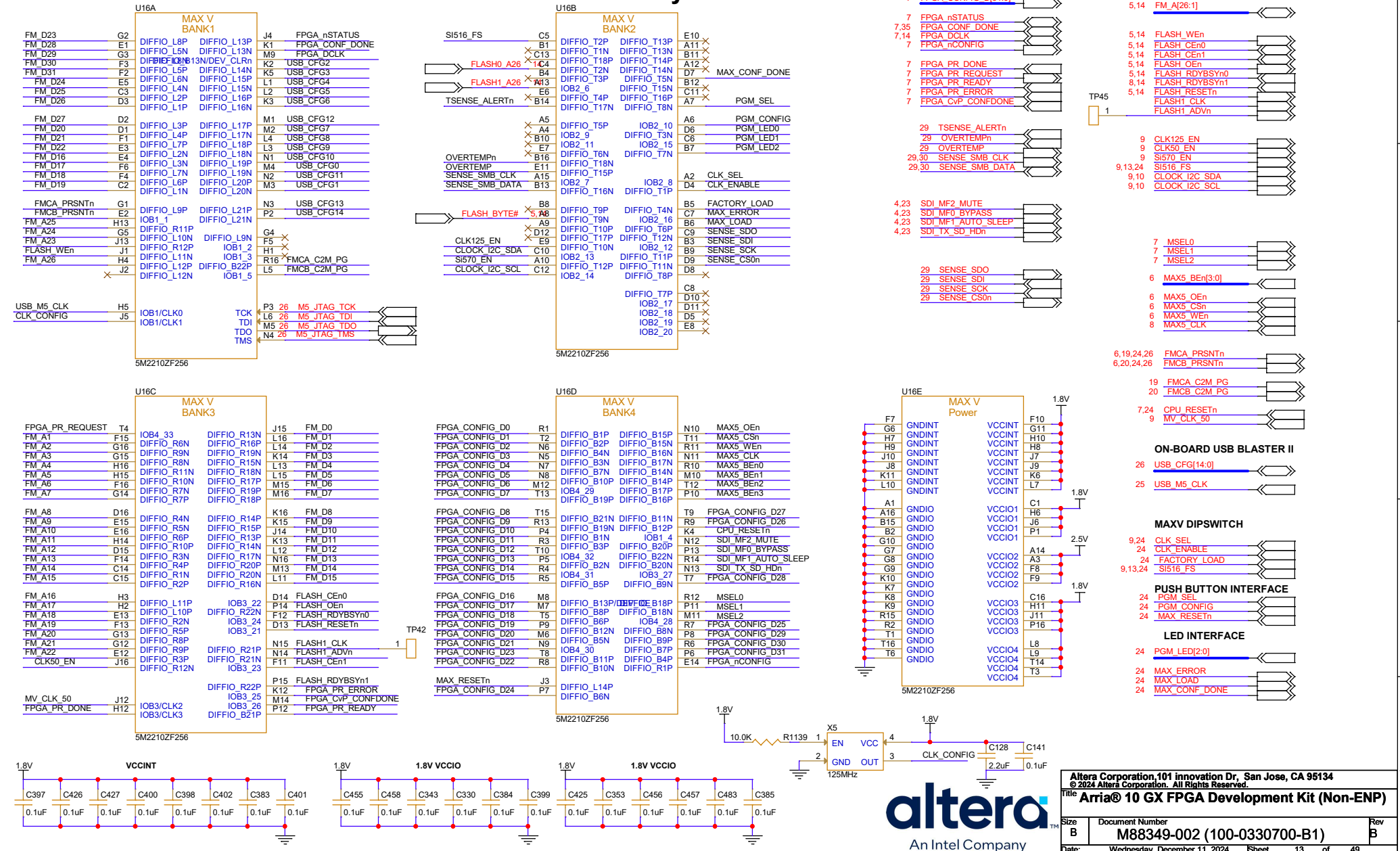


Altera Corporation, 101 innovation Dr, San Jose, CA 95134
© 2024 Altera Corporation. All Rights Reserved.

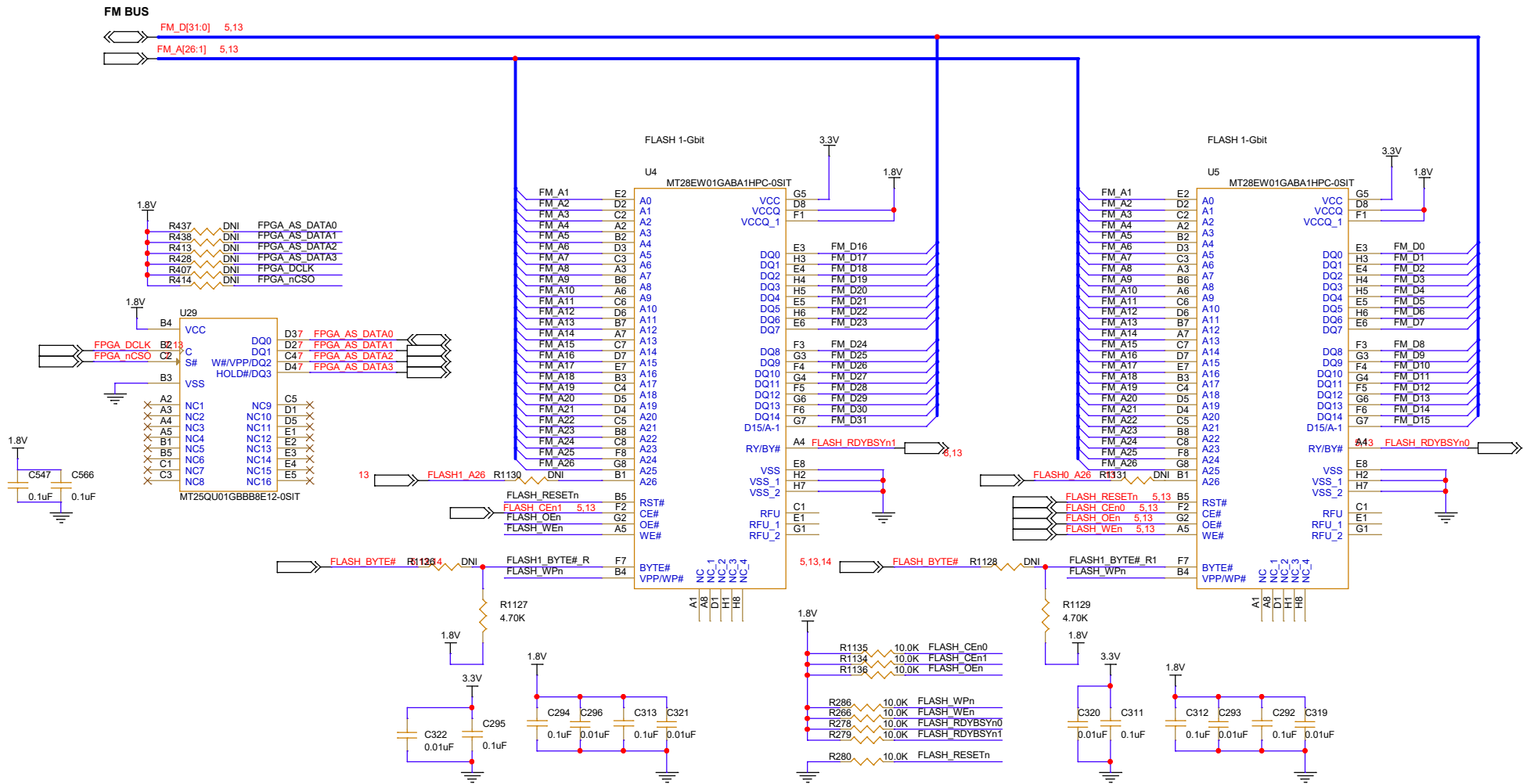
Title **Arria® 10 GX FPGA Development Kit (Non-ENP)**

Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
Date: Wednesday, December 11, 2024	Sheet 12 of 49	

5M2210 System Controller



FLASH



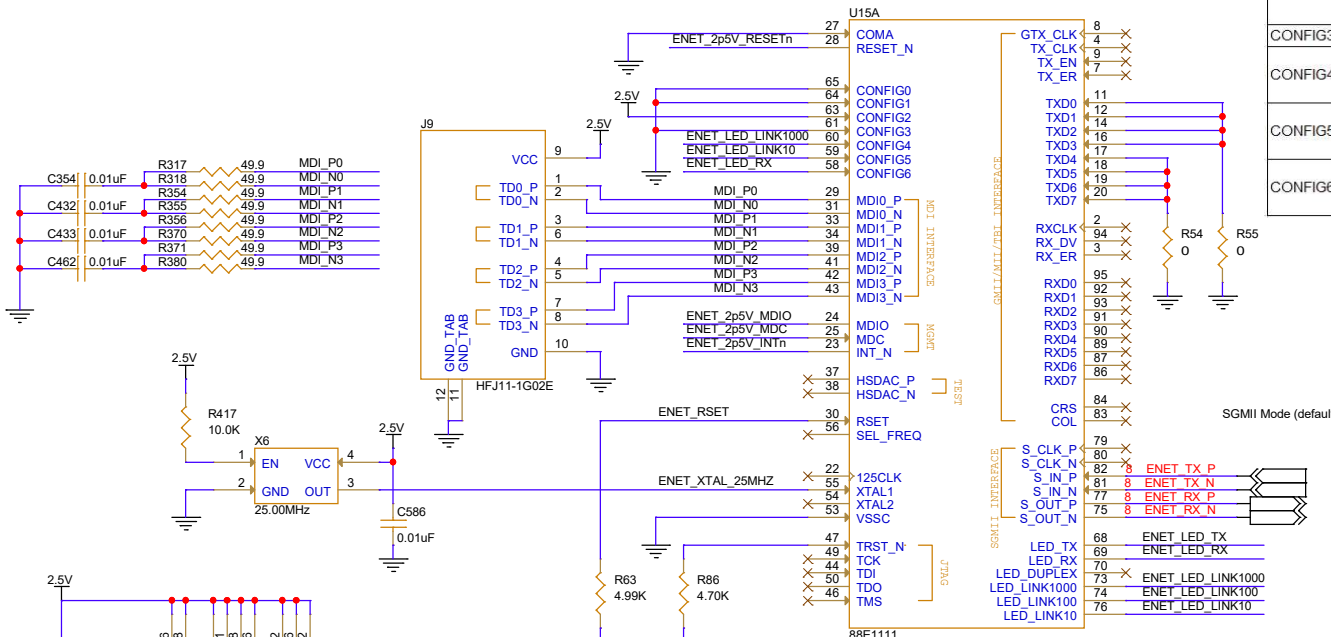
- When using a single x16 flash device a word consists of 16 data bits so addressing starts with FM_A1 mapped to address bit 1 in software.
- When using dual x16 flash devices for an equivalent x32 (x16|x16) flash device a word consists of 32 data bits so addressing starts with FM_A1 mapped to address bit 2 in software.



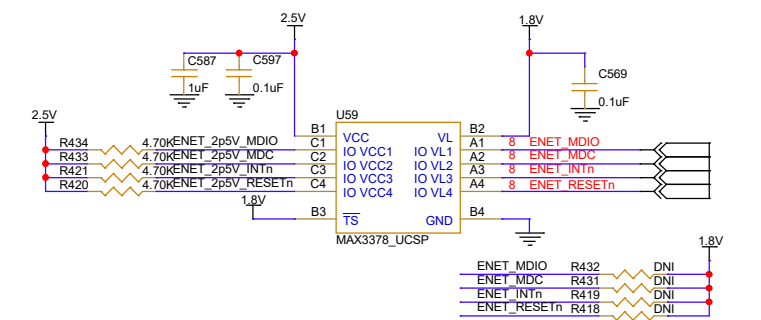
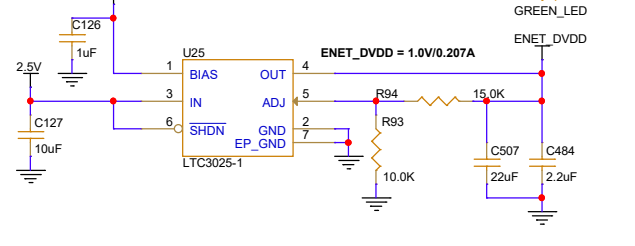
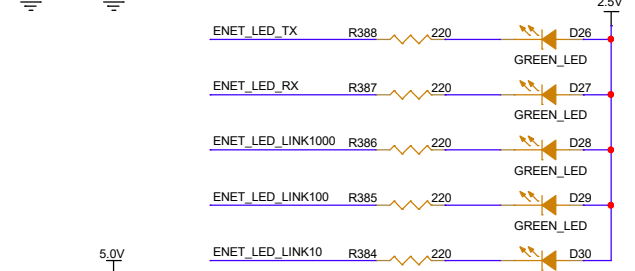
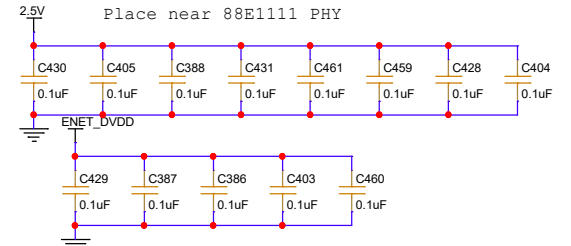
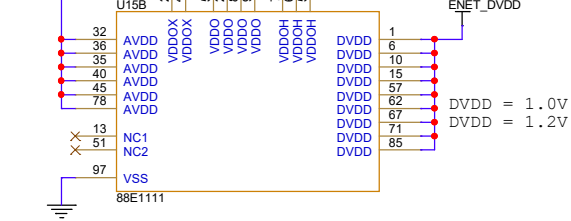
Altera Corporation, 101 Innovation Dr., San Jose, CA 95134 © 2024 Altera Corporation. All Rights Reserved.		
Title: Arria® 10 GX FPGA Development Kit (Non-ENP)		
Size: B	Document Number: M88349-002 (100-0330700-B1)	Rev: B
Date: Wednesday, December 11, 2024	Sheet: 14	of 49

10/100/1000 Ethernet

Pin	Pin Connection	Setting Bit[2:0]	Definition
CONFIG0	GND	000	MDIO PHY Address bit (2:0) = 000
CONFIG1	GND	000	Enable Pause, PHY Address bits (4:3) = 00
CONFIG2	VDDO (2.5V or 3.3V)	111	1110 = Auto-negotiate, advertise all capabilities, prefer Master 100BASE-x FULL-DUPLEX/Auto-Negotiation enabled, 100BASE-X half-duplex
CONFIG3	GND	000	Disable crossover, Enable 125CLK
CONFIG4	LED_LINK1000	100	Hardware Config Mode Reg (2:0) = 100 SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	LED_LIN10	110	Disable fiber/copper autoselect, disable sleep mode (enable energy detect), Hardware Config Mode Reg (3) = 0
CONFIG6	LED_RX	010	Select MDIO (over 2-wire serial), interrupt polarity = active low, 50-ohm termination for fiber



88E1111-B2-CAA1C000 EOL
88E1111-B2-NDC2C000 Replacement



Altera Corporation, 101 innovation Dr, San Jose, CA 95134			
© 2024 Altera Corporation. All Rights Reserved.			
Title Arria® 10 GX FPGA Development Kit (Non-ENP)			
Size B	Document Number	Rev B	
	M88349-002 (100-0330700-B1)		
Date:	Wednesday, December 11, 2024	Sheet	15 of 49

External Memory Interface Connector Map

DDR3 x72 [DQS x8]	DDR4 x72 [DQS x8 Groups]	RLDRAM3 x36 [DQS x8/x9 Groups]	QDR IV x36 [DQS x18 Groups]	HiLo Pin Name	HiLo Pin Number
				CONFIG0	L6
				CONFIG1	M6
A0	A0	A0	A1	MEM_ADDR_CMD[0]	F1
A1	A1	A1	A2	MEM_ADDR_CMD[1]	H1
A10	A10	A10	A11	MEM_ADDR_CMD[10]	E4
A11	A11	A11	A12	MEM_ADDR_CMD[11]	F4
A12	A12	A12	A13	MEM_ADDR_CMD[12]	G4
A13	A13	A13	A14	MEM_ADDR_CMD[13]	H4
A14	A14	A14	A15	MEM_ADDR_CMD[14]	J4
A15	A15	A15	A16	MEM_ADDR_CMD[15]	K4
BA0	BA0	BA0	A19	MEM_ADDR_CMD[16]	M1
BA1	BA1	BA1	A20	MEM_ADDR_CMD[17]	M2
BA2	BG0	BA2	A21	MEM_ADDR_CMD[18]	N2
CASn	A17	A17	A18	MEM_ADDR_CMD[19]	L4
A2	A2	A2	A3	MEM_ADDR_CMD[20]	F2
CKE0	CKE0	A20	RWAn	MEM_ADDR_CMD[22]	P5
CKE1	CKE1	WE _n	RWB _n	MEM_ADDR_CMD[21]	M5
Csn0	Csn0	Csn0	LBK0 _n	MEM_ADDR_CMD[22]	P1
Csn1	ActN	Csn1	LBK1 _n	MEM_ADDR_CMD[23]	R4
ODT0	ODT0	A18	LDAn	MEM_ADDR_CMD[24]	M4
ODT1	ODT1	A19	LDB _n	MEM_ADDR_CMD[25]	R3
RASn	A16	A16	A17	MEM_ADDR_CMD[26]	L2
RESETn	RESETn	RESETn	RESETn	MEM_ADDR_CMD[27]	K1
WE _n	BG1	BA3	CFGn	MEM_ADDR_CMD[28]	P2
	ALERTn	Csn3	A22	MEM_ADDR_CMD[29]	N4
A3	A3	A3	A4	MEM_ADDR_CMD[3]	G2
	Csn1	Csn2	AINV	MEM_ADDR_CMD[30]	P4
	PAR	REF _n	A0	MEM_ADDR_CMD[31]	N3
A4	A4	A4	A5	MEM_ADDR_CMD[4]	H2
A5	A5	A5	A6	MEM_ADDR_CMD[5]	J2
A6	A6	A6	A7	MEM_ADDR_CMD[6]	K2
A7	A7	A7	A8	MEM_ADDR_CMD[7]	G3
A8	A8	A8	A9	MEM_ADDR_CMD[8]	J3
A9	A9	A9	A10	MEM_ADDR_CMD[9]	L3
CK_NO	CK_NO	CK_N	CK_N	MEM_CLK_N	V2
CK_PO	CK_PO	CK_P	CK_P	MEM_CLK_P	V1
DM0	LDM_n0		DINVA0	MEM_DMA[0]	B10
DM1	UDM_n0	DM1	QVLDA0	MEM_DMA[1]	C4
DM2	LDM_n1		DINVA1	MEM_DMA[2]	B17
DM3	UDM_n1		QVLDA1	MEM_DMA[3]	F17
DM4	LDM_n2	DQ18	DINVB0	MEM_DMB[0]	M16
DM5	UDM_n2		QVLDB0	MEM_DMB[1]	U16
DM6	LDM_n3	DQ0	DINVB1	MEM_DMB[2]	U11
DM7	UDM_n3		QVLDB1	MEM_DMB[3]	U6
DM8	LDM_n4			MEM_DQ_ADDR_CMD[0]	R6
DQ64	DQ64			MEM_DQ_ADDR_CMD[1]	T1
DQ65	DQ65			MEM_DQ_ADDR_CMD[2]	R2
DQ66	DQ66			MEM_DQ_ADDR_CMD[3]	T2

DDR3 x72 [DQS x8]	DDR4 x72 [DQS x8 Groups]	RLDRAM3 x36 [DQS x8/x9 Groups]	QDR IV x36 [DQS x18 Groups]	HiLo Pin Name	HiLo Pin Number
DQ67	DQ67			MEM_DQ_ADDR_CMD[4]	U2
DQ68	DQ68			MEM_DQ_ADDR_CMD[5]	U3
DQ69	DQ69		AP	MEM_DQ_ADDR_CMD[6]	T4
DQ70	DQ70		A24	MEM_DQ_ADDR_CMD[7]	U4
DQ71	DQ71		A23	MEM_DQ_ADDR_CMD[8]	T5
DQ0	DQ0		DQA0	MEM_DQA[0]	A4
DQ1	DQ1		DQA1	MEM_DQA[1]	B4
DQ10	DQ10	DQ11	DQA9	MEM_DQA[10]	C2
DQ11	DQ11	DQ12	DQA10	MEM_DQA[11]	C3
DQ12	DQ12	DQ13	DQA11	MEM_DQA[12]	E3
DQ13	DQ13	DQ14	DQA12	MEM_DQA[13]	D4
DQ14	DQ14	DQ15	DQA13	MEM_DQA[14]	D1
DQ15	DQ15	DQ16	DQA14	MEM_DQA[15]	D2
DQ16	DQ16	QVLD1	DQA18	MEM_DQA[16]	A12
DQ17	DQ17		DQA19	MEM_DQA[17]	B12
DQ18	DQ18		DQA20	MEM_DQA[18]	B13
DQ19	DQ19		DQA21	MEM_DQA[19]	B14
DQ2	DQ2		DQA2	MEM_DQA[2]	B5
DQ20	DQ20		DQA22	MEM_DQA[20]	C15
DQ21	DQ21		DQA23	MEM_DQA[21]	A16
DQ22	DQ22		DQA24	MEM_DQA[22]	B16
DQ23	DQ23		QKA_N1	MEM_DQA[23]	A18
DQ24	DQ24	DQ27	DQA25	MEM_DQA[24]	C16
DQ25	DQ25	DQ28	DQA26	MEM_DQA[25]	D16
DQ26	DQ26	DQ29	DQA27	MEM_DQA[26]	E16
DQ27	DQ27	DQ30	DQA28	MEM_DQA[27]	F16
DQ28	DQ28	DQ31	DQA29	MEM_DQA[28]	D17
DQ29	DQ29	DQ32	DQA30	MEM_DQA[29]	C18
DQ3	DQ3		DQA3	MEM_DQA[3]	B6
DQ30	DQ30	DQ33	DQA31	MEM_DQA[30]	D18
DQ31	DQ31	DQ34	DQA32	MEM_DQA[31]	E18
		DQ17	DQA15	MEM_DQA[32]	E2
		DQ35	DQA33	MEM_DQA[33]	G16
DQ4	DQ4		DQA4	MEM_DQA[4]	A8
DQ5	DQ5		DQA5	MEM_DQA[5]	B8
DQ6	DQ6		DQA6	MEM_DQA[6]	B9
DQ7	DQ7		QKA_NO	MEM_DQA[7]	A10
DQ8	DQ8	DQ9	DQA7	MEM_DQA[8]	B1
DQ9	DQ9	DQ10	DQA8	MEM_DQA[9]	B2
DQ32	DQ32	DQ19	DQB0	MEM_DQB[0]	H16
DQ33	DQ33	DQ20	DQB1	MEM_DQB[1]	J16
DQ42	DQ42		DQB9	MEM_DQB[10]	P17
DQ43	DQ43		DQB10	MEM_DQB[11]	P18
DQ44	DQ44		DQB11	MEM_DQB[12]	R18
DQ45	DQ45		DQB12	MEM_DQB[13]	T16
DQ46	DQ46		DQB13	MEM_DQB[14]	T17
DQ47	DQ47		DQB14	MEM_DQB[15]	T18
DQ48	DQ48	DQ1	DQB18	MEM_DQB[16]	I11R

DDR3 x72 [DQS x8]	DDR4 x72 [DQS x8 Groups]	RLDRAM3 x36 [DQS x8/x9 Groups]	QDR IV x36 [DQS x18 Groups]	HiLo Pin Name	HiLo Pin Number
DQ49	DQ49	DQ2	DQB19	MEM_DQB[17]	T14
DQ50	DQ50	DQ3	DQB20	MEM_DQB[18]	U14
DQ51	DQ51	DQ4	DQB21	MEM_DQB[19]	V14
DQ34	DQ34	DQ21	DQB2	MEM_DQB[2]	K16
DQ52	DQ52	DQ5	DQB22	MEM_DQB[20]	T13
DQ53	DQ53	DQ6	DQB23	MEM_DQB[21]	T12
DQ54	DQ54	DQ7	DQB24	MEM_DQB[22]	U12
DQ55	DQ55	DQ8	QKB_N1	MEM_DQB[23]	V12
DQ56	DQ56		DQB25	MEM_DQB[24]	T10
DQ57	DQ57		DQB26	MEM_DQB[25]	U10
DQ58	DQ58		DQB27	MEM_DQB[26]	V10
DQ59	DQ59		DQB28	MEM_DQB[27]	T9
DQ60	DQ60		DQB29	MEM_DQB[28]	T8
DQ61	DQ61		DQB30	MEM_DQB[29]	U8
DQ35	DQ35	DQ22	DQB3	MEM_DQB[3]	L16
DQ62	DQ62		DQB31	MEM_DQB[30]	U7
DQ63	DQ63		DQB32	MEM_DQB[31]	V6
			DQB35	MEM_DQB[32]	R16
			DQB33	MEM_DQB[33]	T6
DQ36	DQ36	DQ23	DQB4	MEM_DQB[4]	H17
DQ37	DQ37	DQ24	DQB5	MEM_DQB[5]	K17
DQ38	DQ38	DQ25	DQB6	MEM_DQB[6]	K18
DQ39	DQ39	DQ26	QKB_NO	MEM_DQB[7]	L18
DQ40	DQ40	QVLD0	DQB7	MEM_DQB[8]	M17
DQ41	DQ41		DQB8	MEM_DQB[9]	N18
DQS_N8	DQSL_N4			MEM_DQS_ADDR_CMD_N	V5
DQS_P8	DQSL_P4		FE _n	MEM_DQS_ADDR_CMD_P	V4
DQS_NO	DQSL_NO		DQA17	MEM_DQSA_N[0]	A7
DQS_N1	DQSU_N0	QK1#	DKA_NO	MEM_DQSA_N[1]	A3
DQS_N2	DQSL_N1	DK1#	DQA35	MEM_DQSA_N[2]	A15
DQS_N3	DQSU_N1	QK3#	DKA_N1	MEM_DQSA_N[3]	G18
DQS_P0	DQSL_P0		DQA16	MEM_DQSA_P[0]	A6
DQS_P1	DQSU_P0	QK1	DKA_P0	MEM_DQSA_P[1]	A2
DQS_P2	DQSL_P1	DK1	DQA34	MEM_DQSA_P[2]	A14
DQS_P3	DQSU_P1	QK3	DKA_P1	MEM_DQSA_P[3]	F18
DQS_N4	DQSL_N2	QK2#	DQB17	MEM_DQSB_N[0]	J18
DQS_N5	DQSU_N2	DK0#	DKB_NO	MEM_DQSB_N[1]	V18
DQS_N6	DQSL_N3	QK0#	DQB35	MEM_DQSB_N[2]	V17
DQS_N7	DQSU_N3		DKB_N1	MEM_DQSB_N[3]	V9
DQS_P4	DQSL_P2	QK2	DQB16	MEM_DQSB_P[0]	H18
DQS_P5	DQSU_P2	DK0	DKB_P0	MEM_DQSB_P[1]	U18
DQS_P6	DQSL_P3	QK0	DQB34	MEM_DQSB_P[2]	V16
DQS_P7	DQSU_P3		DKB_P1	MEM_DQSB_P[3]	V8
			QKA_P0	MEM_QKA_P[0]	A11
			QKA_P1	MEM_QKA_P[1]	B18
			QKB_P0	MEM_QKB_P[0]	M18
		DM0	QKB_P1	MEM_QKB_P[1]	V13

Altera Corporation, 101 innovation Dr, San Jose, CA 95134
 © 2024 Altera Corporation. All Rights Reserved.
Title Arria® 10 GX FPGA Development Kit (Non-ENP)



Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
Date: Wednesday, December 11, 2024	Sheet 16 of 49	

External Memory Interface - HiLo connector

J14A

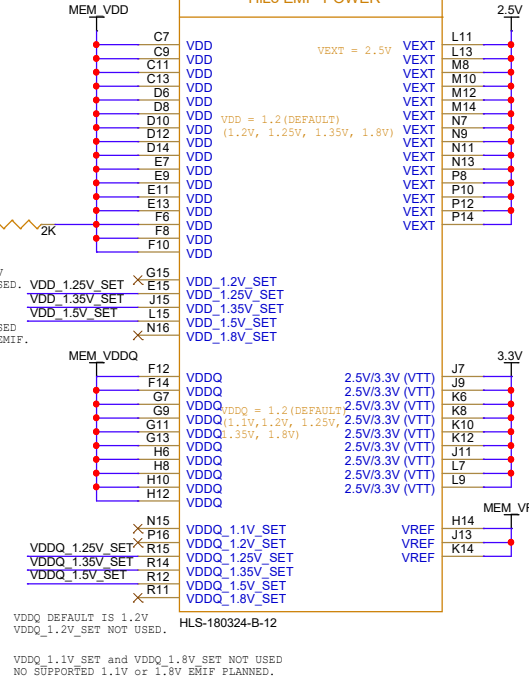
HiLo EMI - EMI SIGNALS

MEM_ADDR_CMD0	F1	MEM_ADDR_CMD0	MEM_DQ_ADDR_CMD0	R6	MEM_DQ_ADDR_CMD0	T1	MEM_DQ_ADDR_CMD0
MEM_ADDR_CMD1	H1	MEM_ADDR_CMD1	MEM_DQ_ADDR_CMD1	T1	MEM_DQ_ADDR_CMD1	R2	MEM_DQ_ADDR_CMD2
MEM_ADDR_CMD2	F2	MEM_ADDR_CMD2	MEM_DQ_ADDR_CMD2	R2	MEM_DQ_ADDR_CMD2	T2	MEM_DQ_ADDR_CMD3
MEM_ADDR_CMD3	G2	MEM_ADDR_CMD3	MEM_DQ_ADDR_CMD3	U2	MEM_DQ_ADDR_CMD4	U3	MEM_DQ_ADDR_CMD5
MEM_ADDR_CMD4	H2	MEM_ADDR_CMD4	MEM_DQ_ADDR_CMD4	T4	MEM_DQ_ADDR_CMD6	U4	MEM_DQ_ADDR_CMD7
MEM_ADDR_CMD5	J2	MEM_ADDR_CMD5	MEM_DQ_ADDR_CMD5	T5	MEM_DQ_ADDR_CMD8	V4	MEM_DQS_ADDR_CMD_P
MEM_ADDR_CMD6	K2	MEM_ADDR_CMD6	MEM_DQ_ADDR_CMD6	V1	MEM_CLK_P	V2	MEM_CLK_N
MEM_ADDR_CMD7	G3	MEM_ADDR_CMD7	MEM_DQ_ADDR_CMD7	L6	MEM_CLK_P	M6	MEM_CLK_N
MEM_ADDR_CMD8	J3	MEM_ADDR_CMD8	MEM_DQ_ADDR_CMD8	CONFIG0		CONFIG1	
MEM_ADDR_CMD9	L3	MEM_ADDR_CMD9	MEM_DQ_ADDR_CMD9	RFU0		RFU1	
MEM_ADDR_CMD10	H4	MEM_ADDR_CMD10	MEM_DQS_ADDR_CMD_P	RFU2		RFU3	
MEM_ADDR_CMD11	F4	MEM_ADDR_CMD11	MEM_DQS_ADDR_CMD_N	RFU4		RFU5	
MEM_ADDR_CMD12	G4	MEM_ADDR_CMD12		RFU6			
MEM_ADDR_CMD13	H4	MEM_ADDR_CMD13					
MEM_ADDR_CMD14	J4	MEM_ADDR_CMD14					
MEM_ADDR_CMD15	K4	MEM_ADDR_CMD15					
MEM_ADDR_CMD16	M1	MEM_ADDR_CMD16					
MEM_ADDR_CMD17	N2	MEM_ADDR_CMD17					
MEM_ADDR_CMD18	N2	MEM_ADDR_CMD18					
MEM_ADDR_CMD19	L4	MEM_ADDR_CMD19					
MEM_ADDR_CMD20	P5	MEM_ADDR_CMD20					
MEM_ADDR_CMD21	M5	MEM_ADDR_CMD21					
MEM_ADDR_CMD22	P1	MEM_ADDR_CMD22					
MEM_ADDR_CMD23	R4	MEM_ADDR_CMD23					
MEM_ADDR_CMD24	M4	MEM_ADDR_CMD24					
MEM_ADDR_CMD25	R4	MEM_ADDR_CMD25					
MEM_ADDR_CMD26	L2	MEM_ADDR_CMD26					
MEM_ADDR_CMD27	K1	MEM_ADDR_CMD27					
MEM_ADDR_CMD28	P2	MEM_ADDR_CMD28					
MEM_ADDR_CMD29	N4	MEM_ADDR_CMD29					
MEM_ADDR_CMD30	P4	MEM_ADDR_CMD30					
MEM_ADDR_CMD31	N3	MEM_ADDR_CMD31					
MEM_DMA0	B10	MEM_DMA0	MEM_DMB0	M16	MEM_DMB0	U16	MEM_DMB1
MEM_DMA1	C4	MEM_DMA1	MEM_DMB1	U11	MEM_DMB2	U6	MEM_DMB3
MEM_DMA2	B17	MEM_DMA2	MEM_DMB2				
MEM_DMA3	F17	MEM_DMA3	MEM_DMB3				
MEM_DQA0	A4	MEM_DQA0	MEM_DQB0	H16	MEM_DQB0	K16	MEM_DQB1
MEM_DQA1	B4	MEM_DQA1	MEM_DQB1	K16	MEM_DQB1	L16	MEM_DQB2
MEM_DQA2	B5	MEM_DQA2	MEM_DQB2	L16	MEM_DQB2	H17	MEM_DQB3
MEM_DQA3	B6	MEM_DQA3	MEM_DQB3	H17	MEM_DQB3	K17	MEM_DQB4
MEM_DQA4	A8	MEM_DQA4	MEM_DQB4	K17	MEM_DQB4	L18	MEM_DQB5
MEM_DQA5	B8	MEM_DQA5	MEM_DQB5	L18	MEM_DQB5	H18	MEM_DQB6
MEM_DQA6	B9	MEM_DQA6	MEM_DQB6	H18	MEM_DQB6	K18	MEM_DQB7
MEM_DQA7	A10	MEM_DQA7	MEM_DQB7	K18	MEM_DQB7	L18	MEM_DQB8
MEM_DQA8	B1	MEM_DQA8	MEM_DQB8	L18	MEM_DQB8	H18	MEM_DQB9
MEM_DQA9	B2	MEM_DQA9	MEM_DQB9	H18	MEM_DQB9	K17	MEM_DQB10
MEM_DQA10	C2	MEM_DQA10	MEM_DQB10	K17	MEM_DQB10	L18	MEM_DQB11
MEM_DQA11	C3	MEM_DQA11	MEM_DQB11	L18	MEM_DQB11	H18	MEM_DQB12
MEM_DQA12	E3	MEM_DQA12	MEM_DQB12	H18	MEM_DQB12	K17	MEM_DQB13
MEM_DQA13	D4	MEM_DQA13	MEM_DQB13	K17	MEM_DQB13	L17	MEM_DQB14
MEM_DQA14	D1	MEM_DQA14	MEM_DQB14	L17	MEM_DQB14	H18	MEM_DQB15
MEM_DQA15	A12	MEM_DQA15	MEM_DQB15	H18	MEM_DQB15	K17	MEM_DQB16
MEM_DQA16	A12	MEM_DQA16	MEM_DQB16	K17	MEM_DQB16	L14	MEM_DQB17
MEM_DQA17	B12	MEM_DQA17	MEM_DQB17	L14	MEM_DQB17	U14	MEM_DQB18
MEM_DQA18	B13	MEM_DQA18	MEM_DQB18	U14	MEM_DQB18	T13	MEM_DQB19
MEM_DQA19	B14	MEM_DQA19	MEM_DQB19	T13	MEM_DQB19	T12	MEM_DQB20
MEM_DQA20	C15	MEM_DQA20	MEM_DQB20	U12	MEM_DQB21	V12	MEM_DQB22
MEM_DQA21	A16	MEM_DQA21	MEM_DQB21	V12	MEM_DQB22	T10	MEM_DQB23
MEM_DQA22	B16	MEM_DQA22	MEM_DQB22	T10	MEM_DQB23	U10	MEM_DQB24
MEM_DQA23	A18	MEM_DQA23	MEM_DQB23	U10	MEM_DQB24	V10	MEM_DQB25
MEM_DQA24	C16	MEM_DQA24	MEM_DQB24	V10	MEM_DQB25	T9	MEM_DQB26
MEM_DQA25	D16	MEM_DQA25	MEM_DQB25	T9	MEM_DQB26	U8	MEM_DQB27
MEM_DQA26	E16	MEM_DQA26	MEM_DQB26	U8	MEM_DQB27	T8	MEM_DQB28
MEM_DQA27	F16	MEM_DQA27	MEM_DQB27	T8	MEM_DQB28	U8	MEM_DQB29
MEM_DQA28	D17	MEM_DQA28	MEM_DQB28	U7	MEM_DQB29	V6	MEM_DQB30
MEM_DQA29	C18	MEM_DQA29	MEM_DQB29	V6	MEM_DQB30	R16	MEM_DQB31
MEM_DQA30	D18	MEM_DQA30	MEM_DQB30	R16	MEM_DQB31	T6	MEM_DQB32
MEM_DQA31	E18	MEM_DQA31	MEM_DQB31	T6	MEM_DQB32		
MEM_DQA32	E2	MEM_DQA32	MEM_DQB32				
MEM_DQA33	G16	MEM_DQA33	MEM_DQB33				
MEM_DQSA_P0	A6	MEM_DQSA_P0	MEM_DQSB_P0	H18	MEM_DQSB_P0	J18	MEM_DQSB_N0
MEM_DQSA_N0	A7	MEM_DQSA_N0	MEM_DQSB_N0	J18	MEM_DQSB_N0	U18	MEM_DQSB_P1
MEM_DQSA_P1	A2	MEM_DQSA_P1	MEM_DQSB_P1	U18	MEM_DQSB_P1	V18	MEM_DQSB_N1
MEM_DQSA_N1	A3	MEM_DQSA_N1	MEM_DQSB_N1	V18	MEM_DQSB_N1	V17	MEM_DQSB_P2
MEM_DQSA_P2	A14	MEM_DQSA_P2	MEM_DQSB_P2	V17	MEM_DQSB_P2	V17	MEM_DQSB_N2
MEM_DQSA_N2	A15	MEM_DQSA_N2	MEM_DQSB_N2	V17	MEM_DQSB_N2	V8	MEM_DQSB_P3
MEM_DQSA_P3	F18	MEM_DQSA_P3	MEM_DQSB_P3	V8	MEM_DQSB_P3	V9	MEM_DQSB_N3
MEM_DQSA_N3	G18	MEM_DQSA_N3	MEM_DQSB_N3	V9	MEM_DQSB_N3		
MEM_OKA_P0	A11	MEM_OKA_P0	MEM_OKB_N0	M18	MEM_OKB_P0		
MEM_OKA_N1	B18	MEM_OKA_N1	MEM_OKB_N1	V13	MEM_OKB_P1		

HLS-180324-B-12

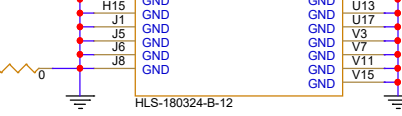
J14B

HiLo EMI - POWER

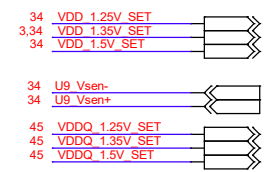


J14C

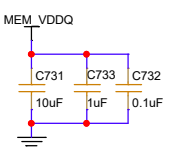
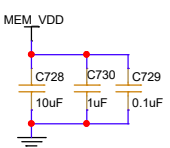
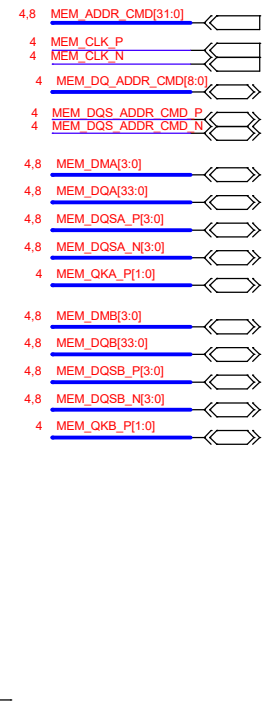
HiLo EMI - GND



POWER CONTROL



MEMORY INTERFACE



Note: Place R1113 and R1114 near to U9 VR

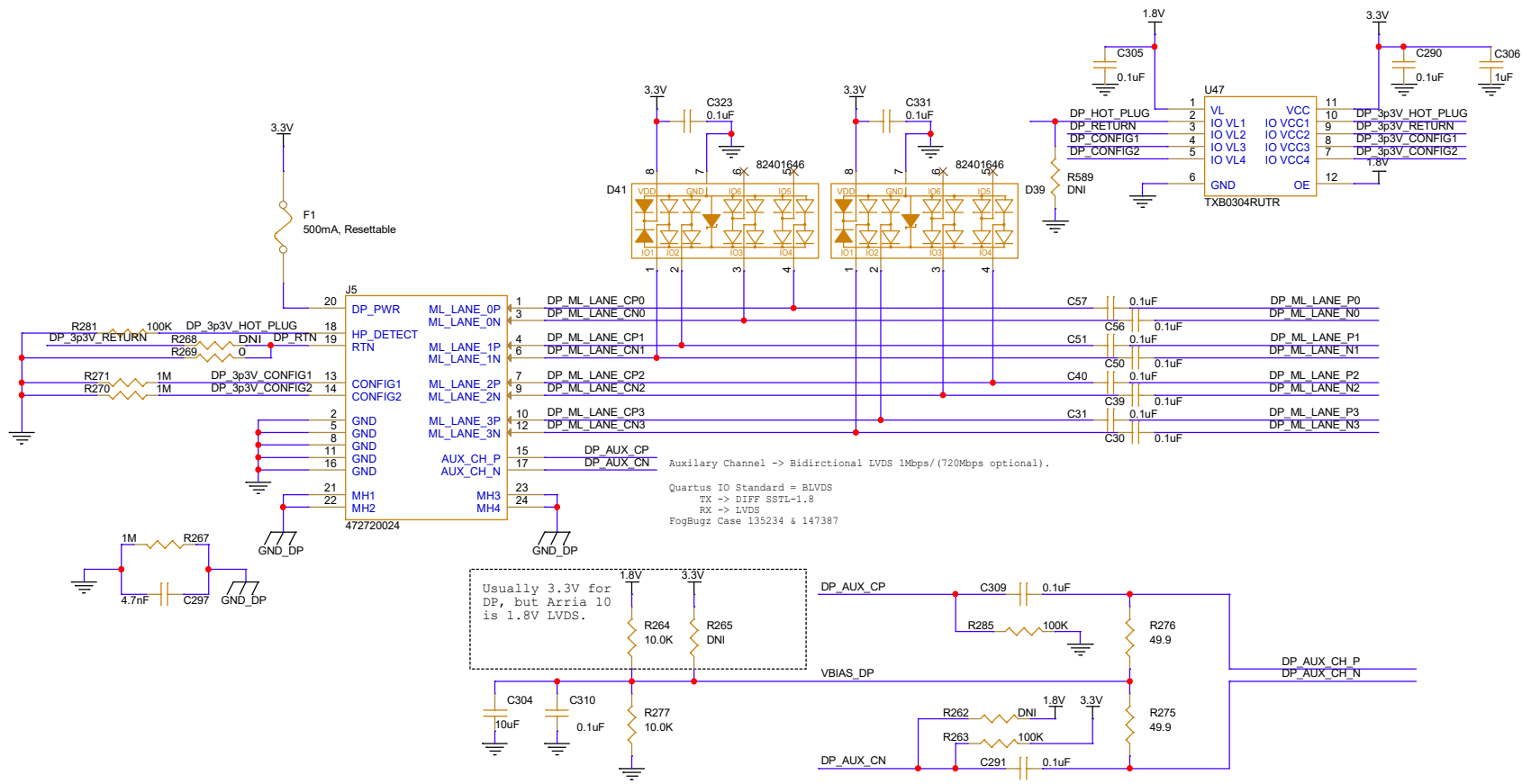
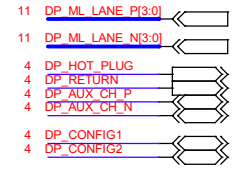


Altera Corporation, 101 Innovation Dr., San Jose, CA 95134
 © 2024 Altera Corporation. All Rights Reserved.
Title: Arria® 10 GX FPGA Development Kit (Non-ENP)

Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
Date: Wednesday, December 11, 2024	Sheet 17	of 49

Display Port (x4)

DISPLAYPORT INTERFACE



Auxiliary Channel -> Bidirectional LVDS 1Mbps/(720Mbps optional).
 Quartus IO Standard = BLVDS
 TX -> DIFF SSTL-1.8
 RX -> LVDS
 FogBugz Case 135234 & 147387

Usually 3.3V for DP, but Arria 10 is 1.8V LVDS.

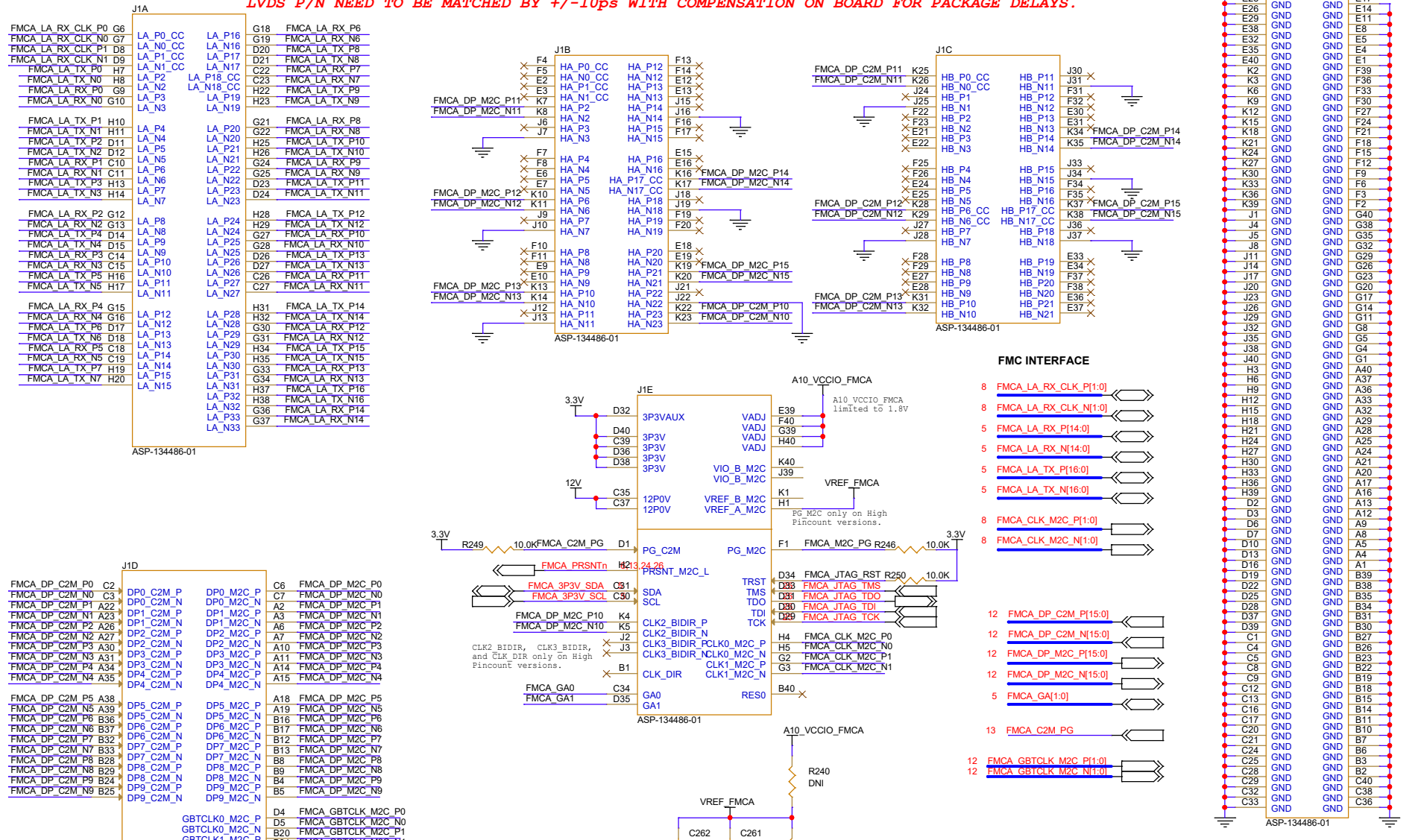
- 1) TX uses diff sstl18 configuration, which is able to meet peak-to-peak differential voltage and common mode voltage spec for DP.
- 2) RX uses LVDS input, but user need to ensure pin voltage at NF receiver end is <1.9v.
 - a. If the channel is AC couple, then user need to choose the correct Vbias_RX so that Vpin < 1.9v. The spec is 0 - 2v, which is quite wide. Selecting Vbias_Rx at 2v region will cause NF device to have reliability issue.
 - b. If the channel is DC couple, user need to make sure TX common mode voltage + ground reference differences between Tx and Rx will not cause Vpin for NF to be higher than 1.9v.



Altera Corporation, 101 innovation Dr, San Jose, CA 95134 © 2024 Altera Corporation. All Rights Reserved.		
Title Arria® 10 GX FPGA Development Kit (Non-ENP)		
Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
Date: Wednesday, December 11, 2024	Sheet 18	of 49

FMC Port A

LVDS P/N NEED TO BE MATCHED BY +/-10ps WITH COMPENSATION ON BOARD FOR PACKAGE DELAYS.



Altera Corporation, 101 innovation Dr, San Jose, CA 95134
 © 2024 Altera Corporation. All Rights Reserved.
Arria® 10 GX FPGA Development Kit (Non-ENP)



Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
Date: Wednesday, December 11, 2024	Sheet 19	of 49

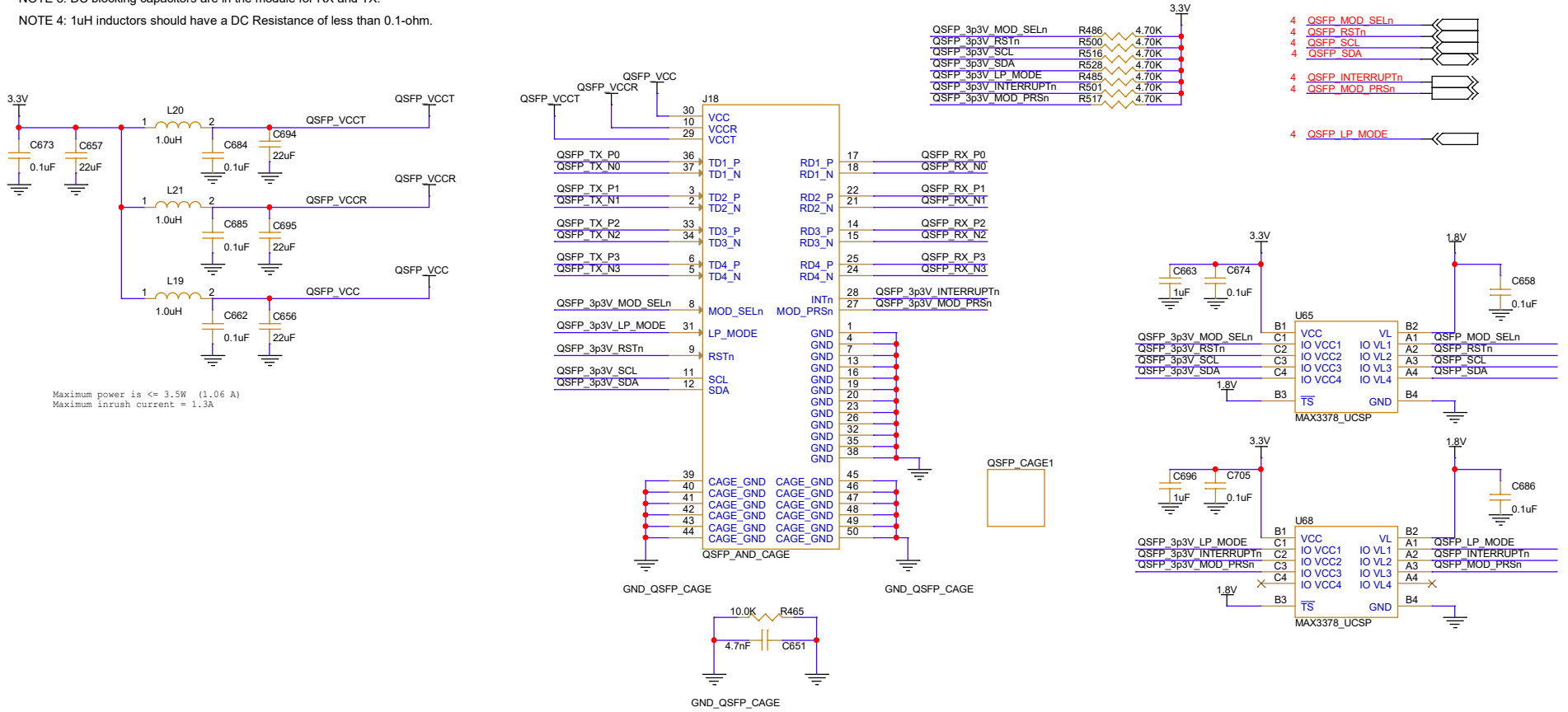
Quad Small Form-factor Pluggable (QSFP) Interface

NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

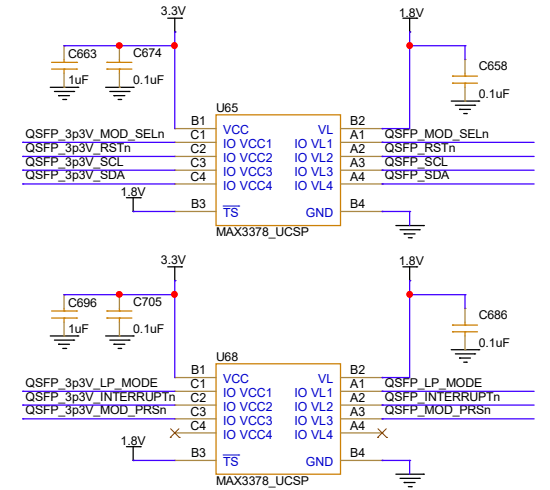
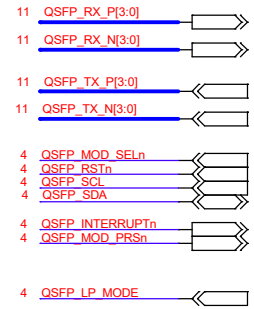
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

NOTE 3: DC blocking capacitors are in the module for RX and TX.

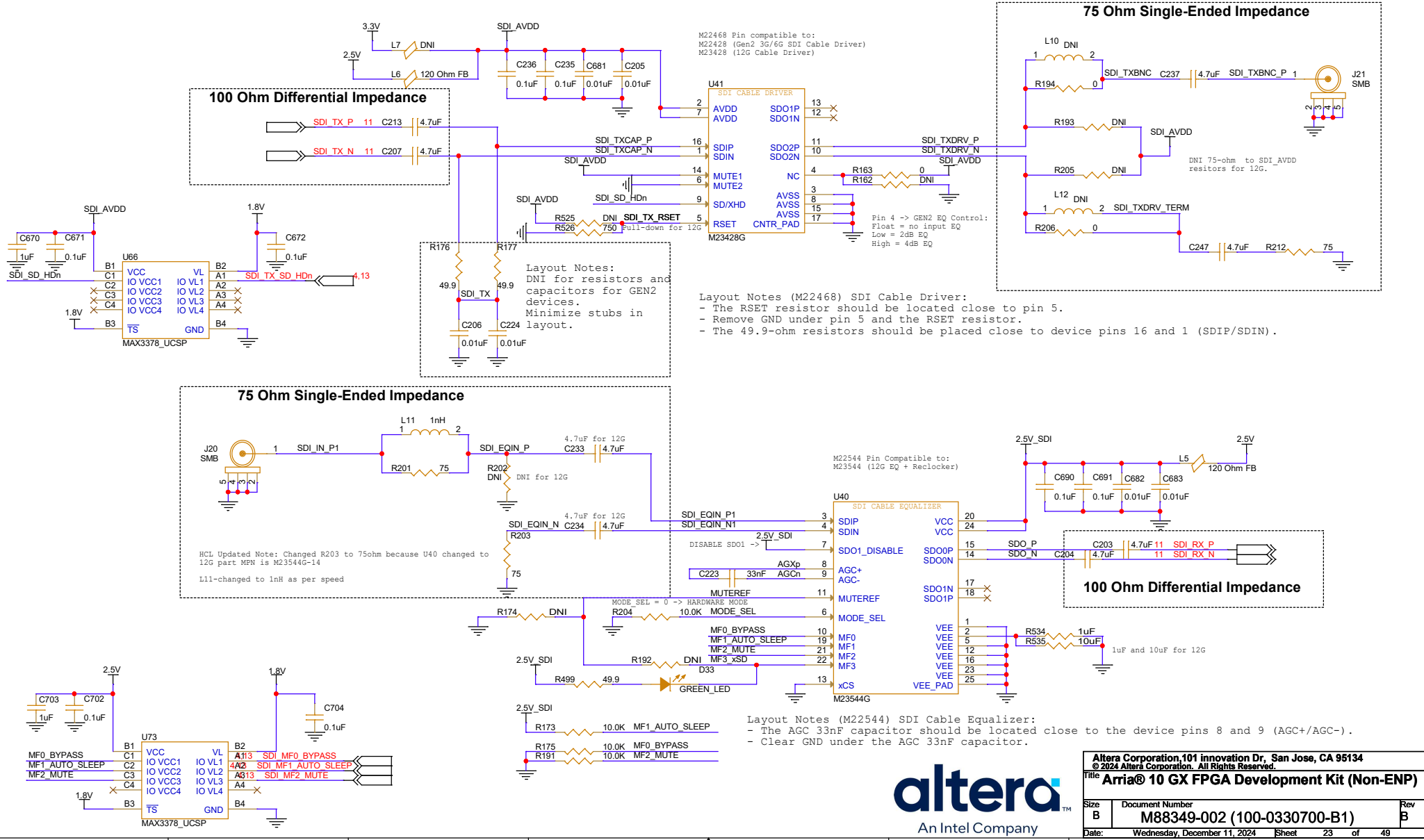
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



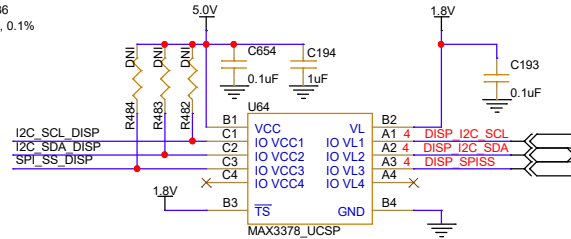
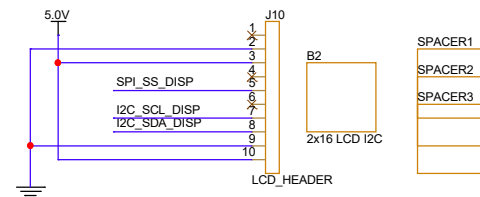
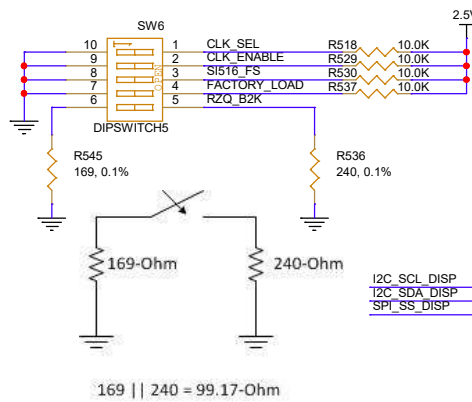
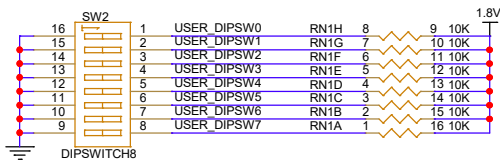
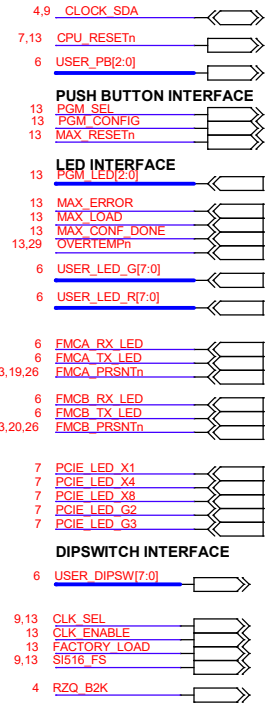
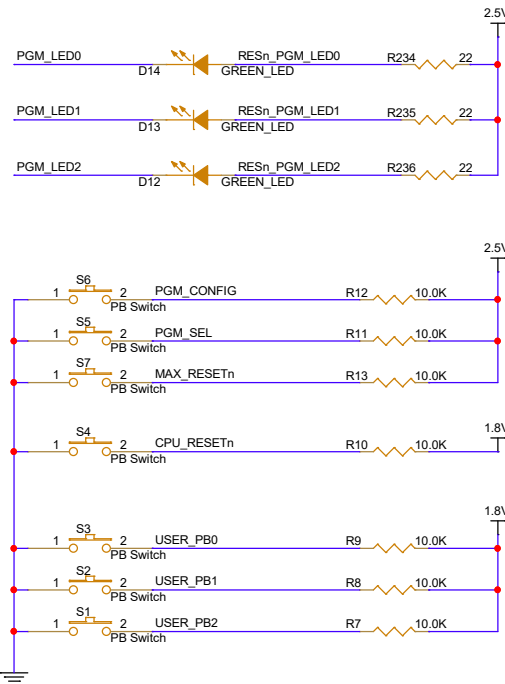
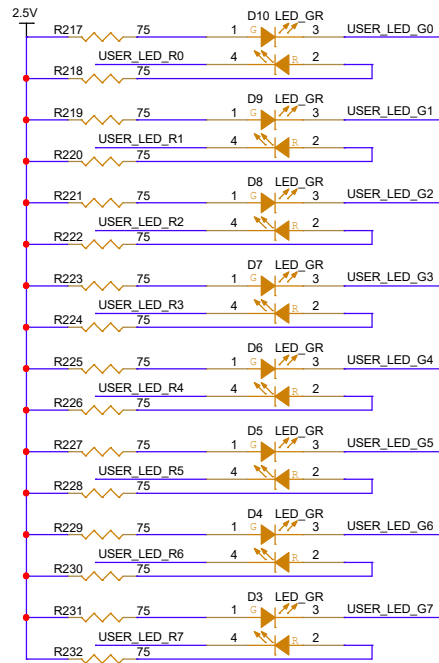
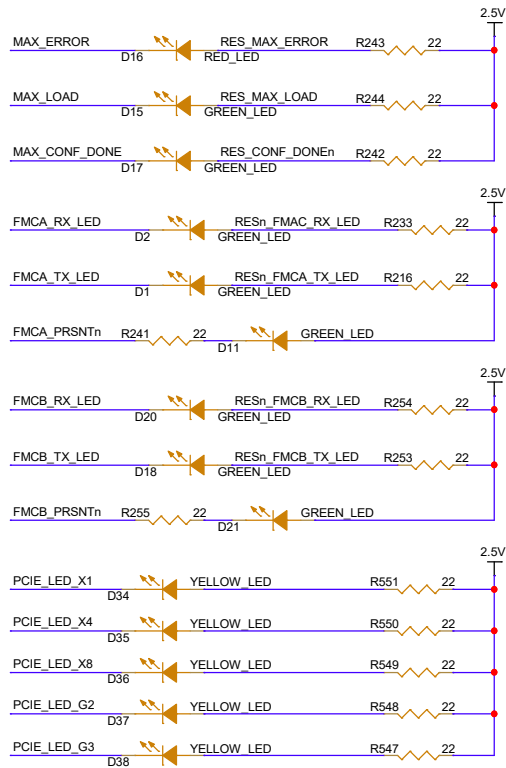
QSFP INTERFACE



SDI Cable Driver, Equalizer, and SMB

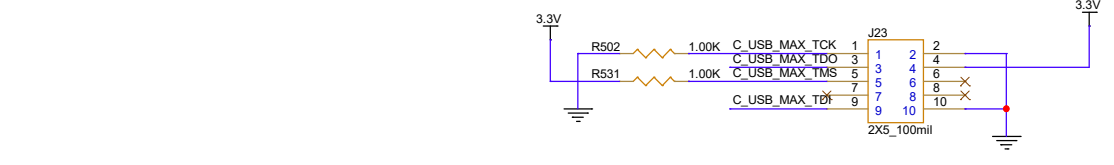
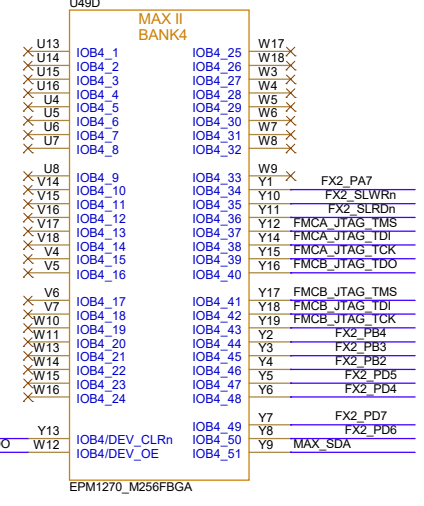
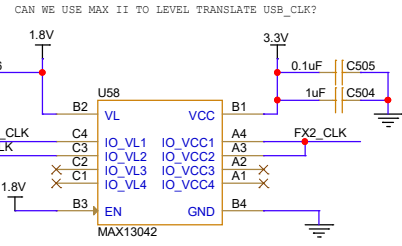
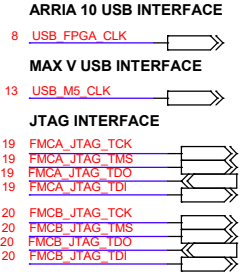
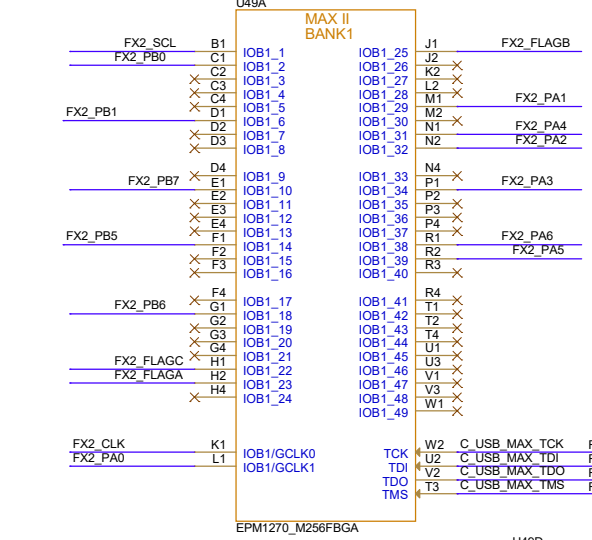
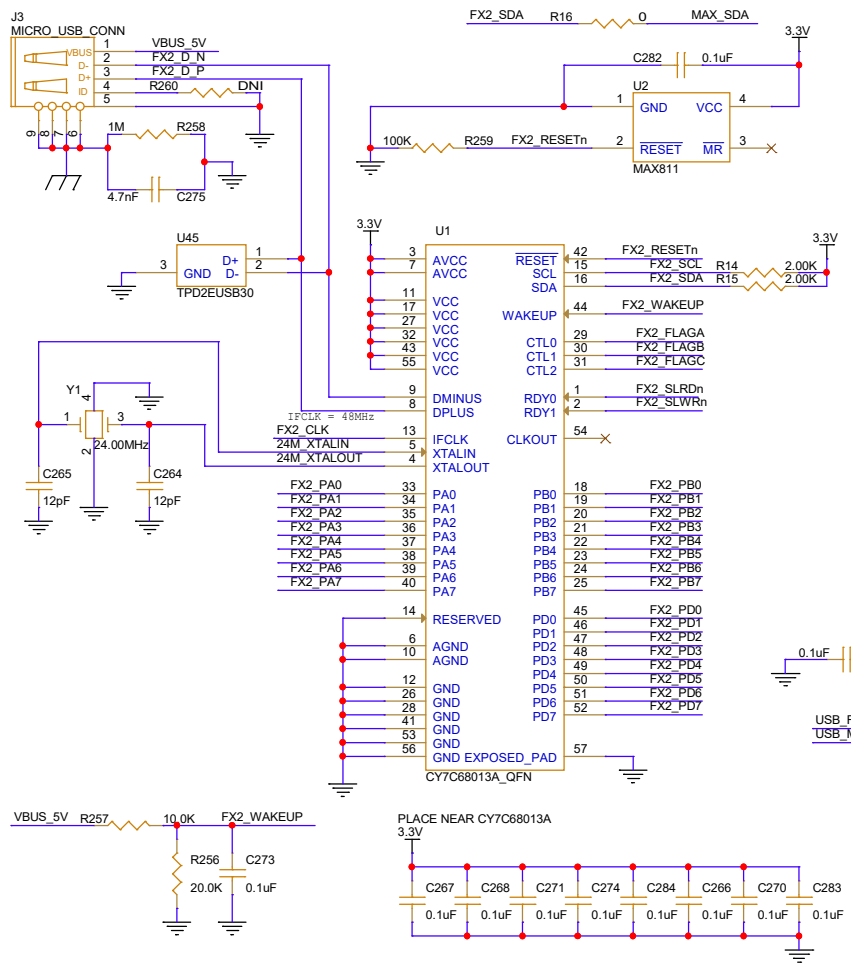


User I/O



Altera Corporation, 101 innovation Dr., San Jose, CA 95134		
© 2024 Altera Corporation. All Rights Reserved.		
Title Arria® 10 GX FPGA Development Kit (Non-ENP)		
Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
Date: Wednesday, December 11, 2024	Sheet 24	of 49

On-Board USB Blaster II - Part 1

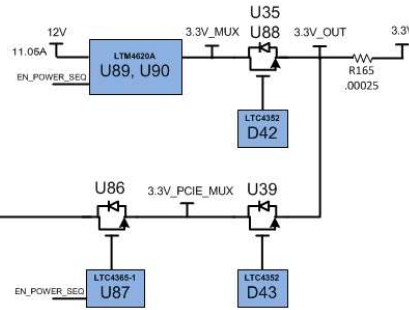
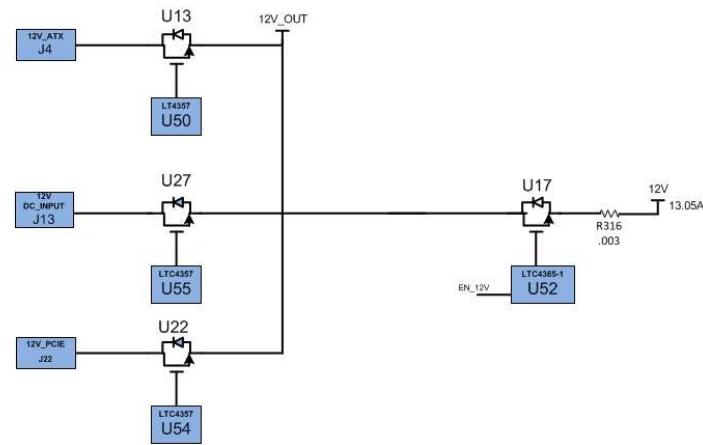


Altera Corporation, 101 innovation Dr, San Jose, CA 95134
 © 2024 Altera Corporation. All Rights Reserved.

Title Arria® 10 GX FPGA Development Kit (Non-ENP)

Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
Date: Wednesday, December 11, 2024	Sheet 25 of 49	

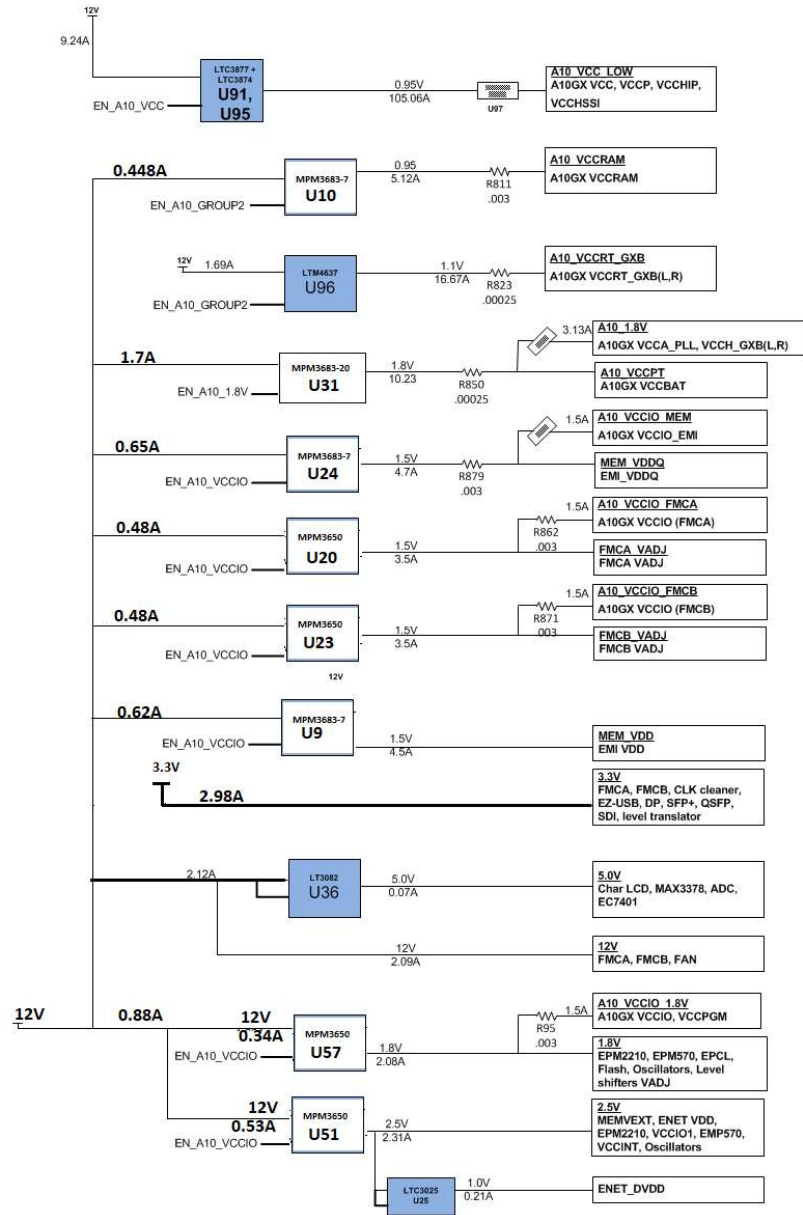
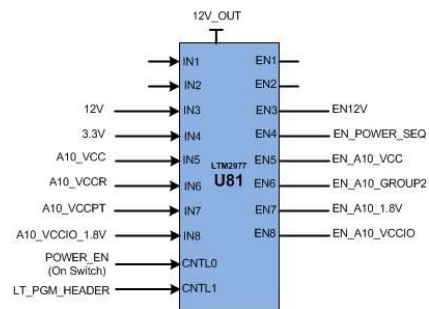
Power Tree



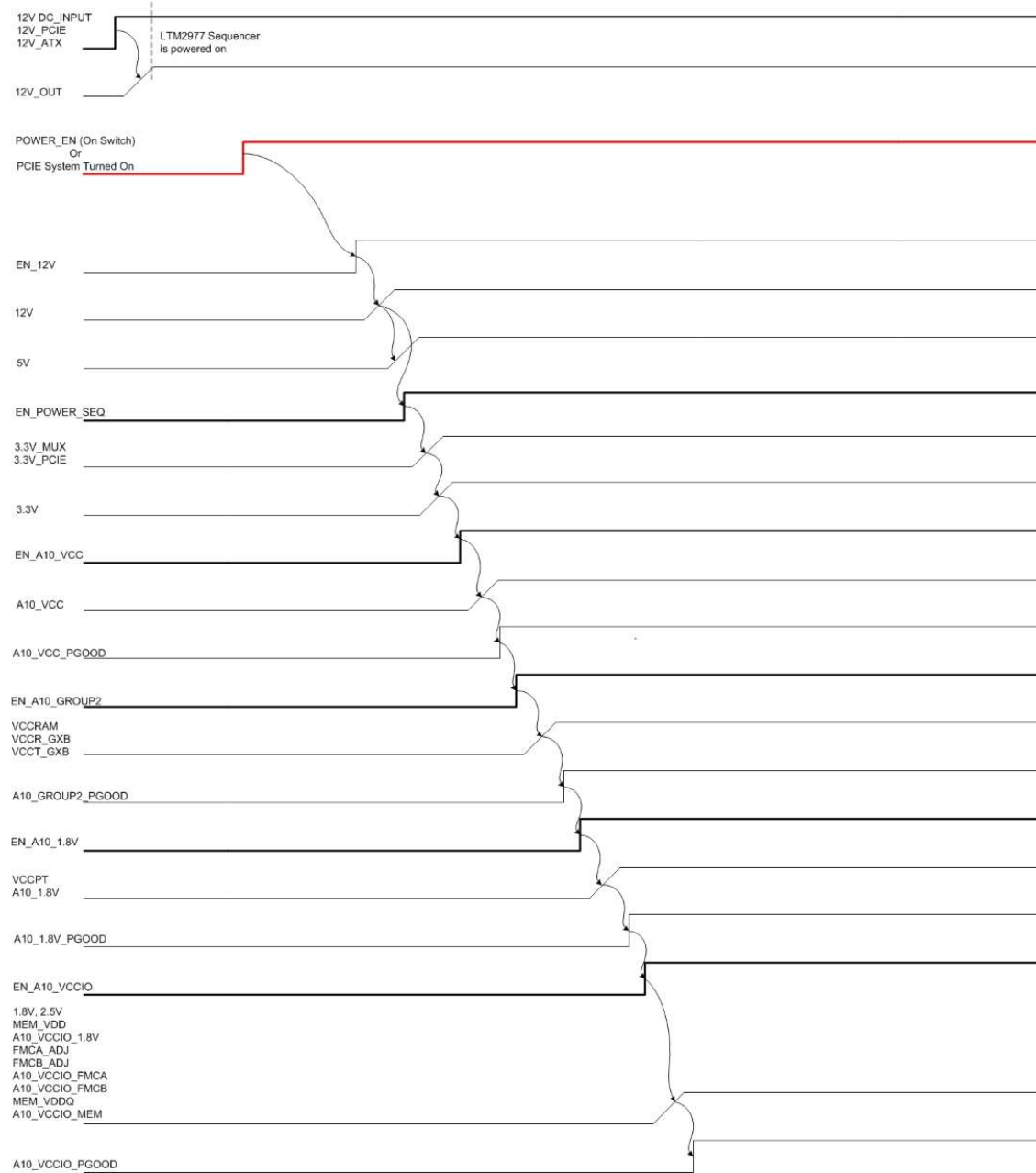
- Power UP Sequencing:
- 1) EN_12V
 - 2) EN_POWER_SEQ
 - 3) EN_A10_VCC
 - 4) EN_A10_GROUP2
 - 5) EN_A10_1.8V
 - 6) EN_A10_VCCIO

- Power DOWN Sequencing:
- 1) DISABLE A10_VCCIO
 - 2) DISABLE A10_1.8V
 - 3) DISABLE A10_GROUP2
 - 4) DISABLE A10_VCC
 - 5) DISABLE POWER_SEQ
 - 6) DISABLE 12V

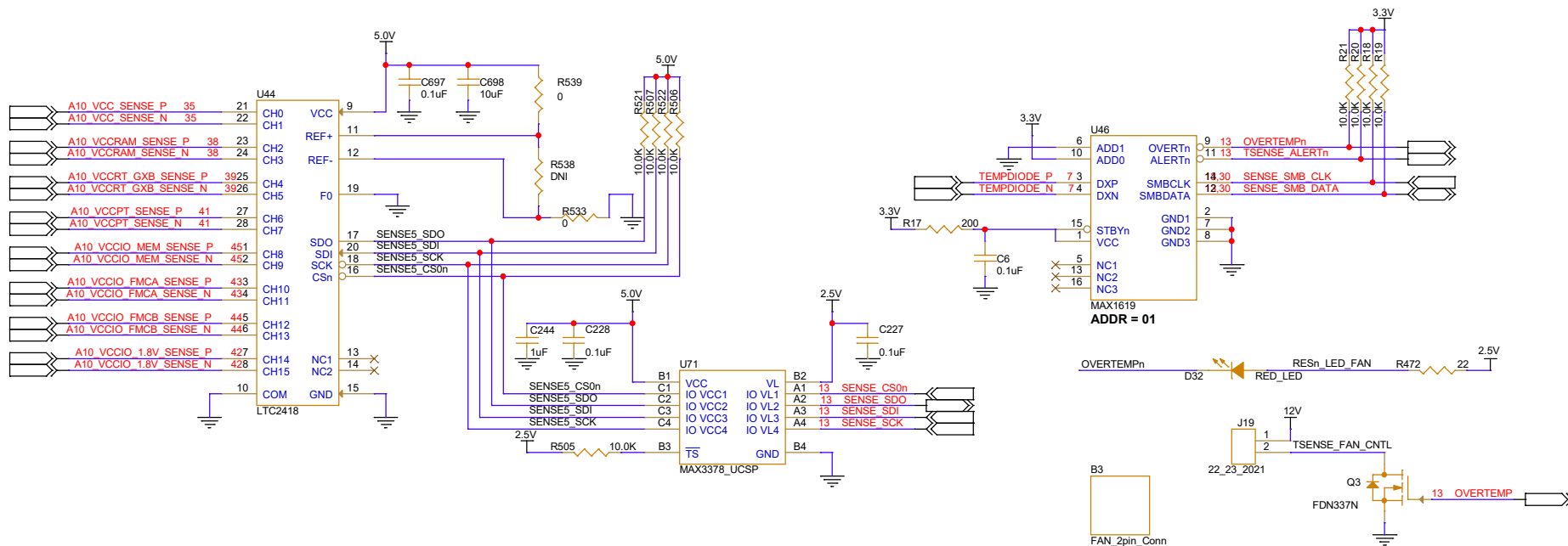
PCIe Component Height Restrictions:
 -Top Side (Max): 14.47mm
 -Bottom Side (Max) 2.67mm



Power-On Sequencing (Power-Off is reverse of Power-On)

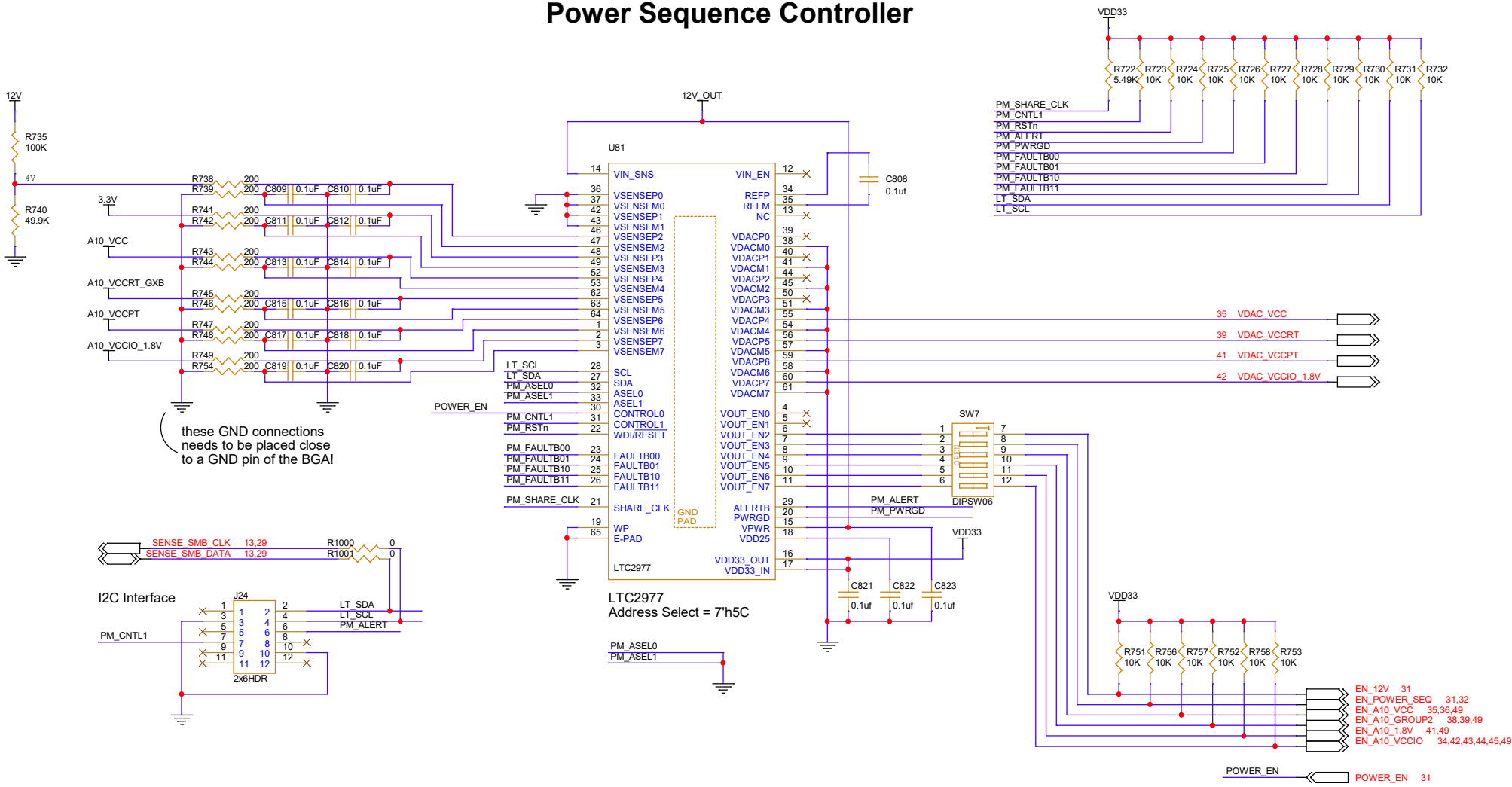


Voltage & Temp Sense



Altera Corporation, 101 Innovation Dr., San Jose, CA 95134 © 2024 Altera Corporation. All Rights Reserved.		
Title: Arria® 10 GX FPGA Development Kit (Non-ENP)		
Size: B	Document Number: M88349-002 (100-0330700-B1)	Rev: B
Date: Wednesday, December 11, 2024	Sheet: 29	of 49

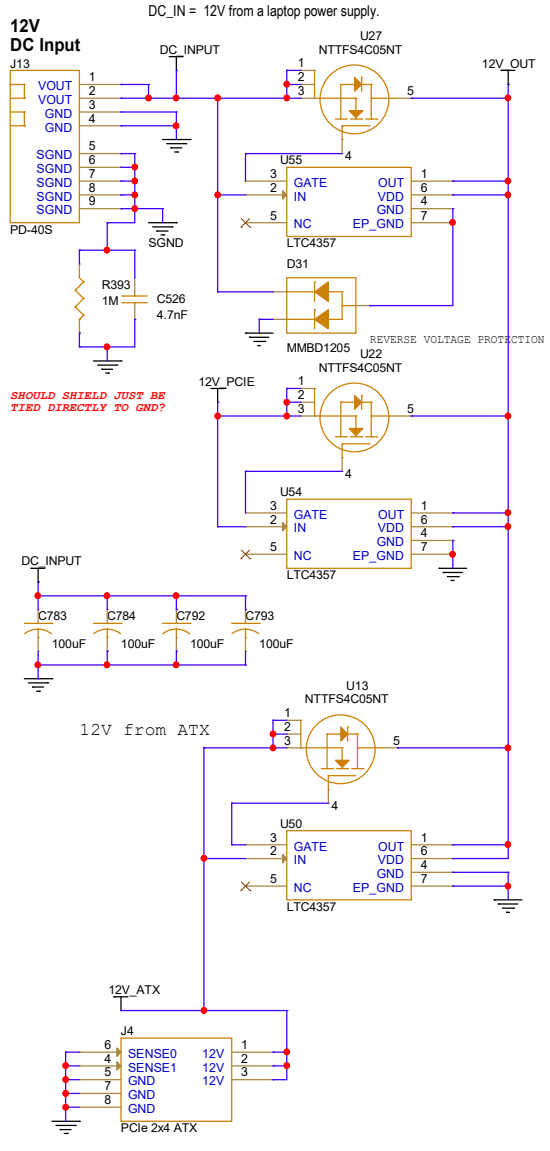
Power Sequence Controller



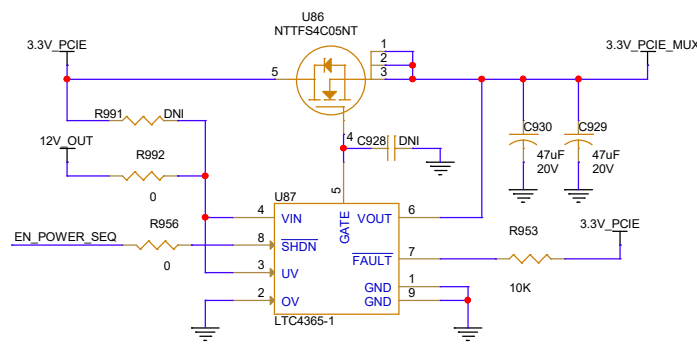
these GND connections needs to be placed close to a GND pin of the BGA!



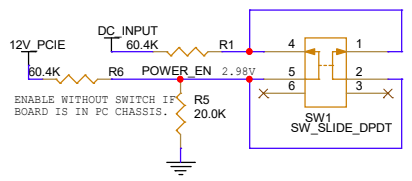
Power - Select Power Input



Sense0 = GND
Sense1 = GND
A 2 x 4 auxiliary power connector is plugged into the card. The card can draw up to 150 W from the auxiliary power connector.

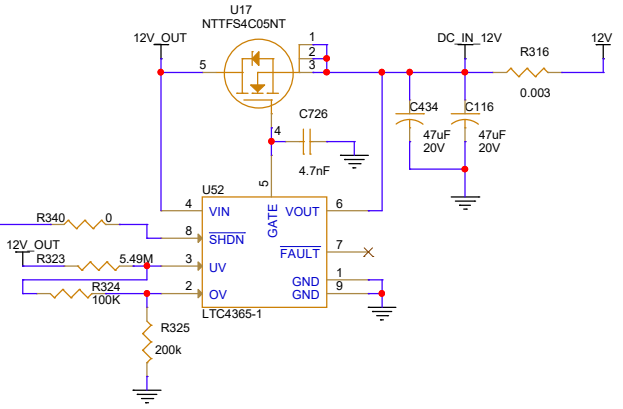


Power On Switch



ENABLE WITHOUT SWITCH IF BOARD IS IN PC CHASSIS.

- 30 EN_12V
- 30.32 EN_POWER_SEQ
- 30 POWER_EN



DC_IN -> 12V (Laptop Supply)	12V_PCIE ATX (2x4 ATX)	DC_IN ATX (Voltage Selected by LTC4357)
12V	12V	12V from 12V ATX IN
12V	0V	12V from DC_IN->12V
0V	12V	12V from 12V ATX IN



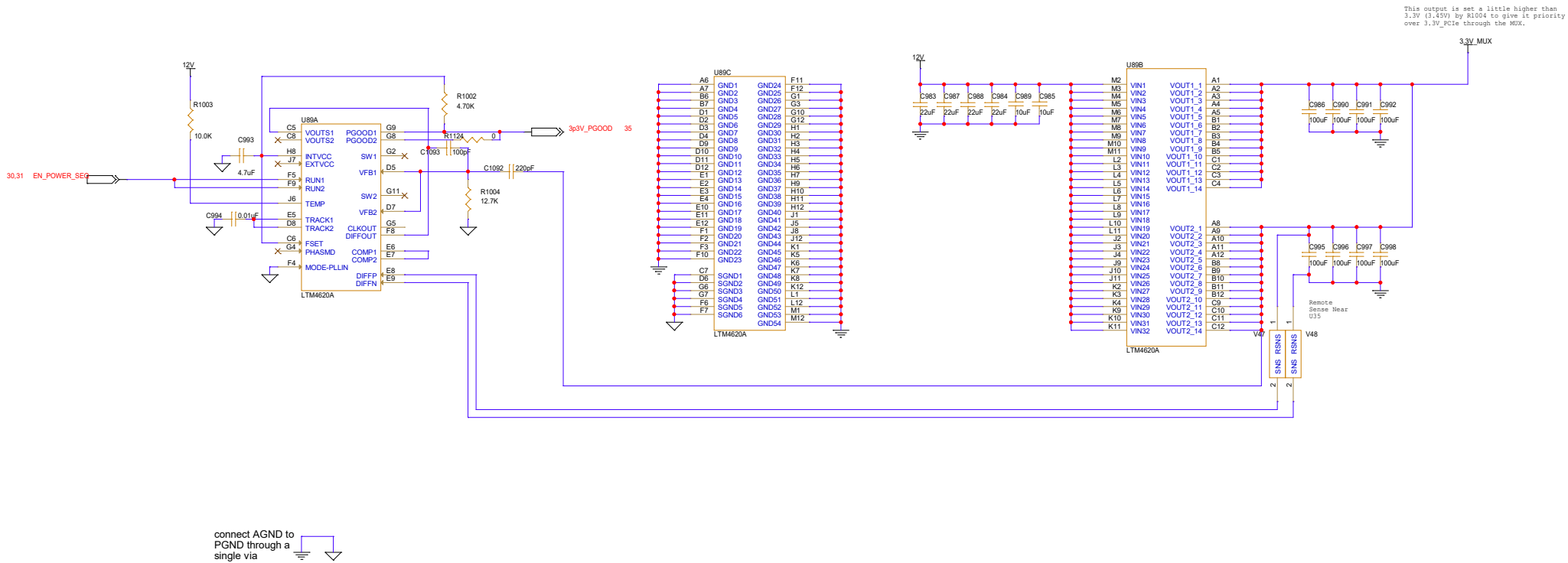
Altera Corporation, 101 innovation Dr, San Jose, CA 95134
© 2024 Altera Corporation. All Rights Reserved.

Title **Arria® 10 GX FPGA Development Kit (Non-ENP)**

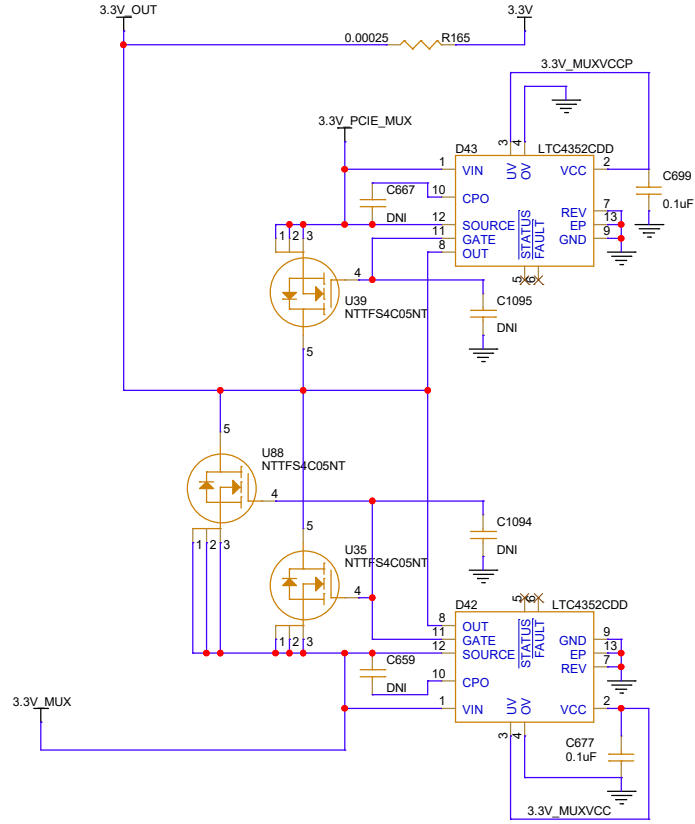
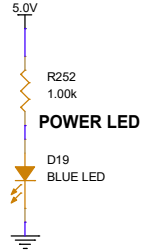
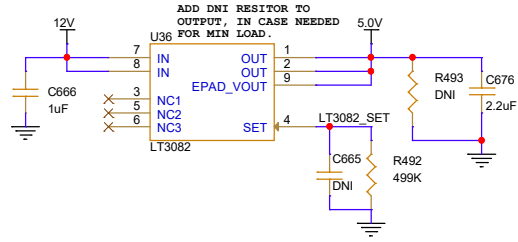
Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
--------	--	-------

Date: Wednesday, December 11, 2024 Sheet 31 of 49

Power - 12V to 3.3V



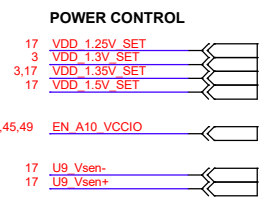
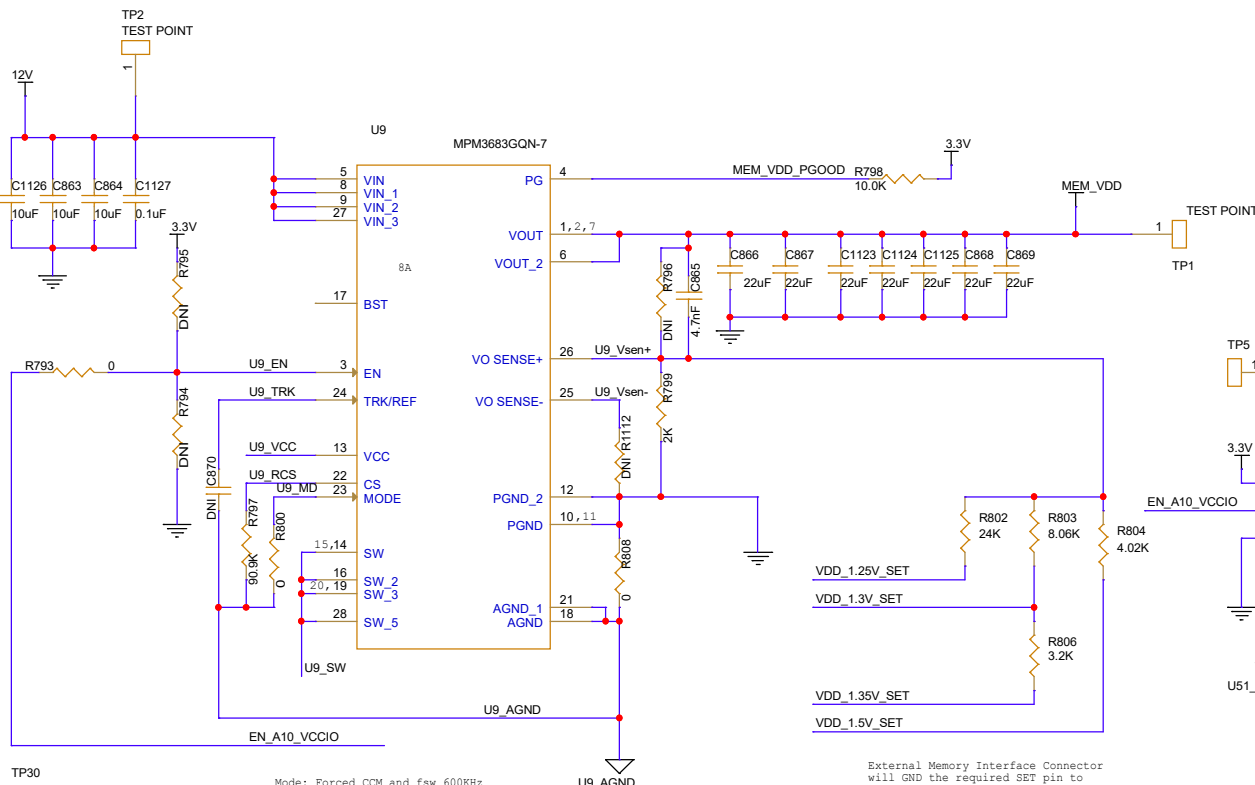
Power 1 - DC Input to 3.3V Output



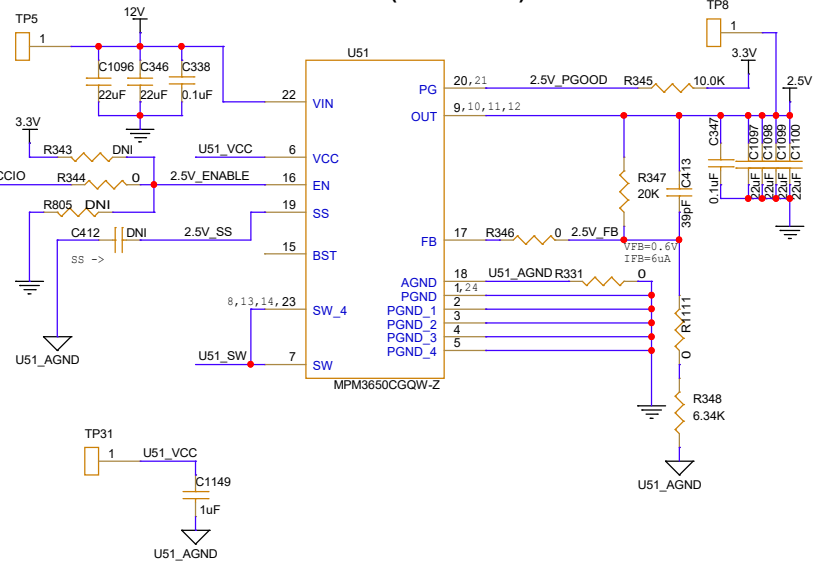
altera
An Intel Company

Altera Corporation, 101 Innovation Dr., San Jose, CA 95134		
© 2024 Altera Corporation. All Rights Reserved.		
Title: Arria® 10 GX FPGA Development Kit (Non-ENP)		
Size: B	Document Number: M88349-002 (100-0330700-B1)	Rev: B
Date: Wednesday, December 11, 2024	Sheet: 33	of 49

Power - MEM_VDD, 2.5V



Arria 10 2.5V (2.5V/2.307A)



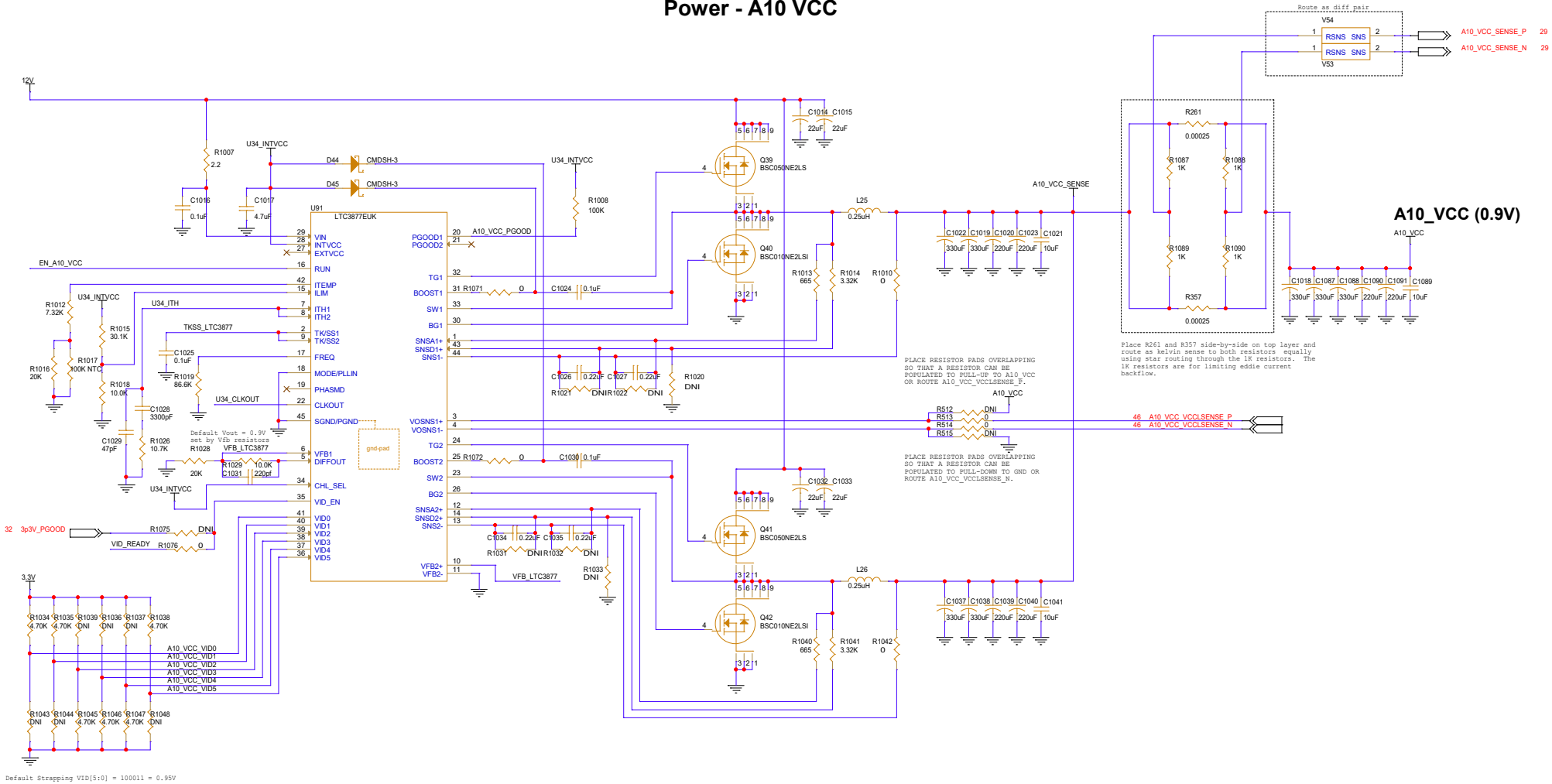
External Memory Interface Connector will GND the required SET pin to generate VDDQ voltage for memory interface. The default value is 1.2V.

Mode: Forced CCM and fsw 600KHz
 Current Limit Condition: VIN=12V, VOUT=1.2V to 1.5V, ILIM=8A, fsw=600KHz

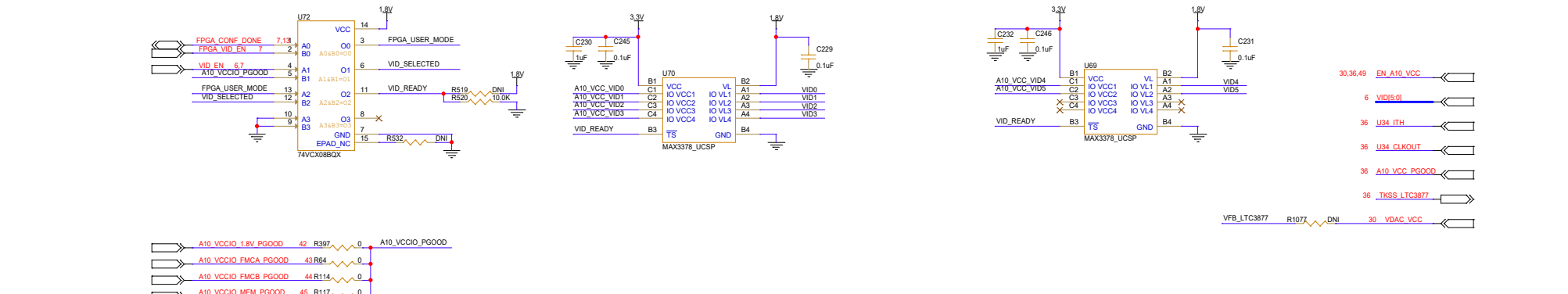


Altera Corporation, 101 innovation Dr., San Jose, CA 95134			
© 2024 Altera Corporation. All Rights Reserved.			
Title Arria® 10 GX FPGA Development Kit (Non-ENP)			
Size B	Document Number M88349-002 (100-0330700-B1)	Rev B	
Date: Wednesday, December 11, 2024	Sheet 34	of 49	

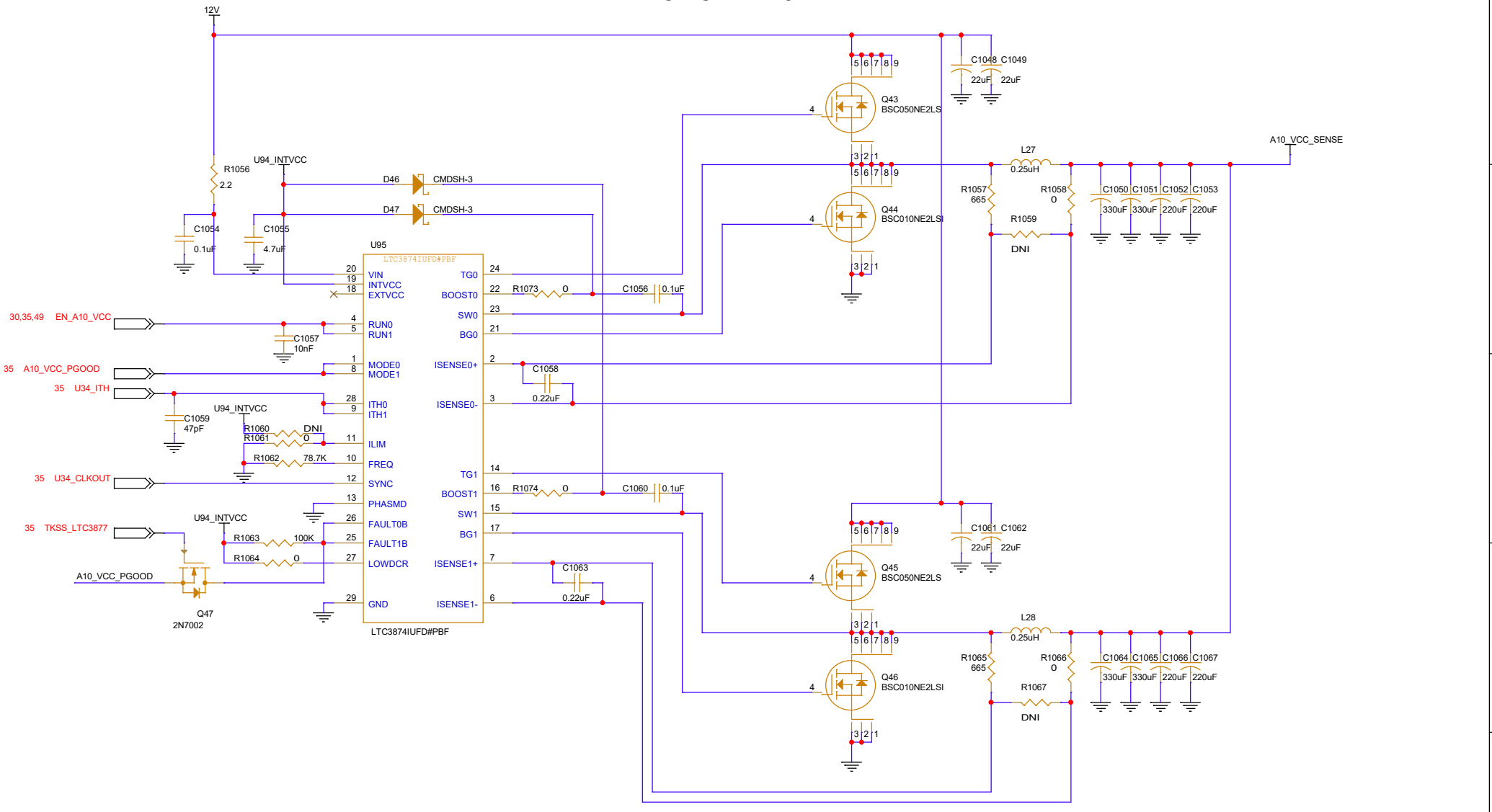
Power - A10 VCC



A10_VCC (0.9V)



Power - A10 VCC



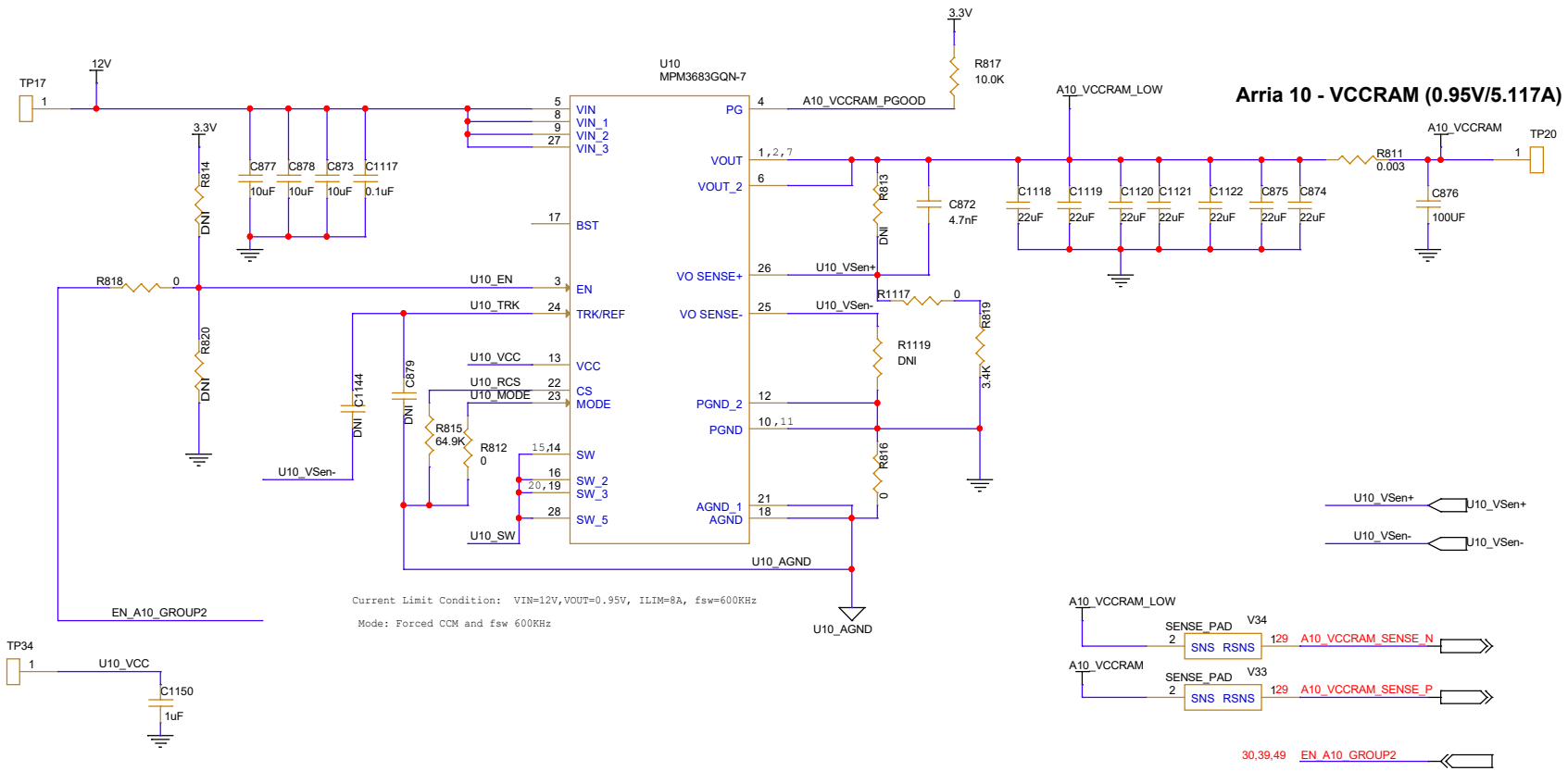
Altera Corporation, 101 Innovation Dr., San Jose, CA 95134		
© 2024 Altera Corporation. All Rights Reserved.		
Title: Arria® 10 GX FPGA Development Kit (Non-ENP)		
Size: B	Document Number: M88349-002 (100-0330700-B1)	Rev: B
Date: Wednesday, December 11, 2024	Sheet: 36	of 49

This page intentionally left blank



Altera Corporation, 101 innovation Dr, San Jose, CA 95134 © 2024 Altera Corporation. All Rights Reserved.		
Title Arria® 10 GX FPGA Development Kit (Non-ENP)		
Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
Date: Wednesday, December 11, 2024	Sheet 37	of 49

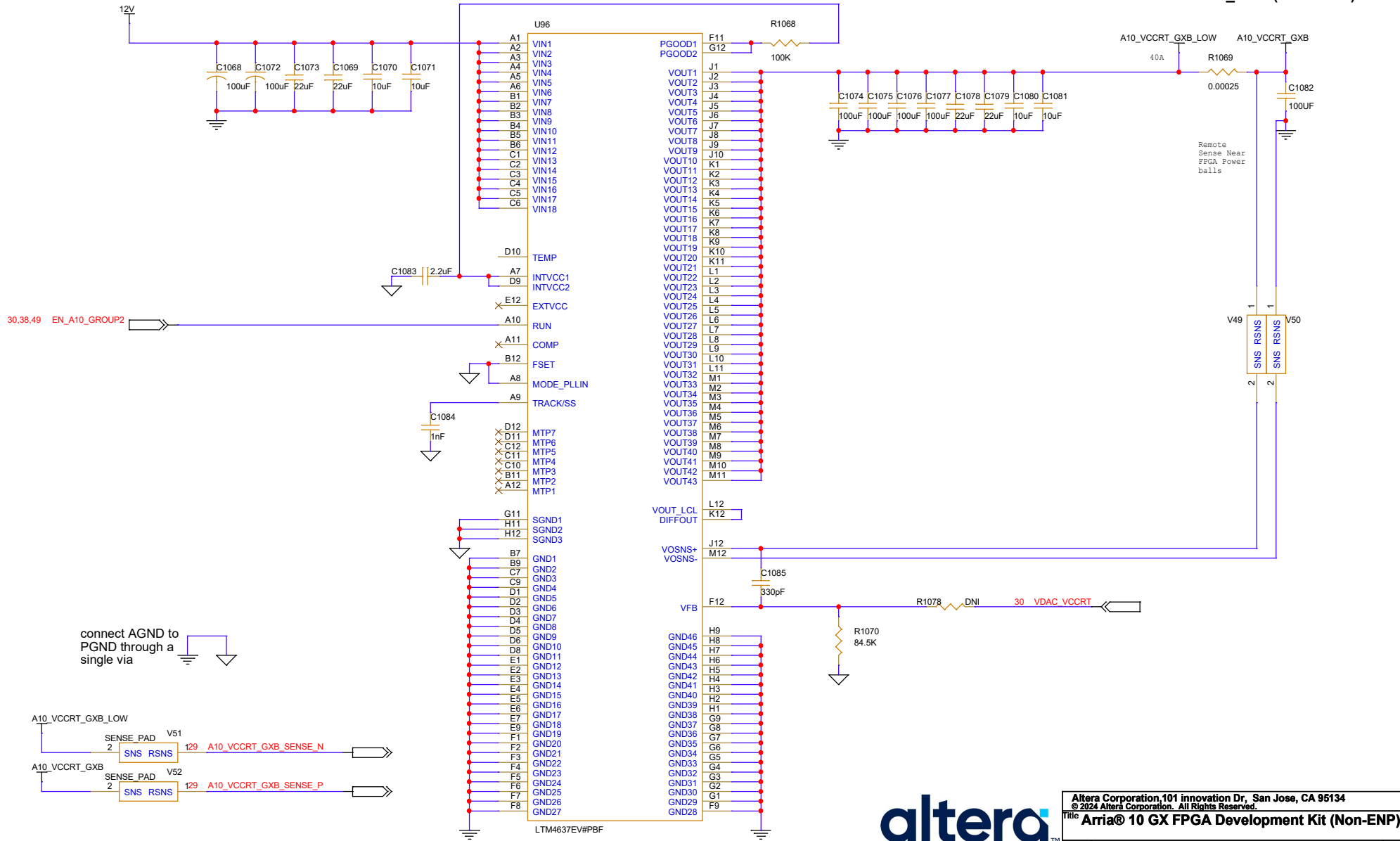
Power - A10 VCCRAM



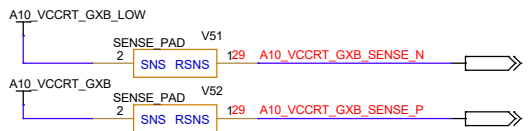
Altera Corporation, 101 Innovation Dr., San Jose, CA 95134 © 2024 Altera Corporation. All Rights Reserved.		
Title: Arria® 10 GX FPGA Development Kit (Non-ENP)		
Size: B	Document Number: M88349-002 (100-0330700-B1)	Rev: B
Date: Wednesday, December 11, 2024	Sheet: 38	of 49

Power - A10 VCCRT GXB

Arria 10 - VCCRT_GXB (1.03V/17A)



connect AGND to PGND through a single via



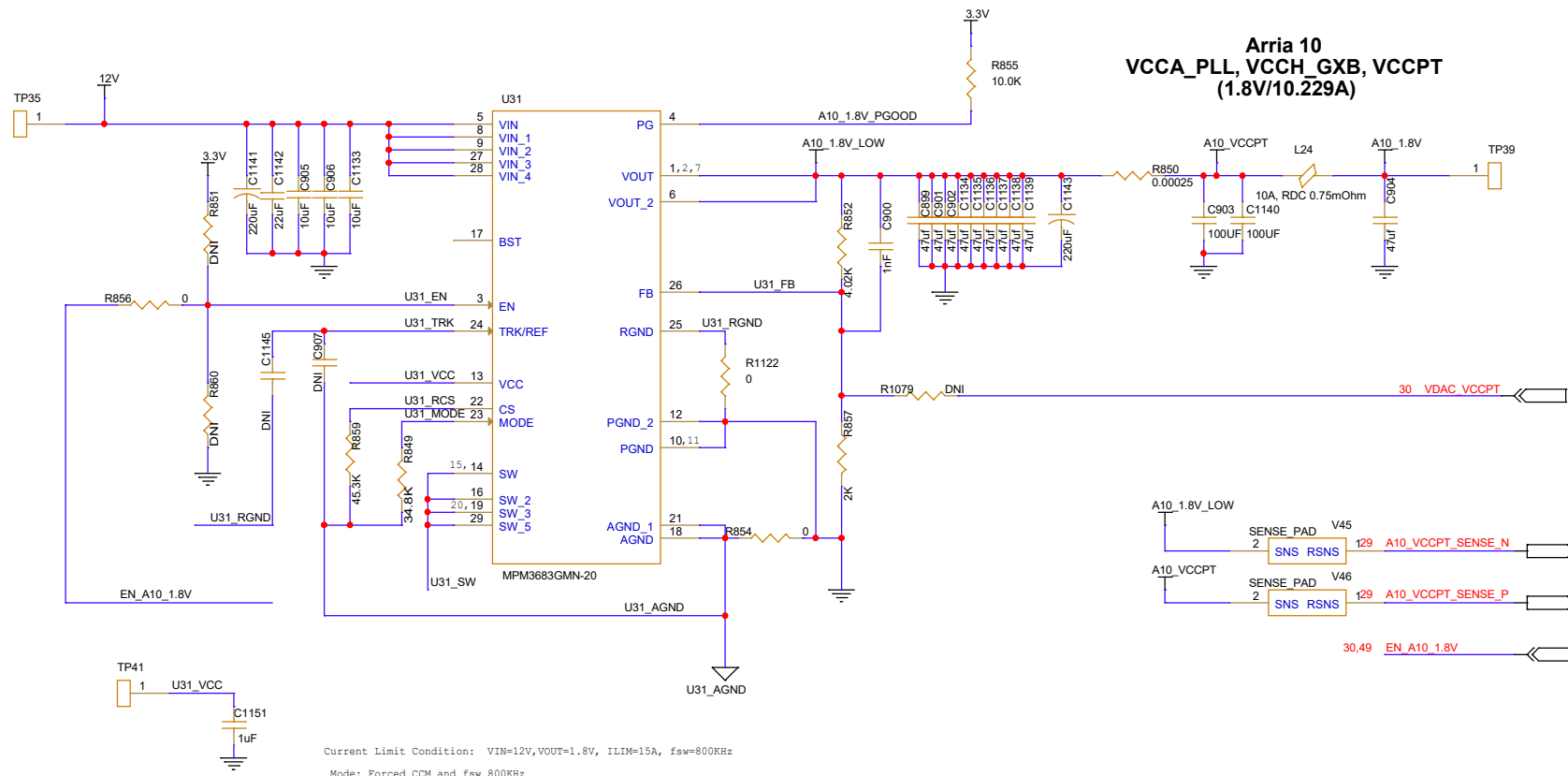
Altera Corporation, 101 Innovation Dr., San Jose, CA 95134			
© 2024 Altera Corporation. All Rights Reserved.			
Title: Arria® 10 GX FPGA Development Kit (Non-ENP)			
Size: B	Document Number: M88349-002 (100-0330700-B1)	Rev: B	
Date: Wednesday, December 11, 2024	Sheet: 39	of: 49	

This page intentionally left blank



Altera Corporation, 101 innovation Dr, San Jose, CA 95134 © 2024 Altera Corporation. All Rights Reserved.		
Title Arria® 10 GX FPGA Development Kit (Non-ENP)		
Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
Date: Wednesday, December 11, 2024	Sheet 40 of 49	

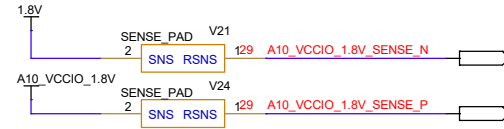
Power - A10 VCCPT & 1.8V



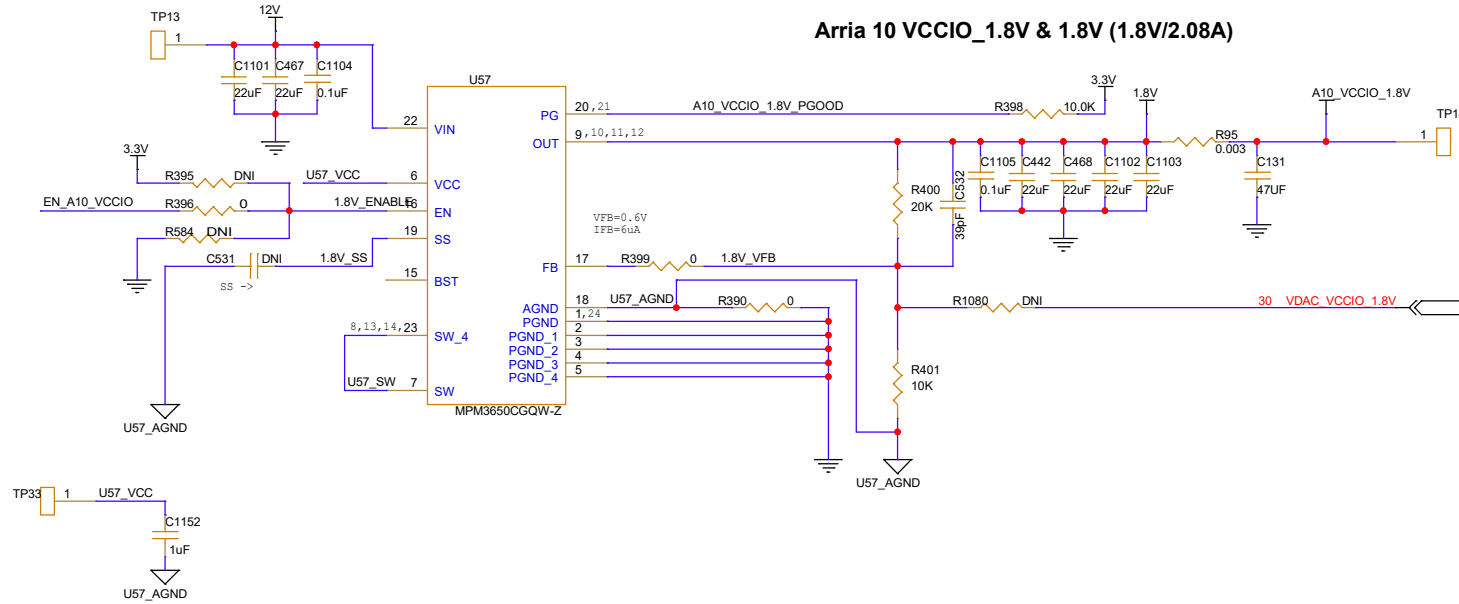
Altera Corporation, 101 Innovation Dr., San Jose, CA 95134 © 2024 Altera Corporation. All Rights Reserved.		
Title: Arria® 10 GX FPGA Development Kit (Non-ENP)		
Size: B	Document Number: M88349-002 (100-0330700-B1)	Rev: B
Date: Wednesday, December 11, 2024	Sheet: 41	of 49

Power - A10 VCCIO 1.8V

30,34,43,44,45,49 EN_A10_VCCIO
 35 A10_VCCIO_1.8V_PGOOD

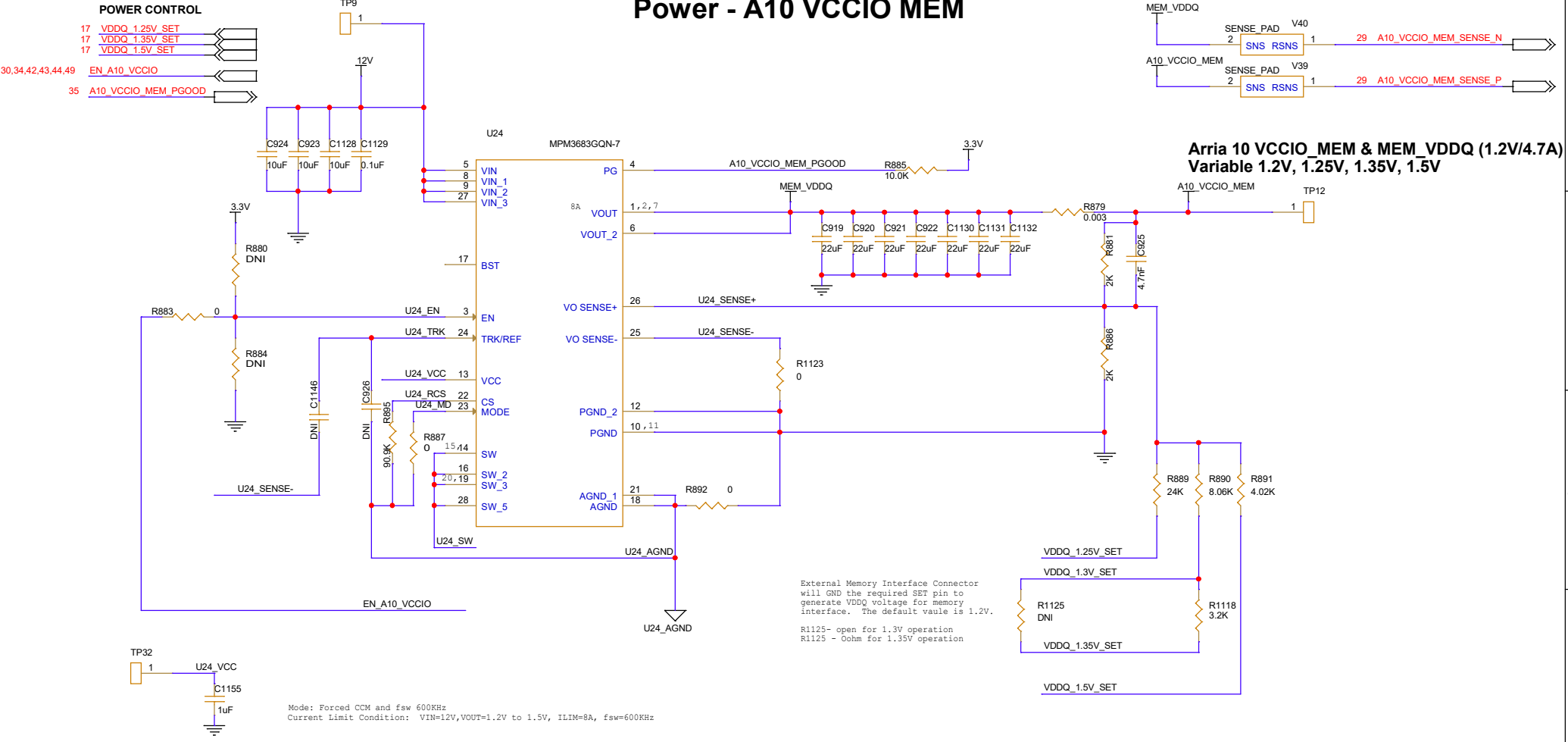


Arria 10 VCCIO_1.8V & 1.8V (1.8V/2.08A)



Altera Corporation, 101 Innovation Dr., San Jose, CA 95134 © 2024 Altera Corporation. All Rights Reserved.		
Title: Arria® 10 GX FPGA Development Kit (Non-ENP)		
Size: B	Document Number: M88349-002 (100-0330700-B1)	Rev: B
Date: Wednesday, December 11, 2024	Sheet: 42 of 49	

Power - A10 VCCIO MEM



**Arria 10 VCCIO_MEM & MEM_VDDQ (1.2V/4.7A)
Variable 1.2V, 1.25V, 1.35V, 1.5V**

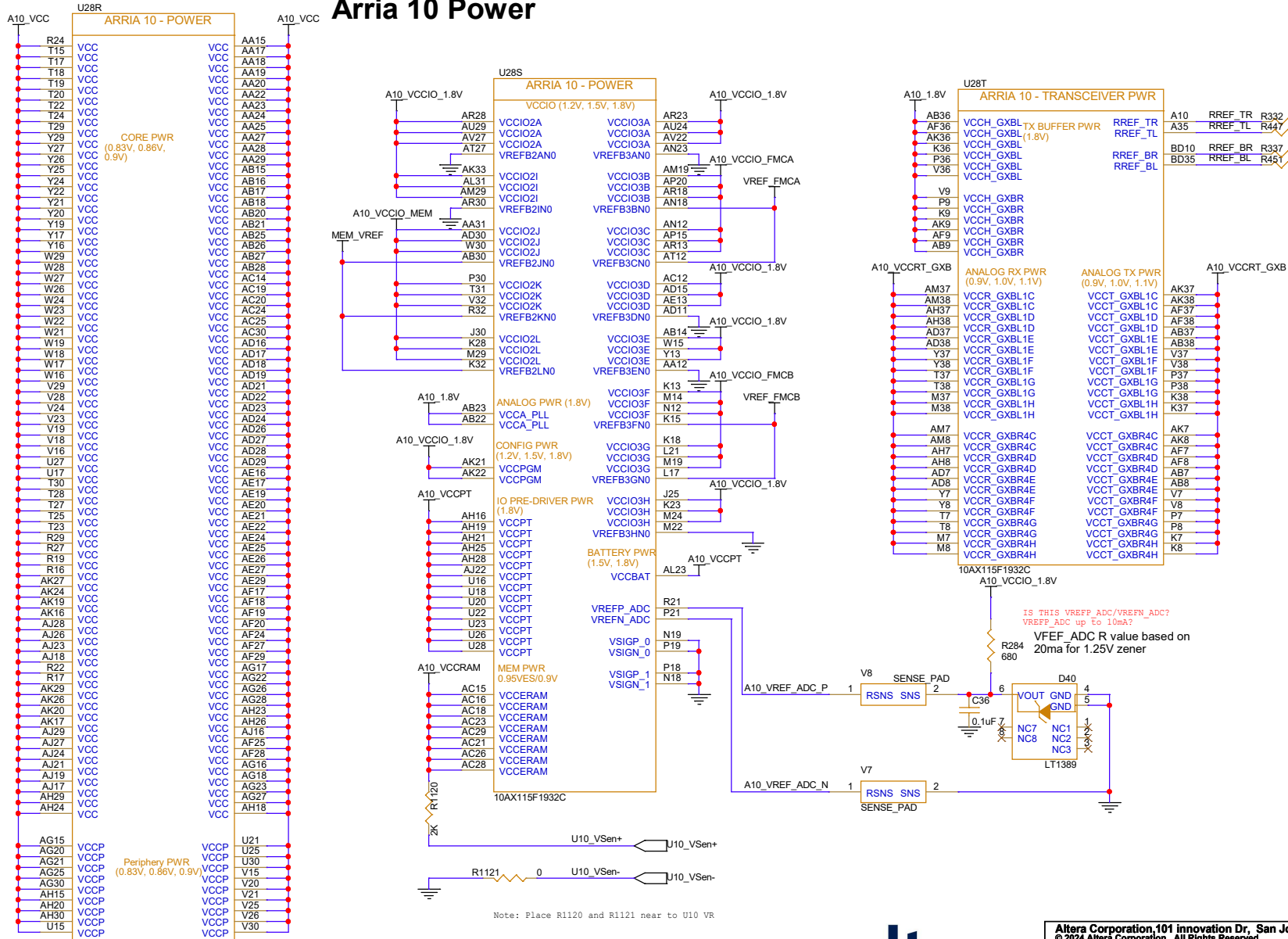
External Memory Interface Connector will GND the required SET pin to generate VDDQ voltage for memory interface. The default value is 1.2V.
R1125- open for 1.3V operation
R1125 - 0ohm for 1.35V operation

Mode: Forced CCM and fsw 600KHz
Current Limit Condition: VIN=12V,VOUT=1.2V to 1.5V, ILIM=8A, fsw=600KHz



Altera Corporation, 101 innovation Dr, San Jose, CA 95134 © 2024 Altera Corporation. All Rights Reserved.		
Title Arria® 10 GX FPGA Development Kit (Non-ENP)		
Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
Date:	Wednesday, December 11, 2024	Sheet 45 of 49

Arria 10 Power



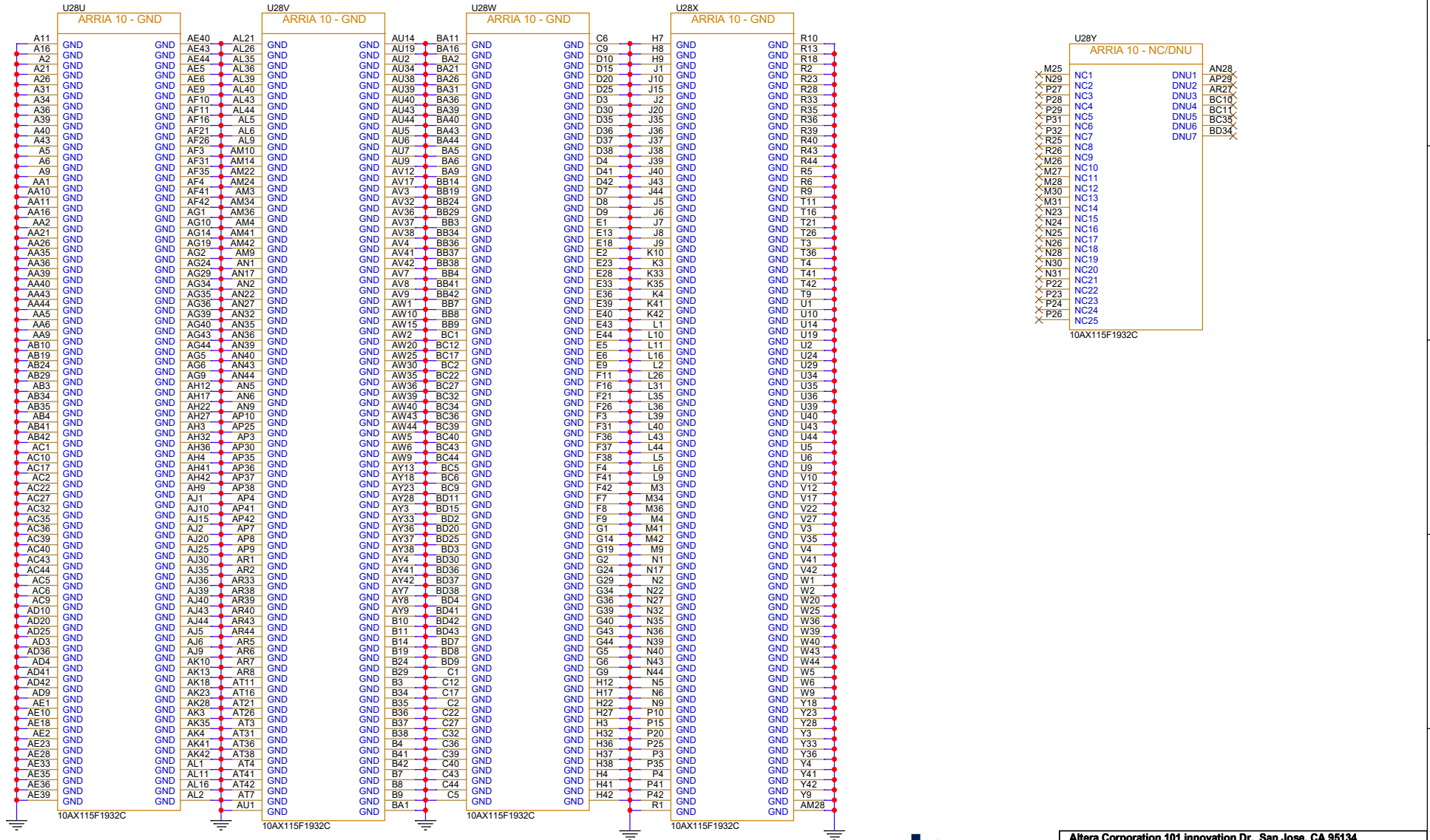
Note: Place R1120 and R1121 near to U10 VR



Altera Corporation, 101 Innovation Dr., San Jose, CA 95134
 © 2024 Altera Corporation. All Rights Reserved.
Title: Arria® 10 GX FPGA Development Kit (Non-ENP)

Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
Date: Wednesday, December 11, 2024	Sheet 46 of 49	

Arria 10 Ground



Altera Corporation, 101 innovation Dr, San Jose, CA 95134
 © 2024 Altera Corporation. All Rights Reserved.

Title Arria® 10 GX FPGA Development Kit (Non-ENP)

Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
Date: Wednesday, December 11, 2024		Sheet 47 of 49

Decoupling

Do Not Copy. Decoupling requirements is design specific. Please use the Early Power Estimator and PDN Tool available on Altera.com to determine your specific decoupling requirements.



SCREW1	STANDOFF1
SCREW2	STANDOFF2
SCREW3	STANDOFF3
SCREW4	STANDOFF4
SCREW5	STANDOFF5



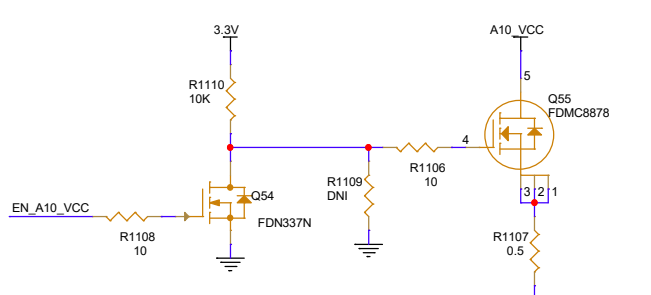
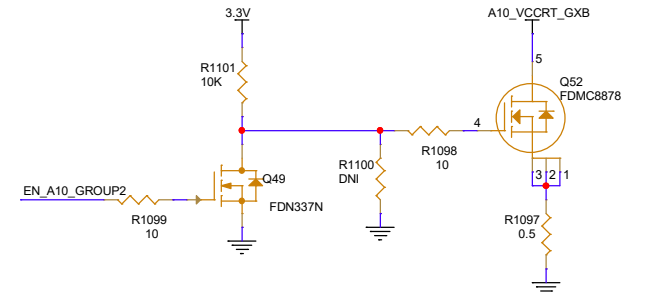
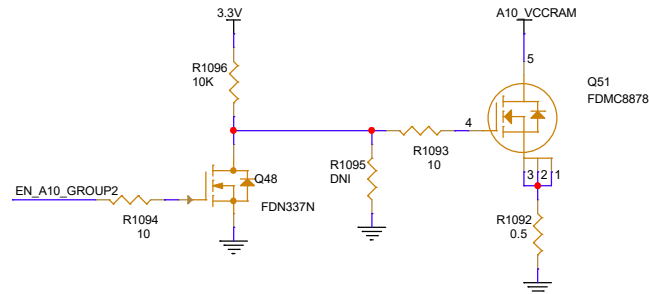
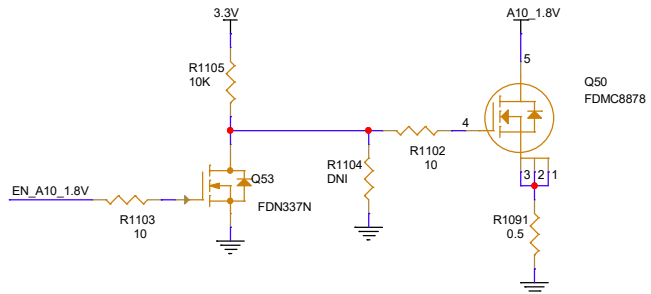
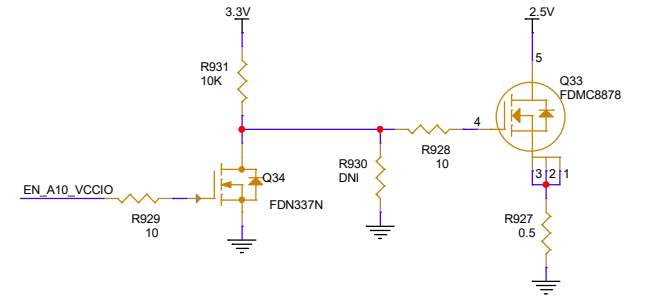
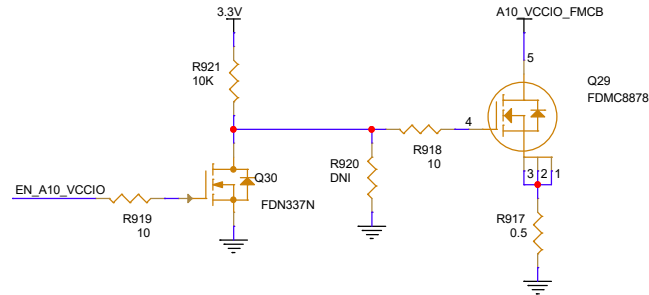
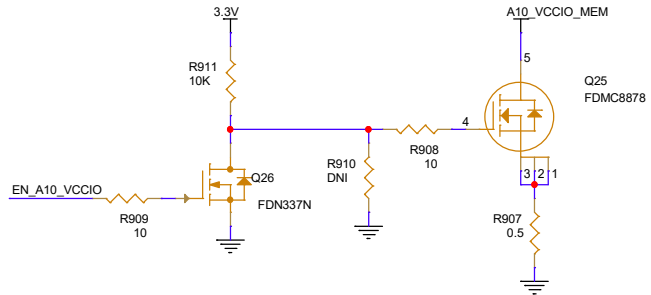
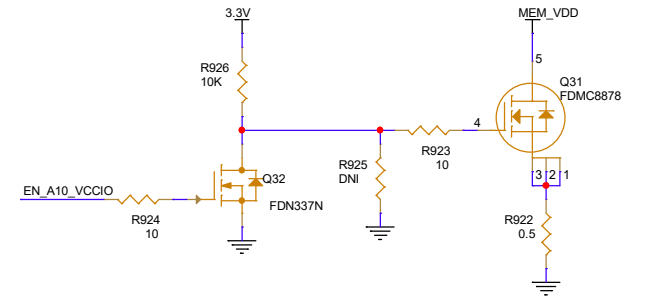
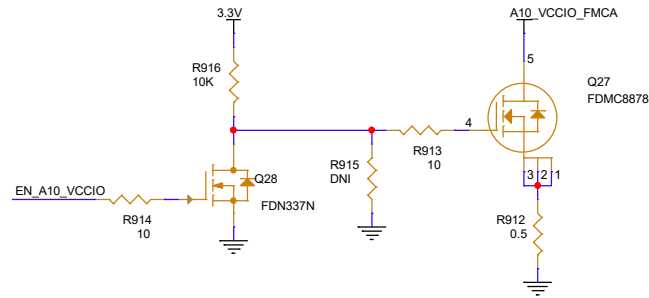
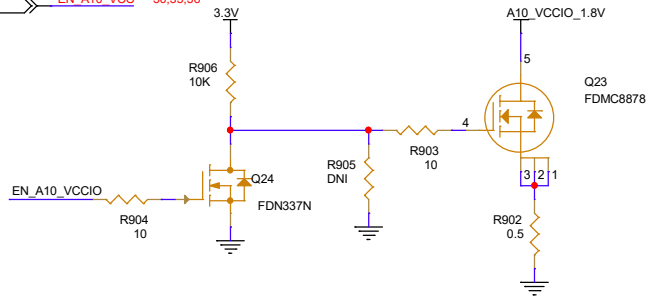
Altera Corporation, 101 Innovation Dr., San Jose, CA 95134
 © 2024 Altera Corporation. All Rights Reserved.

Title: Arria® 10 GX FPGA Development Kit (Non-ENP)

Size B	Document Number M88349-002 (100-0330700-B1)	Rev B
Date: Wednesday, December 11, 2024	Sheet 48 of 49	

Power-down Fast Discharge

EN A10_VCCIO 30,34,42,43,44,45
 EN A10_1.8V 30,41
 EN A10_GROUP2 30,38,39
 EN A10_VCC 30,35,36



Altera Corporation, 101 Innovation Dr., San Jose, CA 95134			
© 2024 Altera Corporation. All Rights Reserved.			
Title: Arria® 10 GX FPGA Development Kit (Non-ENP)			
Size: B	Document Number: M88349-002 (100-0330700-B1)	Rev: B	
Date: Wednesday, December 11, 2024	Sheet: 49	of 49	