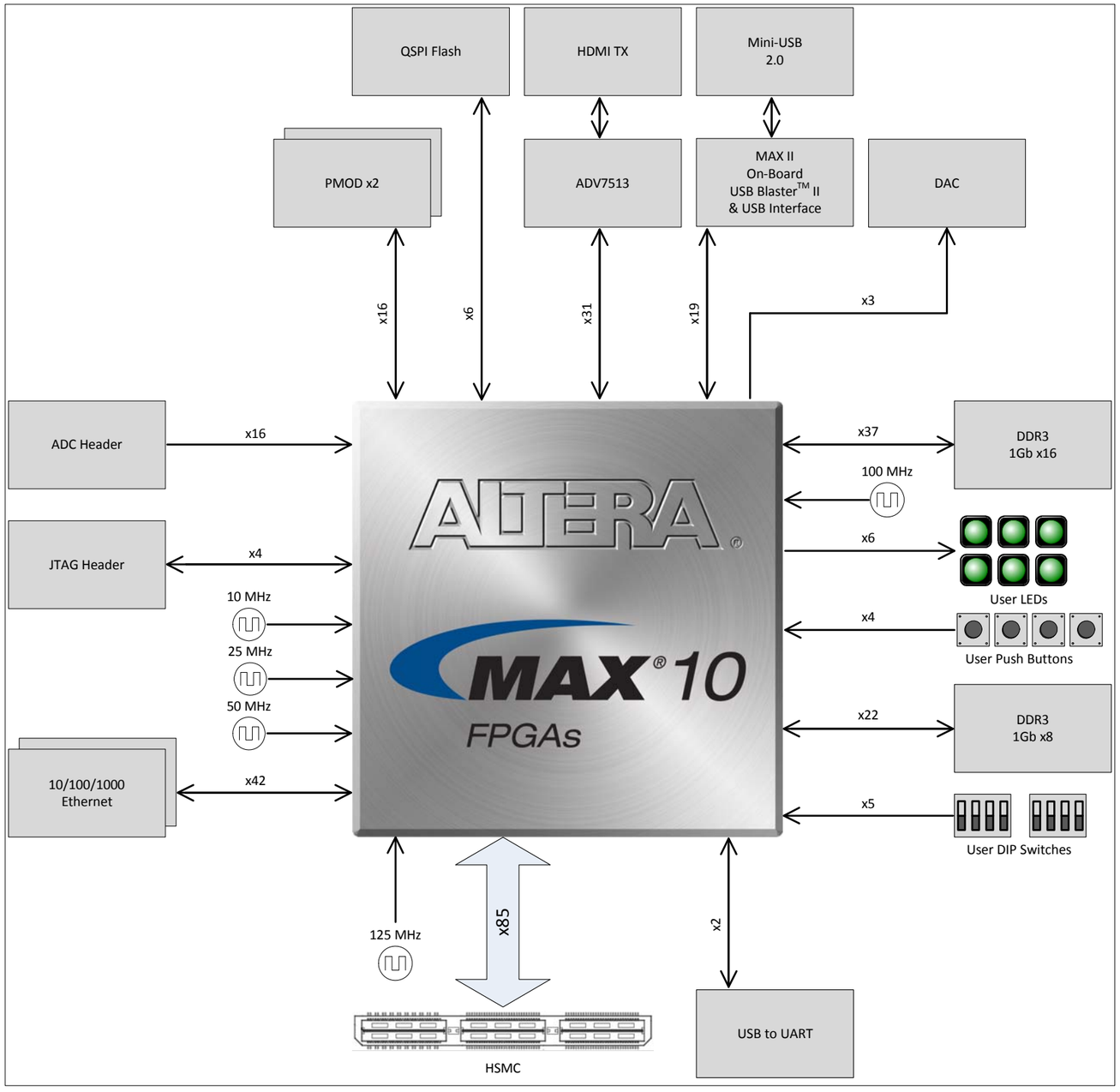
NOTES:

1. Project Drawing Numbers:

Raw PCB	100-0321401- B1
Gerber Files	110-0321401- B1
PCB Design Files	120-0321401- B1
Assembly Drawing	130-0321401- B1
Fab Drawing	140-0321401- B1
Schematic Drawing	150-0321401- B1
PCB Film	160-0321401- B1
Bill of Materials	170-0321401- B1
Schematic Design Files	180-0321401- B1
Functional Specification	210-0321401- B1
PCB Layout Guidelines	220-0321401- B1
Assembly Rework	320-0321401- B1

Pre-Release Schematic
DO NOT COPY

MAX 10 Development Kit Board



REV	DATE	PAGES	DESCRIPTION
A	20 May 2014	All	INITIAL REVISION A RELEASE
B	2 Sep 2014	6	Swap pin AA21 with AA22
		7	Swap pin D5 with C3, and E8 with C6
		23	Change resistor value, R44 to 10K, R106 to 1K, R99 to 2K, R100 to 1K, R104 to 1K
		24	SW3 pin number change
		26 27	Add DNI capacitor, C70 and C166
	24 Sep 2014	1	Add functional diagram
		24	Change resistor value, R169 to 10K
	26 Jan 2015	All	Update notes for release version

PAGE	DESCRIPTION	PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Rev. History	30	MAX10 Ground
2	Power Tree	31	Decoupling
3	Clock Tree		
4	MAX10 Bank 1 & 2		
5	MAX10 Bank 3 & 4		
6	MAX10 Bank 5 & 6		
7	MAX10 Bank 7 & 8		
8	MAX10 Configuration		
9	MAX10 Clocks		
10	PLL		
11	ADC Filter		
12	DAC		
13	DDR3 SDRAM		
14	QSPI FLASH		
15	HSMC Port		
16	GPIO, PMOD		
17	HDMI		
18	10/100/1000 Ethernet A		
19	10/100/1000 Ethernet B		
20	USB to UART		
21	On-Board USB Blaster II-1		
22	On-Board USB Blaster II-2		
23	LED, User IO, Connector		
24	Power1		
25	Power2		
26	Power3		
27	Power4		
28	Power5		
29	MAX10 Power		

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Title: MAX10 FPGA Development Kit (6XX-44292R)		
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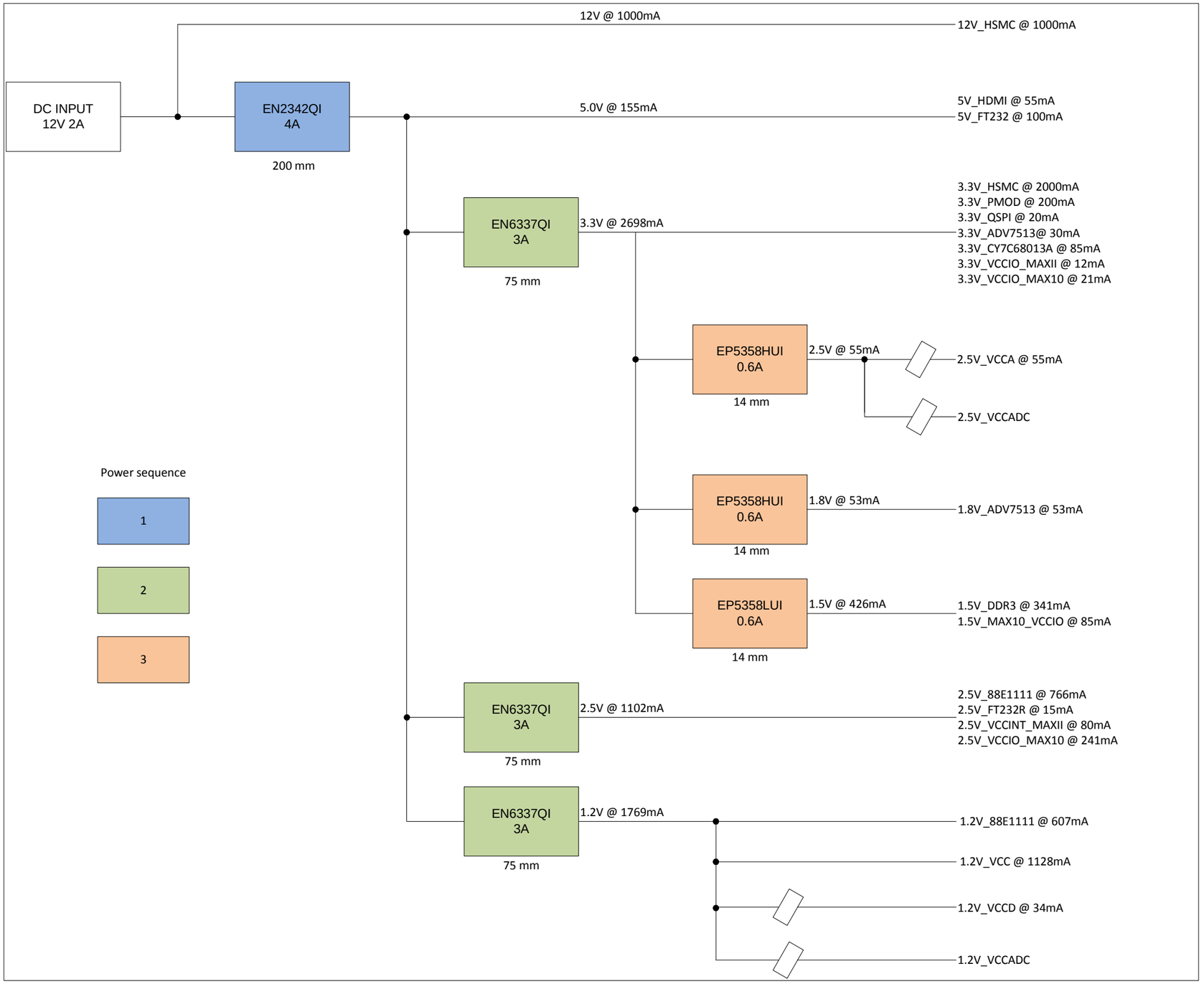
Power Tree



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Title: MAX10 FPGA Development Kit (6XX-44292R)		
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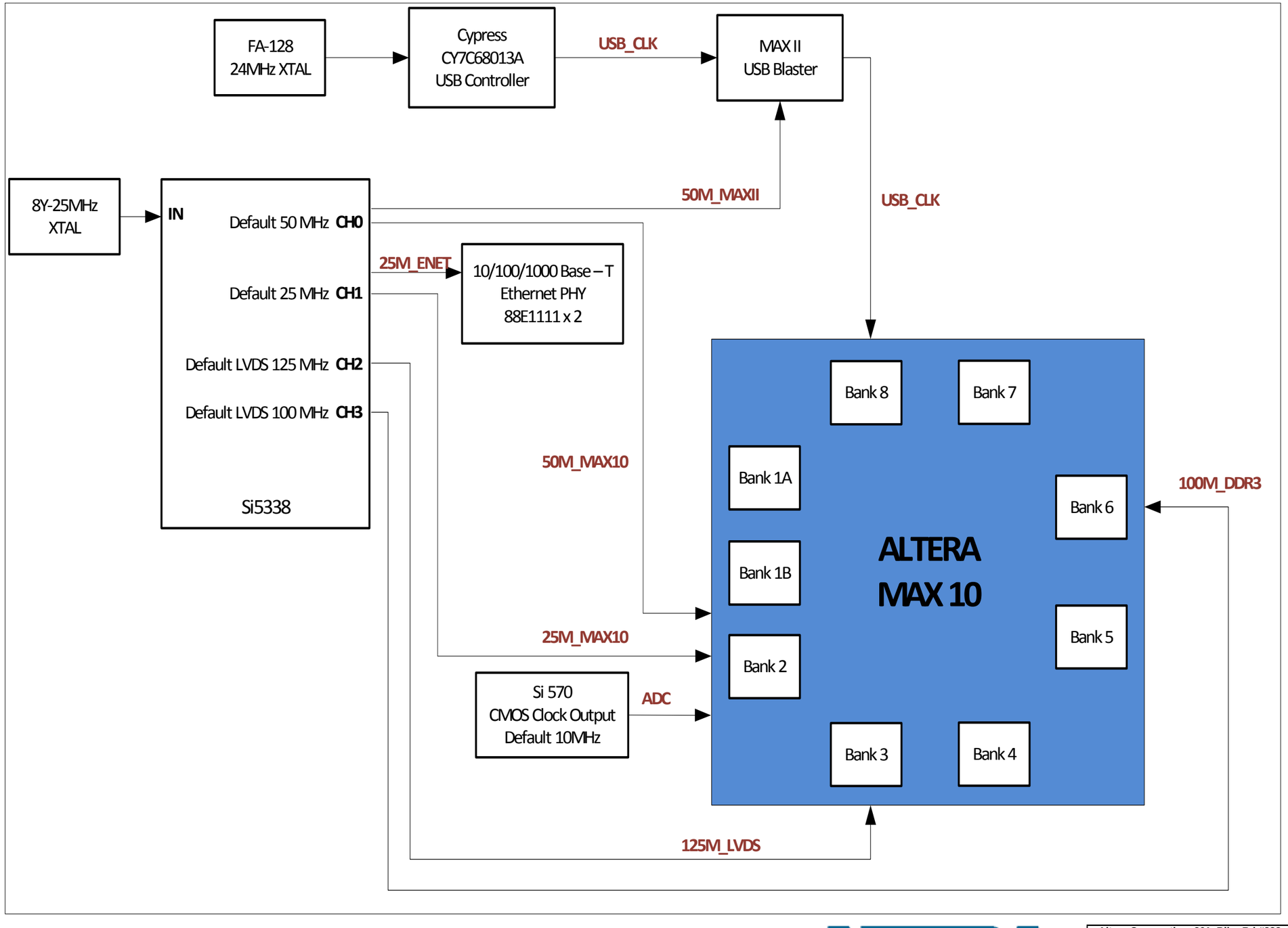
Clock Tree



Title	MAX10 FPGA Development Kit (6XX-44292R)	
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MAX10 Bank 1 & 2

U1A

MAX 10 LEFT BANKS

		BANK-1A (VCCIO = 2.5V)	BANK-1B (VCCIO = 2.5V)
ADC1IN1	F5	DIFFIO_RX_L1N/ADC1IN1	
ADC1IN2	F4	DIFFIO_RX_L1P/ADC1IN2	
ADC2IN1	E4	DIFFIO_RX_L2N/ADC2IN1	
ADC2IN8	E3	DIFFIO_RX_L2P/ADC2IN8	
ADC1IN3	J8	DIFFIO_RX_L3N/ADC1IN3	
ADC1IN4	J9	DIFFIO_RX_L3P/ADC1IN4	
ADC2IN3	G4	DIFFIO_RX_L4N/ADC2IN3	
ADC2IN4	F3	DIFFIO_RX_L4P/ADC2IN4	
ADC1IN6	H3	DIFFIO_RX_L5P/ADC1IN6	
ADC1IN5	J4	DIFFIO_RX_L5N/ADC1IN5	
ADC2IN5	H4	DIFFIO_RX_L6N/ADC2IN5	
ADC2IN6	G3	DIFFIO_RX_L6P/ADC2IN6	
ADC1IN7	K5	DIFFIO_RX_L7N/ADC1IN7	
ADC1IN8	K6	DIFFIO_RX_L7P/ADC1IN8	
ADC2IN2	J3	DIFFIO_RX_L8P/ADC2IN2	
ADC2IN7	K4	DIFFIO_RX_L8N/ADC2IN7	
	K8		DIFFIO_RX_L15N
	D3		DIFFIO_RX_L16N
	D2		DIFFIO_RX_L16P
	K2		DIFFIO_RX_L19N
	L2		DIFFIO_RX_L19P
	L8		DIFFIO_RX_L20N
	L9		DIFFIO_RX_L20P
	E1		DIFFIO_RX_L21N
	F2		DIFFIO_RX_L21P
	H1		DIFFIO_RX_L22N
	J1		DIFFIO_RX_L22P
	G1		DIFFIO_RX_L23N
	F1		DIFFIO_RX_L23P
	M4		DIFFIO_RX_L24N
	M3		DIFFIO_RX_L24P
	K1		DIFFIO_RX_L25N
	L1		DIFFIO_RX_L25P
	C1		VREFB1N0
	D1		IO_BANK1

BANK-2(VCCIO = 2.5V)		
DIFFIO_RX_L29N	P4	ENETA_TX_ER
DIFFIO_RX_L29P	P5	ENETA_TX_D1
DIFFIO_RX_L37N	N3	ENETB_RX_CRS
DIFFIO_RX_L37P	N2	ENETB_RX_COL
DIFFIO_RX_L39N	R4	ENETA_TX_EN
DIFFIO_RX_L39P	R5	ENETA_TX_D0
DIFFIO_RX_L40N	T1	ENETA_RX_D1
DIFFIO_RX_L40P	T2	ENETA_RX_DV
DIFFIO_RX_L41N	N8	ENETA_RX_CRS
DIFFIO_RX_L41P	N9	ENETA_RX_D0
DIFFIO_RX_L42N	P1	ENETA_RX_COL
DIFFIO_RX_L42P	N1	ENETA_RX_D2
DIFFIO_RX_L43N	T3	ENETA_RX_D3
DIFFIO_RX_L43P	U2	ENETA_RX_ER
DIFFIO_RX_L44N	U1	ENETB_TX_D0
DIFFIO_RX_L44P	V1	ENETB_TX_D1
DIFFIO_RX_L45N	U4	ENETB_TX_D3
DIFFIO_RX_L45P	U5	ENETB_TX_ER
DIFFIO_RX_L46N	U3	ENETB_TX_D2
DIFFIO_RX_L46P	V3	ENETB_TX_EN
DIFFIO_RX_L47N	P8	ENETB_RX_D0
DIFFIO_RX_L47P	R7	ENETB_RX_D3
DIFFIO_RX_L48N	W1	ENETA_TX_D2
DIFFIO_RX_L48P	W2	ENETA_TX_D3
DIFFIO_RX_L60N	R1	ENETB_RX_DV
DIFFIO_RX_L60P	R2	ENETB_RX_ER
VREFB2N0	M2	ENETB_RX_D2
IO_BANK2	M1	ENETB_RX_D1

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ADC INPUT

ADC1IN[8:1] 11

ADC2IN[8:1] 11

10/100/1000 Ethernet A

ENETA_TX_D[3:0] 18

ENETA_TX_EN 18

ENETA_TX_ER 18

ENETA_RX_D[3:0] 18

ENETA_RX_DV 18

ENETA_RX_ER 18

ENETA_RX_CRS 18

ENETA_RX_COL 18

10/100/1000 Ethernet B

ENETB_TX_D[3:0] 19

ENETB_TX_EN 19

ENETB_TX_ER 19

ENETB_RX_D[3:0] 19

ENETB_RX_DV 19

ENETB_RX_ER 19

ENETB_RX_CRS 19

ENETB_RX_COL 19

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MAX10 Bank 3 & 4

U1B

MAX 10 BOTTOM BANKS

		BANK-3 (VCCIO = 2.5V)	BANK-4 (VCCIO = 2.5V)		
HSMC_D0	Y7	DIFFIO_RX_B10N	DIFFIO_RX_B25N	W11	HSMC_RX_D_N13
HSMC_D1	Y8	DIFFIO_RX_B10P	DIFFIO_RX_B25P	Y11	HSMC_RX_D_P13
HSMC_D2	AB2	DIFFIO_RX_B12N	DIFFIO_RX_B27N	AB10	HSMC_RX_D_N14
HSMC_D3	AB3	DIFFIO_RX_B12P	DIFFIO_RX_B27P	AB11	HSMC_RX_D_P14
HSMC_RX_D_N6	Y3	DIFFIO_RX_B14N	DIFFIO_RX_B29N	AB12	HSMC_RX_D_N15
HSMC_RX_D_P6	Y4	DIFFIO_RX_B14P	DIFFIO_RX_B29P	AB13	HSMC_RX_D_P15
HSMC_RX_D_N7	AA5	DIFFIO_RX_B17N	DIFFIO_RX_B35N	W12	HSMC_RX_D_N8
HSMC_RX_D_P7	AB5	DIFFIO_RX_B17P	DIFFIO_RX_B35P	W13	HSMC_RX_D_P8
HSMC_RX_D_N5	AB6	DIFFIO_RX_B19N	DIFFIO_RX_B38N	AA14	HSMC_RX_D_N9
HSMC_RX_D_P5	AB7	DIFFIO_RX_B19P	DIFFIO_RX_B38P	AB15	HSMC_RX_D_P9
HSMC_RX_D_N3	AA8	DIFFIO_RX_B21N	DIFFIO_RX_B40N	AA15	HSMC_RX_D_N10
HSMC_RX_D_P3	AB8	DIFFIO_RX_B21P	DIFFIO_RX_B40P	Y16	HSMC_RX_D_P10
HSMC_RX_D_N4	AA9	DIFFIO_RX_B23N	DIFFIO_RX_B42N	AB16	HSMC_RX_D_N11
HSMC_RX_D_P4	AB9	DIFFIO_RX_B23P	DIFFIO_RX_B42P	AA16	HSMC_RX_D_P11
HSMC_RX_D_N0	V4	DIFFIO_RX_B2N	DIFFIO_RX_B44N	AB19	HSMC_RX_D_N16
HSMC_RX_D_P0	V5	DIFFIO_RX_B2P	DIFFIO_RX_B44P	AB20	HSMC_RX_D_P16
HSMC_RX_D_N1	Y1	DIFFIO_RX_B4N	DIFFIO_RX_B46N	AA19	HSMC_SDA
HSMC_RX_D_P1	Y2	DIFFIO_RX_B4P	DIFFIO_RX_B46P	Y18	HSMC_SCL
HSMC_RX_D_N2	AA1	DIFFIO_RX_B6N	DIFFIO_RX_B50N	AB21	HSMC_CLK_IN_N1
HSMC_RX_D_P2	AA2	DIFFIO_RX_B6P	DIFFIO_RX_B50P	AA20	HSMC_CLK_IN_P1
ENET_MDIO	Y5	DIFFIO_RX_B8N	DIFFIO_RX_B58N	AB17	HSMC_RX_D_N12
ENET_MDC	Y6	DIFFIO_RX_B8P	DIFFIO_RX_B58P	AB18	HSMC_RX_D_P12
HSMC_TX_D_N7	W9	DIFFIO_TX_RX_B11N	DIFFIO_TX_RX_B24N	V11	HSMC_TX_D_N13
HSMC_TX_D_P7	W10	DIFFIO_TX_RX_B11P	DIFFIO_TX_RX_B24P	V12	HSMC_TX_D_P13
HSMC_TX_D_N3	W7	DIFFIO_TX_RX_B13N	DIFFIO_TX_RX_B26N	R12	HSMC_TX_D_N14
HSMC_TX_D_P3	W8	DIFFIO_TX_RX_B13P	DIFFIO_TX_RX_B26P	P12	HSMC_TX_D_P14
HSMC_TX_D_N6	R10	DIFFIO_TX_RX_B15N	DIFFIO_TX_RX_B28N	AA11	HSMC_TX_D_N15
HSMC_TX_D_P6	P10	DIFFIO_TX_RX_B15P	DIFFIO_TX_RX_B28P	AA12	HSMC_TX_D_P15
HSMC_TX_D_N5	AA6	DIFFIO_TX_RX_B16N	DIFFIO_TX_RX_B34N	V13	HSMC_TX_D_N8
HSMC_TX_D_P5	AA7	DIFFIO_TX_RX_B16P	DIFFIO_TX_RX_B34P	W14	HSMC_TX_D_P8
HSMC_TX_D_N2	W5	DIFFIO_TX_RX_B1N	DIFFIO_TX_RX_B36N	R13	HSMC_CLK_OUT_N1
HSMC_TX_D_P2	W6	DIFFIO_TX_RX_B1P	DIFFIO_TX_RX_B36P	P13	HSMC_CLK_OUT_P1
HSMC_TX_D_N4	Y10	DIFFIO_TX_RX_B22N	DIFFIO_TX_RX_B37N	Y13	HSMC_TX_D_N9
HSMC_TX_D_P4	AA10	DIFFIO_TX_RX_B22P	DIFFIO_TX_RX_B37P	Y14	HSMC_TX_D_P9
HSMC_TX_D_N1	U6	DIFFIO_TX_RX_B3N	DIFFIO_TX_RX_B39N	V14	HSMC_CLK_OUT_N2
HSMC_TX_D_P1	U7	DIFFIO_TX_RX_B3P	DIFFIO_TX_RX_B39P	W15	HSMC_CLK_OUT_P2
HSMC_TX_D_N0	W4	DIFFIO_TX_RX_B5N	DIFFIO_TX_RX_B41N	U15	HSMC_TX_D_N10
HSMC_TX_D_P0	W3	DIFFIO_TX_RX_B5P	DIFFIO_TX_RX_B41P	V16	HSMC_TX_D_P10
ENETA_INTn	V7	DIFFIO_TX_RX_B7N	DIFFIO_TX_RX_B43N	AA17	HSMC_TX_D_N16
ENETA_RESETn	V8	DIFFIO_TX_RX_B7P	DIFFIO_TX_RX_B43P	Y17	HSMC_TX_D_P16
ENETA_LED_LINK100	R9	DIFFIO_TX_RX_B9N	DIFFIO_TX_RX_B45N	V15	HSMC_TX_D_N11
ENETB_LED_LINK100	P9	DIFFIO_TX_RX_B9P	DIFFIO_TX_RX_B45P	W16	HSMC_TX_D_P11
ENETB_INTn	AA3	VREFB3N0	DIFFIO_TX_RX_B49N	Y19	UART_RX
ENETB_RESETn	AB4	IO_BANK3	DIFFIO_TX_RX_B49P	W18	UART_TX
			VREFB4N0	AA13	HSMC_CLK_OUT0
			IO_BANK4	AB14	HSMC_PRSNTn

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HSMC_RX_D_P0	R249	DNI	HSMC_RX_D_N0	
HSMC_RX_D_P1	R250	DNI	HSMC_RX_D_N1	
HSMC_RX_D_P2	R251	DNI	HSMC_RX_D_N2	
HSMC_RX_D_P3	R252	DNI	HSMC_RX_D_N3	
HSMC_RX_D_P4	R253	DNI	HSMC_RX_D_N4	
HSMC_RX_D_P5	R254	DNI	HSMC_RX_D_N5	
HSMC_RX_D_P6	R255	DNI	HSMC_RX_D_N6	
HSMC_RX_D_P7	R256	DNI	HSMC_RX_D_N7	
HSMC_RX_D_P8	R257	DNI	HSMC_RX_D_N8	
HSMC_RX_D_P9	R258	DNI	HSMC_RX_D_N9	
HSMC_RX_D_P10	R259	DNI	HSMC_RX_D_N10	
HSMC_RX_D_P11	R260	DNI	HSMC_RX_D_N11	
HSMC_RX_D_P12	R261	DNI	HSMC_RX_D_N12	
HSMC_RX_D_P13	R262	DNI	HSMC_RX_D_N13	
HSMC_RX_D_P14	R263	DNI	HSMC_RX_D_N14	
HSMC_RX_D_P15	R264	DNI	HSMC_RX_D_N15	
HSMC_RX_D_P16	R265	DNI	HSMC_RX_D_N16	

HSMC Interface

HSMC_D[3:0]	15
HSMC_RX_D_P[16:0]	15
HSMC_RX_D_N[16:0]	15
HSMC_TX_D_P[16:0]	8,15
HSMC_TX_D_N[16:0]	8,15
HSMC_CLK_IN_P[2:1]	8,15
HSMC_CLK_IN_N[2:1]	8,15
HSMC_CLK_OUT_P[2:1]	15
HSMC_CLK_OUT_N[2:1]	15
HSMC_CLK_IN0	8,15
HSMC_CLK_OUT0	15
HSMC_PRSNTn	15,22
HSMC_SDA	15
HSMC_SCL	15

Ethernet

ENET_MDIO	18,19
ENET_MDC	18,19
ENETA_INTn	18
ENETA_RESETn	18
ENETB_INTn	19
ENETB_RESETn	19
ENETA_LED_LINK100	18
ENETB_LED_LINK100	19

UART

UART_RX	20
UART_TX	20

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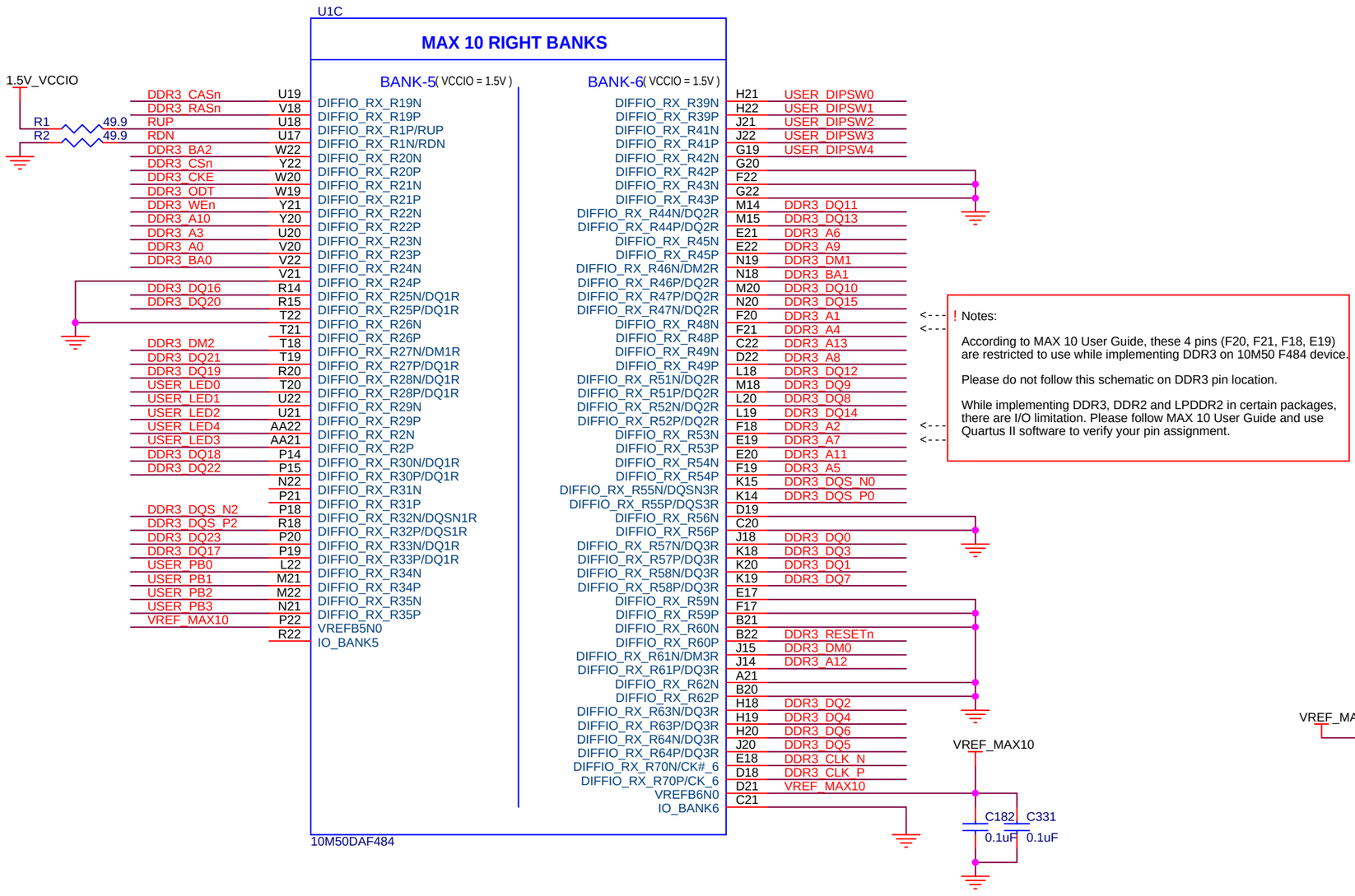
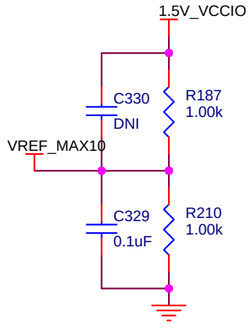
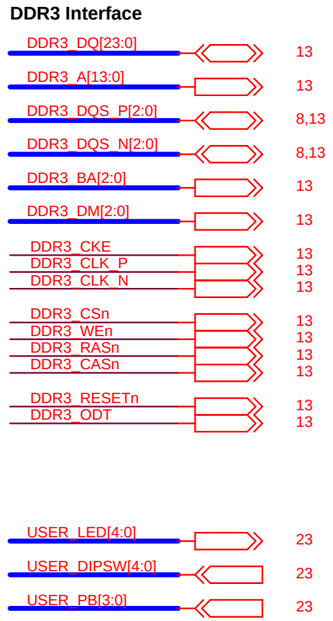
MAX10 Bank 5 & 6







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MAX10 Bank 7 & 8

U1D

MAX 10 TOP BANKS

		BANK-7 (VCCIO = 3.3V)	BANK-8 (VCCIO = 3.3V)		
HDMI_TX_D0	A17	DIFFIO_RX_T10N	DIFFIO_RX_T39N	C7	PMODA_IO0
HDMI_TX_D1	A18	DIFFIO_RX_T10P	DIFFIO_RX_T39P	C8	PMODA_IO1
HDMI_TX_D9	C15	DIFFIO_RX_T15N	DIFFIO_RX_T41N	A6	PMODA_IO2
HDMI_TX_D22	C16	DIFFIO_RX_T15P	DIFFIO_RX_T41P	B7	PMODA_IO3
HDMI_TX_D4	A16	DIFFIO_RX_T16N	DIFFIO_RX_T42P	D8	PMODA_IO4
HDMI_TX_D21	B16	DIFFIO_RX_T16P	DIFFIO_RX_T43N	A4	PMODA_IO5
USB_DATA4	J13	DIFFIO_RX_T17N	DIFFIO_RX_T43P	A5	PMODA_IO6
USB_DATA3	H14	DIFFIO_RX_T17P	DIFFIO_RX_T44N	E9	PMODA_IO7
USB_DATA5	C13	DIFFIO_RX_T18N	DIFFIO_RX_T45P	A2	PMODB_IO4
USB_DATA6	C14	DIFFIO_RX_T18P	DIFFIO_RX_T45N	A3	PMODB_IO5
USB_DATA0	B14	DIFFIO_RX_T19N	DIFFIO_RX_T46P	B3	PMODB_IO7
USB_DATA7	A14	DIFFIO_RX_T19P	DIFFIO_RX_T46N	B4	PMODB_IO6
USB_DATA1	E15	DIFFIO_RX_T1N	DIFFIO_RX_T47P	B5	PMODB_IO2
USB_DATA2	E16	DIFFIO_RX_T1P	DIFFIO_RX_T47N	C4	PMODB_IO3
USB_ADDR1	E13	DIFFIO_RX_T20N	DIFFIO_RX_T48P	E8	PMODB_IO0
USB_WRn	D14	DIFFIO_RX_T20P	DIFFIO_RX_T49N	D5	PMODB_IO1
USB_SDA	E12	DIFFIO_RX_T21P	DIFFIO_RX_T49P	C5	QSPI_IO2
USB_RDn	D13	DIFFIO_RX_T21N	DIFFIO_RX_T51N	B1	QSPI_IO3
HDMI_TX_VS	J12	DIFFIO_RX_T22N	DIFFIO_RX_T51P	B2	QSPI_CLK
HDMI_TX_D13	H13	DIFFIO_RX_T22P	DIFFIO_RX_T53N	C2	QSPI_CSn
HDMI_TX_D2	A12	DIFFIO_RX_T23N	DIFFIO_RX_T53P	C3	QSPI_IO1
HDMI_TX_D8	A13	DIFFIO_RX_T23P	VREFB8N0	D7	JTAG_SAFE
HDMI_TX_D15	D12	DIFFIO_RX_T24N	IO_BANK8	C6	QSPI_IO0
HDMI_TX_D16	C12	DIFFIO_RX_T24P			
HDMI_SCL	A10	DIFFIO_RX_T25N			
HDMI_TX_D11	A11	DIFFIO_RX_T25P			
HDMI_TX_DE	C10	DIFFIO_RX_T26N			
HDMI_TX_D10	C11	DIFFIO_RX_T26P			
HDMI_TX_D7	B11	DIFFIO_RX_T27N			
HDMI_TX_D5	B12	DIFFIO_RX_T27P			
USB_SCL	J11	DIFFIO_RX_T28N			
USB_FULL	H12	DIFFIO_RX_T28P			
USB_RESETn	B8	DIFFIO_RX_T31N			
USB_OEn	A9	DIFFIO_RX_T31P			
USB_EMPTY	C17	DIFFIO_RX_T2N			
USB_ADDR0	D17	DIFFIO_RX_T2P			
	C9	DIFFIO_RX_T30N			
DAC_SYNC	B10	DIFFIO_RX_T30P			
DAC_SCLK	A7	DIFFIO_RX_T29P			
DAC_DIN	A8	DIFFIO_RX_T29N			
HDMI_TX_D6	F15	DIFFIO_RX_T5N			
HDMI_TX_D3	F16	DIFFIO_RX_T5P			
HDMI_TX_D19	B19	DIFFIO_RX_T6N			
HDMI_TX_D17	C19	DIFFIO_RX_T6P			
HDMI_TX_D20	B17	DIFFIO_RX_T7N			
HDMI_TX_D18	C18	DIFFIO_RX_T7P			
HDMI_TX_HS	A19	DIFFIO_RX_T8N			
HDMI_TX_D12	A20	DIFFIO_RX_T8P			
HDMI_TX_D14	E14	DIFFIO_RX_T9N			
HDMI_TX_INT	D15	DIFFIO_RX_T9P			
HDMI_SDA	B15	VREFB7N0			
HDMI_TX_D23	A15	IO_BANK7			

10M50DAF484

HDMI TX

HDMI_TX_D[23:0]	17
HDMI_TX_HS	17
HDMI_TX_VS	17
HDMI_TX_DE	17
HDMI_TX_INT	17
HDMI_SDA	17
HDMI_SCL	17

PMOD

PMODA_IO[7:0]	16
PMODB_IO[7:0]	16

MAX10 USB INTERFACE

USB_DATA[7:0]	22
USB_ADDR[1:0]	22
USB_FULL	22
USB_EMPTY	22
USB_SCL	22
USB_SDA	22
USB_RESETn	22
USB_OEn	22
USB_RDn	22
USB_WRn	22

QSPI FLASH

QSPI_IO[3:0]	14
QSPI_CLK	14
QSPI_CSn	14

DAC

DAC_SYNC	12
DAC_SCLK	12
DAC_DIN	12
JTAG_SAFE	22

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MAX10 Clock

U1E

MAX 10 CLOCK

BANK-2 (VCCIO = 2.5V)

HSMC_CLK_IN0	N4	DIFFIO_RX_L28N/CLK0N	DIFFIO_RX_L38N/DPCLK0	P3	ENETA_RX_CLK
CLK_10_ADC	N5	DIFFIO_RX_L28P/CLK0P	DIFFIO_RX_L38P/DPCLK1	R3	ENETB_RX_CLK
CLK_25_MAX10	M8	DIFFIO_RX_L36N/CLK1N	DIFFIO_RX_L59N/PLL_L_CLKOUTN	T5	ENETA_GTX_CLK
CLK_50_MAX10	M9	DIFFIO_RX_L36P/CLK1P	DIFFIO_RX_L59P/PLL_L_CLKOUTP	T6	ENETB_GTX_CLK

BANK-3 (VCCIO = 2.5V)

HSMC_CLK_IN_N2	V9	DIFFIO_TX_RX_B18N/CLK6N
HSMC_CLK_IN_P2	V10	DIFFIO_TX_RX_B18P/CLK6P
CLK_LVDS_125_N	R11	DIFFIO_TX_RX_B20N/CLK7N
CLK_LVDS_125_P	P11	DIFFIO_TX_RX_B20P/CLK7P

BANK-4 (VCCIO = 2.5V)

		DIFFIO_TX_RX_B57N/PLL_B_CLKOUTN
		DIFFIO_TX_RX_B57P/PLL_B_CLKOUTP
W17	HSMC_TX_D_N12	
V17	HSMC_TX_D_P12	

BANK-6 (VCCIO = 1.5V)

CLK_DDR3_100_N	N15	DIFFIO_RX_R38N/CLK2N	DIFFIO_RX_R50N/DPCLK2/DQSn2R	L15	DDR3_DQS_N1
CLK_DDR3_100_P	N14	DIFFIO_RX_R38P/CLK2P	DIFFIO_RX_R50P/DPCLK3/DQS2R	L14	DDR3_DQS_P1
	K21	DIFFIO_RX_R40N/CLK3N	DIFFIO_RX_R69N/PLL_R_CLKOUTN	G17	
	K22	DIFFIO_RX_R40P/CLK3P	DIFFIO_RX_R69P/PLL_R_CLKOUTP	H17	

BANK-8 (VCCIO = 3.3V)

ENETA_TX_CLK	E10	DIFFIO_RX_T38N/CLK4N			
ENETB_TX_CLK	E11	DIFFIO_RX_T38P/CLK4P			
	J10	DIFFIO_RX_T40P/CLK5P	DIFFIO_RX_T52N/PLL_T_CLKOUTN	E6	IP_SECURITY
USB_CLK	H11	DIFFIO_RX_T40N/CLK5N	DIFFIO_RX_T52P/PLL_T_CLKOUTP	D6	HDMI_TX_CLK

10M50DAF484

CLK_LVDS_125_N	R33 100	CLK_LVDS_125_P
CLK_DDR3_100_N	R52 100	CLK_DDR3_100_P
HSMC_CLK_IN_N1	R94 DNI	HSMC_CLK_IN_P1
HSMC_CLK_IN_N2	R95 DNI	HSMC_CLK_IN_P2

HDMI TX

HDMI_TX_CLK	17
HSMC_TX_D_N12	15
HSMC_TX_D_P12	15

HSMC

HSMC_CLK_IN0	15
HSMC_CLK_IN_P[2:1]	5,15
HSMC_CLK_IN_N[2:1]	5,15

Ethernet

ENETA_RX_CLK	18
ENETB_RX_CLK	19
ENETA_TX_CLK	18
ENETB_TX_CLK	19
ENETA_GTX_CLK	18
ENETB_GTX_CLK	19

DDR3

DDR3_DQS_N1	13
DDR3_DQS_P1	13

From PLL

CLK_10_ADC	10
CLK_50_MAX10	10
CLK_25_MAX10	10
CLK_LVDS_125_P	10
CLK_LVDS_125_N	10
CLK_DDR3_100_P	10
CLK_DDR3_100_N	10
IP_SECURITY	16
USB_CLK	21

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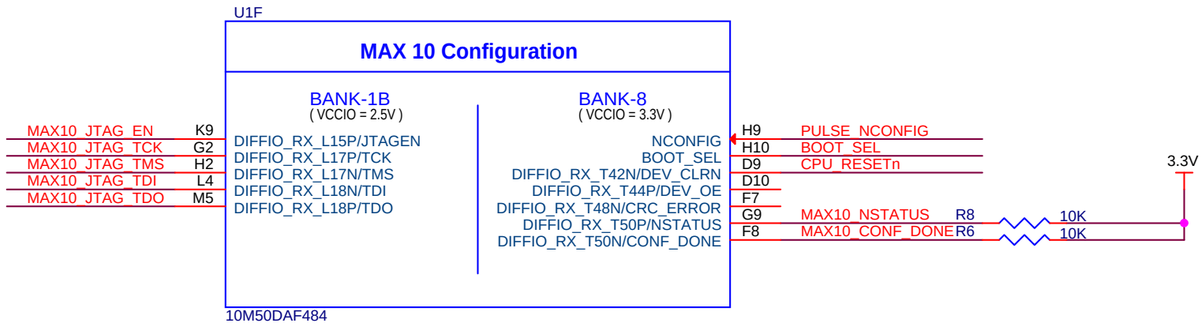
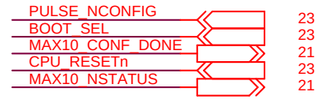
MAX10 Configuration



Configuration



JTAG

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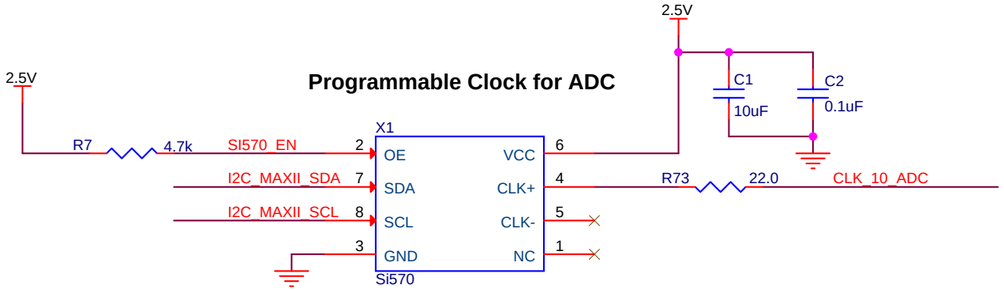
PLL

Programmable Clock for ADC



Notes:
Use Clock Control GUI
Default 10MHz

I2C Address 55 HEX

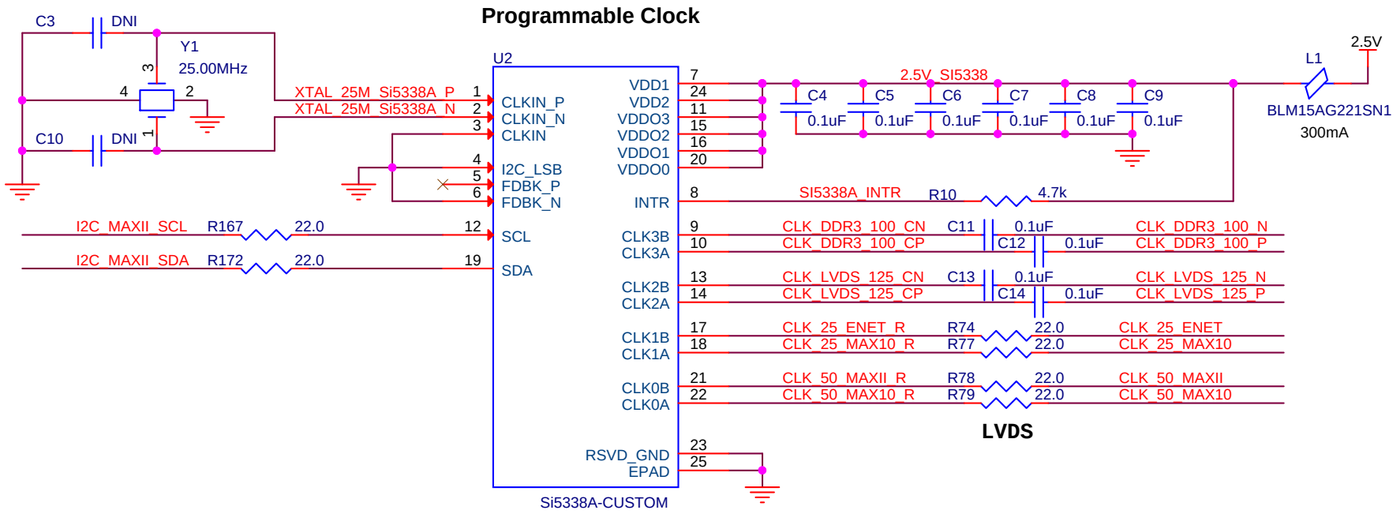
Clock control

I2C_MAXII_SCL 22,28
I2C_MAXII_SDA 22,28
SI5338A_INTR 22
SI570_EN 22

Clock out

CLK_10_ADC 8
CLK_50_MAX10 8
CLK_50_MAXII 21
CLK_25_ENET 18,19
CLK_25_MAX10 8
CLK_LVDS_125_P 8
CLK_LVDS_125_N 8
CLK_DDR3_100_P 8
CLK_DDR3_100_N 8

Programmable Clock



LVDS

Notes:
Si5338 Programmable Oscillator Use Clock Control GUI
(Defaults 50MHz, 25MHz, 125MHz, 100MHz)

I2C Address 70 HEX

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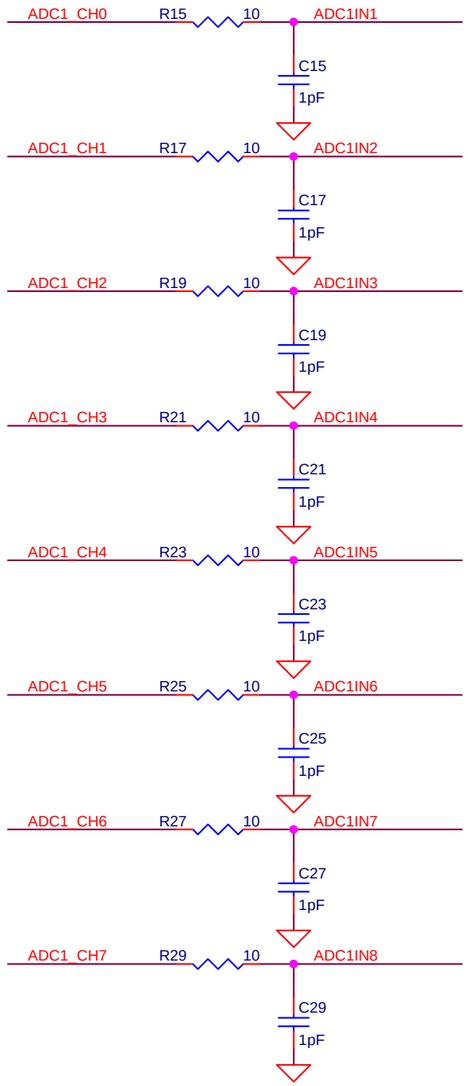
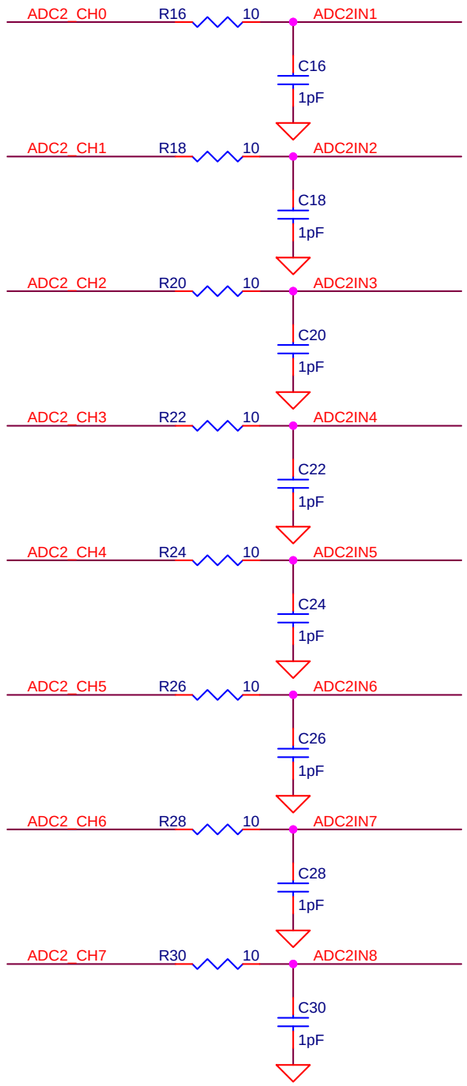
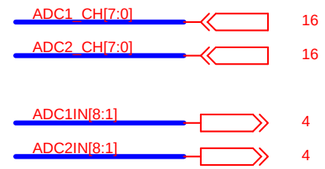
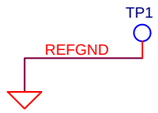
ADC Filter

Notes:
Put the 1pF capacitors close to each MAX10 analog pin.









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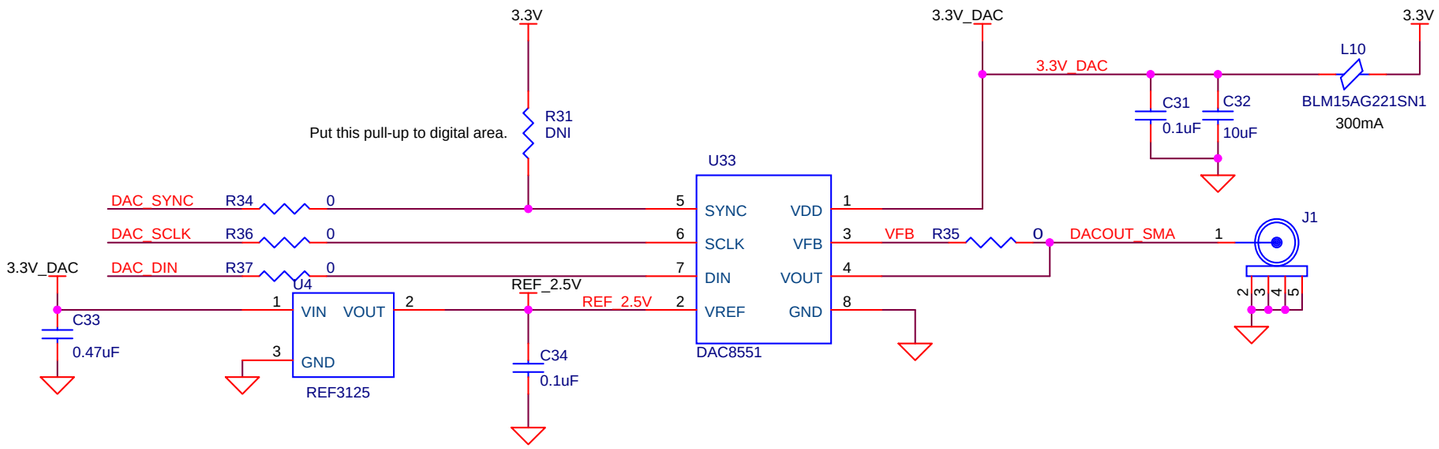
DAC



DAC_SYNC 7

DAC_SCLK 7

DAC_DIN 7

Notes:
1. Put 0.1uF capactor close to VREF pin.
2. Everything related to this DAC should be connected to analog ground.
3. For better DC accuracy, VFB should be connected to VOUT at loadpoints.
4. Thermal pad should be connected to GND.

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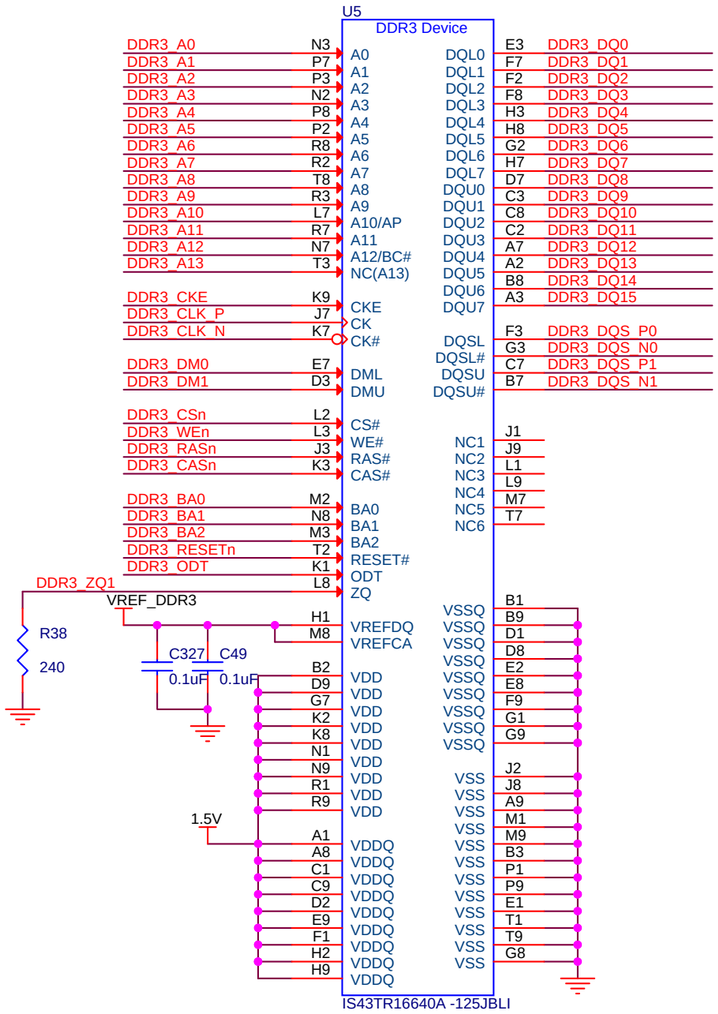
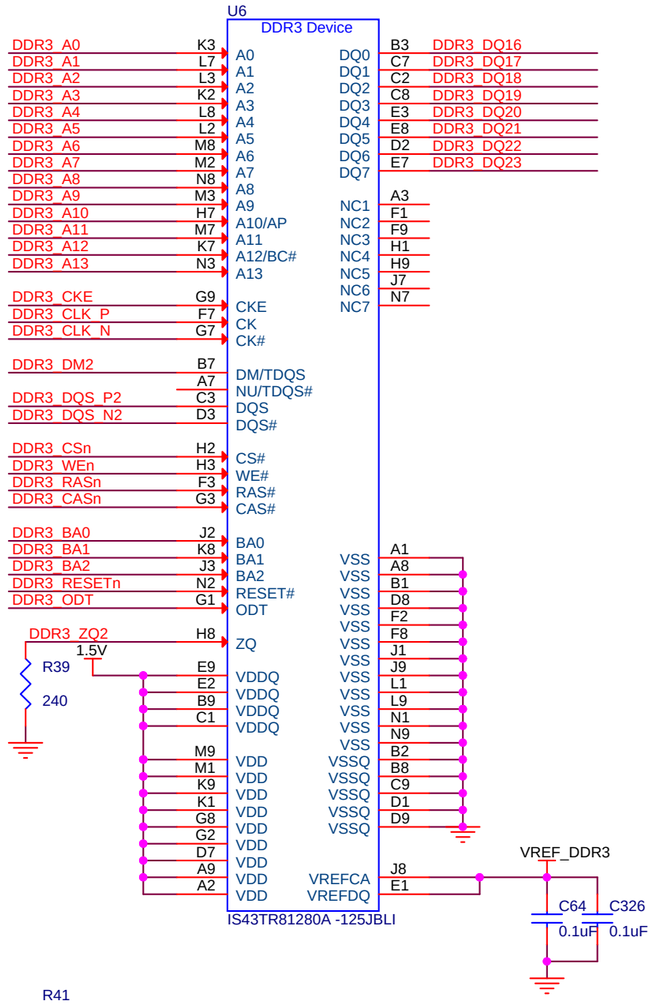
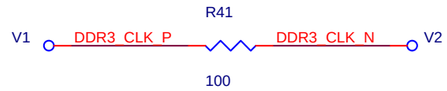
DDR3 SDRAM

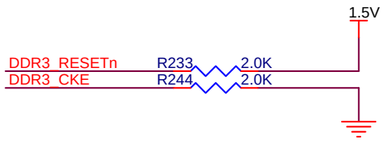
DDR3 SDRAM A (64Mx16)



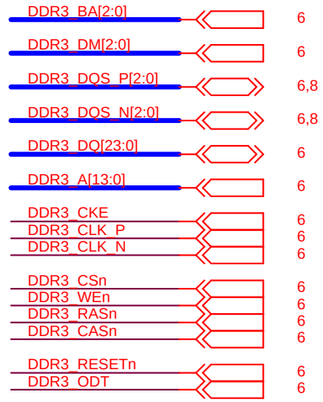
DDR3 SDRAM B (128Mx8)

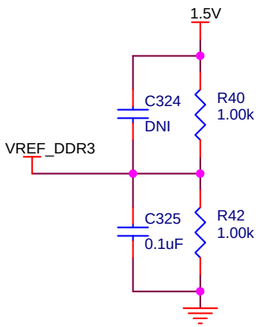






FPGA Interface





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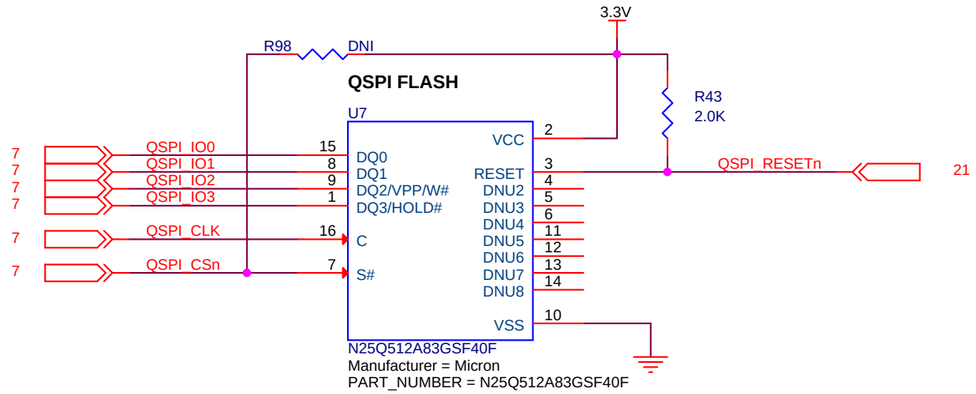
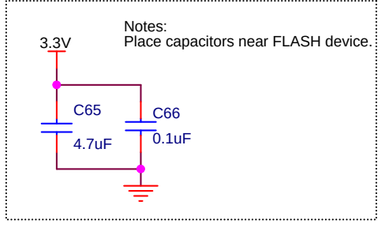
QSPI FLASH





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HSMC Port

FPGA Interface

HSMC_D[3:0] 5
HSMC_TX_D_P[16:0] 5,8
HSMC_TX_D_N[16:0] 5,8
HSMC_RX_D_P[16:0] 5
HSMC_RX_D_N[16:0] 5
HSMC_CLK_OUT_P[2:1] 5
HSMC_CLK_OUT_N[2:1] 5
HSMC_CLK_IN_P[2:1] 5,8
HSMC_CLK_IN_N[2:1] 5,8
HSMC_PRSNTn 5,22

J2

BANK 1

5	HSMC_SDA	33	34	HSMC_SCL	5
22	HSMC_JTAG_TCK	35	36	HSMC_JTAG_TMS	22
22	HSMC_JTAG_TDO	37	38	HSMC_JTAG_TDI	22
5	HSMC_CLK_OUT0	39	40	HSMC_CLK_IN0	8

BANK 2

	HSMC_D0	41	42	HSMC_D1	
	HSMC_D2	43	44	HSMC_D3	
		45	46		
	HSMC_TX_D_P0	47	48	HSMC_RX_D_P0	
	HSMC_TX_D_N0	49	50	HSMC_RX_D_N0	
		51	52		
	HSMC_TX_D_P1	53	54	HSMC_RX_D_P1	
	HSMC_TX_D_N1	55	56	HSMC_RX_D_N1	
		57	58		
	HSMC_TX_D_P2	59	60	HSMC_RX_D_P2	
	HSMC_TX_D_N2	61	62	HSMC_RX_D_N2	
		63	64		
	HSMC_TX_D_P3	65	66	HSMC_RX_D_P3	
	HSMC_TX_D_N3	67	68	HSMC_RX_D_N3	
		69	70		
	HSMC_TX_D_P4	71	72	HSMC_RX_D_P4	
	HSMC_TX_D_N4	73	74	HSMC_RX_D_N4	
		75	76		
	HSMC_TX_D_P5	77	78	HSMC_RX_D_P5	
	HSMC_TX_D_N5	79	80	HSMC_RX_D_N5	
		81	82		
	HSMC_TX_D_P6	83	84	HSMC_RX_D_P6	
	HSMC_TX_D_N6	85	86	HSMC_RX_D_N6	
		87	88		
	HSMC_TX_D_P7	89	90	HSMC_RX_D_P7	
	HSMC_TX_D_N7	91	92	HSMC_RX_D_N7	
		93	94		
	HSMC_CLK_OUT_P1	95	96	HSMC_CLK_IN_P1	
	HSMC_CLK_OUT_N1	97	98	HSMC_CLK_IN_N1	
		99	100		

BANK 3

	HSMC_TX_D_P8	101	102	HSMC_RX_D_P8	
	HSMC_TX_D_N8	103	104	HSMC_RX_D_N8	
		105	106		
	HSMC_TX_D_P9	107	108	HSMC_RX_D_P9	
	HSMC_TX_D_N9	109	110	HSMC_RX_D_N9	
		111	112		
	HSMC_TX_D_P10	113	114	HSMC_RX_D_P10	
	HSMC_TX_D_N10	115	116	HSMC_RX_D_N10	
		117	118		
	HSMC_TX_D_P11	119	120	HSMC_RX_D_P11	
	HSMC_TX_D_N11	121	122	HSMC_RX_D_N11	
		123	124		
	HSMC_TX_D_P12	125	126	HSMC_RX_D_P12	
	HSMC_TX_D_N12	127	128	HSMC_RX_D_N12	
		129	130		
	HSMC_TX_D_P13	131	132	HSMC_RX_D_P13	
	HSMC_TX_D_N13	133	134	HSMC_RX_D_N13	
		135	136		
	HSMC_TX_D_P14	137	138	HSMC_RX_D_P14	
	HSMC_TX_D_N14	139	140	HSMC_RX_D_N14	
		141	142		
	HSMC_TX_D_P15	143	144	HSMC_RX_D_P15	
	HSMC_TX_D_N15	145	146	HSMC_RX_D_N15	
		147	148		
	HSMC_TX_D_P16	149	150	HSMC_RX_D_P16	
	HSMC_TX_D_N16	151	152	HSMC_RX_D_N16	
		153	154		
	HSMC_CLK_OUT_P2	155	156	HSMC_CLK_IN_P2	
	HSMC_CLK_OUT_N2	157	158	HSMC_CLK_IN_N2	
		159	160	HSMC_PRSNTn	

		1	2		
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		11	12		
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		161	162		
		163	164		
		165	166		
		167	168		
		169	170		
		171	172		

3.3V
12V
GND_1_1 GND_1_2 GND_1_3 GND_1_4 GND_2_1 GND_2_2 GND_2_3 GND_2_4 GND_3_1 GND_3_2 GND_3_3 GND_3_4
PSNTn
HSMC

Note:
Place capacitors near HSM connector.

12V C67 10uF
3.3V C68 10uF

2.5V
R45 49.9
D2 GREEN_LED
HSMC_PRSNTn

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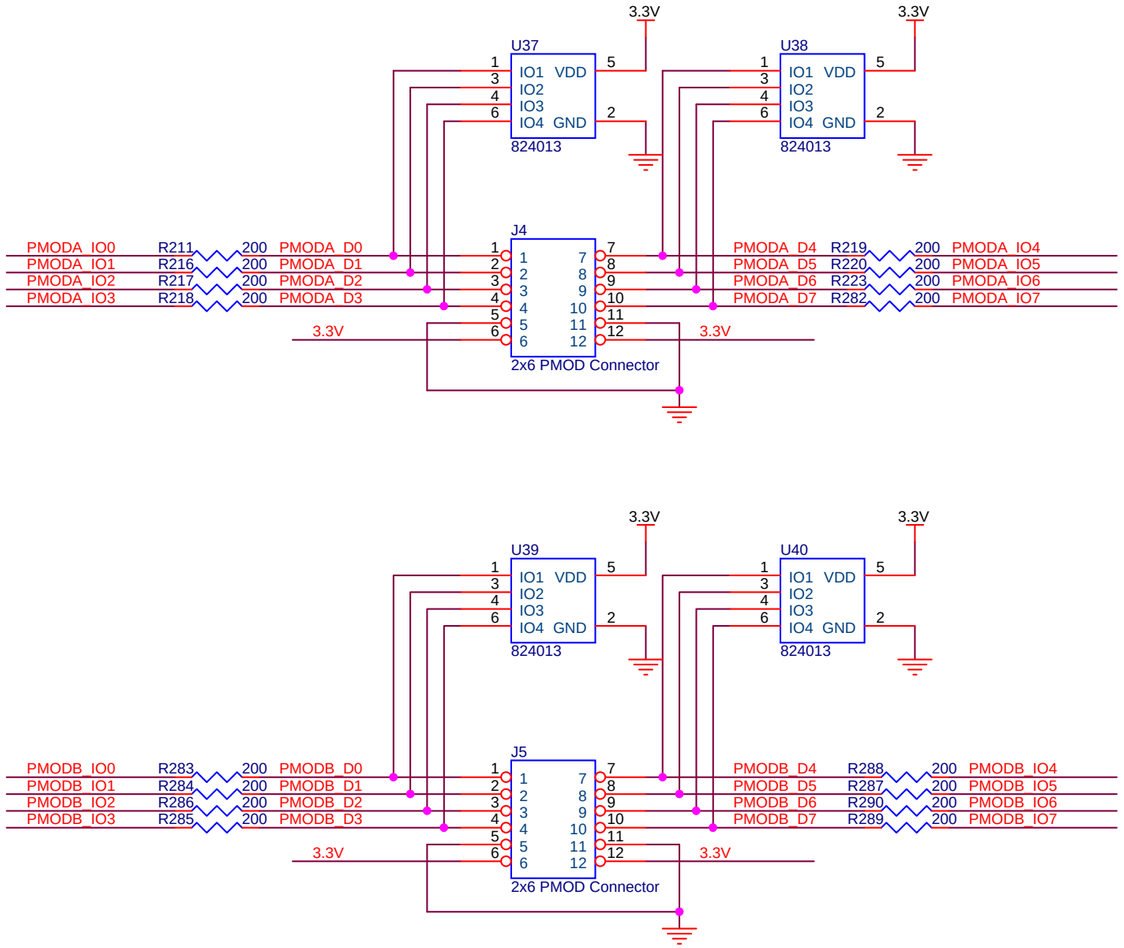
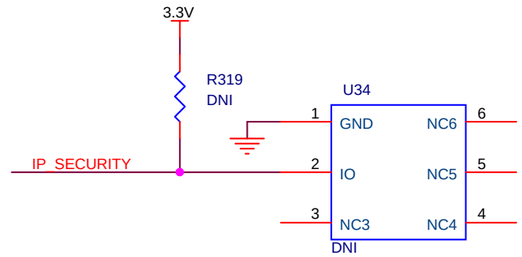
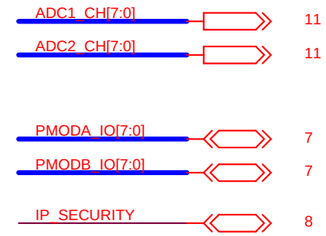
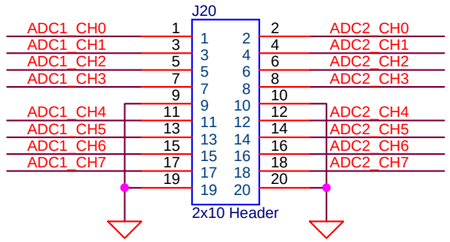
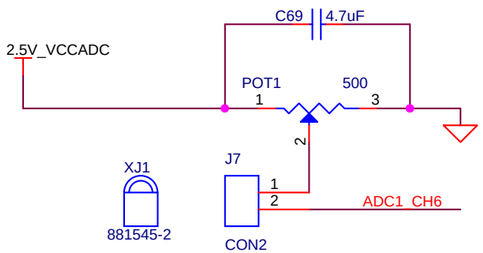
GPIO, PMOD











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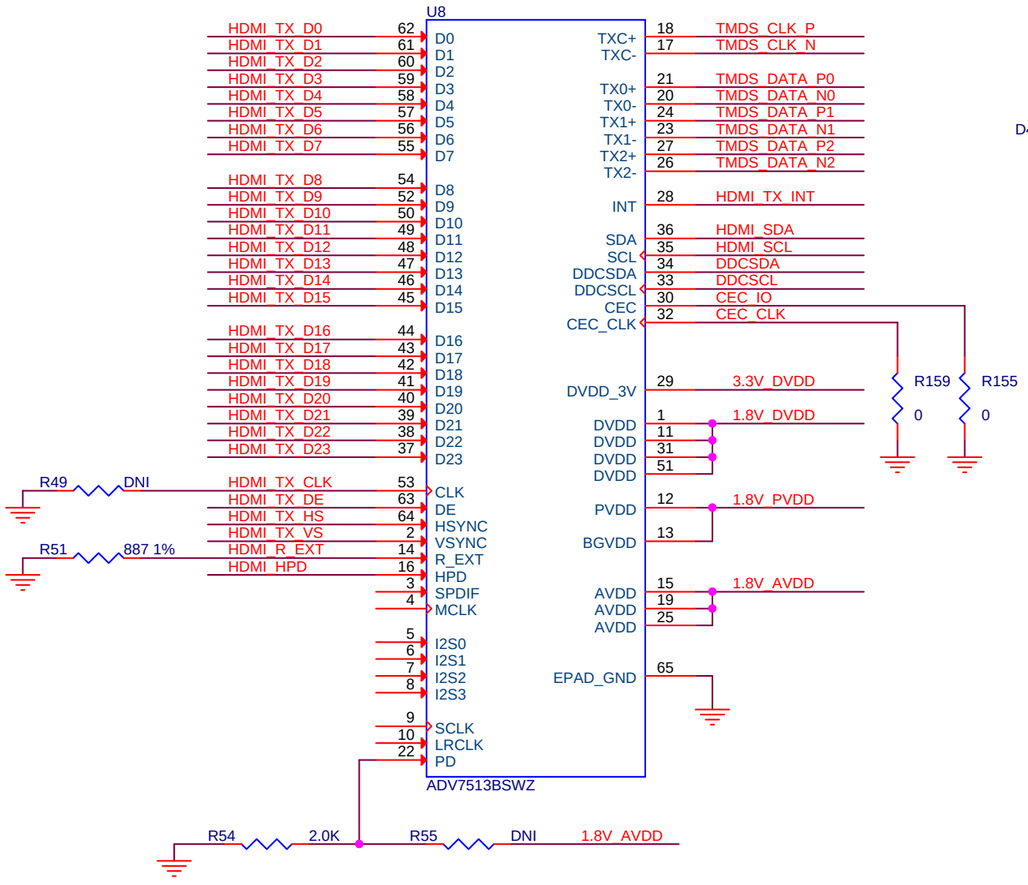
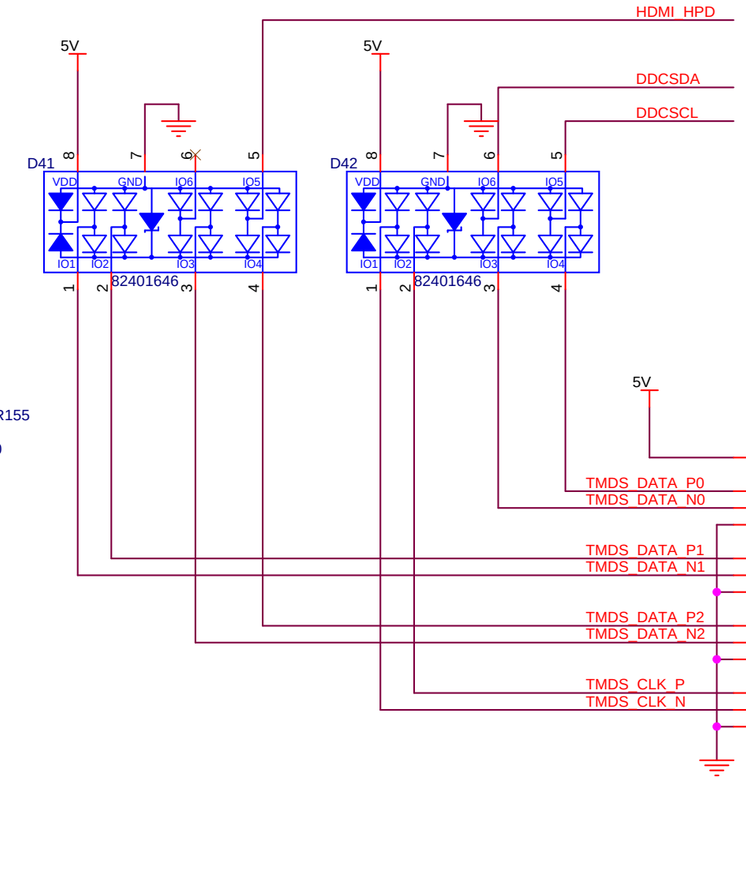
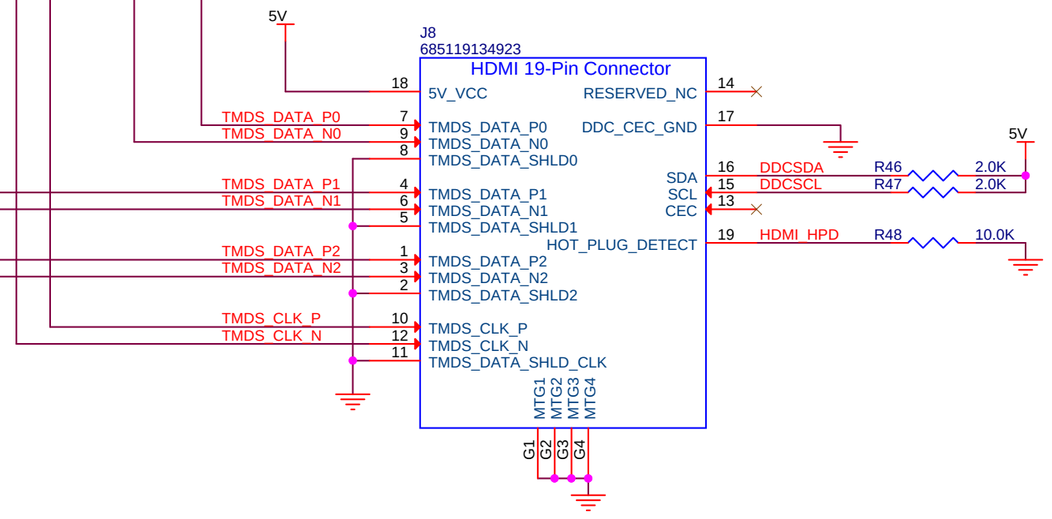
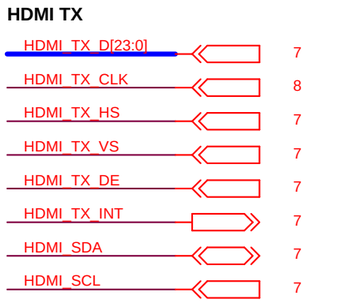
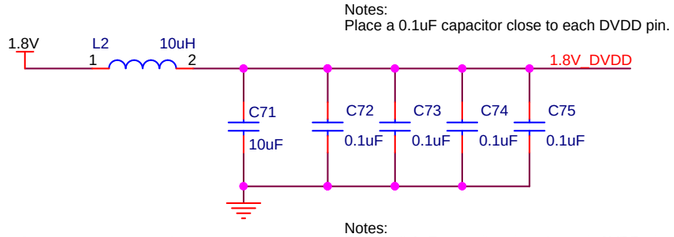
HDMI

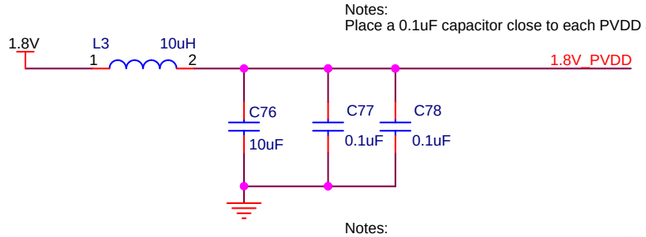


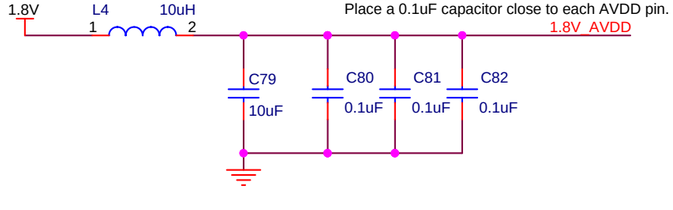


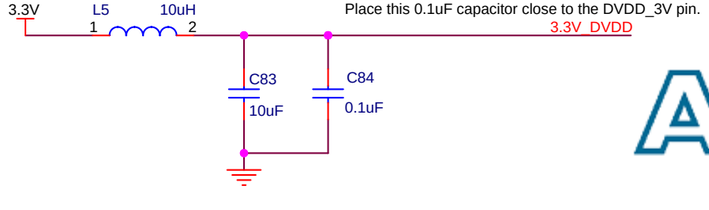












Title	MAX10 FPGA Development Kit (6XX-44292R)	
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10/100/1000 Ethernet A

Ethernet PHY A

2.5V
R59 4.7k ENET_MDIO 5,19
R60 4.7k ENET_MDC 5,19
R61 4.7k ENETA_INTn 5
R62 4.7k ENETA_RESETn 5

RJ45
RJ1A
7499151120
Green
Yellow
2.5V A11
ENETA_LED_LINK1000 R206 49.9 A12
ENETA_LED_LINK100 R301 DNI
2.5V A14
ENETA_LED_TX R207 49.9 A13
LED_G+
LED_G-
LED_Y+
LED_Y-
VCC A1
TD0_P A2
TD0_N A3
TD1_P A4
TD1_N A7
TD2_P A5
TD2_N A6
TD3_P A8
TD3_N A9
GND A10
GND_TAB A16
GND_TAB A15
R205 DNI

2.5V
ENETA_LED_TX 61
ENETA_CONF4 60
ENETA_LED_RX 58

U9A
Ethernet PHY, 88E1111

ENETA_RESETn	28	COMA
	27	RESET_N
	65	CONFIG0
	64	CONFIG1
	63	CONFIG2
	61	CONFIG3
	60	CONFIG4
	59	CONFIG5
	58	CONFIG6
ENETA_MDI_P0	29	MDI0_P
ENETA_MDI_N0	31	MDI0_N
ENETA_MDI_P1	33	MDI1_P
ENETA_MDI_N1	34	MDI1_N
ENETA_MDI_P2	39	MDI2_P
ENETA_MDI_N2	41	MDI2_N
ENETA_MDI_P3	42	MDI3_P
ENETA_MDI_N3	43	MDI3_N
ENET_MDIO	24	MDIO
ENET_MDC	25	MDC
ENETA_INTn	23	INT_N
V27 ENETA_HSDAC_P	37	HSDAC_P
V28 ENETA_HSDAC_N	38	HSDAC_N
ENETA_RSET	30	RSET
	56	SEL_FREQ
CLK_25_ENET	22	125CLK
	55	XTAL1
	54	XTAL2
	53	VSSC
ENETA_TRST_N	47	TRST_N
	49	TCK
	44	TDI
	50	TDO
	46	TMS

MDI INTERFACE
MGMT
TEST
JTAG

R71 4.99K 1%
R72 4.7k

GMII/MII/TBI INTERFACE

GTX_CLK	8	ENETA_GTX_CLK
TX_CLK	4	ENETA_TX_CLK
TX_EN	9	ENETA_TX_EN
TX_ER	7	ENETA_TX_ER
TXD0	11	ENETA_TX_D0
TXD1	12	ENETA_TX_D1
TXD2	14	ENETA_TX_D2
TXD3	16	ENETA_TX_D3
TXD4	17	
TXD5	18	
TXD6	19	
TXD7	20	
RXCLK	2	ENETA_RX_CLK
RX_DV	94	ENETA_RX_DV
RX_ER	3	ENETA_RX_ER
RXD0	95	ENETA_RX_D0
RXD1	92	ENETA_RX_D1
RXD2	93	ENETA_RX_D2
RXD3	91	ENETA_RX_D3
RXD4	90	
RXD5	89	
RXD6	87	
RXD7	86	
CRS	84	ENETA_RX_CRS
COL	83	ENETA_RX_COL

SGMII INTERFACE

S_CLK_P	79	
S_CLK_N	80	
S_IN_P	82	
S_IN_N	81	
S_OUT_P	77	
S_OUT_N	75	
LED_TX	68	ENETA_LED_TX
LED_RX	69	ENETA_LED_RX
LED_DUPLEX	70	ENETA_LED_DUPLEX
LED_LINK1000	73	ENETA_LED_LINK1000
LED_LINK100	74	ENETA_LED_LINK100
LED_LINK10	76	

FPGA Interface

ENETA_TX_D[3:0]	4
ENETA_GTX_CLK	8
ENETA_TX_CLK	8
ENETA_TX_EN	4
ENETA_TX_ER	4
ENETA_RX_D[3:0]	4
ENETA_RX_CLK	8
ENETA_RX_DV	4
ENETA_RX_ER	4
ENETA_RX_CRS	4
ENETA_RX_COL	4
CLK_25_ENET	10,19
ENETA_LED_LINK100	5

Notes:
MDI signals termination

C85	0.01uF	ENETA_MDI_0	R63 49.9	ENETA_MDI_P0
			R64 49.9	ENETA_MDI_N0
C86	0.01uF	ENETA_MDI_1	R65 49.9	ENETA_MDI_P1
			R66 49.9	ENETA_MDI_N1
C87	0.01uF	ENETA_MDI_2	R67 49.9	ENETA_MDI_P2
			R68 49.9	ENETA_MDI_N2
C88	0.01uF	ENETA_MDI_3	R69 49.9	ENETA_MDI_P3
			R70 49.9	ENETA_MDI_N3

RGMII Mode (default)

ENETA_CONF4 R75 0 ENETA_LED_DUPLEX RGMII Mode
2.5V
R76 DNI MII Mode

Notes:
Overlap R75 and R76 pads

2.5V
U9B
Ethernet PHY, 88E1111

26	48	VDDOX
5	21	VDDO
88	96	VDDO
		VDDO
72	66	VDDOH
	52	VDDOH
		VDDOH
32	36	AVDD
35	40	AVDD
45	78	AVDD
1	6	DVDD
10	15	DVDD
57	62	DVDD
67	71	DVDD
85		DVDD
13	51	NC1 NC2
97		VSS

1.2V

2.5V
Notes:
Place capacitors near Ethernet PHY A pins
C89 0.1uF
C90 0.1uF
C91 0.1uF
C92 0.1uF
C93 0.1uF
C94 0.1uF
C95 0.1uF
C96 0.1uF

1.2V
C97 0.1uF
C98 0.1uF
C99 0.1uF
C100 0.1uF
C101 0.1uF

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10/100/1000 Ethernet B

Ethernet PHY B

2.5V
R83 4.7k ENETB_INTn 5
R82 4.7k ENETB_RESETn 5

RJ45
RJ1B
Green
LED_G+
LED_G-
Yellow
LED_Y+
LED_Y-
2.5V B11
ENETB_LED_LINK1000 R208 49.9 B12
ENETB_LED_LINK100 R302 DNI
2.5V B14
ENETB_LED_TX R209 49.9 B13
VCC B1
TD0_P B2
TD0_N B3
TD1_P B4
TD1_N B7
TD2_P B5
TD2_N B6
TD3_P B8
TD3_N B9
GND B10
GND_TAB
GND_TAB
B16 B15
7499151120
R204 DNI

U10A
ENETB_RESETn 27 28 COMA RESET_N
ENETB_LED_TX 65 CONFIG0
64 CONFIG1
63 CONFIG2
ENETB_LED_TX 61 CONFIG3
ENETB_CONF4 60 CONFIG4
59 CONFIG5
ENETB_LED_RX 58 CONFIG6
2.5V
2.5V
ENETB_MDI_P0 29 MDI0_P
ENETB_MDI_N0 31 MDI0_N
ENETB_MDI_P1 33 MDI1_P
ENETB_MDI_N1 34 MDI1_N
ENETB_MDI_P2 39 MDI2_P
ENETB_MDI_N2 41 MDI2_N
ENETB_MDI_P3 42 MDI3_P
ENETB_MDI_N3 43 MDI3_N
MDI INTERFACE
ENET_MDIO 24 MDIO
ENET_MDC 25 MDC
ENETB_INTn 23 INT_N
MGNT
V29 ENETB_HSDAC_P 37 HSDAC_P
V30 ENETB_HSDAC_N 38 HSDAC_N
TEST
ENETB_RSET 30 RSET
56 SEL_FREQ
22 125CLK
CLK_25_ENET 55 XTAL1
54 XTAL2
53 VSSC
ENETB_TRST_N 47 TRST_N
49 TCK
44 TDI
50 TDO
46 TMS
JTAG
R92 4.99K 1%
R93 4.7k
Ethernet PHY, 88E1111

GMII/MII/TBI INTERFACE
GTX_CLK 8 ENETB_GTX_CLK
TX_CLK 4 ENETB_TX_CLK
TX_EN 9 ENETB_TX_EN
TX_ER 7 ENETB_TX_ER
TXD0 11 ENETB_TX_D0
TXD1 12 ENETB_TX_D1
TXD2 14 ENETB_TX_D2
TXD3 16 ENETB_TX_D3
TXD4 17
TXD5 18
TXD6 19
TXD7 20
RXCLK 2 ENETB_RX_CLK
RX_DV 94 ENETB_RX_DV
RX_ER 3 ENETB_RX_ER
RXD0 95 ENETB_RX_D0
RXD1 92 ENETB_RX_D1
RXD2 93 ENETB_RX_D2
RXD3 91 ENETB_RX_D3
RXD4 90
RXD5 89
RXD6 87
RXD7 86
CRS 84 ENETB_RX_CRS
COL 83 ENETB_RX_COL
SGMII INTERFACE
S_CLK_P 79
S_CLK_N 80
S_IN_P 82
S_IN_N 81
S_OUT_P 77
S_OUT_N 75
LED_TX 68 ENETB_LED_TX
LED_RX 69 ENETB_LED_RX
LED_DUPLEX 70 ENETB_LED_DUPLEX
LED_LINK1000 73 ENETB_LED_LINK1000
LED_LINK100 74 ENETB_LED_LINK100
LED_LINK10 76

FPGA Interface

ENETB_TX_D[3:0] 4
ENETB_GTX_CLK 8
ENETB_TX_CLK 8
ENETB_TX_EN 4
ENETB_TX_ER 4
ENETB_RX_D[3:0] 4
ENETB_RX_CLK 8
ENETB_RX_DV 4
ENETB_RX_ER 4
ENETB_RX_CRS 4
ENETB_RX_COL 4
CLK_25_ENET 10,18
ENETB_LED_LINK100 5
ENET_MDIO 5,18
ENET_MDC 5,18

Notes:
MDI signals termination

C102 0.01uF ENETB_MDI_0 R84 49.9 ENETB_MDI_P0
C103 0.01uF ENETB_MDI_1 R85 49.9 ENETB_MDI_N0
C104 0.01uF ENETB_MDI_2 R86 49.9 ENETB_MDI_P1
C105 0.01uF ENETB_MDI_3 R87 49.9 ENETB_MDI_N1
R88 49.9 ENETB_MDI_P2
R89 49.9 ENETB_MDI_N2
R90 49.9 ENETB_MDI_P3
R91 49.9 ENETB_MDI_N3

RGMII Mode (default)

ENETB_CONF4 R96 0 ENETB_LED_DUPLEX RGMII Mode
R97 DNI 2.5V MII Mode

Notes:
Overlap R96 and R97 pads

Notes:
Place capacitors near Ethernet PHY B pins

2.5V
C106 0.1uF
C107 0.1uF
C108 0.1uF
C109 0.1uF
C110 0.1uF
C111 0.1uF
C112 0.1uF
C113 0.1uF

1.2V
C114 0.1uF
C115 0.1uF
C116 0.1uF
C117 0.1uF
C118 0.1uF

2.5V
U10B
26 48 5 21 88 96 72 66 52
VDDOX VDDOX VDDO VDDO VDDO VDDO VDDOH VDDOH VDDOH
32 AVDD
36 AVDD
35 AVDD
40 AVDD
45 AVDD
78 AVDD
13 NC1
51 NC2
97 VSS
DVDD 1
DVDD 6
DVDD 10
DVDD 15
DVDD 57
DVDD 62
DVDD 67
DVDD 71
DVDD 85
1.2V
Ethernet PHY, 88E1111

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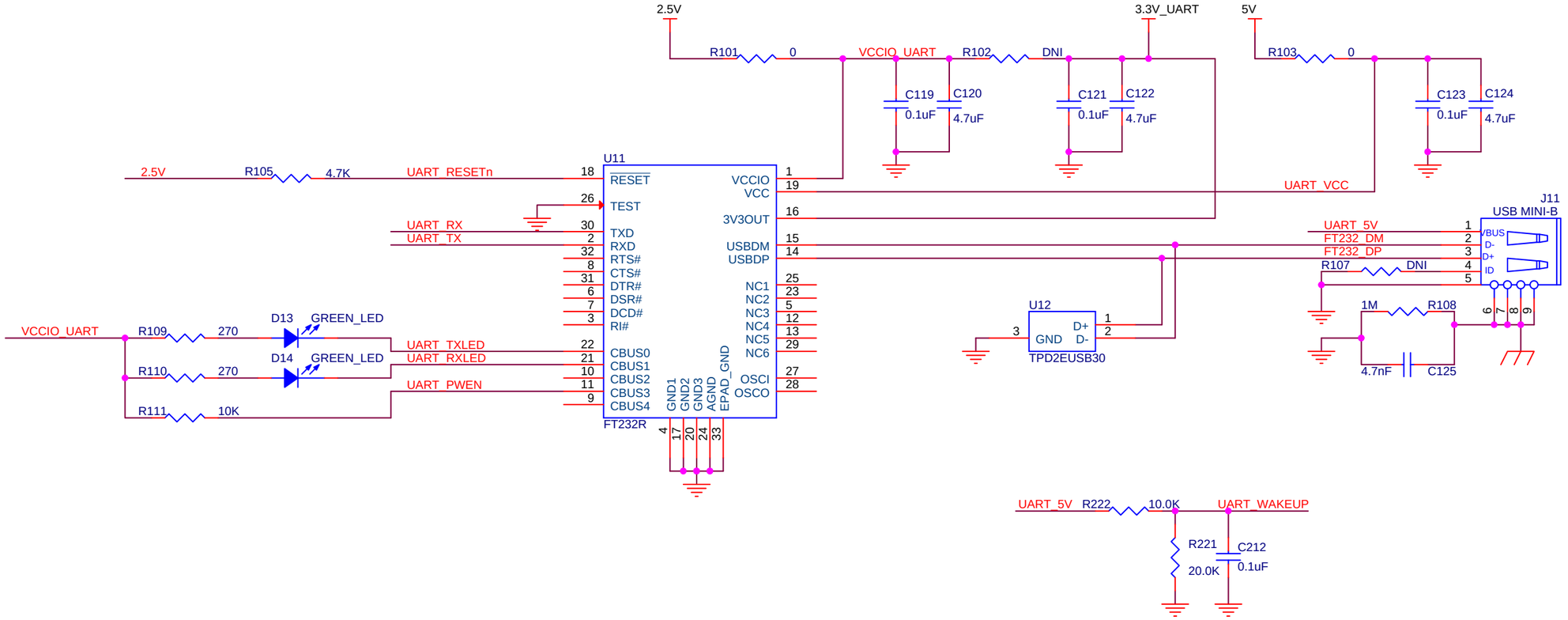
USB to UART

FPGA Interface

UART_RX 5
UART_TX 5
UART_RESETn 21
UART_WAKEUP 21

2.5V default 3.3V optional



Altera Corporation, 301, Bibo Rd #888, Shanghai, China, 201203

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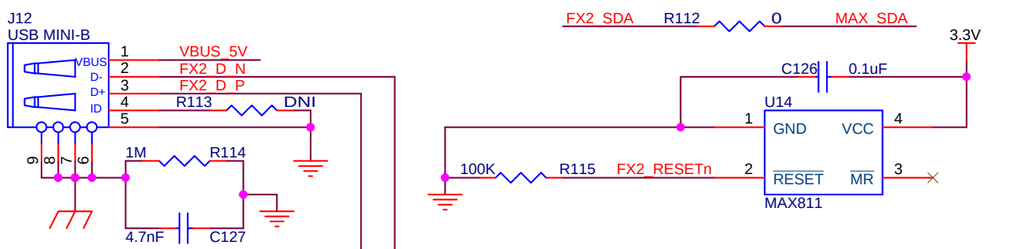
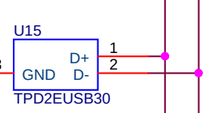
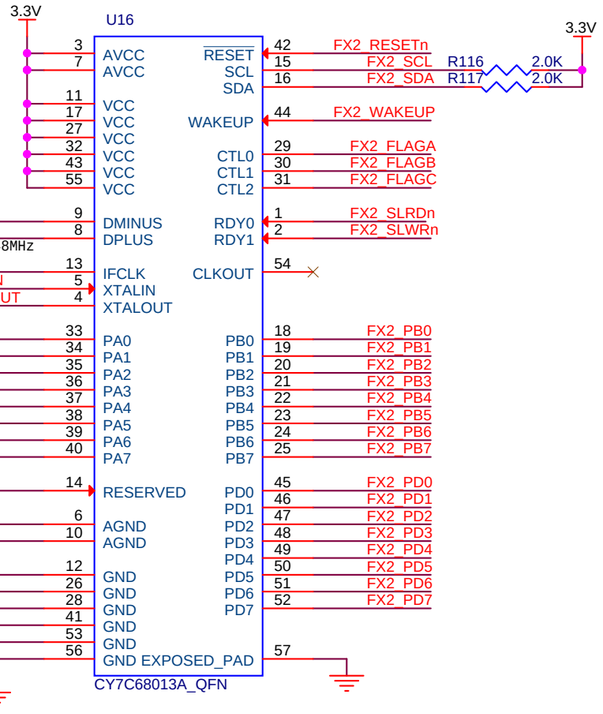
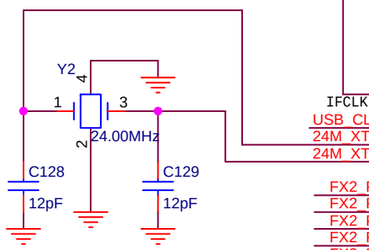
On-Board USB Blaster II-1

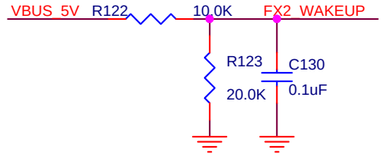




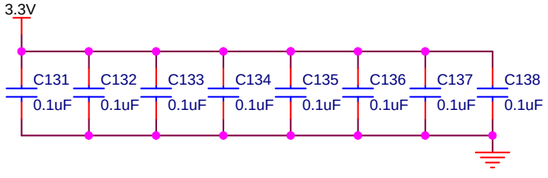


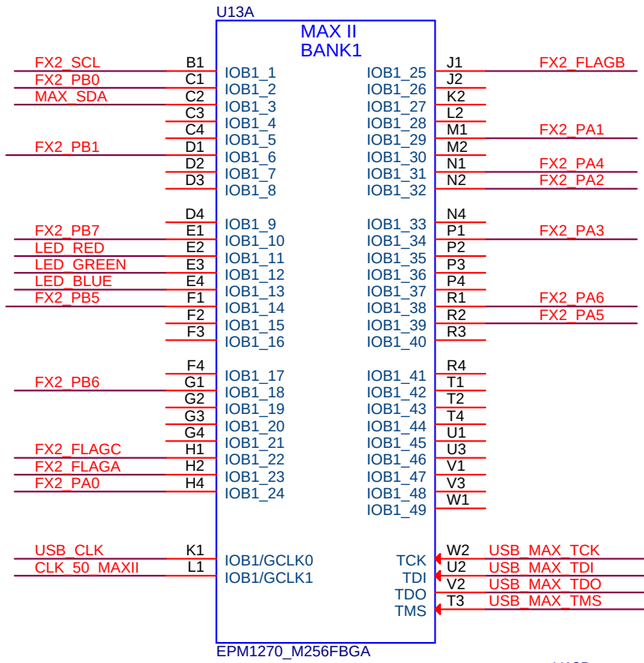


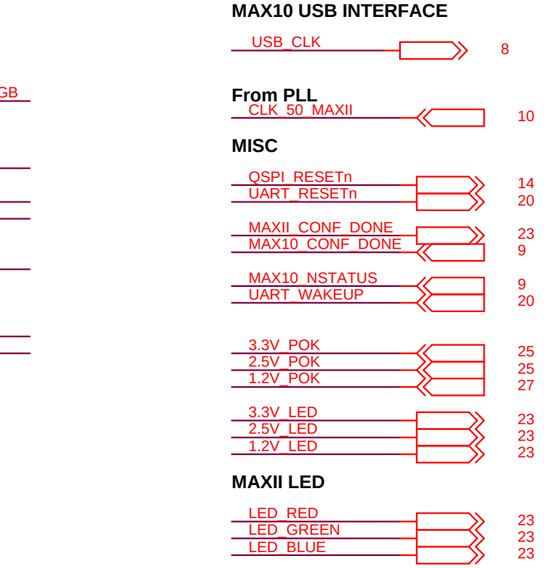
IFCLK = 48MHz

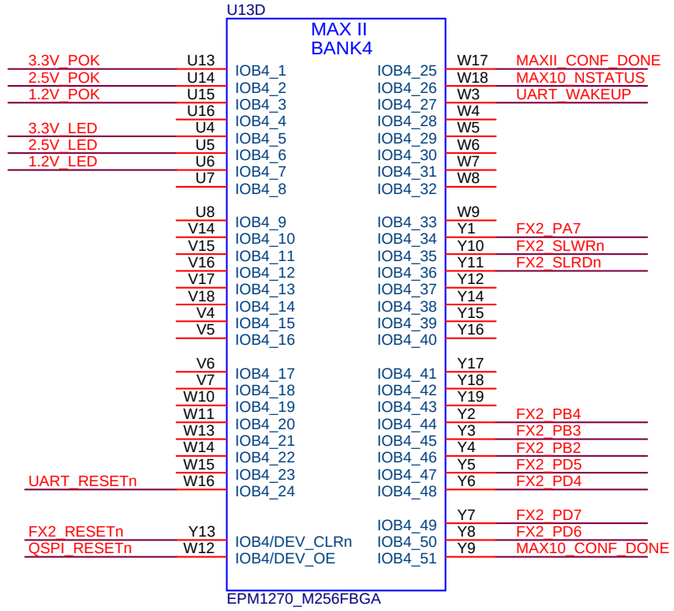


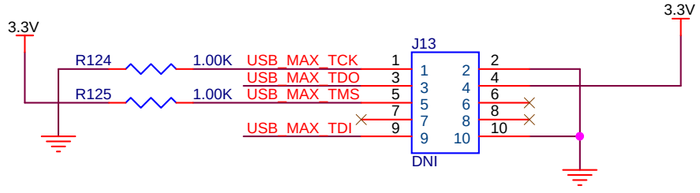
PLACE NEAR CY7C68013A











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On-Board USB Blaster II-2

U13B
MAX II
BANK2
EPM1270_M256FBGA

SI5338A_INTR	A1	IOB2_1	IOB2_25	B14	HSMC_JTAG_MASTERn
	A10	IOB2_2	IOB2_26	B15	I2C_MAXII_SCL
SI570_EN	A11	IOB2_3	IOB2_27	B16	I2C_MAXII_SDA
HSMC_PRSNTn	A12	IOB2_4	IOB2_28	B17	
	A13	IOB2_5	IOB2_29	B18	
	A14	IOB2_6	IOB2_30	B19	
	A15	IOB2_7	IOB2_31	B2	
	A16	IOB2_8	IOB2_32	B3	
	A17	IOB2_9	IOB2_33	B4	
MAX10_JTAG_TDO	A18	IOB2_10	IOB2_34	B5	
	A19	IOB2_11	IOB2_35	B6	
	A2	IOB2_12	IOB2_36	B7	
	A20	IOB2_13	IOB2_37	B8	
	A3	IOB2_14	IOB2_38	B9	
	A4	IOB2_15	IOB2_39	C14	
	A5	IOB2_16	IOB2_40	C15	
	A6	IOB2_17	IOB2_41	C16	
HSMC_JTAG_TDO	A7	IOB2_18	IOB2_42	C17	
HSMC_JTAG_TMS	A8	IOB2_19	IOB2_43	C5	
HSMC_JTAG_TCK	A9	IOB2_20	IOB2_44	C6	
	B10	IOB2_21	IOB2_45	C7	
	B11	IOB2_22	IOB2_46	D13	
	B12	IOB2_23	IOB2_47	D14	
	B13	IOB2_24	IOB2_48	D15	
			IOB2_49	D16	
			IOB2_50	D5	
			IOB2_51	D6	
			IOB2_52	D7	
			IOB2_53	D8	

2.5V
R243 10.0K MAX10_JTAG_EN
R126 10.0K MAX10_JTAG_TDI
R127 10.0K MAX10_JTAG_TMS
R128 1.00K MAX10_JTAG_TCK
2.5V
R129 10.0K HSMC_JTAG_TDI
R130 10.0K HSMC_JTAG_TMS
R131 1.00K HSMC_JTAG_TCK

U13C
MAX II
BANK3
EPM1270_M256FBGA

USB_DATA2	B20	IOB3_1	IOB3_25	J20	USB_DATA0
USB_DATA3	C18	IOB3_2	IOB3_26	K19	
	C19	IOB3_3	IOB3_27	K20	USB_RDn
USB_EMPTY	C20	IOB3_4	IOB3_28	L19	USB_DATA6
	D17	IOB3_5	IOB3_29	M19	USB_DATA5
	D18	IOB3_6	IOB3_30	N17	
	D19	IOB3_7	IOB3_31	N19	
USB_ADDR0	D20	IOB3_8	IOB3_32	N20	USB_DATA7
	E17			P17	MAX10_BYPASSn
	E18	IOB3_9	IOB3_33	P18	HSMC_BYPASSn
JTAG_HEADER_TMS	E19	IOB3_10	IOB3_34	P19	
USB_FULL	E20	IOB3_11	IOB3_35	P20	
	F17	IOB3_12	IOB3_36	R17	
	F18	IOB3_13	IOB3_37	R18	
	F19	IOB3_14	IOB3_38	R19	
USB_ADDR1	F20	IOB3_15	IOB3_39	R20	
		IOB3_16	IOB3_40		
JTAG_HEADER_TDO	G17	IOB3_17	IOB3_41	T17	
	G18	IOB3_18	IOB3_42	T18	
JTAG_HEADER_TDI	G19	IOB3_19	IOB3_43	T19	USB_WRn
USB_OEn	G20	IOB3_20	IOB3_44	T20	USB_SCL
	H17	IOB3_21	IOB3_45	U17	
	H19	IOB3_22	IOB3_46	U18	
USB_DATA1	H20	IOB3_23	IOB3_47	U19	
USB_DISABLEn	J19	IOB3_24	IOB3_48	U20	USB_RESETn
				V19	
			IOB3_49	V20	USB_SDA
			IOB3_50	W19	
			IOB3_51	W20	JTAG_SAFE
JTAG_HEADER_TCK	M20	IOB3/GCLK2	IOB3_52	Y20	JTAG_LOCK
USB_DATA4	L20	IOB3/GCLK3	IOB3_53		

3.3V
R132 1.00k USB_SCL
R133 1.00k USB_SDA
R134 1.00k USB_FULL
R135 1.00k USB_EMPTY

R56 DNI HSMC_JTAG_MASTERn

JTAG_HEADER_TCK R136 DNI C139 DNI
R137 1.00k

U13E
MAX II
Power
EPM1270_M256FBGA

J4	GNDINT	VCCINT	K4	2.5V	
U12	GNDINT	VCCINT	U11	2.5V	
M17	GNDINT	VCCINT	L17	2.5V	
D12	GNDINT	VCCINT	D11	2.5V	
H3	GNDIO	VCCIO1	K3	3.3V	
J3	GNDIO	VCCIO1	L3	3.3V	
M4	GNDIO	VCCIO1	L4	3.3V	
N3	GNDIO	VCCIO1	M3	3.3V	
U9	GNDIO				
V8	GNDIO	VCCIO2	C9	2.5V	
V9	GNDIO	VCCIO2	C10	2.5V	
V13	GNDIO	VCCIO2	D10	2.5V	
H18	GNDIO	VCCIO2	C11	2.5V	
J17	GNDIO		J18		
N18	GNDIO	VCCIO3	K17	3.3V	
C8	GNDIO	VCCIO3	K18	3.3V	
D9	GNDIO	VCCIO3	L18	3.3V	
C12	GNDIO	VCCIO3			
C13	GNDIO		U10	3.3V	
M18	GNDIO	VCCIO4	V10	3.3V	
		VCCIO4	V11	3.3V	
		VCCIO4	V12	3.3V	
		VCCIO4			

Notes:
Place capacitors near MAX II device.

2.5V	C140	0.1uF	C141	0.1uF	
3.3V	C142	0.1uF	C143	0.1uF	
2.5V	C144	0.1uF	C145	0.1uF	
3.3V	C146	0.1uF	C147	0.1uF	
3.3V	C148	0.1uF	C149	0.1uF	

USB Blaster Programming Header
(uses JTAG mode only)

3.3V
R138 1.00k USB_DISABLEn
3.3V
J14
2X5_100mil

2	2	1	1	JTAG_HEADER_TCK_R	R247 22.0 JTAG_HEADER_TCK
4	4	3	3	JTAG_HEADER_TDO_R	R248 22.0 JTAG_HEADER_TDO
6	6	5	5	JTAG_HEADER_TMS_R	R266 22.0 JTAG_HEADER_TMS
8	8	7	7	JTAG_LOCK_R	R267 22.0 JTAG_LOCK
10	10	9	9	JTAG_HEADER_TDI_R	R276 22.0 JTAG_HEADER_TDI

3.3V
R139 1.00k
R140 1.00k

MAX10 USB INTERFACE

USB_DATA[7:0]		7
USB_ADDR[1:0]		7
USB_FULL		7
USB_EMPTY		7
USB_SCL		7
USB_SDA		7
USB_RESETn		7
USB_OEn		7
USB_RDn		7
USB_WRn		7
I2C_MAXII_SCL		10,28
I2C_MAXII_SDA		10,28

JTAG INTERFACE

MAX10_JTAG_EN		9
MAX10_JTAG_TCK		9
MAX10_JTAG_TMS		9
MAX10_JTAG_TDO		9
MAX10_JTAG_TDI		9
HSMC_JTAG_TCK		15
HSMC_JTAG_TMS		15
HSMC_JTAG_TDO		15
HSMC_JTAG_TDI		15
HSMC_PRSNTn		5,15
MAX10_BYPASSn		23
HSMC_BYPASSn		23
SI570_EN		10
SI5338A_INTR		10
JTAG_SAFE		7

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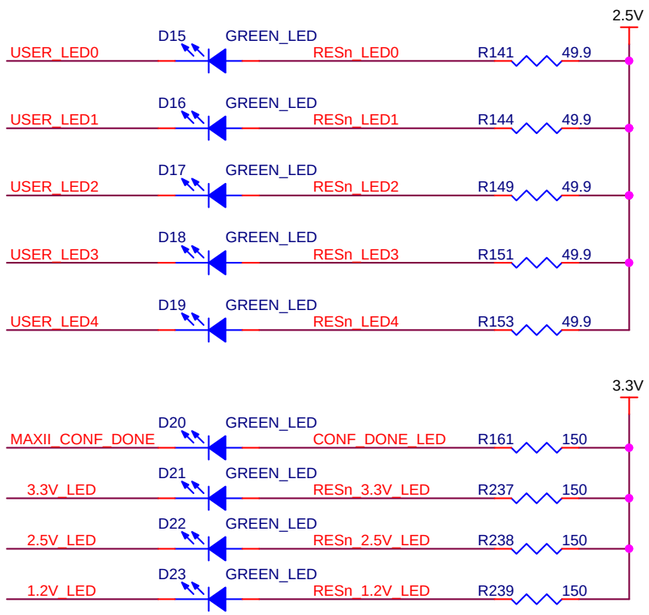
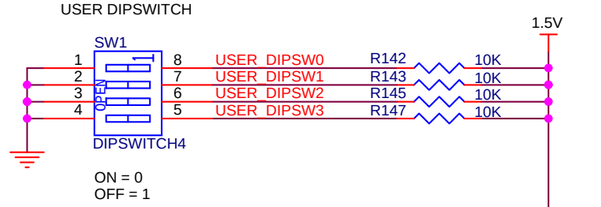
LED, User IO, Connector

LED

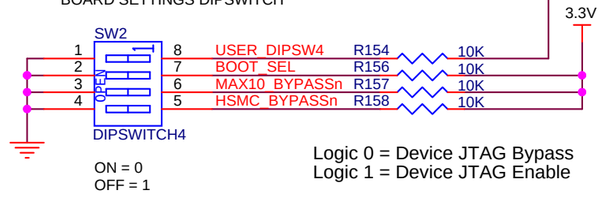


USER DIPSWITCH



ON = 0
OFF = 1

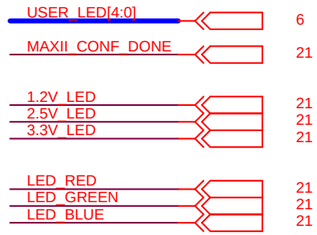
BOARD SETTINGS DIPSWITCH



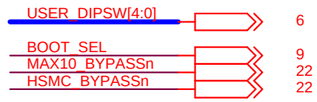
ON = 0
OFF = 1

Logic 0 = Device JTAG Bypass
Logic 1 = Device JTAG Enable

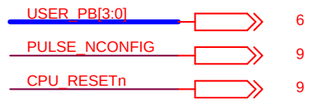
LED



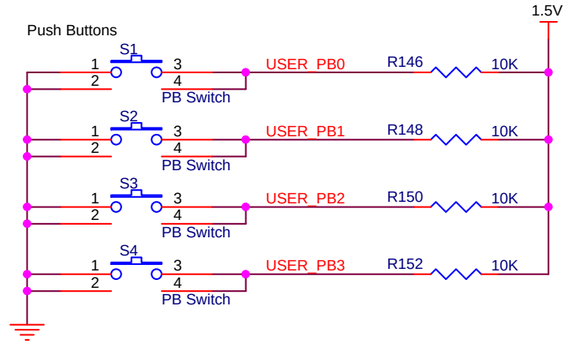
Swtiches

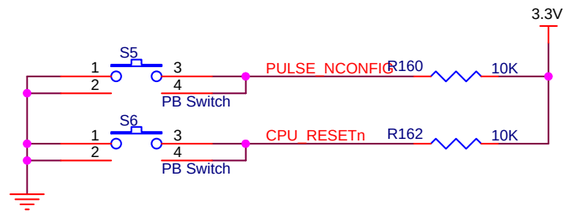


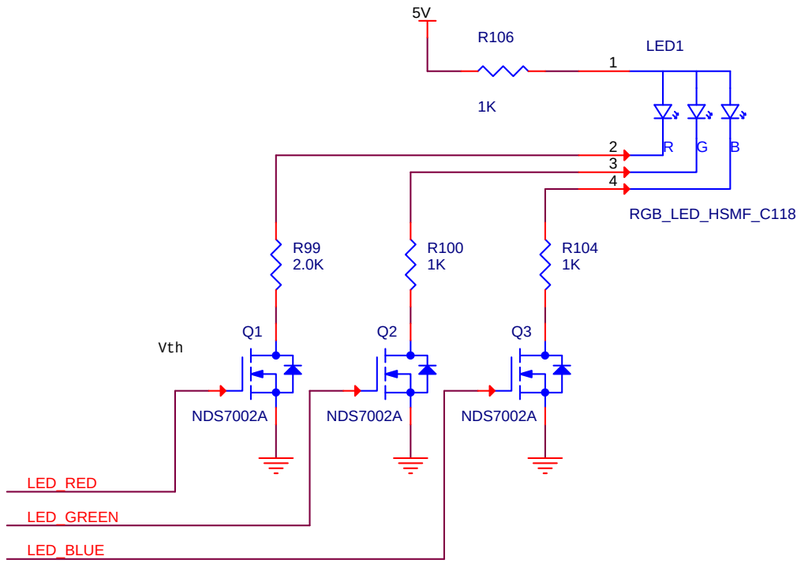
Buttons

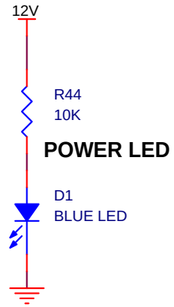


Push Buttons









Title: MAX10 FPGA Development Kit (6XX-44292R)		
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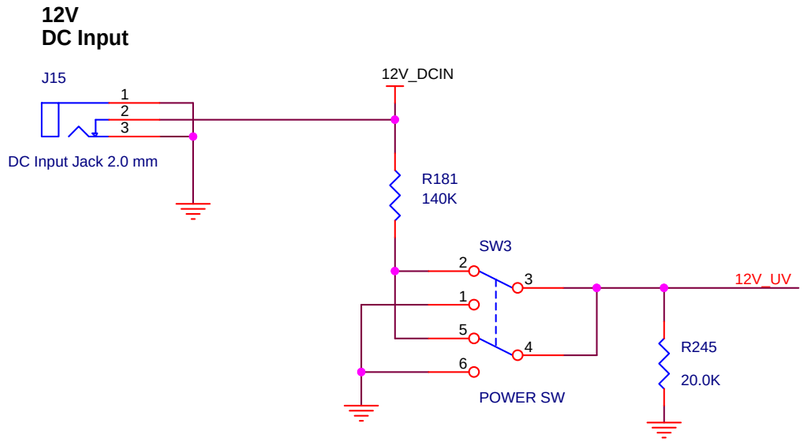
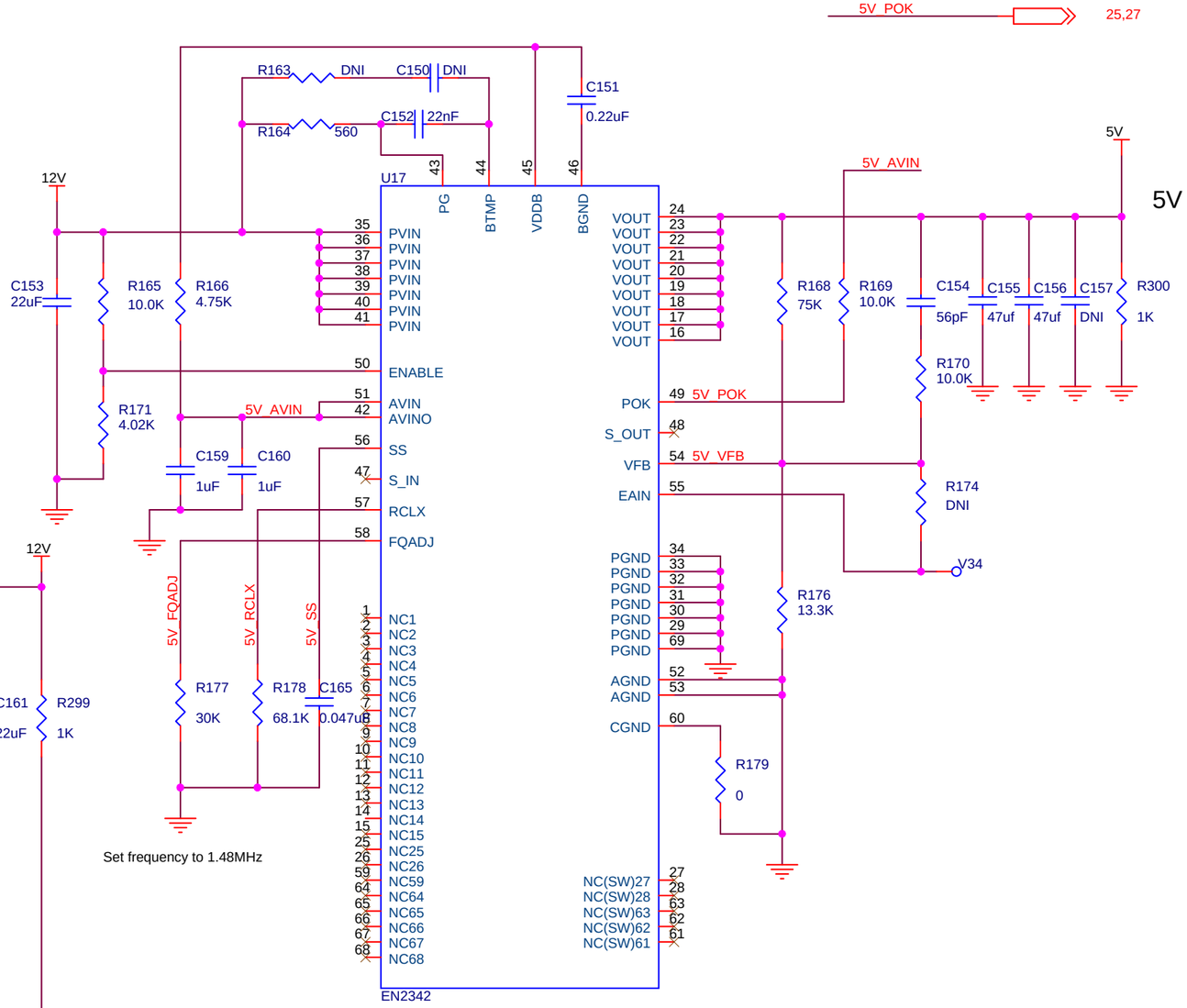
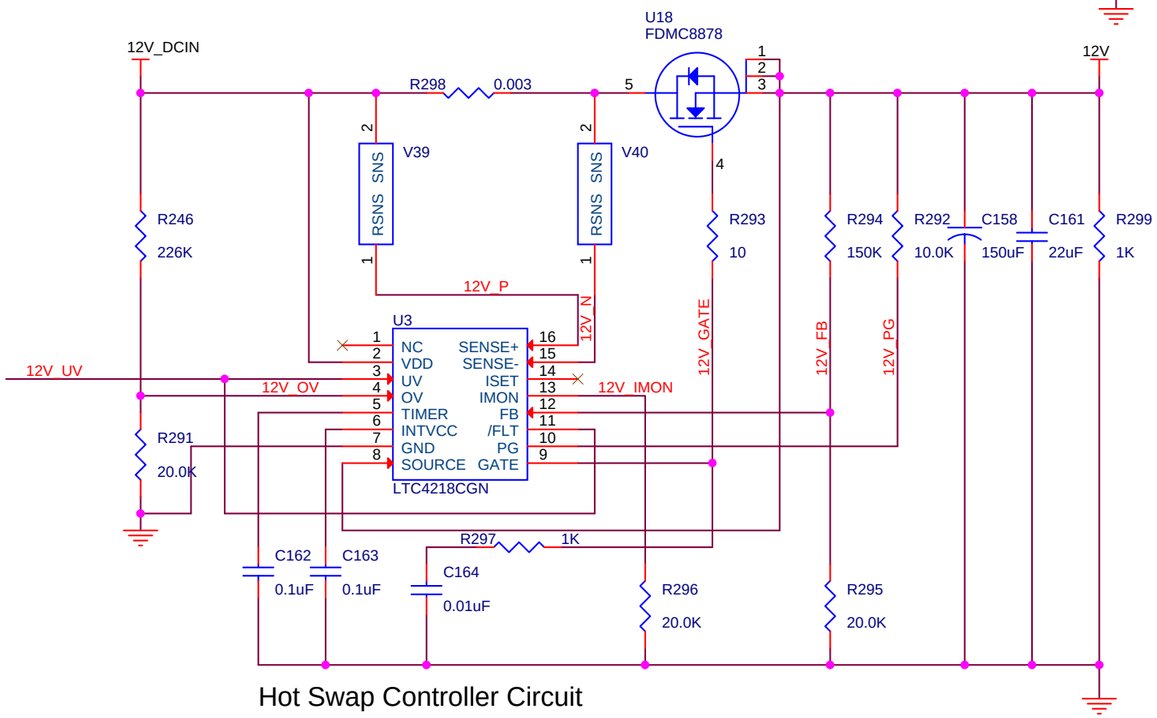
Power - 12V_DCIN / 5V







Hot Swap Controller Circuit

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Power - 3.3V / 2.5V

5V_POK 24,27
3.3V_POK 21
2.5V_POK 21

MAX10 3.3V (3.3V/2.698A)

U22

5V
C168 22uF
5V
R185 DNI
5V_POK R190 0 3.3V_EN 27 ENA
5V
33 AVIN
SS -> 22nF * 80kOhm = 1.76msec +/-25%
C176 22nF 1.8V_SS 30 SS
R194 0 1.8V_LLM 26 SYNC/LLM
R198 DNI 1.8V_RLLM 29 RLLM
Resistor for LLM mode only.
Open (DNI) for PWM mode.

Default to internal pull-up on LLM
to allow automatic engagement of
Light Load Mode.
Min (VIN - VOUT) = 315mV for PWM
Min (VIN - VOUT) = 800mV for LLM

19 PVIN
20 PVIN
21 PVIN

3.3V
POK 28 3.3V_POK R184 10.0K 3.3V
VOUT 5 6 7 8 9 10 11
C169 47UF C171 47UF
R192 200k C174 15pF
VFB 31 3.3V_VFB
VFB=0.75V
IFB=5nA
R195 59.0K
PGND 13 14 15 16 17 18 39
AGND 32

EN6337
NC(SW)1 NC(SW)2 NC3 NC4 NC(SW)12 NC22 NC23 NC24 NC25 NC(SW)34 NC(SW)35 NC(SW)36 NC(SW)37 NC(SW)38
1 2 3 4 12 22 23 24 25 34 35 36 37 38

5V
R200 560

MAX10 2.5V (2.5V/1.132A)

U23

5V
C170 22uF
5V
R189 DNI
5V_POK R191 0 2.5V_EN 27 ENA
5V
33 AVIN
SS -> 22nF * 80kOhm = 1.76msec +/-25%
C177 22nF 2.5V_SS 30 SS
R196 0 2.5V_LLM 26 SYNC/LLM
R199 DNI 2.5V_RLLM 29 RLLM
Resistor for LLM mode only.
Open (DNI) for PWM mode.

Default to internal pull-up on LLM
to allow automatic engagement of
Light Load Mode.
Min (VIN - VOUT) = 315mV for PWM
Min (VIN - VOUT) = 800mV for LLM

19 PVIN
20 PVIN
21 PVIN

3.3V
POK 28 2.5V_POK R186 10.0K 2.5V 2.5V_VCCIO
VOUT 5 6 7 8 9 10 11
C172 47UF C173 47UF
R281 0.1
R193 200k C175 15pF
VFB 31 2.5V_FB
VFB=0.75V
IFB=5nA
R197 84.5K
PGND 13 14 15 16 17 18 39
AGND 32

EN6337
NC(SW)1 NC(SW)2 NC3 NC4 NC(SW)12 NC22 NC23 NC24 NC25 NC(SW)34 NC(SW)35 NC(SW)36 NC(SW)37 NC(SW)38
1 2 3 4 12 22 23 24 25 34 35 36 37 38

5V
R201 560

2.5V_VCCIO
V35
2 SNS RSNS 1 2.5V_VCCIO_SENSE_P 28
2.5V
V36
2 SNS RSNS 1 2.5V_VCCIO_SENSE_N 28

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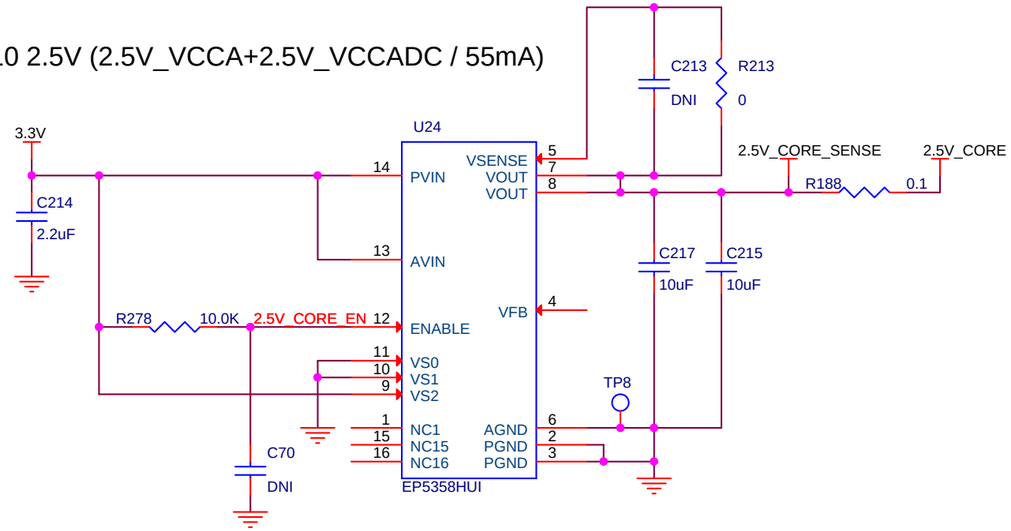
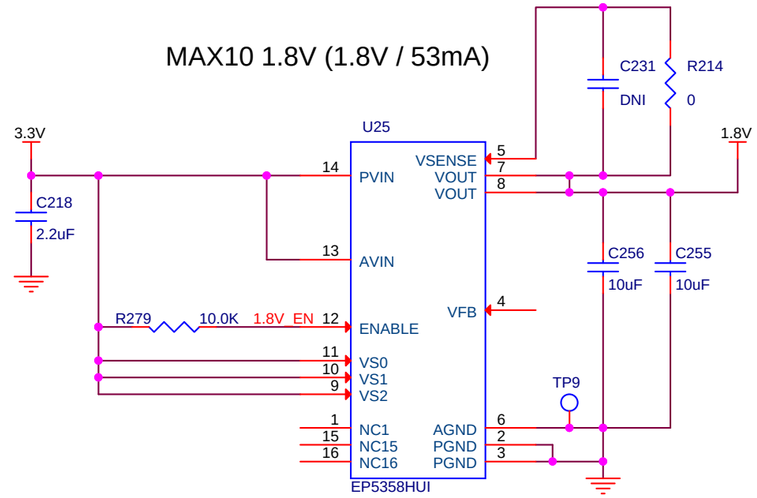
Power - 2.5V_VCC / 1.2V

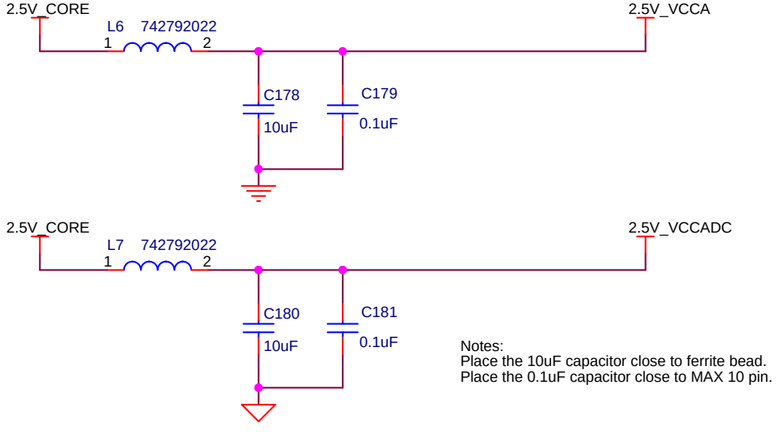
1.2V_POK → 21,27

MAX10 2.5V (2.5V_VCCA+2.5V_VCCADC / 55mA)

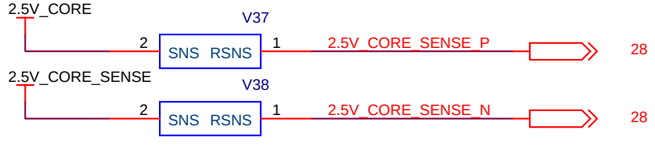


MAX10 1.8V (1.8V / 53mA)





Notes:
Place the 10uF capacitor close to ferrite bead.
Place the 0.1uF capacitor close to MAX 10 pin.



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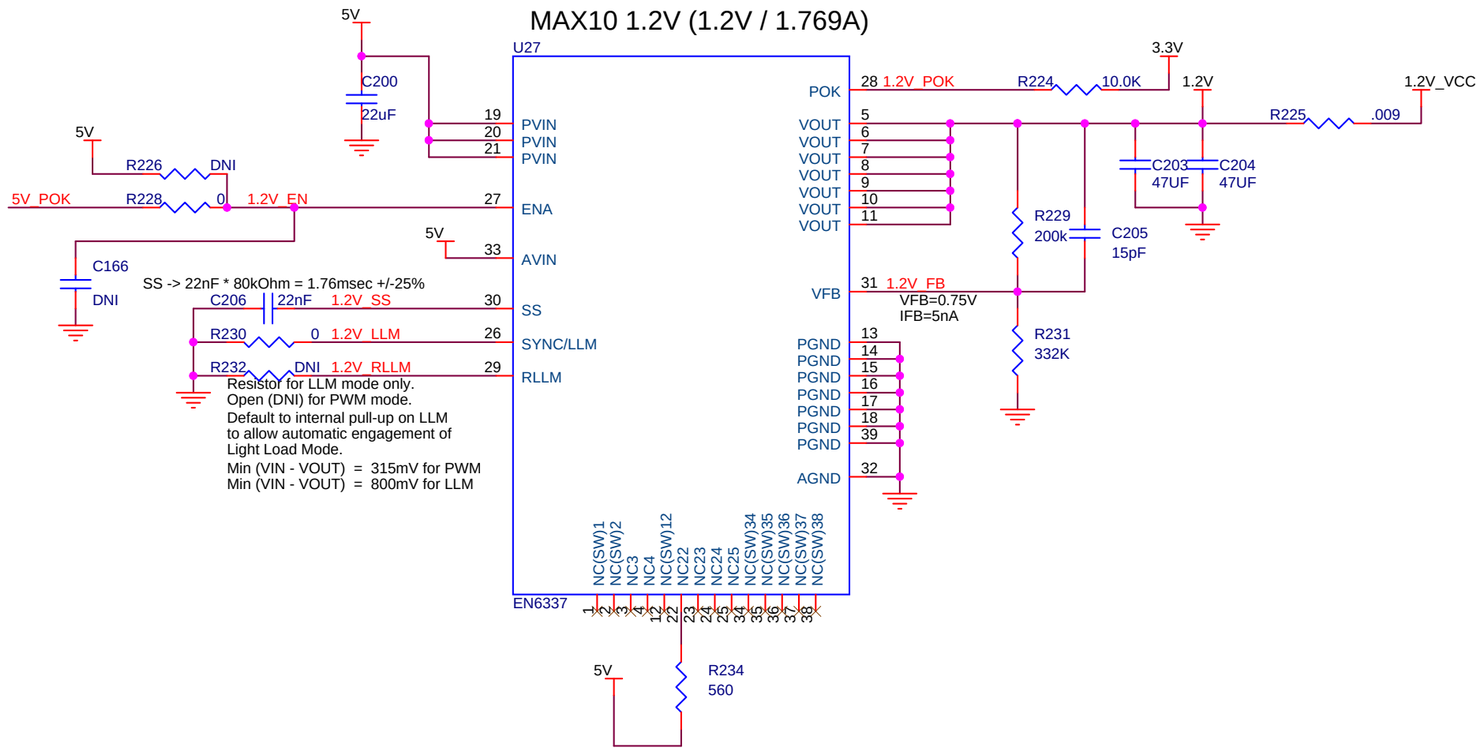
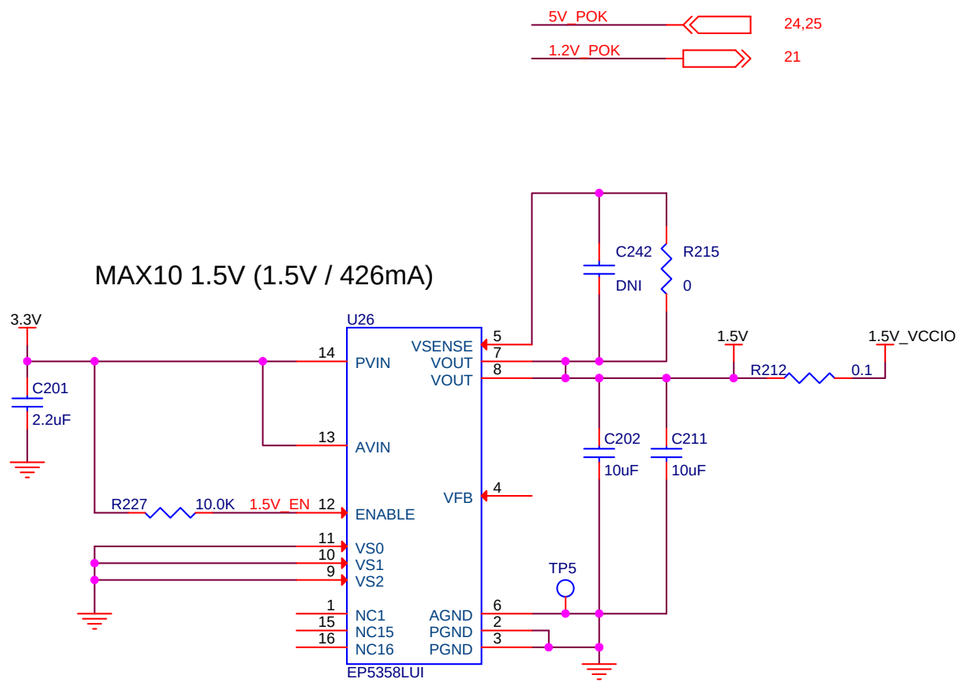
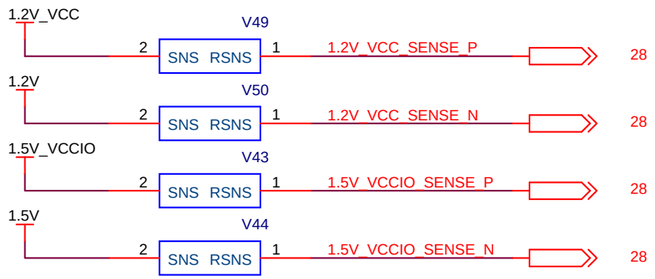
Power - 1.5V / 1.2V

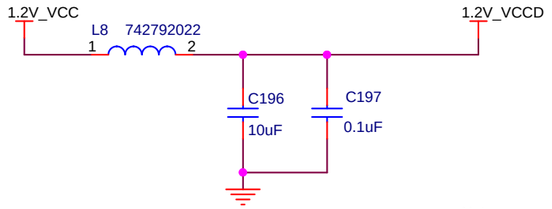
MAX10 1.2V (1.2V / 1.769A)

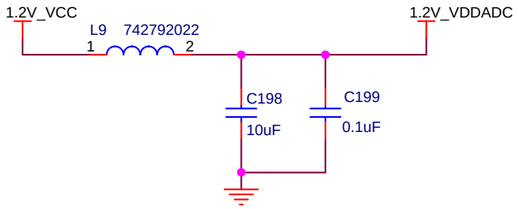


MAX10 1.5V (1.5V / 426mA)









Notes:
Place the 10uF capacitor close to ferrite bead.
Place the 0.1uF capacitor close to MAX 10 pin.

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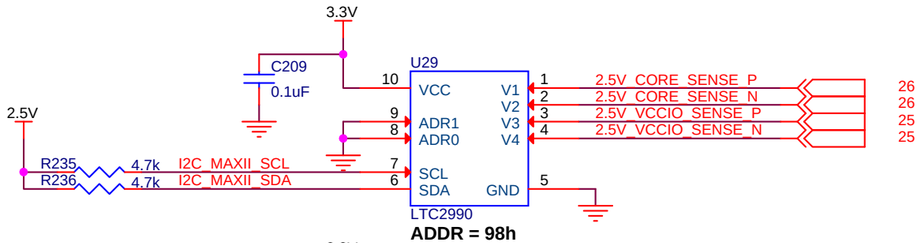
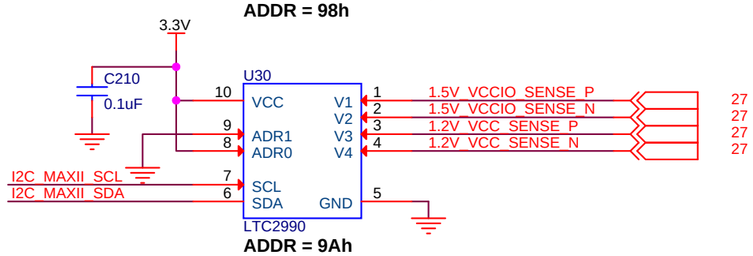
Power - Power Monitor





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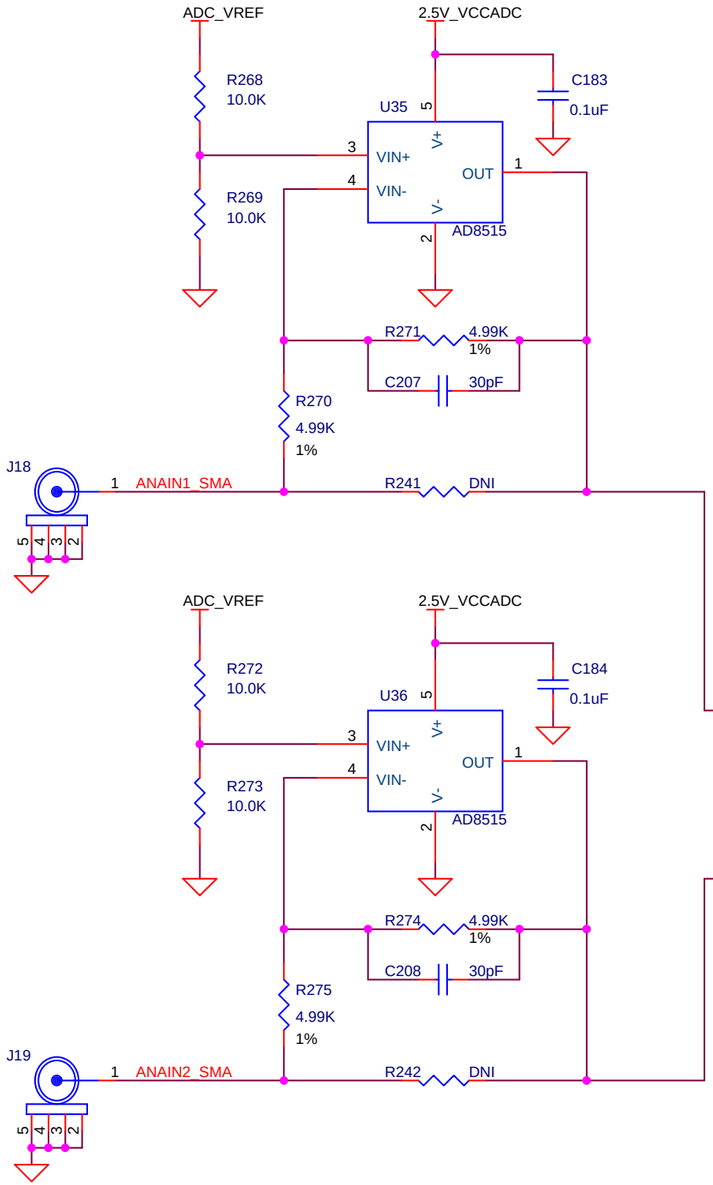
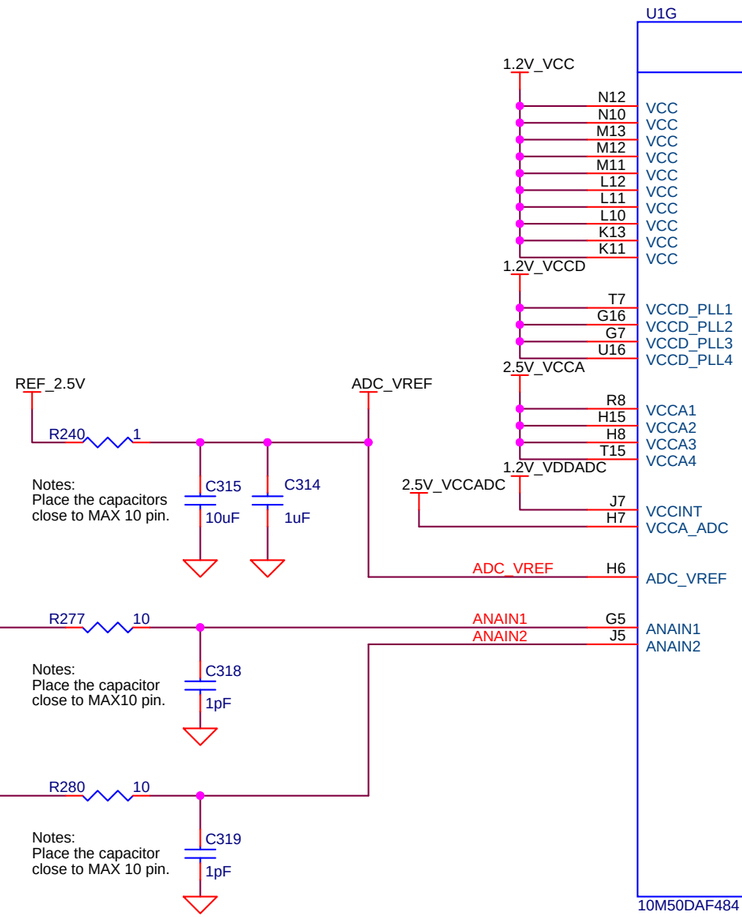
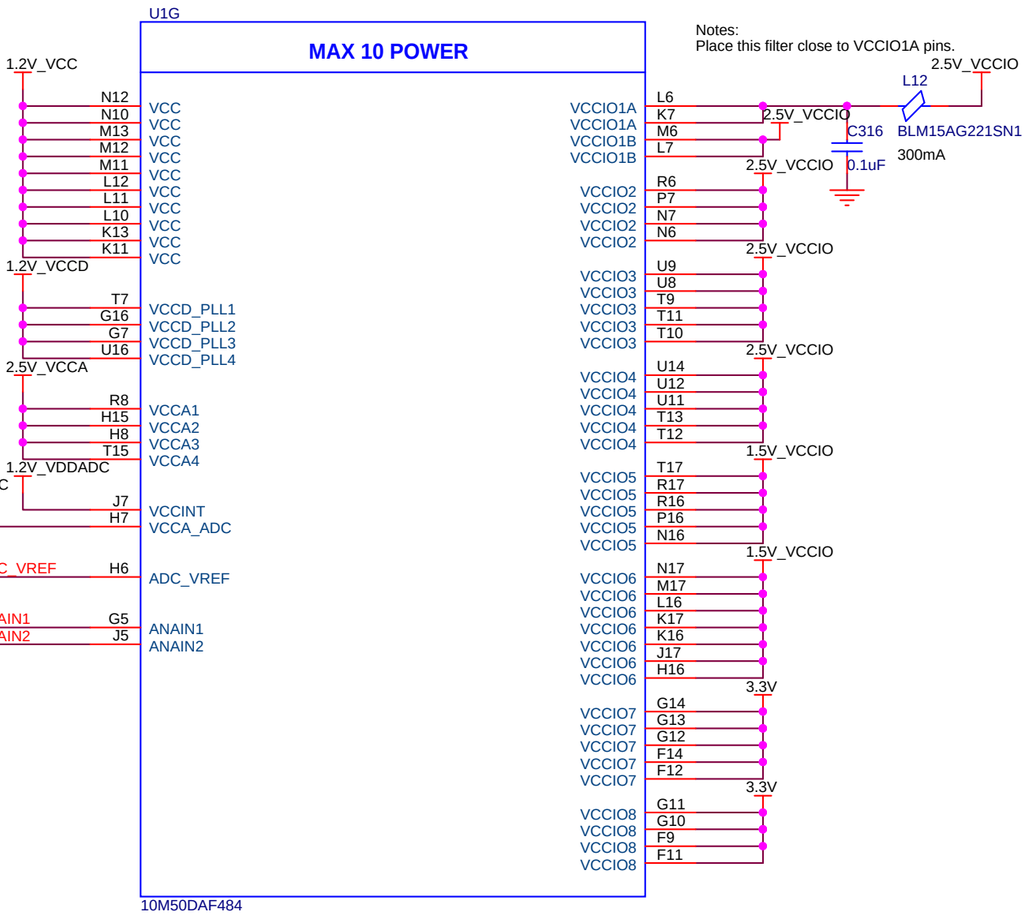
MAX10 Power







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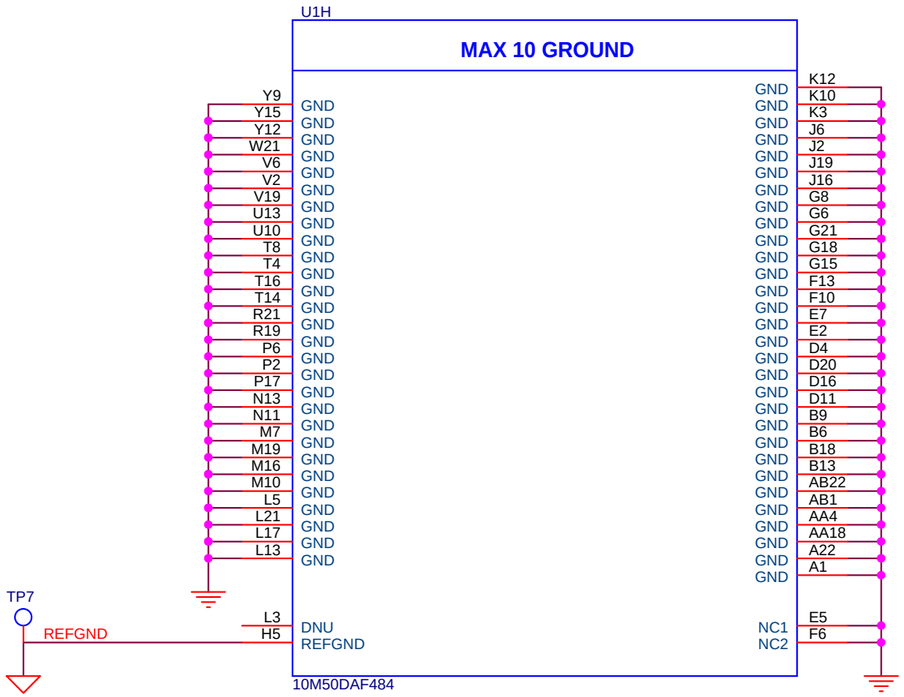
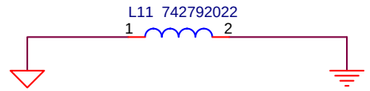
MAX10 Ground



Notes:
1. Use REFGND as ground reference.
2. Route analog input signal adjacent to AVSSREF as possible.

Notes:
Place this FB close to MAX 10 ADC_VREF.



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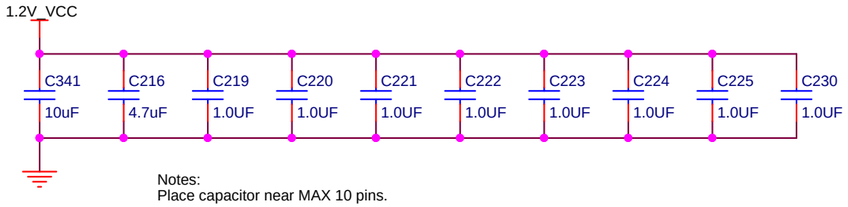
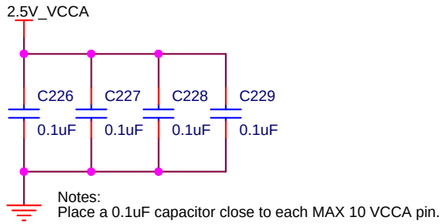
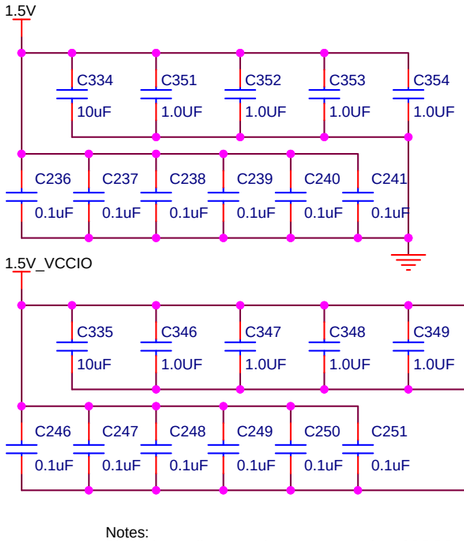
MAX10 Decoupling



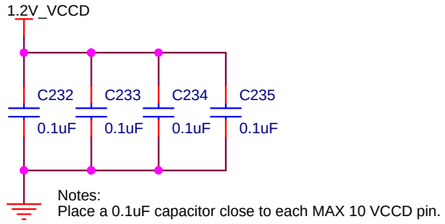
Notes:
Place capacitor near MAX 10 pins.



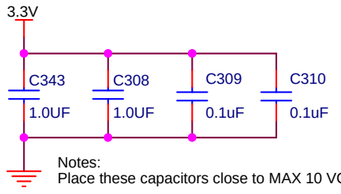
Notes:
Place a 0.1uF capacitor close to each MAX 10 VCCA pin.



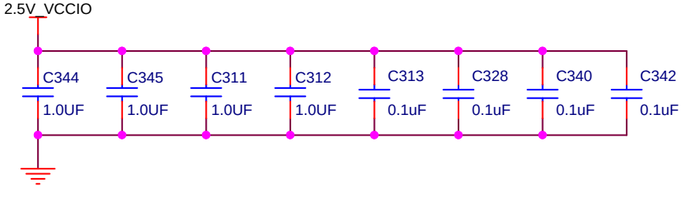
Notes:
Place decoupling capacitors on power pins of DDR3 and MAX 10.
Place 100UF capacitors on center of the power rail between DDR3 and MAX 10.



Notes:
Place a 0.1uF capacitor close to each MAX 10 VCCD pin.



Notes:
Place these capacitors close to MAX 10 VCCIO7 and VCCIO8 pins.



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