



## A Complete Development Environment

### Introduction

The Altera® MAX® 10 FPGA Development Kit, supported by the license-free Quartus® II Web Edition development software, provides a full-featured design platform built around a 50 K logic elements (LEs) MAX 10 FPGA, optimized for system level integration with on-die analog-to-digital converter (ADC), dual-configuration flash, and DDR3 memory interface support.

### What's in the Box

#### • Hardware

The development kit includes the following hardware:

- MAX 10 FPGA development board running on MAX 10 10M50DAF484C6GES FPGA
- DDR3 memory
- Quad serial peripheral interface (SPI) flash
- Two Gigabit Ethernet (GbE) RJ-45 ports
- One mini-USB2.0 UART
- One HSMC connector supporting LVDS and single-ended I/Os
- High-definition multimedia interface (HDMI) video output
- Two Digilent Pmod™ Compatible connectors
- Analog channels input with two dedicated SMA connectors and one 2 x 10 header, and output with one external digital-to-analog converter (DAC) device
- AC adapter power cables
- Mini-USB cable

#### • Software

Download and install MAX 10 FPGA Development Kit installer to obtain the following items:

- Design examples
  - Board Update Portal design
  - Board Test System (BTS) design
- Documentation
  - MAX 10 FPGA Development Kit User Guide
  - Board design files
- Design software\*
  - Quartus II software (required)
  - Nios® II processor (optional)
  - MegaCore® intellectual property (IP) library (optional)
  - Mentor Graphics® ModelSim®-Altera software (optional)

\* The kit installer can be downloaded directly from [www.altera.com/products/devkits/altera/kit-max-10-development.html](http://www.altera.com/products/devkits/altera/kit-max-10-development.html).  
The free Quartus® II Web Edition development software can be downloaded directly from <http://dl.altera.com/?edition=web>.

You can use this development kit to:

- Develop designs for the 10M50D, F484 package FPGA
- Measure the performance of the MAX 10 FPGA analog-to-digital block conversion
- Interface MAX 10 FPGAs to DDR3 memory at 300 MHz performance
- Run embedded operating system using the Nios II processor
- Take advantage of the modular and scalable design by using high-speed mezzanine card (HSMC) connectors to interface to one of over 40 different HSMCs provided by Altera® partners. For a complete list of HSMC connectors available for this development kit, refer to [https://www.altera.com/products/boards\\_and\\_kits/daughter-cards.html](https://www.altera.com/products/boards_and_kits/daughter-cards.html)
- Interface to daughtercards and peripherals using Digilent Pmod Compatible connectors. For a complete list of Pmod Compatible cards, refer to [www.digilentinc.com/Products/Catalog.cfm?NavPath=2,401&Cat=9](http://www.digilentinc.com/Products/Catalog.cfm?NavPath=2,401&Cat=9)
- Measure FPGA power ( $V_{CC\_CORE}$  and  $V_{CC\_IO}$ ) using the power monitor graphical user interface (GUI)
- Reuse the kit's PCB board and schematic as a model for your design

## Keep Your Board Current with the Board Update Portal

The Board Update Portal design example included in this development kit facilitates easy development of software and board flash memory updates, allowing you to:

- Access useful information on [www.altera.com](http://www.altera.com), including the page that contains updated software and design examples.
- Load software files into the Quad SPI flash memory on your board.

The following steps ensure that you have the latest software available on both your computer and your board. The Board Update Portal design example, which includes a Nios II embedded processor, an Ethernet media access control (MAC), and a web page, is stored in the “factory” portion of your board's flash memory. The source for this design is installed with the development kit software. When your board is connected to a DHCP-enabled network, the Nios II processor obtains an Internet protocol address and allows you to interface with your board over the network through a web page.

Before you proceed, ensure that you have the following:

- A computer with a connection to a working Ethernet port on a DHCP-enabled network.
- A separate working Ethernet port connected to the same network for your board.
- The Ethernet, power cables, and development board included in your kit.

### Step 1. Connect to the Board Update Portal

1. Install the latest Altera software tools, including Quartus II software, Nios II processor, and IP functions. If necessary, download the Quartus II Web Edition software from <http://dl.altera.com/?edition=web>
2. With the board powered down, set DIP SW2 switch 2 to the ON position (factory default), which loads the factory default design from MAX 10 FPGA internal flash image 0 on power-up.
3. Attach the Ethernet cable from RJ-45 port A (the bottom one) to your network hub.
4. Power up the board. The board connects to your network server and obtains an Internet protocol address.
5. On the Windows Start menu, click **All Programs > Altera > Nios II EDS > Nios II Command Shell**.

- In the Nios II command shell, type the following command:

```
nios2-terminal ↵
```

When the IP address has been assigned, it will be displayed as follows:

- Launch a web browser on a computer that is connected to the same network, and type the

```
Created "Inet main" task (Prio: 2)
Created "clock tick" task (Prio: 3)
Acquired IP address via DHCP client for interface: et1
IP address: 137.57.125.34
Subnet Mask: 255.255.255.0
Gateway : 137.57.125.200
```

Internet protocol address displayed on the Nios II command shell. The Board Update Portal web page appears on your PC.

- Click on the "**MAX 10 FPGA Development Kit**" link and download the latest version of the development kit software. The version number noted in the "**Downloads**" section of the website corresponds to the version of Quartus II software used to create the design examples.
- Browse through the additional designs that are available. Check this website often for new designs and for updates to existing designs and documentation. Note that some designs may require specific versions of the Altera Complete Design Suite to function properly.
- This development kit is supported by the license-free Quartus II Web Edition software. No license is required in the Web Edition software to compile and generate programming files for the MAX 10 FPGA family.
- Proceed to Step 3.

If you cannot connect to the Board Update Portal, go to [www.altera.com/products/boards\\_and\\_kits/dev-kits/altera/max-10-fpga-development-kit.html](http://www.altera.com/products/boards_and_kits/dev-kits/altera/max-10-fpga-development-kit.html) to ensure that you have the latest development kit software, and proceed with Step 2.

### Step 2. Install the development kit software

Install the latest development kit software and follow the instructions from `*\factory_recovery\build_factory_source\readme.txt` to recover the factory build.

### Step 3. Update the user software portion

To update the user software portion of flash memory on your board, follow these steps:

- Prepare your software image and change it to **user\_flash.flash** file with elf2flash utility, make sure the "--reset" option is set to Flash memory base address + Reset Vector Offset (0x0083\_0000).
- Perform the steps in Step 1 to display the Board Update Portal web page.
- In the Software File Name field, specify your **user\_flash.flash** file.
- Click **Upload**.
- Reprogram the user's dual configuration image into Configuration Flash Memory (CFM)
  - Image 0: BUP A build
  - Image 1: User's Nios II processor-based build
  - Make sure the user's Nios II processor-based build boots up from reset vector offset "0x0083\_0000".
- Power off the board.
- Change the SW2 switch 2 to the OFF position (1) to make sure that it boots up from image 1.
- Power on the board.

The new user software image and user hardware build now run in the FPGA.

