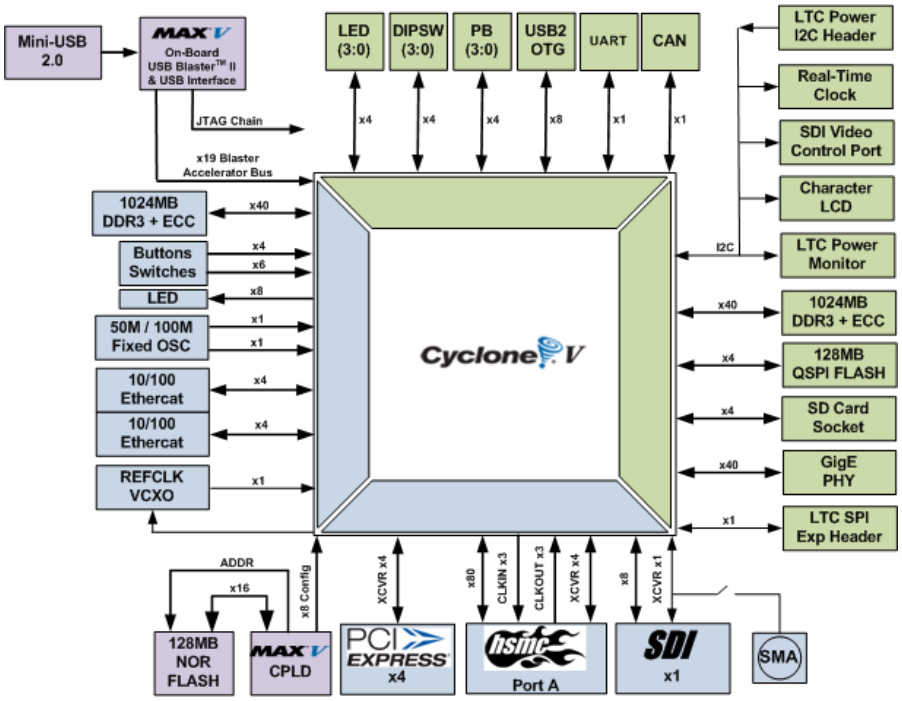
NOTES:

1. Project Drawing Numbers:

Raw PCB	100-0321003-E1
Gerber Files	110-0321003-E1
PCB Design Files	120-0321003-E1
Assembly Drawing	130-0321003-E1
Fab Drawing	140-0321003-E1
Schematic Drawing	150-0321003-E1
PCB Film	160-0321003-E1
Bill of Materials	170-0321003-E1
Schematic Design Files	180-0321003-E1
Functional Specification	210-0321003-E1
PCB Layout Guidelines	220-0321003-E1
Assembly Rework	320-0321003-E1

Cyclone V SoC FPGA Development Kit Board

REV	DATE	PAGES	DESCRIPTION
E1	07/11/2014	All	INITIAL REVISION RELEASE



PAGE	DESCRIPTION	PAGE	DESCRIPTION
1	Title, Notes, Block Diag, Rev. History	30	Power 3 - 1.5V FPGA
2	FPGA Package Top	31	Power 3 - 2.5V FPGA
3	PCI Express Edge Connector	32	Power 3 - 2.5V HPS
4	Cyclone V GX SoC Bank 3,4	33	Power 3 - 1.5V & 1.5V HPS
5	Cyclone V GX SoC Bank 5,6	34	Power 3 - 3.3V HPS
6	Cyclone V GX SoC Bank 7	35	Power 1.1V_HPS , 5.0V , 1.8V
7	Cyclone V GX SoC Bank 8	36	Power 4 - Linear Regulators
8	Cyclone V GX SoC Transceiver Banks	37	Power 6 - Power & Temp Monitor
9	Cyclone V GX SoC Clocks	38	CycloneV GX SOC Power
10	PLL	39	CycloneV GX SOC Ground
11	Cyclone V GX SoC Configuration	40	Decoupling
12	JTAG	41	Changes History
13	1024MB DDR3 (x32) - FPGA		
14	1024MB DDR3 (x32 + ECC) - HPS		
15	FLASH , EPCQ		
16	5M2210 System Controller		
17	HSMC PORT A		
18	10/100/1000 Ethernet - HPS		
19	10/100M Ethernet - FPGA		
20	SDI Cable Driver , SMA & SMB		
21	QSPI FLASH & RESET Circuit		
22	USB2.0 & Micro SD Card		
23	User I/O , RTC		
24	UART , CAN		
25	On - Board USB Blaster II		
26	FPGA Power Monitor		
27	HPS Power Monitor		
28	Power 1 - DC I/P & 12V , 3.3V O/P		
29	Power 2		

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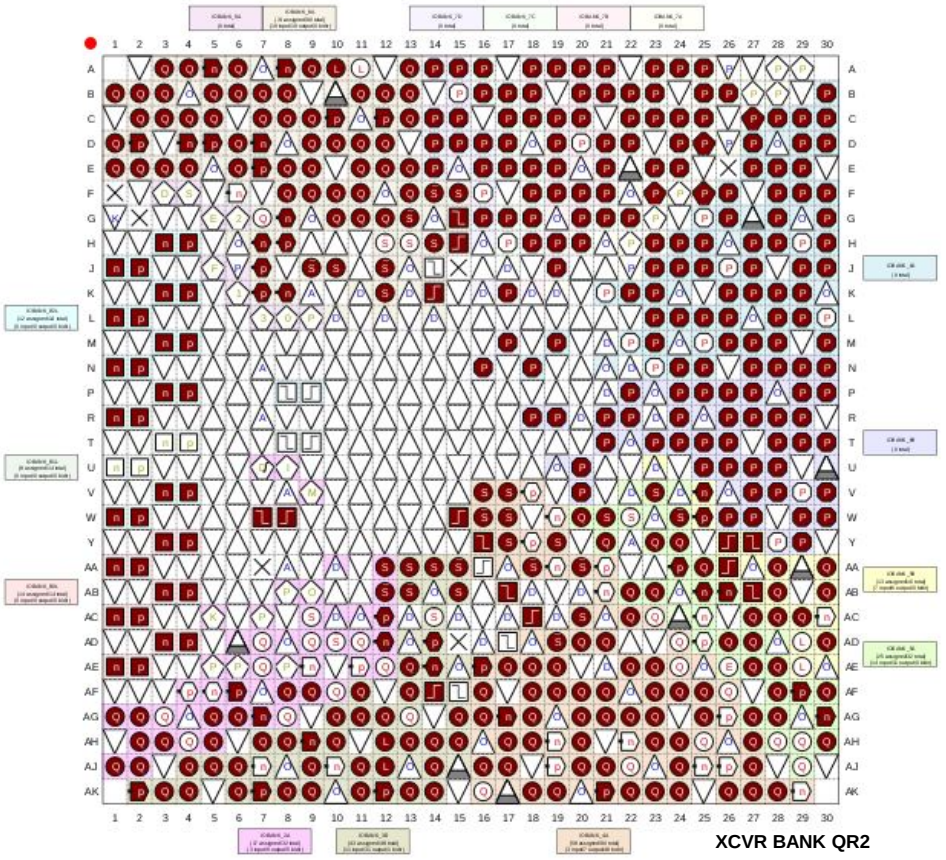
FPGA Package Top View

I/O Bank Usage

	I/O Bank	Usage	VCCIO Voltage	VREF Voltage	VCCPD Voltage
1	B2L	0 / 14 (0 %)	--	--	--
2	B1L	0 / 14 (0 %)	--	--	--
3	B0L	0 / 14 (0 %)	--	--	--
4	3A	28 / 32 (88 %)	2.5V	--	2.5V
5	3B	43 / 48 (90 %)	1.5V	0.75V	2.5V
6	4A	58 / 80 (73 %)	1.5V	0.75V	2.5V
7	5A	25 / 32 (78 %)	2.5V	--	2.5V
8	5B	13 / 16 (81 %)	2.5V	--	2.5V
9	6B	34 / 45 (76 %)	1.5V	0.75V	2.5V
10	6A	48 / 57 (84 %)	1.5V	0.75V	2.5V
11	7A	19 / 19 (100 %)	3.3V	--	3.3V
12	7B	20 / 22 (91 %)	3.3V	--	3.3V
13	7C	12 / 12 (100 %)	3.3V	--	3.3V
14	7D	12 / 14 (86 %)	3.3V	--	3.3V
15	8A	74 / 80 (93 %)	2.5V	--	2.5V

Top View - Wire Bond

Cyclone V - 5CSXFC6D6F31C7



XCVR BANK QR2

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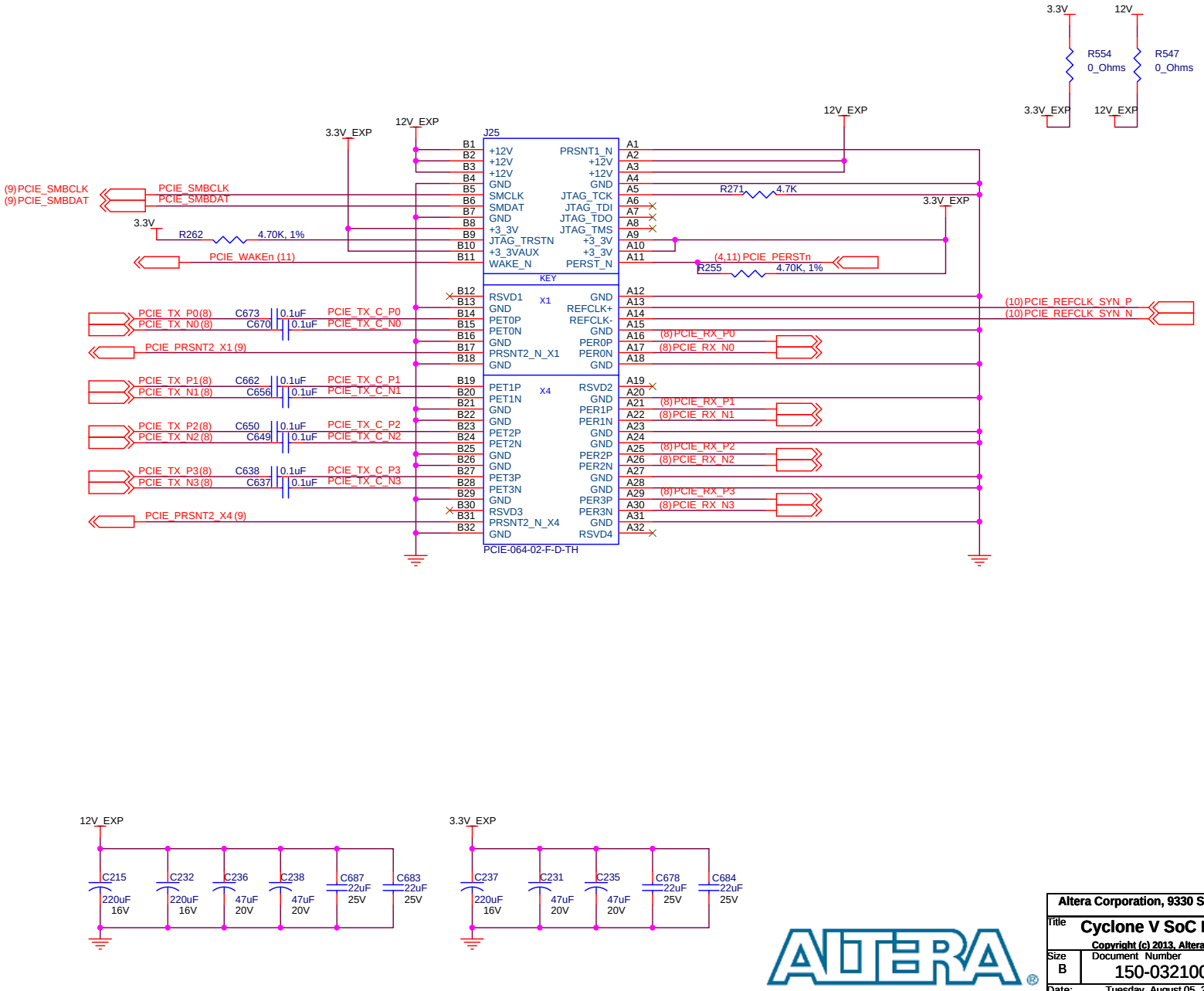
PCI Express Connector



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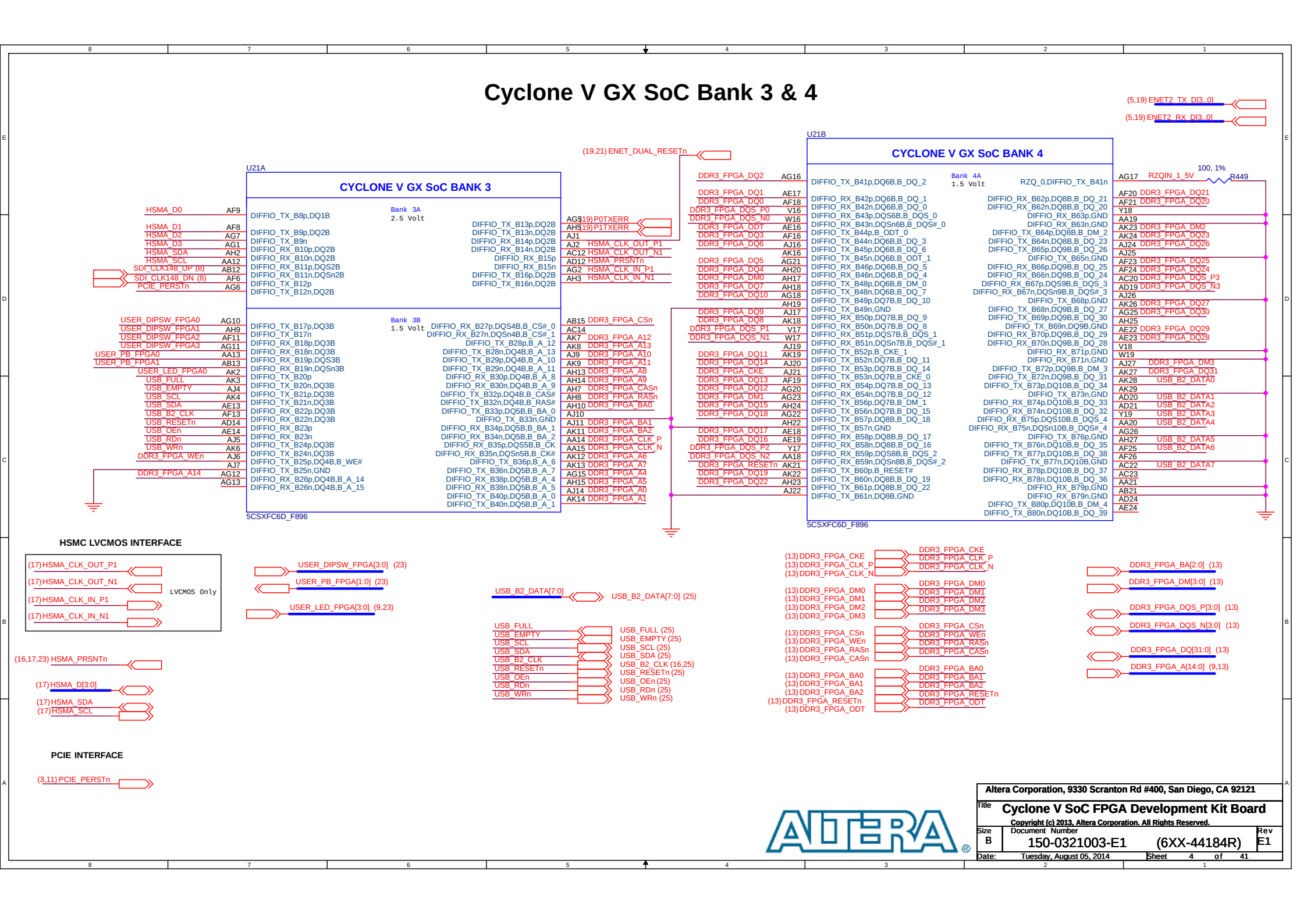
Cyclone V GX SoC Bank 3 & 4



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Size B	Document Number 150-0321003-E1 (6XX-44184R) Rev E1
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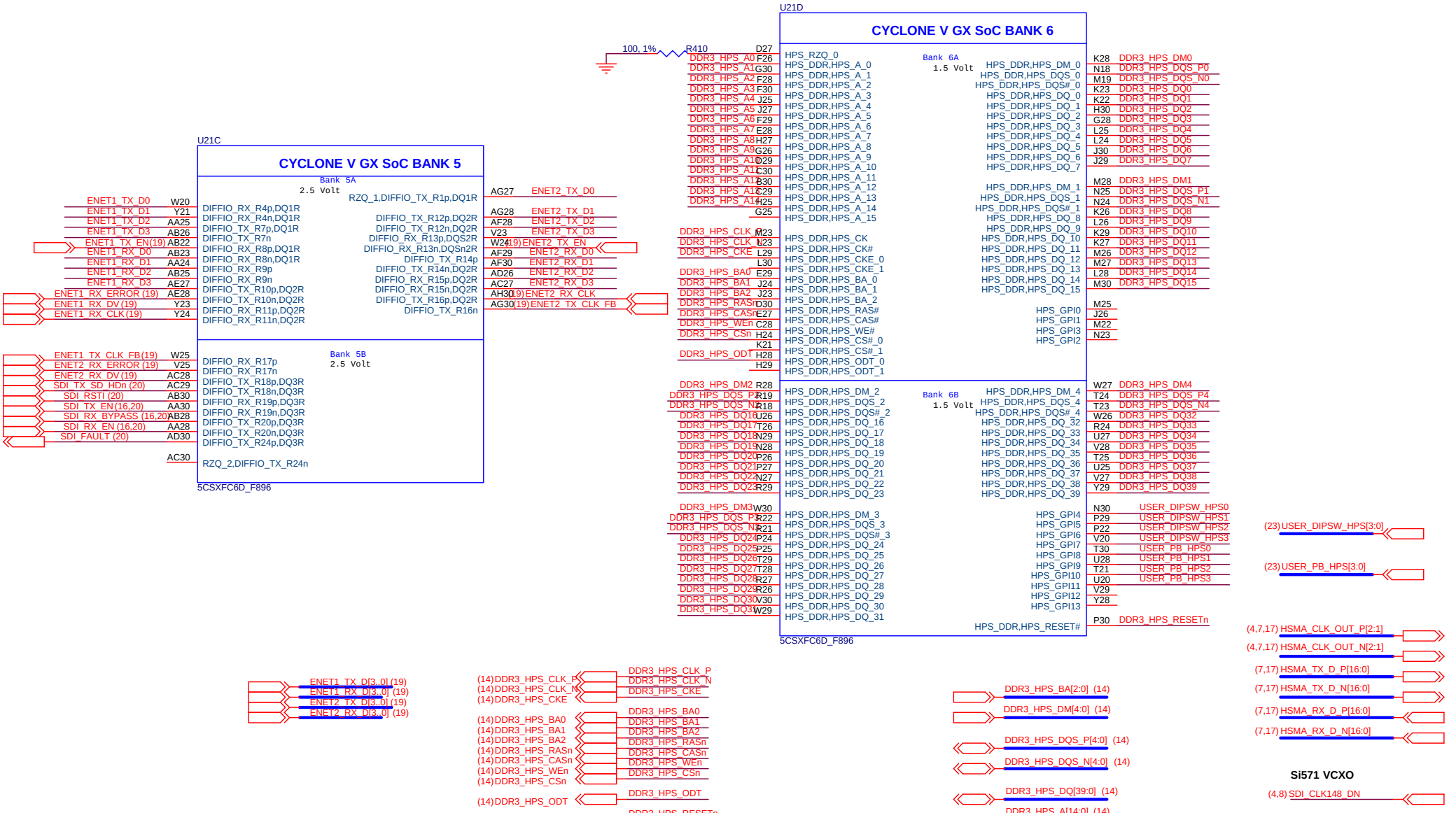
Cyclone V GX SoC Bank 5 & 6



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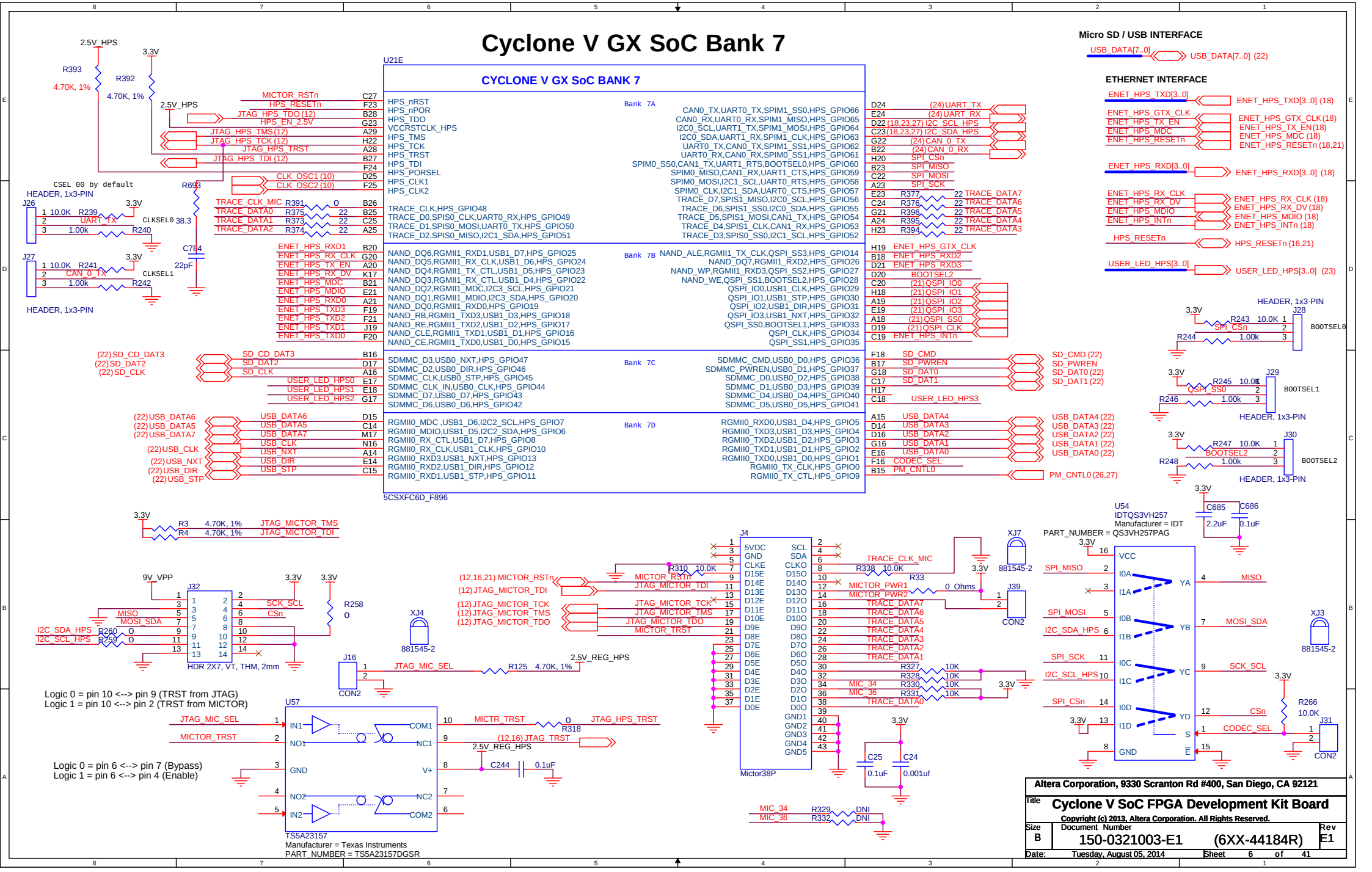
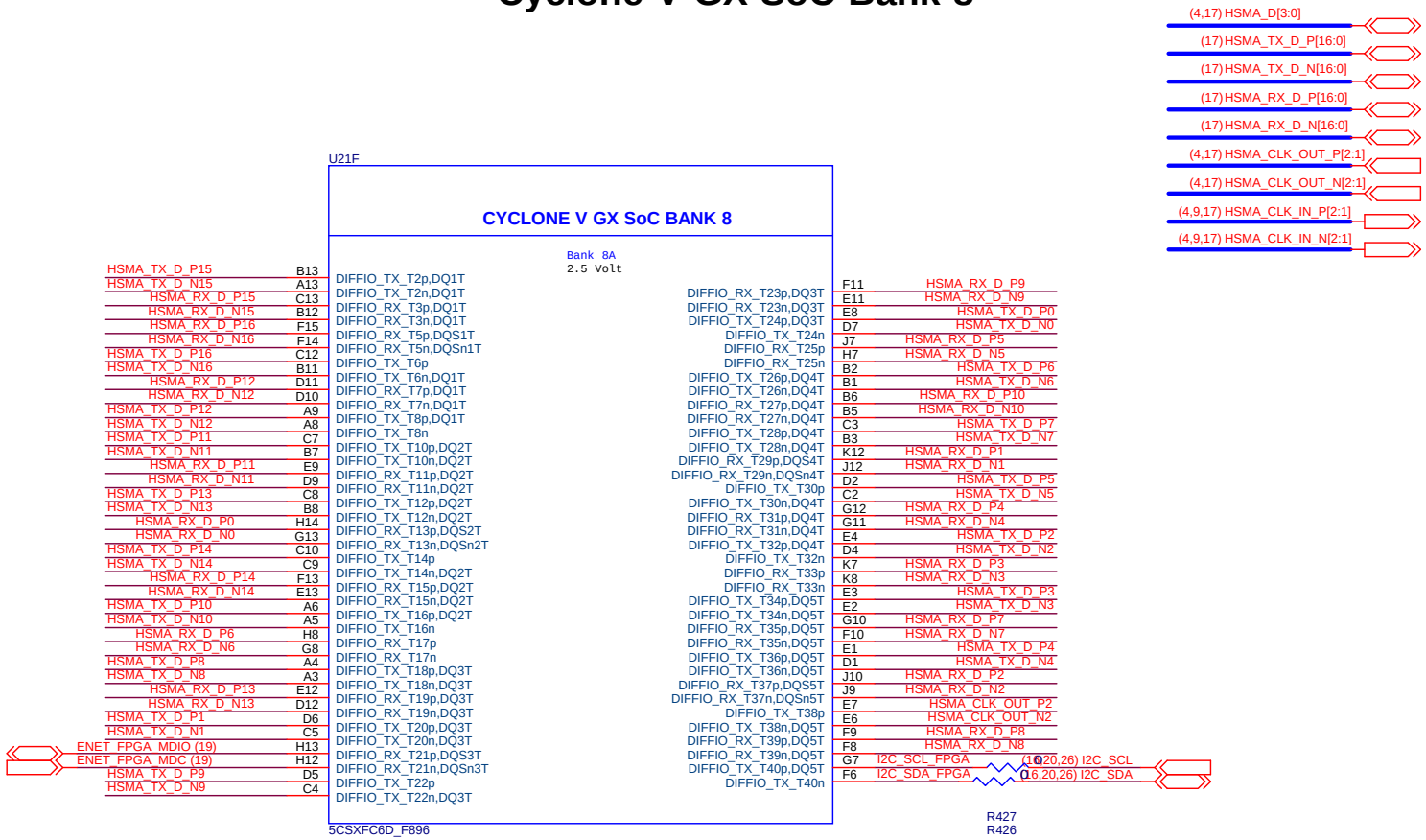
Cyclone V GX SoC Bank 7



Cyclone V GX SoC Bank 8



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Size	Document Number	Rev
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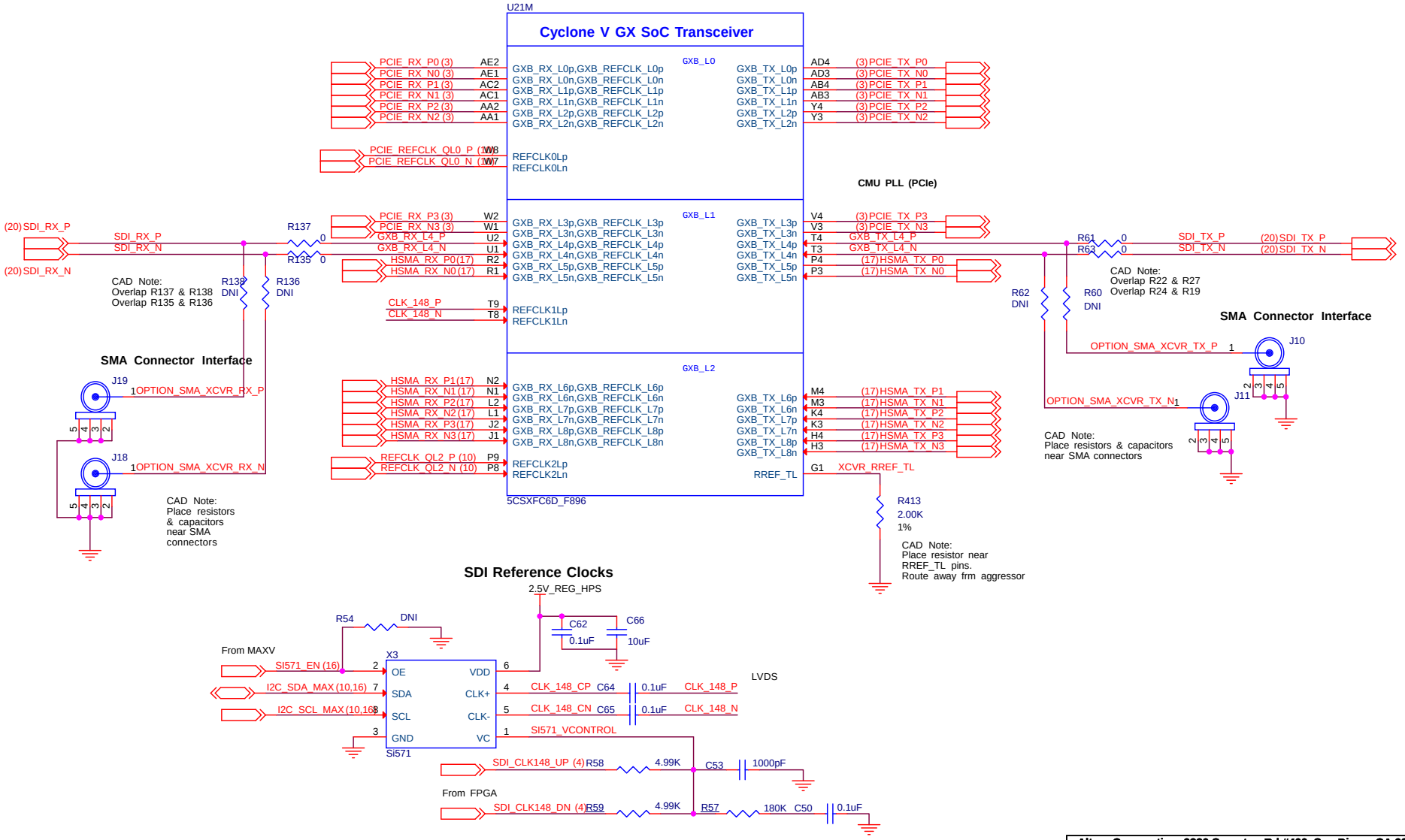
Cyclone V GX SoC Transceivers and Power



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Size: B	Document Number: 150-0321003-E1 (6XX-44184R)	Rev: E1
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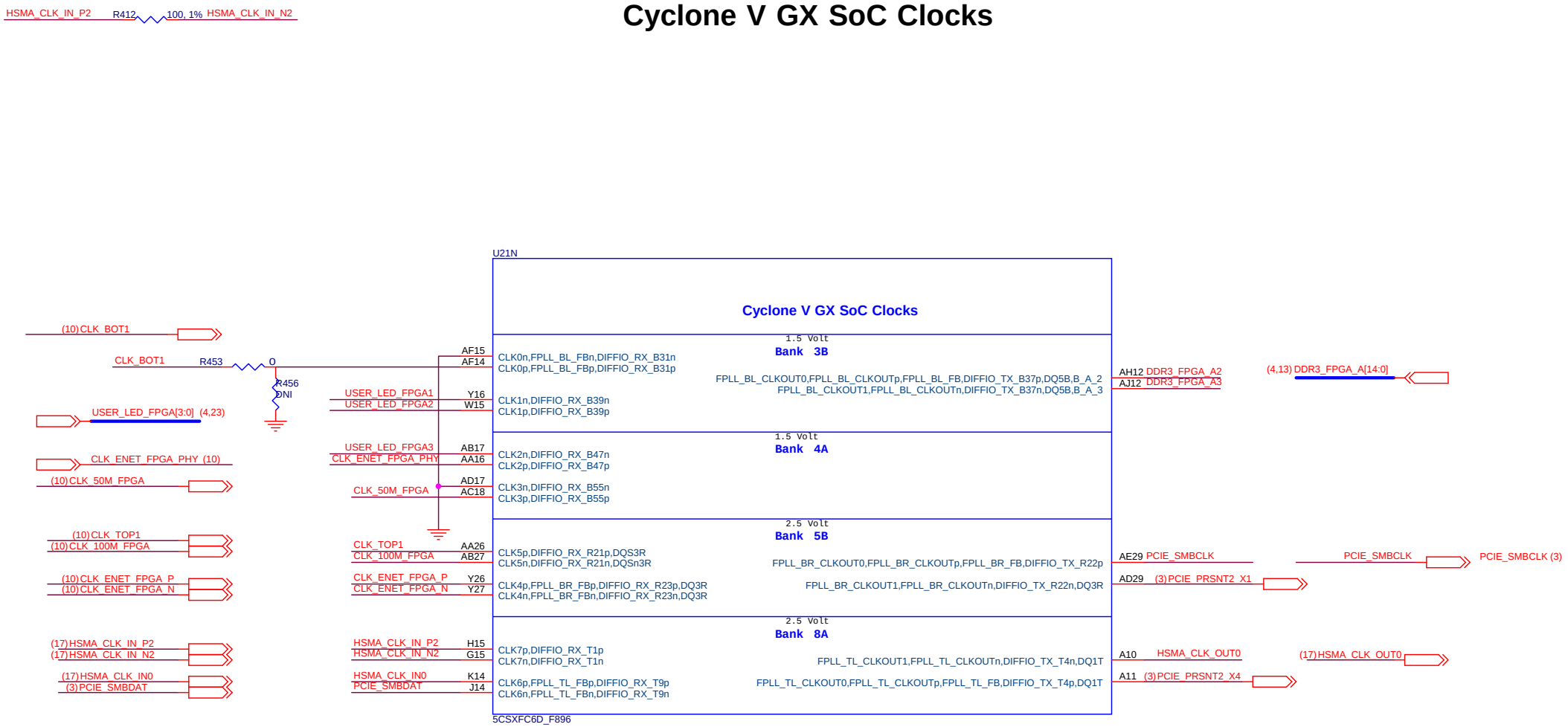
Cyclone V GX SoC Clocks



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Size	Document Number	Rev
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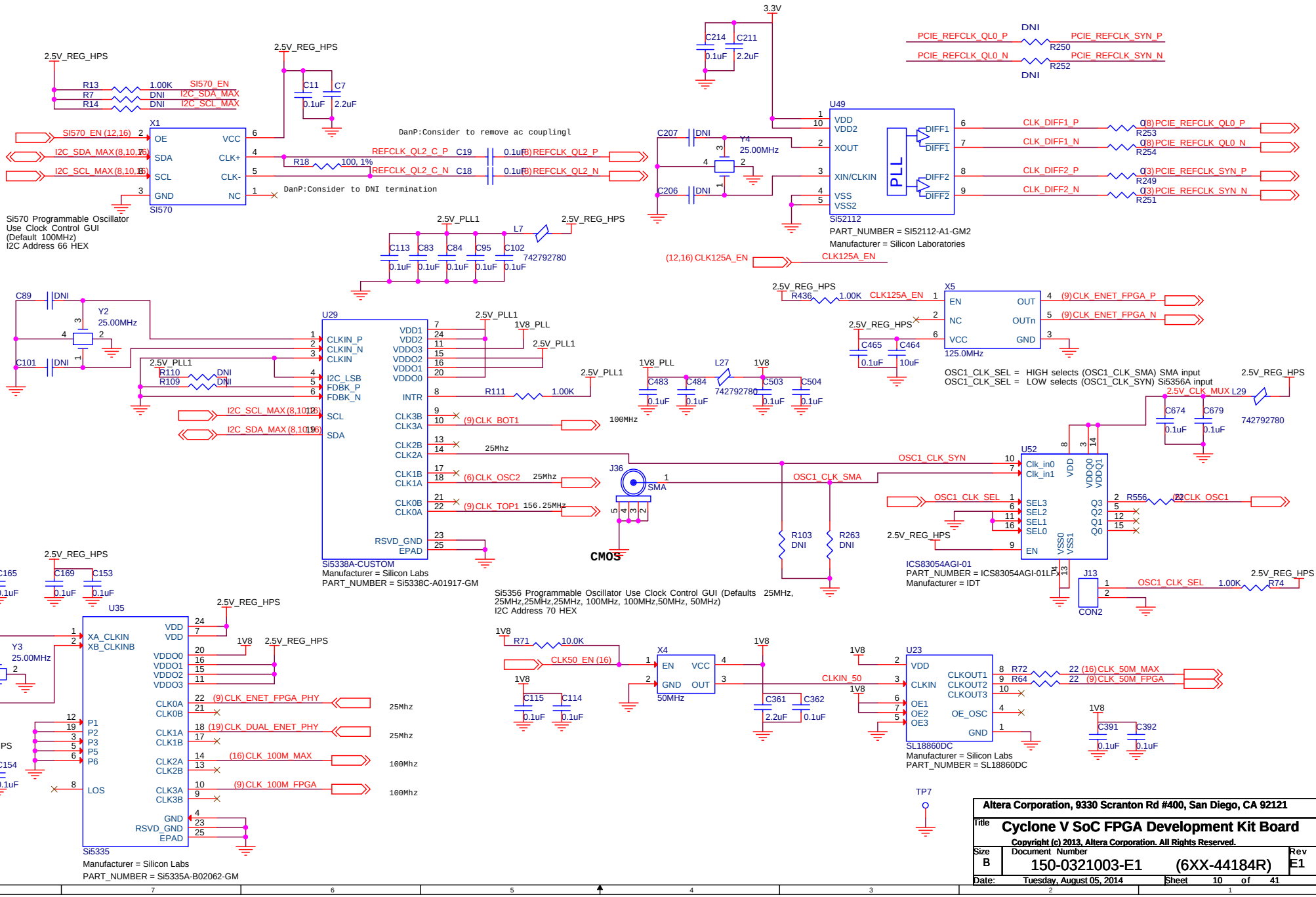
PLL



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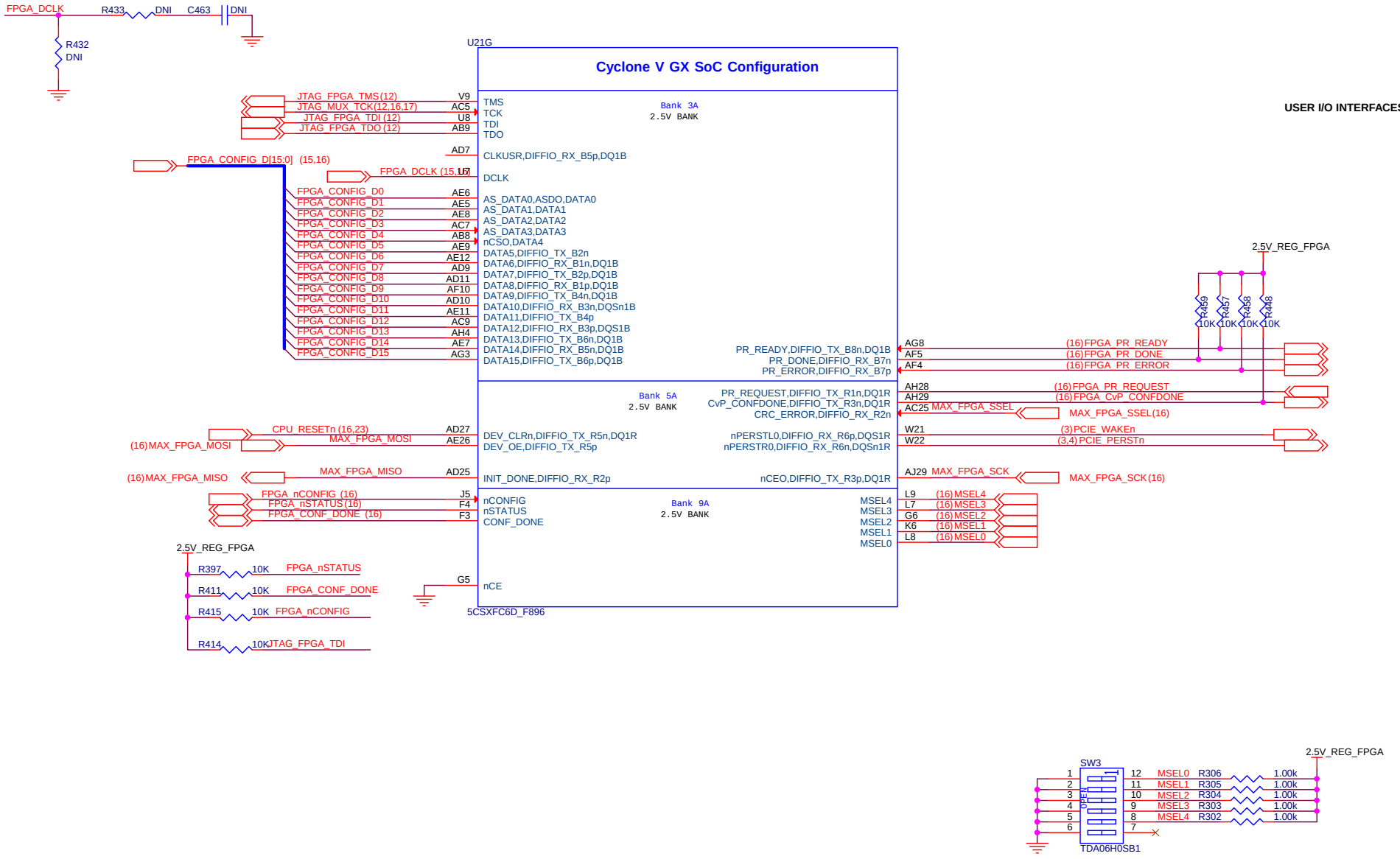
Cyclone V GX SoC Configuration



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JTAG

USB Blaster Programming Header
(uses JTAG mode only)

2.5V_REG_HPS
R212 1.00k
2.5V_REG_HPS
USB_DISABLEn (25)
J23
2 4 6 8 10
1 3 5 7 9
(12,25) JTAG_TCK
JTAG_BLASTER_TDI
(12,25) JTAG_TMS
(12,25) JTAG_BLASTER_TDO
70247-1051
R209 0
(6,16) JTAG_TRST
(6,16,21) MICTOR_RST#
2.5V_REG_HPS
R210 1.00k
R201 1.00k
JTAG_BLASTER_TDO
R202 DNI
JTAG_BLASTER_TDI

Populate R58 if you would like to Master the JTAG chain through HSMA

JTAG Chain Control

SW4
1 2 3 4
8 7 6 5
HPS_JTAG_EN R325 1.00k
FPGA_JTAG_EN R324 1.00k
HSMA_JTAG_EN R323 1.00k
MAX_JTAG_EN R322 1.00k
2.5V_REG_HPS
TDA04H0SB1
ON = not-in-chain
OFF = in-chain

SW2
8 7 6 5
1 2 3 4
CLK125A_EN R317 10.0K
SI570_EN R308 10.0K
FACTORY_LOAD R307 10.0K
SECURITY_MODE R287 10.0K
2.5V_REG_HPS
1V8
TDA04H0SB1

(10,16) CLK125A_EN
(10,16) SI570_EN
(16) FACTORY_LOAD
(16) SECURITY_MODE
CLK125A_EN
SI570_EN
FACTORY_LOAD
SECURITY_MODE

U16

3.3V
16 VCC
(11,12,16,17) JTAG_MUX_TCK
2 I0A
JTAG_MUX_TCK
4 YA
(6) JTAG_HPS_TCK
(6,12) JTAG_MICTOR_TCK
3 I1A
JTAG_MICTOR_TCK
(12) JTAG_MUX_TMS
5 I0B
JTAG_MUX_TMS
7 YB
(6,12) JTAG_HPS_TMS
(6,12) JTAG_MICTOR_TMS
6 I1B
JTAG_MICTOR_TMS
JTAG_MUX_HPS_TDI
11 I0C
JTAG_MUX_HPS_TDI
9 YC
(6) JTAG_HPS_TDI
(6,12) JTAG_MICTOR_TDO
10 I1C
JTAG_MICTOR_TDO
(11,12) JTAG_FPGA_TDI
14 I0D
JTAG_FPGA_TDI
12 YD
(6) JTAG_HPS_TDO
(6,12) JTAG_MICTOR_TDI
13 I1D
JTAG_MICTOR_TDI
1 S
JTAG_HPS_SEL
8 GND
15 E
IDTQS3VH257
Manufacturer = IDT
PART_NUMBER = QS3VH257PAG
3.3V
C40 2.2uF
C41 0.1uF
3.3V
R43 1.00k JTAG_HPS_SEL

JTAG_HPS_SEL
XJ5
881545-2
J6
1 2
CON2

U15

3.3V
16 VCC
(12,25) JTAG_TCK
2 I0A
JTAG_TCK
4 YA
JTAG_MUX_TCK
JTAG_MUX_TCK(11,12,16,17)
(6,12) JTAG_MICTOR_TCK
3 I1A
JTAG_MICTOR_TCK
(12,25) JTAG_TMS
5 I0B
JTAG_TMS
7 YB
JTAG_MUX_TMS
JTAG_MUX_TMS(12)
(6,12) JTAG_MICTOR_TMS
6 I1B
JTAG_MICTOR_TMS
(25) JTAG_BLASTER_TDI
11 I0C
JTAG_BLASTER_TDI
9 YC
JTAG_MUX_TDI
JTAG_MUX_TDI(12)
(6,12) JTAG_MICTOR_TDI
10 I1C
JTAG_MICTOR_TDI
(12,25) JTAG_BLASTER_TDO
14 I0D
JTAG_BLASTER_TDO
12 YD
JTAG_MUX_TDO
(6,12) JTAG_MICTOR_TDO
13 I1D
JTAG_MICTOR_TDO
1 S
JTAG_SEL
8 GND
15 E
IDTQS3VH257
Manufacturer = IDT
PART_NUMBER = QS3VH257PAG
3.3V
R44 1.00k JTAG_SEL
3.3V
C38 2.2uF
C39 0.1uF
JTAG_SEL
XJ6
881545-2
J7
1 2
CON2

TS5A23157 Switch Functions

When Pins 1 & 5 are:
LOW --> NC to/from COM = ON and NO to/from COM = OFF
HIGH --> NC to/from COM = OFF and NO to/from COM = ON

Logic 0 = pin 10 <--> pin 9 (HPS Bypass)
Logic 1 = pin 10 <--> pin 2 (HPS Enable)
Logic 0 = pin 6 <--> pin 7 (HPS Bypass)
Logic 1 = pin 6 <--> pin 4 (HPS Enable)

U7
HPS_JTAG_EN 1 IN1
JTAG_MUX_HPS_TDI 0 R40 HPS 2 NO1
3 GND
JTAG_MUX_TMS 4 NO2
HPS_JTAG_EN 5 IN2
COM1 10 JTAG_MUX_TDO
NC1 9 FPGA 0 R24 (11,12) JTAG_FPGA_TDI
2.5V_REG_HPS
V+ 8 C266 0.1uF
2.5V_REG_HPS
NC2 7 BP_HPS_TMS R25 1.00k
COM2 6 (6,12) JTAG_HPS_TMS
1 0
TS5A23157

Logic 0 = pin 10 <--> pin 9 (FPGA Bypass)
Logic 1 = pin 10 <--> pin 2 (FPGA Enable)
Logic 0 = pin 6 <--> pin 7 (FPGA Bypass)
Logic 1 = pin 6 <--> pin 4 (FPGA Enable)

U8
FPGA_JTAG_EN 1 IN1
JTAG_FPGA_TDO (11) 2 NO1
3 GND
JTAG_MUX_TMS 4 NO2
FPGA_JTAG_EN 5 IN2
COM1 10 HSMA 0 R26 (17) JTAG_HSMA_TDI
NC1 9 (11,12) JTAG_FPGA_TDI
2.5V_REG_HPS
V+ 8 C265 0.1uF
2.5V_REG_HPS
NC2 7 BP_FPGA_TMS R27 1.00k
COM2 6 (11) JTAG_FPGA_TMS
1 0
TS5A23157

Logic 0 = pin 10 <--> pin 9 (HSMA Bypass)
Logic 1 = pin 10 <--> pin 2 (HSMA Enable)
Logic 0 = pin 6 <--> pin 7 (HSMA Bypass)
Logic 1 = pin 6 <--> pin 4 (HSMA Enable)

U9
HSMA_JTAG_EN 1 IN1
JTAG_HSMA_TDO (17) 2 NO1
3 GND
JTAG_MUX_TMS 4 NO2
HSMA_JTAG_EN 5 IN2
COM1 10 MAX 0 R28 (16) JTAG_MAX_TDI
NC1 9 JTAG_HSMA_TDI
2.5V_REG_HPS
V+ 8 C264 0.1uF
2.5V_REG_HPS
NC2 7 BP_HSMA_TMS R29 1.00k
COM2 6 (17) JTAG_HSMA_TMS
1 0
TS5A23157

Logic 0 = pin 10 <--> pin 9 (MAX II Bypass)
Logic 1 = pin 10 <--> pin 2 (MAX II Enable)
Logic 0 = pin 6 <--> pin 7 (HSMBBypass)
Logic 1 = pin 6 <--> pin 4 (HSMB Enable)

U10
MAX_JTAG_EN 1 IN1
JTAG_MAX_TDO (16) 2 NO1
3 GND
JTAG_MUX_TMS 4 NO2
MAX_JTAG_EN 5 IN2
COM1 10 MUX 0 R30 (12) JTAG_MUX_TDI
NC1 9 JTAG_MAX_TDI
2.5V_REG_HPS
V+ 8 C263 0.1uF
2.5V_REG_HPS
NC2 7 BP_MAX_TMS R31 1.00k
COM2 6 (16) JTAG_MAX_TMS
1 0
TS5A23157
Manufacturer = Texas Instruments
PART_NUMBER = TS5A23157DGSR

ALTERA®

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Size B	Document Number 150-0321003-E1 (6XX-44184R) Rev E1
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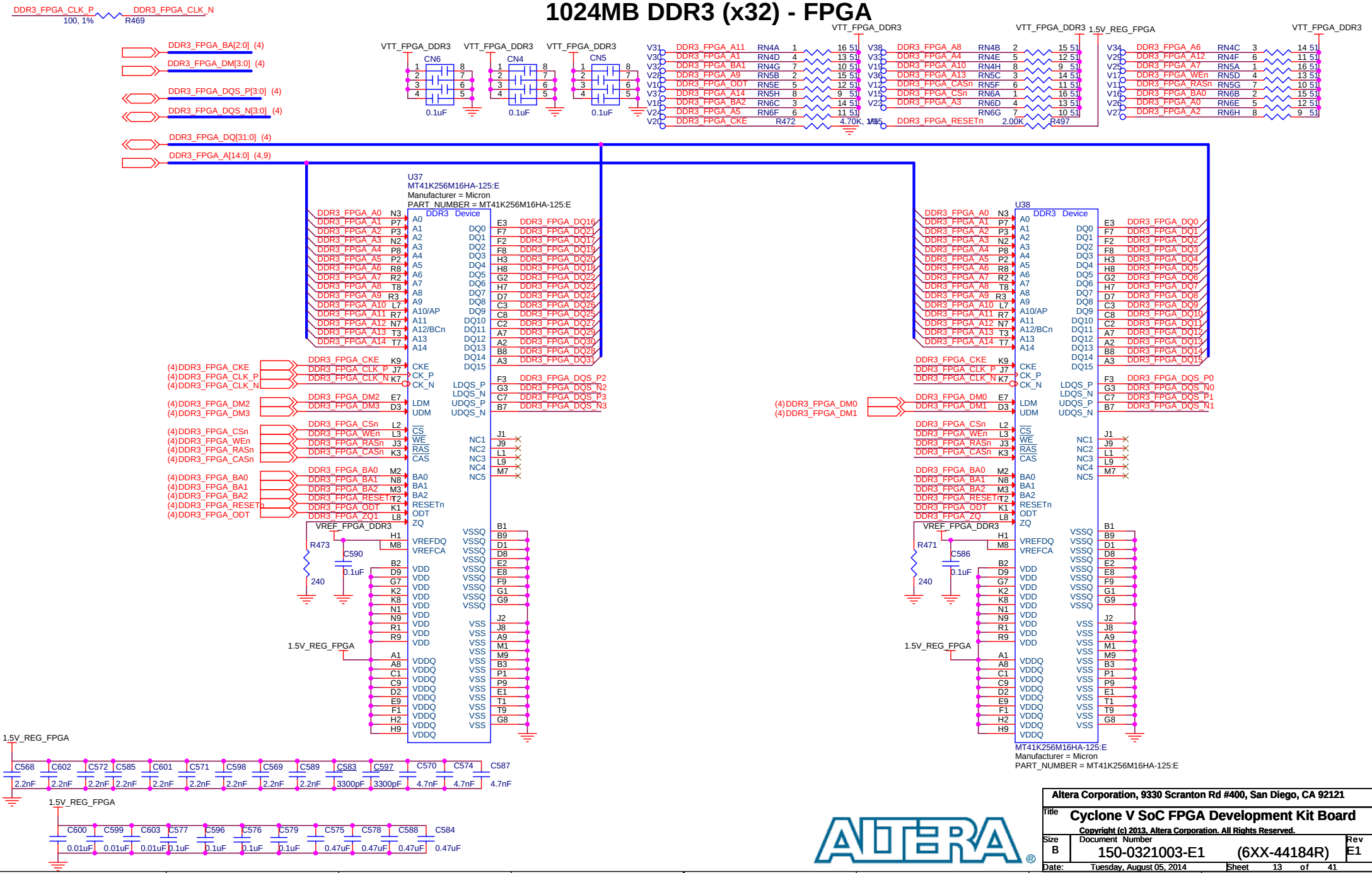
1024MB DDR3 (x32) - FPGA



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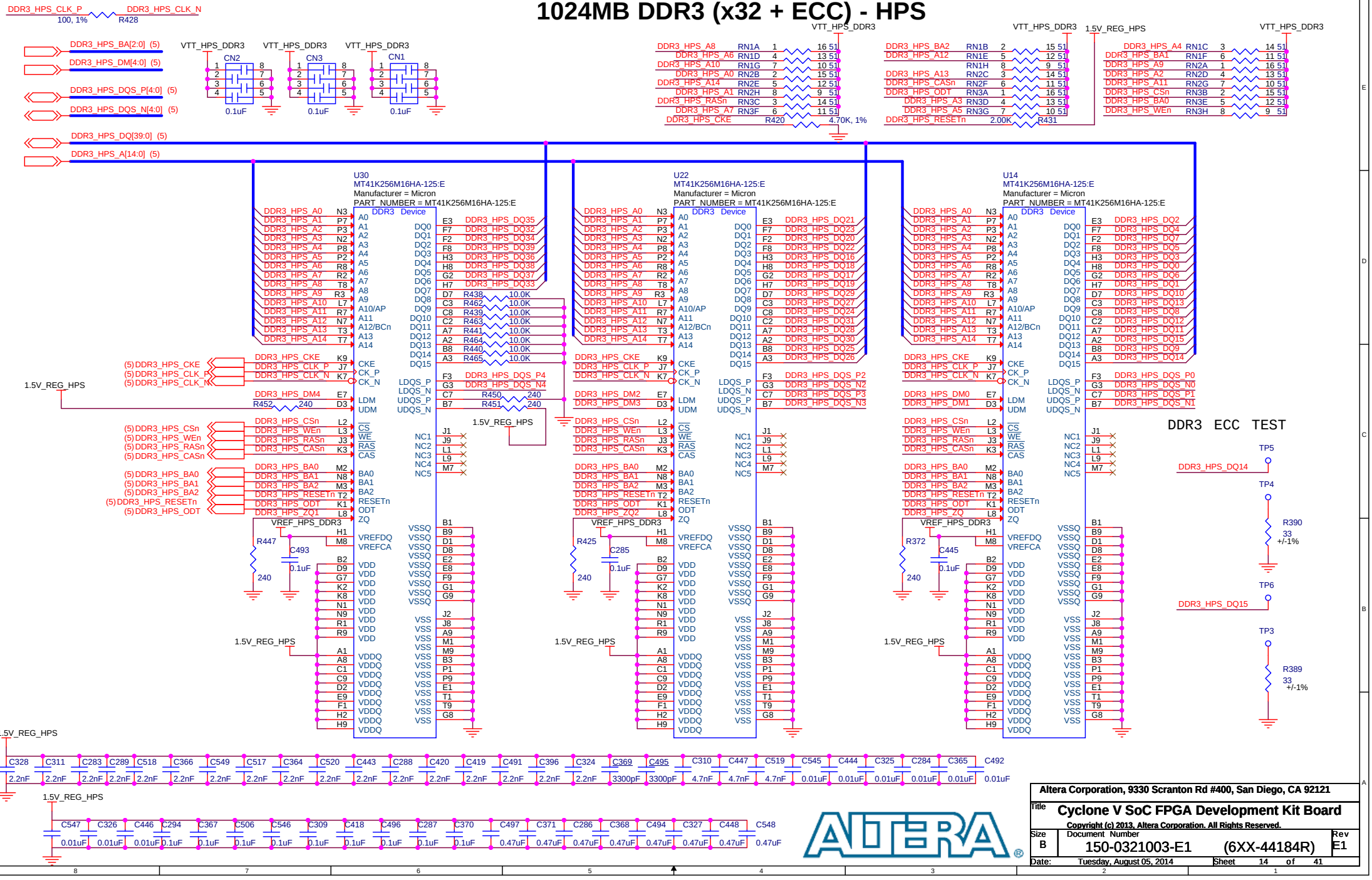
1024MB DDR3 (x32 + ECC) - HPS



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Title: **Cyclone V SoC FPGA Development Kit Board**

Size	Document Number	Rev
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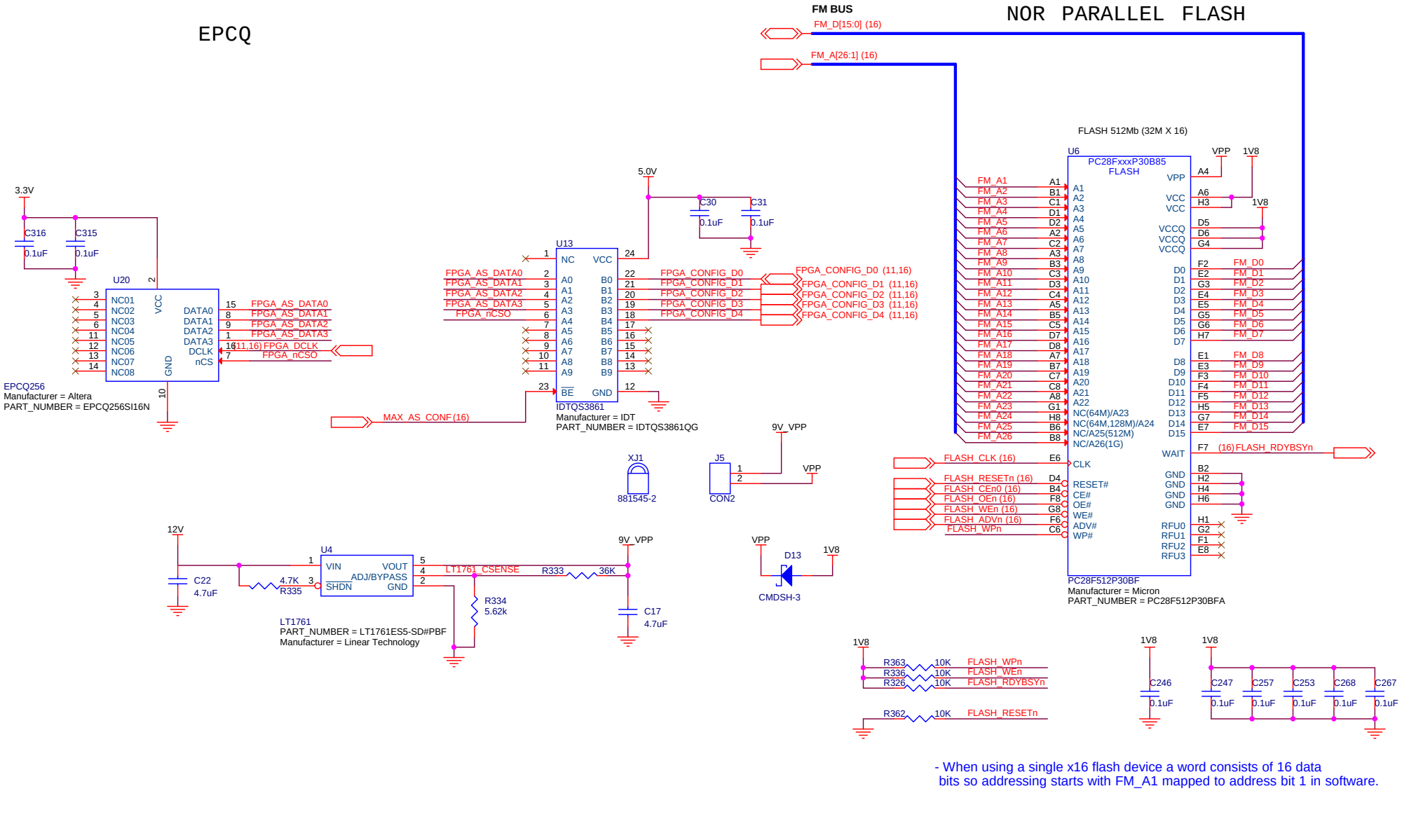
FLASH, EPCQ



- When using a single x16 flash device a word consists of 16 data bits so addressing starts with FM_A1 mapped to address bit 1 in software.

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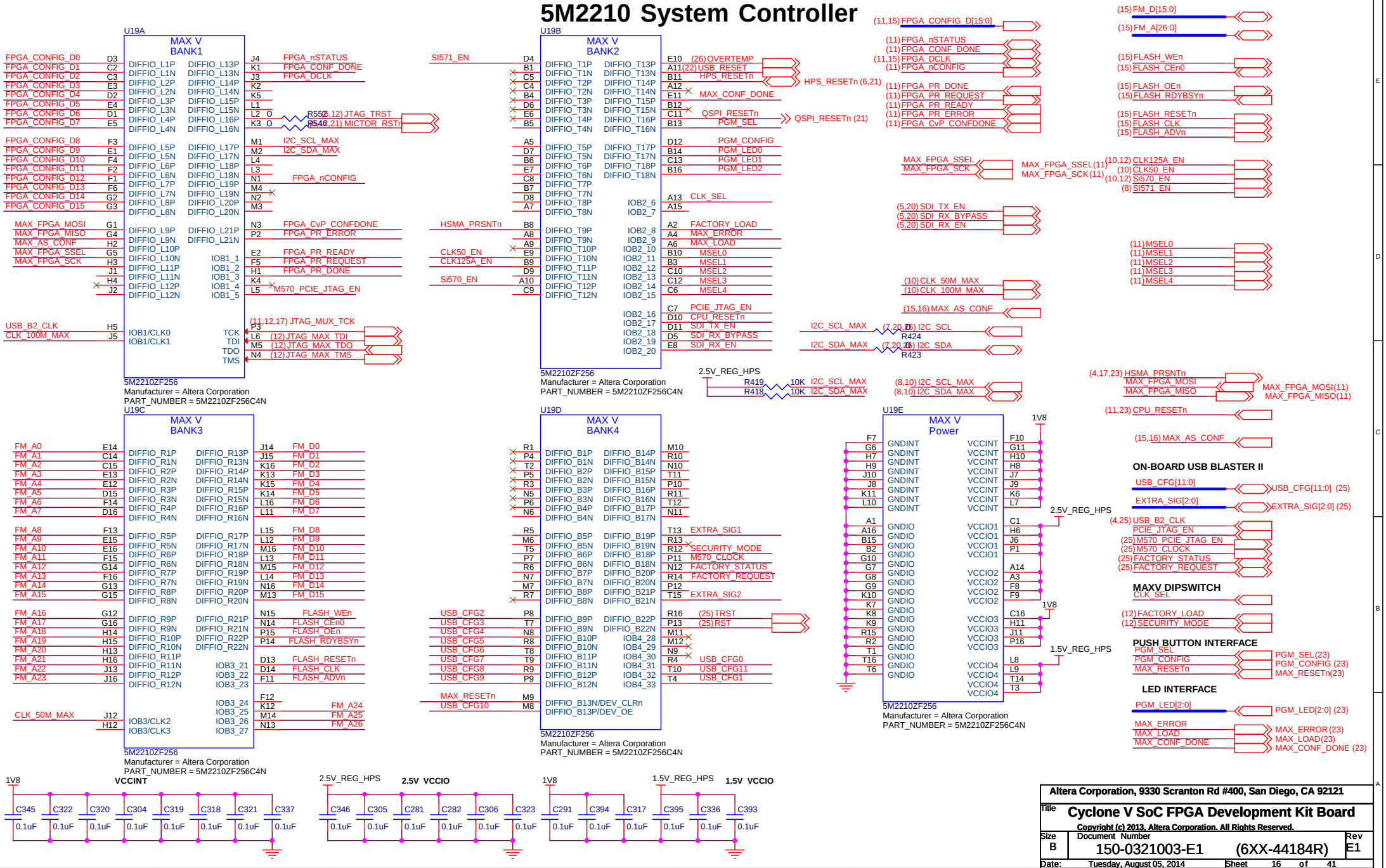
5M2210 System Controller



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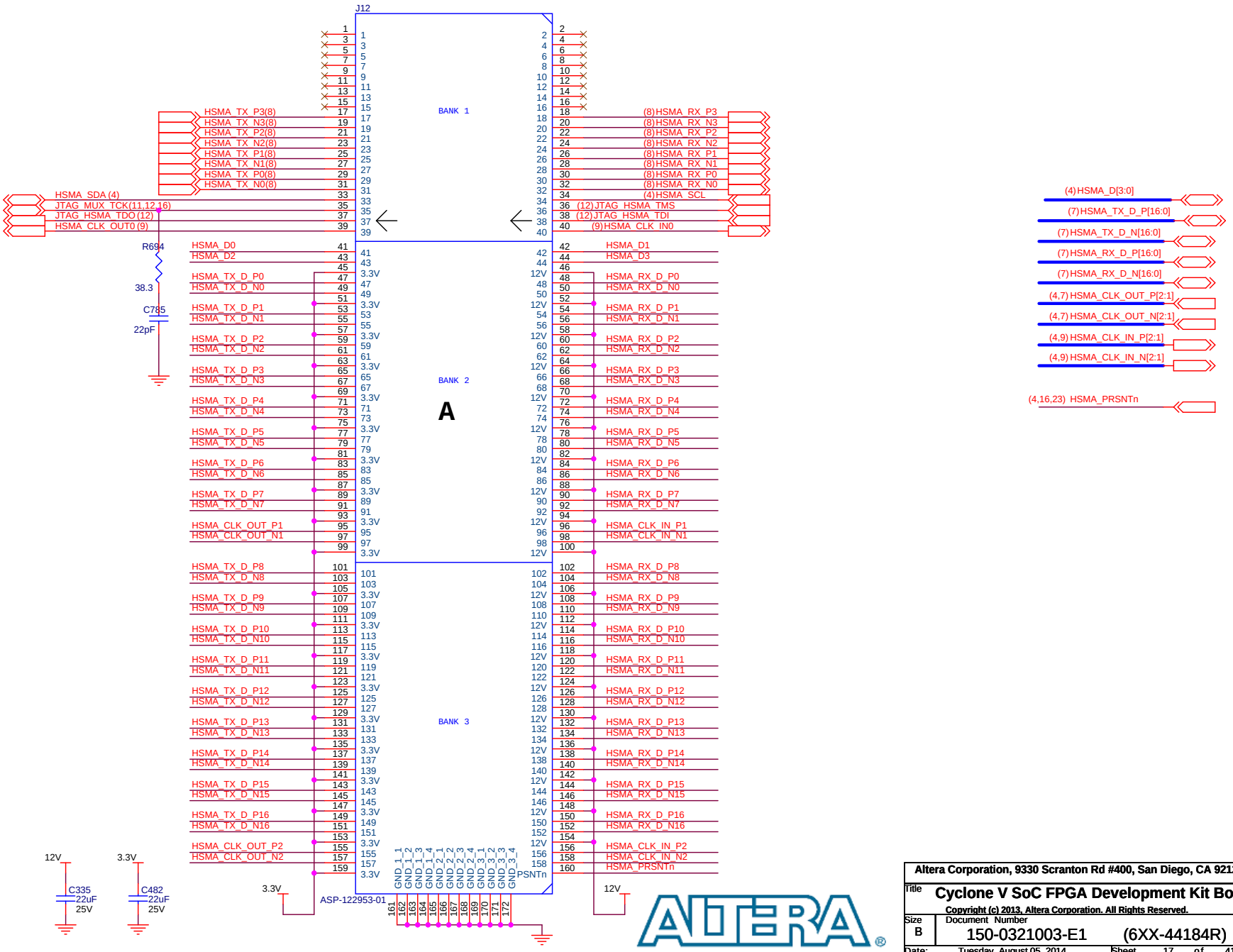
HSMC Port A



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Title	Cyclone V SoC FPGA Development Kit Board
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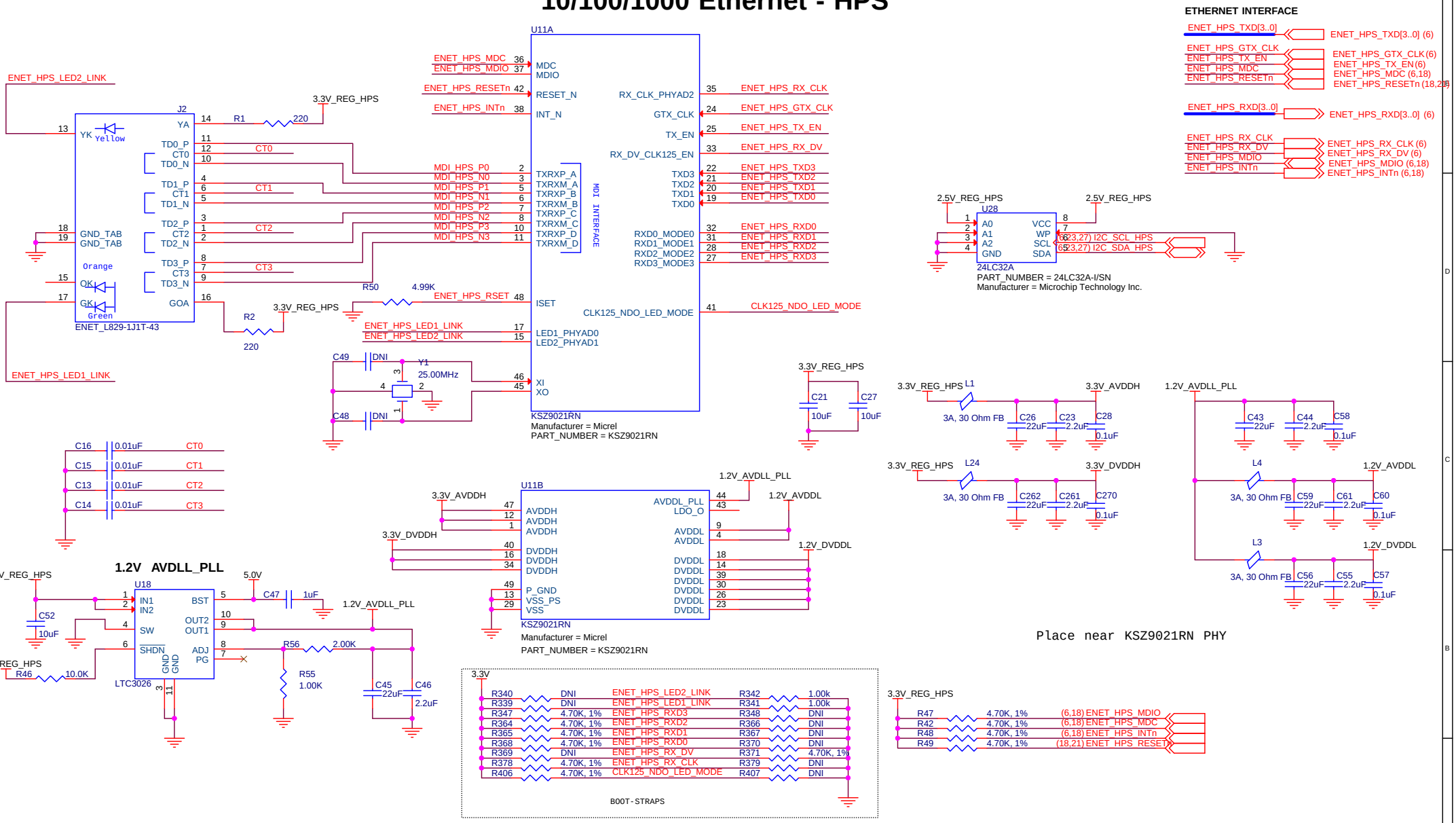
10/100/1000 Ethernet - HPS



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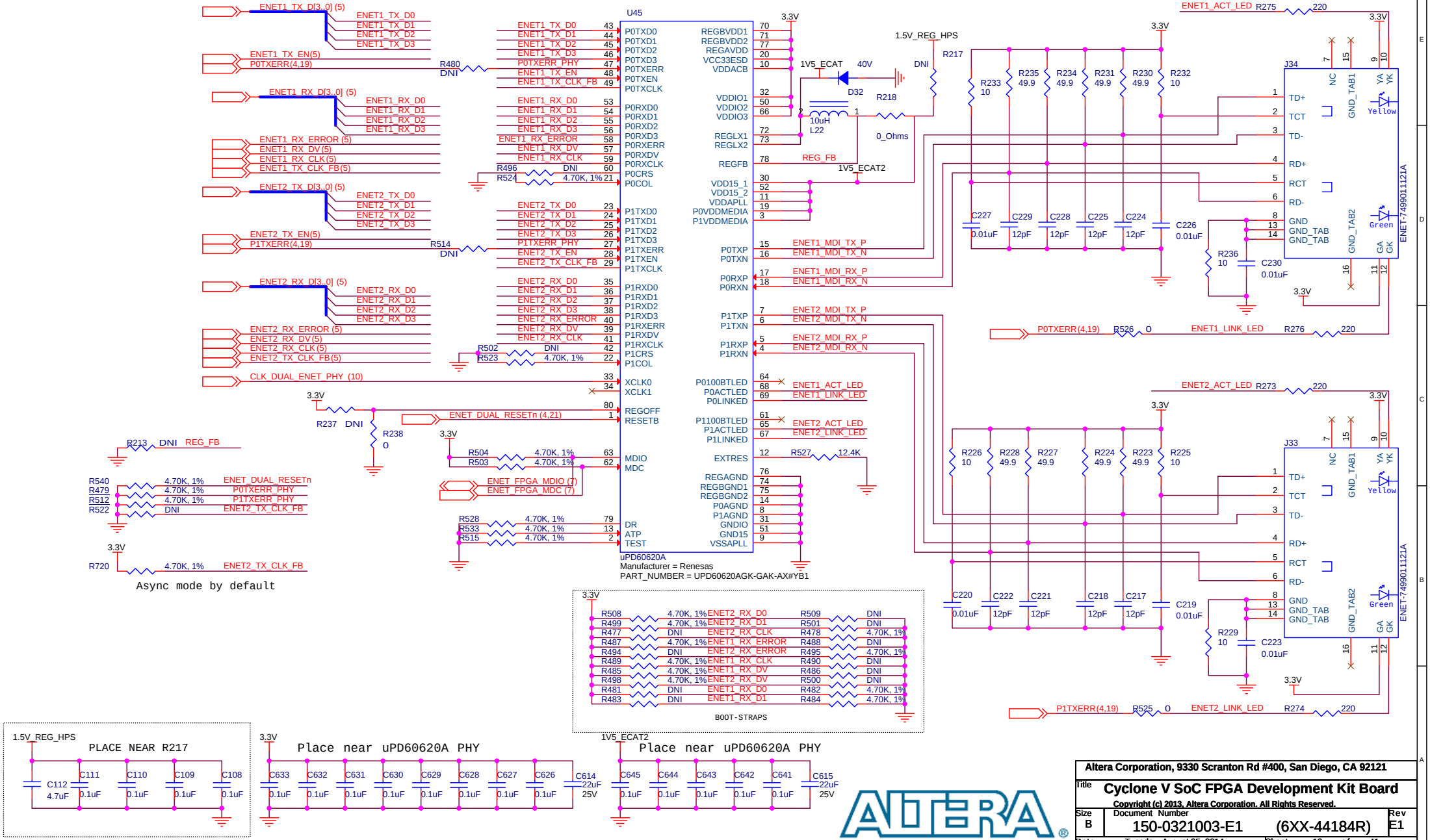
10/100M Ethernet - FPGA



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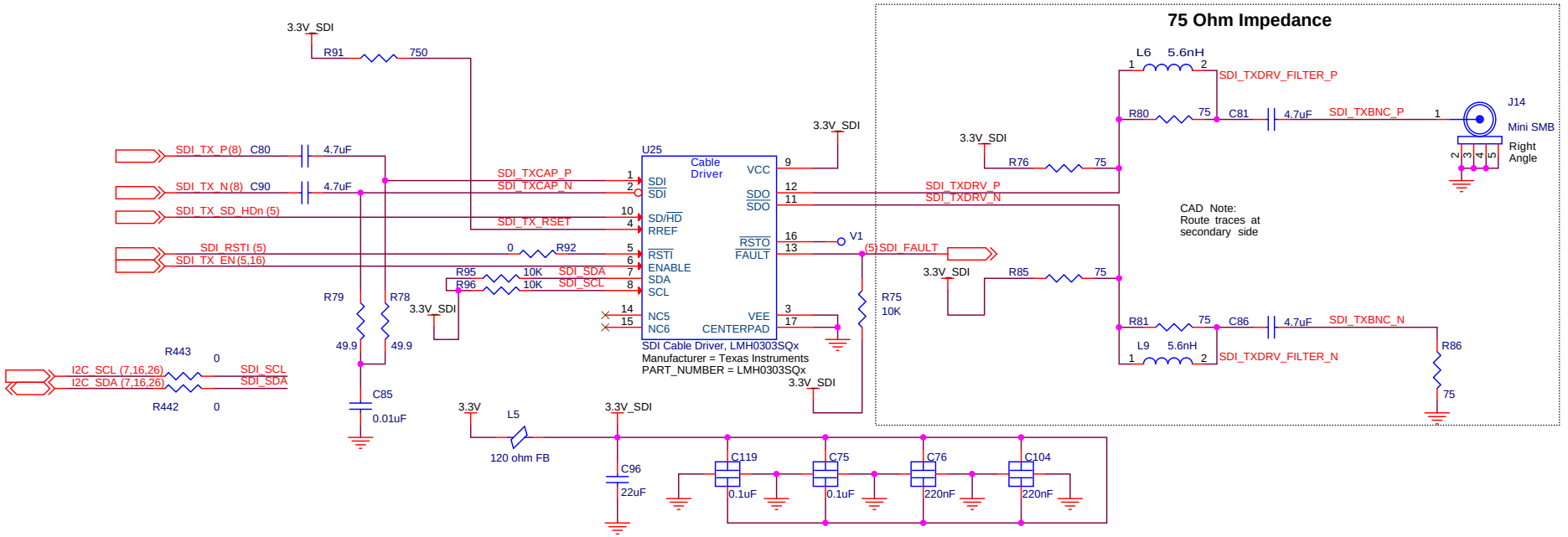
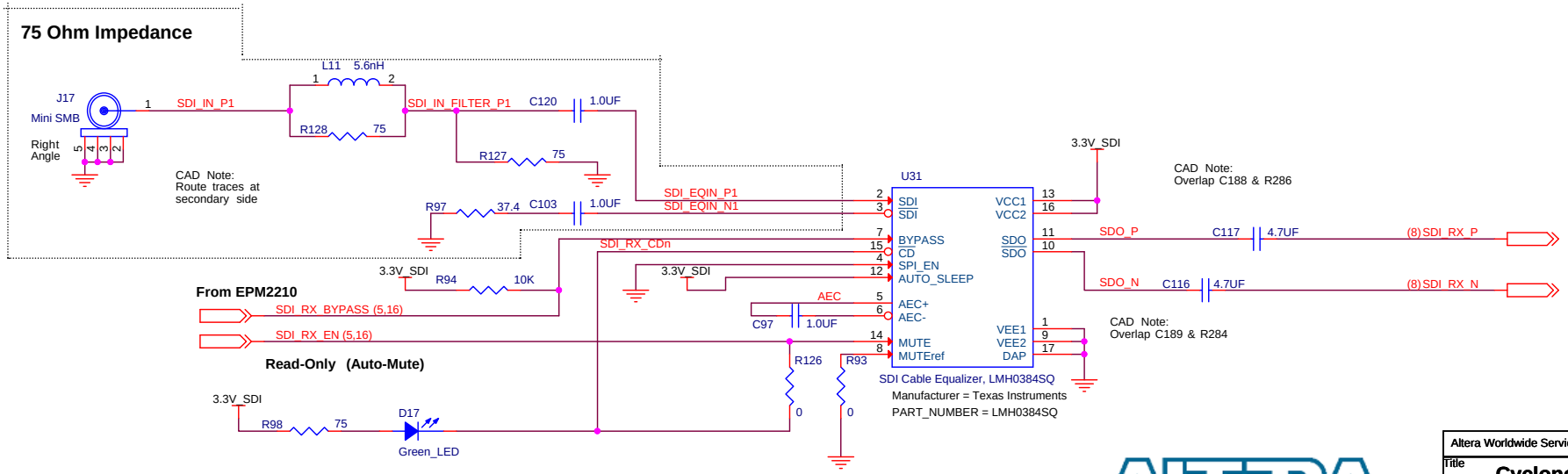
SDI Cable Driver, Equalizer, SMA Option and SMB





Altera Worldwide Service, Plot 6, Bayan Lepas Technoplex, Penang, Malaysia

Title: **Cyclone V SoC FPGA Development Kit Board**

Size	Document Number	Rev
B	150-0321003-E1 (6XX-44184R)	E1

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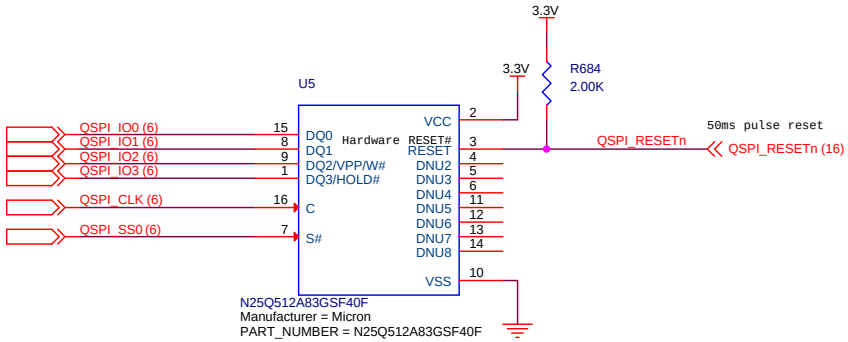
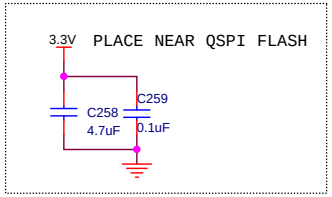
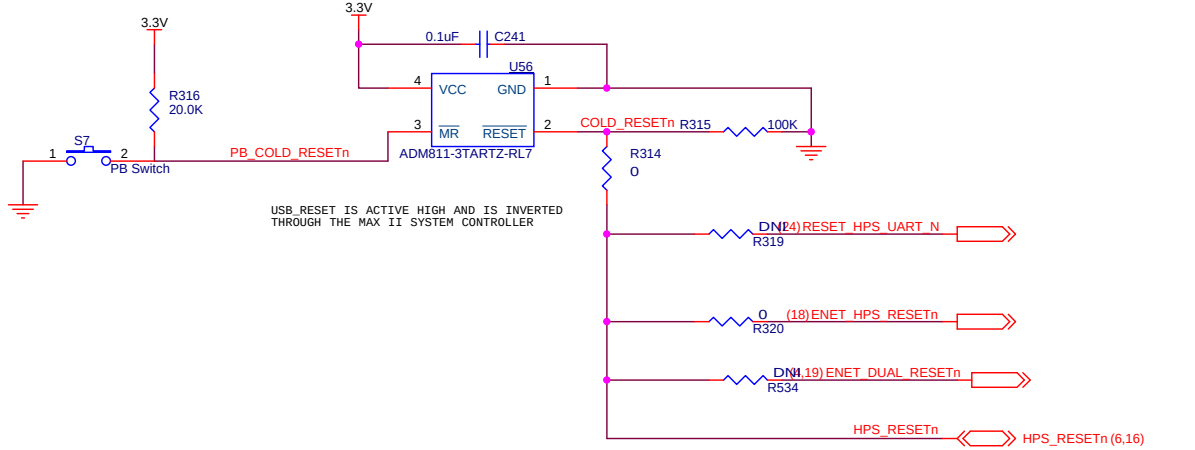
QSPI Flash & Reset Circuit

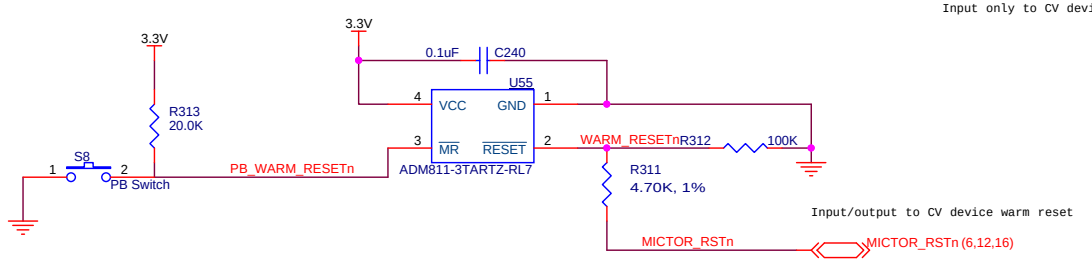
QSPI FLASH





RESET CIRUIT





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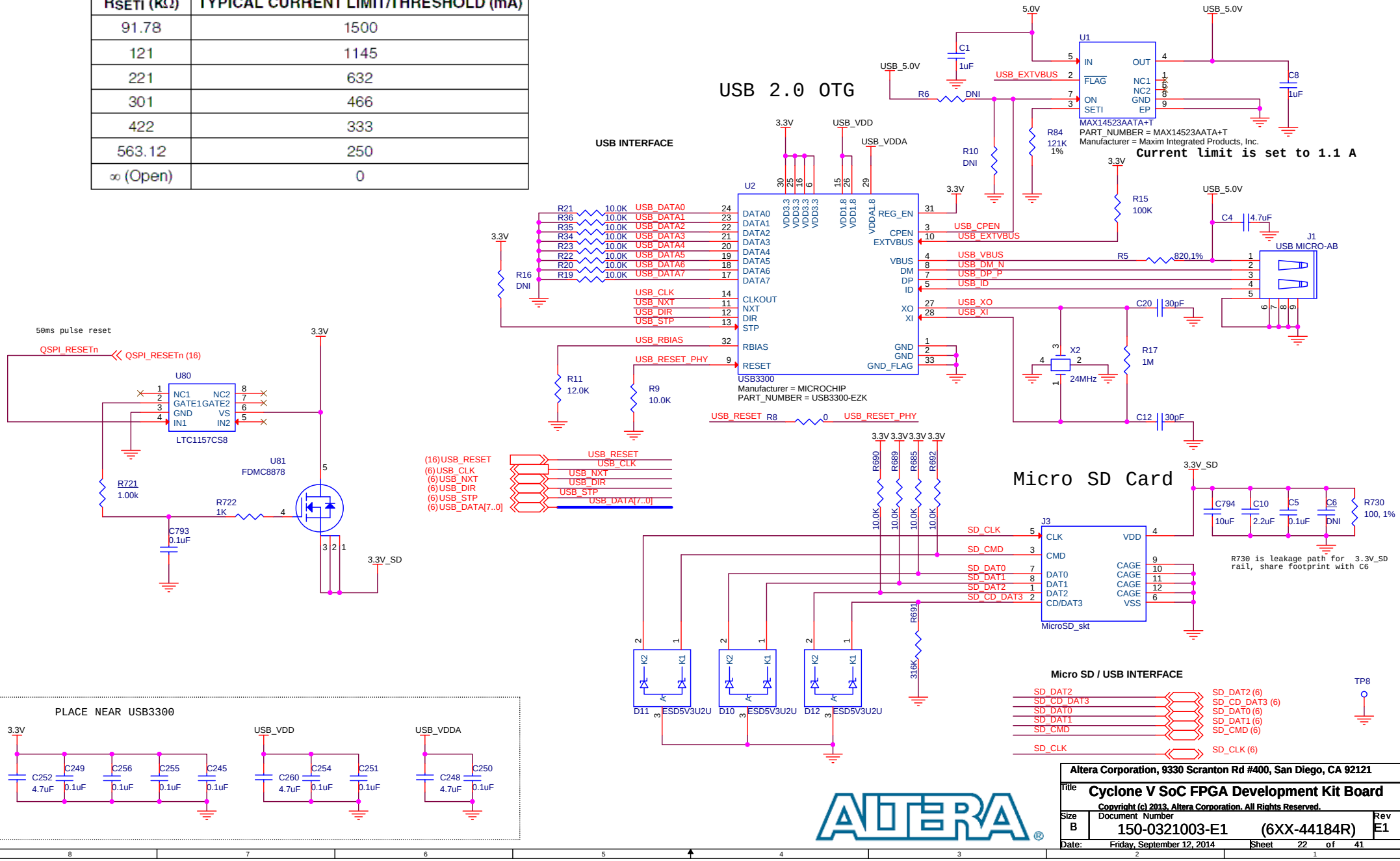
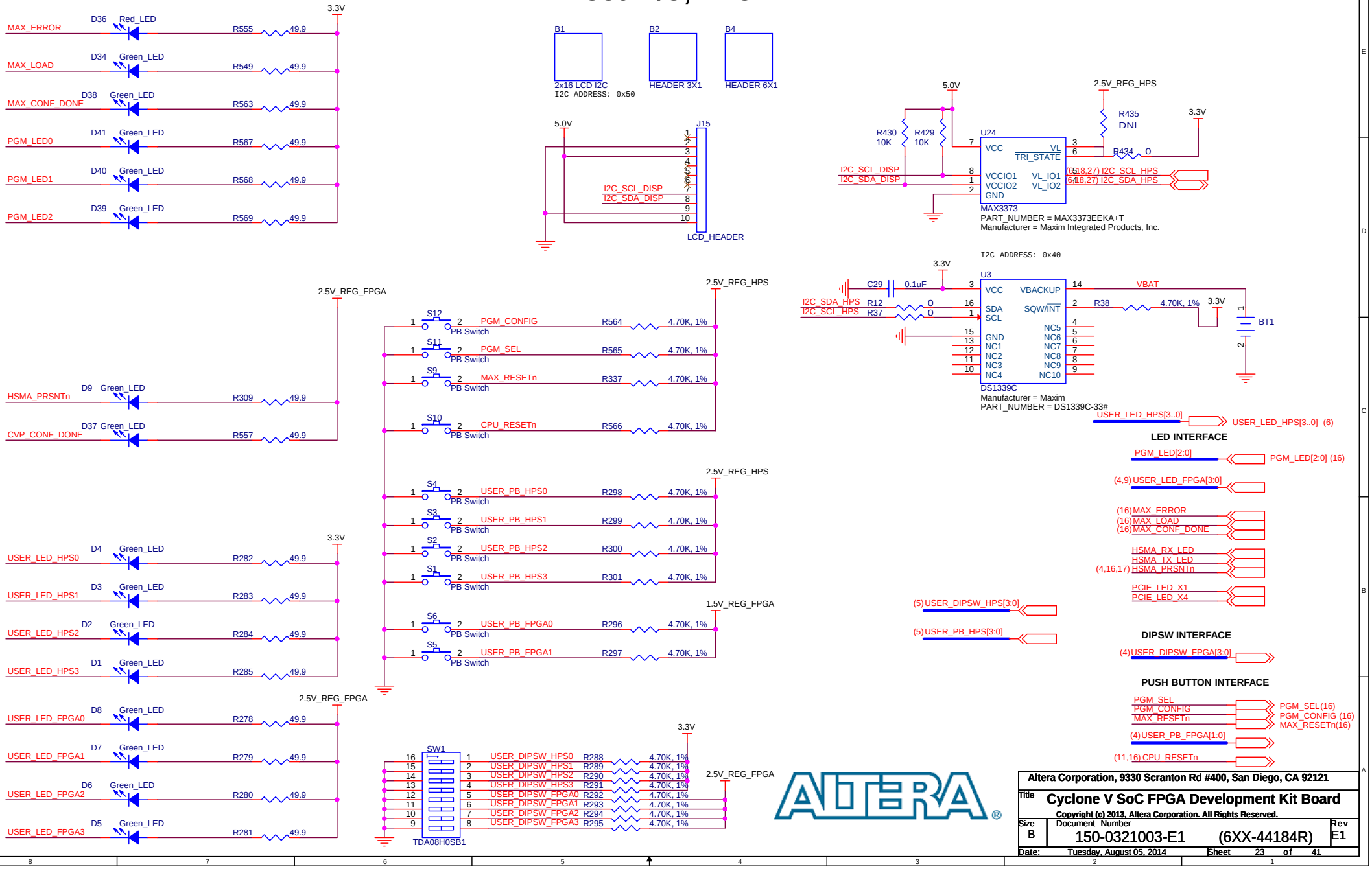
USB 2.0 OTG , Micro SD Card

R_{SETI} (kΩ)	TYPICAL CURRENT LIMIT/THRESHOLD (mA)
91.78	1500
121	1145
221	632
301	466
422	333
563.12	250
∞ (Open)	0



User I/O, RTC



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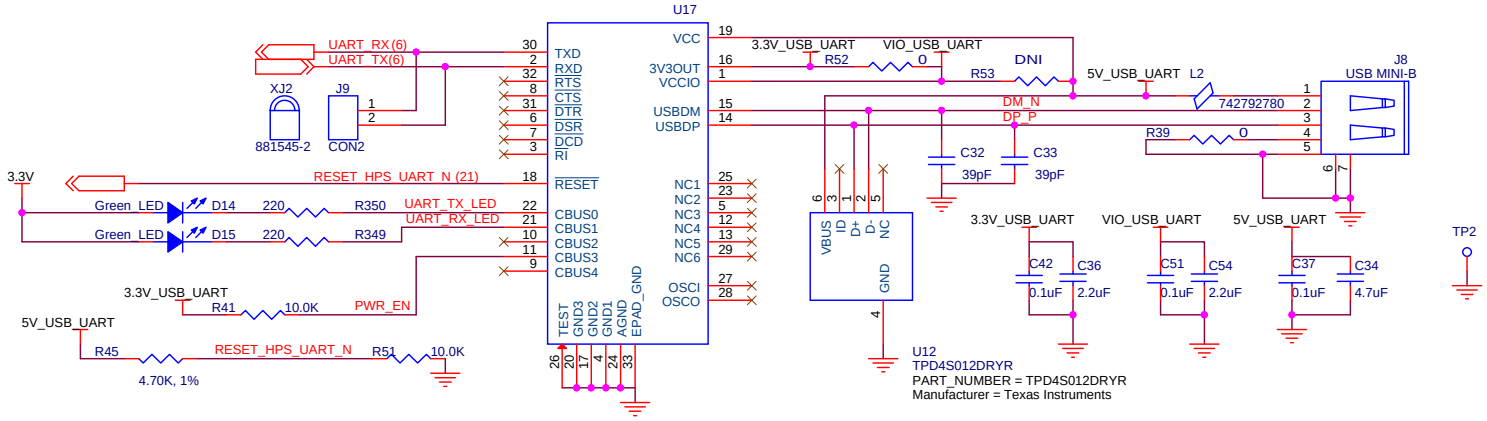
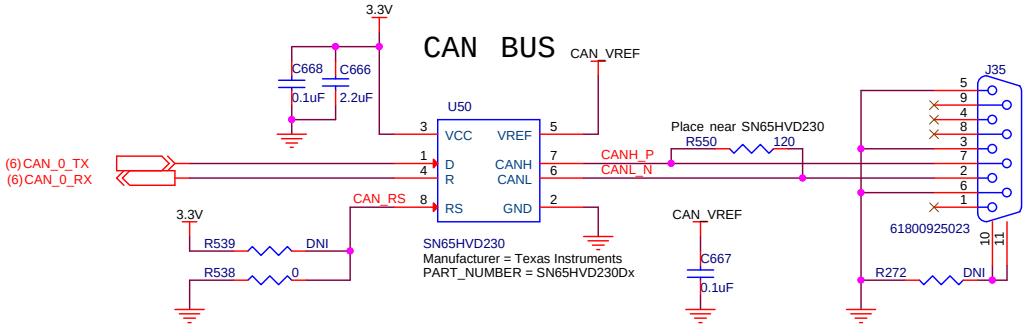
UART, CAN

UART





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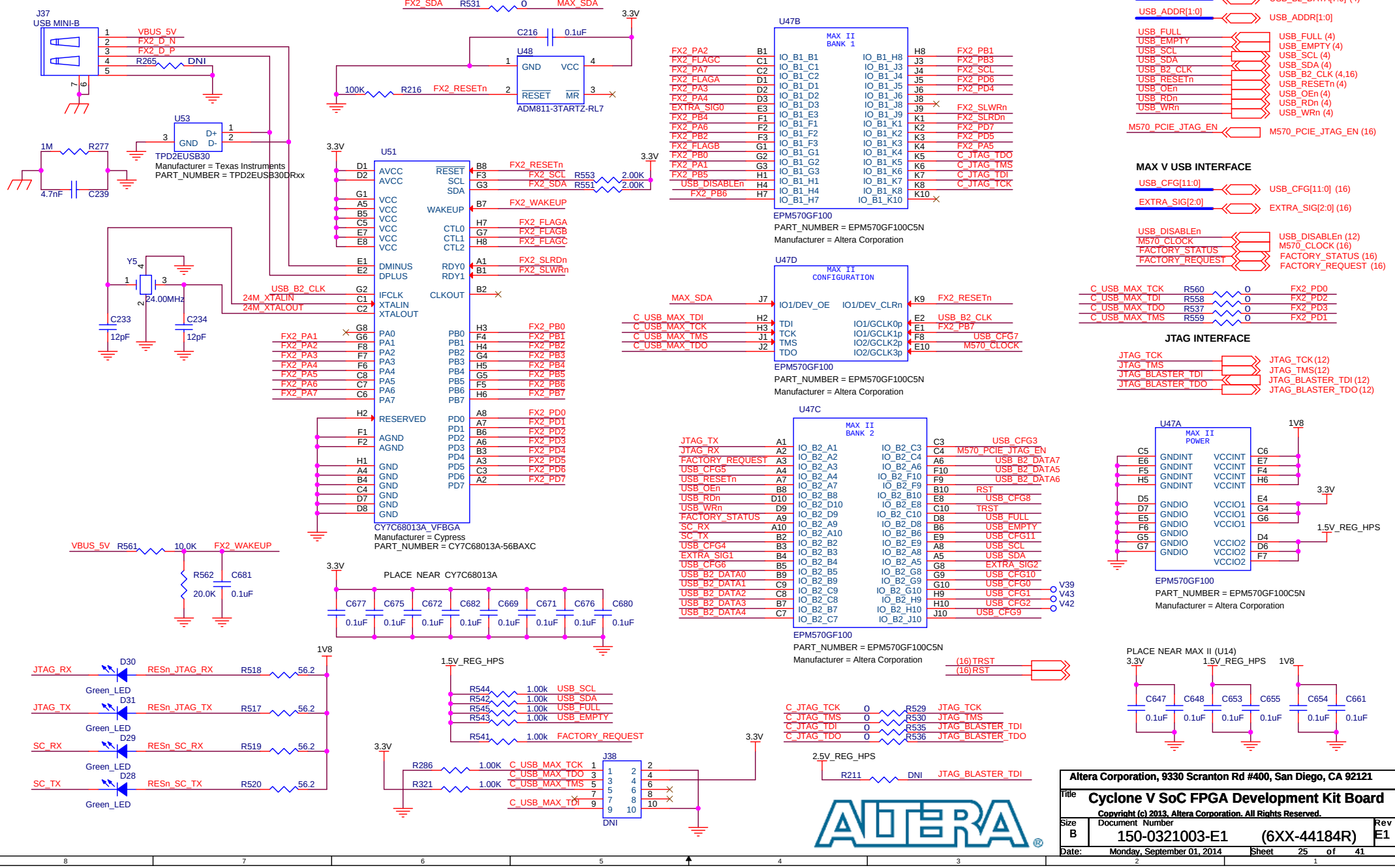
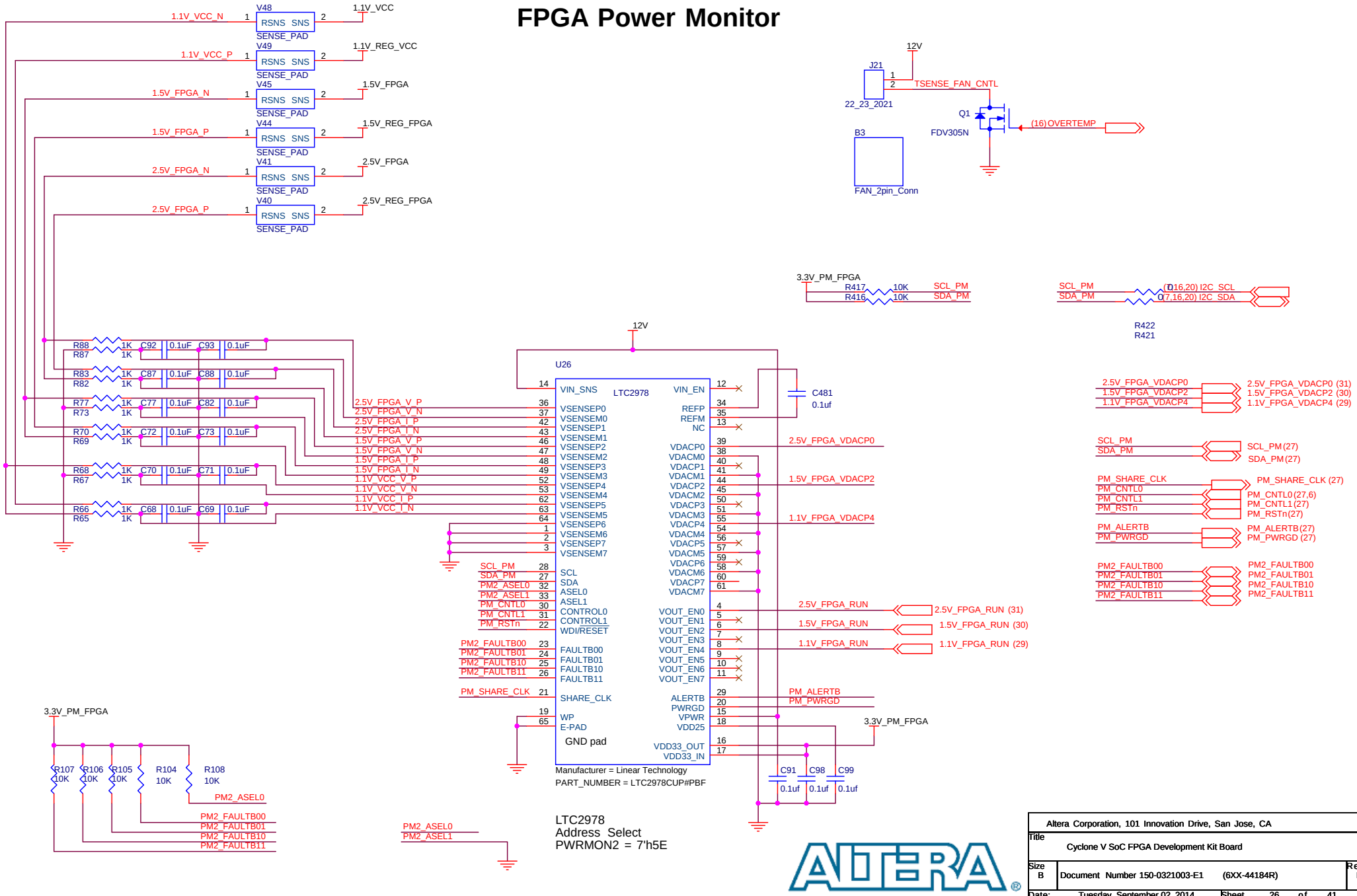
On-Board USB Blaster II



FPGA Power Monitor



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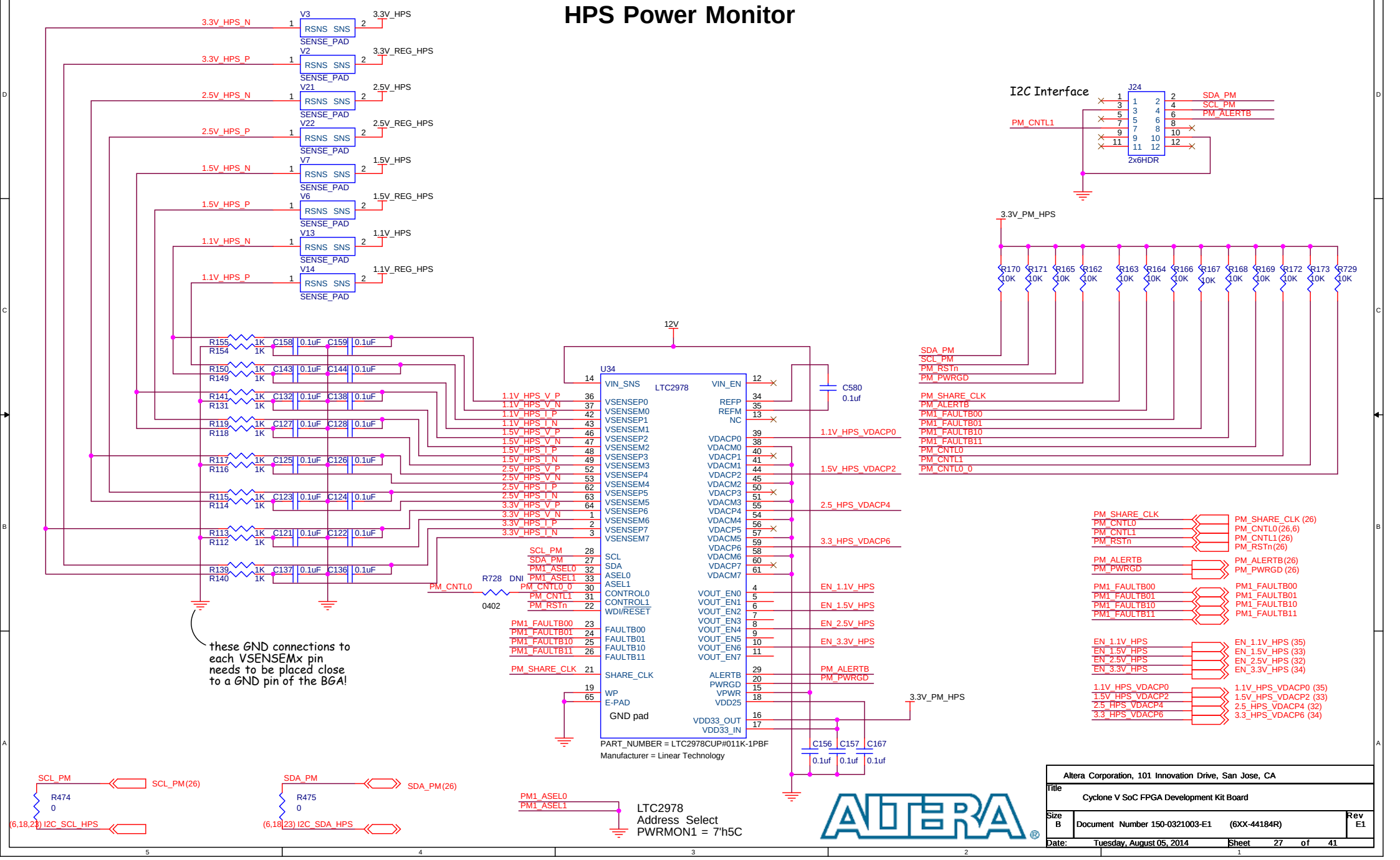
HPS Power Monitor



Altera Corporation, 101 Innovation Drive, San Jose, CA			
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Power 1 - DC Input & 12V, 3.3V Output

DC_INPUT only:
SW5 = ON, 12V_SHDNn = 3.3V_SHDNn = HIGH;
12V_SHDNn_1 = 2.38V which is larger than U78's UV
SW5 = OFF, 12V_SHDNn = 3.3V_SHDNn = LOW;
12V_SHDNn_1 = 0V which is less than U78's UV

12V_ATX only:
SW5 = ON, 12V_SHDNn = LOW, 3.3V_SHDNn = HIGH;
12V_SHDNn_1 = 1.5V which is same with U78's UV
SW5 = OFF, 12V_SHDNn = 3.3V_SHDNn = LOW;
12V_SHDNn_1 = 0V which is less than U78's UV

Don't support both DC_INPUT and 12V_ATX case

There are totally 2x22uF+2x47uF buck cpas on DC_IN rail, the value of C788 need to be set based on this.

There are totally 11x22uF buck cpas on 12V rail, the value of C791 need to be set based on this.

LTC3855EUJ
Manufacturer = Linear Technology
Manufacturer Part Num = LTC3855EUJ#PBF

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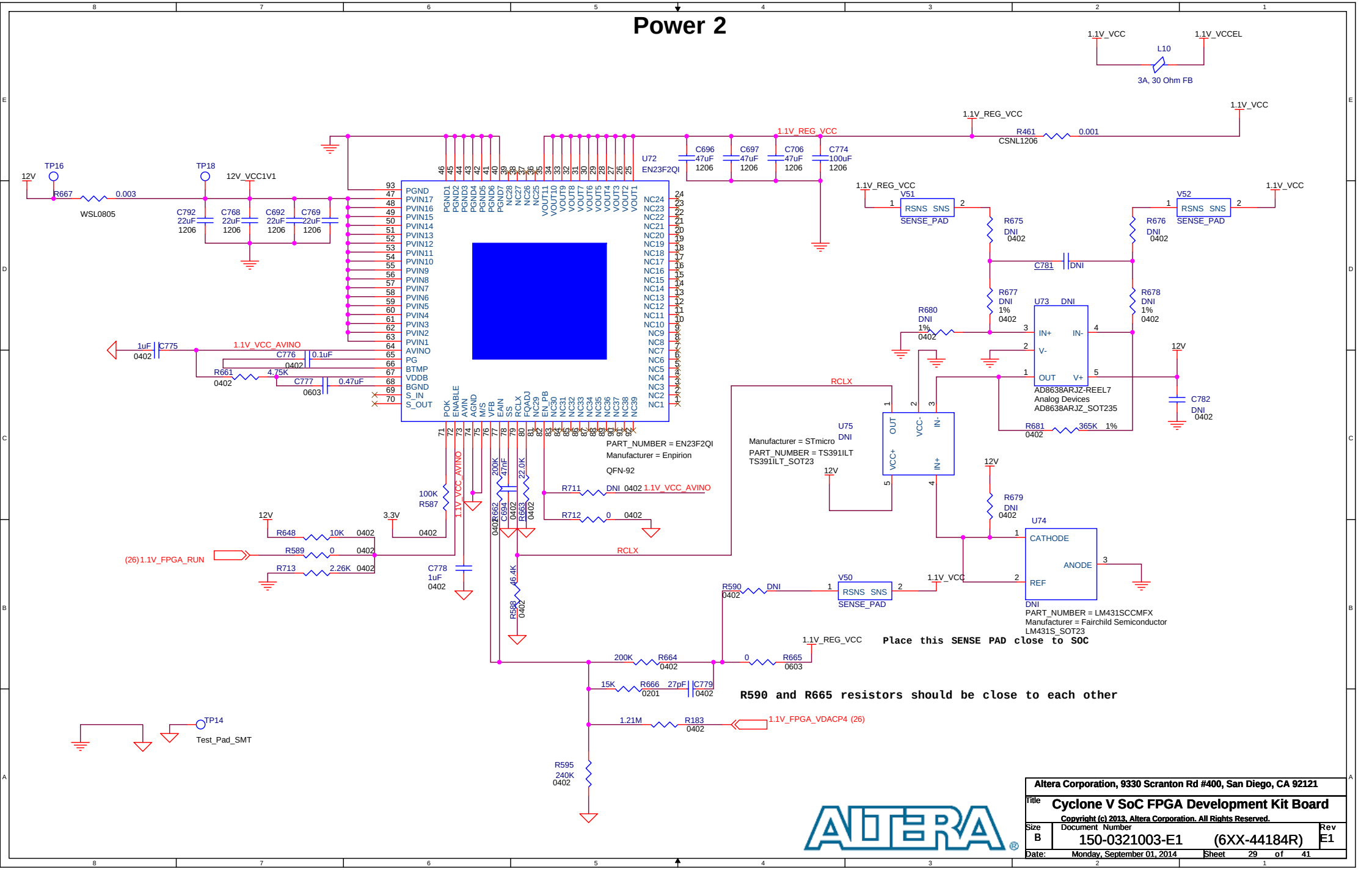
Power 2



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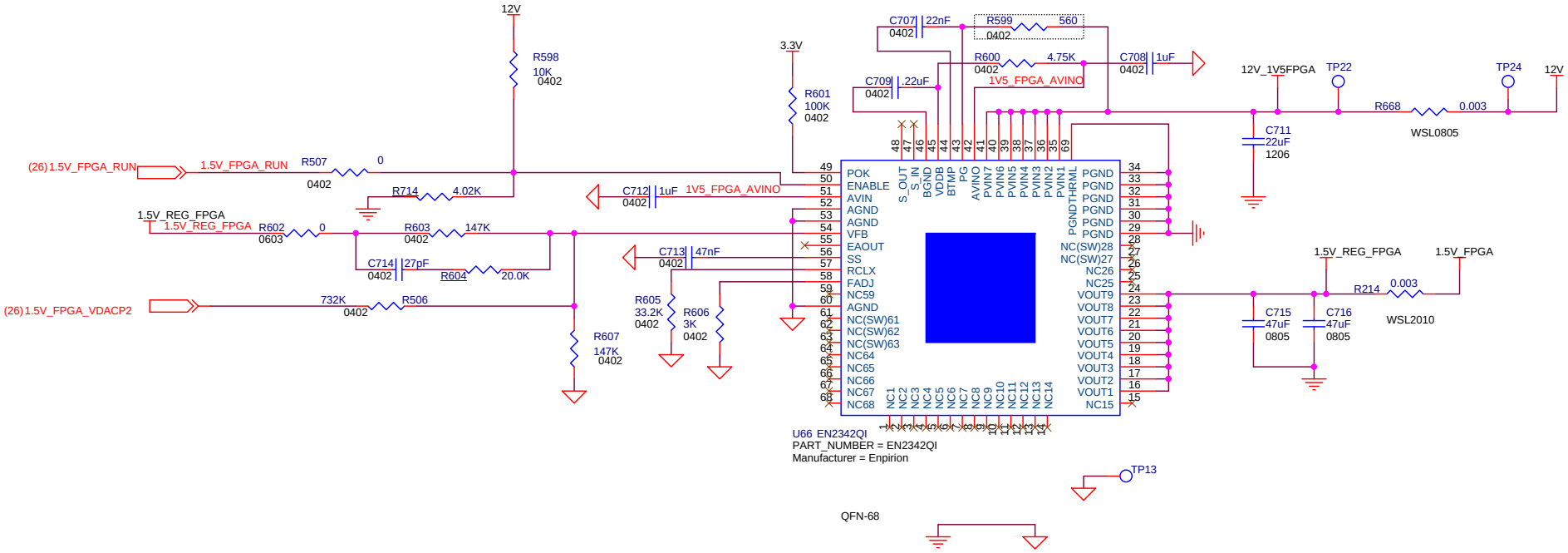
Power 3 - 1.5V FPGA



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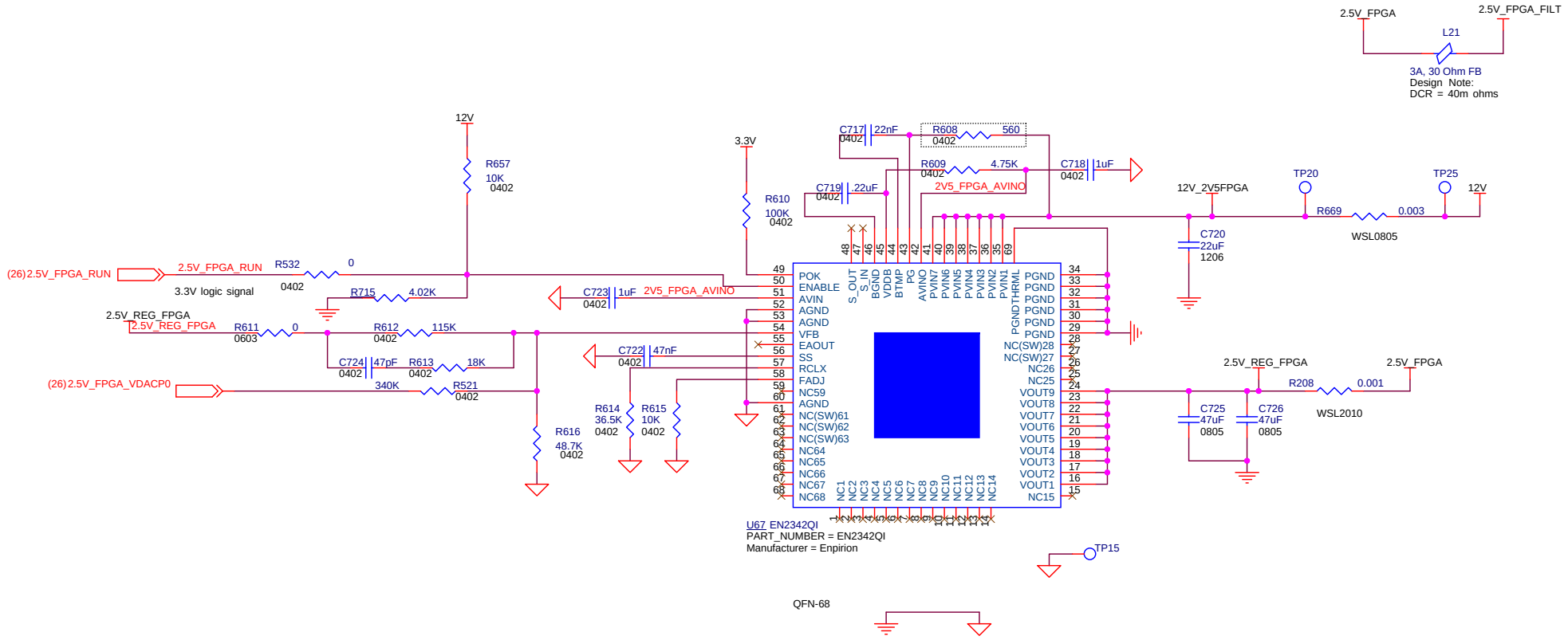
Power 3 - 2.5V FPGA



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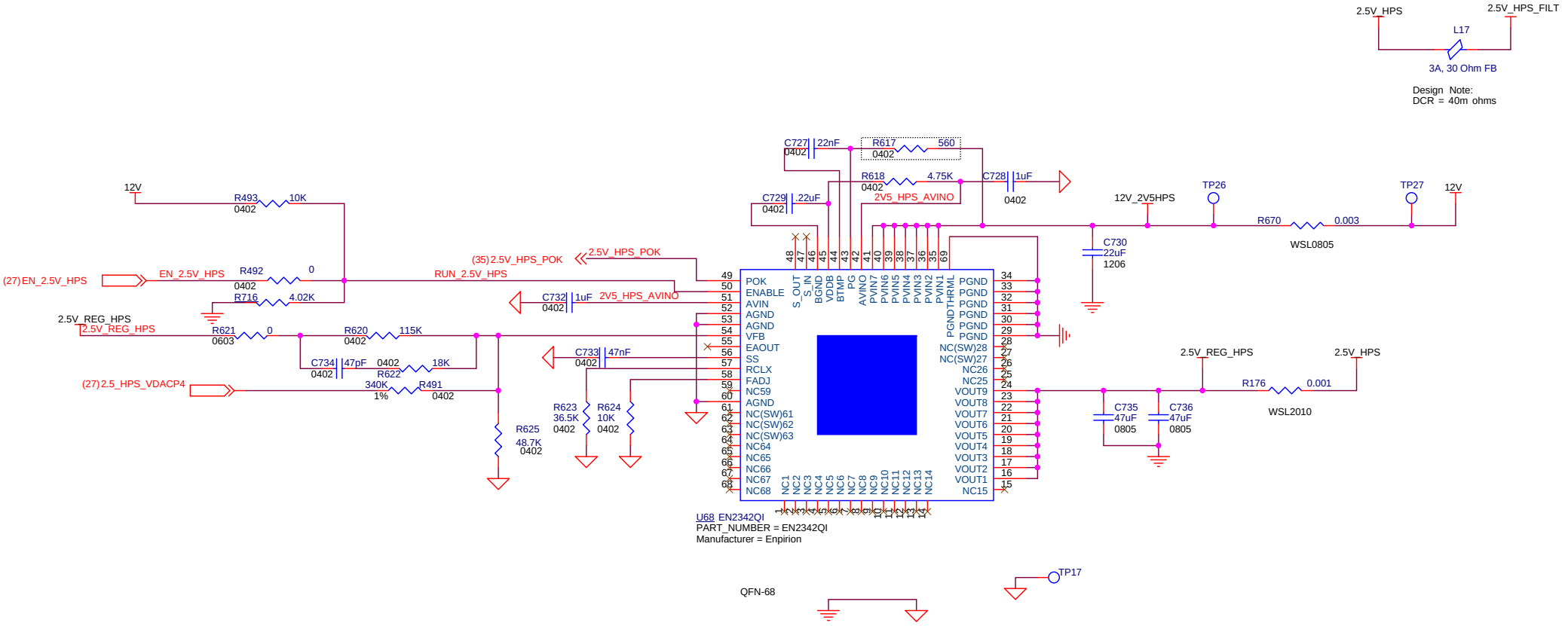
Power 3 - 2.5V HPS



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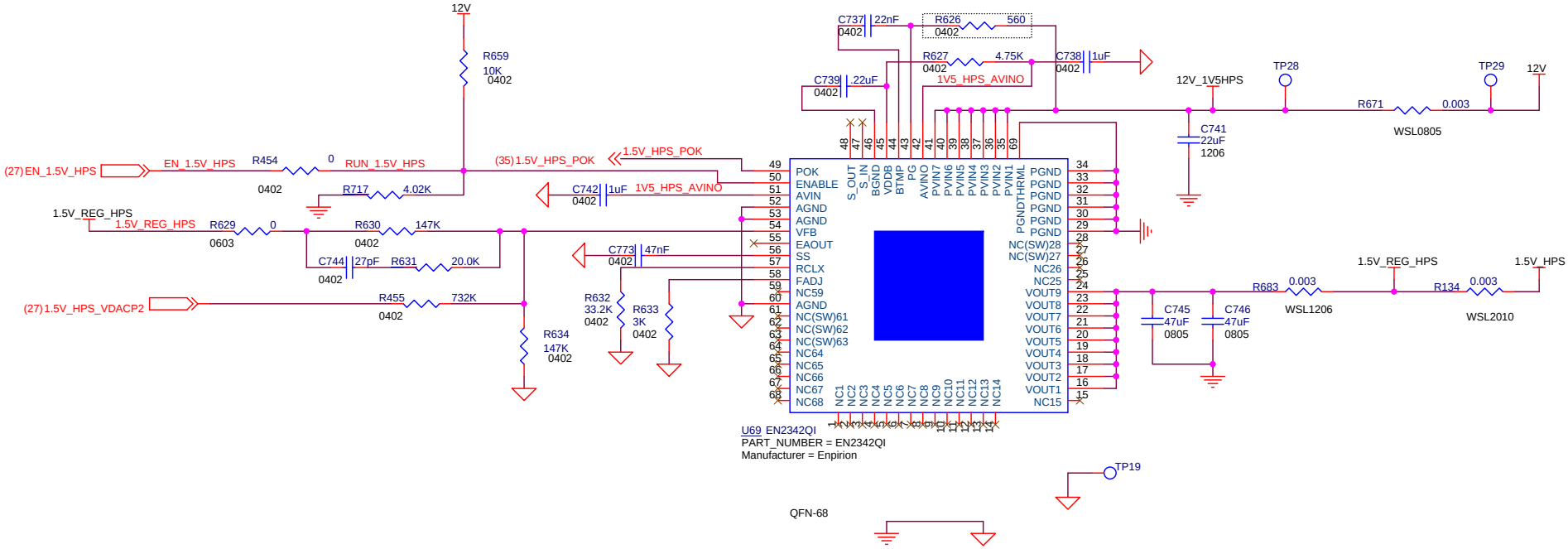
Power 3 - 1.5V & 1.5V HPS



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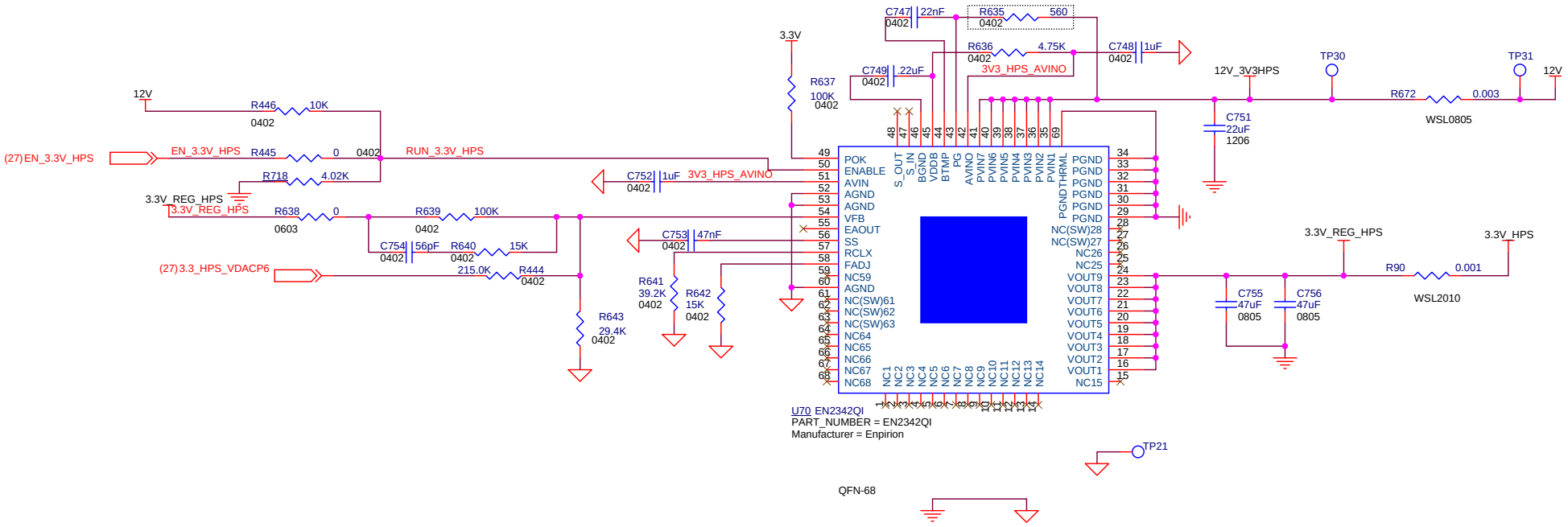
Power 3 - 3.3V HPS



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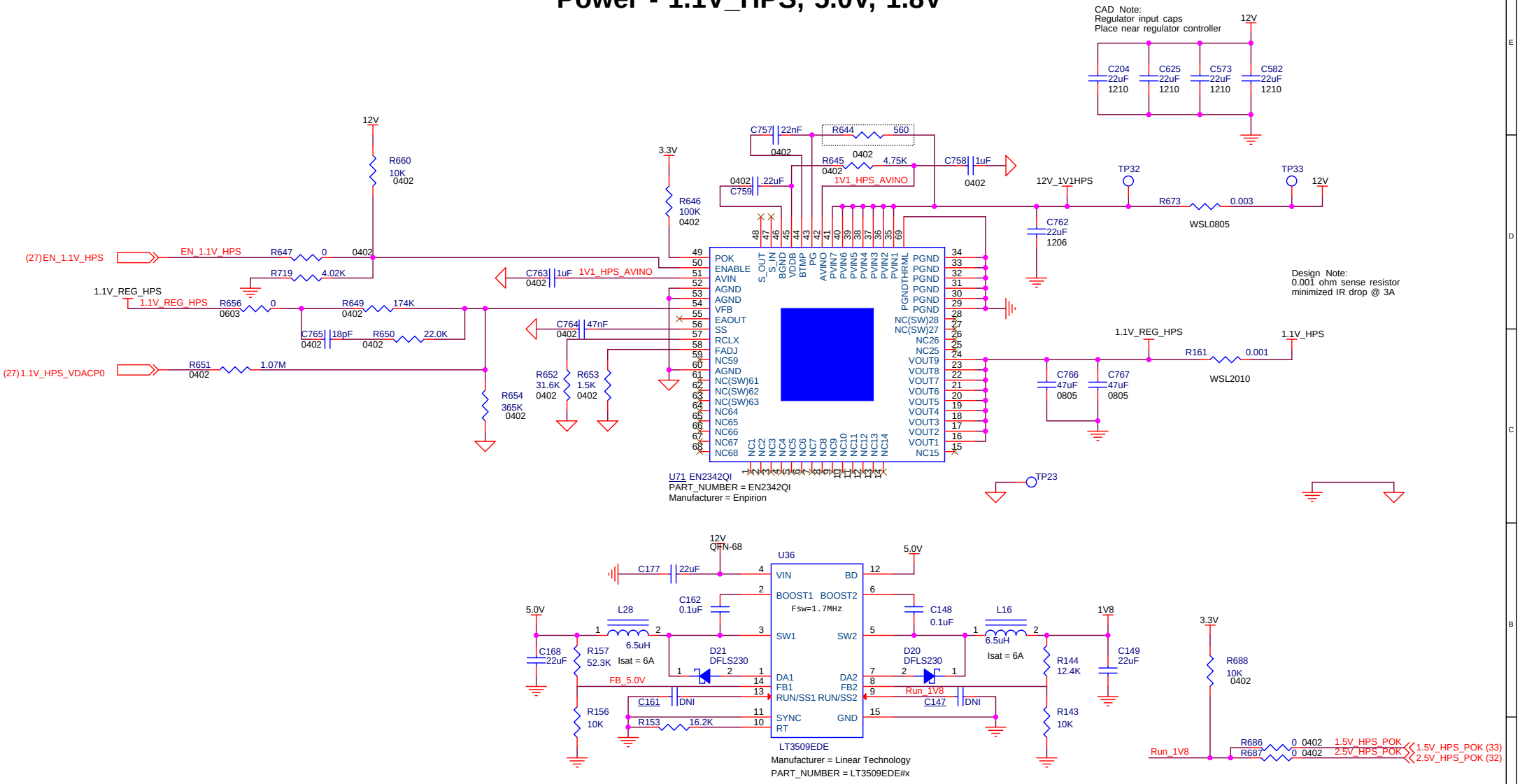
Power - 1.1V_HPS, 5.0V, 1.8V



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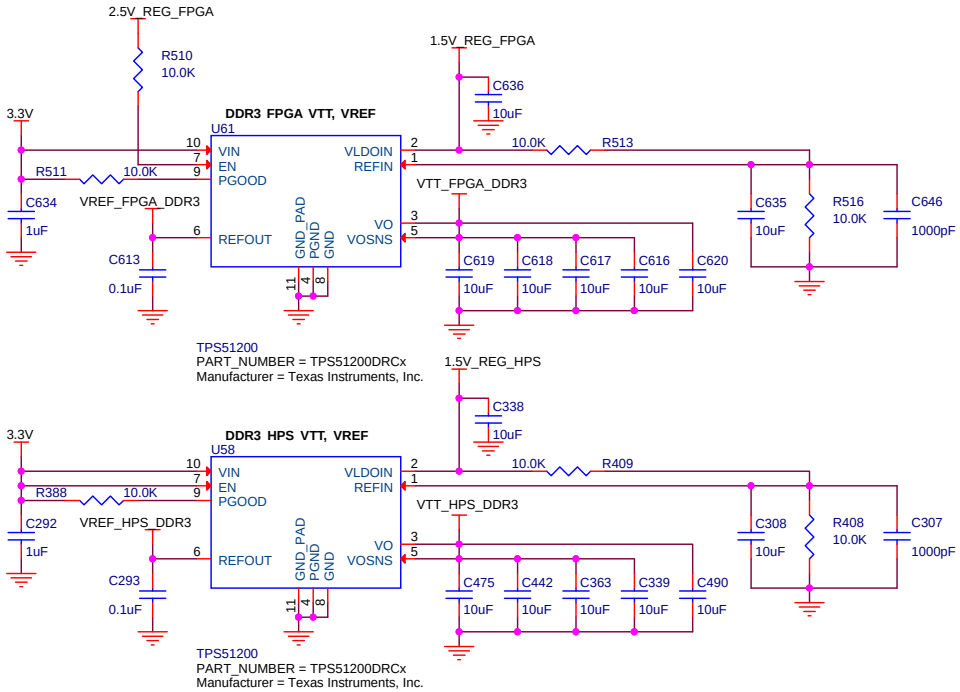
Power 4 - Linear Regulators



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Power 6 - Power & Temperature Monitor

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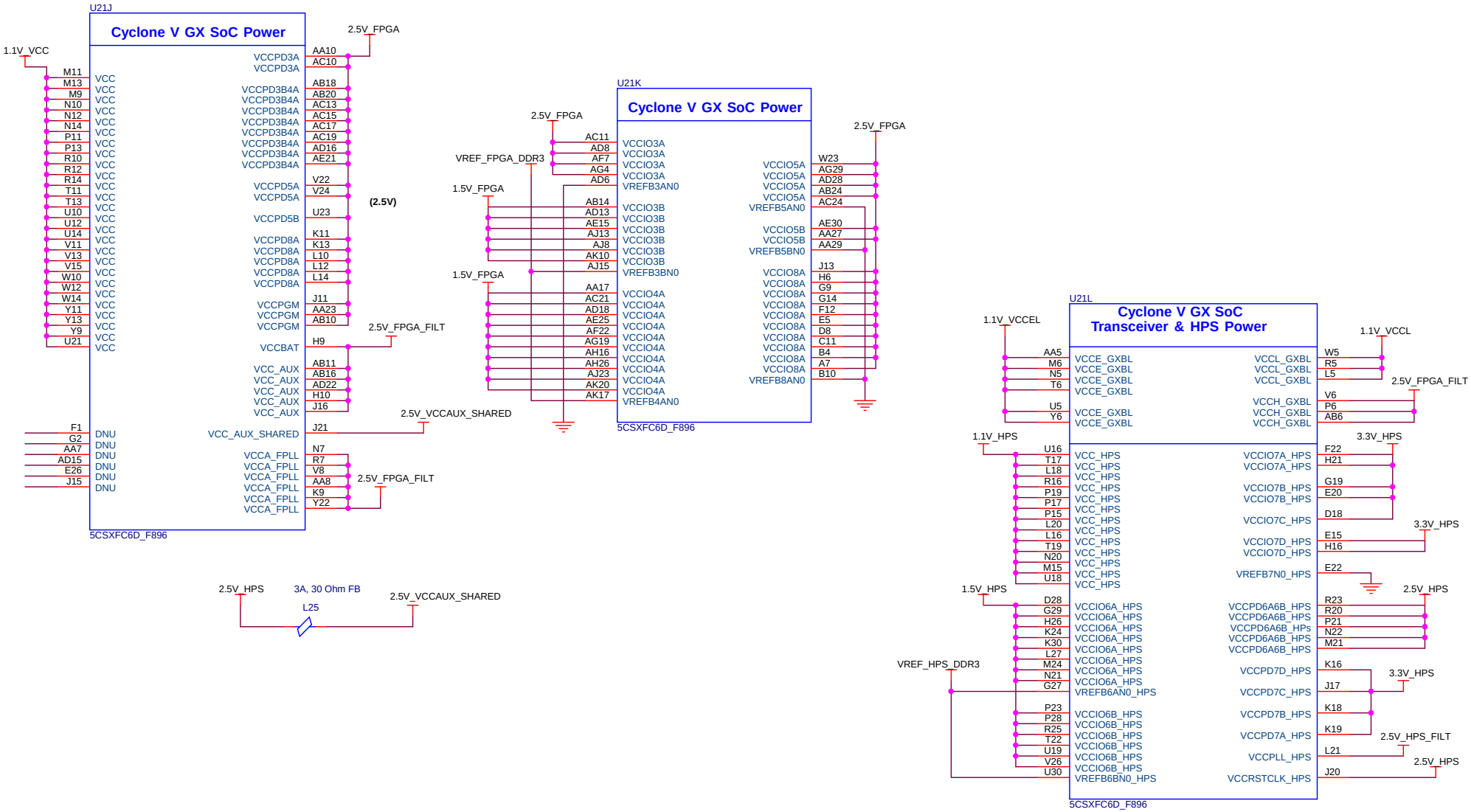
Power 7 - Cyclone V GX SoC Power



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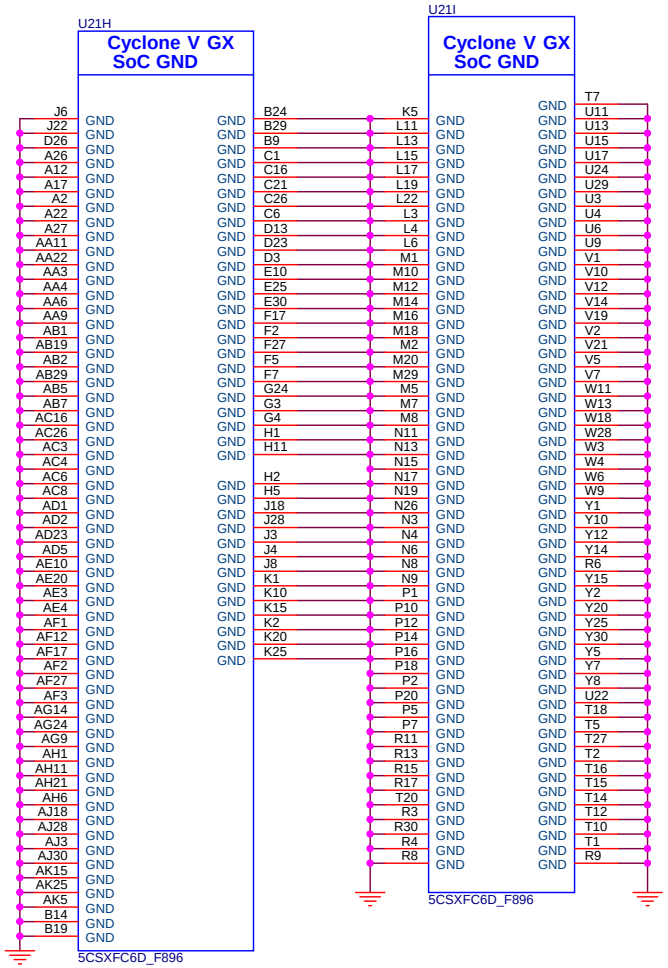
Power 8 - Cyclone V GX SoC Ground



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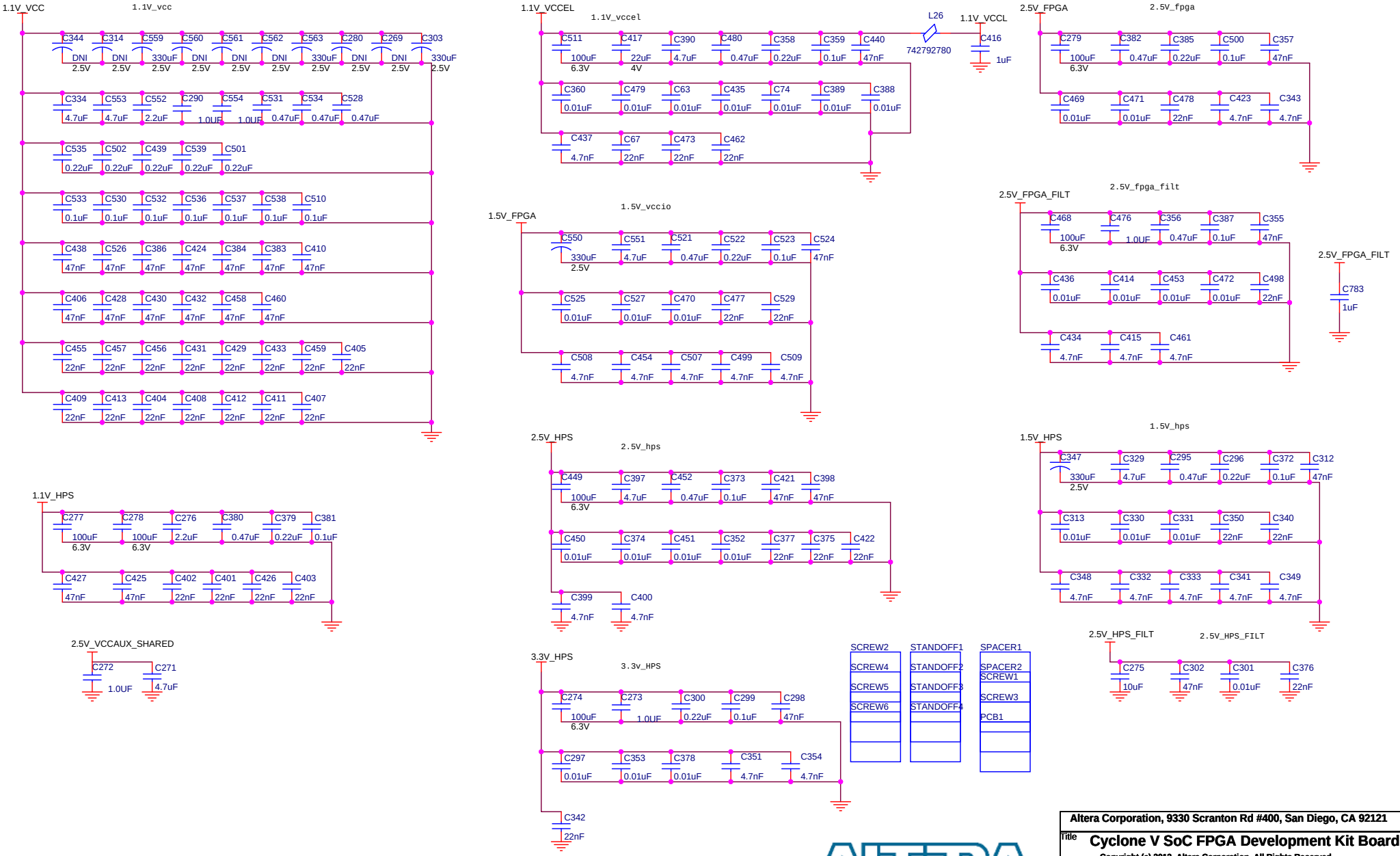
Decoupling



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REV	DATE	PAGES	DESCRIPTION
E1	7/11/2014	28	Add two Hot-Plug Controller circuit (LTC4218)
	7/11/2014	28	When 12V_ATX is using, auto disable LTC3855' s 12V_REG by S_W5
	7/11/2014	29-35	Generate ENABLE signal using resistor divider circuit for all Enpirion parts
	7/11/2014	29	One more 22uF bulk cap for EN23F2QI PVIN rail
	7/11/2014	29-35	Replace EN23F0QI with EN23F2QI, EN2340QI with EN2342QI
	7/11/2014	29	Put option for pre-bias circuit on EN23F2QI CGND (EN_PB) pin
	7/11/2014	29	Changing switching frequency of EN23F2QI (R663=22K)
	7/11/2014	29	DNI external current limitation circuit of EN23F2QI
	7/11/2014	40	DNI some 330uF bulk decoupling caps for 1.1V VCC rail, only use C559, C563 and C303
	7/11/2014	19	Change Dual Ethernet PHY to async mode by default with R720
	7/11/2014	6,27	HPS GPIO control the FPGA power management chip
	7/11/2014	22	Add hard reset SD card (power recycle)
	7/11/2014	6	Use jumper J39 to replace R32 resistor
	7/11/2014	5,6	Update 5CSXFC6D_F896 schematic symbol on HPS_GPI[13:0] and VCCRSTCLK_HPS
	7/11/2014	8	Move R137/R135 to the right side of R138/R136
	7/15/2014	8	Change R57 to 180K, change R58,R58 to 4.99K ohm
	8/01/2014	29	Change R588 to 46.4K for EN23F2QI parts which has data code U418 or higher
	8/29/2014	21, 25	Replace U48/U55/U56 with ADM811-3T for longer delay
	9/12/2014	22	Replace R721 with 1K. Replace C6 with R730 100ohm resistor.

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