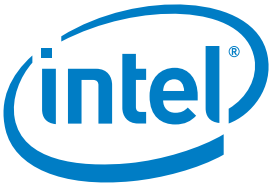

Intel® Enpirion® Power Solutions

Intel Arria® 10 Power Solution Reference Design – 30W Core

Reference Design Overview

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1. Description

This reference design demonstrates a complete power solution for a 30W core Intel® Arria® 10 FPGA or SoC FPGA design with complementary peripherals. This design is an upgraded variant of the power solution design used with Intel's Arria 10 SoC Development Kit. This solution is intended to provide a complete and validated Intel Arria 10 power solution, using Intel Enpirion® Power Solutions to achieve excellent power performance and high overall board power density.

This reference design provides complete power tree schematics. Intel implemented the design in hardware to perform an extended suite of system power testing and validation, as shown in Figure 1. A description of these tests and the results can be found in the *Design Validation and Test Results* section within this document.

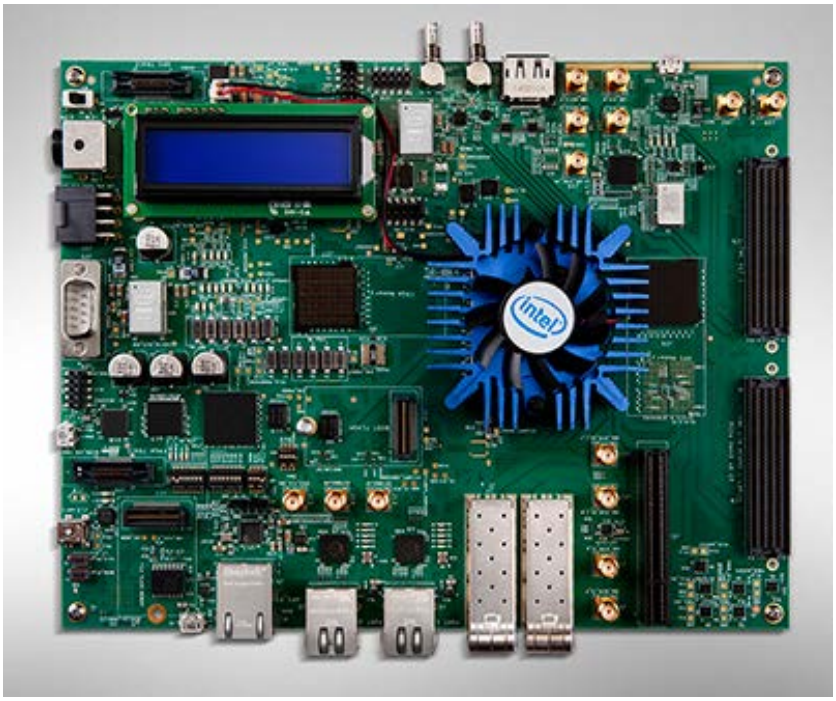

Figure 1: Reference Design Implemented In Hardware

1.1 Design Performance Highlights

- Achieves ±8.7 mV steady-state Arria 10 V_{CC} accuracy, exceeding the specification†
- Achieves <±2% Arria 10 V_{CC} deviation during load transient, exceeding the specification†

† Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks. Performance comparison methodology and detailed results documented the *Design Validation and Test Results* section of this document.

1.2 Additional Resources

Table 1: Additional Resources

Resource	Description
Reference Design Overview	Web page for this reference design, including: ▪ Reference Design Schematics ▪ Reference Design Overview
Intel® Enpirion® Power Solutions	Additional information about Intel Enpirion Power Solution products, including devices recommended for powering Arria 10 FPGAs and SoCs
Intel® Arria® 10 FPGA Support	Complete set of Arria 10 FPGA design resources, including: ▪ Arria 10 Datasheet ▪ Arria 10 Pin Connection Guidelines ▪ Arria 10 Handbook: Power Management in Arria 10 Devices ▪ Power Sequencing Guidelines
Intel Arria 10 SoC Support	Complete set of Arria 10 SoC design resources, including: ▪ Arria 10 Datasheet ▪ Arria 10 Pin Connection Guidelines ▪ Arria 10 Handbook: Power Management in Arria 10 Devices ▪ Power Sequencing Guidelines
Early Power Estimator	Tool that enables designers to estimate power consumption of their unique FPGA or SoC design
Intel Arria 10 Power Distribution Network Tool	Tool that enables designers to quickly and accurately determine the right number of decoupling capacitors to use in their unique FPGA or SoC design for optimal cost and performance trade-offs

2. System Overview

2.1 Design Component Blocks

This reference design is an upgraded variant of the complete power solution for Intel's Arria 10 SoC Development Kit, which includes both Intel Arria 10 SoC power rails as well as power rails for several peripherals. It utilizes highly integrated PowerSoC power management devices from the Intel Enpirion Power Solutions line of products. The complete power solution is designed to enable support for several component blocks, including:

- Arria 10 FPGA or SoC
- Intel Enpirion Power Solutions power management devices (see *Power Solution Block Diagram* section)
- FPGA configuration circuitry
  - Active Serial (AS) x1 or x4 configuration (EPCQ1024L)
  - MAX® V CPLD (5M2210ZF256) in a 256-pin FBGA package as the system controller
  - MAX V CPLD (5M2210ZF256) in a 256-pin FBGA package as the I/O multiplier CPLD
- Clocking circuitry
  - Programmable oscillator
  - Clock cleaner
  - 100 MHz clock generator for PCIe interface
  - 148.5 MHz voltage control oscillator for SDI interface
- Memory interfaces
  - HPS memory size (HILO card):
    - 2GB DDR3 (256Mb x 40 x dual rank)
    - 1GB DDR3 (256Mb x 40 x single rank)
    - 1GB DDR4 (256Mb x 40 x single rank)
  - FPGA memory size (HILO Card):
    - 4GB DDR3 (256Mb x72 x dual rank)
    - 2GB DDR3 (256Mb x72 x single rank)
    - 2GB DDR4 (256Mb x 72 x single rank)
    - 16MB QDRV (4Mb x 36)
    - 128MB RLDRAM3(16Mb x 72)
  - HPS Boot Flash (Flash card):
    - NAND flash (x8) : 128MB
    - QSPI flash: 128MB
    - SD Micro flash card: 4GB
  - Optional FPGA File Flash (Flash card):

        - NAND flash (x8): 128MB
        - QSPI flash: 128MB
        - SD Micro flash card: 4GB
- Communication ports
    - HPS Communication ports:
        - USB 2.0 port
        - RGMII 10/100/1000 Ethernet port
        - USB-UART port
        - DB-9 RS-232 Port
        - I2C port (I2C1 of shared I/O bit 12 and 13)
    - FPGA I/O connections:
        - FPGA V57.1 High Pin Count FMC slot
        - FPGA Intel Low Pin Count FMC slot
        - FMC_PCIe Gen2 x8 EP cable
        - FPGA PCIe GEN1/2/3 x8 RC slot
    - FPGA Communication ports:
        - 2x SGMII Gigabit Ethernet ports
        - 2x 10Gb/s SFP+ ports
        - Display port (DP)
        - SDI/SDO video port
        - SPI port
        - UART port
    - FPGA Debug ports:
        - 16-bit Trace port (FPGA Trace)
- General user I/O, including LEDs and displays

2.2 Power Solution Block Diagram

Figure 2 shows the full power tree for this reference design, including power rails required for and Intel Arria 10 FPGA or SoC as well as power rails required for various peripherals. Figure 3 shows a simplified power tree for the Arria 10 power rails only. The testing and validation for this design focused on the critical Arria 10 V_{CC} core voltage rail, which is powered by an EM2130L01QI 30A digital PowerSoC from the Intel Enpirion Power Solutions family of products.

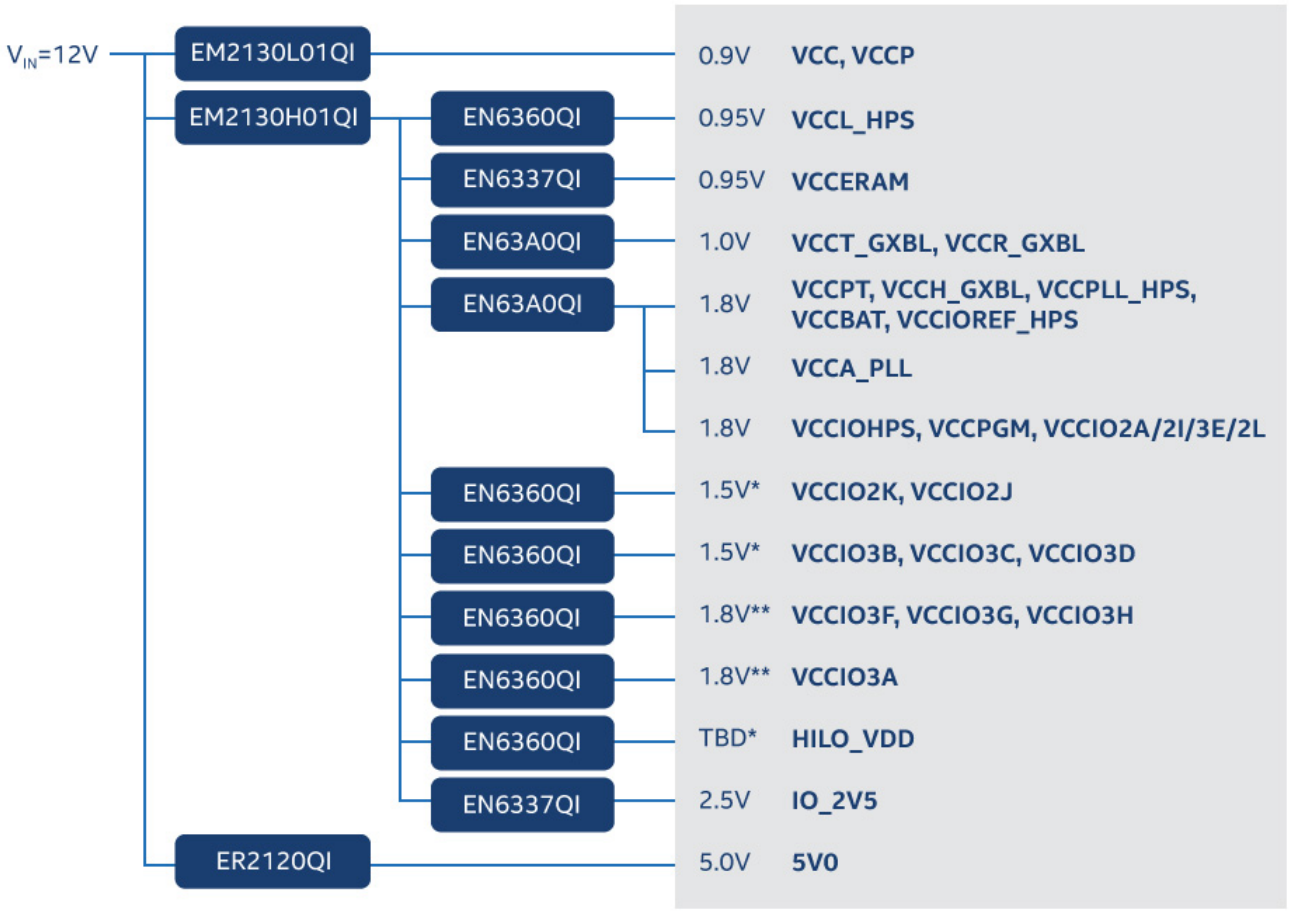

Figure 2: Full Reference Design Power Tree

NOTE: **Variable voltage: 1.2V, 1.25V, 1.3V, 1.35V, 1.5V, or 1.8V*

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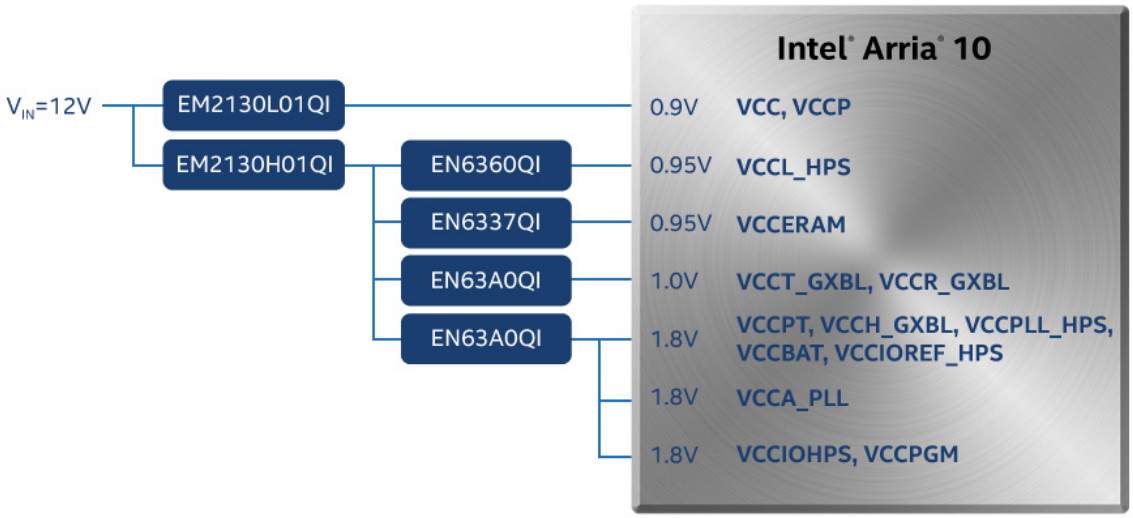


Figure 3: Simplified Reference Design Power Tree - Arria 10 Power Supply Only

This reference design follows Intel's Arria 10 power rail recommendations as found in the following resources:

- Arria 10 Pin Connection Guidelines: provides an overview of each pin, including power input pins, and how that pin should be connected in hardware; provides guidance and recommendations for power rail sharing.
- Application Note AN692: describes how Arria 10 power rails should be sequenced during power-up and power-down.

2.3 Highlighted Products

Intel® Arria® 10 FPGAs and SoCs

Intel Arria 10 FPGAs and SoCs deliver high performance at 20 nm. Arria 10 FPGAs and SoCs integrate a number of features including a suite of power reduction features, 25.78 Gbps transceivers, hard floating-point DSP, variants with integrated 1.5 GHz dual-core CPUs, and more.

For more information about Intel Arria 10 FPGAs and SoCs, please visit www.altera.com/arria10 and https://www.altera.com/products/soc/overview.html.

Intel® Enpirion® Power Solutions

Intel Enpirion Power Solutions provide high-efficiency power management for FPGAs and SoCs and complementary peripherals. These robust, easy-to-use products meet the most stringent power requirements—all in a small footprint.

Intel Enpirion power system-on-chip (PowerSoC) products combine advanced technologies—such as high-frequency silicon design, digital communication and control, magnetics, and packaging—into a turnkey product. Unlike discrete power products, PowerSoCs give designers complete power systems that are fully simulated, characterized, and production qualified.

Together, Intel FPGAs and Enpirion power products deliver an optimal system solution that has:

- High system efficiency with lower power consumption and less heat.
- High integration in a small footprint for maximum power density and a faster, lower risk design cycle.
- Low component count and high reliability.

Additionally, Intel Enpirion products are fully validated, improving end system time to market and minimizing board spins.

Table 2 lists the Intel Enpirion devices used in this design.

Table 2: Featured Intel Enpirion Power Solutions

Device	Output Current
EM2130x01QI	30A
EN63A0QI	12A
EN6360QI	8A
EN6337QI	3A
ER2120QI	2A

3. Design Validation and Test Results

3.1 Test Methodology

Intel's Low Power Voltage Regulator Test Tool (LPVRTT) was used to execute the power performance testing included in this section. This tool enables comprehensive yet fast system power testing. The LPVRTT connects to the Arria 10 FPGA or SoC footprint and emulates a wide range of load conditions across the frequency domain while measuring various power parameters like transient response. The LPVRTT is shown in Figure 4.

The power performance testing was focused on the Arria 10 SoC V_{CC} power rail. This design recommends Intel's EM2130L01QI for supplying this rail, and is designed to support V_{CC} loads up to 30A. The EM2130 is a digital 30A PowerSoC designed to simplify the complex task of building high performance FPGA systems. It features an efficient and power dense footprint, a digital control architecture, and a PMBus™ compliant digital control interface. The EM2130 is footprint compatible with the EM2120x01QI 20A digital PowerSoC and the EM2140P01QI 40A digital PowerSoC, which enables this reference design to be scalable across a wide range of Arria 10 designs. The EM2130L01QI is ideal for powering the V_{CC} power rail as it features 0.5% set-point accuracy with extremely low output ripple, and a fast transient response with minimal bulk capacitance – all of which enables users to easily meet the V_{CC} steady-state and dynamic power requirements.

This design was validated with the following test equipment:

- 30W core Arria 10 reference design demonstration board, shown in Figure 1
- Intel Voltage Low Power Voltage Regulator Test Tool (LPVRTT) and graphical user interface
- Tektronix* MSO 5204B oscilloscope
- FLIR ONE* thermal imaging camera

Figure 4: Low Power Voltage Regulator Test Tool (LPVRTT)

3.2 Performance Summary

3.2.1 Meeting Arria 10 Steady-State Power Requirements

The steady-state core voltage power supply (V_{CC}) requirement for Arria 10 is described in Table 3, which is referenced from the Arria 10 datasheet. In this table, the Minimum, Typical, and Maximum values describe only the budget for the DC (steady-state) power supply tolerance and does not include the dynamic tolerance requirements.

Table 3: Arria 10 Recommended Operating Conditions, V_{CC} Power Supply

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
VCC	Core voltage power supply	Standard and low power[1]	0.87	0.9	0.93	V

1. *This table shows only the specification for -1, -2, and -3 grade devices operated at 0.9V. See the Arria 10 Datasheet for the latest information and full table of recommended operating conditions.*

This means that the power supply for the V_{CC} core power rail must maintain a V_{CC} voltage within ±30 mV. The overall static accuracy of a power supply is the combined output voltage accuracy and output voltage ripple.

To determine how this design's static performance compares to the Arria 10 requirement, we summed the device accuracy, which is guaranteed by device production test, and the device output ripple, which is measured on the design hardware.

As found in the EM2130L01QI datasheet, the EM2130 achieves ±0.5% set-point accuracy for 0˚C < $T_{ambient}$ < 85˚C.

The EM2130L01QI ripple was measured using a Tektronix* MSO 5204B oscilloscope. The measurement was taken with 250 MHz bandwidth at the Arria 10 V_{CC} input pin location using 1 MΩ termination and AC coupling.

As shown in Figure 5, in this design the EM2130L01QI achieves 8.4 mV peak-to-peak ripple at full 30A load.

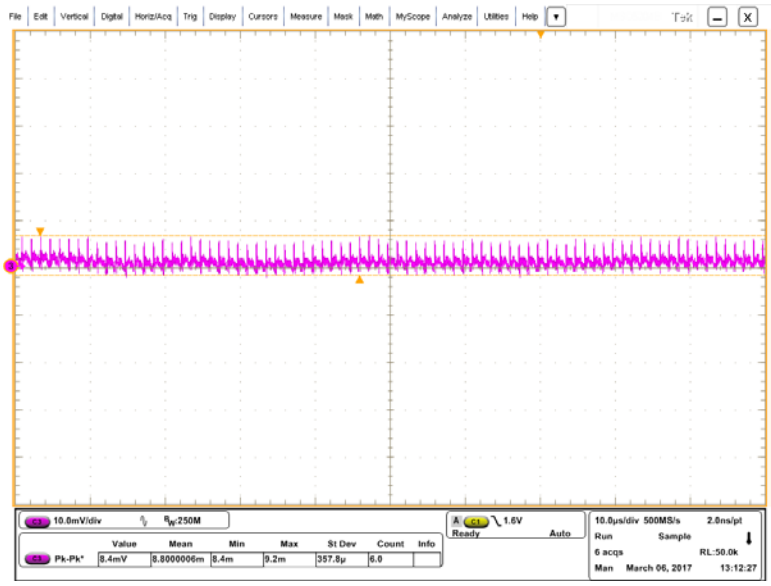


Figure 5: Measured V_{CC} Supply Ripple

In this design, the EM2130L01QI powering the Arria 10 V_{CC} rail is set to regulate to 0.9V from an input voltage of 12V. With 0.5% set-point accuracy and 8.4 mV peak-to-peak ripple (±4.2 mV), the actual V_{CC} rail voltage will fall between 0.9V ± 8.7 mV, where the accuracy variance is ±4.5 mV and the ripple variance is ±4.2 mV. This design therefore far exceeds the Arria 10 steady-state requirement that the V_{CC} rail be regulated within ±30 mV, providing over 20 mV of headroom in ensuring that the V_{CC} steady-state power specification is met for seamless Arria 10 FPGA or SoC operation.

Figure 6 provides a conceptual overview comparing the EM2130L01QI's steady-state accuracy performance versus the Arria 10 requirements. Figure 6a shows the Arria 10 V_{CC} rail total steady-state accuracy requirements; the power supply must maintain steady-state regulation of V_{CC} to 0.9V ± 30 mV. Figure 6b shows that the EM2130L01QI will regulate to V_{CC} = 0.9V with

±8.7 mV, including the combined steady-state variance due to device accuracy and output ripple.

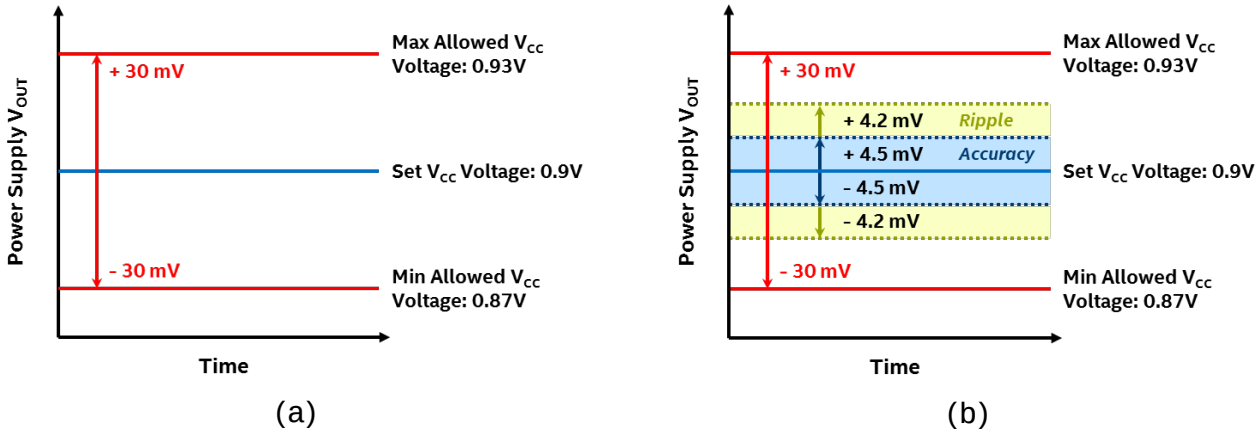


Figure 6: Comparing EM2130L01QI Static Accuracy Versus Arria 10 Requirement

3.2.2 Meeting Arria 10 Dynamic (Transient) Power Requirements

The dynamic core voltage power supply (V_{CC}) requirement for Arria 10 is found in "Recommended settings for Arria® 10 device power rails" table, located within the Arria 10 Power Distribution Network (PDN) Tool under the "Information" tab, as shown in Figure 7. This table shows the maximum allowed percentage voltage deviation, called "Noise Tolerance," during a dynamic percentage current change, or load step. As an example, a 0.9V V_{CC} core voltage rail is allowed to overshoot or undershoot by up to 45 mV when there is a 50% load step.

Recommended settings for Arria® 10 device power rails

Rail Name	Default voltage (V)	Noise Tolerance (%)	Dynamic Current Change (%)	Description
VCC	0.9 / 0.95	5	50	Core
VCCIO	1.2 - 3.0	5	100	I/O Bank
VCCPT	1.8	5	50	I/O Pre-drivers
VCCPGM	1.2 / 1.5 / 1.8	5	50	Programming Power
VCCERAM	0.9 / 0.95	5	50	Programmable Power Tech Aux
VCCBAT	1.2 / 1.5 / 1.8	5	100	Battery Back-up Power Supply
VCCA_PLL	1.8	5	10	PLL (Analog)
VCCR_GXB	0.95 / 1.03 / 1.12	3	30	Transceiver RX (Analog)
VCCT_GXB	0.95 / 1.03 / 1.12	2	60	Transceiver TX (Analog)
VCCH_GXB	1.8	3	15	Transceiver I/O Buffer Block
VCCP	0.9 / 0.95	5	33	Periphery Supply Voltage
VCCL_HPS	0.9 / 0.95	5	60	HPS Core
VCCIO_HPS	1.8 / 2.5 / 3.0	5	100	HPS I/O Bank
VCCIOREF_HPS	1.8	5	50	HPS I/O Pre-drivers
VCCPLL_HPS	1.8	5	10	HPS PLL (analog)

*Refer to **Arria 10 Device Handbook** and **Arria 10 Device Family Pin Connection Guidelines** for detailed description of power rail functions and default voltages.*

Figure 7. Arria 10 Allowed Voltage Deviation During Load Transient

This design recommends a EM2130L01QI to supply the VCC voltage, and is designed to support V_{CC} loads up to 30A. The LPVRTT was used to measure the EM2130L01QI's performance during a 15A (50%) load step. Figure 8 shows the test conditions and results, which are displayed within within the LPVRTT graphical user interface. The EM2130L01QI achieves a deviation of 35 mV_{P-P}, which translates to approximately ±17.5 mV or ±1.94% - far exceeding the maximum allowed deviation of ±5%.

Figure 8: V_{CC} Transient Response and Ripple During 15A (50%) Load Step

3.2.3 Thermal Performance

A FLIR ONE* thermal imaging camera was used to photograph the EM2130L01QI powering the Arria 10 V_{CC} rail. After running for 20 minutes at full 30A load with minimal airflow, the board temperature was measured at approximately 44°C and the EM2130L01QI internal temperature was measured at 50°C using the device's integrated PMBus interface and telemetry capabilities. Figure 9 shows the thermal image.

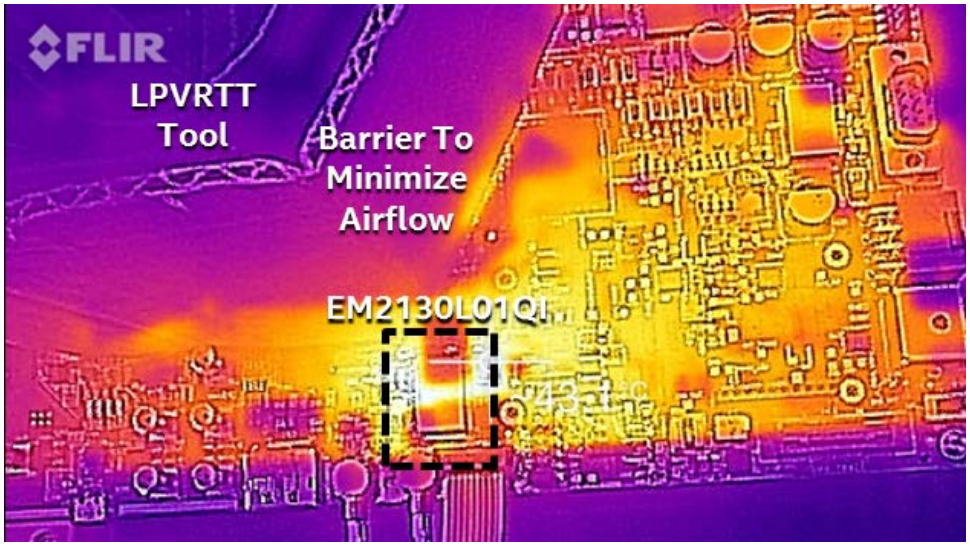
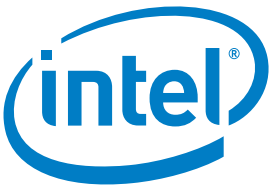


Figure 9: Thermal Image Of EM2130L01QI At Full 30A Load For 20 Minutes



4. Revision History

Revision Number	Description	Revision Date
001	Initial release.	March 2017