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## Low-Cost FPGA Solution for PCI Express Implementation

### Introduction

PCI Express is rapidly establishing itself as the successor to PCI, providing higher performance, increased flexibility, and scalability for next-generation systems, as well as maintaining software compatibility with existing PCI applications. As PCI Express becomes the standard interconnect for leading-edge embedded applications, system designers must address the challenges associated with the usability of this new protocol. Altera and Texas Instruments (TI) offer an easy to use PCI Express solution for the low-cost market segment.

### Low-Cost PCI Express Solution

A high-volume, low-cost PCI Express x1 end-point solution can be easily designed today with the following features:

- Altera® low-cost Cyclone™ II FPGA
- Altera PCI Express Compiler x1 MegaCore® function with free evaluation
- TI low-cost x1 PCI Express XIO1100 physical layer (PHY) using the Physical Interface for PCI Express (PIPE) interface

Cyclone II FPGAs are interoperable with many different PHYs. However, to ensure that Altera has the easiest-to-use, lowest-cost solution in the market, Altera has collaborated closely with TI, a leader in PCI Express technology. This paper illustrates how the Altera/TI PCI Express solution can displace costly, high-risk devices such as ASICs, and offers the most flexible, easiest-to-use, lowest-cost solutions in the market.

#### *Altera Cyclone II FPGAs*

Altera Cyclone II devices extend the reach of FPGAs further into cost-sensitive, high-volume applications. These devices are built on TSMC's highly successful 90-nm process technology using 300-mm wafers and offer higher densities, more features, higher performance, and lower power consumption than competing 90-nm FPGAs. Cyclone II FPGAs are supported by free Quartus® II Web Edition software.

#### *Altera PCI Express Compiler x1 MegaCore Function*

Altera PCI Express x1 MegaCore functions can be used to design PCI Express endpoint applications, including non-transparent bridges, or truly unique designs combining multiple PCI Express components in a single Altera device. The PCI Express x1 MegaCore function is PCI Express Base Specification Revision 1.0a-compliant, and implements all required, and most optional, features of the specification for the transaction, data link, and media access controller (MAC) sublayers.

PCI Express x1 MegaCore functions support all memory, I/O, configuration, and message transactions. The x1 MegaCore functions have a highly optimized application interface to achieve maximum effective throughput. Because the x1 MegaCore function is parameterized, it can be customized to meet design requirements using IP Toolbench. Additionally, the MegaCore function supports end-to-end cyclic redundancy code (ECRC) and advanced error reporting for x1 lanes for systems requiring high reliability.

#### *TI External PCI Express Transceiver/PHY*

The XIO1100 PHY from TI is based on third-generation PHY technology and is a fully compliant x1 PCI Express physical-layer transceiver device. It supports an x1 link at 2.5 Gbps each way and consumes less than 250 mW of power. It also supports both the 8 bit and 16-bit PIPE interface standard, which is supported by leading digital IP vendors in the industry. The designer has a choice of clocking SDR or DDR on a 125-MHz clock. The XIO1100 PHY is available in a small-footprint, low-cost BGA package.

## Implementing PCI Express Using Cyclone II FPGAs and External TI XIO1100 x1 PHY

The PCI Express data link layer, transaction layer and MAC sub-layer can be implemented in the Cyclone II FPGA using the configurable Altera PCI Express x1 MegaCore, whereas the physical coding sub-layer (PCS) and physical media attachment (PMA) sub-layer are implemented using the external TI x1 PCI Express XIO1100 PHY.

The PCI Express physical layer is broken down into the MAC, PCS, and PMA sub-layers. The PMA sub-layer specifies analog domain of the physical interface. The PCS sub-layer provides 8b/10b encoding in the transmit direction and decoding in the receive direction, as well as elastic buffers for rate matching. Figure 1 shows the implementation of PCI Express using Cyclone II FPGAs and external TI x1 PHY.

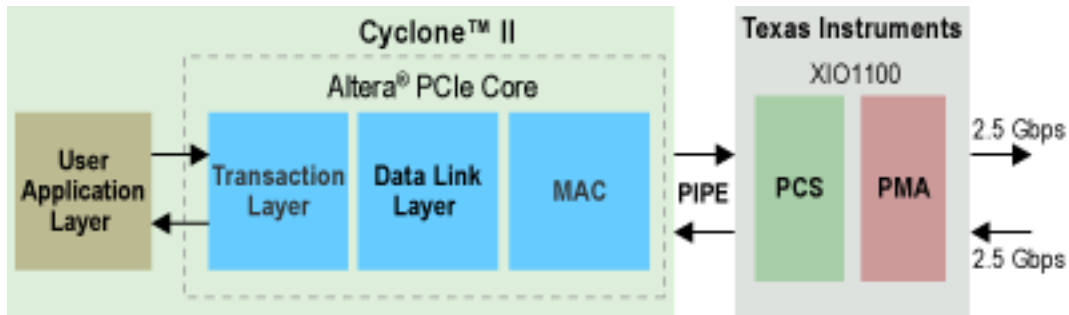


Figure 1. Implementing PCI Express Using Cyclone II and External TI x1 PHY

The MAC sub-layer controls the physical interface with state machines for link training and initialization, including polarity inversion, signal rate negotiation and bit lock, symbol detection, link width negotiation, and for multilane links, lane reversal, and lane-to-lane de-skew. The PIPE, a logical interface between the PCS and MAC sub-layers, connects the PCI Express PHY and the PCI Express MAC layer to a PCI Express serial link.

TI's XIO1100 is a PCI Express PHY that interfaces the PCI Express MAC layer to a PCI Express serial link. It uses a PIPE-based interface called TI-PIPE that includes a source-synchronous clock to simplify board layout. TXCLK/RXCLK travels in parallel with the data. In this way, the clock suffers the same delay and drift as the data, enabling the data to be reliably clocked into the receiving device. TI-PIPE also allows an 8- or 16-bit pin-configurable interface.

The x1 PHY interfaces to a 2.5-Gbps PCI Express serial link with a transmit differential pair and a receive differential pair. The PHY is responsible for handling the 8b/10b encoding/decoding and scrambling/unscrambling of the outgoing data. In addition, the PHY must recover/interpolate the clock on the receiver side based on the transitions guaranteed by the 8b/10b mechanism and supply this to the receive side of the data link-layer logic.

## Benefits of Implementing PCI Express Using Low-Cost Programmable Logic With x1 External PHY

While some ASICs and ASSPs can provide fully integrated PCI Express solutions, there are several benefits of using Altera's Cyclone II FPGAs along with TI external x1 PHY to implement PCI Express. New generations of products are introduced to market more rapidly than ever before. Windows of opportunity for market success are shrinking, causing manufacturers to look for new, flexible, low-cost, and fast-development solutions. Below are some of the key benefits provided by the Altera and TI low-cost PCI Express solution.

### Rapid and Low-Cost Innovation

While ASSPs and ASICs provide a low-cost, fixed platform for PCI Express solutions, ASSPs reduce the ability to differentiate and to add the latest in-demand features, and ASICs are notorious for significantly jeopardizing on-time delivery and for their high development cost. Solely relying on ASICs and ASSPs can put the product behind those of the competition with late-to-market, "me-too" products. Additionally, many ASSPs provide fixed functionality whether the design needs it or not, and are available in more-expensive high-pin-count packages.

The cost of designing ASICs is also increasing every year. In addition to the non-recurring engineering (NRE) and mask costs, development costs are increasing due to ASIC design complexity. Moreover, issues such as power, signal integrity, clock tree synthesis, and manufacturing defects can add significant risk and time-to-market delays. To overcome the risk of respins, high NRE costs, and to reduce time-to-market delays, FPGAs offer a viable and competitive option to ASIC development.

Cyclone II FPGAs with a TI x1 PHY provide rapid, low-cost innovation cycles and greater product differentiation to increase margins; it can get the product to market first. Altera's solution is already fully tested and available now. Additionally designers must realize that not every application will require the full functionality offered by many PCI Express ASSPs. For many designs, a single x1 PCI Express port implemented in a flexible, low-cost Cyclone II FPGA interfacing to an external TI x1 transceiver (XIO1100) may be the optimal solution in terms of cost and features.

### *Differentiation*

With Altera's Cyclone II FPGAs, development efforts can be focused on implementing the features and enhancements that are critical to establishing market leadership. If an ASSP or an ASIC is already being used, it can be kept for standard, yet complex, functions, while using Altera PLDs or structured ASICs for the latest high-value features. This methodology allows the addition of differentiating features for a longer period of time and faster innovation than alternative silicon technologies.

### *Integration*

If FPGAs are already being used in a design and PCI Express functionality needs to be added, the Altera solution makes it simple to integrate PCI Express. Simply drop the MegaCore in the design and attach an x1 PHY to the existing FPGA design. Everything from the PCI Express MAC sub-layer, data link layer, transaction layer, PIPE interface, and PHY has already been defined, leaving the designer time to focus on the unique portions of their product.

The solution can also benefit from integrating other portions of the design such as signal processing operations, external memory interfaces, and clock management into the FPGA. These functions can be implemented efficiently using the available embedded resources within Altera Cyclone II FPGAs, including logic elements (LEs), multipliers, and phased locked loops (PLLs). By using programmable logic to integrate various functions including PCI Express, companies can reduce the product's cost and form factor and increase the performance of their application.

### *Reusability*

Altera FPGAs provide a programmable logic solution for a variety of PCI applications. With PCI Express rapidly establishing itself as the successor to PCI by providing higher performance, increased flexibility, and scalability for next-generation systems, it is much cheaper and easier to transition to PCI Express from PCI by using an existing FPGA. In addition, the user can maintain software compatibility with existing PCI applications.

### *Risk-Management*

The Altera/TI low-cost solution can ensure that implementations go as smoothly as possible.

### **Reprogrammability**

ASICs typically have at least a one-year development cycle. During this development time or after production, the product requirement may change due to changing standards, consumer demand, etc. leaving a less than optimal product. Programmable logic solves these problems. Users can reduce risk with a PLD as they can always modify the design even after production.

Altera's Cyclone II FPGAs are ideal for developing PCI Express products at a fraction of the development cost and time of traditional technologies. Whether a concept product is being developed by adding enhancements to older ASSPs or ASICs, or a new, highly complex function is being developed from scratch, Altera has the right solution. Because Altera products are reprogrammable, costly and time-consuming silicon respins for ASIC design changes

and long and uncertain waiting periods for new versions of ASSPs can be eliminated. Altera solutions save time and money, and enable leading-edge designs.

### PCI SIG Compliance

To ensure the highest reliability, Altera's PCI Express solutions are fully tested in hardware at PCI-SIG-sponsored PCI Express compliance workshops. This means that designers can consider the PCI Express portion of their design fully completed and tested. This is especially important in open-ended PCI Express endpoints where the product needs to work with various unknown system manufacturers.

### Support for New Protocol Standards

It is very hard to keep up with the ever-evolving protocol standards. Changing a design in an ASIC because of a specification change can be very expensive and result in late-to-market products lagging behind the competition. To overcome the risk of respins, high NRE costs, and to reduce time-to-market delays, FPGAs offer a flexible and competitive option.

### Obsolescence Proof

Cyclone II FPGAs and XIO1100 PCI Express PHYs are standard off-the-shelf parts that will be in production for many years, ensuring that the product will not have an abrupt end due to supplier problems.

### Applications

FPGAs with external x1 PCI Express PHY solutions meet the needs of several low-cost applications in consumer, storage, industrial, and communications end markets. Some examples of the end applications are:

- TV tuners, 1394a/b controllers, and general purpose I/O
- Industrial control data acquisition products
- Video capture cards
- High-performance I/O infrastructure for desktop applications

An example of an application that uses an FPGA and an external x1 PCI Express PHY is bridging to Gigabit Ethernet or a chassis-to-chassis connection within larger equipment. With 2.5-Gbps maximum throughput, customers can use this for control data purposes, replacing PCI 32/33 and 64/33 implementations. This solution also enables makers of PCs and I/O add-on cards to begin the transition to native PCI Express technology while preserving compatibility with existing PCI system software and firmware.

### Conclusion

The Cyclone II FPGA, used in conjunction with a TI XIO1100 x1 PCI Express PHY and Altera PCI Express x1 MegaCore, provides a low-cost, flexible, low-power, and fully PCI Express specifications-compliant solution.

### Further Information

- More information on Altera Cyclone II FPGAs:  
<http://www.altera.com/products/devices/cyclone2/cy2-index.jsp>
- More information on TI x1 PCI Express Physical Layer transceiver (XIO1100):  
<http://focus.ti.com/lit/ml/sllb100/sllb100.pdf>
- Download the free Quartus II Web Edition software supporting all Cyclone II FPGA devices:  
[https://www.altera.com/support/software/download/altera\\_design/quartus\\_we/dnl-quartus\\_we.jsp](https://www.altera.com/support/software/download/altera_design/quartus_we/dnl-quartus_we.jsp)
- Download a free evaluation version of the Altera PCI Express Compiler x1 MegaCore function:  
<http://www.altera.com/products/ip/iup/pci-express/m-alt-pcie8.html>
- PCI Express Base Specification Revision 1.0a:  
<http://www.pcisig.com/specifications/pciexpress/base>
- Cyclone II PCI Express Development Kit:  
A complete Cyclone II PCI Express Development Kit will be available in Q2 2006, including a Cyclone II EP2C35 FPGA, Texas Instruments XIO1100 PHY, and complete reference design.



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