White Paper

The Quest for Digital Broadcast Quality: Addressing Quality Hot Spots

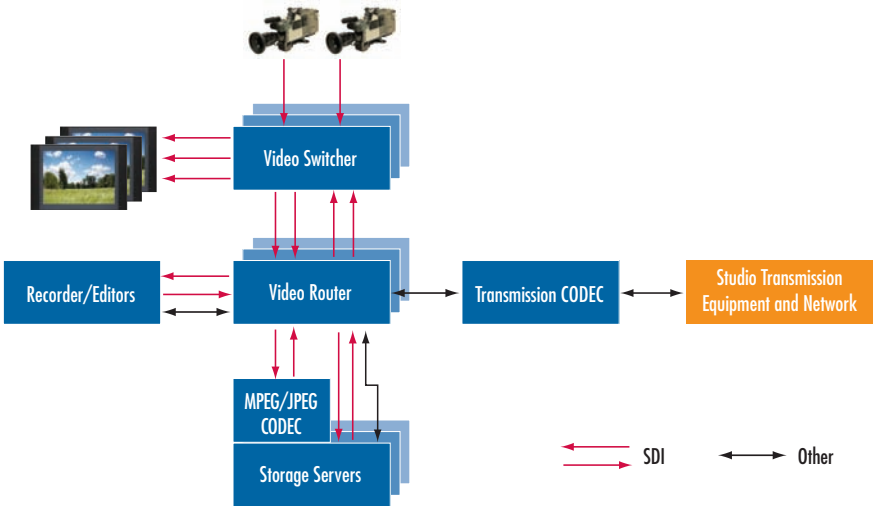
Introduction

Digital signal processing within digital televisions (DTVs) has advanced significantly, resulting in improved picture and audio quality. Further improvements in DTV technology over the next several years will continue to enhance the quality, but the largest gains in the HD video experience will be achieved by improving the A/V source received by the DTV. The video source, for example, is a highly degraded version of the original source captured in the studio. Improvements in the studio and broadcast infrastructure represent the greatest upsides for future quality improvements. This white paper examines the quality "hot spots" (degradation points) HDTV may suffer, from the time it is captured to the moment it is experienced by the consumer, and discusses ways of preserving and improving the quality within existing distribution bandwidth restrictions.

Enabling 1080p in the Studio for Full HD Quality

A DTV video studio environment contains various equipment, including video switchers and routers, storage servers, professional-grade cameras, and monitors, as well as recording, editing, encoding, and decoding equipment. The video switcher creates the video stream that is broadcast through television distribution channels, mixing live video from multiple cameras as well as prerecorded video from the storage servers, video tape or digital recorders (VTRs or VDRs), and editors to create a fluid video program (see Figure 1). Video switchers also feed studio monitors directly, allowing the user, most often a producer, to see the input and output video from the switchers. Video data is typically compressed and decompressed with MPEG or JPEG compression algorithms for storage or transmission to the end viewers.

Figure 1. Typical Studio Connectivity



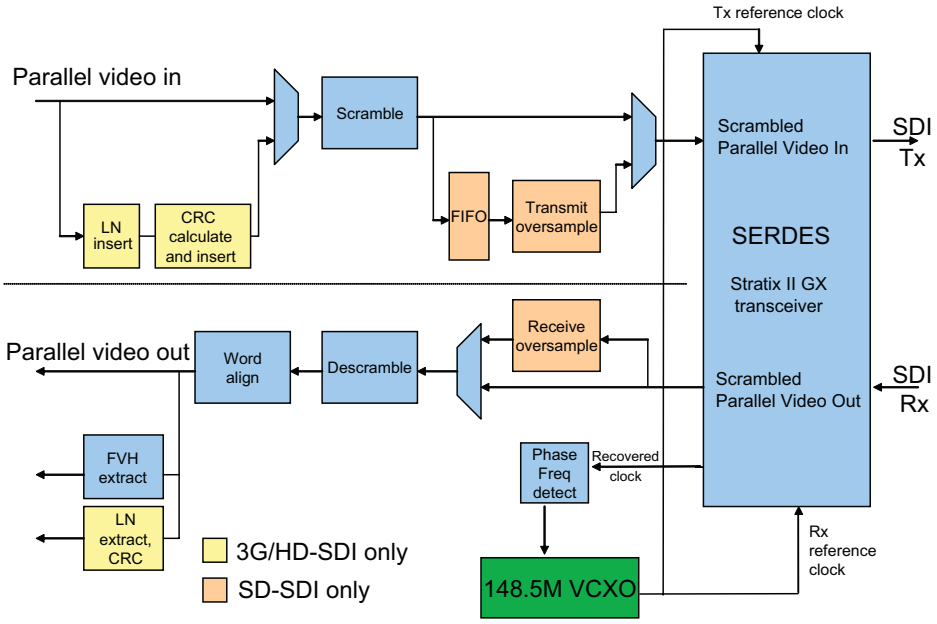
Today's high-definition (HD) video studio environment must support a network of equipment operating at HD data-transfer rates. Production studios use coaxial cable to transport SMPTE259M (SDI) and SMPTE292M (HD-SDI) video and embedded audio between equipment. HD-SDI interfaces support data rates of up to 1.485 Gbps and are sufficient to handle HD resolutions associated with 1080I and 720p. However, the need for the higher quality full-HD video, enabled by 1080p, has increased bandwidth requirements.

Enabling 1080p, apart from improving the picture quality, has other benefits in video production studios. It is the highest level of resolution the standards enable and is free of the complexity and motion errors associated with interlace formats. Since both 720p and 1080I formats are popular in North America and Europe, and likely to coexist for the foreseeable future, this creates a dilemma for studios as to which format to use during production.

If the studios were to use 1080p during production, it would be easier to convert to 1080I or 720p without loss of quality. Fortunately, SMPTE recently ratified new 1080p standards that open up the bandwidth bottleneck of the SDI cabling used in studios. New SMPTE standards 424M (which defines the bit serial data format and the PHY characteristics of a 3-Gbps SDI link) and 425M (which defines the mapping of various formats for transmitting over SDI video on 3-Gbps link) leverage core technology improvements of FPGAs and PHY interface chips to double the SDI cable bandwidth from 1.485 Gbps to 2.97 Gbps, sufficient to support full 1080p serial video transport on a single link.

To enable fast development and deployment of highly flexible next-generation switchers, cameras, servers, and other studio equipment supporting 1080p, Altera provides a hardware-tested SDI MegaCore® function that implements triple-rate SD-SDI, HD-SDI, and 3G-SDI (see Figure 2). The MegaCore function automatically detects and switches between SD-, HD-, and 3G-SDI depending on the type of video data received. It also captures and/or transmits standard-definition (SD) video, 720p HD, 1080i HD, or 1080p HD. Only a single 148.5-MHz voltage-controlled crystal oscillator (VCXO) is needed for these SDI rates.

Figure 2. Altera's Triple-Rate SDI MegaCore Block Diagram



The SDI MegaCore function includes all the required receive and transmit building blocks for the key data rates of 270 Mbps, 1.485 Gbps, and 2.970 Gbps. The receive block has a cyclic redundancy check (CRC) decoder, a line-number extraction, video framing and timing extraction, and format detector. The transmit block is comprised of a CRC encoder and line number insertion. The legacy SD-SDI block includes a word scrambler for the transmitting side and a word alignment with descrambling for the receiving side.

Stratix® II GX FPGAs can support the triple-rate SDI data speeds on up to 20 full-duplex transceiver channels. Arria™ GX FPGAs—the low-cost transceiver family—can support the triple-rate speeds on up to 12 full-duplex transceiver channels. The transceiver circuitry on the Stratix II GX and Arria GX FPGAs integrates hard-coded clock/data recovery (CDR) and serializer/deserializer (SERDES) functions. To eliminate clock-to-data skew, the CDR circuit on the FPGA uses an external reference clock to train its voltage-controlled oscillator (VCO) loop to recover a clock that is both phase and frequency aligned with incoming data. SDI characterization of Stratix II GX devices shows that the devices have wide margins to receive and transmit jitter specifications. (A characterization report is available to qualified customers.) Altera also offers an A/V development kit based on the Stratix GX II FPGA family, which directly supports 1080p SDI interfacing.

1080p Video Processing

Once you have captured 1080p video, it must be processed in an uncompressed domain with a framework capable of supporting the bandwidth and performance requirements. Typical processing functions include scaling, de-interlacing, chroma resampling, color space conversion, and mixing. A studio system commonly involves most of these functions stitched together along with high-speed memory interfaces. System designers use third-party IP along with their "secret sauce" to build such systems. However, to develop such high-performance systems rapidly, a framework is needed that has readily available functions with standard interfaces, as well as a means for designers to drop their own or third-party IP into the design. Such a framework would make the integration of these functions fast and efficient.

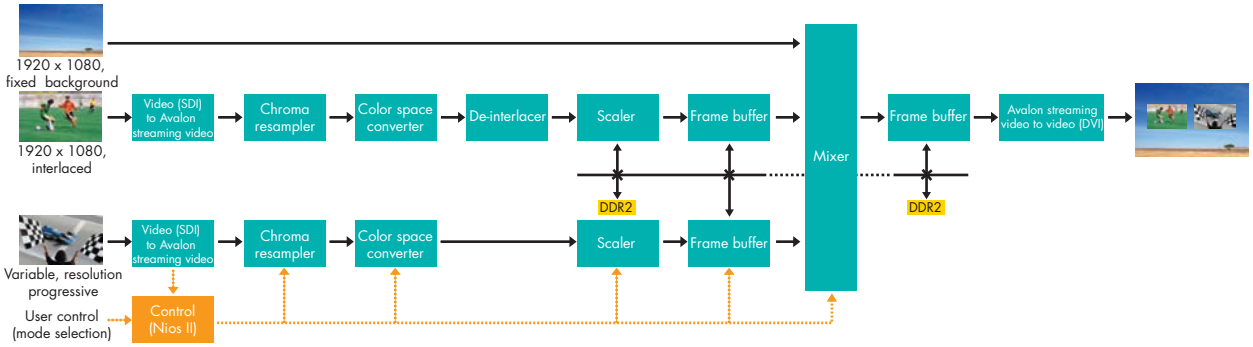
Altera provides such a framework, which includes a library of functions listed in Table 1. These functions can be configured and parametrized to handle full HD (1080p) data rates. The functions are also SOPC Builder-ready and use the common interface known as Avalon® streaming video, making it easy for them to talk to each other. SOPC Builder makes it easy for the designer to integrate the different components into their system. Altera also provides 1080p reference designs for broadcast application which can act as a starting points for the designers. Altera's Stratix III FPGAs, which have 330K LEs, 768 DSP blocks and up to 16 Mbits of internal RAM, are ideal platforms for video and image processing. Stratix III FPGAs also support external DDR2 and DDR3 memory at 533+ MHz.

Table 1. Video and Image Processing Suite IP MegaCore Functions

IP MegaCores Function	Description
Color Space Converter	Converts image data between a variety of different color spaces such as RGB to YCrCb
Chroma Resampler	Changes the sampling rate of the chroma data for image frames, for example from 4:2:2 to 4:4:4 or 4:2:2 to 4:2:0
Gamma Corrector	Performs gamma correction on a color space to compensate for the non-linear characteristics of display monitors
2D FIR Filter	Implements a 3 x 3, 5 x 5, or 7 x 7 finite impulse response (FIR) filter on an image data stream to smooth or sharpen images
2D Median Filter	Implements a 3 x 3, 5 x 5, or 7 x 7 filter that removes noise in an image by replacing each pixel value with the median of neighboring pixel values
Alpha Blending Mixer	Mixes and blends multiple image streams-useful for implementing text overlay and picture-in-picture mixing
Scaler	Resizes image frames using bilinear, bicubic, and custom polyphase algorithms. Also supports real-time updates of both the image sizes and the scaling coefficients
De-Interlacer	Converts interlaced video formats to progressive video format
Line Buffer Compiler	Efficiently maps image line buffers to Altera on-chip memory

Figure 3, an example reference design from Altera, shows a two-channel compile time parametrizable video processing system capable of capturing and processing 1080p video. Channel one accepts interlaced video using an SDI interface and converts it to progressive video. The second channel accepts progressive video of any resolution. The two inputs are mixed, scaled, and output on a DVI interface at 1080p resolution.

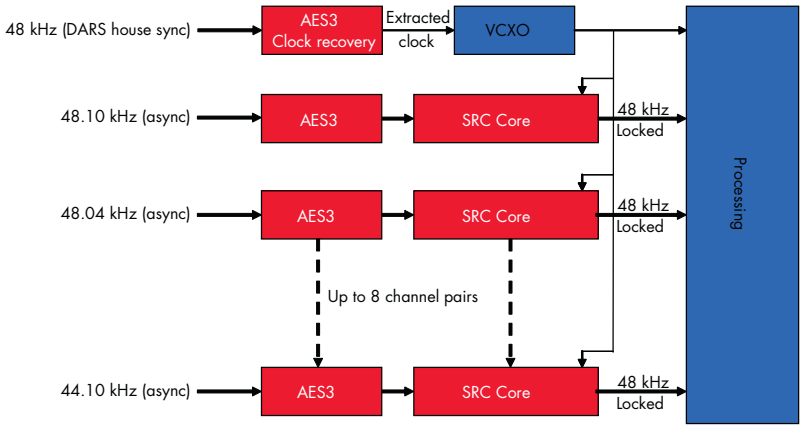
Figure 3. 1080p Video Reference Design



High-Quality Multi-Channel Audio SRC

Re-sampling audio from multiple sources with different native rates to create a single synchronized program stream is a common occurrence in production and post-production environments. As demonstrated in Figure 4, there is a tremendous variability in actual needs for broadcast-quality sample rate conversions (SRCs) including number of channels, frequency range of inputs, final output rate, and interface requirements.

Figure 4. System SRC Integration Example



An IP products and design services company provides the industry's most versatile and quality-focused solution for audio SRCs. This SRC solution supports input samples from 32 kHz to 96 kHz and outputs a range from 32 kHz to 192 kHz, providing superior flexibility and adaptability to the individual application needs. The SRC supports parallel PCM, AES/EBU, and I²S interface standards, plus up to eight stereo pair inputs and eight stereo pair outputs, all customized by the designer at compile time.

Raising the Bar in Video Compression Quality

Enhancing the quality of video captured or upconverted is only the first step in improving the video received by the consumer. Video compression, a video hot spot in the distribution channel, enables cost-effective distribution to head end subscription points and infrastructure. The various generations of compression standards range from MPEG to MPEG-4, with four methods for compression: discrete cosine transform (DCT), vector quantization (VQ), fractal compression, and discrete wavelet transform (DWT). Table 2 summarizes the various MPEG standards.

Table 2. Compression Standards

Standard	Data Rate	Applications
MPEG	<1.5 Mbps	VCD for CD-ROM; Level 3 is most popular for MP3 audio
MPEG-2	1.5 Mbps to 15 Mbps	DTV for cable satellite and terrestrial broadcast
MPEG-4	0.5 Mbps to 40 Mbps	Video conferencing, surveillance, and broadcasting with Part 10 for H.264

MPEG-2 compression is the most widely used standard today, and was created and adopted at a time when the future of HD was widely debated and HD content was almost nonexistent. The total capacity of cable and satellite plants were built to a simple formula: total number of expected MPEG-2-compressed SD channels x average compressed video bitrate = capacity. Without improvements in compression, every HD channel added to the lineup meant eliminating up to four SD channels.

To combat this issue, the ITU-T Video Coding Experts Group (VCEG) and the ISO/IEC Moving Picture Experts Group (MPEG) introduced the MPEG-4 Part 10 standard (also called H.264). H.264 provides high-quality video at a bitrate substantially lower than previous standards without enough of an increase in complexity to make the design impractical (i.e., excessively expensive) to implement. Current H.264 solutions are far from their potential in terms of quality of video at a set bitrate.

Because H.264 ASSP solutions usually target the consumer market, they are not expected to offer continual improvements in quality of video at a set data rate. However, these improvements are required by the broadcast market. Altera® FPGAs do offer video quality improvements, in addition to continual improvements in hardware cost through aggressive migration to new process technologies (65 nm and beyond) and architecture enhancements targeted at video applications.

Altera's Stratix II and Stratix III FPGA families are ideal platforms for H.264 implementation as they provide critical memory bandwidth. Stratix III devices offer up to 16 Mbits of internal memory (in 9K and 144K blocks) at clock rates of up to 600 MHz for a total bandwidth in excess of 25 Terabits per second. Stratix III FPGAs support external DDR2 and DDR3 memory at 533+ MHz. In addition, Altera's unique ternary adder architecture improves implementation of motion estimation, another critical function in H.264, by as much as 50 percent over other FPGA architectures.

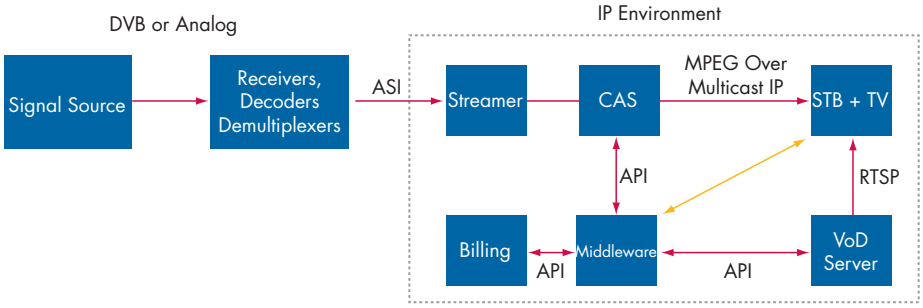
Low-Cost Video Delivery Over IP With FEC for Maximum QoS

Distribution of video through cable plants and other private networks is moving to video over Internet protocol (IP). IP networks are used continuously with growing popularity for carrying video, voice, and data in a triple-play scheme. This move requires low-cost solutions that address the quality of service (QoS) due to packet corruption over long distance and multi-channel requirements. The same IP network that was designed for non-real-time data is now tasked to handle high-speed real-time video traffic to consumers.

The Altera Video Over IP reference design implements a system that bridges MPEG transport stream (TS) data and Ethernet-based IP networks. The reference design accepts TS data from several inputs and encapsulates it for transmission over an Ethernet network.

Figure 5 shows a typical video over IP application in a real system. The design uses industry standard user datagram protocol (UDP)/IP network encapsulation, with real-time transport protocol (RTP) encapsulation and The Professional MPEG Forum's (Pro-MPEG) Code of Practice #3 (CoP3) forward error correction (FEC) available as an option. The design supports both 100-Mbps (full-duplex) and 1-Gbps Ethernet connections. By using hardware encapsulation, the design achieves line-rate gigabit Ethernet performance with minimal transmission latency. The design also accepts traffic from an Ethernet network to recover the TS data. For RTP encapsulated data, the design includes a receiver buffer to absorb network jitter and correct for packet reordering and duplication. CoP3 FEC-based lost packet recovery is available as an option.

Figure 5. Typical Video Over IP Infrastructure



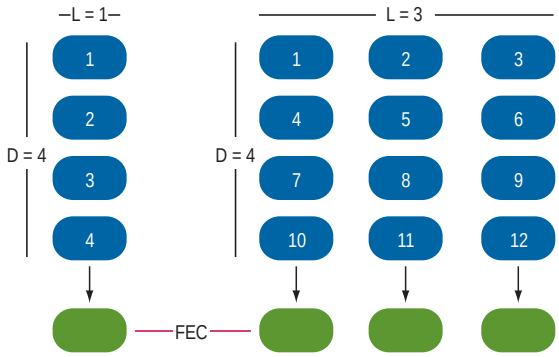
One of the methods for ensuring a minimum level of data integrity in an IP environment is to use payload-aware processing. Payload-aware processing involves IP encapsulation, timing correction, and application layer FEC. A link-level FEC is not sufficient to prevent packet loss due to burst noise from the transmission channel. However, embedding the FEC into the payload-aware device can reduce packet loss to a minimum. Altera's Video Over IP reference design demonstrates the transmission of MPEG-2 TS data over IP-based networks with Pro-MPEG CoP3 FEC.

The Pro-MPEG Wide Area Network (WAN) working group focuses on establishing interoperability practices for systems that provide an exchange of high-quality programming material over WANs using IP. This group has produced a code of practice for the transmission of MPEG-2 TS data over IP networks. This code of practice recommends the transmission protocol (for example, RTP/UDP/IP mapping) and FEC scheme, and discusses issues such as timing recovery, jitter tolerance, and latency. The recommendations for the transmission protocol have been followed in the reference design, although the use of RTP is optional to support legacy UDP/IP standards.

The Pro-MPEG FEC is a two-dimensional XOR algorithm with several possibilities as to how large the data matrix can be. This FEC dictates that there must be between 1 and 20 columns and 4 and 20 rows. Also, the total number of packets in one matrix may not exceed 100. Here is an example of this simple FEC concept: If *A* and *B* are RTP packets, then $F = A \oplus B$ is called the FEC packet associated to the $\{A, B\}$ protection set. F is the result of the XOR operator byte after byte on both RTP packets. An interesting property of the operator is that if $F = A \oplus B$, then $A = B \oplus F$ and $B = A \oplus F$. If *A* or *B* is discarded, *A* or *B* can then be recovered using the F FEC packet.

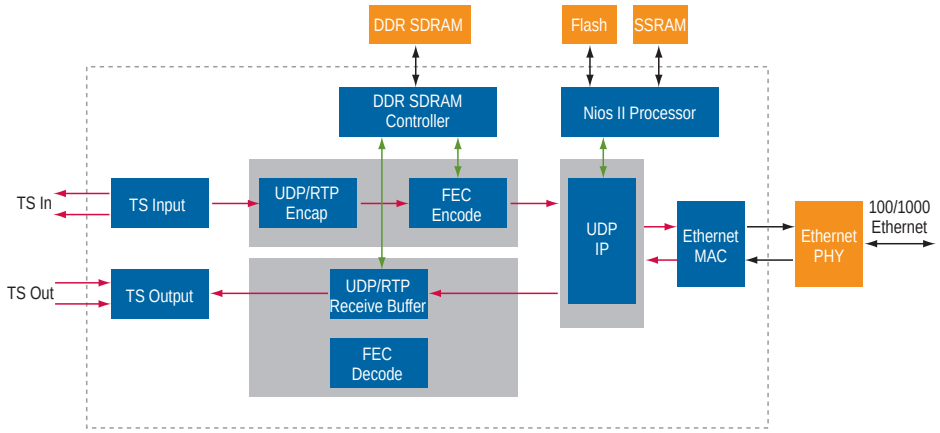
Figure 6 shows a Pro-MPEG matrix arrangement and the resulting FEC overhead data in green.

Figure 6. Matrix Arrangement Examples



Altera provides a demonstration design, which supports two data channels for TS-to-Ethernet, and two channels for Ethernet-to-TS. The demonstration uses external SDRAM for the transmitter FEC packet buffering and for the receiver payload and FEC packet buffering. A Nios® II processor allows the user to write software to control and monitor the design operation. The demonstration is mapped to the Nios II Development Kit, Cyclone II Edition, for hardware demonstration and evaluation purposes. This reference design is shown in Figure 7.

Figure 7. Complete Video Over IP Block Diagram



The 100-Mbps or 1-Gbps Ethernet with industry-standard UDP/IP or RTP/UDP/IP encapsulation performed in hardware can provide line-rate gigabit Ethernet throughput with minimal, deterministic latency and a configurable UDP/IP socket for each individual A/V stream. IP multicast is supported for broadcast applications with an optional second Ethernet port for redundant network architectures. The design also supports multiple independent streams (SPTS or MPTS), which scale efficiently from 1 to 256 individual A/V streams at a total TS bandwidth of greater than 900 Mbps.

Conclusion

The HD quality provided by today's broadcast industry to the consumer is marginal at best. As consumers gain experience and their expectations increase, it is imperative that the quality hot spots discussed in this white paper are properly addressed. Fortunately, quality improvements are now possible through the work Altera and its partners have done in full HD capture, audio rate conversion, high quality compression, video scaling, and video transport. Upgrading broadcast systems with these programmable FPGA solutions will result in improved quality, lower bit rates, and an improved customer experience.

Further Information

- Altera Video Over IP reference design:
  www.altera.com/support/refdesigns/sys-sol/broadcast/ref-video.html
- For more information on other 1080p reference designs using Altera's video framework, contact Altera sales:
  www.altera.com/corporate/contact/con-index.html

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101 Innovation Drive
San Jose, CA 95134
www.altera.com