Enabling Low-Power EO/IR System Development with FPGAs and Image- and Sensor-Processing IP

WP-01129-1.0 White Paper

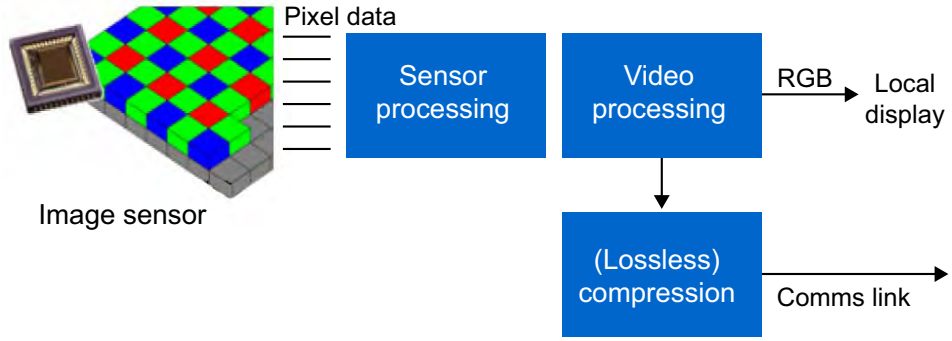
Before embarking on the development of a next-generation electro-optical and infrared (EO/IR) system, it is important to not only understand the power and performance characteristics of the FPGA, but also the various functions developed both as IP and reference designs. Altera's VIP Suite of MegaCore® functions provide sensor control and various image-processing capabilities, including buffering, scaling, filtering, and combining video streams in real time. Imagize's FP-5500 compact video-processing engine offers sensor processing and image fusion on an Altera® Cyclone® FPGA platform, meeting system performance and size, weight, and power (SWaP) requirements for next-generation EO/IR systems. Implementing these functions on Altera's Cyclone IV FPGAs can kick-start development efforts for next-generation EO/IR and display systems, as well as provide a canned solution for the "boring" aspects of system design, leaving the designer free to innovate on value-add functions.

Introduction

Military imaging systems are becoming increasingly sophisticated, incorporating multiple advanced sensors ranging from thermal infrared, to visible, to even ultraviolet focal planes. Not only do these sensor outputs need to be corrected, interpolated, etc., often images from multiple sensors must be combined and further processed for local display and/or for transmission.

Figure 1 shows a high-level block diagram of a typical signal chain implemented in an electro-optical infrared (EO/IR) system. As shown, the processed image is compressed many times (usually lossless) before being transmitted over a communications link.

Figure 1. Typical Signal Chain for an EO/IR System



Combining exceptional image quality with low power consumption is the key challenge when designing EO/IR systems. For hand-held and wearable systems, such as night-vision goggles (NVGs) or weapon sights, the critical specification is often the number of hours a unit can run on AA batteries. According to military estimates, "An infantry soldier requires one AA battery an hour in combat." *(1)*

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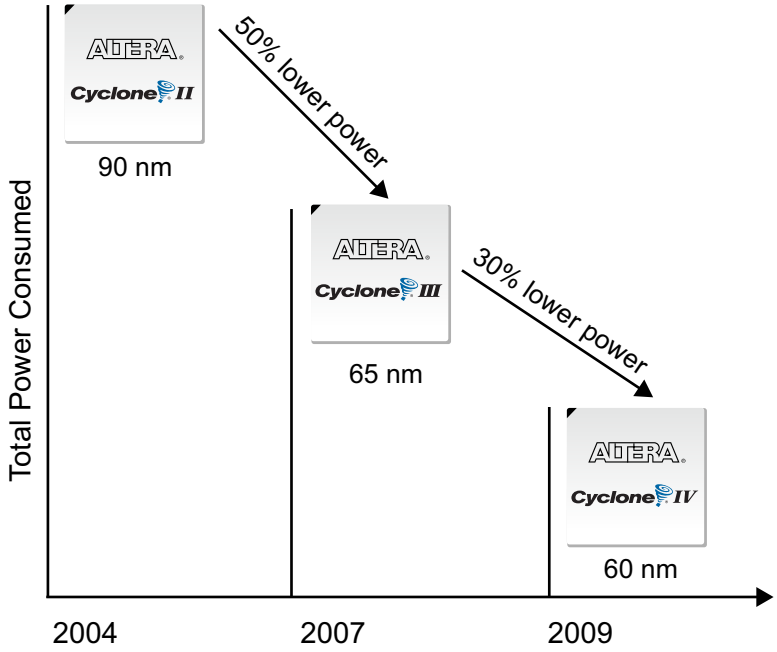
Low-power FPGAs are the platform of choice for almost all state-of-the-art EO/IR systems because they meet the needs for programmability, real-time video-processing performance, and low power consumption. In fact, each successful generation of low-power FPGAs have featured both lower static and dynamic power consumption by utilizing a combination of architectural enhancements and lower core voltages. As the process technology continues to march downwards, the average power consumed by these FPGAs has dropped 30% or more each generation, as shown in Figure 2.

Figure 2. Power Reduction in Successive Generations of Low-Power FPGAs of Comparable Density



Altera's Cyclone® IV FPGA family extends the Cyclone FPGA series' low-power leadership by providing the market's lowest cost, lowest power FPGAs with a transceiver variant. Ideal for high-volume, cost-sensitive applications, Cyclone IV FPGAs enable designers to meet increasing bandwidth requirements while lowering costs. The family includes:

- Cyclone IV GX FPGAs with up to eight integrated 3.125-Gbps transceivers
- Cyclone IV E FPGAs for a wide spectrum of general logic applications

Offering up to 150,000 logic elements (LEs), Cyclone IV FPGAs consume up to 30% less total power than the previous generation. This low-power, programmable silicon platform provides ample computational power to implement the sensor-control and image-processing algorithms required for most HD video processing systems.

The first group of these algorithms is responsible for the configuration and operation of the image sensor (also called focal plane array (FPA)). These algorithms include the generation of video timing and control signals for exposure control, readout logic, and synchronization.

Next, the pixel streams generated by the sensors are processed by a second group of algorithms that addresses the imperfections of the focal plane. Functions such as non-uniformity correction (NUC), defective pixel replacement, noise filtering, and pixel binning may be used to improve image quality. For a color-capable focal plane, demosaicing may be performed. The corrected video stream is then used to implement functions such as automatic gain and exposure control, wide dynamic range (WDR) processing, white balancing, and gamma correction.

In addition, FPGA-based camera cores are able to implement video-processing algorithms that further enhance the output video. These processing stages may include functions such as image scaling (digital zoom), (de)warping, windowing, electronic image stabilization, super-resolution, external video overlay, image fusion, and on-screen display. In some cases, the captured and processed video stream may need to be compressed before it is transmitted to a control station.

Essentially, the EO/IR system implements high-quality sensor control and image processing within a tightly constrained power budget, all while retaining the programmability required for last-minute specification changes and field upgradeability.

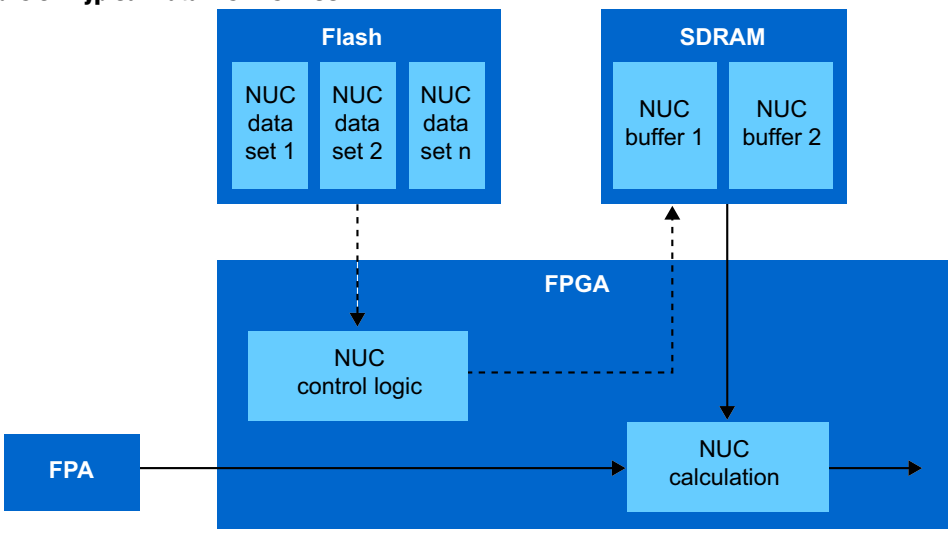
Sensor Processing

The focal planes used in EO/IR systems require flexible and accurate timing and a variety of control signals to properly operate. Programmable phase-locked loops (PLLs) are a standard feature in power-efficient Cyclone IV FPGAs and are an excellent choice for generating these timing signals. Furthermore, efficient clock distribution networks within the FPGAs allow for the logic designer to meet the timing specs of practically any EO/IR focal plane used in low-power applications. The variety of high-speed differential and single-ended I/O standards supported by Cyclone IV FPGAs is also a key factor when interfacing to the focal planes and/or the associated read-out integrated circuits (ROICs).

NUC and pixel replacement algorithms typically require only a few mathematical operations per pixel, but these calculations must be made at pixel rate and with data that may be different for every pixel. The critical design element for achieving low power is therefore affected by the way data movement is architected. For NUC, pixel-specific coefficients must be streamed into the logic block implementing the correction formulas. For smaller sensors, these coefficients may be stored in an internal FPGA memory, thus providing excellent power efficiency. For larger sensors, these data must be buffered in external memory and read out in sync with the pixel stream for every video frame. In either case, the need to change the corrective data set usually is based on some selected parameter, such as the FPA temperature.

The sensors' storage needs can be facilitated by flash memory, which can store multiple sets of correction data and update the contents of the correction buffer when needed. As shown in Figure 3, the correction coefficients may be double buffered to allow the relatively slow data stream from the flash memory to complete before the new set of data is applied. When required, the next set of correction data may be loaded in the background while the current set of correction coefficients is applied at video rate.

Figure 3. Typical Data Flow for NUC

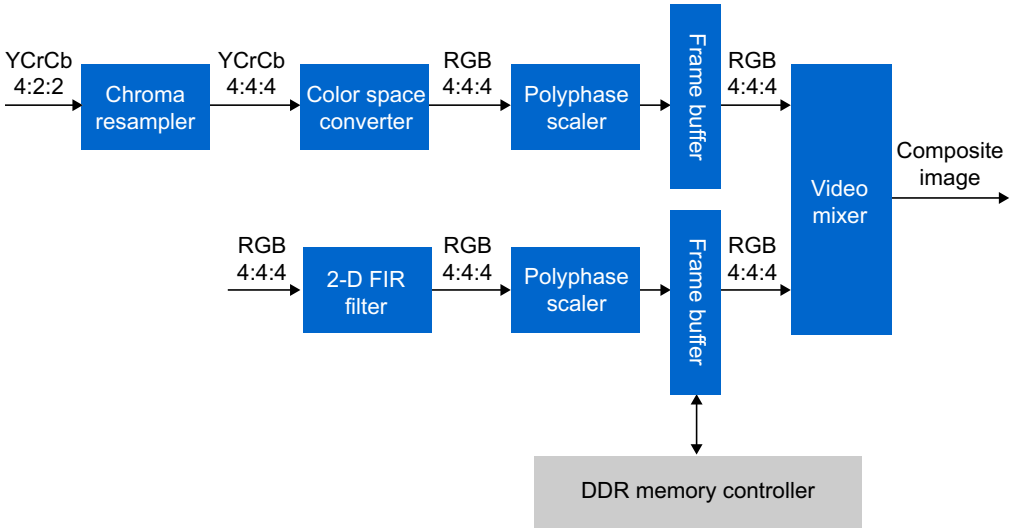


This relatively simple example shows how the flexibility of the FPGA routing fabric provides highly efficient ways to move data without creating architectural bottlenecks. This flexibility allows the designer to create data pathways that fit the algorithm rather than change the algorithm to fit a pre-defined architecture. Flexibility is a key advantage of FPGA solutions compared to processor-based systems and is critical for achieving very low power consumption.

Video Processing

Military EO/IR systems are often set up so that the images from multiple sensors must be fused together and shown on a custom display with non-standard resolutions. Figure 4 shows a block diagram of a typical video-processing system that might be used to generate a composite image from two video sources on a custom display. The input video is first formatted into the desired color space and subsequently scaled (or resized) and alpha blended (or mixed)-among the most commonly used video functions-with multiple other video streams.

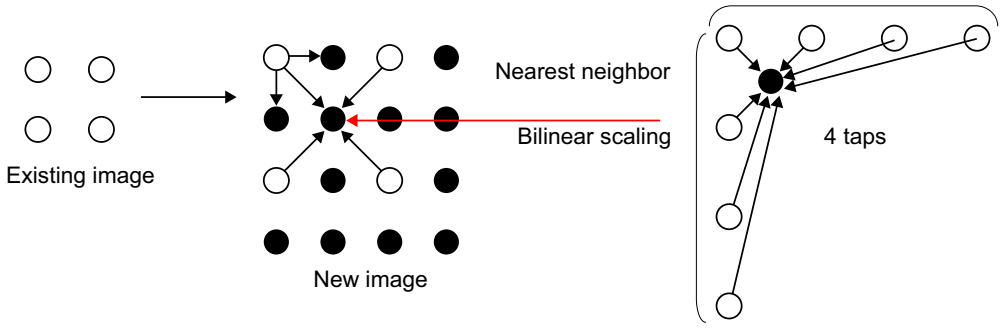
Figure 4. Video Datapath to Generate a Composite Image from Multiple Sources



Scaling

Scaling can be as simple as copying the previous pixel (or dropping it) or can be implemented with complex interpolation filtering techniques to generate a new pixel. With all generated pixels shown in solid black and all original pixels in white, Figure 5 demonstrates the difference between the different algorithms that can be used for scaling, ranging from nearest neighbor algorithm (i.e., copy the preceding pixel) to multi-tap scaling.

Figure 5. Different Video Scaling Algorithms Yield Different Video Qualities

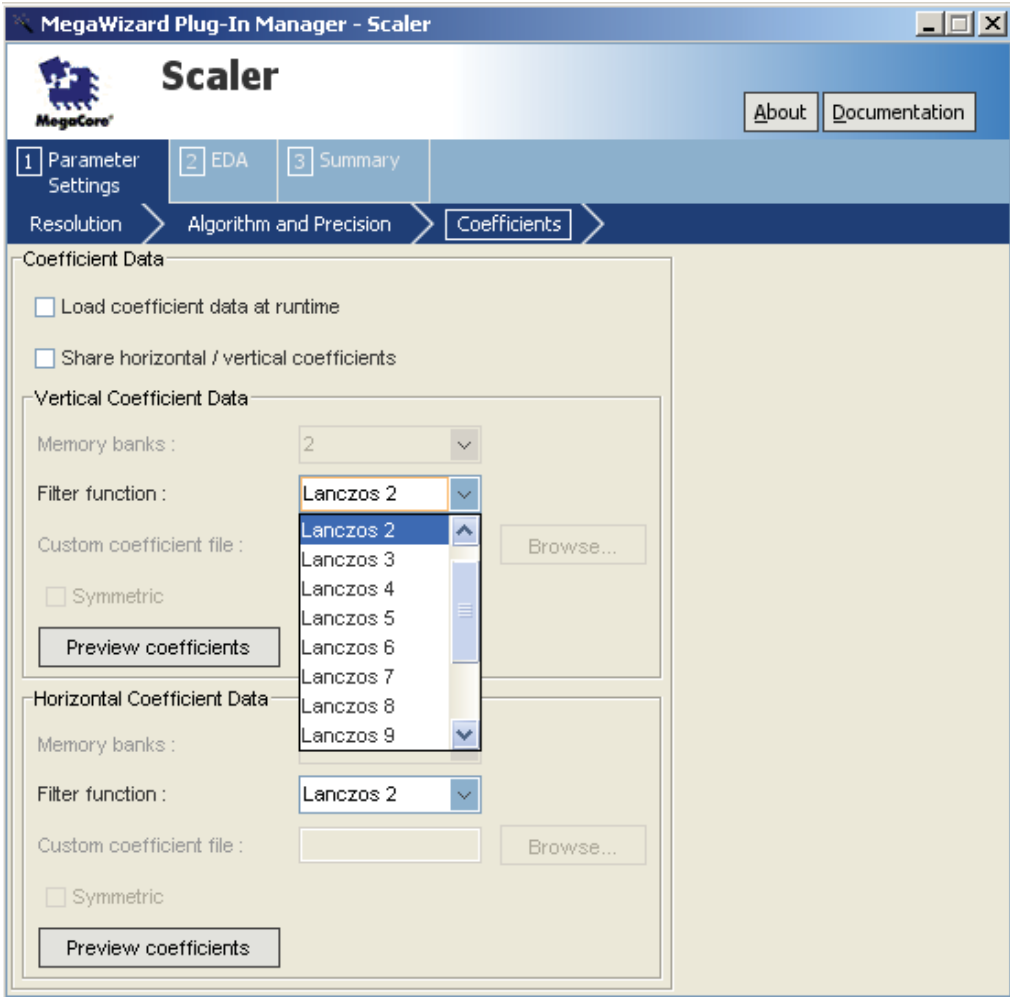


A more complex method is to take an average of the two neighboring pixels in both the vertical and horizontal dimensions. Sometimes this is referred to as bilinear scaling, because it uses a pixel array of size 2x2 to compute the value of a single pixel. Taking this concept further, one can compute the new pixel based on m pixels in the horizontal dimension and n pixels in the vertical dimension. Figure 5 shows how a pixel is generated with four pixels in each dimension, a method known as a 4-tap scaling engine.

It is important to note that the coefficients-the weights assigned to each pixel-determine the quality of the scaled image. Many FPGA vendors provide a reference design or an intellectual property (IP) function that builds a multi-tap scaling engine using either pre-built or custom coefficient values.

Figure 6 shows a scaling IP core developed by Altera. This core comes pre-built with various "Lanczos" filter functions, which are multivariate interpolation methods used to compute new values for any digitally sampled data. When used for scaling digital images, the Lanczos function indicates which pixels in the original image, and in what proportion, make up each pixel of the final image.

Figure 6. Video Scaling IP Automates the Implementation of Polyphase Scaling Algorithms



A designer can either select from a range of Lanczos algorithms to scale the image or bypass these altogether in favor of custom coefficients. In either case, the function automates the tedious job of generating the HDL code for what is essentially a two-dimensional filter. It then maps it to FPGA structures such as the digital signal processing (DSP) blocks and the embedded memory blocks, thus improving productivity and reducing design time.

Alpha Blending

Another common process is the mixing and overlay of two or more video streams. This is usually performed by the alpha blending function. The function generates a composite pixel from, for example, two pixels. One pixel is assigned an opacity value, α. When α is zero, that pixel is completely transparent, that is, it is not displayed. When that α is 1, the pixel is completely opaque, so only that pixel is seen and the other pixel is not displayed. In mathematical terms, the value of the composite pixel is calculated as:

$$C = \alpha P1 + (1 - \alpha)P2$$

In addition, this technique can be used to create translucent images because α can be set anywhere between 0 and 1. While this is a relatively simple way to mix video streams and add text overlay, it is computationally expensive because it uses two multiply operations and one add operation per pixel, per frame.

Some IPs allow the designer to implement multilayer alpha blending with high-precision values for α. Figure 7 shows the alpha blending IP from Altera that efficiently mixes up to 12 image layers, and provides support for both picture-in-picture mixing and image blending with the ability to set a value for α for each pixel with an eight-bit resolution.

Figure 7. Alpha Blending IP Facilitates the Creation of a Composite Image from Multiple Video Sources

Image Fusion

Image-fusion algorithms provide a more sophisticated method of combining information from two (or more) images. While a thermal (IR) image and a visible (TV) image depict the same scene (Figure 8), each contains different information. If one was to apply alpha blending to select how dominant one or the other image is in the combined output, no single value for α would be able to bring out all the information available from the sensors.

Figure 8. Sensor Image Fusion with Simultaneous Utilization of Multiple EO Sensors, Typically with Complementary Capabilities Such as Visible (TV) and Thermal Infrared (IR)

While the visible image (Figure 8, top left) contains information about the surroundings, the thermal image (Figure 8, top right) only shows discernible features where the temperature differs from the background. Conversely, the performance of the thermal sensor is unaffected by the strong light source, while the visible sensor provides no information in the same area due to saturation.

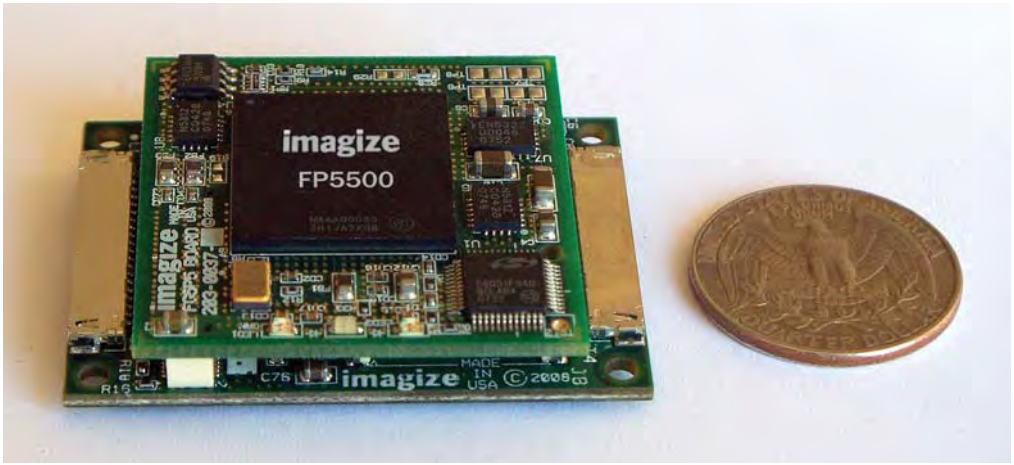
In the fused view (Figure 8, bottom), a seamless combination of information from both input modalities is achieved on a pixel-by-pixel basis. Details missing from one modality are filled in from the other and vice versa. As a simplest form of fusion, one may apply alpha blending with a different α value for every pixel calculated from local image statistics. State-of-the-art fusion algorithms, however, typically go beyond that to perform a decomposition of the input images, extracting relevant features around every pixel. These features are then combined to form a fused image.

Low-Power Video Processing Platforms

Even complex algorithms such as feature-based image fusion can be efficiently mapped onto low-power FPGAs. Utilizing DSP and distributed memory resources, highly efficient designs can be created for real-time manipulation of high-definition video. Altera's Cyclone IV FPGAs provide power-efficient, yet flexible, platforms for implementing real-time video-processing algorithms. Incorporating an FPGA-based image-processing core into camera or in-line video-processing electronics offers a highly flexible architecture capable of supporting a range of algorithmic IP and I/O interfaces while minimizing power consumption.

An example for such a design is Imagize's FP-5500 video processing engine, shown in Figure 9. The compact 25 cm3 module consists of an FPGA board and an easily customizable I/O board. The unit weighs only 20 g, but provides a highly configurable platform for real-time manipulation of multi-megapixel (MP) video streams at a typical power consumption of 500 mW. Owing to the reconfigurable nature of FPGA technology, the same hardware platform can support multiple end products via different firmware loads and can be rapidly customized. Using the FP-5500 module or its application-specific versions, OEMs and system integrators can quickly incorporate real-time video enhancement, motion processing, and image fusion in a variety of products including portable, handheld, and wearable applications.

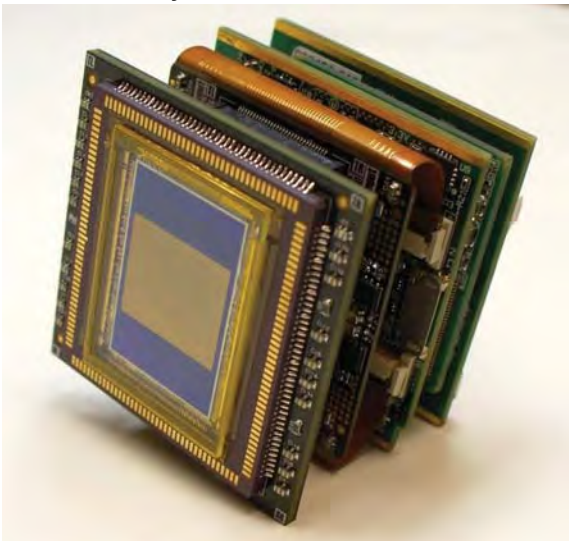
Figure 9. Imagize's FP-5500 Compact Video Processing Engine, Based on a Cyclone III FPGA



The size, weight, and power (SWaP) metrics of designs based on Altera's low-power FPGA technology compare favorably with alternative technologies such as CPU-, graphics processing unit (GPU)-, or DSP-based architectures. This is primarily the result of the inherent flexibility of the programmable fabric, which allows the architecture to be optimized for a given algorithm rather than the algorithm being forced to fit a fixed computing architecture. By putting computation where the data is rather than shuttling operands between the main memory, the cache, and an arithmetic logic unit (ALU), a significant increase in power efficiency can be achieved.

The low-power capabilities of the FPGA-based design approach are borne out in systems such as the high-definition camera core shown in Figure 10. In this design, a 5.5-MP CMOS image sensor is controlled by logic in a Cyclone III EP3C55 FPGA. Operating at 30 frames per second, the FPGA performs high-speed readout, exposure control, NUC, pixel processing, and frame-buffering functions, yet consumes only 1 W of power. While the data rates required by an advanced sensor, such as the one used in this application, push the limits of the Cyclone III fabric, this design establishes a performance benchmark that puts common high-definition video standards, such as 1080p HDTV formats, well within the capabilities of Cyclone III devices.

Figure 10. High-Resolution Camera Application Based on Imagize's FP-5500 Engine, Fairchild Imaging's CMOS Sensor, and Altera's Cyclone III EP3C55 FPGA



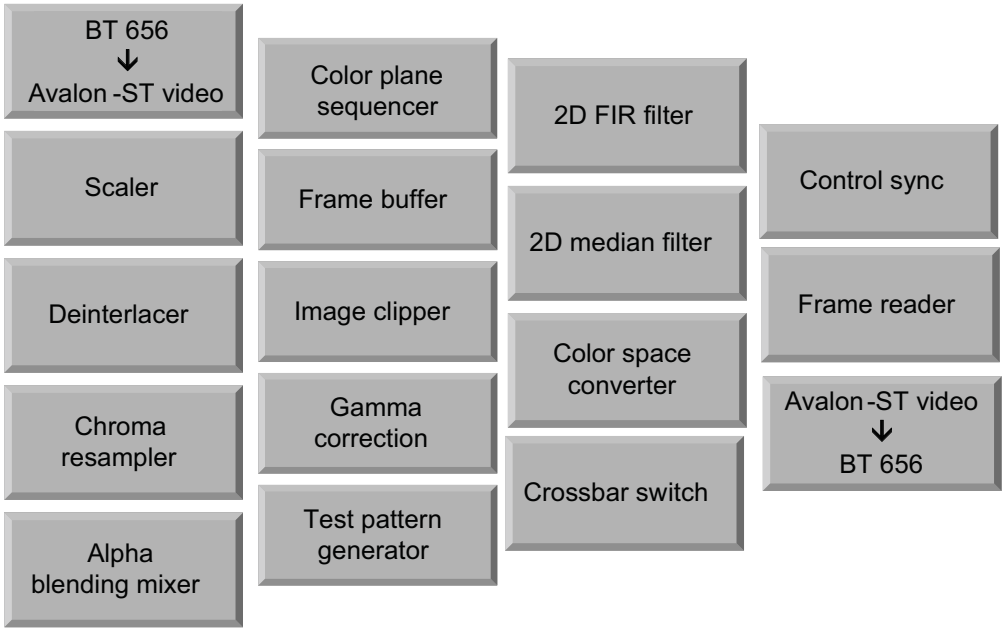
VIP Suite

Altera's Video and Image Processing (VIP) Suite is a collection of tools and building-block video MegaCore® functions designed to speed the development and implementation of the custom image-format conversion design. It consists of the following components:

- Building-block video IP cores
- Format-conversion reference designs that showcase FPGA capabilities and provide a starting point for design
- Open-source, low-overhead video interface that allows mixing and matching of custom and/or off-the shelf IP blocks
- System-level design tools for integrating processors and memory subsystems
- Variety of video development kits for rapid design prototyping

The key component of this framework is the largest portfolio of video-processing building blocks available as a single suite of IP cores (Figure 11). These blocks are designed to be plug-and-play with standard streaming video interfaces, thus allowing the quick and efficient design of a custom video-processing chain.

Figure 11. Altera's VIP Suite



Conclusion

Before embarking on the development of a next-generation EO/IR system-be it be weapons sight, a night-vision goggle system, or a custom display-it is important to not only understand the power and performance characteristics of the FPGA but also the various functions that have been developed as IP and reference designs. Altera's VIP Suite of MegaCore functions, along with solutions from third-party IP vendor Imagize, provide sensor processing and various forms of image processing, including scaling, alpha blending, and image fusion. Implementing these functions on Altera's Cyclone IV FPGAs can kick-start development efforts for next-generation EO/IR and display systems, as well as provide a canned solution for the "boring" aspects of the system design, leaving the designer free to innovate on value-add functions.

Further Information

1. "The Current Status of Fuel Cell Technologies for Portable Military Applications," 25th International Battery Seminar and Exhibit, 17 - 20 March 2008, Fort Lauderdale, FL, Jonathan M. Cristiani, Chemical Engineer, US Army CERDEC C2D Army Power Div.: www.dtic.mil/cgi-bin/GetTRDoc?AD=ADA491714&Location=U2&doc=GetTRDoc.pdf
2. Video and Image Processing (VIP) Suite MegaCore Functions: www.altera.com/products/ip/dsp/image_video_processing/m-alt-vipsuite.html
3. Imagize FP-5500 Embedded Image Processing Engine Product Information: www.imagizellc.com

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- Tibor Kozek, Ph.D., CTO, Imagize LLC
- Juju Joyce, Sr. Strategic Marketing Engineer, Military and Aerospace Group, Altera Corporation

Document Revision History

Table 1 shows the revision history for this document.

Table 1. Document Revision History

Date	Version	Changes
May 2010	1.0	Initial release.