White Paper

FPGA

An Intel Company

Top 7 Reasons to Replace Your Microcontroller with a MAX® 10 FPGA

Differentiate products, meet time-to-market schedules, and navigate processor obsolescence risk with MAX® 10 FPGAs and the Nios® V processor.

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Introduction

Processors, whether microprocessors or microcontrollers, are one of the most universal components in digital electronic systems. With the recent rapid growth of Internet of Things (IoT) solutions this prevalence continues to increase. Whether designing for the IoT revolution or bleeding edge products that require novel solutions, a commercial off-the-shelf (COTS) processor cannot provide the optimal combination of performance, peripherals, form factor, scalability, or life cycle persistence to deliver competitive differentiation and time-to-market needs. With COTS processors, designers must compromise on microcontrollers with fixed functionality by choosing to either overpay for features they don't need or over-designing their system to add features the COTS lack. FPGA-based solutions, with their integrated fully customizable soft processing capability, enable true flexibility and scalability—addressing custom needs with programmable hardware and software in a single chip.

The Nios® V processor is an FPGA-optimized 32-bit RISC Harvard architecture soft-core processor. As the FPGA is programmable, the Nios V processor is also configurable -- enabling it to meet the exact requirements of any application. In addition, the processor peripheral set is easily configured to meet any application-specific requirement. MAX 10 FPGA-based solutions, based on the Nios V processors, overcome the limitations of COTS by enabling a unique single-chip embedded system that can be customized for product differentiation and optimization. The innovative architecture of MAX 10 FPGAs and the flexibility of Nios V processors provide an unmatched alternative solution for today's embedded designers.

Single-chip, Instant-on Capability

By integrating 55 nm embedded flash onto the MAX 10 FPGA die, the capability for a true single-chip embedded system with both hardware and software customization is fully realized. Imagine a CPU with customizable hardware features that can change real-time in the field to match the Quality of Service (QoS) or feature packages licensed by the end customer. Better yet, the ability to upgrade a system's microcontroller hardware for changes due to emerging standards, functionality missing in initial release due to time-to-market pressures, or product upgrades purchased after the initial installation. These scenarios are not physically possible with COTS processors, but are possible when utilizing Nios V processors with MAX 10 FPGA's embedded flash and remote update capability.

The MAX 10 embedded flash contains two FPGA configuration image partitions as shown in Figure 1; one of these can be used to guarantee failsafe remote-updates to the FPGA hardware image. If the remote update or dual-configuration capability is not required, the general-purpose user flash memory (UFM) can be expanded (up to 700 Kilobytes) for additional software code storage space.

System boot and management also benefit from the on-die flash. In traditional FPGA systems with embedded processor technology, whether hard or soft, the FPGA takes a "non-instant" amount of time to power-up and configure. With MAX 10 FPGA's on-die flash, the FPGA powers-up instantly (in a few milliseconds) as the first component in the system, allowing the custom FPGA logic to not only completely manage system bring-up but also allowing the Nios V system to be available at system power-on for software diagnostics or prognostics.

This single-chip integration and hardware upgrade capability give embedded designers reduced cost of ownership by eliminating product design defects, product returns, and providing competitive advantage with customized hardware.

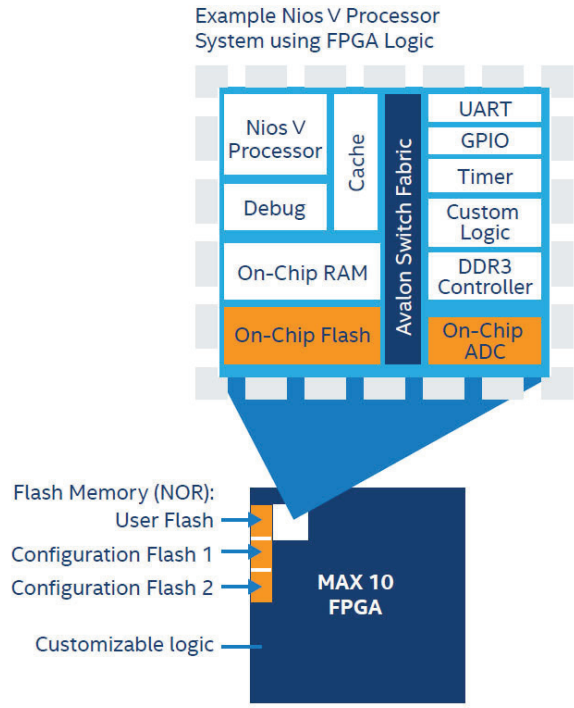

Figure 1. Single-Chip Nios V Processor Capability with Dual-Configuration Partitions

Analog-to-digital Converters

MAX 10 FPGA integrates up to two 12 bit analog-to-digital converter (ADC) blocks with up to 17 input channels that can be used to measure environmental conditions, manage power-up and power-down sequencing, control motor torque, and so on. The 12 bit ADCs include programmable digital interfaces, sample sequence control, hardware averaging, and interrupt thresholds for voltages and device temperature. By using these ADCs in Nios V processor designs, microcontrollers or external ADCs can be replaced to reduce system cost and complexity.

Small Form Factor, Integrated Devices

With packaging as small as 3 x 3 mm2, MAX 10 FPGA's single-chip solution is the smallest configurable FPGA footprint in the industry. These small package sizes allow the MAX 10 FPGA to replace or augment ASICs, ASSPs and microcontroller units (MCUs) in portable or space-constrained applications. As shown in Figure 2, combined with the highly integrated Intel® Enpirion® Power Solutions, MAX 10 FPGA's on-die flash, ADC, phase-locked loops (PLLs), and configurable Nios V processors reduce board space by up to 50% over competing FPGA solutions with discrete power supplies. MAX 10 FPGAs have a single supply device option, possible through an on-die regulator, which further minimizes board space and complexity by eliminating the need for multiple power rails to the device. This reduction in chip count and PCB size keeps system costs down while increasing system reliability for an optimized embedded system.

Customizable Peripheral Sets

With the perfect fit of CPUs, memory interfaces, and custom peripherals to meet the unique demands of every new design, the Nios V processors offer tremendous flexibility where designers need it. Designers may choose from different Nios V CPU flavors to optimize the processor for performance or size and can even create custom CPU

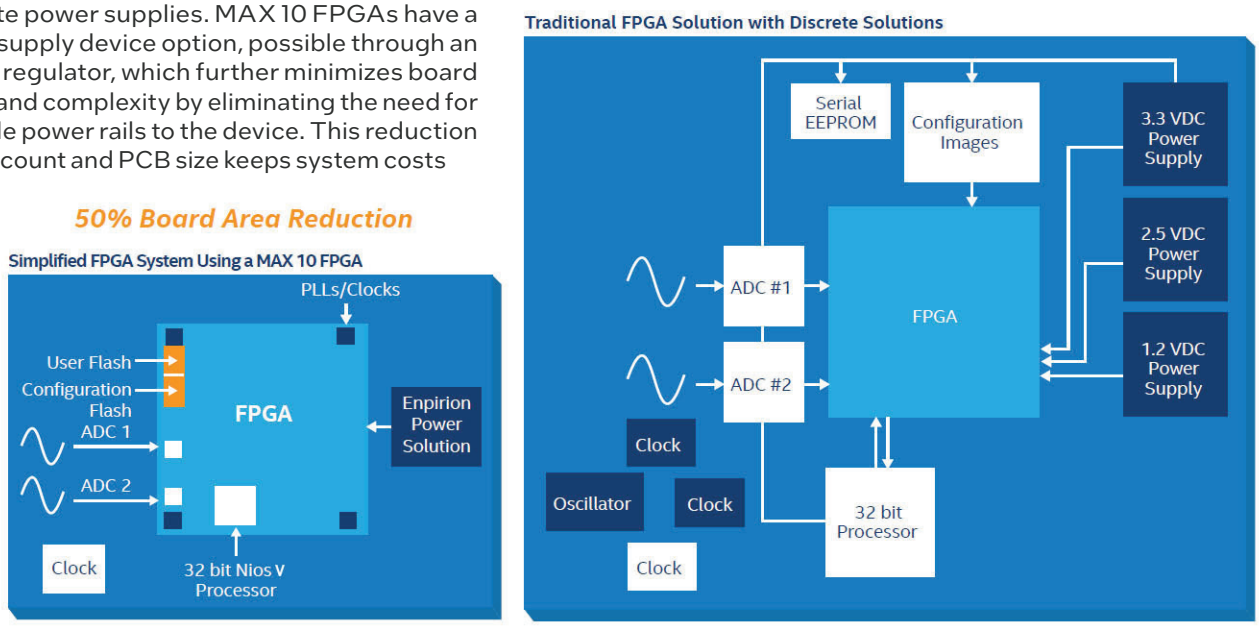

Figure 2. Board Space Reduction vs. Traditional FPGA Solutions

configurations to meet their needs. Customized peripherals in the FPGA can be an embedded system's "secret sauce" allowing any number of general purpose I/Os (GPIOs), Ethernet MACs, serial interfaces, multiple CPUs, and so on. A large library of embedded peripherals are available to plug into your custom system or designers have the option of creating their entirely unique and custom hardware peripheral blocks using Verilog HDL or VHDL. Assembling the exact set of peripherals necessary for an end system, which are not available in COTS products, gives embedded designers a differentiating advantage over their competition by maximizing functional efficiency and engineering costs.

Real-time Processing Optimization

Traditionally, embedded developers have had limited options for accelerating performance near the end of a design cycle, including buying a faster processor or last minute hand-tuning of assembly subroutines. While both options can be effective, the trade-offs they bring are too large to ignore. MAX 10 FPGAs and Nios V processors provide an entirely new toolbox of performance-enhancing features.

Using custom hardware accelerators, designers can optimize their system performance in a way not possible with traditional off-the-shelf processors. The configurable nature of Nios V processor systems allow designers to create custom components in FPGA logic that can run as a co-processor unit for complex algorithms. These accelerator or co-processing units can run in parallel to the Nios V processor, executing functions orders of magnitude faster than software execution. Figure 3 illustrates an example custom accelerator and its relative performance to software-only implementation.

Nios V processors provide many other options for reducing risk in embedded design, as shown in Table 1.

Life Cycle Benefits

Nios V processors in MAX 10 FPGAs help developers maximize return on a product by providing life cycle benefits at every stage of a product's life. For time-to-market needs,

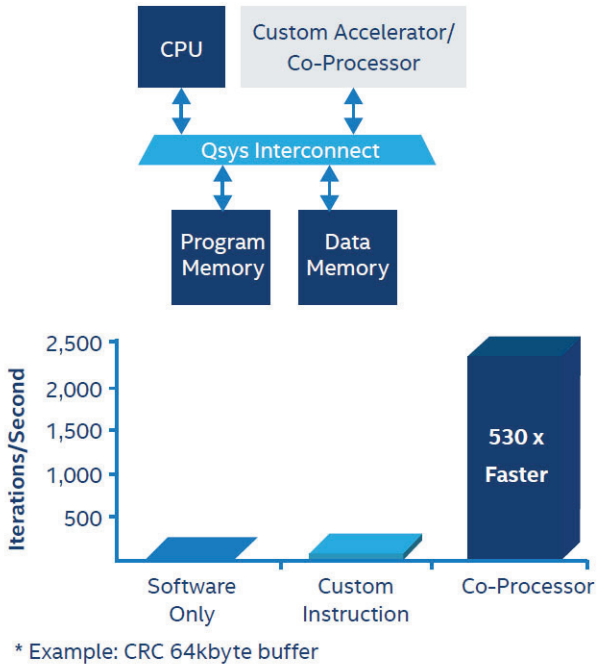

Figure 3. Custom Accelerator Performance Gains

the hardware programmability of the MAX 10 FPGA allows design errors to be fixed quickly with simple changes to the FPGA design. Being first to market can often mean shipping a less-complete product than desired. MAX 10 FPGA-based systems using a Nios V processor offer the unique advantage of being able to update hardware features to products already deployed in the field, the same way software is updated. This solves several problems:

- Extends product life, allowing the hardware to be feature-filled over time
- Reduces the risk of using hardware that is based on emerging (or changing) standards
- Simplifies hardware bug fixes and eliminates the need for product returns and rework

Feature	Description
High-performance processor core	Optimized for performance-critical applications, the Nios V processor has a 5-stage pipeline, dynamic branch prediction, instruction and data caches, and a vectored interrupt controller (VIC) in MAX 10 FPGAs.
Multiprocessor systems	Use multiple NiosV processors in your system to scale performance or to divide software applications into simpler parallel tasks. The hardware and software development tool suites include support for creating custom multicore systems. Nios V processors, combined with the larger density MAX 10 FPGAs are ideal platform for creating high-performance multiprocessor applications.
Custom instructions	Accelerate time-critical software operations by adding custom instructions to the Nios V instruction set where custom hardware can execute the operations faster than any possible software routine. Supported for Nios V/g processors only.
Hardware accelerators	If the process or algorithm that requires performance acceleration is too complex or datapath dependent for implementation as a custom instruction, it can be implemented as a custom high-performance co-processor unit that can run in parallel to the Nios V processor.
Real-time	The Nios V processor has an option to replace the standard interrupt unit with a low-latency vectored interrupt unit to deliver faster and more deterministic interrupt response. For the ultimate real-time response and determinism, core functions can be implemented in FPGA logic bringing the performance of hardware but without losing the controllability and flexibility of software.
Fast configurable on-chip memory	Create fixed low-latency on-chip memory buffers for performance-critical applications.

Table 1. Potential Performance Enhancements with Nios V Processors in MAX 10 FPGAs

To accommodate a diverse customer base, embedded processor vendors offer a range of configuration choices within a processor family, but inevitably many of these processor variants are obsoleted earlier than the rest of the family. Savvy designers realize that the soft Nios V processors are not subject to the same market pressures as hard processors. Nios V processor designers have a perpetual license to create and deploy customized Nios V processor-based designs in MAX 10 FPGAs, so even if the underlying FPGA hardware changes, the investment in application software is preserved. Figure 4 illustrates sales output against a product lifecycle.

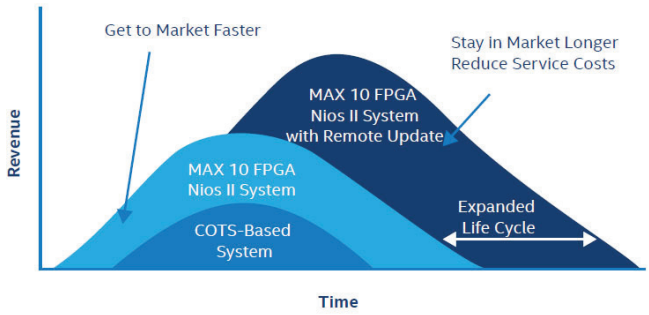

Figure 4. End Product Revenue Extension Using MAX 10 FPGAs with Nios V Processors

The feature upgrade and customization capability with Nios V processor systems can eliminate obsolescence risk, extend your end products time-in-market life, and maximize ROI of the product. This results in a much lower total cost of ownership (TCO) than traditional COTS processors with their fixed functions and obsolescence risks.

Industry-leading Development Tools

When designing with the Nios V embedded processor, designers have access to a portfolio of mature, robust software development tools and software components available from Intel and Nios V ecosystem partners.

The free Qsys system integration tool saves significant time and effort in the FPGA design process by automatically configuring soft intellectual property (IP) and generating interconnect logic to connect IP functions and subsystems. The easy-to-use GUI provides a simple, quick method for configuration and integration of peripherals into FPGA system designs.

The Ashling RiscFree* IDE is a free, comprehensive development package for Nios V processor software design. This package can import the hardware configuration to build a custom board support package for your unique processor configuration and system design, enabling you to start writing software immediately. The Nios V EDS contains not just Eclipse-based development tools but also device drivers, a bare metal Hardware Abstraction Layer (HAL) library, a commercial grade network stack, an evaluation version of a real-time operating system (RTOS) and example software. Thanks to its popularity all the major RTOS vendors support the Nios V processor and there is a Linux* distribution and active developer community on www.rocketboards.org.

Conclusion

Embedded designers are under increasing pressure to differentiate their products, meet faster time-to-market schedules, and navigate the risks and challenges of processor component obsolescence. Nios V processors used in single-chip MAX 10 FPGAs, remove obsolescence risks, increase differentiation through custom hardware and performance optimization, and reduce system costs with integrated features and small form factor offerings. System architects using the synergy of Nios V processors and MAX 10 FPGA programmability are equipped with a measurable advantage on the road to product success.

Where to Get More Information

For more information about Intel and MAX 10 FPGAs, visit www.intel.com/content/www/us/en/products/details/fpga/max/10.html

1 https://www.intel.com/content/www/us/en/products/details/fpga/nios-processor/v.html

2 https://www.intel.com/content/www/us/en/design-example/714689/intel-max-10-fpga-first-nios-ii-processor-design-for-terasic-s-intel-max-10-fpga-neek-board.html

3 https://www.intel.com/content/www/us/en/software/programmable/quartus-prime/qts-platform-designer.html

4 https://www.intel.com/content/www/us/en/support/programmable/support-resources/fpga-training/overview.html

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