Meeting the Low Power Imperative at 28 nm

WP-01158-2.1 White Paper

This document describes how Altera's 28-nm devices enable product developers to control power consumption in today's increasingly power sensitive applications.

Introduction

Reducing power consumption in electronic products is no longer just a good idea; for many product developers and manufacturers, it is an essential strategy for gaining competitive advantage in an increasingly power-aware and power-hungry world. Lower power consumption delivers the following clear advantages to designers and end users:

- Enables developers to address more power-constrained or thermally-restrictive markets
- Provides developers more freedom to increase capabilities within the same thermal and power budget
- Lowers operational and material costs and results in more compact products
- Reduces stringent cooling requirements
- Provides social responsibility benefits

Component suppliers must provide developers and manufacturers with the best options to reduce energy consumption and address this power imperative—or quickly find themselves at significant disadvantage. Altera's latest generation 28-nm devices empower product developers and manufacturers to directly address the power imperative.

Low Power Imperative

The US Department of Energy predicts that global electricity generation will exceed 20 trillion kilowatt hours (kWh) by 2015, and 35 trillion kWh by 2035, as illustrated in Figure 1. (1) Electronic equipment is one of the fastest-growing segments of that increase, driven by elements such as data centers and communications networks. For example, power consumption for servers and other internet infrastructure in the US doubled, from over 20 billion kWh in 2000, to over 40 billion kWh in 2005. (2) Likewise, worldwide power consumption for the same functions has similarly doubled in that same time period, going from over 60 billion kWh in 2000, to over 120 billion kWh in 2005. (3)

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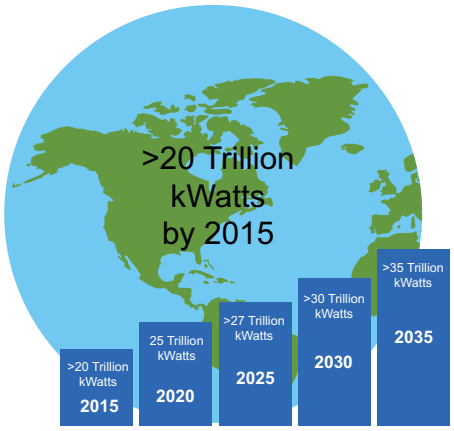
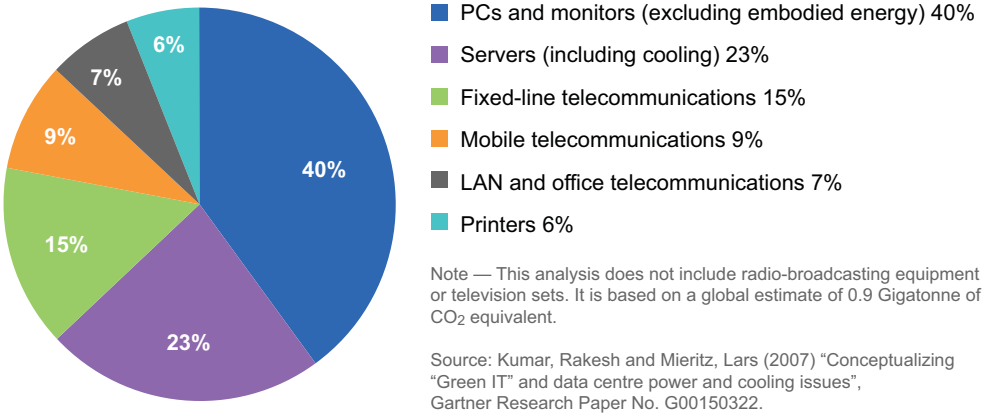
Figure 1. Forecasted Growth in Global Electricity Generation



Looking forward, data centers in the US are projected to consume up to 100 billion kWh in 2011, and double that by 2020 if historical trends are followed. This rapid increase has real economic impact. By 2015 the energy costs for server operation will *exceed* the costs of the server hardware [(4)]—a shift that could significantly impact the economics of the global communications and data center infrastructure.

Data centers account for only part of the rapid increase in electronic product power consumption. Other power consumption increases include the communication networks that transport the data, and the PCs and monitors that often serve as the endpoints for the data streams. Taken together, these elements comprise the information and communications technology (ICT) sector. Multiple industry groups measure the energy consumption of the ICT sector in terms of CO_2 equivalent emissions, reflecting the industry's concern over its role in producing greenhouse gasses. The ICT sector generates over 500 megatons of CO_2 equivalents annually—with over 30% of that attributed to wired and wireless communications—and the total is estimated to exceed 1.4 gigatons by 2020 if these trends continue, as shown in Figure 2. [(5)]

Figure 2. Estimated Distribution of Global ICT CO_2 Emissions



Note — This analysis does not include radio-broadcasting equipment or television sets. It is based on a global estimate of 0.9 Gigatonne of CO_2 equivalent.

Source: Kumar, Rakesh and Mieritz, Lars (2007) "Conceptualizing "Green IT" and data centre power and cooling issues", Gartner Research Paper No. G00150322.

These rapid rises in energy demand have prompted governments and industry to increase energy efficiency. For example, the US government—estimated to be the largest consumer of energy in the USA at an annual cost of over $20 billion—is under direction to reduce power consumption in a number of ways, including only purchasing products that consume 1 watt or less of standby power. (6) Similarly, the European Union has adopted regulations requiring products to draw only 1W to 2 W of standby power, with a reduction to 0.5 W or 1 W by 2013. Similarly, California has adopted regulations requiring televisions to consume 49% less electricity by 2013. (8)

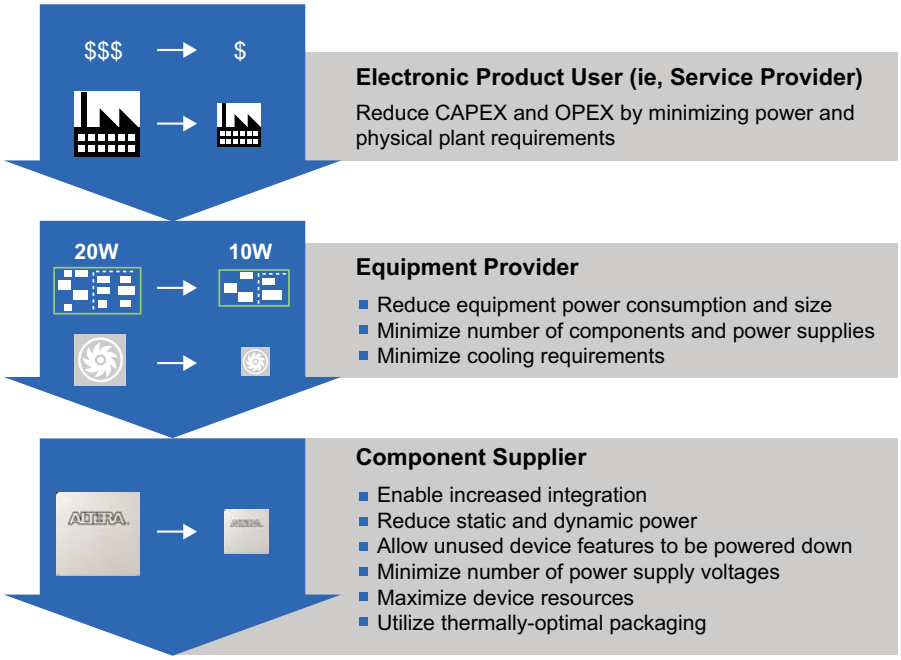
Private companies and industry bodies are also acting to reduce power consumption. For example, Verizon mandates that all new equipment must be at least 20% more energy efficient than its predecessor. (9) According to the industry group GreenTouch™, the global communications network is currently responsible for 300 million tons of CO_2 equivalents, (10) and according to the GSMA consortium for mobile communications, the worldwide mobile communications infrastructure including portable devices produces 245 megatons of CO_2 equivalents. (11)

Both of these organizations propose minimizing the generation of greenhouse gasses by setting specific targets. For example, GreenTouch proposes to increase the energy efficiency of the Internet and other communications networks by 1,000 times and specify the exact means to accomplish this improvement by 2015. (12) Similarly, the GSMA recommends efforts to maintain the current levels of global greenhouse gas emissions from the mobile industry, despite anticipated growth in the number of mobile connections by 70% to 8 billion by the year 2020. This goal requires decreasing the amount of greenhouse gas emissions per connection by 40% by the year 2020, compared to 2009. The same GSMA document predicts that "energy efficiency could save 15% of global emissions in 2020. It is one of the lowest-cost quick return options for cutting emissions." (11)

Ideal Low Power Components

With these power reduction goals in mind, product developers must deliver greater functionality while reducing the energy consumption of their products. In addition, power reduction also provides attractive economic benefits for end users. For example, in the case of a service provider who relies on electronic products as part of their business model, reducing power consumption lowers the operational expenditures associated with powering and cooling the electronic equipment. Also, lower overall power consumption can reduce the physical power supply requirements. All of these factors can also minimize the actual footprint of the physical plant, which reduces capital and operational costs. As shown in Figure 3, these end user requirements translate to requirements for the equipment provider, and ultimately for the component supplier.

Figure 3. Power Reduction Requirements Through the Supply Chain



FPGAs and programmable logic devices (PLDs) are uniquely suited to enable product developers to cost-effectively control power consumption in the following ways:

- Provides the rapid integration of many on-board logic, memory, and processor components into fewer devices or even a single device
- Reduces the total support components, power rails, board space, and associated power required to implement complex electronic systems
- Allows exploration of different implementation approaches and algorithms to fine-tune power consumption

Programmable logic's flexibility and power advantages make it an attractive choice when balanced against the cost and time-to-market disadvantages of full custom silicon.

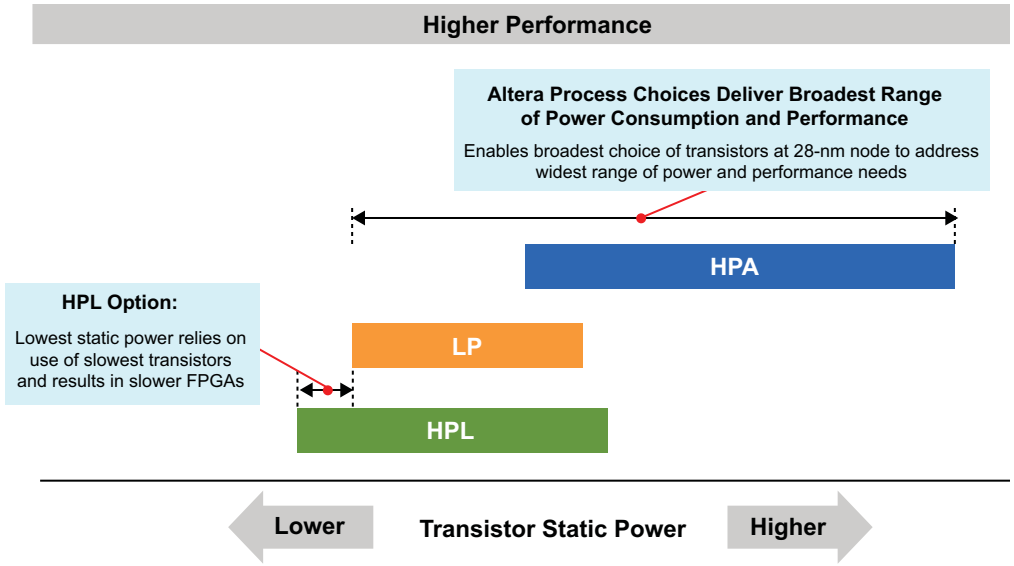
Tailored Power at 28 nm

At the 28-nm node, Altera devices enable designers to tailor power consumption to specific target markets and applications. Altera's approach leverages multiple semiconductor processes across its 28-nm product portfolio, as well as product or family-specific architecture optimizations, and hardened IP. As a result, Altera's 28-nm FPGAs consume up to 40% less power compared to their prior generation counterparts.

Figure 4 shows three 28-nm process options available from Taiwan Semiconductor Corporation (TSMC), which is the semiconductor foundry chosen by programmable logic vendors at the 28-nm node. Within each of these processes are available a number of transistors with a range of static power characteristics. Those transistors on the left side of the band use less static power, and those on the right use more. There is also a relationship between the static power consumption and the performance of

these transistors. In general, the higher the performance of the transistors, the higher their static power consumption. Altera uses both the 28LP and 28HP processes to provide the widest range of performance and power consumption options for its 28-nm products. The third process option, 28HPL, provides some transistors that draw less static power as indicated by the section labeled "HPL Option," but significant use of these transistors would result in FPGAs that are correspondingly slower—unacceptably slow for many designers. Accordingly, the 28HPL process for FPGAs requires use of its faster and leakier transistors, reducing or eliminating any static power advantage.

Figure 4. 28-nm Process Options from TSMC



Altera's devices consume the lowest total power of any FPGAs at the 28-nm node. The exceptional power characteristics of these devices result from a focused effort to reduce power consumption at all levels of product development. This effort begins with the 28HP and 28LP semiconductor processes.

For more information about Altera's efforts to reduce power in its high-performance 28HP-based Stratix® V device family, refer to the *Reducing Power Consumption and Increasing Bandwidth on 28-nm FPGAs* white paper.

Unlike the Stratix V family, Altera's other 28-nm FPGA products—the Cyclone® V and Arria® V families—are designed for applications that do not require the absolute highest performance and bandwidth. As a result, they are based on the 28LP process, which is designed to provide the lowest total power, as described by TSMC:

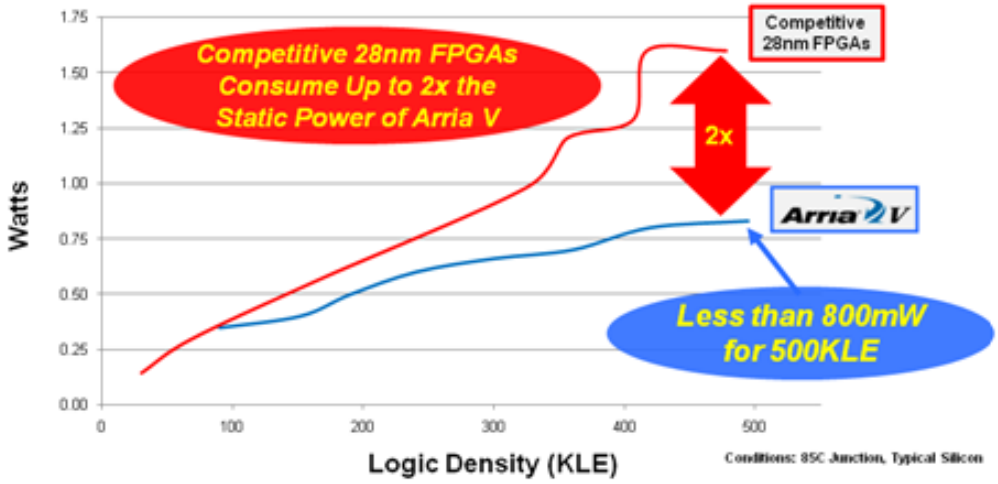
"The SiON-based 28LP process, the family's lowest total power and cost-effective technology, is expected to provide twice the gate density, up to 50% more speed or 30-50% lower power consumption than TSMCs' 40LP technology."

Other major semiconductor vendors seeking the absolute lowest power at the 28-nm node also choose the 28LP process, as Qualcomm demonstrated when they announced, "Qualcomm's work with TSMC yielded our Snapdragon™ S4 class of processors, including the Snapdragon S4 MSM8960™, a highly-integrated, dual-core SoC designed to reduce power in cutting-edge smartphones and tablets. The

Snapdragon S4 class of processors are manufactured in TSMC's highly sophisticated 28LP process, enabling Qualcomm to deliver the breakthrough combination of high performance and ultra low power to mobile devices." (13)

Building on this low-power foundation, Altera took additional steps to reduce static power in its 28LP devices by maximizing the use of transistors that are less "leaky" and therefore draw less static current. In addition, the Cyclone V and Arria V families offer a number of device features that can be disabled, including transceivers, I/O banks, PCI Express® blocks, memory blocks and fractional PLLs. These combined efforts result in devices that consume 70% less static power compared to prior generation FPGAs. For example, the Arria V family offers devices that consume less than 750 mW at 500K LEs—much lower than the static power consumed by the current generation of midrange and high-end 40-nm FPGAs. Even competitive 28-nm FPGAs consume up to 2.6X the static power of Arria V FPGAs. Figure 5 shows the typical static power of the Arria V GX devices in the solid blue line and the worst-case power in the dotted blue line. Similarly, the solid red line indicates the typical static power of competitive midrange 28-nm FPGAs, and the dotted line shows the worst-case power. With these characteristics, Arria V devices have the lowest static power consumption of any FPGAs in their class.

Figure 5. Arria V Static Power Comparison



Low Dynamic Power Architecture

In addition to low static power, Altera's Cyclone V and Arria V devices deliver low dynamic power to achieve the lowest total power. Altera's approach to achieving low dynamic power begins with the 28LP process, which targets power-sensitive applications including portable consumer, wireless connectivity, and cellular baseband. Describing their motivation for offering an advanced process designed for lowest total power rather than just static or dynamic power alone, TSMC states:

"(Our) decision to build on proven SiON technology for the 28LPT process is driven by changing wireless and portable consumer application dynamics under unrelenting pressure for products to hit market windows. Consumers a few years ago wanted low-leakage handsets that supported long battery life. Today's consumers increasingly rely on their wireless devices for Internet browsing, video streaming,

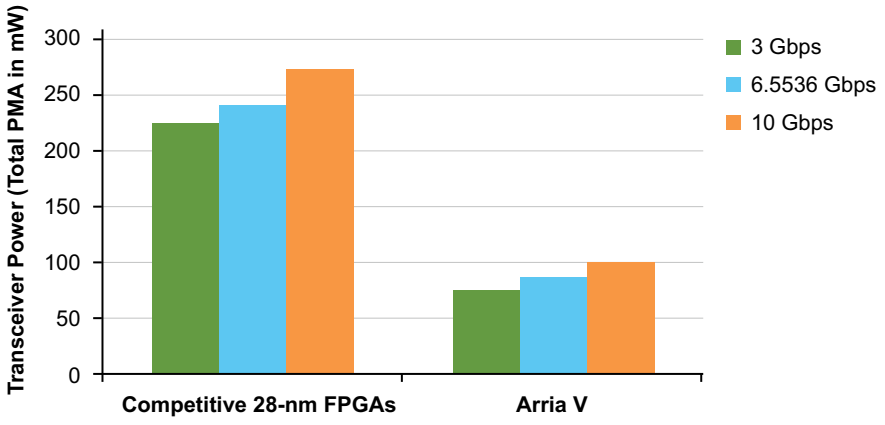
music, mobile TV, GPS navigation, along with traditional phone and texting services. Active usage power consumption is now a much larger factor in battery life. SiON gate technology, because of its smaller gate capacitance and therefore lower active power than HKMG (high-K metal gate), provides a solution with lower total power, cost, and risk for power-limited applications."

The 28LP process features low gate capacitances to reduce active power gate capacitances that are 30% lower than 28HPL. In Cyclone V and Arria V devices, Altera also adopted other strategies to reduce device capacitance, including high reliance on hard IP for memory controllers, PCI Express, and transceiver protocol support to reduce die area and its associated capacitance. Finally, Altera has also made significant optimizations to the basic architectural blocks of the Cyclone V and Arria V devices, as compared to Stratix V devices. These optimizations reduce silicon area and associated capacitance, and tune the 28LP-based device families for the performance required by their target applications. For example, a Logic Array Block (LAB, a collection of 10 Adaptive Logic Modules) in an Arria V device is 40% smaller in die area than the Stratix V LAB. The hard memory controllers featured in Cyclone V and Arria V devices similarly reduce the die area and associated capacitance of the external memory interface function. All of these reductions in device capacitance translate to lower dynamic power via the familiar power equation below, where *C* represents the capacitance of the switching circuit:

$$\text{Dynamic Power} = 1/2CV^2 \times f$$

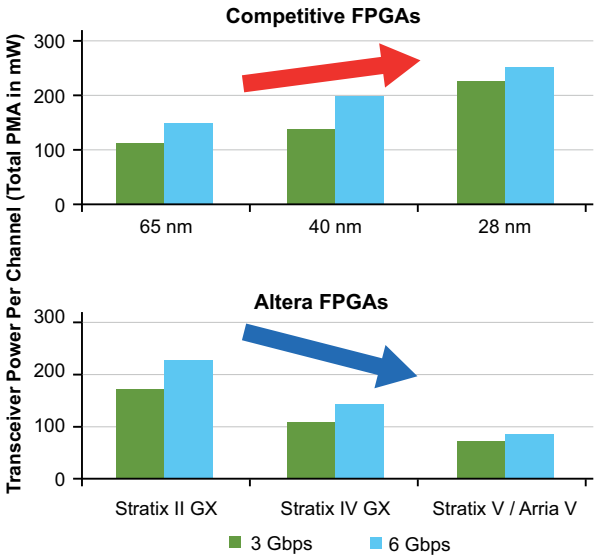
Altera has also reduced dynamic power in device transceivers. Altera's extensive transceiver design expertise is unmatched in the industry, and this unique advantage is reflected in the low dynamic power consumption of its transceivers. For example, at 6.5536 Gbps, Arria V transceivers consume less than 100mW of power, significantly lower than transceivers in 28-nm competitive FPGAs, as shown in Figure 6. For designs that utilize the up to 36 transceivers available in Arria V devices, the power savings is over 5 W.

Figure 6. Transceiver Total Power per Channel at 6.5536 Gbps at 85C Junction



Altera's low transceiver power at the 28-nm node is the result of over a decade of honing and enhancing proprietary architecture. This continuous, extensive experience with advanced transceiver technology is unmatched in the programmable logic industry and results in a historical trend of steady power reduction over time. Competitive solutions have a record of increasing transceiver power with each product generation, as shown in Figure 7, which graphs the power of the transceiver physical media attachment (PMA) across multiple generations of FPGAs.

Figure 7. Historical Trend in Transceiver Power



These static and dynamic power optimizations result in Altera 28LP-based FPGAs that consume up to 40% less total power than the prior generation of devices, with reductions across all areas of power consumption, as shown in Figure 8.

Figure 8. Cyclone V Power Reductions

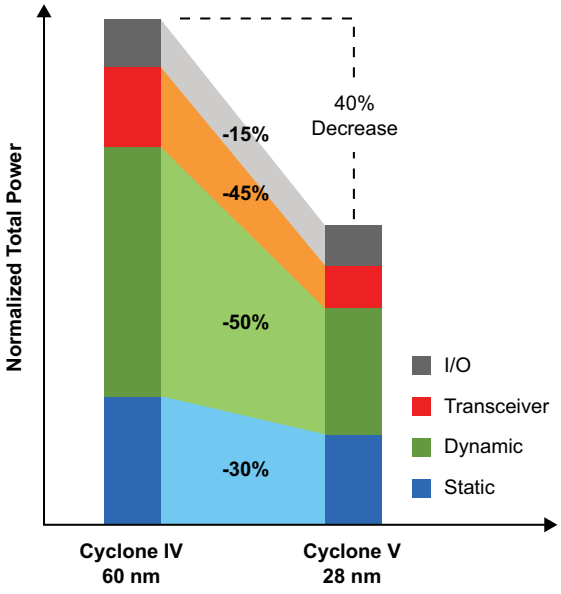
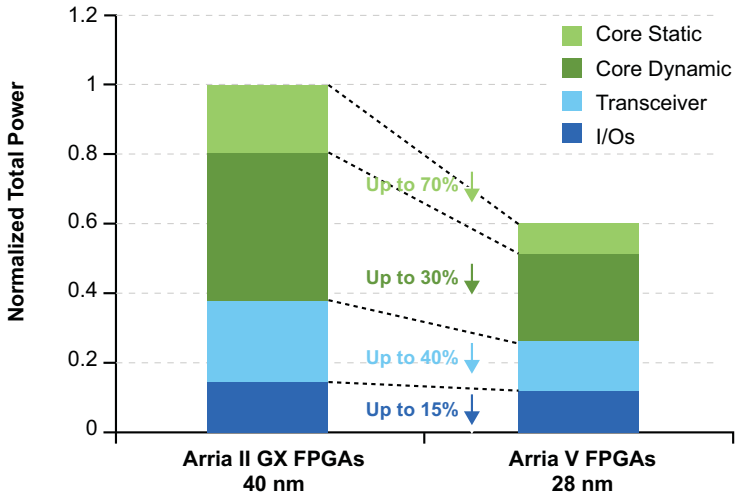


Figure 9 shows similar results for Arria V devices.

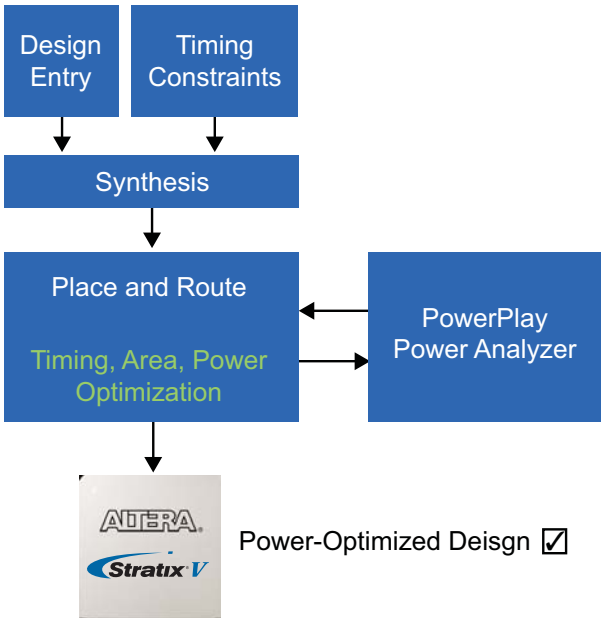
Figure 9. Arria V Power Reductions



Power Optimization through Software Innovation

In addition to process and architectural innovations, Altera has made many investments in software power optimization in Quartus II software. Power-driven compilation focuses on reducing the design's total power consumption using power-driven synthesis and power-driven place-and-route. This power reduction method is transparent to designers and enabled through simple compilation settings. The design engineer simply sets the timing constraints as part of the design entry process and synthesizes the design to meet performance. The Quartus II software automatically selects the required performance for each functional block as well as minimizes power through power-aware placement, routing, and clocking, as illustrated in Figure 10.

Figure 10. Quartus II Design Flow Including Automatic Power Optimization



The Quartus II software performs various compilation stages to minimize total power of designs. At the synthesis stage, the Quartus II software extracts clock-enable signals for clock gating, minimizes RAM blocks accessed, and restructures logic to eliminate high-toggling nets. At the fitter stage, the Quartus II software localizes high-toggling nets to reduce dynamic power, optimizes logic placement to reduce clock power, and implements power-efficient DSP and RAM block configurations. Finally, at the assembler level, the Quartus II software programs unused circuitry to minimize toggling or power down when possible. The resulting design meets the designer's timing requirements with the minimum power.

As shown in Table 1, the designer has the option to select different levels of power optimization to meet the design constraints. Selecting the **Extra Effort** setting offers the greatest power savings at the expense of longer compilation times. Results vary based on design and effort level selected. This feature reduces power without designer intervention, while having minimal impact on design performance. In addition, the power optimization is guided by detailed models of the circuitry and by advanced statistical techniques that estimate which signals are toggling the most often. This information allows Altera to determine power-efficient implementations without extra input from the designer (such as a time-consuming simulation of the design to determine switching rates).

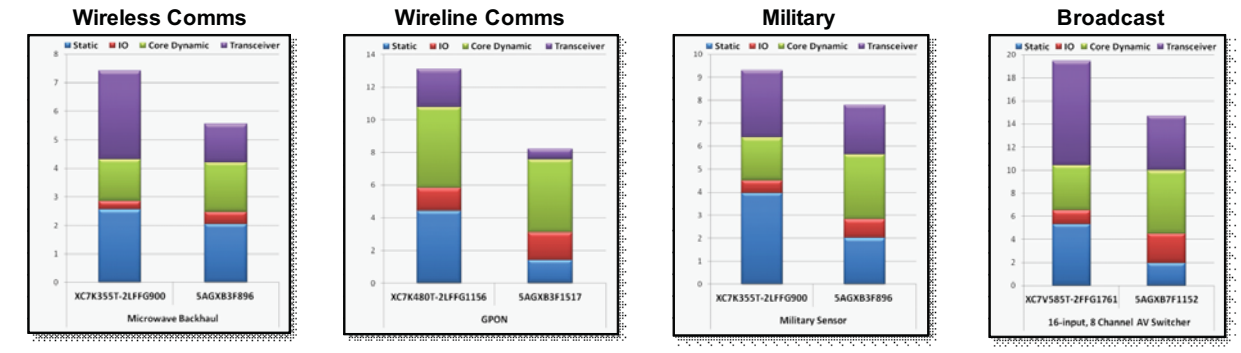
Table 1. Power Optimization Settings in Quartus II Software

Setting	Description
Off	Not netlist, routing, or performance optimizations are performed to minimize power.
Normal	Low compute effort algorithms are applied to minimize power through netlist optimizations, as long as they do not reduce design performance.
Extra Effort	High compute effort algorithms are applied to minimize power through netlist optimizations. Maximum performance may be affected.

Benchmarks

Altera provides the most advanced, lowest power-consuming FPGAs available in the industry. Benchmarks estimating total power for various representative applications further demonstrate the low-power advantage that Arria V devices deliver over their 28-nm competition. Figure 11 shows the result of some of these benchmarks, all of which are documented on Altera's wiki site for further study.

Figure 11. Arria V FPGAs vs. 28-nm Competition on Total Power



Conclusion

The benefits of Altera's low-power 28-nm devices include lower product costs, lower or relaxed power budgets, fewer thermal restrictions, the ability to address more markets, and options to increase capability within the same thermal/power budget. With this comprehensive approach to power reduction in 28-nm products, Altera enables designers to address the stringent demands of the power imperative.

Further Information

- *Reducing Power Consumption and Increasing Bandwidth on 28-nm FPGAs*
  www.altera.com/literature/wp/wp-01148-stxv-power-consumption.pdf

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Acknowledgements

- Martin S. Won, Senior Member of Technical Staff, Altera Corporation.

Document Revision History

Table 2 lists the revision history for this document.

Table 2. Document Revision History

Date	Version	Changes
September 2012	2.1	■ Updated Arria V FPGA transceiver speed to 6.5536 Gbps
November 2011	2.0	■ Minor text edits ■ Updated Figure 5, Figure 6, and Figure 7 ■ Added Benchmarks section and Figure 11
April 2011	1.1	Corrected minor typographical errors.
March 2011	1.0	Initial release.