White Paper

3-Gbps SDI Video (SMPTE 424M)

Introduction

The movie industries are creating more and more high-definition (HD) video content for distribution to meet an increasing demand from consumers. The current practice in recording studios for supporting an HD 1080p format is to use a dual-link connection (SMPTE 372) from the cameras to the mixing and recording equipment. Dual-link connections require twice the number of cables as single-link connections, resulting in increased equipment cost and increased complexity within the studio facility. A committee of the Society of Motion Picture and Television Engineers (SMPTE) is working to finalize a single-link, 1080p-capable standard called SMPTE 424M. This new standard will simplify hardware design while reducing cost and facility setup complexity. This standard provides a means of transporting an uncompressed digital video stream using two high-definition, serial-digital-interface (HD-SDI, or SMPTE 292M) data structures, each running at 1.485 Gbps and resulting in a single 2.970-Gbps video link interface, or 3-Gbps SDI in short form. SMPTE 424M is currently defined in the initial trial version as the committee works toward the 3-Gbps SDI standardization. This paper describes Altera's implementation of a 3-Gbps SDI video interface supporting the new standard.

High Definition Defined

HD is defined as 1920x1080 pixels or 2 megapixels per frame. The two types of HD video are interlaced video and progressive video. Table 1 summarizes some of the common video formats.

Table 1. HD Video Formats

Format	Scan Type	Active Lines	Active Horizontal Pixels	Data Rate (Gbps)	Main Application	SDI Link
1080p60	Progressive	1080	1920	2.970	HD for film	Dual
1080p59.64	Progressive	1080	1920	2.970/1.001	HD for film	Dual
1080p50	Progressive	1080	1920	2.970	HD for film	Dual
1080i60	Interlaced	1080	1920	1.485	TV networks	Single
1080p59.94	Interlaced	1080	1920	1.485/1.001	TV networks	Single
1080p50	Interlaced	1080	1920	1.485	European HD TV	Single
720p60	Progressive	720	1280	1.485	TV networks	Single
720p59.94	Progressive	720	1280	1.485/1.001	TV networks	Single
1035i60	Interlaced	1035	1920	1.485	Japanese TV	Single

The majority of today's video distribution system or video switcher/router uses HD-SDI at a data rate of 1.485 Gbps or 1.485/1.001 Gbps. The movie industry currently uses 3-Gbps SDI for video content distribution and storage, and it is gaining popularity with television networks. Eventually consumers will receive the 1080p version of HDTV.

Technology for 3-Gbps SDI Video Processing

Stratix® II GX FPGAs can support either the HD-SDI or 3-Gbps SDI serial data speeds on 4 to 20 full-duplex transceiver channels. The native frequency of operation ranges from 622 Mbps to 6.375 Gbps, and an oversampling technique is used for SD-SDI running at 270 Mbps. The transceiver circuitry on the Stratix II GX FPGA integrates hard-coded clock/data recovery (CDR) and serializer-deserializer (SERDES) functions. To eliminate clock-to-data skew, the CDR circuit on the FPGA uses an external reference clock to train its voltage-controlled oscillator (VCO) loop to recover a clock that is both phase and frequency aligned with incoming data.

Figure 1 shows a typical system requirement for 3-Gbps SDI.

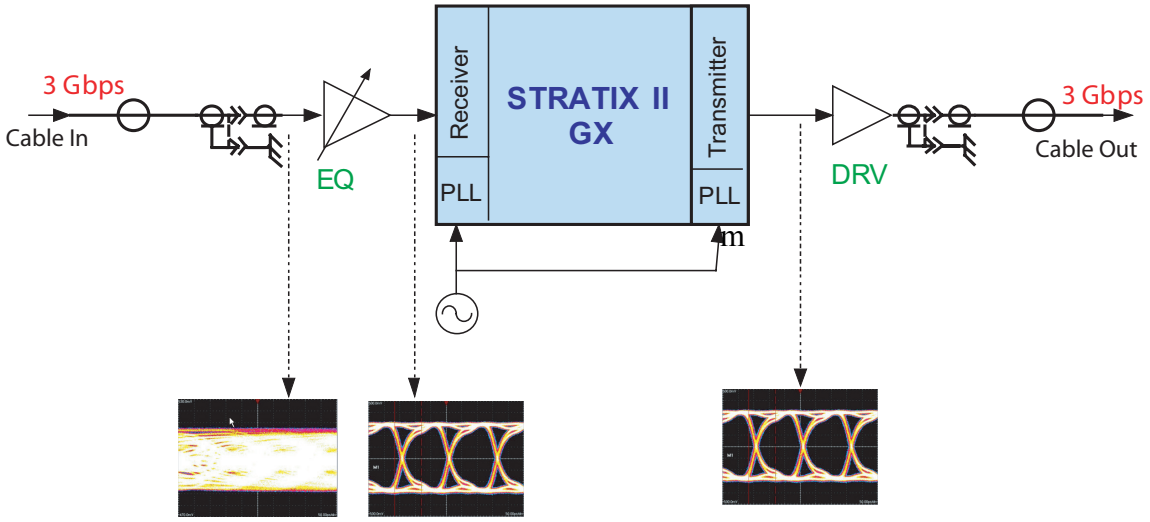

Figure 1. System Configuration

The transceiver converts the high-speed serial data to a slower 20-bit parallel data format that can be processed in the FPGA core on the receiving side. The FPGA uses its internal memory and DSP blocks to implement embedded audio demultiplexing, video switching/rerouting, or video processing. The processed data can also be converted back to a high-speed serial signal on the transmitting side of the transceiver. For better noise-filtering performance, both the receiving and transmitting phase-locked loops (PLLs) use true analog PLL circuitry.

The physical interface into the FPGA's transceivers requires an external cable equalizer and cable driver for the Belden 1694A 75-Ω coaxial cable. The cable length can run between 100 to 300 meters depending on the data rate. The cable equalizer is a complex analog component that automatically adapts to the cable length to restore the serial data's eye diagram opening after the dispersive signal loss from the cable's length. On the transmitting side, the cable driver must have enough drive current to handle the load of the long coaxial cable.

Multirate SDI MegaCore

The multirate SDI MegaCore® includes all the receive and transmit building blocks for the three key data rates of 270 Mbps, 1.485 Gbps, and 2.970 Gbps. The receive block has the CRC decoder, the line-number extraction, video framing and timing extraction, and format detector. The transmit block is comprised of the CRC encoder and line number insertion. The legacy SD-SDI block includes the word scrambler for the transmitting side and the word alignment with descrambling for the receiving side. Figure 2 shows the block diagram of the multirate SDI MegaCore.

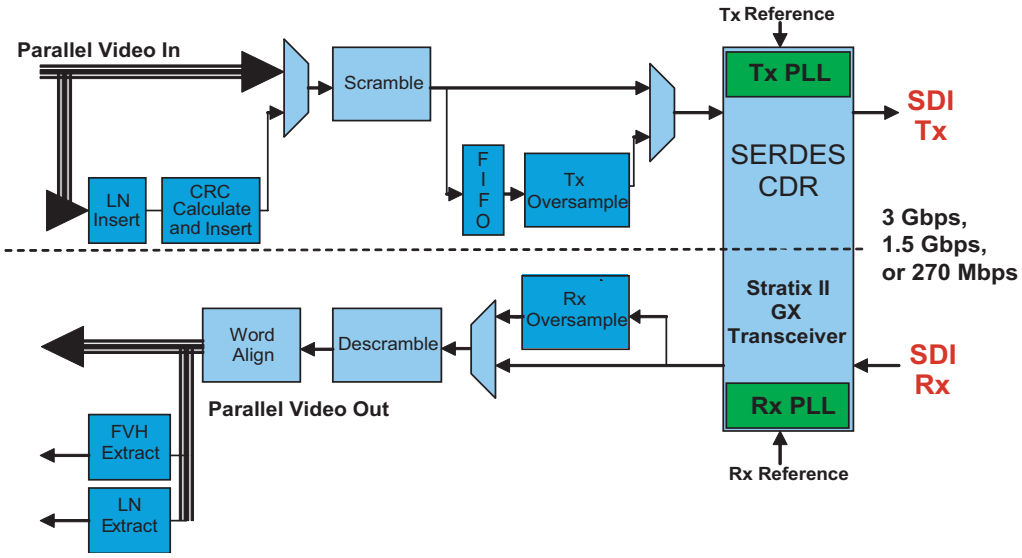

Figure 2. SDI MegaCore Block Diagram

Designing for 3-Gbps SDI

Some of the challenges in designing a clean 3-Gbps SDI system are layout and the high-speed signal integrity design rules set forth by the IC vendors. The transceiver and PLL portions of an FPGA must be powered by separate linear voltage regulators with sufficient drive current. Two types of decoupling are used: bulk decoupling for low frequency noise and local decoupling for high frequency noise. The amount of bulk decoupling depends on the number of outputs switching from the FPGA, load capacitance, slew rate, and inductance of the PCB plane and routing traces. The placement of the decoupling capacitors and its traces must be kept as short as possible without creating any unwanted series inductance. There should be separate power and ground planes for the sensitive analog circuitries. Strict transmission line routing guidelines must also be carefully followed.

Conclusion

A 3-Gbps SDI system will reduce cost and simplify hardware design for broadcast equipment manufacturers. In combination, Altera® Stratix II GX FPGAs and the off-the-shelf ASSP cable equalizer and driver provide a complete 3-Gbps SDI solution. 3-Gbps SDI solutions have been submitted by a number of IC vendors to ITU and SMPTE, so it looks likely to become the next serial video standard.

Further Information

- Using Stratix GX in HDTV Video Production Applications
  www.altera.com/literature/wp/wp_hdtv.pdf
- SDI Reference Design
  www.altera.com/end-markets/refdesigns/sys-sol/broadcast/ref-sdi.html
- SDI With Stratix GX
  www.altera.com/literature/an/an339.pdf

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