Basic Boundary-Scan Test Troubleshooting Guideline

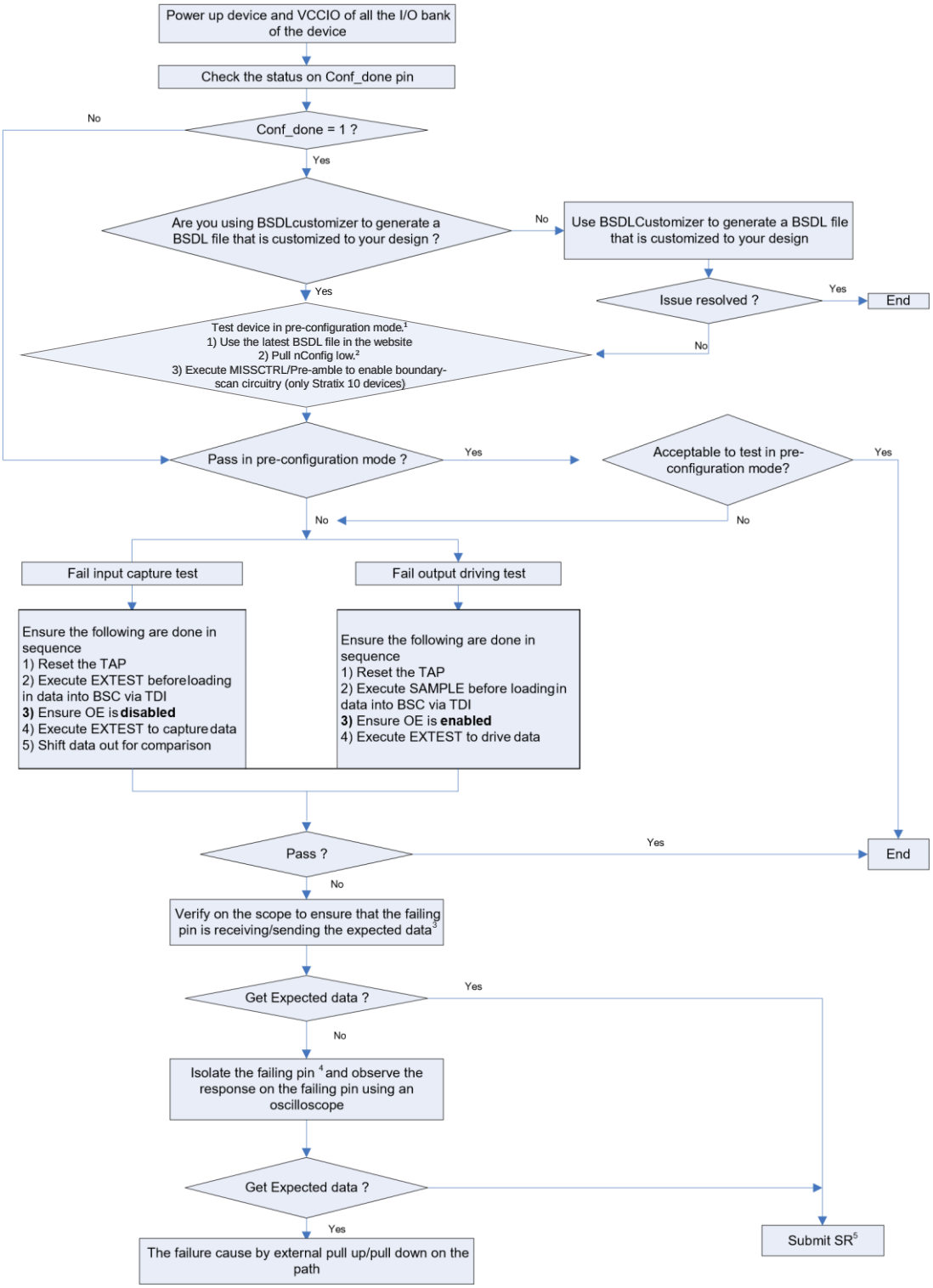
Introduction

This guideline helps you troubleshoot in the event a device fails the boundary scan test using BSDL file (can be downloaded from Intel's website) prior to seeking technical assistance from Intel PSG.

A checklist is also provided to assist you in troubleshooting the BST failure seen.

In the BST troubleshooting flow, it is assumed that

1) The device under test is mounted properly and there is no continuity issue
2) TAP controller advances to the proper state
3) Signals on the JTAG lines are clean
4) You do not to invoke the private instructions documented in the BSDL file at any time as these private instructions may render the device inoperable.



BST Troubleshooting Flow

Note :

1) If the device passes the BST in pre-configuration mode, we can conclude that the failing pin is not accidentally pulled up or down. If you are not able to test the design in pre-configuration mode, please submit SR and state the reason.
2) For Arria 10 and Cyclone 10 GX device, you need to pull nCONFIG to high and wait for nSTATUS goes high after power up. Once the JTAG circuitry is enabled, you may pull nCONFIG to low to perform BST in pre-configuration mode.
3) This is to ensure that valid data is present at the pins for input capturing or output driving test.
4) This includes removing all the external components that may present on the failing pins (e.g. pull up/pull down resistors, other chips in the chain). Purpose is to ensure that the failing pins are not accidentally pulled up or down by external circuitry.
5) To reduce the time for gathering information that is required to understand the issue, it is advised to provide the following information when submitting SR.
    a) complete list of the failing pins and the test that the pins failed
    b) What are the JTAG instructions used (e.g. SAMPLE,EXTEST)
    c) Description of the scan chain and configuration mode (setting on the MSEL pins)
    d) Steps taken in debugging and the results
    e) Pin file and the design file if you are performing BST in post configuration.
    f) Schematic diagram showing the VCCIO, Vref and the connections of the failing pins.
    g) Information for the BST tool that you used.
    h) Scope shots for the failing pins.

Checklist for BST Troubleshooting

Items	Checked
1. Are you using BSDL file that is downloaded from Intel Website? *Note: Use the latest BSDL file from Intel Website.*	
2. If you are testing the device in pre-configuration mode, do you use pre-configuration BSDL file? *Note: For pre-configuration BST, a pre-configuration BSDL file is needed. Use BSDL file from Intel Website directly for Pre-Configuration BST.*	
3. If you are testing the device in post-configuration mode, do you use the post-configuration BSDL file? *Note: For post-configuration BST, a post-configuration BSDL file is needed. Use Post-Configuration BSDL Generator from Intel Website to generate post-configuration BSDL using pre-configuration BSDL file available in Intel Website. Refer to BSDLFAQ question 11 for more information regarding to post-configuration BSDL.*	
4. Have you powered up the VCCIO for each of the I/O bank? *Note : VCCIO powers the I/O buffers of an I/O bank. If VCCIO of an I/O bank is not powered up, you are not able to capture or drive any signal on the I/O pins in that I/O bank.*	
5. Have you checked and ensured that signals on the JTAG lines are clean? *Note: Noisy JTAG lines put the TAP controller into a wrong state, causing BST failure*	
6. Have you checked and ensured that the PCB netlist used for generating test vector is correct? *Note: Please check the netlist and make sure the sequence of the devices in the JTAG chain is correct*	
7. If you are testing the device in pre-configuration mode, have you pulled nConfig low externally and verified CONF_DONE is low? *Note: Pulling nConfig pin to low ensures the flash memory is reset. Checking CONF_DONE pin can determine if the device has been configured.*	
8. When you perform output driving test, are you carrying it out in the sequence that is shown in the troubleshooting flow? *Note: This is the sequence used in factory for verifying the output driving test*	
9. When you perform input capture test, are you carrying it out in the sequence that is shown in the troubleshooting flow? *Note: This is the sequence used in factory for verifying the input driving test*	
10. If you have external pull up or pull down resistors on the failing pins, have you tried to perform BST with those resistors removed? *Note: This isolates if the failure seen is caused by external pull up or pull down resistors*	

11. On the pins that failed the input capture test, have you verified on the pins using an oscilloscope that the device is receiving the expected data? *Note: It is important that valid data is present at the pin. This also verifies if the issue seen is due to the device not able to capture correctly or the other device in the chain is not driving the correct signal*	
12. On the pins that failed the output driving test, have you verified on the pins using an oscilloscope that the device is driving the expected data? *Note: This verifies if the device is not able to drive out signal or the other device in the chain is not able to capture correctly*	
13. Did you perform BST for HSSI pins (except Arria 10, Cyclone 10 GX and Stratix 10 devices) after configuration? *Note: BST on HSSI pins in Arria II GX, Arria V GX, Cyclone IV and Stratix V devices only supported in post-configuration mode*	
14. Have you powered up the HPS power rails for SoC devices? *Note: For SoC devices, you must power up both HPS and FPGA to perform Boundary Scan Test*	
15. Did you use two BSDL files for SoC devices which are available from Intel Website? *Note: For SoC devices, you need to use two BSDL files (one for FPGA JTAG and the other one for HPS JTAG). The BST on HPS pins are controlled by the FPGA JTAG pins, thus the* *BSDL file for FPGA JTAG contains all the pins' behavior information. Whereas the BSDL for HPS JTAG only contains the supported instruction for HPS*	
16. Did you perform BST only when nSTATUS goes high after power-up for Arria 10 and Cyclone 10 GX devices? *Note: In Arria 10 and Cyclone 10 GX devices, the JTAG circuitry will only be enabled when nSTATUS goes high after powered up. The nSTATUS will go high when the nCONFIG is set to '1'. Once the JTAG circuitry is enabled, you may pull nCONFIG pin, to low to perform BST before configuration*	
17. For pre-configuration BST in Stratix 10 Device, did you enable the boundary-scan circuitry? *Note: MISCTRL instruction **OR** pre-amble sequence is required to enable the boundary scan circuitry in Stratix 10 Device. Refer to the note pointer for each device in Intel Stratix 10 BSDL Website to check which requirement to be used.*	

Revision History

Revision	Date	Description of Change
1.00	05/31/2007	Initial Release
1.01	01/09/2008	• Update introduction to ensure customer does not invoke private instructions that are documented in the BSDL file • Update the checklist for BST troubleshooting
1.02	07/16/2012	• Update checklist for post-configuration BSDLfile
1.03	12/27/2017	• Update the checklist for BST troubleshooting
1.04	3/25/2019	• Update the BST Troubleshooting Flow to include MISCTRL/Pre-amble in Stratix 10 devices • Rearrange the sequence Checklist for BST Troubleshooting • Update point in BST Troubleshooting Checklist, "for pre-configuration BST, a pre-configuration BSDL file is needed". • Change www.altera.com to Intel Web • Add MISCCTRL/Pre-amble in BST Troubleshooting Checklist • Update sentence "**For post-configuration BST, a post-configuration BSDL file is needed. Refer to BSDLFAQ question 11 for generating the post-configuration BSDL file.**" to "**For post-configuration BST, a post-configuration BSDL file is needed. Use Post-Configuration BSDL Generator from Intel Website to generate post-configuration BSDL using pre-configuration BSDL file available in Intel Website. Refer to BSDLFAQ question 11 for more information regarding to post-configuration BSDL.**"