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## High-Speed Board Design Advisor

### *High-Speed Channel Design and Layout*

#### Introduction


This document contains a step-by-step tutorial and checklist with a best-practice set of guidelines for high-speed channel design and layout.

This document assumes familiarity with the following tools and support collateral:

- Altera® Stratix® II GX Handbook:  
[www.altera.com/literature/lit-s2gx.jsp](http://www.altera.com/literature/lit-s2gx.jsp)
- Altera Stratix II GX Pinouts:  
[www.altera.com/literature/lit-dp.jsp](http://www.altera.com/literature/lit-dp.jsp)

Altera's Stratix II GX FPGA-based development kits deliver quality proven implementations and comprise board schematics, layout files, and board-specific guideline documents, which can be used as a starting point for user designs:


- Transceiver Signal Integrity Development Kit, Stratix II GX Edition:  
[www.altera.com/products/devkits/altera/kit-signal\\_integrity\\_s2gx.html](http://www.altera.com/products/devkits/altera/kit-signal_integrity_s2gx.html)
- PCI Express Development Kit, Stratix II GX Edition:  
[www.altera.com/products/devkits/altera/kit-pciexpress\\_s2gx.html](http://www.altera.com/products/devkits/altera/kit-pciexpress_s2gx.html)
- Audio Video Development Kit, Stratix II GX Edition:  
[www.altera.com/products/devkits/altera/kit-dsp-professional.html](http://www.altera.com/products/devkits/altera/kit-dsp-professional.html)

 Additional high-speed channel design-related net seminars and online lectures can be found in “[Further Information](#)”.

The demand for more system bandwidth has driven the definition of several new protocol-rich high-speed serial interconnects standards up to 6.375 Gbps. Today's challenge is managing the complexity of printed circuit boards (PCBs) while avoiding signal integrity problems associated with increased data rates and faster edge rates. Altera recommends working with the PCB vendor when assigning stack-up and selecting materials.

#### Define the Design Goal

- Specify the data rates and edge rate.
- Specify the number of channels
- Specify the length of the high-speed channels. This will determine the use of  $V_{OD}$ , equalization, and pre-emphasis, which allows Stratix II GX FPGAs to drive backplanes up to 50 inches.

 Refer to Section I, “Stratix II GX Transceiver User Guide,” of the Stratix II GX Handbook for further information about transceiver modes and features, pre-emphasis, and equalization:  
[www.altera.com/literature/hb/stx2gx/stxiigx\\_sii5v2\\_01.pdf](http://www.altera.com/literature/hb/stx2gx/stxiigx_sii5v2_01.pdf).

#### Design Steps for a High-Speed Differential Channel

##### *Selection of the Board and Trace Material, Control of Losses*

- Work closely with the PCB vendor for selection of materials
- There are various materials and types to choose from, (e.g., Rogers, Taconic, Polyclad, Park Nelco) with different values for loss tangent (dissipation factor,  $\tan \delta$ ) and dielectric constant (permittivity,  $\epsilon$ ). Refer to the PCB vendor for guidelines for:
  - Material selection

- Dielectric thickness selection (core material, pre-preg, impedance matching)
- Copper thickness selection
- Copper plating selection (e.g., rolled vs. electro-deposited)
- Choose loss tangent (dissipation factor,  $\tan \delta$ )
  - Low loss tangent provides lower losses, but don't pay extra for  $\tan \delta < 0.010$ .
  - Stratix II GX signal integrity features pre-emphasis and equalization compensate for high frequency losses up to 50 inches of FR-4 material and for data rates of 6.25 Gbps.
- Choose copper trace geometry
  - Use wide traces to minimize losses (skin effect, dielectric loss).
  - Use 5 mils < line width < 8 mils for FR-4.
- Choose dielectric constant (permittivity,  $\epsilon$ )
  - Considerations for selection: stability and accuracy of  $\epsilon$

### *Design a 100 $\Omega$ Impedance-Matched Channel*

- Route signals as edge-coupled differential pairs
  - Edge-coupled microstrip or stripline will allow the thinnest total PCB thickness while optimizing the via stub length
  - High-differential impedance easily achievable
  - Control length matching and routing through fine pitch holes
- Tight coupling gives higher interconnect density, allows fewer layers, and provides better noise immunity, but requires a certain dielectric thickness for impedance matching. Looser coupling is acceptable if density is not an important driver of a thinner dielectric.
- For lowest total dielectric thickness and reasonable interconnect density, use  $s = 2w$  (where  $s$  is spacing between differential line,  $w$  is line width)
- The impedance is dependant on:
  - Topology
  - Dielectric constant of PCB material
  - Dielectric height
  - Conductor width
  - Conductor thickness (small extent)
  - Consider impedance calculators
  - If spacing changes, line width should compensate
- For time or propagation delay, consider delay calculators
- Reference signal lines to at least one  $V_{SS}$  plane
- Use on-chip termination
- Remove the planes under any SMT launch pads to at least a depth equal to the pad diameter and equal to or greater than that used with DC blocking capacitors, connectors, and FPGA ball-grid array (BGA) breakout

### *How to Design the BGA Breakout*

- Use the rules for differential vias to design the BGA breakout
- Use large clearance holes (antipads) in the via stack


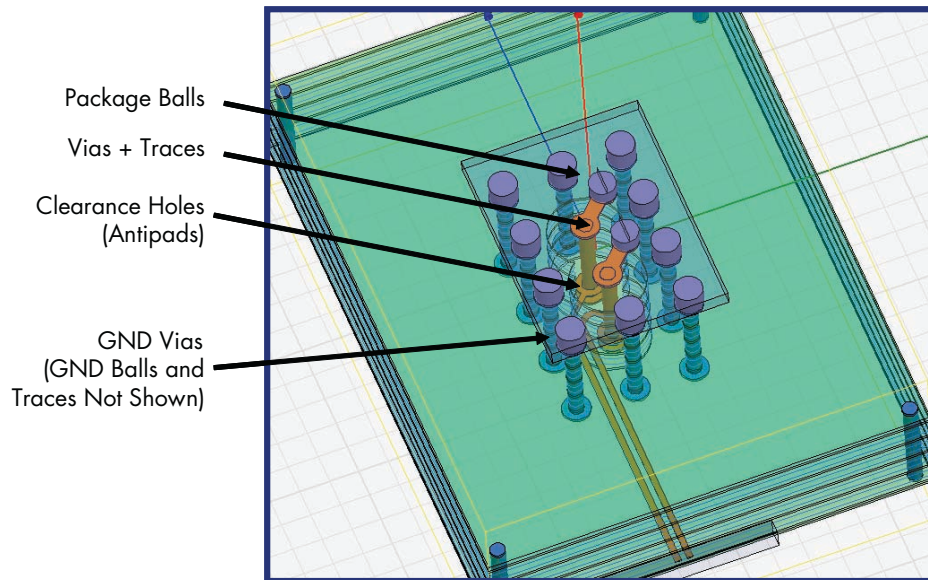
 For more information about package information for Stratix II GX devices, refer to the Stratix II GX Handbook, Volume 2, Section VII, "PCB Guidelines":  
[www.altera.com/literature/hb/stx2gx/stxiigx\\_sii5v2\\_07.pdf](http://www.altera.com/literature/hb/stx2gx/stxiigx_sii5v2_07.pdf)

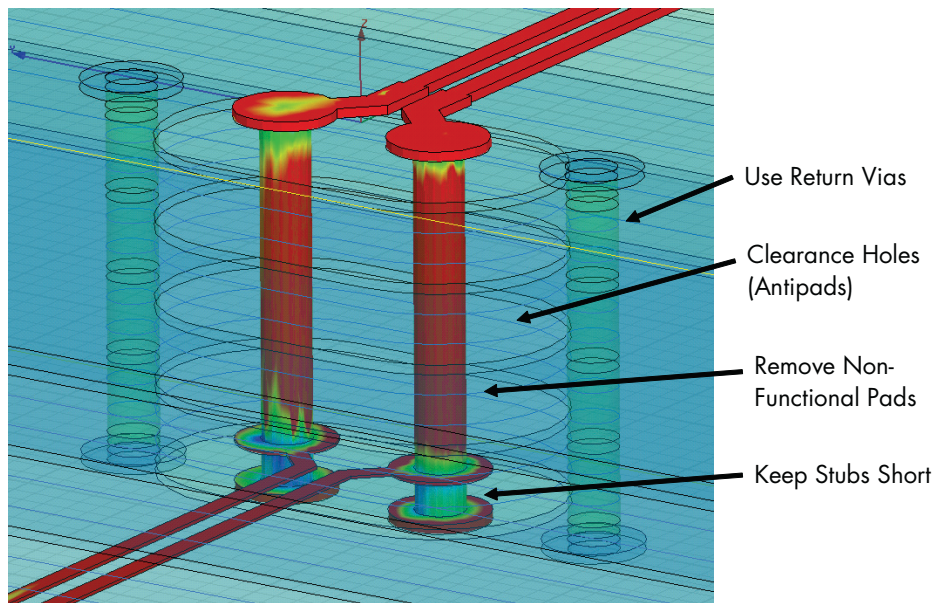
Figure 1. BGA Breakout Layout Example



### How to Design Optimal Differential Vias

- ❑ Use closely coupled impedance matched differential vias.
- ❑ Use a return via in close proximity to a signal via.
- ❑ Use as large a clearance hole (antipads) as possible in the via stack.
- ❑ Remove all non-functional pads (NFPs).
- ❑ Keep dangling stubs <50 mils by defining the top and bottom layers as differential signal layers, or use back-drilling of vias if stubs cannot be avoided.

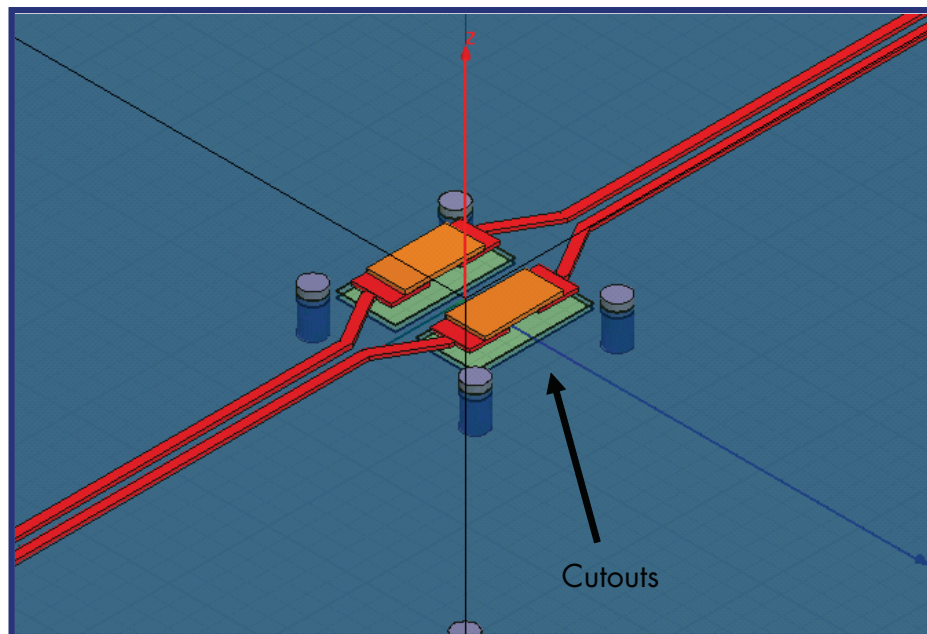
Figure 2. Optimal Differential Via Layout Example



### How to Design With DC Blocking Capacitors

- Use cutouts under the SMT launch pads to a depth at least equal to the pad diameter or within 10 mils under the capacitor.
- Use small form factor capacitors, no larger than 0402,  $C > 1$  nF.
- In general, it doesn't matter where the DC blocking capacitors are placed (on the Tx or Rx side). However, placing them towards the Rx side allows for better skew control between the DC blocking capacitors and the FPGA because of the shorter trace. The DC offset introduced by potential non-optimal skew before the DC blocking capacitors will be removed.

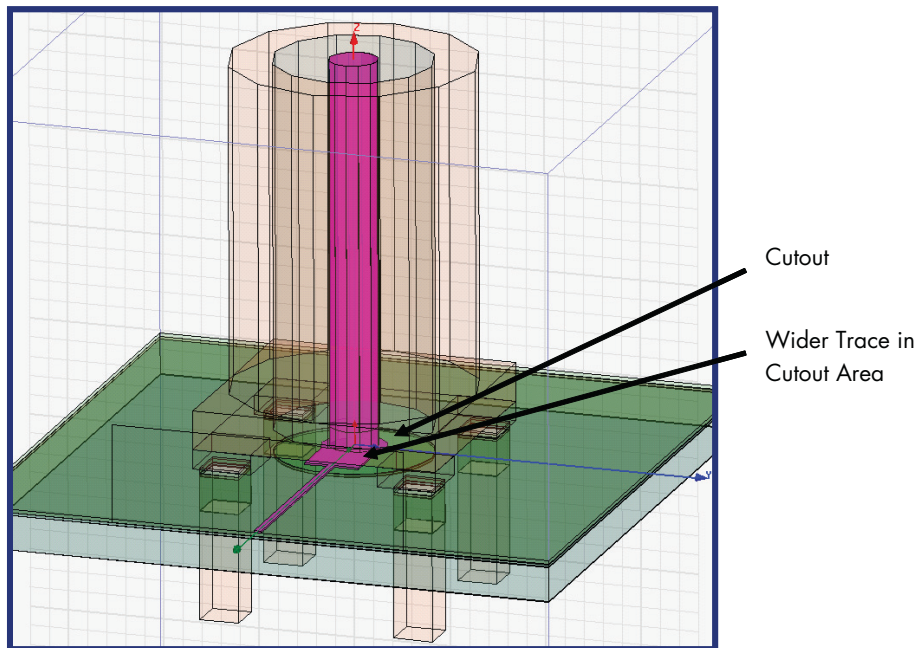
Figure 3. DC Blocking Capacitors Layout Example



### How to Design With Connectors

- Select connectors with  $<5\%$  impedance mismatch and  $<1\%$  cross talk (NEXT, FEXT)
- Use cutouts under the SMT launch pads to at least a depth equal to the pad diameter
- Widen the trace in the cutout area to match the impedance

Figure 4. SMA Connector Layout Example

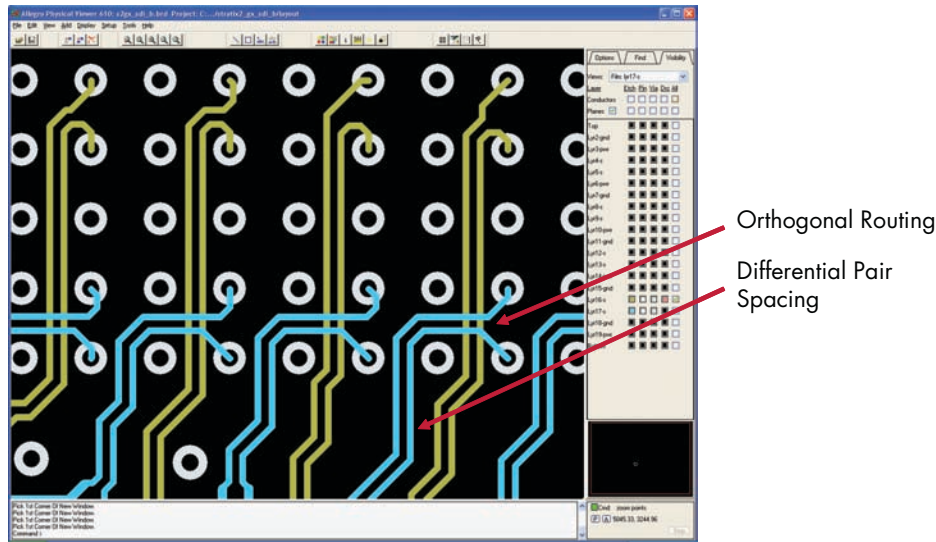


### How to Avoid Crosstalk

- ❑ Coupling is determined by geometry (trace separation, distance to ground(s), and parallel length).
- ❑ Use differential pairs
  - Provide lower crosstalk, lower radiation
  - Common mode noise rejection
  - Reduces ground reference problems
- ❑ Guidelines for differential pairs
  - Keep adjacent differential pair spacing  $> 3w$  (dielectric thickness)
  - Do not route Tx lines adjacent to Rx lines
  - Do not route pairs on adjacent layers co-parallel in broadside topology. Instead, use orthogonal routing on signal on different layers.



Figure 5. Layout Example of How to Avoid Crosstalk



### How to Control the Differential Skew

- ❑ Match line lengths to 20 mils.
- ❑ Keep the lines in a pair symmetric.
- ❑ Avoid a pitch for the two lines in a pair in the range 8 to 11 mils. Avoid signal pitch matching one-half glass wave pitch. Pitch should equal spacing between differential line plus line width.
- ❑ For loosely coupled pairs, traces can be moved away from each other.

### Routing Guidelines

- ❑ Use 45-degree angles (no 90-degree corners).
- ❑ No T-junctions greater than 250 mils
- ❑ No T-junctions for critical nets or clocks

### How to Use $V_{OD}$ , Equalization and Pre-Emphasis for Channel Optimization

- ❑ Altera's Transceiver Signal Integrity Development Kit, Stratix II GX Edition enables a thorough evaluation of Stratix II GX transceiver signal integrity and the transceiver performance from 600 Mbps to 6.375 Gbps: [www.altera.com/products/devkits/altera/kit-signal\\_integrity\\_s2gx.html](http://www.altera.com/products/devkits/altera/kit-signal_integrity_s2gx.html).
- ❑ Thousands of Stratix II GX eye diagrams are available with Altera's Eye Viewer: [www.altera.com/technology/signal/devices/stratix2gx/character/sgl-s2gx-character.html#siigxviewer](http://www.altera.com/technology/signal/devices/stratix2gx/character/sgl-s2gx-character.html#siigxviewer).
- ❑ Use Altera's pre-emphasis and equalization link estimator (PELE) technology to accelerate finding the optimal signal integrity settings. The PELE technology is available with Mentor Graphics® HyperLynx tools: [www.mentor.com](http://www.mentor.com).
- ❑ Plug and Play Signal Integrity is available in all production Stratix II GX FPGAs featuring adaptive dispersion compensation engine (ADCE) and hot-socketing: [www.altera.com/technology/signal/ppsi/sgl-plugin-and-play-si.html](http://www.altera.com/technology/signal/ppsi/sgl-plugin-and-play-si.html).

### Signal Integrity Modeling and Simulation Tool Vendors

- ❑ For IBIS and SPICE models, please refer to the Stratix II GX Signal Integrity Center: [www.altera.com/technology/signal/devices/stratix2gx/sgl-s2gx.html](http://www.altera.com/technology/signal/devices/stratix2gx/sgl-s2gx.html).

- Mentor Graphics HyperLynx features PELE, Altera's pre-emphasis and equalization link estimator technology: [www.mentor.com](http://www.mentor.com)

- Cadence:  
[www.cadence.com](http://www.cadence.com)
- Ansoft:  
[www.ansoft.com](http://www.ansoft.com)
- Agilent  
[www.agilent.com](http://www.agilent.com)
- CST:  
[www.cst.com](http://www.cst.com)

## Further Information

- Dr. Eric Bogatin's online lecture, "OLL-801 - Best Board Design Practices for High-Speed Serial Links":  
[www.bethesignal.com](http://www.bethesignal.com)
- Altera's Net Seminar Series: Optimizing High-Speed Serial Design:  
[www.altera.com/education/net\\_seminars/all/ns-optimize-high-speed-series06.html](http://www.altera.com/education/net_seminars/all/ns-optimize-high-speed-series06.html)
- *High-Speed Board Design Advisor: Power Distribution Network:*  
[www.altera.com/literature/tb/tb-092.pdf](http://www.altera.com/literature/tb/tb-092.pdf)
- *High-Speed Board Design Advisor: Thermal Management:*  
[www.altera.com/literature/tb/tb-093.pdf](http://www.altera.com/literature/tb/tb-093.pdf)
- *High-Speed Board Design Advisor: Pinout Definition:*  
[www.altera.com/literature/tb/tb-094.pdf](http://www.altera.com/literature/tb/tb-094.pdf)
- *High-Speed Board Design Advisor: Hardware Integration, Test, and Debug:*  
[www.altera.com/literature/tb/tb-096.pdf](http://www.altera.com/literature/tb/tb-096.pdf)



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