

3. ALTGX_RECONFIG Megafunction User Guide for Stratix IV Devices

SIV53004-3.1

You can use the ALTGX_RECONFIG MegaWizardTM Plug-In Manager in the Quartus[®] II software to create and modify design files for the Stratix[®] IV device family. This chapter describes the different Quartus II settings for dynamic reconfiguration in the ALTGX_RECONFIG MegaWizard Plug-In Manager.

The MegaWizard Plug-In Manager helps you create or modify design files that contain custom megafunction variations. These auto-generated MegaWizard files can then be instantiated in a design file. The MegaWizard Plug-In Manager allows you to specify options for the ALTGX_RECONFIG megafunction.

Start the MegaWizard Plug-In Manager using one of the following methods:

- Choose the MegaWizard Plug-In Manager command (Tools menu).
- When working in the Block Editor (schematic symbol), open the Edit menu and choose Insert Symbol. The Symbol dialog box appears. In the Symbol dialog box, click MegaWizard Plug-In Manager.
- Start the stand-alone version of the MegaWizard Plug-In Manager by typing the following command at the command prompt: qmegawiz.

Dynamic Reconfiguration

This section describes the options available on the individual pages of the ALTGX_RECONFIG MegaWizard Plug-In Manager.



The MegaWizard Plug-In Manager provides a warning if any of the settings you choose are illegal.

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Figure 3–1 shows the first page of the MegaWizard Plug-In Manager. To generate an ALTGX_RECONFIG custom megafunction variation, select **Create a new custom megafunction variation**. Click **Next**.

Figure 3–1. MegaWizard Plug-In Manager (Page 1)



Figure 3–2 shows the second page of the MegaWizard Plug-In Manager. Select the following options (click **Next** when you are done):

- 1. In the list of megafunctions on the left, click the "+" icon beside the I/O item. From the options presented, choose **ALTGX_RECONFIG megafunction**.
- 2. From the drop-down menu beside **Which device family will you be using**?, select **Stratix IV**.
- 3. From the radio buttons under Which type of output file do you want to create?, choose your output file format (AHDL, VHDL, or Verilog HDL).
- 4. In the box beneath **What name do you want for the output file?**, enter the file name or click the **Browse** button to search for it.
- For the design to compile successfully, always enable the dynamic reconfiguration controller for all the ALTGX instances in the design.





Figure 3–3 shows page 3 of the ALTGX_RECONFIG MegaWizard Plug-In Manager. From the drop-down menu, select the number of channels controlled by the dynamic reconfiguration controller.



MegaWizard Plug-In Manager [page 3	of 8]			
ALTGX_RECONFIG		_		
Toma e		E	About	Documentation
Parameter 2 EDA 3 Summary Settings Reconfiguration settings Analog controls Channel and TX	PLL reconfiguration > Error checks/Data rate switch	\rangle		
	Currently select	ted <u>d</u> evice family:	Stratix	IV 🗸
reconfig_clk reconfig_togxb[3.0] verte_all busy, verte_all channel_reconfig_done reconfig_mode_sel[3.0] reconfig_ddress_out[5.0] tx_vodctrl[5.0] aeq_togxb[23.0] rete_switch_ctrl[1.0] ctrl_readdata[15.0] reconfig_dddress_out[5.0] ctrl_waitrequest	What is the number of channels controlled by the recor Note : When the controller is used to drive multiple inst - The starting channel number of the alt4gxb ins and - The number of channels controlled is one more What are the features to be reconfigured by the recon	ifig controller? ances of the alt4gxl tances must be uniq than the last chann fig controller?	Matc 2 b megafund que and a m nel number.	h project/default channels tion, uultiple of 4,
aeq_fromgxb[70]	Reconfiguration mode	'reconfig_mode_s	sel'	~
ctrl_writedata[150]	☑ Analog controls	0000)	
ctrl_write	☑ Data rate division in TX	0011		
ctrl_read	☑ Channel and TX PLL select/reconfig			
	CMU PLL reconfiguration	0100)	
	Channel and CMU PLL reconfiguration	0101		
	Channel reconfiguration with TX PLL select	0110)	
	Central PCS reconfiguration	0111		
	Adaptive Equalization control			*
	reconfig_mode_self column indicates the value that net activate the specified reconfiguration mode. This is app selected.	eds to be set on the licable, only when n	e 'reconfig_r nultiple reco	mode_sel' port to onfig operations are
Resource Usage 1 att_aeq_s4 + 1 att_cal + 1 att_eyemon + 163 lut +				

Table 3–1 lists the available options on page 3 of the MegaWizard Plug-In Manager for your ALTGX_RECONFIG custom megafunction variation. Select the **Match project/default** option if you want to change the device **Currently selected device family** options.

Make your selections on page 3, then click Next.

	Table 3-1.	MegaWizard Plug-In Manager	Options (Page 3)	(Part 1 of 2)
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ALTGX_RECONFIG Setting	Description	Reference
	Determine the highest logical channel address among all the ALTGX instances connected to the ALTGX_RECONFIG instance. Round it up to the next multiple of four and set that number in this option.	
What is the number of channels controlled by the reconfig controller?	Depending on this setting, the ALTGX_RECONFIG MegaWizard Plug-in Manager generates the appropriate signal width for the interface signal (reconfig_fromgxb) between the ALTGX_RECONFIG and the ALTGX instances. It also gives the necessary bus width for all the selected physical media attachment (PMA) signals.	"Total Number of Channels Controlled by the ALTGX_RECONFIG Instance" section of the <i>Dynamic</i> <i>Reconfiguration in Stratix IV</i> <i>Devices</i> chapter
	Depending on the number of channels set, the resource estimate changes because this is a soft implementation that uses fabric logic resources. The resource estimate is shown in the bottom left of Page 3 of the MegaWizard Plug-in Manager.	

ALTGX_RECONFIG Setting	Description	Reference
	This feature is always enabled by default:	
	 Offset Cancellation for Receiver Channels—After the device powers up, the dynamic reconfiguration controller performs offset cancellation on the receiver portion of all the transceiver channels controlled by it. 	"Offset Cancellation" section of the <i>Dynamic Reconfiguration in Stratix IV Devices</i> chapter.
	These features are available for selection:	
	 Analog Controls—Allows dynamic reconfiguration of PMA controls such as Equalization, Pre-emphasis, DC Gain, and voltage offset differential (VOD). 	
	 Data rate division in TX—Allows dynamic reconfiguration of the transmitter local divider settings to 1, 2, or 4. The transmitter channel data rate is reconfigured based on the local divider settings. 	
	 Channel and TX PLL select/reconfig—The following features are available under this option: 	"PMA Controls Reconfiguration
What are the features to be reconfigured by the reconfig controller?	 CMU PLL Reconfiguration—Allows you to dynamically reconfigure the clock multiplier unit (CMU) phase-locked loop (PLL) to a different data rate. 	Mode Details" section, "Data Rate Division in Transmitter Mode Details" section, "CMU PLL Reconfiguration Mode Details"
	 Channel and CMU PLL reconfiguration—Allows the dynamic reconfiguration of the transceiver channel from one functional mode to another and also the CMU PLL reconfiguration. 	section, "Channel and CMU PLL Reconfiguration Mode Details" section, "Channel reconfiguration with TX PLL Select Mode Details" section, and the "Adaptive
	 Channel reconfiguration with TX PLL select— Allows you to select additional transmitter PLLs for the transceiver channel and reconfigure the functional mode of the channel. 	Equalization (AEQ)" section in the Dynamic Reconfiguration in Stratix IV Devices chapter.
	 Central Control Unit reconfiguration—Allows you to reconfigure bonded mode configurations from one to another. 	
	 Adaptive Equalization Control —Allows you to reconfigure the adaptive equalization hardware (AEQ) in the receiver portion of the transceivers. Enable one time mode for a single channel mode is a single stable equalization value is set up and locked for the specified channel by the AEQ hardware. 	
What are the features to be reconfigured by the reconfig controller?	• EyeQ control—Allows you to reconfigure the EyeQ hardware in the receiver portion of the transceivers.	"EyeQ" section in the <i>Dynamic</i> <i>Reconfiguration in Stratix IV</i> <i>Devices</i> chapter.

Table 3-1. MegaWizard Plug-In Manager Options (Page 3) (Part 2 of 2)

Figure 3–4 shows page 4 of the ALTGX_RECONFIG MegaWizard Plug-In Manager.



ALTGX_RECONFIG			About Documentation
Parameter 2 EDA 3 Summary Settings Analog controls Channel and T	X PLL reconfiguration > Error checks/D	ata rate switch 🔪	
reconfig_clk reconfig_togxb[3.0] reconfig_fromgxb[16.0] busy write_all channel_reconfig_done reconfig_mode_sel[3.0] reconfig_address_out[5.0]	 Use 'logical_channel_address' port All the channels will be updated wil asserted. Use the same control signal for all of The controller allows the dynamic reco through the use of dedicated control p checking its corresponding checkbox. 	for Analog controls reconfig h the current value of contr channels nfiguration and/or reading b orts, You may select to use	uration ol inputs when the write_all input is ack of the following analog settings any of these control ports by
tx voidcri[0] aed_togxb[230], rate_switch_ctrl[10] ctrl_readdata[150], reconfig_data[150] ctrl_waitrequest, logical_channel_address[0] aed_trongxb[70], ctrl_writedata[150] ctrl_waitrequest, ctrl_writedata[150] ctrl_readdata[150],	Setting Voltage Dutput Differential (VDD) Pre-emphasis control pre-tap Pre-emphasis control 1st post-tap Pre-emphasis control 2nd post-tap Equalizer DC gain Equalizer control	Write control Image: tx_vodctrl tx_preemp_0t tx_preemp_1t tx_preemp_2t rx_eqdcgain rx_eqdctl	Read control tx_vodctrl_out tx_preemp_0t_out tx_preemp_1t_out tx_preemp_2t_out rx_eqdcgain_out rx_eqctrl_out
Ctrl_address[150]			

Table 3–2 lists the available options on page 4 of the MegaWizard Plug-In Manager for your ALTGX_RECONFIG custom megafunction variation.

Make your selections on page 4, then click Next.

Table 3–2. MegaWizard Plug-In Manager Options (Page 4) (Part 1 of 2)

ALTGX_RECONFIG Setting	Description	Reference	
Use 'logical_channel_add ress' port for Analog controls reconfiguration	This option is applicable only for Analog controls reconfiguration and is available for selection when the number of channels controlled by the ALTGX_RECONFIG instance is more than one. The dynamic reconfiguration controller reconfigures only the channel whose logical channel address is specified at the logical_channel_address port. The width of this port is selected by the ALTGX_RECONFIG MegaWizard Plug-In Manager depending on the number of channels controlled by the dynamic reconfiguration controller. The maximum width of the logical_channel_address port is 9 bits.	"Dynamic Reconfiguration Controller Port List" and "Method 1—Using the logical_channel_address Port" sections of the <i>Dynamic</i> <i>Reconfiguration in Stratix IV</i> <i>Devices</i> chapter.	
Use the same control signal for all channels	This option is available for selection when the number of channels controlled by the ALTGX_RECONFIG instance is more than one. When you enable this option, the dynamic reconfiguration controller writes the same control signals to all the channels connected to it. You cannot select this option if you enable the Use 'logical_channel_address' port for Analog controls reconfiguration option.	Method 2 and Method 3 of the "PMA Controls Reconfiguration Mode Details" section of the <i>Dynamic Reconfiguration in</i> <i>Stratix IV Devices</i> chapter.	

ALTGX_RECONFIG Setting	Description	Reference
	The PMA control ports available to write various analog settings to the transceiver channels controlled by the dynamic reconfiguration controller are as follows:	
	 tx_vodctr1—V_{OD}; 3 bits per channel 	
	 tx_preemp_0t—Pre-emphasis control pre-tap; 5 bits per channel 	
	 tx_preemp_1t—Pre-emphasis control 1st post-tap; 5 bits per channel 	
	 tx_preemp_2t—Pre-emphasis control 2nd post-tap; 5 bits per channel 	
Write Control	rx_eqdcgain—Equalizer DC gain; 3 bits per channel	
	 rx_eqctrl—Equalizer control; 4 bits per channel 	
	These are optional signals. The signal widths are based on the setting you entered for the What is the number of channels controlled by the reconfig controller? option and whether you enabled the Use	
	reconfiguration option. The port width is also determined by the Use the same control signal for all channels option.	
	At least one of these PMA control ports must be enabled to configure and use the dynamic reconfiguration controller.	"Dynamically Reconfiguring PMA Controls" section of the <i>Dynamic</i> <i>Reconfiguration in Stratix IV</i>
	The PMA control ports available to read the existing values from the transceiver channels controlled by the dynamic reconfiguration controller are as follows:	<i>Devices</i> chapter.
	tx_vodctrl_out—V _{OD} ; 3 bits per channel	
	 tx_preemp_0t_out—Pre-emphasis control pre-tap; 5 bits per channel 	
	 tx_preemplt_out—Pre-emphasis control 1st post-tap; 5 bits per channel 	
	 tx_preemp_2t_out—Pre-emphasis control 2nd post-tap; 5 bits per channel 	
Read Control	rx_eqdcgain_out—Equalizer DC gain; 3 bits per channel	
	rx_eqctrl_out—Equalizer control; 4 bits per channel	
	These are optional signals. The signal widths are based on the setting you entered for the What is the number of channels controlled by the reconfig controller? option	
	and whether you enabled the Use	
	<pre>'logical_channel_address' port for Analog controls reconfiguration option.</pre>	
	The PMA controls are available for selection only if you select the corresponding write control. Read and write transactions cannot be performed simultaneously.	

Table 3–2. MegaWizard Plug-In Manager Options (Page 4) (Part 2 of 2)

Figure 3–5 shows page 5 of the ALTGX_RECONFIG MegaWizard Plug-In Manager.



MegaWizard Plug-In Manager [page 5 of ALTGX_RECONFIG I Parameter I B Summary	of 8]
Reconfiguration settings Analog controls Channel and TX P reconfig_clk reconfig_togxb[3.0] reconfig_fromgxb[16.0] data_valid reconfig_mode_sel[3.0] tx_vodctr[und[1.0] tx_vodctr[11.0] tx_preemp_0t_out[19.0] tx_reconfig_ndet[11.0] rx_eqctr[11.0] tx_eqctr[11.0] rx_eqctr[11.0] reconfig_addat[15.0] rdt_readdata[15.0] ctrl_wratedata[15.0] ctrl_wratequest ctrl_wratedata[15.0] otheress[1.0]	Lit reconfiguration Error checks/Data rate switch Channel reconfiguration is performed on a per channel basis. The channel to be reconfigured is specified by the value of logical_channel_address port. Channel reconfiguration is performed on a per channel basis. The channel to be reconfigured is specified by the value of logical_channel_address port. Channel reconfiguration is performed on a per channel basis. The channel to be reconfigured is specified by the value of logical_channel_address port. Channel reconfiguration are written in a single write cycle What is the read latency of the MIF contents? Use 'reconfig_address_out' The reconfig_address_out' The reconfig_address_en' The reconfig_address_en' The reconfig_address_en' The reconfig_address_en' Use 'reconfig_address' Asserting the reset_reconfig_address' Asserting the reset_reconfig_address' Assertion Use 'reconfig_address' to input address from the MIF in reduced MIF reconfiguration Use 'logical_tx_pll_sel The logical_tx_pll_sel port is used to select the logical PLL to be reconfigured in the PLL reconfiguration mode(s) and is used to select the PLL driving the channel in the channel reconfiguration with PLL select mode. Use 'logical_tx_pll_sel_en' The logical_tx_pll_sel_en' <
Resource Usage 1 alt_aeq_s4 + 1 alt_cal + 1 alt_eyemon + 265 lut + 309 reg	Cancel Sack Next > Finish

Table 3–4 lists the available options on page 5 of the MegaWizard Plug-In Manager for your ALTGX_RECONFIG custom megafunction variation.

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ALTGX_RECONFIG Setting	Description	Reference
Enable continuous write of all the words needed for reconfiguration.	For a continuous write operation, select the Enable continuous write of all the words needed for reconfiguration option to pulse the write_all signal once to write an entire memory initialization file (.mif).	"Dynamic Reconfiguration Controller Port List" section in the Dynamic Reconfiguration in Stratix IV Devices chapter.
What is the read latency of the MIF contents?	This option is available only if you have selected the Enable continuous write of all the words needed for reconfiguration option. Enter the desired latency in terms of the reconfig_clk cycles it takes for each .mif word to be present at the reconfig_data port. For more information, refer to Figure 3–6.	"Dynamic Reconfiguration Controller Port List" section in the Dynamic Reconfiguration in Stratix IV Devices chapter.

ALTGX_RECONFIG Setting	Description	Reference
Use 'reconfig_address_out'	This option is enabled by default when you select the Channel and TX PLL select/reconfig option. The value on reconfig_address_out[5:0] indicates the address associated with the words in the .mif , which contains the dynamic reconfiguration instructions. The dynamic reconfiguration controller automatically increments the address at the end of each .mif write transaction.	"Dynamic Reconfiguration Controller Port List" section in the <i>Dynamic Reconfiguration in</i> <i>Stratix IV Devices</i> chapter.
Use 'reconfig_address_en'	When high, this optional output status signal indicates that the address used in the .mif write transaction cycle has changed. This signal is asserted when the .mif write transaction is completed (when the busy signal is de-asserted).	"Dynamic Reconfiguration Controller Port List" section in the Dynamic Reconfiguration in Stratix IV Devices chapter.
Use 'reset_reconfig_address'	When asserted, this optional control signal resets reconfig_address_out (the current reconfiguration address) to 0 .	"Dynamic Reconfiguration Controller Port List" section in the Dynamic Reconfiguration in Stratix IV Devices chapter.
	This is an optional control signal. The logical_tx_pll_sel[1:0] signal refers to the logical reference index of the CMU PLL. The functionality of the signal depends on the feature activated, as shown below:	
	 CMU PLL reconfiguration—The corresponding CMU PLL is reconfigured based on the value at logical_tx_pll_sel[1:0]. 	"Guidelines for logical_tx_pll_sel and logical_tx_pll_sel_en Ports"
	 Channel and CMU PLL reconfiguration—The corresponding CMU PLL is reconfigured based on the value at this signal. The transceiver channel listens to the CMU PLL selected by logical_tx_pll_sel[1:0]. 	<i>Reconfiguration in Stratix IV</i> <i>Devices</i> chapter.
	Channel reconfiguration with TX PLL select— The transceiver channel listens to the TX PLL selected by logical_tx_pll_sel[1:0].	
Use 'logical_tx_pll_sel_en'	This is an optional control signal. When you enable this signal, the value set on the logical_tx_pll_sel[1:0] signal is valid only if the logical_tx_pll_sel_en is set to 1 .	"Guidelines for logical_tx_pll_sel and logical_tx_pll_sel_en Ports" section in the <i>Dynamic</i> <i>Reconfiguration in Stratix IV</i> <i>Devices</i> chapter.

Table 3–3. MegaWizard Plug-In Manager Options (Page 5) (Part 2 of 2)

Figure 3–6 shows that the read latency of the .mif contents is 2, as it takes two reconfig_clk cycles for the .mif data to become available on the reconfig_data port after providing address on the reconfig_address_out port.



Figure 3–6. Read Latency

Figure 3–7 shows page 6 of the ALTGX_RECONFIG MegaWizard Plug-In Manager.



ALTGX_RECONFIG	About Documentation
Parameter 2 EDA 3 Summary Settings configuration settings Analog controls Channel and TX PLL	reconfiguration > Error checks/Data rate switch >
reconfig_clk reconfig_togxb[3.0] read data_valid gead busy reconfig_mode_sel[3.0] tx_vodctr_out[11.0] tx_vodctr_out[19.0] tx_preemp_0t_out[19.0] tx_preemp_2t[19.0] rx_eqdcgain_out[11.0] tx_eqdcgain[15.0] rx_eqdtr_out[15.0] rate_switch_out[15.0] rate_switch_out[15.0] ctr_writedata[15.0] ctr_readdata[15.0] ctr_address[15.0] ctr_waitrequest	 Enable lilegal mode checking When lilegal mode check is enabled, the controller will check for illegal inputs and recover from them. The output port 'error' will be driven high when illegal inputs are specified. Enable self recovery When self recovery is enabled, the controller will automatically recover and quit an operation if the operation didn't complete within the expected time. The output port 'error' will be driven high whenever self recovery happens. Data rate switch Data rate switch Data rate division is performed on a per channel basis. The channel to be reconfigured is specified by the value of the logical_channel_address port. A value of '00' on 'rate_switch_ctrl' specifies a division of 1, '01' specifies a division of 2 and '10' specifies a division of 4 Y Use 'rate_switch_out' port to read out the current data rate division Lise 'rat_bayes' port to enable RX only, TX only or duplex reconfiguration A value of '00' on 'rat_bayes' port settings only and '10' TX settings only
Resource Usage 1 alt_aeq_s4 + 1 alt_cal + 1 alt_eyemon + 285 lut +	

Table 3–4 lists the available options on page 6 of the MegaWizard Plug-In Manager for your ALTGX_RECONFIG custom megafunction variation.

Make your selections on page 6, then click Next.

Table 3–4. MegaWizard Plug-In Manager Options (Page 6)

ALTGX_RECONFIG Setting	Description	Reference
Enable illegal mode checking	When you select this option, the ALTGX_RECONFIG MegaWizard Plug-In Manager provides the error output port. The dynamic reconfiguration controller detects the error conditions within two reconfig_clk cycles, de-asserts the busy signal, and asserts the error signal for two reconfig_clk cycles.	"Error Indication During Dynamic Reconfiguration" section of the <i>Dynamic Reconfiguration in</i> <i>Stratix IV Devices</i> chapter.
Enable self recovery	When you select this option, the controller automatically recovers if the operation did not complete within the expected time. The error signal is driven high whenever the controller performs a self recovery.	"Error Indication During Dynamic Reconfiguration" section of the <i>Dynamic Reconfiguration in</i> <i>Stratix IV Devices</i> chapter.
Use rate_switch_out port to read out the current data rate division	The rate_switch_out[1:0] signal is available when you select Data Rate Division in TX mode. You can read the existing local divider settings of a transmitter channel at this port. The decoding for this signal is listed below: 2'b00—Division of 1 2'b01—Division of 2 2'b10—Division of 4 2'b11—Not supported	"Data Rate Division in Transmitter Mode Details" mode section in the <i>Dynamic Reconfiguration in</i> <i>Stratix IV Devices</i> chapter.
Use the rx_tx_duplex_sel port to enable RX only, TX only or duplex configuration	You can read or write the receiver and transmitter settings, only the receiver settings, or only the transmitter settings, based on the value you set at the rx_tx_duplex_sel[1:0] port; 2'b00—Duplex mode 2'b10—TX only mode 2'b10—TX only mode 2'b11—unsupported value (do not use this value) If you disable the rx_tx_duplex_sel[1:0] port, the dynamic reconfiguration controller reads or writes both the receiver and transmitter settings.	"Dynamically Reconfiguring PMA Controls" section of the <i>Dynamic</i> <i>Reconfiguration in Stratix IV</i> <i>Devices</i> chapter.

Figure 3–8 shows page 7 (the Simulation Libraries page) of the MegaWizard Plug-In Manager, which is used for dynamic reconfiguration selection.

Make your selections, then click Next.

Fiyure 5–0. meyawizaru Fiuy-ili mallayer—AltuA_necomfiu (Sililulatioli Librati	Figure 3–8	8. MegaWizard Plu	g-In Manager–	-ALTGX_RECONFIG	(Simulation Librarie
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egaWizard Plug-In Manager [page 7 of	[8] EDA
ALTGX_RECONFIG	<u>About</u> <u>D</u> ocumentation
	Simulation Libraries To properly simulate the generated design files, the following simulation model file(s) are needed
reconfig_clk reconfig_togxb[30] reconfig_fromgxb[160] data_valid read busy, write_all tx_vodctri_out[110] tx_vodctri[110] tx_preemp_0t_out[190] tx_preemp_0t[190] tx_preemp_1t_out[190] tx_preemp_0t[190] tx_reqdcgain_out[110] tx_preemp_1t[10.0] rx_eqdcgain_out[110] tx_preemp_2t[190] rx_eqdcgain_out[110] rx_eqctri_out[150] rate_switch_out[10] rate_switch_ctrr[10] reconfig_data[150] gaeq_togxb[230] aeq_togxb[230] ded_tri_write ctrl_waitrequest	File Description altera_mf Altera megafunction simulation library lpm LPM megafunction simulation library
ctrl_address[15.0] jogical_channel_address[1.0] Resource Usage 1 att_aeq_s4 + 1 att_cal + 1 att_eyemon + 285 lut + 311 reg	you are synthesizing your design with a third-party synthesis tool, using a timing and resource estimation netlist can allow for better design optimization. Not all third-party synthesis tools support this feature - check with the tool vendor for complete support information. Note: Netlist generation can be a time-intensive process. The size of the design and the speed of your system affect the time it takes for netlist generation to complete. Generate netlist

Table 3–5 lists the available option on page 7 of the MegaWizard Plug-In Manager for your ALTGX_RECONFIG custom Megafunction variation.

Make your selections on page 7, then click Next.

Table 3-5. MegaWizard Plug-In Manager Options (Page 7)

ALTGX_RECONFIG Setting	Description	Reference
Generate a netlist for synthesis area and timing estimation	Selecting this option generates a netlist file that third-party synthesis tools can use to estimate the timing and resource usage.	_

Figure 3–9 shows page 8 (the last page) of the MegaWizard Plug-In Manager for the dynamic reconfiguration protocol set up. You can select optional files on this page.

After you make your selections, click **Finish** to generate the files.



ALTGX_RECONFIG About	AegaWizard Plug-In Manager [page 8 of	8] Sum	ımary				X
Parameter Settings Summary Image: Settings Summary reconfig.clk reconfig.togxb[3.0] reconfig.clk reconfig.togxb[3.0] write_all tx_vodctri_touti1.0] tx_preemp_01(10.0] tx_preemp_10(00119.0) tx_reddgain(11.0) tx_reddgain out[1.0] tx_reddgain(11.0) rx eqdcgain out[1.0] rx_eqdcfig1.0] rest exturb_out[1.0] rx_eqdcgain(11.0) rx eqdcgain out[1.0] reconfig.ddat(15.0) ret reduction ddat(15.0) ret reduction ddat(15.0) ret reduction ddat(15.0) ret returbed ddat(15.0) returbed ddat(15.0) returbed ddat(15.0) retur exddataddat[5.0] ctr	ALTGX_RECONFIG				<u>A</u> bout	Documentat	on
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Document Revision History

Table 3–6 lists the revision history for this chapter.

 Table 3–6.
 Document Revision History (Part 1 of 2)

Date	Version	Changes
February 2011	3.1	■ Updated Table 3–1.
		 Applied new template.
		 Updated chapter title.
		 Minor text edits.
November 2009	3.0	■ Updated Table 3–1.
		■ Updated Table 3–3.
		Added Figure 3–6.
		Made minor text edits.

Date	Version	Changes
		 Updated Table 3–3.
June 2009	2.1	 Added introductory sentences to improve search ability.
		 Minor text edits.
March 2009	2.0	Updated screen shots.
November 2008	1.0	Added chapter to the Stratix IV Device Handbook

Table 3-6. Document Revision History (Part 2 of 2)