

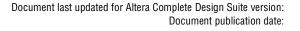
PowerPlay Early Power Estimator for Altera CPLDs

User Guide



101 Innovation Drive San Jose, CA 95134 www.altera.com

UG-01093-1.0



10.1 December 2010







Contents



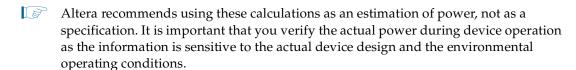
Chapter 1. PowerPlay Early Power Estimator Overview	
Setting Up the PowerPlay EPE	1–1
Download and Install the PowerPlay EPE	1–1
Estimating Power Consumption	
Estimating Power Consumption Before Starting the CPLD Design	
Estimating Power Consumption While Creating the CPLD Design	
Estimating Power Consumption After Completing the CPLD Design	
Entering Information into the PowerPlay Early Power Estimator	
Clearing All Values	
Manually Entering Values	
Importing a File	
•	
Chapter 2. PowerPlay Early Power Estimator Worksheets	
Power Estimation Using the PowerPlay Early Power Estimator	2–1
Main Worksheet	2–1
Input Parameter	2–2
Power	
Thermal Analysis	2–4
Power Supply Current	
Other Input Section	
Core Worksheet	
Clock Section	
Logic Section	
User Flash Memory Section	
I/O Worksheet	
Factors Affecting the PowerPlay Early Power Estimator Spreadsheet Accuracy	
Toggle Rate	
Airflow	
Temperature	
Chapter 3. Power Saving Techniques	
Additional Information	
Document Revision History	Info–1
How to Contact Altera	
Typographic Conventions	

iv Contents



1. PowerPlay Early Power Estimator Overview

This user guide describes the PowerPlay Early Power Estimator (EPE) support for MAX® II and MAX V device families and provides a step-by-step explanation of how to use this tool at any stage of the CPLD design. There are also details about thermal analysis and the factors that contribute to CPLD power consumption. You can calculate the CPLD power with the Microsoft Excel-based PowerPlay EPE spreadsheet or the PowerPlay Power Analyzer in the Quartus® II software by entering the device resources, operating frequency, toggle rates, and other parameters into the PowerPlay EPE spreadsheet.



For more information about available device resources, I/O standard supports, and other device features, refer to the respective device family handbook.

The features of the PowerPlay EPE spreadsheet include:

- Estimating the power consumption of your design before creating the design or during the design process
- Importing device resource information from the Quartus II software into the PowerPlay EPE spreadsheet with the use of the Quartus II-generated PowerPlay EPE file
- Performing preliminary thermal analysis of your design

Setting Up the PowerPlay EPE

This section describes how to set up the PowerPlay EPE, estimating power consumption, and entering information into the PowerPlay EPE spreadsheet.

Download and Install the PowerPlay EPE

The PowerPlay EPE spreadsheet for Altera® devices is available from the PowerPlay Early Power Estimators (EPE) and Power Analyzer on the Altera website. You can download the Microsoft Excel (.xls) file and begin the power analysis for your designs.

By default, the macro security level in Microsoft Excel 2003 and Microsoft Excel 2007 is set to **High** and macros are automatically disabled. For the features in the PowerPlay EPE spreadsheet to function properly, you must enable macros.

To change the macro security level in Microsoft Excel 2003, perform the following steps:

- 1. On the Tools menu, click **Options**.
- 2. On the **Security** tab, click **Macro Security**.
- 3. On the **Security Level** tab of the **Security** dialog box, choose **Medium**. Click **Ok**.
- 4. On the Options window, click **Ok**.
- 5. Close the PowerPlay EPE spreadsheet and reopen it.
- 6. A pop-up window asks you whether or not to enable macros each time you open a spreadsheet that contains macros, click **Enable Macros**.

To change the macro security level in Microsoft Excel 2007, perform the following steps:

- 1. Click the **Office** button in the upper left corner of the .xlsx file.
- 2. At the bottom of the menu, click **Excel Options**.
- 3. Click **Trust Center** on the left and then click **Trust Center Settings**.
- 4. In the **Trust Center** dialog box, click **Macro Settings**. Turn on the **Disable all** macros with notification option.
- 5. Close the PowerPlay EPE spreadsheet and reopen it.
- 6. A security warning appears beneath the Office ribbon. Click **Options**.
- 7. In the Microsoft Office Security Options dialog box, turn on Enable this content.

Estimating Power Consumption

You can use the PowerPlay EPE spreadsheet to estimate the power consumption at any point of your design cycle. You can use the PowerPlay EPE spreadsheet to estimate the power consumption if you have not begun your design, or if your design is not complete.



While the PowerPlay EPE spreadsheet can provide you with an estimate for your complete design, Altera recommends using the PowerPlay Power Analyzer in the Quartus II software to obtain this estimate for your complete design because the PowerPlay Power Analyzer can give you a more accurate analysis of your exact routing and the various modes of operation.

Estimating Power Consumption Before Starting the CPLD Design

Table 1–1 lists the advantage and disadvantages of using the PowerPlay EPE spreadsheet before you begin your CPLD design.

Table 1-1. Power Estimation Before Designing CPLD

Advantage	Disadvantage
 You can obtain power estimation before starting your CPLD design. 	Accuracy depends on your inputs and your estimation of the device resources; where this information may change (during or after your design is complete), your power estimation results may be less accurate.
	Process can be time consuming.

To estimate power consumption using the PowerPlay EPE spreadsheet before starting your CPLD design, perform the following steps:

- 1. On the Main worksheet of the PowerPlay EPE spreadsheet, select the target family, device, and package from the **Device** and **Package** drop-down list.
- 2. Enter values for each worksheet in the PowerPlay EPE spreadsheet. Different worksheets in the PowerPlay EPE spreadsheet display different power sections, such as clocks and I/Os.
- 3. The calculator displays the estimated power consumption in the **Total** column.

Estimating Power Consumption While Creating the CPLD Design

If your CPLD design is partially complete, you can import the PowerPlay EPE file (<revision name>_early_pwr.csv) generated by the Quartus II software to the PowerPlay EPE spreadsheet. After importing the information from the <revision name>_early_pwr.csv file into the PowerPlay EPE spreadsheet, you can edit the PowerPlay EPE spreadsheet to reflect the device resource estimates for your final design.

Table 1–2 lists the advantage and disadvantages if you use the PowerPlay EPE spreadsheet for a CPLD design that is partially complete.

Table 1-2. Power Estimation if Your CPLD Design is Partially Complete

Advantage	Disadvantage
 You can perform power estimation early in the CPLD design cycle. 	 Accuracy depends on your inputs and your estimation of the device resources; where this
 Provides the flexibility to automatically fill in the PowerPlay EPE spreadsheet based on the Quartus II software compilation results. 	information may change (during or after your design is complete), your power estimation results may be less accurate.
	Process can be time consuming.

To estimate power consumption with the PowerPlay EPE spreadsheet if your CPLD design is partially complete, refer to "Importing a File" on page 1–4.

Estimating Power Consumption After Completing the CPLD Design

If your design is complete, Altera recommends using the PowerPlay Power Analyzer in the Quartus II software. The PowerPlay Power Analyzer provides the most accurate estimate of device power consumption. To determine power consumption, the PowerPlay Power Analyzer uses simulation, user mode, and default toggle rate assignments, in addition to placement-and-routing information.



For more information about the power estimation feature, how to use the PowerPlay Power Analyzer, and generating the PowerPlay EPE file in the Quartus II software, refer to the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Entering Information into the PowerPlay Early Power Estimator

You can either manually enter power information into the PowerPlay EPE spreadsheet or load a PowerPlay EPE file generated by the Quartus II software. You can also clear all current values in the PowerPlay EPE spreadsheet.

To use the PowerPlay EPE spreadsheet, enter the device resources, operating frequency, toggle rates, and other parameters in the PowerPlay EPE spreadsheet. If you do not have an existing design, you must estimate the number of device resources your design uses and enter the information into the PowerPlay EPE spreadsheet.

Clearing All Values

You can reset all the user-entered values in the PowerPlay EPE spreadsheet by clicking the **Reset** button.



To use the Reset feature, you must enable macros for the spreadsheet. If you have not enabled macros for the spreadsheet, you must manually reset all the user-entered values.

Manually Entering Values

You can manually enter values into the PowerPlay EPE spreadsheet in the appropriate section. White unshaded cells are input cells that you can modify. Each section contains a column that allows you to specify a module name based on your design.

Importing a File

Importing a file saves you time and effort otherwise spent on manually entering information into the PowerPlay EPE spreadsheet. You can also manually change any of the values after importing a file.

To generate the PowerPlay EPE file, perform the following steps:

- 1. Compile the partial CPLD design in the Quartus II software.
- 2. On the Project menu, click **Generate PowerPlay Early Power Estimator File** to generate the *<revision name>_early_pwr.csv* file in the Quartus II software.

To import the Quartus II file into the PowerPlay EPE spreadsheet, perform the following steps:

- 1. In the PowerPlay EPE spreadsheet, click **Import QII File**.
- 2. Browse to a PowerPlay EPE file generated from the Quartus II software and click **Open**. The file has a name of *<revision name>_early_pwr.csv*.
- 3. In the confirmation window, click **OK**.
- 4. If the file is imported, click **OK**. Clicking OK acknowledges the import is complete. If there are any errors during the import, an **.err** file is generated with details.



You must import the PowerPlay EPE file into the PowerPlay EPE spreadsheet before modifying any information in the PowerPlay EPE spreadsheet. Also, you must verify all your information after importing a file.

To import the EPE file into the PowerPlay EPE spreadsheet, perform the following steps:

- 1. In the PowerPlay EPE spreadsheet, click **Import EPE**.
- 2. Browse to a PowerPlay EPE spreadsheet file (.xls) and click Open.
- 3. In the confirmation window, click **OK**.

Importing the Quartus II PowerPlay EPE file or the PowerPlay EPE spreadsheet from the Quartus II software populates all input values on the Main worksheet as per specified in the Quartus II software. These parameters include:

- Device
- Package
- Temperature grade
- Power characteristics
- V_{CCINT} supply voltage
- Ambient temperature, T_A (°C)
- Airflow



For more information about these parameters, refer to "Main Worksheet" on page 2–1.

The clock frequency (f_{MAX}) values imported into the PowerPlay EPE spreadsheet are the same as the f_{MAX} values taken from the Quartus II software as per the design. You can manually edit the f_{MAX} values and the toggle percentage in the PowerPlay EPE spreadsheet to suit your design requirements.



2. PowerPlay Early Power Estimator Worksheets

This chapter describes how to evaluate and manage MAX II and MAX V power using the PowerPlay EPE spreadsheet.

This chapter contains the following sections:

- "Power Estimation Using the PowerPlay Early Power Estimator" on page 2–1
- "Factors Affecting the PowerPlay Early Power Estimator Spreadsheet Accuracy" on page 2–13

Power Estimation Using the PowerPlay Early Power Estimator

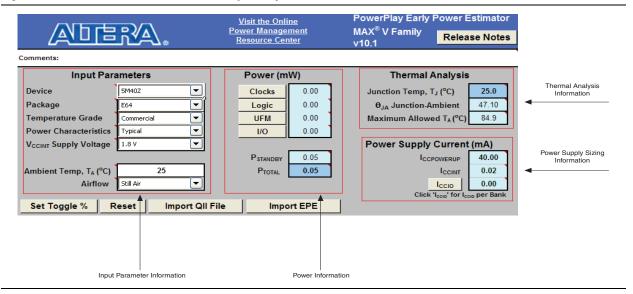
This section provides information about each worksheet of the PowerPlay EPE spreadsheet. The PowerPlay EPE spreadsheet provides the ability to enter information into worksheets based on architectural features. The PowerPlay EPE spreadsheet also provides a subtotal of power consumed by each architectural feature and is reported in each worksheet in mWatts (mW).

Main Worksheet

The Main worksheet of the PowerPlay EPE spreadsheet summarizes the power and current estimates for the design. The Main worksheet displays the total thermal power, thermal analysis, and power supply sizing information.

Figure 2–1 shows the Main worksheet of the PowerPlay EPE spreadsheet.

Figure 2–1. Main Worksheet of the PowerPlay EPE Spreadsheet





Only use the results obtained as an estimation of power, not as a specification of power. The actual I_{CC} must be verified during device operation, as this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

The accuracy of the power estimation depends on the information you enter. The power consumed can also vary depending on the toggle rates you enter. The following sections describe the sections in the Main worksheet of the PowerPlay EPE spreadsheets.

Input Parameter

Different MAX II and MAX V devices consume different amounts of power for the same design. The larger the device, the more power it consumes because of a larger clock tree.

Table 2–1 lists the values you must specify in the Input Parameter section in the Main worksheet of the PowerPlay EPE spreadsheet, as shown in Figure 2–1.

Table 2-1. Input Parameter Section Information

Input Parameter	Description						
	Select your device.						
Device	Larger devices consume more static power and have higher clock dynamic power. All power components are unaffected by the device you use.						
	Select the package that you are using.						
Package	Larger packages provide a larger cooling surface and more contact points to the circuit board, leading to lower thermal resistance. Package selection does not affect dynamic power.						
	Select the appropriate temperature grade. This field only affects the allowed maximum junction temperature range.						
Temperature Grade	Different device families support different temperature grades. For more information about the supported temperature grade and the recommended operating range for the device junction temperature, refer to the <i>DC</i> and Switching Characteristics chapter in the MAX II Device Handbook and the <i>DC</i> and Switching Characteristics for MAX V Devices chapter in the MAX V Device Handbook.						
D Ohti-ti	Select the typical or theoretical worst-case silicon process.						
Power Characteristics	There is a process variation from die-to-die. This primarily impacts static power consumption.						
V _{CCINT} Supply Voltage	The voltage of the V_{CCINT} power supply. For MAX IIG, MAX IIZ, and MAX V devices, the supply voltage is 1.8 V . For other MAX II devices, it can be either 2.5 V or 3.3 V . Devices with lower V_{CCINT} have lower total standby power consumption.						
Ambient Temperature, T _A (°C)	Enter the air temperature near the CPLD device. This value can range from -40°C to 125°C , depending on the device temperature grade. This parameter is used to compute junction temperature based on power dissipation and thermal resistances through the top of the chip.						
Airflour	Select an available ambient airflow in linear-feet per minute (Ifm) or meters per second (m/s). The values are 100 Ifm (0.5 m/s), 200 Ifm (1.0 m/s), 400 Ifm (2.0 m/s), or Still Air.						
Airflow	Increased airflow results in a lower junction-to-air thermal resistance and lowers the junction temperature.						

Power

This section describes the power dissipated in the MAX II and MAX V devices. The total thermal power is shown in mWatts and is a sum of the thermal power of all the resources being used in the device.

Table 2–2 lists the thermal power parameters in the PowerPlay EPE spreadsheet, as shown in Figure 2–1 on page 2–1.

Table 2-2. Power Section Information

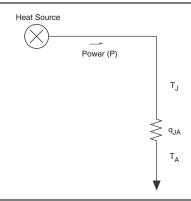
Column Heading	Description				
Clocks	Represents the dynamic power consumed by the clock networks. To view the details, click Clocks .				
Logic	Represents the dynamic power consumed by the logic elements (LEs) and associated routing. To view the details, click Logic .				
UFM	Represents the dynamic power consumed by the UFM block. To view the details, click UFM .				
1/0	Represents the dynamic power consumed by the I/O pins and associated routing. To view the details, click I/O.				
P _{STANDBY}	Represents the static power consumed irrespective of the clock frequency. The value includes static power consumed by the I/O banks and the voltage regulator.				
	P_{STANDBY} depends on the device you select and the V_{CCINT} supply voltage.				
P _{TOTAL}	Represents the total power consumed by the CPLD device. For more information about the current draw from the CPLD supply rails, refer to "Power Supply Current" on page 2–5.				

Thermal Analysis

To determine the junction temperature (T_J) of the device in ${}^{\circ}C$, the ambient temperature and airflow are taken into consideration by the PowerPlay EPE spreadsheet.

The device is considered a heat source and the junction temperature is the temperature at the device. The thermal resistance of the path is referred to as the junction-to-ambient thermal resistance (θ_{JA}). Figure 2–2 shows the thermal model for the PowerPlay EPE spreadsheet.

Figure 2-2. PowerPlay Early Power Estimator Thermal Model



The PowerPlay EPE spreadsheet determines the θ_{JA} based on the device, package, and airflow selected in the input parameters section.

The PowerPlay EPE spreadsheet calculates the total power based on the device properties which provide θ_{JA} and the ambient and junction temperature, as shown in Equation 2–1.

Equation 2-1.

$$P \,=\, \frac{T_J - T_A}{\theta_{JA}}$$

Table 2–3 lists the thermal analysis parameters in the PowerPlay EPE spreadsheet, as shown in Figure 2–1 on page 2–1.

Table 2-3. Thermal Analysis Section Information

Column Heading	Description
Junction Temp, T _J (°C)	Represents the device junction temperature estimation based on the supplied thermal parameters.
θ _{JA} Junction-Ambient	Represents the junction-to-ambient thermal resistance between the device and the ambient air (in °C/W).
Maximum Allowed T _A (°C)	Represents a guideline for the maximum ambient temperature (in °C) that you can subject the device to without violating the maximum junction temperature, based on the supplied cooling solution and device temperature grade.

Power Supply Current

The power supply current, shown in mA, provides the estimated current consumption for power supplies. The $I_{\text{CCPOWERUP}}$ is only applicable during power up when the configuration flash memory (CFM) block downloads to the SRAM. The I_{CCINT} current is the supply current required from V_{CCINT} . The total I_{CCIO} current is the supply current required from V_{CCIO} for all I/O banks. For more information about the estimates of I_{CCIO} based on I/O banks, refer to the "I/O Worksheet" on page 2–9.

Table 2–4 lists the power supply current parameters in the PowerPlay EPE spreadsheet, as shown in Figure 2–1 on page 2–1.

Table 2-4. Power Supply Current Section Information

Column Heading	Description				
I _{CCPOWERUP}	Represents the maximum current drawn during power up.				
I _{CCINT}	Represents the total current drawn from the I _{CCINT} supply.				
I _{CCIO}	Represents the total current drawn from the I _{CCIO} power rails. For more information about the current drawn from each I/O rail, refer to "I/O Worksheet" on page 2–9.				

Other Input Section

Figure 2–3 shows the four buttons under the other input parameters section in the PowerPlay EPE spreadsheet.

Figure 2–3. Other Input Section in PowerPlay EPE Spreadsheet



Table 2–5 lists the four buttons under the other input parameters section in the PowerPlay EPE spreadsheet.

Table 2-5. Other Input Section Information

Column Heading	Description			
Set Toggle %	Sets the toggle rate for the "Logic Section" on page 2–7 and "I/O Worksheet" on page 2–9.			
Reset	Clears all input values in the PowerPlay EPE spreadsheet.			
Import QII File	For more information about how to import the Quartus II File, refer to "Entering Information into the PowerPlay Early Power Estimator" on page 1–4.			
Import EPE	For more information about how to import the EPE spreadsheet, refer to "Entering Information into the PowerPlay Early Power Estimator" on page 1–4.			

Core Worksheet

The Core worksheet of the PowerPlay EPE spreadsheet includes the clock, logic, and user flash memory (UFM) sections.

Clock Section

MAX II and MAX V devices have four global clocks each. Each row in the Clock worksheet of the PowerPlay EPE spreadsheet represents a clock network or a separate clock domain. Enter the following parameters for each design module:

- Clock frequency (in MHz)
- Total fanout for each clock network you use
- Local clock enable percentage

Figure 2-4 shows the Clock section in the PowerPlay EPE spreadsheet.

Figure 2-4. Clock Section in the PowerPlay EPE Spreadsheet

Clock Domain	Clock Freq (MHz)	Total Fanout	Local Enable %	Total Power (mW)	User Comments
	0.0	0	50%	0.00	
	0.0	0	50%	0.00	
	0.0	0	50%	0.00	
	0.0	0	50%	0.00	

Table 2–6 lists the values you must specify in the Clock section of the PowerPlay EPE spreadsheet.

Table 2-6. Clock Section Information

Column Heading	Description
Clock Domain	Specify a name for the clock network in this column. This is an optional value.
Clock Freq (MHz)	Enter the frequency of the clock domain. This value is limited by the maximum frequency specification for the device family.
Total Fanout	Enter the total number of LE flipflops fed by this clock. The number of resources driven by every global clock is reported in the Fan-out column of the Quartus II Compilation Report. In the Compilation Report, select Filter and click Resources Section. Select Global and Other Fast Signals and click Fan-out.
	Enter the average percentage of time that clock enable is high for the destination flipflops.
Local Enable %	Local clock enables for flipflops in LEs are promoted to logic array block (LAB)-wide signals. When you disable a given flipflop, the LAB-wide clock is disabled, cutting clock power and the power for down-stream logic. This worksheet models only have impact on the clock tree power.
Total Power (mW)	This is the total power dissipation due to clock distribution.
User Comments	Enter any comments. This is an optional value.

Logic Section

A design is a combination of several design modules operating at different frequencies and toggle rates. Each design module can have a different amount of logic. For the most accurate power estimation, partition the design into different design modules. Each row in the Logic section of the PowerPlay EPE spreadsheet represents a separate design module.

Figure 2–5 shows the Logic section in the PowerPlay EPE spreadsheet.

Figure 2-5. Logic Section in the PowerPlay EPE Spreadsheet

				Power (mW)			
Logic Module	Clock Freq (MHz)	# LEs	Toggle %	Routing	Block	Total	User Comments
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	
	0.0	0	12.5%	0.00	0.00	0.00	

Table 2–7 lists the parameters in the Logic section of the PowerPlay EPE spreadsheet.

Table 2-7. Logic Section Information (Part 1 of 2)

Column Heading	Description			
Logic Module	Specify a name for each module of the design. This is an optional value.			
Clock Freq (MHz)	Enter a clock frequency (in MHz). This value is limited by the maximum frequency specification for the device families.			
	100 MHz with a 12.5% toggle means that each look-up table (LUT) or flipflop output toggles 12.5 million times per second (100 \times 12.5%).			
# LEs	Enter the number of LEs in this module.			
	Enter the average percentage of logic toggling on each clock cycle. The toggle percentage ranges from 0 to 100% . Typically, the toggle percentage is 12.5%, which is the toggle percentage of a 16-bit counter. To ensure you do not underestimate the toggle percentage, use a higher toggle percentage. Most logic only toggles infrequently; therefore, toggle rates of less than 50% are more realistic.			
Toggle %	For example, a TFF with its input tied to V_{CC} has a toggle rate of 100% because its output is changing logic states on every clock cycle (refer Figure 2–6). Figure 2–7 shows an example of a 4-bit counter. The first TFF with LSB output cout 0 has a toggle rate of 100% because the signal toggles on every clock cycle. The toggle rate for the second TFF with output cout 1 is 50% because the signal only toggles on every two clock cycles. Consequently, the toggle rate for the third TFF with output cout 2 and the fourth TFF with output cout 3 are 25% and 12.5%, respectively. Therefore, the average toggle percentage for this 4-bit counter is $(100 + 50 + 25 + 12.5)/4 = 46.875\%$.			

Table 2-7. Logic Section Information (Part 2 of 2)

Column Heading	Description
	This shows the power of dissipation due to the estimated routing.
Routing	Routing power depends on placement-and-routing information, which is a function of your design complexity. The values shown represent the routing power based on experimentation of more than 100 designs.
	For detailed analysis based on your design's routing, use the Quartus II PowerPlay Analyzer.
	This shows the power dissipation due to the internal toggling of the LEs.
Block	Logic block power is a combination of the function implemented and the relative toggle rates of the various inputs. The PowerPlay EPE spreadsheet uses an estimate based on an observed behavior across more than 100 designs.
	For accurate analysis based on your design's exact synthesis, use the Quartus II PowerPlay Analyzer.
Total	This shows the total power dissipation. The total power dissipation is the sum of the routing and block power.
User Comments	Enter any comments. This is an optional value.

Figure 2–6 shows the T-Flipflop.

Figure 2-6. T-FlipFlop

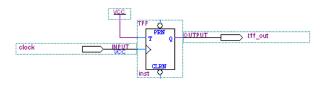
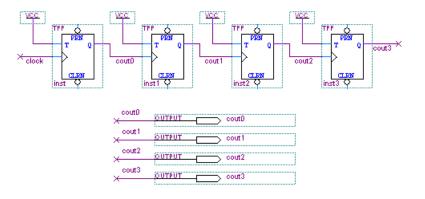


Figure 2–7 shows an example of a 4-bit counter.

Figure 2-7. 4-Bit Counter



User Flash Memory Section

When your design uses the UFM, the PowerPlay EPE spreadsheet considers the time spent during read operations into the power estimation. Figure 2–8 shows the UFM section in the PowerPlay EPE spreadsheet.

Figure 2–8. UFM Section in PowerPlay EPE Spreadsheet

UFM Module	Read %	Total Power (mW)	User Comments
	0.0%	0.00	

Table 2–8 lists the parameters in the UFM section of the PowerPlay EPE spreadsheet.

Table 2-8. UFM Section Information

Column Heading	Description
UFM Module	Specify a name for the UFM module in this column. This is an optional value.
Read %	Enter the percentage of time the UFM spends in Read mode. It takes 16 clock cycles to shift the serial data out after an internal UFM read so the read operation occurs less than 1/17 (or about 6%) of the time. The clock in this calculation is the UFM block's DRCLK signal.
Total Power (mW)	Total power dissipation due to reading from the UFM block (mW). Programming and erasing can only be performed for a limited number of times over the life of the device so they do not contribute to average power.
User Comments	Enter any comments. This is an optional value.

I/O Worksheet

MAX II and MAX V devices feature programmable I/O pins that support a wide range of industry I/O standards for increased design flexibility. The I/O section in the PowerPlay EPE spreadsheet allows you to estimate the I/O pin power consumption based on the pin's I/O standards.

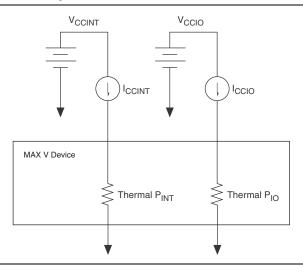
The total thermal power is the sum of the thermal power consumed by the device from each power rail, as shown in Equation 2–2:

Equation 2-2.

Thermal Power = Thermal Pint + Thermal Pio

Figure 2–9 shows a graphical representation of the thermal power consumption.

Figure 2-9. Thermal Power Representation



If you specify the I/O bank for the I/O pins in the I/O section, the PowerPlay EPE spreadsheet estimates the current for each I/O bank based on the V_{CCIO} settings. Figure 2–10 shows the I/O bank parameter settings.

Figure 2-10. I/O Bank Parameter Setting



Table 2–9 lists the I/O bank parameters in the I/O worksheet of the PowerPlay EPE spreadsheet, as shown in Figure 2–10.

Table 2-9. I/O Bank Section Information

Column Heading	Description
V _{CCIO}	Select the V_{CCIO} voltage for each bank. Use this to cross-check the selected I/O standards in the I/O section for warning purposes.
I _{CCIO}	Shows the total supply current due to the I/O pins in each I/O bank.
Unassigned	Represents the I _{CCIO} of all the I/O modules not assigned to an I/O bank.

Each row in the I/O module represents a design module where the I/O pins have the same frequency, toggle percentage, average capacitive load, I/O standard, and I/O bank. Figure 2–11 shows the I/O module of the PowerPlay EPE spreadsheet.

Figure 2–11. I/O Module Setting

														Po	wer (m	W)	Supply Cu	rrent (mA)	
Module	I/O Stand	ard	Clock Freq (MHz)	# Output Pins	# Input Pins	# Bidir Pins	I/O Ban		oggle %		Load (pF)	Bank I/O Std Check	Bank Voltage Check	Routing	Block	Total	I _{CCINT}	I _{CCIO}	User Comments
	1.5-V 2mA	~	0.0	0	0	0	?	▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	▼	0.0	0	0	0	?	▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	▼	0.0	0	0	0	? [▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	▼	0.0	0	0	0	? [▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	▼	0.0	0	0	0	? [▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	~	0.0	0	0	0	?	▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	~	0.0	0	0	0	?	▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	~	0.0	0	0	0	?	▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	▼	0.0	0	0	0	?	▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	▼	0.0	0	0	0	?	▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	▼	0.0	0	0	0	? [▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	▼	0.0	0	0	0	? [▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	▼	0.0	0	0	0	? [▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	▼	0.0	0	0	0	? [▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	▼	0.0	0	0	0	?	▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	▼	0.0	0	0	0	?	▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	▼	0.0	0	0	0	?	₹ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	-	0.0	0	0	0	?	▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	-	0.0	0	0	0	?	▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	
	1.5-V 2mA	-	0.0	0	0	0	?	▼ 1	12.5%	####	0	N/A	N/A	0.00	0.00	0.00	0.00	0.00	

Table 2–10 lists the I/O module parameters in the I/O worksheet of the PowerPlay EPE spreadsheet.

Table 2-10. I/O Module Section Information (Part 1 of 2)

Column Heading	Description
Module	Specify a name for the module in this column. This is an optional value.
I/O Standard	Select the I/O standard for the input, output, or bidirectional pins in this module from the pull-down list. The calculated I/O power varies based on the I/O standard.
Clock Freq (MHz)	Enter the clock frequency (in MHz). This value is limited by the maximum frequency specification for the device families.
	A 100 MHz input clock with a 12.5% toggle means that each I/O pin toggles 12.5 million times per second ($100 \times 12.5\%$).
# Output Pins	Enter the number of output pins in this module.
# Input Pins	Enter the number of input pins in this module.
# Bidir Pins	Enter the number of bidirectional pins in this module.
	An I/O pin configured as bidirectional but is used only as an output pin consumes more power than an I/O configured as an output-only pin due to the toggling of the input buffer every time the output buffer toggles as they share a common pin.
I/O Bank	Select the I/O bank for the module. If you do not know which I/O bank the pins will be assigned to, leave the value as "?". Assigning the I/O module to a bank ensures whether your I/O voltage assignments are compatible or not, allowing per bank I_{CCIO} reporting.
	The PowerPlay EPE spreadsheet does not take any I/O placement constraints into consideration except for the I/O standard and bank match and the I/O voltage.
Toggle %	Enter the average percentage of input, output, and bidirectional pins toggling on each clock cycle. For input pins used as clocks, the toggle percentage ranges from 0 to 200 % because clocks toggle at twice the frequency.
	Typically, the toggle percentage is 12.5%. To be more conservative, you can use a higher toggle percentage.

Table 2–10. I/O Module Section Information (Part 2 of 2)

Column Heading	Description
	Enter the average percentage of time that the:
	output I/O pins are enabled.
	bidirectional I/O pins are outputs and enabled.
0E %	During the remaining time the:
	output I/O pins are tri-stated.
	bidirectional I/O pins are inputs.
	The value you enter must be a percentage between 0 and 100 %.
	Enter the pin loading external to the chip (in pF).
Load (pF)	This only applies to outputs and bidirectional pins. Pin and package capacitance is already included in the I/O model. Therefore, only include the off-chip capacitance in the Load parameter.
Bank I/O Std Check	Indicates whether the selected I/O standard is available on the selected I/O bank or not. Not all I/O banks support every I/O standard.
Bank Voltage Check	Indicates whether the selected I/O bank has a voltage compatible with the selected I/O standard or not.
	This shows the power dissipation due to estimated routing.
Routing	Routing power depends on placement-and-routing information, which is a function of your design complexity. The values shown represent the routing power based on experimentation of more than 100 designs.
	For detailed analysis based on your design's routing, use the Quartus II PowerPlay Power Analyzer.
	This shows the power dissipation due to internal and load toggling of the I/O.
Block	For accurate analysis based on your design's I/O configuration, use the Quartus II PowerPlay Power Analyzer.
Total	This shows the total power dissipation. The total power dissipation is the sum of the routing and block power.
I _{CCINT}	This shows the current drawn from the I_{CCINT} power rail and powers the internal digital circuitry and routing.
I _{CCIO}	This shows the current drawn from this bank's V _{CCIO} power rail.
User Comment	Enter any comments. This is an optional value.

Factors Affecting the PowerPlay Early Power Estimator Spreadsheet Accuracy

There are many factors that affect the estimated values displayed in the PowerPlay EPE spreadsheet. In particular, the input parameters entered concerning toggle rates, airflow, and temperature must be accurate to ensure that the system is modeled correctly in the PowerPlay EPE spreadsheet.

Toggle Rate

The toggle rates specified in the PowerPlay EPE spreadsheet can have a large impact on the dynamic power consumption displayed. To obtain an accurate estimate, you must input toggle rates that are realistic. Determining realistic toggle rates requires you to know what kind of input the CPLD is receiving and how often it toggles.

To get an accurate estimate even if the design is not complete, isolate the separate modules in the design by functionality and estimate the resource usage along with the toggle rates of the resources. The easiest way to accomplish this is to leverage previous designs to estimate the toggle rates for modules with similar functionality.

The input data in Figure 2–12 is encoded for data transmission and has a roughly 50% toggle rate.

Figure 2-12. Decoder and Encoder Block Diagram



In this case, you must estimate the following:

- Data toggle rate
- Mod input toggle rate
- Resource estimate for the Decoder module, RAM, Filter, Modulator, and Encoder
- Toggle rate for the Decoder module, RAM, Filter, Modulator, and Encoder

You can generate these estimates in many ways. If you used similar modules in the past with data inputs of roughly the same toggle rate, you can leverage that information. If there are MATLAB simulations available for some blocks, you can obtain the toggle rate information. If the HDL is available for some of the modules, you can simulate them.

If the HDL is complete, the best way to determine toggle rate is to simulate the design. The accuracy of toggle rate estimates depends on the accuracy of the input vectors. Therefore, determining whether or not the simulation coverage is high gives you a good estimate of how accurate the toggle rate information is.

The Quartus II software can determine toggle rates of each resource used in the design if you provide information from simulation tools. Designs can be simulated in many different tools and the information provided to the Quartus II software through a Signal Activity File (.saf). The Quartus II PowerPlay Power Analyzer provides the most accurate power estimate. You can import the Comma-Separated Value File (.csv) from the Quartus II software into the PowerPlay EPE spreadsheet for estimating power after the design is complete.

Airflow

The PowerPlay EPE spreadsheet allows you to specify the airflow present at the device. This value affects thermal analysis and can significantly affect the power consumed by the device. To obtain an accurate estimate, you must correctly determine the airflow at the CPLD, not the output of the fan providing the airflow.

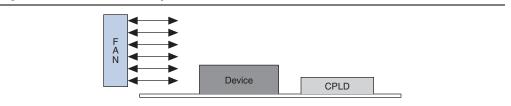
It is often difficult to place the device adjacent to the fan providing the airflow. The path of the airflow is likely to traverse a length on the board before reaching the device, thus diminishing the actual airflow the device receives. Figure 2–13 shows a fan that is placed at the end of the board. The airflow at the CPLD is weaker than it is at the fan.

Figure 2-13. Airflow and CPLD Position



It is also necessary to take into consideration the blocked airflow. Figure 2–14 shows a device blocking the airflow from the CPLD, significantly reducing the airflow seen at the CPLD. The airflow from the fan also has to cool board components and other devices before reaching the CPLD.

Figure 2-14. Airflow with Component and CPLD Positions



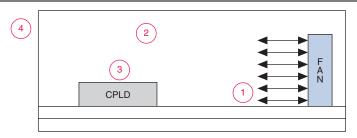
The considerations above can heavily influence the airflow received at the device. When entering information into the PowerPlay EPE spreadsheet, you have to consider these implications in order to get an accurate airflow value at the CPLD.

Temperature

To calculate the thermal information of the device correctly, you are required to enter the ambient air temperature for the device in the PowerPlay EPE spreadsheet. Ambient temperature refers to the temperature of the air around the device. This is usually higher than the ambient temperature outside of the system. To get an accurate representation of ambient temperature for the device, you must measure the temperature as close to the device as possible with a thermocouple device.

Entering the incorrect ambient air temperature can drastically alter the power estimates in the PowerPlay EPE spreadsheet. Figure 2–15 shows a simple system with the CPLD housed in a box. In this case, the temperature is very different at each of the numbered locations.

Figure 2-15. Temperature Variances



For example, location 3 is where the ambient temperature pertaining to the device should be obtained for input into the PowerPlay EPE spreadsheet. Locations 1 and 2 are cooler than location 3 and location 4 and is likely close to 25 °C if the ambient temperature outside the box is 25 °C. Temperatures close to devices in a system are often in the neighborhood of 50–60 °C but the values can vary significantly. In order to obtain accurate power estimates from the PowerPlay EPE spreadsheet, it is very important to get a realistic estimate of the ambient temperature near the CPLD device.



3. Power Saving Techniques

This chapter describes ways to reduce power cosumption.

The following guidelines reduce power consumption for an application:

- Slow the operation in portions of the circuit. I_{CC} is proportional to the frequency of the operation. Slowing parts of a circuit lowers the I_{CC}; therefore, reduces the power. MAX II and MAX V devices provide global or array clock source for all registers. Signals that do not require high-speed operation can use a slower array clock that reduces the system power consumption.
- Reduce the number of outputs. Standby and dynamic current are required to support all the I/O pins on the device. Reducing the number of I/O pins can reduce current necessary for the device thus reduces the power.
- Reduce the loading and external capacitance on the outputs. Excessive loading and capacitance of the PCB traces and other ICs on the output pins significantly increases power. Keeping the excess load and external capacitance to a minimum on the output pins whenever possible significantly reduces the current necessary for the device.
- Reduce the amount of circuitry in the device. Power depends on the amount of internal logic that switches at any given time. Reducing the amount of logic in a device reduces the current in the device and thus reduces the power.
- Modify the design to reduce power. Identify areas in the design that you can revise to reduce the power requirements. Common solutions include reducing the number of switching nodes and required logic and removing any redundant or unnecessary signals.
- Modify the I/O Locations. Grouping the I/O pins from common logic blocks allows the Quartus II software to place the associated logic closer together. The more compact a logic block and I/O, the lower its dynamic power (this is especially true of low utilization designs with the I/O spread around the device).
- Increase the performance requirements in the constraint file. Improving the performance that is beyond the need for operation reduces the power dissipation. The Quartus II software optimizes the design and places logic closer together, uses shorter routing and fewer logic levels, and lowers dynamic power and improves performance.
- MAX II and MAX V devices offer a power-down capability that conserves battery life for portable applications. For more information about the power-down capability in MAX II devices and an application design example, refer to AN 422: Power Management in Portable Systems Using MAX II CPLDs.



This chapter provides additional information about this user guide and Altera.

Document Revision History

The following table lists the revision history for this user guide.

Date	Version	Changes
December 2010	1.0	Initial release.

How to Contact Altera

To locate the most up-to-date information about Altera® products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
recillical training	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table lists the typographic conventions this user guide uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, Save As dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, qdesigns directory, \textbf{D}: drive, and \textbf{chiptrip.gdf} file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, Stratix IV Design Guidelines.
	Indicates variables. For example, $n + 1$.
italic type	Variable names are enclosed in angle brackets (< >). For example, <file name=""> and <project name="">.pof file.</project></file>
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.

Visual Cue	Meaning
"Subheading Title"	Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
	Indicates signal, port, register, bit, block, and primitive names. For example, data1, tdi, and input. The suffix n denotes an active-low signal. For example, resetn.
Courier type	Indicates command line commands and anything that must be typed exactly as it appears. For example, c:\qdesigns\tutorial\chiptrip.gdf.
	Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword SUBDESIGN), and logic function names (for example, TRI).
4	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	A question mark directs you to a software help system with related information.
•••	The feet direct you to another document or website with related information.
CAUTION	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
WARNING	A warning calls attention to a condition or possible situation that can cause you injury.
2	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.

Info-2