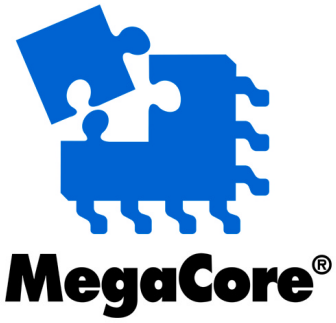

ATM Cell Processor 622 Mbps MegaCore Function

CP622

August 2001
User Guide

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com

A-UG-IPCP622-1.01

About this User Guide

User Guide

This user guide provides comprehensive information about the Altera® ATM Cell Processor 622 Mbps MegaCore® Function (CP622).

Table 1 shows the user guide revision history

Go to the following sources for more information:

- See "Features" on page 12 for a complete list of the core features, including new features in this release.
- Refer to the CP622 **readme** file for late-breaking information that is not available in this user guide.

Table 1. User Guide Revision History

Date	Description
February 2001	First version of user guide.
August 2001	First revision. Added "Core Verification Summary" section. Revised the "Getting Started" chapter.

How to Find Information

- The Adobe Acrobat Find feature allows you to search the contents of a PDF file. Click on the binoculars icon in the top toolbar to open the Find dialog box, or click the right mouse button for a pull-down menu.
- Bookmarks serve as an additional table of contents.
- Thumbnail icons, which provide miniature previews of each page, provide a link to the pages.
- Numerous links, shown in green text, allow you to jump to related information.

How to Contact Altera

For the most up-to-date information about Altera products, go to the Altera world-wide web site at http://www.altera.com.

For additional information about Altera products, consult the sources shown in Table 2.

Table 2. How to Contact Altera

Information Type	Access	USA & Canada	All Other Locations
Altera Literature Services	Electronic mail	lit_req@altera.com *(1)*	lit_req@altera.com *(1)*
Non-technical customer service	Telephone hotline	(800) SOS-EPLD	(408) 544-7000 (7:30 a.m. to 5:30 p.m. Pacific Time)
	Fax	(408) 544-7606	(408) 544-7606
Technical support	Telephone hotline	(800) 800-EPLD (7:00 a.m. to 5:00 p.m. Pacific Time)	(408) 544-7000 *(1)* (7:30 a.m. to 5:30 p.m. Pacific Time)
	Fax	(408) 544-6401	(408) 544-6401 *(1)*
	Electronic mail	telecom@altera.com	telecom@altera.com
	FTP site	ftp.altera.com	ftp.altera.com
General product information	Telephone	(408) 544-7104	(408) 544-7104 *(1)*
	World-wide web site	http://www.altera.com	http://www.altera.com

Note:
(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The *ATM Cell Processor 622 Mbps MegaCore Function (CP622) User Guide* uses the typographic conventions shown in Table 3.

Table 3. Conventions

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\maxplus2** directory, **d:** drive, **chiptrip.gdf** file.
Bold italic type	Book titles are shown in bold italic type with initial capital letters. Example: ***1999 Device Data Book***.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75 (High-Speed Board Design)*.
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: <*file name*>, <*project name*>**.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of Quartus II and MAX+PLUS II Help topics are shown in quotation marks. Example: "Configuring a FLEX 10K or FLEX 8000 Device with the BitBlaster™ Download Cable."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `_n`, e.g., `reset_n`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\max2work\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c.,...	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Abbreviations and Acronyms

AHDL	Altera Hardware Description Language
ATM	Asynchronous Transfer Mode
CLP	Cell Loss Priority
CPU	Central processing unit
EDA	Electronic Design Automation
ESB	Embedded System Block
FIFO	First In First Out
GFC	Generic Flow Control
HEC	Header Error Control
I/O	Input/Output
IP	Intellectual Property
LE	Logic Element
LSB	Least Significant Bit
LSByte	Least Significant Byte
Mbps	Megabits per second
MSB	Most Significant Bit
MSByte	Most Significant Byte
OAM	Operations, Administration, and Maintenance
PC	Personal computer
PHY	OSI Physical Layer
RX	Receive
RXATC	Receive ATM Transmission Convergence sub-block
TC	Transmission Convergence
TX	Transmit
TXATC	Transmit ATM Transmission Convergence sub-block
UDF	User Defined Field
UTOPIA	Universal Test & Operations Physical Interface for ATM
VCI	Virtual Channel Identifier
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VPI	Virtual Path Identifier

Contents

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General Description

The ATM Cell Processor 622 Mbps MegaCore® Function (CP622) uses the MegaWizard® Plug-In—within the Quartus® II software—to generate variants in AHDL, VHDL, or Verilog HDL, which you can instantiate into your design. Table 1 shows the optional features available to generate all variants of the CP622.

Table 1. Optional Features

Options	Parameters	Choices
Basic Configuration		
Generic cell filters *(1)*	FILT	0,1,4
Cell insertion and extraction to processor interface *(2)*	CIE	Y/N
Performance monitoring of—received or transmitted—corrected, corrupted, and filtered cells *(3)*	PM	Y/N

Notes:
(1) An OAM cell filter is included in the base core design to filter OAM cells.
(2) Requires one or four generic cell filters.
(3) Yes allows all performance monitor counts: received cells, transmitted cells, discarded cells, corrected HECs, uncorrected HECs, HEC error cells, Atlantic error cells, OAM cells, and generic filtered cells. No allows only a count of errored cells.

The CP622 is capable of performing all of the operations required to support the TC sublayer of an ATM PHY device, in compliance with all applicable standards, including:

- International Telecommunications Union, Recommendation, *ISDN User Network Interfaces, ITU-T I.432,* March 1993
- ATM Forum, *Utopia, An ATM-PHY Interface Specification, Level 2, Version 1.0, af-phy039.000,* June 1995
- Altera Corporation, *Atlantic™ Interface Specification*.

For the purpose of this user guide, "receive" indicates data flowing into the CP622 from the Midbus interface for transmission through the Atlantic interface; "transmit" indicates data received from the Atlantic interface for transmission through the Midbus interface. Thus the Atlantic interface is the source for transmit packets, and the sink for received packets.

Features

This user guide aims to describe the full-feature CP622.

Receiver Features

- ATM cell delineation
- Byte-boundary detection
- Loss of cell delineation indication
- Header single-bit error correction and multi-bit error detection
- External ATM cell GFC extraction
- Payload descrambling
- ATM cell formatting (8 to 16 bits)
- Discarding of OAM cells, and selectable cell filtering
- Cell insertion and extraction through AIRbus interface
- Performance monitoring of corrected, corrupted, and filtered cells

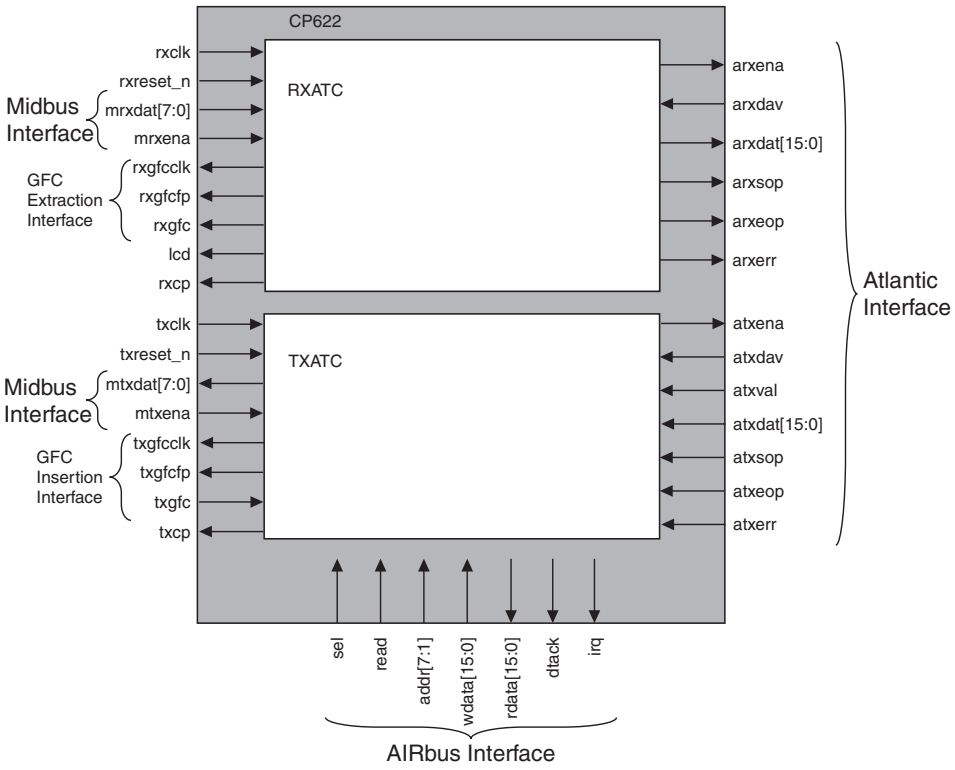
Transmitter Features

- Internal HEC generation and insertion
- Cell rate decoupling with programmable idle cell header and payload
- External ATM cell GFC insertion
- Payload scrambling
- ATM cell formatting (16 to 8 bits)
- Discarding of OAM cells, and selectable cell filtering
- Cell insertion and extraction through AIRbus interface
- Performance monitoring of corrected, corrupted, and filtered cells

Functional Description

The CP622 operates in full-duplex mode, and comprises two blocks: the RXATC block, and the TXATC block. Figure 1 shows a block diagram of the CP622, including the three interfaces that support it. See "Interfaces & Protocols" on page 20 for more information.

Figure 1. Block Diagram



Receiver Description

RXATC

The RXATC block performs ATM cell delineation, payload descrambling, HEC error detection, cell filtering, cell insertion/extraction, and cell formatting. The RXATC is designed to interface to a cell-based FIFO buffer, using the Atlantic interface.

Cell Delineation

Cell delineation detects cell boundaries in the received data stream by searching for valid HECs.

The incoming data stream can be either bit- or byte-aligned. If the incoming data stream is bit-aligned, the user can enable a software feature to byte-align the data. The cells must be sent contiguously, with the same number of octets. An ATM cell is 53 octets in length, therefore a cell boundary should exist every 53rd octet.

HEC Error Correction

Received cells that contain no HEC errors are forwarded to the filtering circuit. If an incorrect HEC is detected, a syndrome is produced to determine whether a single- or multi-bit error has occurred. The user can choose (software programmable) whether to discard, or forward the cell, depending on what is selected for the HECPASS bit. A single-bit error can be corrected (software programmable). For a multi-bit error, the HEC can be recalculated from the header information (software programmable).

Payload Descrambling

A self-synchronous descrambler is used to optionally descramble (software programmable) the payload data of an ATM cell.

GFC Extraction

GFC extraction allows the GFC field—a four bit value that carries information about local flow control within the header of an ATM cell—to be extracted. Extraction is achieved using a serial input port and controlled by GFC enable register bits. When enabled, the GFC value is extracted during each cell processing period. No modification is made to the GFC field since this is only an observation feature.

Filtering (FILT)

The CP622 contains a base OAM filter that discards specified OAM cells. The CP622 also includes a filtering option which allows for four generic filters to be added. The filters are independent of each other, because they perform their function in parallel. The filters selectively mask out any of the header bits for comparison, to find matching or un-matching bits. The sense bit—used to select cells that match or do not match the pattern—is also programmable by software. All filters can mark a cell if it meets their filtering requirements. Then, the arbitration process can take appropriate action.

Arbitration

Once a cell has been identified from the filtering stage, cell arbitration determines the action to be performed on that cell. There are two groups of possible actions: the first allows the cell to be discarded, or forwarded to the Atlantic interface; the second provides the ability to copy, or not copy the cell to a cell memory accessible via the AIRbus interface.

If the chosen action is to forward the cell, the filter circuits can also be used to simply count the traffic matching the pattern, without discarding it. This feature allows a user to audit the cell traffic activity without interrupting cell flow. Since the pattern is arbitrary, the filter can be used to count cells for a specific VPI, or cells for a specific VCI, or even cells with the CLP bit set. The filter circuit also has the ability of copying marked cells to memory, and then examining the payload through the AIRbus interface. All counting and copying is done without affecting the user traffic in any way.

Cells are only counted when cell delineation has been achieved. Statistics are collected for cells that are forwarded to the Atlantic, and for cells that have been internally discarded.

The discarding of a cell creates an opening for another cell to be inserted into the data stream. Arbitration identifies this opening and inserts an available cell from the cell insertion memory.

Idle/unassigned cells are added to the transmit data stream for the purpose of cell rate decoupling. To perform proper cell rate decoupling, the OAM filter, or one of the generic filters, should be programmed to discard all incoming idle/unassigned cells, especially before the cells are forwarded to the Atlantic interface.

Cell Insertion/Extraction (CIE)

A four-cell FIFO buffer is used for both insertion and extraction of the data path. Processor accesses are used to write to the insertion FIFO buffer and read from the extraction FIFO buffer. The cell arbitrator controls the insertion or extraction of cells from the data stream. External devices can only insert or extract one octet of cell data plus associative control information per access through the AIRbus interface. The RXATC data path can do simultaneous insertion and extraction since two separate four-cell FIFO buffers are used.

When a cell is identified for extraction, the arbitrator sends the entire cell to the extraction memory and raises an interrupt to flag the event. An interrupt is also set to indicate that at least one cell is available in cell memory, the interrupt can only be cleared when no cells remain in the FIFO buffer.

To insert a cell into the data stream, the external device must place an entire cell into memory. An interrupt indicates whether there is room available, and can only be cleared when the entire FIFO buffer is filled. The arbitrator waits for a cell to be discarded before it places the cell into the data stream. When a cell is discarded, it creates an opportunity—a period of time— when an entire insertion cell can be inserted into the data stream without interrupting the main data stream, and without causing any valid cells to be discarded. The data stream has priority over cell insertion. This method is used to insert OAM cells.

Performance Monitoring (PM)

The CP622 also includes a performance monitoring option which allows for certain statistics to be collected:

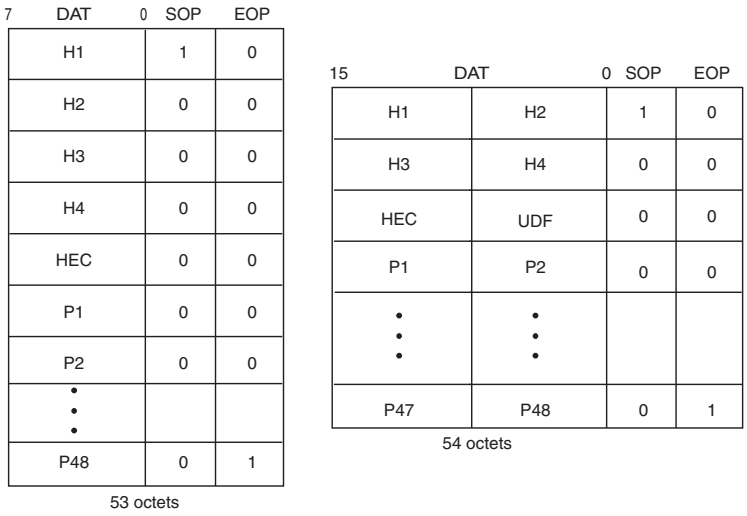
- Received cells
- Discarded cells
- Correctable HEC cells
- Uncorrectable HEC cells
- OAM filtered cells
- Generic filtered cells

Formatting

The RXATC connects to the 16-bit data path Atlantic interface. Formatting converts a 53-octet cell on an 8-bit data path (Midbus interface) to a 54-octet cell on a 16-bit data path (Atlantic interface). Figure 2 shows the 53 and 54 octet cell structures.

UDF1—the fifth octet of the formatted 54 octet cell—represents the HEC, and UDF2—the sixth octet—represents the HEC error status. An all 0s pattern represents the status of an error free HEC sequence, all 1s represent an uncorrectable HEC sequence, and alternating 1s and 0s represent a correctable HEC sequence.

Figure 2. 53 and 54 Octet Cell Structure



TXATC

The TXATC performs cell formatting, cell filtering, cell insertion/extraction, HEC regeneration and insertion, and payload scrambling. The TXATC is designed to interface to a cell-based FIFO buffer, using the Atlantic interface.

Formatting

The TXATC connects to the 16-bit data path Atlantic interface. Formatting converts a 54-octet cell on a 16-bit data path (Atlantic interface) to a 53-octet cell on an 8-bit data path (Midbus interface). Figure 2 shows the 53 and 54 octet cell structures. The UDF2 is stripped out and discarded from the cell.

Filtering (FILT)

The CP622 contains a base OAM filter that discards specified OAM cells. The CP622 also includes a filtering option which allows for four generic filters to be added. The filters are independent of each other, because they perform their function in parallel. The filters selectively mask out any of the header bits for comparison, to find matching or un-matching bits. The sense bit—used to select cells that match or do not match the pattern—is also programmable by software. All filters can mark a cell if it meets their filtering requirements. Then, the arbitration process can take appropriate action.

Arbitration

Once a cell has been identified from the filtering stage, cell arbitration determines the action to be performed on that cell. There are two groups of possible actions: the first allows the cell to be discarded, or forwarded to the Atlantic interface; the second provides the ability to copy, or not copy the cell to a cell memory accessible via the AIRbus interface.

If the chosen action is to forward the cell, the filter circuits can also be used to simply count the traffic matching the pattern, without discarding it. This feature allows a user to audit the cell traffic activity without interrupting cell flow. Since the pattern is arbitrary, the filter can be used to count cells for a specific VPI, or cells for a specific VCI, or even cells with the CLP bit set. The filter circuit also has the ability of copying marked cells to memory, and then examining the payload through the AIRbus interface. All counting and copying is done without affecting the user traffic in any way.

Cell Insertion/Extraction (CIE)

A four-cell FIFO buffer is used for both insertion and extraction of the data path. Processor accesses are used to write to the insertion FIFO buffer and read from the extraction FIFO buffer. The cell arbitrator controls the insertion or extraction of cells from the data stream. External devices can only insert or extract one octet of cell data plus associative control information per access through the AIRbus interface. The TXATC data path can do simultaneous insertion and extraction since two separate four-cell FIFO buffers are used.

When a cell is identified for extraction, the arbitrator sends the entire cell to the extraction memory and raises an interrupt to flag the event. An interrupt is also set to indicate that at least one cell is available in cell memory, the interrupt can only be cleared when no cells remain in the FIFO buffer.

To insert a cell into the data stream, the external device must place an entire cell in memory. An interrupt indicates whether there is room available and can only be cleared when the entire FIFO buffer is filled. The arbitrator waits for a cell to be discarded, or for the Atlantic interface to indicate that a cell is not available, before it places the cell into the data stream. This method is used to insert OAM cells.

Idle Cell Generation

If no valid cells are available from either the Atlantic interface, or insertion memory, an idle cell with programmable header and payload is inserted to adapt to the cell rate of cells being pulled from the Midbus interface.

Performance Monitoring (PM)

The CP622 also includes a performance monitoring option which allows for certain statistics to be collected:

- Transmitted cells
- Discarded cells
- HEC errors
- Atlantic errored cells
- OAM filtered cells
- Generic filtered cells

HEC Generation

HEC is generated and inserted into the transmitted ATM cell. Two other options (software programmable) are available to the user: forwarding the received HEC, or inverting the transmitted HEC for debugging purposes.

GFC Insertion

GFC insertion allows a value to be inserted into the GFC field of the header of an ATM cell. Insertion is made using a serial input port and controlled by GFC enable register bits. The GFC enable bits must be set for the existing GFC value to be modified. When enabled, the GFC value is inserted during each cell processing period. If the next transmit cell is an idle/unassigned cell and the GFC enable register bits are set, the GFC value in the Idle Cell Header register is overwritten.

Payload Scrambling

A self-synchronous scrambler is used to optionally scramble (software programmable) the payload data of an ATM cell.

Interfaces & Protocols

Midbus Interface

The Midbus interface is a simple synchronous full-duplex data path bus. The CP622 Midbus runs at 77.76 MHz over a single byte lane in each direction. In the RX direction, data is transferred from the Midbus master to the slave (CP622). In the TX direction, data is transferred from the slave (CP622) to the master. In each direction, the Midbus can carry eight bits per clock cycle. It includes midbus receive data (`mrxdat[7:0]`) and midbus receive enable (`mrxena`) lines to indicate valid data transfers in the RX direction, and midbus transmit data (`mtxdat[7:0]`) and midbus transmit enable (`mtxena`) lines to indicate valid data requests in the TX direction. Since the CP622 is a slave to the Midbus it can work with any Midbus master.

AIRbus Interface

The AIRbus interface provides access to internal registers using a simple synchronous internal processor bus protocol. This consists of separate read data (`rdata[15:0]`) and write data (`wdata[15:0]`) buses, a data transfer acknowledge (`dtack`) signal, and a select (`sel`) signal. An address (`addr[7:1]`) bus and read (`read`) signal indicate the location and type of access within the block. The `rdata` buses and `dtack` signals can be merged from multiple blocks using a simple OR function. The `dtack` signal is sustained until the block `sel` is removed (four-way handshaking) meaning the AIRbus can cross clock domain boundaries. The CP622 is an AIRbus slave with a data width of 16 bits.

Atlantic Interface

The Atlantic interface is a full-duplex synchronous bus protocol supporting both packets and cells. The CP622 is an Atlantic interface master using a 16-bit wide data path to deliver cells to the slave.

More detailed information on the Midbus, AIRbus, and Atlantic interfaces is available from the Altera web site at **http://www.altera.com**.

GFC Access

GFC access provides the ability to insert and extract the GFC field of the header of an ATM cell. The GFC field is represented as the first four bits of the first header byte carrying information about local flow control. Access can be made using a serial input port. A separate GFC enable register exists for the TX and RX directions. If the GFC enable bit for the corresponding GFC bit is set, the existing GFC value is replaced with the value on the GFC serial interface. When enabled, the GFC value is inserted or extracted during each cell processing period. If the next transmit cell is an idle/unassigned cell and the GFC enable register bit is set, the GFC value in the Idle Cell Header register is overwritten. A signal called `rxgfcfp/txgfcfp` is used to align the serial data to the MSB relating to GFC[3]. A signal called `rxgfcclk/txgfcclk` is a synthesized clock created from `rxclk/txclk` divided by 2.

Figure 3 shows a timing diagram for GFC extraction. The `rxgfcclk`, `rxgfcfp` and `rxgfc` signals are outputs. The `rxgfcfp` indicates the value on the `rxgfc` line is GFC[3] and is contiguously followed by GFC[2], GFC[1] and GFC[0] synchronous to `rxgfcclk`. The data is transmitted on the falling edge of the clock and data should be sampled on the rising edge of `rxgfcclk` by external circuitry.

Figure 3. Receive GFC Extraction

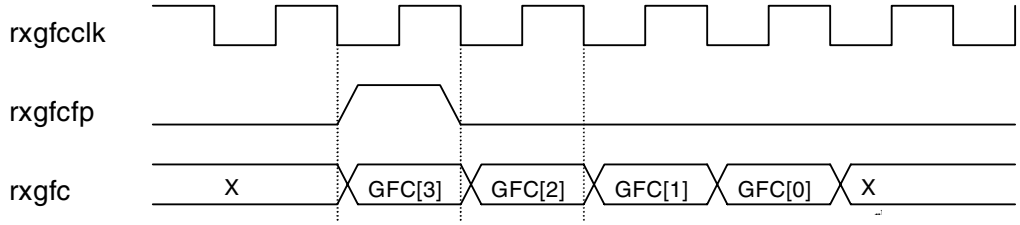
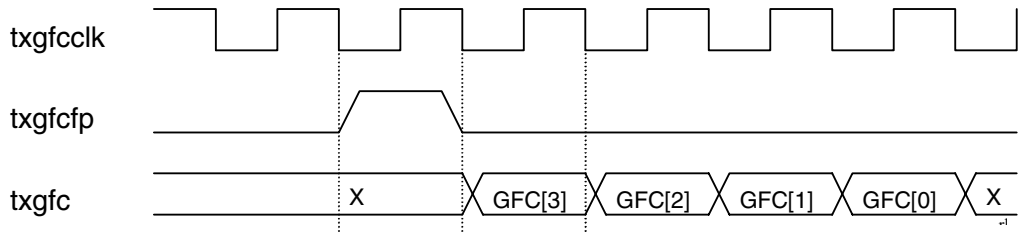


Figure 4 shows a timing diagram for GFC insertion. The `txgfcclk` and `txgfcmsb` signals are outputs and the `txgfc` signal is an input. The `txgfcmsb` indicates the next value required on the `txgfc` line is GFC[3] and is contiguously followed by GFC[2], GFC[1] and GFC[0] synchronous to `txgfcclk`. The data is transmitted on the falling edge of the clock from external circuitry and data should be sampled on the rising edge of `txgfcclk` by internal circuitry.

Figure 4. Transmit GFC Insertion



I/O Signals

Table 2 describes the input/output signals used by the CP622.

Table 2. I/O Signals

Port	Direction	Description
Receive Interface Signals		
rxclk	Input	Clock
rxreset_n	Input	Active low reset
rxcp	Output	Cell pulse: indicates cell has been received.
lcd	Output	Loss of cell delineation
Receive GFC Interface Signals		
rxgfcclk	Output	Serial generic flow control clock
rxgfcfp	Output	Serial generic flow control frame pulse
rxgfc	Output	Serial generic flow control data
Midbus Receive Interface Signals		
mrxena	Input	Enable
mrxdat[7:0]	Input	Data bus
Atlantic Receive Interface Signals		
arxena	Output	Enable
arxdav	Input	Data available
arxdat[15:0]	Output	Data bus
arxsop	Output	Start of packet
arxeop	Output	End of packet
arxerr	Output	Error indication
Transmit Interface Signals		
txclk	Input	Clock
txreset_n	Input	Active low reset
txcp	Output	Cell pulse: indicates cell has been transmitted.

Table 2. I/O Signals

Port	Direction	Description
Transmit GFC Interface Signals		
txgfcclk	Output	Serial generic flow control clock
txgfcfp	Output	Serial generic flow control frame pulse
txgfc	Output	Serial generic flow control data
Midbus Transmit Interface Signals		
mtxena	Input	Enable
mtxdat[7:0]	Output	Data bus
Atlantic Transmit Interface Signals		
atxena	Output	Enable
atxdav	Input	Data available
atxval	Input	Data valid
atxdat[15:0]	Input	Data bus
atxsop	Input	Start of packet
atxeop	Input	End of packet
atxerr	Input	Error indication
AIRbus Interface Signals		
sel	Input	Select
read	Input	Read: high for read cycles, and low for write.
addr[7:0]	Input	Address
wdata[15:0]	Input	Write data
rdata[15:0]	Output	Write data: all zeros if sel is not asserted.
dtack	Output	Data transfer acknowledge
irq	Output	Interrupt request

Performance

Table 3 shows the required speed and estimated gate count of the CP622 in an APEX 20KE device.

Table 3. Performance *Note (1)*

LEs	ESBs	f_{MAX} (MHz)
1,917– 4,834	0 – 4	77.76 required to support 622.08 Mbps

Note:
(1) The numbers for the LEs and ESBs are approximate as of August 2001. They reflect the range from the basic to the full feature variant.

Software Interface

Memory Map

All addresses access 16-bit registers and are shown as hexadecimal values. The value is the byte address, thus bit 0 is not used. All addresses are even.

Table 4. Memory Map (Part 1 of 3)

Byte Address	Register	Description
'h00	RXATC_CTRL	Control Register
'h02	RXATC_STAT	Status Register
'h04	RXATC_IS	Interrupt Status Register
'h06	RXATC_IE	Interrupt Enable Register
'h08	RXATC_OAM	OAM Filter Control Register
'h0A	RXATC_IMEM	Insertion Memory Access
'h0C	RXATC_EMEM	Extraction Memory Access
'h20	RXATC_PM_ERR	Error Performance Monitoring
'h22	RXATC_PM_CELL	Cell Performance Monitoring
'h24	RXATC_PM_DISC	Discard Cell Performance Monitoring
'h26	RXATC_PM_CHEC	Correctable HEC Performance Monitoring
'h28	RXATC_PM_UHEC	Uncorrectable HEC Performance Monitoring
'h2A	RXATC_PM_OAM	OAM Filter Performance Monitoring
'h2C	RXATC_PM_FILT0	Filter 0 Performance Monitoring
'h2E	RXATC_PM_FILT1	Filter 1 Performance Monitoring
'h30	RXATC_PM_FILT2	Filter 2 Performance Monitoring
'h32	RXATC_PM_FILT3	Filter 3 Performance Monitoring
'h40	RXATC_FILT0_CTRL	Filter 0 Control Register
'h42	RXATC_FILT0_PAT0	Filter 0 Pattern
'h44	RXATC_FILT0_PAT1	Filter 0 Pattern
'h46	RXATC_FILT0_CHK0	Filter 0 Check
'h48	RXATC_FILT0_CHK1	Filter 0 Check
'h4A	RXATC_FILT1_CTRL	Filter 1 Control Register
'h4C	RXATC_FILT1_PAT0	Filter 1 Pattern
'h4E	RXATC_FILT1_PAT1	Filter 1 Pattern
'h50	RXATC_FILT1_CHK0	Filter 1 Check
'h52	RXATC_FILT1_CHK1	Filter 1 Check
'h54	RXATC_FILT2_CTRL	Filter 2 Control Register
'h56	RXATC_FILT2_PAT0	Filter 2 Pattern
'h58	RXATC_FILT2_PAT1	Filter 2 Pattern
'h5A	RXATC_FILT2_CHK0	Filter 2 Check
'h5C	RXATC_FILT2_CHK1	Filter 2 Check

Table 4. Memory Map (Part 2 of 3)

Byte Address	Register	Description
'h5E	RXATC_FILT3_CTRL	Filter 3 Control Register
'h60	RXATC_FILT3_PAT0	Filter 3 Pattern
'h62	RXATC_FILT3_PAT1	Filter 3 Pattern
'h64	RXATC_FILT3_CHK0	Filter 3 Check
'h66	RXATC_FILT3_CHK1	Filter 3 Check
'h80	TXATC_CTRL	Control Register
'h82	TXATC_STAT	Status Register
'h84	TXATC_IS	Interrupt Status Register
'h86	TXATC_IE	Interrupt Enable Register
'h88	TXATC_OAM	OAM Filter Control Register
'h8A	TXATC_IDLE	Idle Cell Control Register
'h8C	TXATC_IMEM	Insertion Memory Access
'h8E	TXATC_EMEM	Extraction Memory Access
'hA0	TXATC_PM_ERR	Error Performance Monitoring
'hA2	TXATC_PM_CELL	Cell Performance Monitoring
'hA4	TXATC_PM_DISC	Discard Cell Performance Monitoring
'hA6	TXATC_PM_HERR	HEC Error Performance Monitoring
'hA8	TXATC_PM_AERR	Atlantic Error Performance Monitoring
'hAA	TXATC_PM_OAM	OAM Filter Performance Monitoring
'hAC	TXATC_PM_FILT0	Filter 0 Performance Monitoring
'hAE	TXATC_PM_FILT1	Filter 1 Performance Monitoring
'hB0	TXATC_PM_FILT2	Filter 2 Performance Monitoring
'hB2	TXATC_PM_FILT3	Filter 3 Performance Monitoring
'hC0	TXATC_FILT0_CTRL	Filter 0 Control Register
'hC2	TXATC_FILT0_PAT0	Filter 0 Pattern
'hC4	TXATC_FILT0_PAT1	Filter 0 Pattern
'hC6	TXATC_FILT0_CHK0	Filter 0 Check
'hC8	TXATC_FILT0_CHK1	Filter 0 Check
'hCA	TXATC_FILT1_CTRL	Filter 1 Control Register
'hCC	TXATC_FILT1_PAT0	Filter 1 Pattern
'hCE	TXATC_FILT1_PAT1	Filter 1 Pattern
'hD0	TXATC_FILT1_CHK0	Filter 1 Check
'hD2	TXATC_FILT1_CHK1	Filter 1 Check
'hD4	TXATC_FILT2_CTRL	Filter 2 Control Register
'hD6	TXATC_FILT2_PAT0	Filter 2 Pattern
'hD8	TXATC_FILT2_PAT1	Filter 2 Pattern

Table 4. Memory Map (Part 3 of 3)

Byte Address	Register	Description
'hDA	TXATC_FILT2_CHK0	Filter 2 Check
'hDC	TXATC_FILT2_CHK1	Filter 2 Check
'hDE	TXATC_FILT3_CTRL	Filter 3 Control Register
'hE0	TXATC_FILT3_PAT0	Filter 3 Pattern
'hE2	TXATC_FILT3_PAT1	Filter 3 Pattern
'hE4	TXATC_FILT3_CHK0	Filter 3 Check
'hE6	TXATC_FILT3_CHK1	Filter 3 Check

Registers

Table 5 lists the access codes used to describe the type of register bits.

Table 5. Registers

Code	Description
RW	Read/Write
RO	Read-Only
RW1C	Read/Write 1 to Clear
RW0S	Read/Write 0 to Set
RTC	Read to Clear
RTS	Read to Set
RTCW	Read to Clear/Write
RTSW	Read to Set/Write
RWTC	Read/Write any value to Clear
RWTS	Read/Write any value to Set
RWSC	Read/Write Self-Clearing
RWSS	Read/Write Self-Setting
UR0	Unused bits/Read as 0
UR1	Unused bits/Read as 1

RXATC Register Description

The following tables describe the registers for the receiver section of the CP622.

RXATC_CTRL - Control Register - 'h00 (Part 1 of 2)

Field	Bits	Access	Function	Default
BITALIGN	14	RW	Bit Alignment When this bit is set to '1', it enables bit alignment for cell delineation. The cell or byte boundary can exist anywhere in the received data. Bit alignment shifts and searches the data until cell alignment is found. If the data is byte-aligned, this bit should not be set because it may lengthen the duration of cell delineation.	0
GFCEXT	13:10	RW	GFC Extraction These bits determine whether or not to send each individual received GFC bit to the GFC serial output interface. When the corresponding bit is set to '1', the GFC bit from the ATM header is placed on the serial interface, otherwise it is forced low. GFC extraction provides the ability to extract a value from the GFC field of the header of an ATM cell. The GFC field is represented as the first four bits of the first header byte carrying information about local flow control. Extraction is made using a serial input port and controlled by a GFC enable register bit. When enabled, the GFC value is extracted during each cell-processing period. No modification is made to the GFC field since this is only an observation feature.	0
HECTHRD	9:8	RW	HEC Threshold The thresholds indicate the number of valid cells required in the HEC detection state to return back to the HEC correction state. For example, if HECTHRD is set to 'b10, and if the RXATC is in the detection state, then after detecting 4 cells, the RXATC goes back to HEC correction state. 'b00 - 1 ATM cell with a valid HEC (default) 'b01 - 2 ATM cells with a valid HEC 'b10 - 4 ATM cells with a valid HEC 'b11 - 8 ATM cells with a valid HEC	0

RXATC_CTRL - Control Register - 'h00 (Part 2 of 2)

Field	Bits	Access	Function	Default
HECSTAT	7	RW	HEC Status When this bit is set to '1', the HEC status information is written to the UDF2. Status information: 'h00 - error free HEC sequence 'hFF - uncorrectable HEC sequence 'hAA - correctable HEC sequence	0
HECINS	6	RW	HEC Insert When this bit is set to '1', it inserts the HEC octet into the UDF1.	0
HECADD	5	RW	HEC Addition When this bit is set to '1', it performs modula 2 addition of x*6 + x*4 + x*2 + 1 ('b0101_0101) to the header before the HEC comparison.	1
HECPASS	4	RW	HEC Pass Controls cell discard when a HEC error is detected. If this bit is set to '0', all cells with uncorrectable headers are discarded. Cells are only passed in the SYNC delineation state, all cells with uncorrectable headers are normally discarded. If this bit is set to '1', all uncorrectable headers are passed in the SYNC state, and the HEC correction state machine remains in the correction state.	0
HECCOR	3	RW	HEC Correction Controls the HEC error correction of the header. When this bit is set to '1', single bit header errors are corrected. When it is set to '0', single bit errors are always treated as uncorrectable errors.	0
HECRGN	2	RW	Regenerate HEC When this bit is set to '1', the HEC is regenerated for all cells with uncorrectable headers. The generating polynomial is x*8 + x*2 + x + 1 with the optional modula 2 addition of x*6 + x*4 + x*2 + 1, based on the HECADD bit.	0
DESCRAM	1	RW	Descrambling When this bit is set to '1', payload self-synchronous descrambling is performed, using the x*43 + 1 polynomial.	0
EN	0	RW	Enable When this bit is set to '0', the cell processor is disabled. The cell processor remains in a static state and continues to ignore enables until the bit is set to '1'. The CPU must set the EN bit to '1' before cells can be received.	1

RXATC_STAT - Status Register - 'h02

Field	Bits	Access	Function	Default
IMEMDAV	4	RO	Insertion Memory Data Available This bit indicates the current Insertion Memory Data Available status. It is set to '1' when the insertion memory has room for an entire cell to be written to memory.	0
EMEMDAV	3	RO	Extraction Memory Data Available This bit indicates the current Extraction Memory Data Available status. It is set to '1' when the extraction memory has an entire cell to be read from memory.	0
LCD	2	RO	Loss of Cell Delineation This bit indicates the current Loss of Cell Delineation status. It is set to '1' when the cell delineation state machine transitions from the SYNC state back to the HUNT state. This transition occurs after ALPHA (=7) consecutive incorrect HECs have been received, and it remains set until SYNC is achieved.	0
OCD	1:0	RO	Out of Cell Delineation These bits indicate the current Out of Cell Delineation status. When set to 'b11, they indicate that cell delineation is in the HUNT state. At the beginning of cell delineation, the state machine is in the HUNT state looking for a correct HEC. If a correct HEC is found, the state machine transitions to the PRESYNC state, represented by 'b01. If an incorrect HEC is detected before DELTA (=6) consecutive correct HECs are received, the state machine goes back to the HUNT state. If DELTA (=6) correct cells are detected consecutively, it proceeds to the SYNC state represented by the value of 'b00.	0

RXATC_IS - Interrupt Status Register - 'h04 (Part 1 of 3)

Field	Bits	Access	Function	Default
IMEMOFLW	9	RW1C	Insertion Memory Overflow Interrupt When this bit is set to '1', it indicates that the insertion memory has overflowed. Thus any attempt to write a cell to the extraction memory results in the cell being discarded.	0
EMEMOFLW	8	RW1C	Extraction Memory Overflow Interrupt When this bit is set to '1', it indicates that the extraction memory has overflowed. Thus any attempt to write a cell to the extraction memory results in the cell being discarded.	0

RXATC_IS - Interrupt Status Register - 'h04 (Part 2 of 3)

Field	Bits	Access	Function	Default
IMEMDAV	7	RW1C	Insertion Memory Data Available Interrupt When this bit is set to '1', it indicates that the insertion memory has room available for an entire cell to be written to memory.	0
EMEMDAV	6	RW1C	Extraction Memory Data Available Interrupt When this bit is set to '1', it indicates that the extraction memory has an entire cell available to be read from memory.	0
IMEMCELL	5	RW1C	Cell Insertion Interrupt When this bit is set to '1', it indicates that a cell has been drawn from memory, and been inserted into the data path.	0
EMEMCELL	4	RW1C	Cell Extraction Interrupt When this bit is set '1', it indicates that a cell has been extracted from the data path, and placed into the extraction memory.	0
UHEC	3	RW1C	Uncorrectable HEC Error Interrupt When this bit is set to '1', it indicates that an uncorrectable HEC error has been detected. Uncorrectable HEC errors occur for all multi-bit errors. It is also set for single bit errors, only when the HEC correction state machine has been disabled.	0
CHEC	2	RW1C	Correctable HEC Error Interrupt When this bit is set to '1', it indicates that a correctable HEC error has been detected. Correctable HEC errors occur for single bit errors only when the HEC correction state machine has been set to detect and correct.	0
LCD	1	RW1C	Loss of Cell Delineation Interrupt This bit indicates the Loss of Cell Delineation. It is set to '1' when the cell delineation state machine transitions from the SYNC state back to the HUNT state. This transition occurs after ALPHA (=7) consecutive incorrect HECs have been received.	0

RXATC_IS - Interrupt Status Register - 'h04 (Part 3 of 3)

Field	Bits	Access	Function	Default
OCD	0	RW1C	Out of Cell Delineation Interrupt This bit indicates the Out of Cell Delineation. If set to '1', this bit indicates that cell delineation is in the HUNT or PRESYNC state. At the beginning of the cell delineation, the state machine is in the HUNT state looking for a correct HEC. If one is found, it transitions to the PRESYNC state and remains there. If an incorrect HEC is detected before DELTA (=6) consecutive correct HECs are received, the state machine goes back to the HUNT state. If DELTA (=6) correct cells are detected consecutively, it proceeds to the SYNC state. This interrupt can only be cleared when the state machine is in the SYNC state.	0

RXATC_IE - Interrupt Enable Register - 'h06 (Part 1 of 2)

Field	Bits	Access	Function	Default
IMEMOFLW	9	RW	Insertion Memory Overflow Interrupt Enable This bit enables the Insertion Memory Overflow interrupt to be asserted on the IRQ line.	0
EMEMOFLW	8	RW	Extraction Memory Overflow Interrupt Enable This bit enables the Extraction Memory Overflow interrupt to be asserted on the IRQ line.	0
IMEMDAV	7	RW	Insertion Memory Data Available Interrupt Enable This bit enables the Insertion Memory Data Available interrupt to be asserted on the IRQ line.	0
EMEMDAV	6	RW	Extraction Memory Data Available Interrupt Enable This bit enables the Extraction Memory Data Available interrupt to be asserted on the IRQ line.	0
IMEMCELL	5	RW	Cell Insertion Interrupt Enable This bit enables the Cell Insertion interrupt to be asserted on the IRQ line.	0
EMEMCELL	4	RW	Cell Extraction Interrupt Enable This bit enables the Cell Extraction interrupt to be asserted on the IRQ line.	0
UHEC	3	RW	Uncorrectable HEC Error Interrupt Enable This bit enables the Uncorrectable HEC Error interrupt to be asserted on the IRQ line.	0
CHEC	2	RW	Correctable HEC Error Interrupt Enable This bit enables the Correctable HEC Error interrupt to be asserted on the IRQ line.	0

RXATC_IE - Interrupt Enable Register - 'h06 (Part 2 of 2)

Field	Bits	Access	Function	Default
LCD	1	RW	Loss of Cell Delineation Interrupt Enable This bit enables the Loss of Cell Delineation interrupt to be asserted on the IRQ line.	0
OCD	0	RW	Out of Cell Delineation Interrupt Enable This bit enables the Out of Cell Delineation interrupt to be asserted on the IRQ line.	0

RXATC_OAM - OAM Filter Control Register - 'h08 (Part 1 of 2)

Field	Bits	Access	Function	Default
MGFC	15:12	RW	Match GFC These four bits are used to include the specified GFC bits in the OAM filter pattern. When set to '0', the corresponding GFC bit is masked from the pattern and represents a don't care bit that matches both a logical one and logical zero.	4'b1111
MPT	11:9	RW	Match PT These three bits are used to include the specified PT bits in the OAM filter pattern. When set to '0', the corresponding PT bit is masked from the pattern and represents a don't care bit that matches both a logical one and logical zero.	3'b111
MCLP	8	RW	Match CLP This bit is used to include the specified CLP bit in the OAM filter pattern. When set to '0', the CLP bit is masked from the pattern and represents a don't care bit that matches both a logical one and a logical zero.	1'b1
GFC	7:4	RW	GFC These four bits identify the Generic Flow Control (GFC) bits of the first octet of the OAM filter pattern. Together, the GFC, PT, and CLP form a base filter pattern. Any header value matching this set pattern is discarded. The VPI and VCI for the OAM filter is statically set '0'. A GFC match can be used to exclude certain GFC bits from this filter pattern.	0
PT	3:1	RW	Payload Type These three bits are used to determine the payload type (PT) for filtering OAM cells. The PT bits precede the CLP bit found in the fourth octet. Together, the GFC, PT, and CLP form a base filter pattern. Any header value matching this set pattern is discarded. The VPI and VCI for the OAM filter is statically set '0'. A PT match can be used to exclude the PT bit from the OAM filter pattern.	0

RXATC_OAM - OAM Filter Control Register - 'h08 (Part 2 of 2)

Field	Bits	Access	Function	Default
CLP	0	RW	Cell Loss Priority When this bit is set to '1', it asserts the cell loss priority (CLP) of the OAM cell to '1'; otherwise it is set to '0'. The CLP is the last bit of the header found in the fourth octet. Together, the GFC, PT, and CLP bits form a base filter pattern. Any header value matching this set pattern is discarded. The VPI and VCI for the OAM filter is statically set '0'. A CLP match can be used to exclude certain CLP bits from the OAM filter pattern.	1'b1

RXATC_IMEM - Insertion Memory Access - 'h0A

Field	Bits	Access	Function	Default
SOP	8	RW	Insertion Memory SOP When this bit is '1', it indicates that the octet to be written to the insertion memory is the first word of the cell, or the start of cell. This bit is set when the first octet of the cell word is placed on the data line, and is not to be set again until the cell transaction has been completed, thus allowing for proper cell insertion. This bit should be set to '0' after the first octet has been written.	0
DAT	7:0	RW	Cell Insertion Memory Data When data is written to this location, the data is transferred to the Insertion Memory. To do an entire cell transfer, 53 octets must be written before the next cell of data can be accessed. Remember, sop MUST be set on the first octet of a cell to be placed into the insertion memory.	0

RXATC_EMEM - Extraction Memory Access - 'h0C (Part 1 of 2)

Field	Bits	Access	Function	Default
SOP	8	RO	Extraction Memory SOP When this bit is '1', it indicates that the octet to be read from the extraction memory is the first octet of the cell, or the start of cell. This bit is set when the first octet of the cell word is placed on the data line, and is not to be set again until the cell transaction has been completed.	0

RXATC_EMEM - Extraction Memory Access - 'h0C (Part 2 of 2)				
Field	**Bits**	**Access**	**Function**	**Default**
DAT	7:0	RO	Cell Insertion/Extraction Memory Data When data is read from this location, the data is transferred from the Extraction Memory. When data is written to this location, the data is transferred to the Insertion Memory. To do an entire cell transfer, 53-octets must be read before the next cell of data can be accessed. Remember, sop indicates the first octet of a cell.	0

RXATC_PM_ERR - Error Performance Monitoring - 'h20				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	Error Counter This 16-bit register represents the number of errors detected by the transmitter cell processor. It includes all header and Atlantic interface errors. The counter is incremented for each error, and will saturate after it reaches 'hFFFF.	0

RXATC_PM_CELL - Cell Performance Monitoring - 'h22				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	Cell Counter This 16-bit register represents the number of cells that have been written into the cell buffer. Cells that have been discarded due to HEC errors, filtering, or non-successful writes caused by an overflow of the cell buffer are not counted. This register is incremented for each cell that is successfully written. The counter will saturate after it reaches 'hFFFF.	0

RXATC_PM_DISC - Discard Cell Performance Monitoring - 'h24				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	Discarded Cell Counter This 16-bit register represents the number of discarded cells. HEC errors, filtering, or non-successful writes provoked by an overflow of the cell buffer cause cells to be discarded. This counter is incremented for each discarded cell, and will saturate after it reaches 'hFFFF.	0

RXATC_PM_CHEC - Correctable HEC Performance Monitoring - 'h26				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	Correctable HEC Counter This 16-bit register represents the number of cells that have had a single bit error and header corrected. This register is incremented when a correctable HEC sequence, in the HEC correction mode, is detected. The counter will saturate after it reaches 'hFFFF.	0

RXATC_PM_UHEC - Uncorrectable HEC Performance Monitoring - 'h28				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	Uncorrectable HEC Counter This 16-bit register represents the number of cells that have had a multi-bit error or an uncorrected single bit error in its HEC sequence. This register is incremented for each cell that has an uncorrected HEC sequence, and will saturate after it reaches 'hFFFF.	0

RXATC_PM_OAM - OAM Filter Performance Monitoring - 'h2A				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	OAM Filter Performance Monitoring This 16-bit register represents the number of cells that are filtered by the OAM filter. The criteria for cell filtering is based upon the OAM filter control register. This counter is incremented for cells that match the OAM filter pattern, and the entire cell is discarded. The counter will saturate after it reaches 'hFFFF.	0

RXATC_PM_FILT0 - Filter 0 Performance Monitoring - 'h2C				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	Filter Performance Monitoring This 16-bit register represents the number of cells that are filtered. The cell filtering criteria is based upon the associative CTRL, PAT and CHK filter registers. The filter must be enabled and match the cell based on the pattern, sense, and check for this register to be incremented. The counter will saturate after it reaches 'hFFFF.	0

RXATC_PM_FILT1 - Filter 1 Performance Monitoring - 'h2E				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	Filter Performance Monitoring This 16-bit register represents the number of cells that are filtered. The cell filtering criteria is based upon the associative CTRL, PAT and CHK filter registers. The filter must be enabled and match the cell based on the pattern, sense, and check for this register to be incremented. The counter will saturate after it reaches 'hFFFF.	0

RXATC_PM_FILT2 - Filter 2 Performance Monitoring - 'h30				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	Filter Performance Monitoring This 16-bit register represents the number of cells that are filtered. The cell filtering criteria is based upon the associative CTRL, PAT and CHK filter registers. The filter must be enabled and match the cell based on the pattern, sense, and check for this register to be incremented. The counter will saturate after it reaches 'hFFFF.	0

RXATC_PM_FILT3 - Filter 3 Performance Monitoring - 'h32				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	Filter Performance Monitoring This 16-bit register represents the number of cells that are filtered. The cell filtering criteria is based upon the associative CTRL, PAT and CHK filter registers. The filter must be enabled and match the cell based on the pattern, sense, and check for this register to be incremented. The counter will saturate after it reaches 'hFFFF.	0

RXATC_FILT0_CTRL - Filter 0 Control Register - 'h40				
Field	**Bits**	**Access**	**Function**	**Default**
ACT	3:2	RW	Filter Action These two bits control the filter action. If bit 2 is set to '1', the filter performs the copy cell action. If bit 2 is set to '0', the filter performs the don't copy cell action. If bit 1 is set to '1', the filter performs the discard cell action. If bit 1 is set to '0', the filter performs the enqueue cell action.	0
SEN	1	RW	Filter Sense This bit controls the filter mode. If set to '1', it acts on cells that matches the pattern. If set to '0', it acts on cells that do NOT match the pattern.	0
EN	0	RW	Filter Enable When this bit is set to '1', the filter is enabled.	0

RXATC_FILT0_PAT0 - Filter 0 Pattern - 'h42				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Pattern Lower These bits are the lower bit pattern that must match the first 32 bits of the incoming cell for the filter to take action. Note, only the bits with a corresponding bit set in the CHECK register are actually checked.	0

RXATC_FILT0_PAT1 - Filter 0 Pattern - 'h44				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Pattern Upper These bits are the upper bit pattern that must match the first 32 bits of the incoming cell for the filter to take action. Note, only the bits with a corresponding bit set in the CHECK register are actually checked.	0

RXATC_FILT0_CHK0 - Filter 0 Check - 'h46				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Check Lower These bits set the lower bits of the check area. Any bit position set to '1' is actually checked. The corresponding bit in PAT must match the corresponding bit in the incoming cell header for there to be a full match. Any bit position set to '0' is not checked, therefore the bit in the PAT is effectively a don't care bit.	0

RXATC_FILT0_CHK1 - Filter 0 Check - 'h48				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Check Lower These bits set the lower bits of the check area. Any bit position set to '1' is actually checked. The corresponding bit in PAT must match the corresponding bit in the incoming cell header for there to be a full match. Any bit position set to '0' is not checked, therefore the bit in the PAT is effectively a don't care bit.	0

RXATC_FILT1_CTRL - Filter 1 Control Register - 'h4A				
Field	**Bits**	**Access**	**Function**	**Default**
ACT	3:2	RW	Filter Action These two bits control the filter action. If bit 2 is set to '1', the filter performs the copy cell action. If bit 2 is set to '0', the filter performs the don't copy cell action. If bit 1 is set to '1', the filter performs the discard cell action. If bit 1 is set to '0', the filter performs the enqueue cell action.	0
SEN	1	RW	Filter Sense This bit controls the filter mode. If set to '1', it acts on cells that matches the pattern. If set to '0', it acts on cells that do NOT match the pattern.	0
EN	0	RW	Filter Enable When this bit is set to '1', the filter is enabled.	0

RXATC_FILT1_PAT0 - Filter 1 Pattern - 'h4C				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Pattern Lower These bits are the lower bit pattern that must match the first 32 bits of the incoming cell for the filter to take action. Note, only the bits with a corresponding bit set in the CHECK register are actually checked.	0

RXATC_FILT1_PAT1 - Filter 1 Pattern - 'h4E				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Pattern Upper These bits are the upper bit pattern that must match the first 32 bits of the incoming cell for the filter to take action. Note, only the bits with a corresponding bit set in the CHECK register are actually checked.	0

RXATC_FILT1_CHK0 - Filter 1 Check - 'h50				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Check Lower These bits set the lower bits of the check area. Any bit position set to '1' is actually checked. The corresponding bit in PAT must match the corresponding bit in the incoming cell header for there to be a full match. Any bit position set to '0' is not checked, therefore the bit in the PAT is effectively a don't care bit.	0

RXATC_FILT1_CHK1 - Filter 1 Check - 'h52				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Check Lower These bits set the lower bits of the check area. Any bit position set to '1' is actually checked. The corresponding bit in PAT must match the corresponding bit in the incoming cell header for there to be a full match. Any bit position set to '0' is not checked, therefore the bit in the PAT is effectively a don't care bit.	0

RXATC_FILT2_CTRL - Filter 2 Control Register - 'h54				
Field	**Bits**	**Access**	**Function**	**Default**
ACT	3:2	RW	Filter Action These two bits control the filter action. If bit 2 is set to '1', the filter performs the copy cell action. If bit 2 is set to '0', the filter performs the don't copy cell action. If bit 1 is set to '1', the filter performs the discard cell action. If bit 1 is set to '0', the filter performs the enqueue cell action.	0
SEN	1	RW	Filter Sense This bit controls the filter mode. If set to '1', it acts on cells that matches the pattern. If set to '0', it acts on cells that do NOT match the pattern.	0
EN	0	RW	Filter Enable When this bit is set to '1', the filter is enabled.	0

RXATC_FILT2_PAT0 - Filter 2 Pattern - 'h56				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Pattern Lower These bits are the lower bit pattern that must match the first 32 bits of the incoming cell for the filter to take action. Note, only the bits with a corresponding bit set in the CHECK register are actually checked.	0

RXATC_FILT2_PAT1 - Filter 2 Pattern - 'h58				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Pattern Upper These bits are the upper bit pattern that must match the first 32 bits of the incoming cell for the filter to take action. Note, only the bits with a corresponding bit set in the CHECK register are actually checked.	0

RXATC_FILT2_CHK0 - Filter 2 Check - 'h5A				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Check Lower These bits set the lower bits of the check area. Any bit position set to '1' is actually checked. The corresponding bit in PAT must match the corresponding bit in the incoming cell header for there to be a full match. Any bit position set to '0' is not checked, therefore the bit in the PAT is effectively a don't care bit.	0

RXATC_FILT2_CHK1 - Filter 2 Check - 'h5C				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Check Lower These bits set the lower bits of the check area. Any bit position set to '1' is actually checked. The corresponding bit in PAT must match the corresponding bit in the incoming cell header for there to be a full match. Any bit position set to '0' is not checked, therefore the bit in the PAT is effectively a don't care bit.	0

RXATC_FILT3_CTRL - Filter 3 Control Register - 'h5E				
Field	**Bits**	**Access**	**Function**	**Default**
ACT	3:2	RW	Filter Action These two bits control the filter action. If bit 2 is set to '1', the filter performs the copy cell action. If bit 2 is set to '0', the filter performs the don't copy cell action. If bit 1 is set to '1', the filter performs the discard cell action. If bit 1 is set to '0', the filter performs the enqueue cell action.	0
SEN	1	RW	Filter Sense This bit controls the filter mode. If set to '1', it acts on cells that matches the pattern. If set to '0', it acts on cells that do NOT match the pattern.	0
EN	0	RW	Filter Enable When this bit is set to '1', the filter is enabled.	0

RXATC_FILT3_PAT0 - Filter 3 Pattern - 'h60				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Pattern Lower These bits are the lower bit pattern that must match the first 32 bits of the incoming cell for the filter to take action. Note, only the bits with a corresponding bit set in the CHECK register are actually checked.	0

RXATC_FILT3_PAT1 - Filter 3 Pattern - 'h62				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Pattern Upper These bits are the upper bit pattern that must match the first 32 bits of the incoming cell for the filter to take action. Note, only the bits with a corresponding bit set in the CHECK register are actually checked.	0

RXATC_FILT3_CHK0 - Filter 3 Check - 'h64				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Check Lower These bits set the lower bits of the check area. Any bit position set to '1' is actually checked. The corresponding bit in PAT must match the corresponding bit in the incoming cell header for there to be a full match. Any bit position set to '0' is not checked, therefore the bit in the PAT is effectively a don't care bit.	0

RXATC_FILT3_CHK1 - Filter 3 Check - 'h66				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Check Lower These bits set the lower bits of the check area. Any bit position set to '1' is actually checked. The corresponding bit in PAT must match the corresponding bit in the incoming cell header for there to be a full match. Any bit position set to '0' is not checked, therefore the bit in the PAT is effectively a don't care bit.	0

TXATC Register Description

The following tables describe the registers for the transmitter section of the CP622.

TXATC_CTRL - Control Register - 'h80 (Part 1 of 2)				
Field	**Bits**	**Access**	**Function**	**Default**
GFCINS	9:6	RW	GFC Insert These bits determine whether or not each individually transmitted GFC bit should be inserted from the GFC serial input interface. When the bit is set to '1', the GFC bit is altered with the serial GFC bit. Otherwise, the value is not modified. GFC insertion provides the ability to insert a value into the GFC field of the header of an ATM cell. The GFC field is represented as the first four bits of the first header byte carrying information about local flow control. Insertion is done using a serial input port and controlled by a GFC enable register bit. If the GFC enable bit is not set, the existing GFC value is not modified. When enabled, the GFC value is inserted during each cell-processing period. If the next transmit cell is an idle/unassigned cell, and the GFC enable register bit is set, the GFC value in the Idle Cell Header register is overwritten.	0
HECCHK	5	RW	HEC Check When this bit is set to '1', the incoming HEC is checked against the regenerated HEC. When it is set to '0', the HEC error checking is disabled, and all HEC errors are ignored.	0
HECINV	4	RW	HEC Invert When this bit is set to '1', HEC inversion is performed.	0
HECADD	3	RW	HEC Addition When this bit is set to '1', it performs Modula 2 addition of x*6 + x*4 + x*2 + 1 ('b0101_0101) on the header, before HEC comparison.	1
HECRGN	2	RW	Regenerate the HEC When this bit is set to '1', the HEC for all cells with uncorrectable headers is regenerated. The generating polynomial is x*8 + x*2 + x + 1 with the optional modula 2 addition of x*6 + x*4 + x*2 + 1 based on the hecadd bit. The regenerate bit is set to '0' by default.	0
SCRAM	1	RW	Scrambling When this bit is set to '1', payload self-synchronous scrambling is performed, using the x*43 + 1 polynomial.	0

TXATC_CTRL - Control Register - 'h80 (Part 2 of 2)

Field	Bits	Access	Function	Default
EN	0	RW	Enable When this bit is '0', the cell processor is disabled. The cell processor remains in a static state and continues to ignore enables until it is set to '1'. Note, the CPU must set the EN bit to '1' before cell can be received.	1

TXATC_STAT - Status Register - 'h82

Field	Bits	Access	Function	Default
IMEMDAV	1	RO	Insertion Memory Data Available This bit indicates the current Insertion Memory Data Available status. It is set to '1' when the insertion memory has room for an entire cell to be written to memory.	0
EMEMDAV	0	RO	Extraction Memory Data Available This bit indicates the current Extraction Memory Data Available status. It is set to '1' when the extraction memory has an entire cell to be read from memory.	0

TXATC_IS - Interrupt Status Register - 'h84 (Part 1 of 2)

Field	Bits	Access	Function	Default
IMEMOFLW	7	RW1C	Insertion Memory Overflow Interrupt When this bit is '1', it indicates that an insertion memory overflow occurred. Any attempt to write a cell to the insertion memory cause the cell to be discarded.	0
EMEMOFLW	6	RW1C	Extraction Memory Overflow Interrupt When this bit is '1', it indicates that an extraction memory overflow occurred. Any attempt to write a cell to the extraction memory causes the cell to be discarded.	0
IMEMDAV	5	RW1C	Insertion Memory Data Available Interrupt When this bit is '1', it indicates that the insertion memory has room for an entire cell to be written to memory.	0
EMEMDAV	4	RW1C	Extraction Memory Data Available Interrupt When this bit is '1', it indicates that the extraction memory has an entire cell to be read from memory.	0
IMEMCELL	3	RW1C	Cell Insertion Interrupt When this bit is '1', it indicates that a cell has been drawn from memory and inserted into the data path.	0

TXATC_IS - Interrupt Status Register - 'h84 (Part 2 of 2)

Field	Bits	Access	Function	Default
EMEMCELL	2	RW1C	Cell Extraction Interrupt When this bit is '1', it indicates that a cell has been extracted from data path and put into memory.	0
AERR	1	RW1C	Atlantic Interface Error Interrupt If this bit is '1', it indicates a cell/packet error has been detected. This register is set when a cell/packet error is found on any word of an incoming cell entering the cell processor.	0
HERR	0	RW1C	HEC Error Interrupt If this bit is '1', it indicates a HEC error has been detected. The criteria is based upon the HEC options found in the control register.	0

TXATC_IE - Interrupt Enable Register - 'h86

Field	Bits	Access	Function	Default
IMEMOFLW	7	RW	Insertion Memory Overflow Interrupt Enable This bit enables the Insertion Memory Overflow interrupt to be asserted on the IRQ line.	0
EMEMOFLW	6	RW	Extraction Memory Overflow Interrupt Enable This bit enables the Extraction Memory Overflow interrupt to be asserted on the IRQ line.	0
IMEMDAV	5	RW	Insertion Memory Data Available Interrupt Enable This bit enables the Insertion Memory Data Available interrupt to be asserted on the IRQ line.	0
EMEMDAV	4	RW	Extraction Memory Data Available Interrupt Enable This bit enables the Extraction Memory Data Available interrupt to be asserted on the IRQ line.	0
IMEMCELL	3	RW	Cell Insertion Interrupt Enable This bit enables the Cell Insertion interrupt to be asserted on the IRQ line.	0
EMEMCELL	2	RW	Cell Extraction Interrupt Enable This bit enables the Cell Extraction interrupt to be asserted on the IRQ line.	0
AERR	1	RW	Atlantic Interface Error Interrupt Enable This bit enables the Cell/Packet Error interrupt to be asserted on the IRQ line.	0
HERR	0	RW	HEC Error Interrupt Enable This bit enables the HEC Error interrupt to be asserted on the IRQ line.	0

TXATC_OAM - OAM Filter Control Register - 'h88				
Field	**Bits**	**Access**	**Function**	**Default**
MGFC	15:12	RW	Match GFC These four bits are used to include the specified GFC bits in the OAM filter pattern. When set to '0', the corresponding GFC bit is masked from the pattern and represents a don't care bit that matches both a logical one and a logical zero.	4'b1111
MPT	11:9	RW	Match PT These three bits are used to include the specified PT bits in the OAM filter pattern. When set to '0', the corresponding PT bit is masked from the pattern and represents a don't care bit that matches both a logical one and a logical zero.	3'b111
MCLP	8	RW	Match CLP This bit is used to include the specified CLP bit in the OAM filter pattern. When set to '0', the CLP bit is masked from the pattern and represents a don't care bit that matches both a logical one and a logical zero.	1'b1
GFC	7:4	RW	GFC These four bits are used to identify the Generic Flow Control (GFC) bits of the first octet of the OAM filter pattern. Together, the GFC, PT, and CLP form a base filter pattern. Any header value matching this set pattern is discarded. The VPI and VCI for the OAM filter is statically set '0'. A GFC match can be used to exclude certain GFC bits from this filter pattern.	0
PT	3:1	RW	Payload Type These three bits are used to determine the payload type (PT) for filtering OAM cells. The PT bits precede the CLP bit found in the fourth octet. Together, the GFC, PT, and CLP form a base filter pattern. Any header value matching this set pattern is discarded. The VPI and VCI for the OAM filter is statically set '0'. A PT match can be used to exclude the PT bit from the OAM filter pattern.	0
CLP	0	RW	Cell Loss Priority When this bit is set to '1', it asserts the cell loss priority (CLP) of the OAM cell to '1'; otherwise it is '0'. The CLP is the last bit of the header found in the fourth octet. Together, the GFC, PT, and CLP bits form a base filter pattern. Any header value matching this set pattern is discarded. The VPI and VCI for the OAM filter is statically set '0'. A CLP match can be used to exclude certain CLP bits from the OAM filter pattern.	1'b1

TXATC_IDLE - Idle Cell Control Register - 'h8A				
Field	**Bits**	**Access**	**Function**	**Default**
PYLD	15:8	RW	Payload These eight bits are used to represent the pattern inserted as payload in idle cells. Idle cells are defaulted to the UNI idle cell payload of 'b01101010.	8'h6A
GFC	7:4	RW	GFC These four bits are used to set GFC bits of the idle cell header. Idle cells are defaulted to 'b0000.	0
PT	3:1	RW	Payload Type These three bits are used to set the PT bits of the idle cell header. Idle cells are defaulted to '0'.	0
CLP	0	RW	Cell Loss Priority This bit is used to set the CLP bit of the idle cell header. Idle cells are defaulted to '1'.	1

TXATC_IMEM - Insertion Memory Access - 'h8C				
Field	**Bits**	**Access**	**Function**	**Default**
SOP	8	RW	Insertion Memory SOP When this bit is '1', it indicates that the octet to be written to the insertion memory is the first word of the cell, or the start of cell. This bit must be set in conjunction with the first octet of the cell word being placed on the data line, and not be set again until the cell transaction has been completed, thus allowing for proper cell insertion. After the first octet has been written, this bit should be set to '0'.	0
DAT	7:0	RW	Cell Insertion Memory Data When data is written to this location, the data is transferred to the Insertion Memory. To do an entire cell transfer, 53-octets must be written before the next cell of data can be accessed. Remember, sop must be set on the first octet of a cell to be placed into the insertion memory.	0

TXATC_EMEM - Extraction Memory Access - 'h8E				
Field	**Bits**	**Access**	**Function**	**Default**
SOP	8	RO	Extraction Memory SOP When this bit is '1', it indicates that the octet to be read from the extraction memory is the first octet of the cell, or the start of cell. This bit is set in conjunction with the first octet of the cell word being placed on the data line, and shall not be set again until the cell transaction has been completed.	0
DAT	7:0	RO	Cell /Extraction Memory Data When data is read from this location, the data is transferred from the Extraction Memory. When data is written to this location, the data is transferred to the Insertion Memory. To do an entire cell transfer, 53-octets must be read before the next cell of data can be accessed. Remember, sop indicates the first octet of a cell.	0

TXATC_PM_ERR - Error Performance Monitoring - 'hA0				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	Error Counter This 16-bit register represents the number of errors detected by the transmitter cell processor, including all header and Atlantic interface errors. This register is incremented for each error, and will saturate after it reaches 'hFFFF.	0

TXATC_PM_CELL - Cell Performance Monitoring - 'hA2				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	Cell Counter This 16-bit register represents the number of cells that have been read from the cell buffer, and that have not been discarded because of filtering or overflow conditions. This register is incremented for each cell successfully read, and will saturate after it reaches 'hFFFF.	0

TXATC_PM_DISC - Discard Cell Performance Monitoring - 'hA4				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	Discarded Cell Counter This 16-bit register represents the number of cells that have been discarded through cell filtering. This register is incremented for each discarded cell, and will saturate after it reaches 'hFFFF.	0

TXATC_PM_HERR - HEC Error Performance Monitoring - 'hA6				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	HEC Error Counter This 16-bit register represents the number of cells that have a HEC error. This register is incremented when a cell HEC error is detected, and will saturate after it reaches 'hFFFF.	0

TXATC_PM_AERR - Atlantic Error Performance Monitoring - 'hA8				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	Atlantic Interface Error Counter This 16-bit register represents the number of cells that have an Atlantic Interface error. This register is incremented for each cell with this error, and will saturate after it reaches 'hFFFF.	0

TXATC_PM_OAM - OAM Filter Performance Monitoring - 'hAA				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	OAM Filter Performance Monitoring This 16-bit register represents the number of cells that are filtered by the OAM filter. The cell filtering criteria is based upon the OAM filter control register. This register is incremented for cells that match the OAM filter pattern, and the entire cell is discarded. The counter will saturate after it reaches 'hFFFF.	0

TXATC_PM_FILT0 - Filter 0 Performance Monitoring - 'hAC				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	Filter Performance Monitoring This 16-bit register represents the number of cells that are filtered. The cell filtering criteria is based upon the associative CTRL, PAT and CHK filter registers. The filter must be enabled and match the cell based on the pattern, sense, and check for this register to be incremented. The counter will saturate after it reaches 'hFFFF.	0

TXATC_PM_FILT1 - Filter 1 Performance Monitoring - 'hAE				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	Filter Performance Monitoring This 16-bit register represents the number of cells that are filtered. The cell filtering criteria is based upon the associative CTRL, PAT and CHK filter registers. The filter must be enabled and match the cell based on the pattern, sense, and check for this register to be incremented. The counter will saturate after it reaches 'hFFFF.	0

TXATC_PM_FILT2 - Filter 2 Performance Monitoring - 'hB0				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	Filter Performance Monitoring This 16-bit register represents the number of cells that are filtered. The cell filtering criteria is based upon the associative CTRL, PAT and CHK filter registers. The filter must be enabled and match the cell based on the pattern, sense, and check for this register to be incremented. The counter will saturate after it reaches 'hFFFF.	0

TXATC_PM_FILT3 - Filter 3 Performance Monitoring - 'hB2				
Field	**Bits**	**Access**	**Function**	**Default**
CNT	15:0	RTCW	Filter Performance Monitoring This 16-bit register represents the number of cells that are filtered. The cell filtering criteria is based upon the associative CTRL, PAT and CHK filter registers. The filter must be enabled and match the cell based on the pattern, sense, and check for this register to be incremented. The counter will saturate after it reaches 'hFFFF.	0

TXATC_FILT0_CTRL - Filter 0 Control Register - 'hC0				
Field	**Bits**	**Access**	**Function**	**Default**
ACT	3:2	RW	Filter Action These two bits control the filter action. If bit 2 is set to '1', the filter performs the copy cell action. If bit 2 is set to '0', the filter performs the don't copy cell action. If bit 1 is set to '1', the filter performs the discard cell action. If bit 1 is set to '0', the filter performs the enqueue cell action.	0
SEN	1	RW	Filter Sense This bit controls the filter mode. If set to '1', it acts on cells that match the pattern. If set to '0', it acts on cells that do NOT match the pattern.	0
EN	0	RW	Filter Enable When this bit is set to '1', the filter is enabled.	0

TXATC_FILT0_PAT0 - Filter 0 Pattern - 'hC2				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Pattern Lower These bits are the lower bit pattern that must match the first 32 bits of the incoming cell for the filter to take action. Note, only the bits with a corresponding bit set in the CHECK register are actually checked.	0

TXATC_FILT0_PAT1 - Filter 0 Pattern - 'hC4				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Pattern Upper These bits are the upper bit pattern that must match the first 32 bits of the incoming cell for the filter to take action. Note, only the bits with a corresponding bit set in the CHECK register are actually checked.	0

TXATC_FILT0_CHK0 - Filter 0 Check - 'hC6				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Check Lower These bits set the lower bits of the check area. Any bit position set to '1' is actually checked. The corresponding bit in PAT must match the corresponding bit in the incoming cell header for there to be a full match. Any bit position set to '0' is not checked, therefore the bit in the PAT is effectively a don't care bit.	0

TXATC_FILT0_CHK1 - Filter 0 Check - 'hC8				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Check Lower These bits set the lower bits of the check area. Any bit position set to '1' is actually checked. The corresponding bit in PAT must match the corresponding bit in the incoming cell header for there to be a full match. Any bit position set to '0' is not checked, therefore the bit in the PAT is effectively a don't care bit.	0

TXATC_FILT1_CTRL - Filter 1 Control Register - 'hCA (Part 1 of 2)				
Field	**Bits**	**Access**	**Function**	**Default**
ACT	3:2	RW	Filter Action These two bits control the filter action. If bit 2 is set to '1', the filter performs the copy cell action. If bit 2 is set to '0', the filter performs the don't copy cell action. If bit 1 is set to '1', the filter performs the discard cell action. If bit 1 is set to '0', the filter performs the enqueue cell action.	0

TXATC_FILT1_CTRL - Filter 1 Control Register - 'hCA (Part 2 of 2)

Field	Bits	Access	Function	Default
SEN	1	RW	Filter Sense This bit controls the filter mode. If set to '1', it acts on cells that match the pattern. If set to '0', it acts on cells that do NOT match the pattern.	0
EN	0	RW	Filter Enable When this bit is set to '1', the filter is enabled.	0

TXATC_FILT1_PAT0 - Filter 1 Pattern - 'hCC

Field	Bits	Access	Function	Default
MATCH	15:0	RW	Filter Pattern Lower These bits are the lower bit pattern that must match the first 32 bits of the incoming cell for the filter to take action. Note, only the bits with a corresponding bit set in the CHECK register are actually checked.	0

TXATC_FILT1_PAT1 - Filter 1 Pattern - 'hCE

Field	Bits	Access	Function	Default
MATCH	15:0	RW	Filter Pattern Upper These bits are the upper bit pattern that must match the first 32 bits of the incoming cell for the filter to take action. Note, only the bits with a corresponding bit set in the CHECK register are actually checked.	0

TXATC_FILT1_CHK0 - Filter 1 Check - 'hD0

Field	Bits	Access	Function	Default
MATCH	15:0	RW	Filter Check Lower These bits set the lower bits of the check area. Any bit position set to '1' is actually checked. The corresponding bit in PAT must match the corresponding bit in the incoming cell header for there to be a full match. Any bit position set to '0' is not checked, therefore the bit in the PAT is effectively a don't care bit.	0

TXATC_FILT1_CHK1 - Filter 1 Check - 'hD2				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Check Lower These bits set the lower bits of the check area. Any bit position set to '1' is actually checked. The corresponding bit in PAT must match the corresponding bit in the incoming cell header for there to be a full match. Any bit position set to '0' is not checked, therefore the bit in the PAT is effectively a don't care bit.	0

TXATC_FILT2_CTRL - Filter 2 Control Register - 'hD4				
Field	**Bits**	**Access**	**Function**	**Default**
ACT	3:2	RW	Filter Action These two bits control the filter action. If bit 2 is set to '1', the filter performs the copy cell action. If bit 2 is set to '0', the filter performs the don't copy cell action. If bit 1 is set to '1', the filter performs the discard cell action. If bit 1 is set to '0', the filter performs the enqueue cell action.	0
SEN	1	RW	Filter Sense This bit controls the filter mode. If set to '1', it acts on cells that match the pattern. If set to '0', it acts on cells that do NOT match the pattern.	0
EN	0	RW	Filter Enable When this bit is set to '1', the filter is enabled.	0

TXATC_FILT2_PAT0 - Filter 2 Pattern - 'hD6				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Pattern Lower These bits are the lower bit pattern that must match the first 32 bits of the incoming cell for the filter to take action. Note, only the bits with a corresponding bit set in the CHECK register are actually checked.	0

TXATC_FILT2_PAT1 - Filter 2 Pattern - 'hD8				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Pattern Upper These bits are the upper bit pattern that must match the first 32 bits of the incoming cell for the filter to take action. Note, only the bits with a corresponding bit set in the CHECK register are actually checked.	0

TXATC_FILT2_CHK0 - Filter 2 Check - 'hDA				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Check Lower These bits set the lower bits of the check area. Any bit position set to '1' is actually checked. The corresponding bit in PAT must match the corresponding bit in the incoming cell header for there to be a full match. Any bit position set to '0' is not checked, therefore the bit in the PAT is effectively a don't care bit.	0

TXATC_FILT2_CHK1 - Filter 2 Check - 'hDC				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Check Lower These bits set the lower bits of the check area. Any bit position set to '1' is actually checked. The corresponding bit in PAT must match the corresponding bit in the incoming cell header for there to be a full match. Any bit position set to '0' is not checked, therefore the bit in the PAT is effectively a don't care bit.	0

TXATC_FILT3_CTRL - Filter 3 Control Register - 'hDE (Part 1 of 2)				
Field	**Bits**	**Access**	**Function**	**Default**
ACT	3:2	RW	Filter Action These two bits control the filter action. If bit 2 is set to '1', the filter performs the copy cell action. If bit 2 is set to '0', the filter performs the don't copy cell action. If bit 1 is set to '1', the filter performs the discard cell action. If bit 1 is set to '0', the filter performs the enqueue cell action.	0

TXATC_FILT3_CTRL - Filter 3 Control Register - 'hDE (Part 2 of 2)				
Field	**Bits**	**Access**	**Function**	**Default**
SEN	1	RW	Filter Sense This bit controls the filter mode. If set to '1', it acts on cells that match the pattern. If set to '0', it acts on cells that do NOT match the pattern.	0
EN	0	RW	Filter Enable When this bit is set to '1', the filter is enabled.	0

TXATC_FILT3_PAT0 - Filter 3 Pattern - 'hE0				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Pattern Lower These bits are the lower bit pattern that must match the first 32 bits of the incoming cell for the filter to take action. Note, only the bits with a corresponding bit set in the CHECK register are actually checked.	0

TXATC_FILT3_PAT1 - Filter 3 Pattern - 'hE2				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Pattern Upper These bits are the upper bit pattern that must match the first 32 bits of the incoming cell for the filter to take action. Note, only the bits with a corresponding bit set in the CHECK register are actually checked.	0

TXATC_FILT3_CHK0 - Filter 3 Check - 'hE4				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Check Lower These bits set the lower bits of the check area. Any bit position set to '1' is actually checked. The corresponding bit in PAT must match the corresponding bit in the incoming cell header for there to be a full match. Any bit position set to '0' is not checked, therefore the bit in the PAT is effectively a don't care bit.	0

TXATC_FILT3_CHK1 - Filter 3 Check - 'hE6				
Field	**Bits**	**Access**	**Function**	**Default**
MATCH	15:0	RW	Filter Check Lower These bits set the lower bits of the check area. Any bit position set to '1' is actually checked. The corresponding bit in PAT must match the corresponding bit in the incoming cell header for there to be a full match. Any bit position set to '0' is not checked, therefore the bit in the PAT is effectively a don't care bit.	0

Core Verification Summary

The full-feature variant of the CP622 was the object of very thorough verification, and should operate according to industry standards. The CP622 was tested by simulation, and for third-party compatibility. Both testing environments are described briefly, including the number of test programs, and their results.

Simulation Environment

The CP622 was simulated using behavioral utilities with multiple simulators, including but not limited to ModelSim AE. The behavioral utilities consist of generic flow control generators and monitors, Midbus generators and monitors, Atlantic generators and monitors, an AIRbus master model, and clock generators.

A test suite using the utilities and the RTL model of the CP622 was used to verify the proper operation of all the features listed on page 12. Table 6 lists the results of the simulation for the full-feature variant of the CP622

Table 6. Results	
Number of test programs *(1)*	56
Number of test programs passing	56
Number of test programs failing	0
Number of test cases *(1)*	118
Number of test cases passing	118
Number of test cases failing	0

Note:
(1) Each test program contains at least one test case.

Compatibility Testing Environment

The full-feature variant of the CP622 was evaluated—within an APEX EP20K1000EFC672 device—against a commercial third-party cell processor with similar features, as required by industry standards. For testing purposes, the CP622 was interconnected with the Altera STS12CFRM MegaCore function, and the Altera PCI MegaCore function was used to interface to the AIRbus and to the third-party cell processor. Figure 5 shows the test board used.

Software from a host PC was used to set registers on the CP622, and the third-party cell processor. The effects of setting these registers, and any corresponding registers, were observed to determine functionality. Tests were run for extended periods of time, thereby testing millions of cells.

Figure 5. Test Board

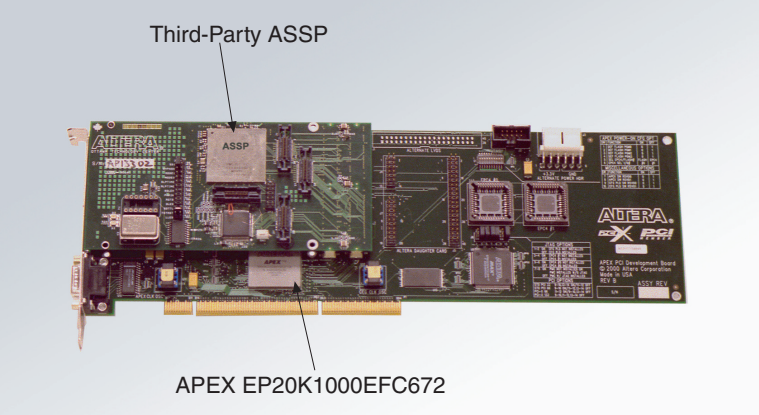


Table 7 lists the results of the hardware verification for the full-feature variant of the CP622.

Table 7. Results

Number of test programs *(1)*	15
Number of test programs passing	15
Number of test programs failing	0
Number of test cases *(1)*	27
Number of test cases passing	27
Number of test cases failing	0

Note:
(1) Each test program contains at least one test case.

Getting Started

User Guide

This section describes how to obtain a variant from the ATM Cell Processor 622 Mbps MegaCore® Function (CP622). It explains how to install the CP622 on your PC, and walks you through the process of implementing the variant in a design.

You can test-drive a CP622 using the Altera® OpenCore® feature—within the Quartus® II software—to instantiate it, to perform place-and-route, to perform static timing analysis, and to simulate it using a third-party simulator, within your custom logic. You only need licenses when you are ready to generate programming files.

Design Walkthrough

This design walkthrough involves the following steps:

1. Obtaining and installing the CP622 MegaCore Function.
2. Generating a custom CP622 for your system using the MegaWizard® Plug-In.
3. Implementing the rest of your system using AHDL, VHDL, or Verilog HDL.
4. Simulating the CP622 within your design.
5. Synthesis, compilation, and place-and-route.
6. Licensing the CP622 to configure the device.
7. Performing post-routing simulation.

The instructions assume that:

- You are using a PC
- You are familiar with the Quartus II software.
- The Quartus II software (the newest version) is installed in the default location.
- You are using the OpenCore feature to test-drive a CP622, or you have licensed it.

Obtaining & Installing the CP622

To start using the CP622, you need to obtain the MegaCore package, which includes the following:

- Data sheet
- User guide
- AIRbus, Midbus, and Atlantic interface functional specifications
- MegaWizard Plug-In
  - Encrypted gate level netlist
  - Place-and-route constraints (where necessary)
  - Secure RTL simulation model
- Demo testbench
- Access to problem reporting system

Downloading the MegaCore Function

If you have Internet access, you can download the ATM Cell Processor 622 Mbps MegaCore function from the Altera web site. Follow the instructions below to obtain the core via the Internet. If you do not have Internet access, you can obtain the core from your local Altera representative.

1. Point your web browser at http://www.altera.com/IPmegastore.
2. In the IP MegaSearch **keyword** field type `ATM`.
3. Click the link for the ATM Cell Processor 622 Mbps MegaCore function.
4. On the product page, click the *Free Test-Drive* icon.
5. Follow the on-line instructions to download the function and save it to your hard disk.

Installing the MegaCore Files

Use the MegaWizard Plug-In to generate the files and install them on your PC. The following instructions describe this process.

For UNIX systems, you must have Java runtime environment version 1.3 before you can use the MegaWizard Plug-In. You can download this file from the Java web site at http://www.java.sun.com.

For Windows, follow the instructions below:

1. Click **Run** (Start menu).

2. Type <*path name*>\<*filename*>**.exe**, where <*path name*> is the location of the downloaded CP622 and <*filename*> is the filename of the CP622. Click **OK**.

3. The **MegaCore Installer** dialog box appears. Follow the MegaWizard Plug-In instructions to finish the installation.

4. Disregard this step if you are using Quartus II version 1.1 or higher. Otherwise, after you have finished installing the files, you must specify the directory in which you installed them as a user library in the Quartus II software. Search for "User Libraries" in Quartus II Help for instructions on how to add these libraries.

Generating a custom CP622

This section describes the design flow using the ATM Cell Processor MegaCore function and the Quartus II development system. A MegaWizard Plug-In is provided with the CP622. The MegaWizard Plug-In Manager—used within the Quartus II software—allows you to create or modify design files to meet the needs of your application. You can then instantiate the CP622 in your design file.

To create a custom CP622 using the MegaWizard Plug-In, follow these steps:

1. Start the MegaWizard Plug-In by choosing the MegaWizard Plug-In Manager command (Tools menu) in the Quartus II software. The **MegaWizard Plug-In Manager** dialog box is displayed.

Refer to Quartus II Help for detailed instructions on how to use the MegaWizard Plug-In Manager.

2. Specify that you want to create a new custom variant and click **Next**.

3. On the second page of the MegaWizard Plug-In, open the **Communications** folder, and select the CP622 from the **ATM** folder.

4. Choose the type of output files (language), specify the folder and name for the files the MegaWizard Plug-In creates, and click **Next**.

5. Select the optional parameters and choices that you require.

6. The final screen lists the design files created by the MegaWizard Plug-In, and indicates the location of the simulation models for the selected variant. Click **Finish.**

Implementing the System

Once you have created your CP622, you are ready to implement it. You can use the files generated by the MegaWizard Plug-In, and use the Quartus II software or other EDA tools to create your design. Table 1 lists the generated files.

Table 1. MegaWizard Plug-In Files

Description	Verilog HDL	VHDL	AHDL
Design File Wrapper	.v	.vhd	.tdf
Sample Instantiation	_inst.v	_inst.vhd	_inst.tdf
Black Box Module	_bb.v	–	–
Symbol files for the Quartus II software used to instantiate the CP622 into a schematic design	.bsf	.bsf	.bsf
An encrypted HDL netlist file	.e.vqm.v	.e.vqm.v	.e.vqm.v

Simulating Your Design

Altera provides three models to be used for functional verification of the CP622 within your design. A Verilog demo testbench, including scripts to run it, is also provided. This demo testbench used with the ModelSim AE simulator demonstrates how to instantiate a model in a design.

To find the simulation models for your selected variant, refer to the last page of the MegaWizard Plug-In Manager. These models and the demo testbench are located on your hard drive, the paths are:

- **sim_lib/<*variant*>/modelsim_verilog/**
- **sim_lib/<*variant*>/modelsim_vhdl/**
- **sim_lib/<*variant*>/visual_ip/**
- **sim_lib/<*variant*>/test/**

<*variant*> is a unique code (aotXXXX_#_cp622) assigned to the specific configuration requested through the MegaWizard Plug-In.

Using the Verilog Demo Testbench

The demo testbench includes some simple stimulus to control the user interfaces of the CP622. Each CP622 variant includes scripts to compile and run the demo testbench using a variety of simulators and models.

Using the Visual IP Software

The Visual IP software facilitates the use of Visual IP simulation models with third-party simulation tools. To view a simulation model, you must have the Visual IP software installed on your system. To download the software, or for instructions on how to use the software, refer to the Altera web site at http://www.altera.com, and search for `Visual IP`. For examples of how to use the provided Visual IP model, refer to the sample scripts included with the demo testbench.

Synthesis, Compilation & Place & Route

After you have verified that your design is functionally correct, you are ready to perform synthesis and place-and-route. Synthesis can be performed by the Quartus II development tool, or by a third-party synthesis tool. The Quartus II software works seamlessly with tools from many EDA vendors, including Cadence, Exemplar Logic, Mentor Graphics, Synopsys, Synplicity, and Viewlogic.

Using Third-Party EDA Tools for Synthesis

To synthesize your design in a third-party EDA tool, follow these steps:

1. Create your custom design instantiating a CP622.
2. Synthesize the design using your third-party EDA tool. Your EDA tool should treat the CP622 instantiation as a black box by either setting attributes or ignoring the instantiation.
3. After compilation, generate a netlist file in your third-party EDA tool.

Using the Quartus II development tool for compilation and place-and-route

To use the Quartus II software to compile and place-and-route your design, follow these steps:

1. Select **Compile mode** (Processing menu).
2. Specify the Compiler settings in the **Compiler Settings** dialog box (Processing menu) or use the Compiler Settings wizard.
3. Disregard this step if you are using Quartus II version 1.1 or higher. Otherwise, specify the user libraries for the project and the order in which the Compiler searches the libraries.

4. Specify the input settings for the project. Choose **EDA Tool Settings** (Project menu). Select **Custom EDIF** in the Design entry/synthesis tool list. Click **Settings**. In the **EDA Tool Input Settings** dialog box, make sure that the relevant tool name or option is selected in the **Design Entry/Synthesis Tool** list.
5. Add your third-party EDA tool-generated netlist file to your project.
6. Add any **.tdf**, **.vhd**, or **.v** files not synthesized in the third-party tool.
7. Add the pre-synthesized and encrypted **.e.vqm.v** file from your working directory, created by the MegaWizard Plug-In Manager.
8. Constrain your design as needed.
9. Compile your design. The Quartus II Compiler synthesizes and performs place-and-route on your design.

Refer to Quartus II Help for further instructions on performing compilation.

Licensing for Configuration

After you have compiled and analyzed your design, you are ready to configure your targeted Altera semiconductor device. If you are evaluating the CP622 with the OpenCore feature, you must license the function before you can generate programming files. To obtain licenses contact your local Altera sales representative.

All current CP622 variants use a single license, with ordering code: PLSM-CP622.

Performing Post-Routing Simulation

After you have licensed the CP622, you can generate EDIF, VHDL, Verilog HDL, and Standard Delay Output Files from the Quartus II software and use them with your existing EDA tools to perform functional modeling and post-routing simulation of your design.

1. Open your existing Quartus II project.
2. Depending on the type of output file you want, specify Verilog HDL output settings or VHDL output settings in the **General Settings** dialog box (Project menu).
3. Compile your design with the Quartus II software, refer to the "Using the Quartus II development tool for compilation and place-and-route"section. The Quartus II software generates output and programing files.

4. You can now import your Quartus II software-generated output files (**.edo**, **.vho**, **.vo**, or .**sdo**) into your third-party EDA tool for post-route, device-level, and system-level simulation.

Notes: