Power Management in Portable Systems Using MAX II CPLDs

Introduction

Portable system designers are concerned with minimizing the static and dynamic current draw of all components within a battery-powered system. This application note highlights the very low static and dynamic power capabilities of MAX® II CPLDs. It also reviews circuit design techniques that allow MAX II devices to achieve zero stand-by current. In addition, MAX II devices can be used as a smart power control manager to power-up and power-down other system components making them zero power.

Battery-Powered Portable Applications

Power management is critical in all electronic applications, but it is even more critical in portable battery-powered applications. Portable electronic applications began with calculators and radios and have grown over the last decade to include popular products such as cell phones, Personal Digital Assistants (PDAs), and MP3 Players. Portability does not stop at consumer gadgets. Many commercial necessities are increasingly becoming portable:

- Bar code scanners
- Point of sale terminals
- Tax collection terminals
- Electronic toll readers
- PIN identification systems
- Radio Frequency Identification Device (RFID) readers/scanners

Increasingly, with the introduction of wireless standards such as BlueTooth, Wireless Fidelity (WiFi), and 802.11e, many industrial applications are no longer limited by wiring or power infrastructure. Portable industrial applications that take advantage of the wireless revolution include:

- Gas and hazardous material sensors
- Global Positioning System (GPS)-based inventory monitors
- Production line and surveillance cameras
- Strain and stress gauges
- Remote operator terminals
- Virtual private networks
- Test and measurement equipment
- Heating Ventilation and Air Conditioning (HVAC) monitor and control systems

Many of these applications are battery-powered. The batteries are ideally alkaline, NiCad, or Lithium-Polymer. All these battery types support an operating voltage range from 3.2 volts (V) (when fully charged) to 2.2 V (when discharged). The most effective device on the Printed Circuit Board (PCB) is the one with the widest operating range. This application note reviews the power advantages of MAX II CPLDs in battery-powered portable applications. It also introduces reference circuits and design techniques for optimum power management in MAX II CPLD-based systems.

Power Management in Portable Systems

Power management is more than simply achieving the lowest standby power dissipation possible. There are three aspects of power design: dissipation, simplicity, and transitions.

Dissipation is the most obvious power management reduction objective of system designers. Power dissipation has two basic components: static power and dynamic power. In most applications, dynamic power is more important for extending battery life, while in some applications, static power is more important. Static power is most important in applications in which battery service is an inconvenience and dynamic activity is only occasional. An example in which static power is important might be a remote HVAC control panel. The HVAC control panel is only used occasionally and is mostly dormant. An example in which dynamic power is most critical is an industrial PDA. The PDA processor, display, and back light source are indispensable and are the dominate source of power dissipation; most other aspects of the design are incidental to the total power dissipation and battery life. Furthermore, in a PDA application, the battery life is designed so the product is functional between charges and the standby life of the batteries is usually not a concern.

Simplicity is another important consideration in power management. Low dynamic or static power dissipation is desirable, but not always at any cost. The power system needs to be as simple as possible. In battery-powered systems, multiple power rails may be prohibitive. A device component that allows for a wide operating voltage range is very desirable. Dividing a system into many power domains and to enable each domain only when its function is required by the system is one way to approach the problem. However, it is critical that a system with multiple domains have a flexible control mechanism and that each domain be easy to power up and power down. The MAX II device has the flexibility to control a very complex set of power domains. MAX II devices have simple power requirements and hot-socket characteristics that make it easy to manage as part of a dynamically controlled power domain.

Transitions are also important considerations in power management. A typical power management system is constantly transitioning from one power mode to another. It is important to understand the characteristics of the components in the system as they transition from on to off and off to on, as well as how they behave when off. Depending on the hot-socket characteristics of a device, a part may burn more power parasitically in the off state then in the on state due to poor hot-socket characteristics. The behavior of MAX II devices in all states and transitions is explored to enable designers to choose the optimum modes for their application.

MAX II CPLD Power Advantage

MAX II devices have many power system characteristics that are beneficial to portable applications. The MAX II device has two core power options. The most useful is the standard device that has a built-in core voltage regulator. The 180-nm core internal VCC requires a 1.8 V power supply. MAX II devices with the MultiVolt™core are easier to use than CoolRunner II devices. The V_{CCINT} can range from 2.35 V to 3.6 V, while the built-in regulator supplies 1.8 V to the core. If supplying the 1.8 V core voltage is optimum for an application, the MAX IIG device allows a supply range of 1.65 V to 1.95 V. The standard voltage for battery-powered systems is 3.0 V, whether it is from two alkaline cells or a single lithium polymer battery. In such systems, the battery supply can vary from 3.2 V to 2.3 V and the MAX II device continues to work. The MAX II device also has MultiVolt I/Os that allow the V_{CCIO} voltage to work over the same range as the core voltage regulator. This allows for a very simple power system in which the V_{CCIO} and the V_{CCINT} are tied together and monitored as the battery voltage declines over its useful life. Figure 1 shows the battery life curve for a typical lithium polymer battery.

Figure 1. Typical Lithium Polymer Battery Life Curve
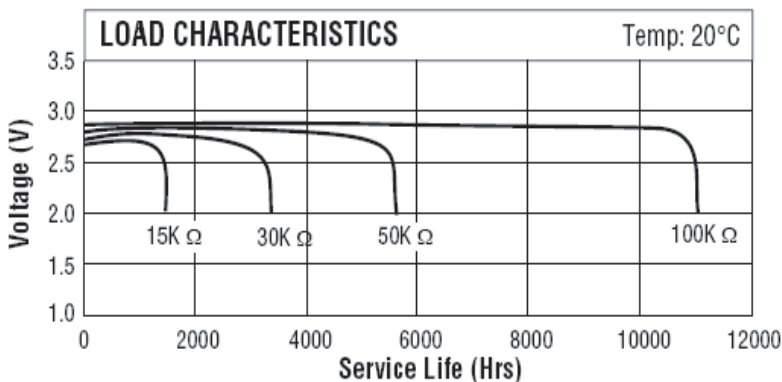
The MultiVolt core feature of MAX II is very useful in any cost- and power-sensitive portable system. The MultiVolt core regulator requires a nominal bias current which is typically 10 mA. The benefits of using the MultiVolt core regulator are much greater than the inconvenience of the regulator bias current. The benefits of a V_{CCINT} with a wide operating range include:

■ The ability to directly connect to a battery supply
■ The reduction of system power supply costs
■ The simple PCB design with fewer power rails
■ The single supply with no power-up sequence requirements
■ The simple power-up and power-down control

Table 1 shows the power characteristics of various Programmable Logic Devices (PLDs). The second column shows the minimum number of power rails needed in a battery-powered 3.3 V I/O portable system. In such a system, at least one or more I/O banks are at 3.3 V. The other power rails are required for non-3.3 V core supplies and various auxiliary supply requirements of the respective PLDs. There is a distinct advantage to having fewer power supplies. MAX II devices require the minimum number of supplies—one supply. Furthermore, MAX II devices have the same single supply capability for 2.5 V systems and can operate over a 2.3 V to 3.6 V range, the range required in a battery-powered portable system. Cyclone devices requiring two supplies are still the best-in-class for low-cost FPGAs, having fewer supplies is part of being a low-cost solution.

The third column of Table 1 shows the number of possible independent I/O bank voltages. Although 3.3 V is the most common system voltage, there are applications that use PLDs for voltage level shifting. MAX II devices have the most number of I/O banks compared to other existing CPLD devices. Even in cases in which only two V_{CCIO} levels are required, having four is an advantage as it offers more flexibility of pin assignments to different power rails. With two V_{CCIO} banks, half of all available user I/Os are assigned to each power rail. If a secondary bank requires only a few signals, many I/Os are wasted by the course granularity of the two V_{CCIO} banks. Four V_{CCIO} banks require that only one-fourth of the available I/Os be assigned to a secondary V_{CCIO} level, leaving three-quarters of the I/Os to operate at the primary V_{CCIO} level.

The fourth column of Table 1 any requirement for sequencing VCC power rails during power-up. No requirements are most desirable, as it puts no restrictions to power-up or power-down V_{CCIO}, V_{CCINT}, or V_{CCAUX} in any specific order. MAX II has no restrictions on the power-up order. If V_{CCIO} and V_{CCINT} use the same supply, power-up or power-down sequences do not apply. If column four reads "yes", you must follow a prescribed sequence results in unwanted current surges, I/O glitches, or possibly a

stuck state. Requiring a specific power-up sequence increases the complexity and total power cost of a system. It may also prevent using the PLD to control the power-up sequence of other devices on the board.

The fifth column of Table 1 shows whether the device has full hot-socket protection. The main hot-socket issue is the I/O pin leakage when power is not applied to the PLD. Hot socket leakage is the current leakage of an I/O pin at VCC or GND when the device V_{CCIO} or V_{CCINT} are not applied. Hot socket leakage causes system power dissipation through an I/O pin even if a device is powered down. MAX II devices offer hot-socketing support with very low static hot socket leakage. The hot-socket feature removes some challenges designers face when using components on PCBs that have a mix of 3.3 V, 2.5 V, and 1.5 V devices that are powered down in different modes. In a portable system, hot-socket support facilitates power-down of sections of the system without unwanted parasitic leakage paths through the CPLD I/O pins.

The MAX II device hot-socketing feature provides:

- Board or device insertion and removal without powering-down the system
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

Hot-socketing has several advantages. The most important advantage from a power consideration is the leakage current through an I/O when the V_{CCINT} or the V_{CCIO} is not powered up. MAX II devices offer all three of the features listed in the above bulleted list for hot-socketing capability without any external components or special design requirements. The following specifications are typical for hot-socketing:

- I/O pins can be driven before and during power-up or power-down without damage.
- I/O pins remain tri-stated during power-up; the device does not drive out before or during power-up, thereby affecting other buses in operation.
- Signal pins do not drive the V_{CCIO} or V_{CCINT} power supplies.
- Input pins do not have static leakage if driven high before V_{CCIO} or V_{CCINT} is applied, (hot socket leakage).

The last characteristic is critical in portable applications in which select sections of the system are powered down to save battery life. Some CPLDs have high leakage, hot socket leakage approximately 1 mA or higher, when their input pins are driven to a VCC level while V_{CCINT} or V_{CCIO} is off. If the device is powered down, but another part of the system is still active and driving an I/O pin high, the leakage on the I/O pin is much greater than the typical standby current. Unlike some competing

devices, a MAX II device does not power up through its I/Os, thus allowing it to be powered down without complex restrictions on the state of signals driving it from active parts of the system.

Table 1. Power Specification Comparisons

Family	Minimum Power Rails *(1)*	Maximum I/O Banks	Power-Up Sequence Requirement	Hot-Socket Leakage
MAX II	1	4	NO	NO
MAX IIG	2	4	NO	NO
MachXO	2 *(2)*	4	NO	YES
MACH4000Z	2	2	NO	YES
CoolRunner II	2	2	YES	YES
Cyclone	2	4	NO	NO
Cyclone II	2	8	NO	NO
Spartan III	3	8	YES	YES

Notes for Table 1:
(1)   Power rails required in a 3.3 V I/O battery-powered system.
(2)   MachXO VCC & V_{CCIO} work over wide range 1.71–3.465 V, but V_{CCAUX} has a limited range of 3.135–3.465 V.

Dynamic Power Advantage

MAX II has an architecture that is closer to an FPGA than a traditional CPLD device. The architecture has several advantages in terms of dynamic power and no disadvantages. It even has advantages over Complementary Metal-Oxide Semiconductor (CMOS) CPLD architectures. There are no DC power differences between the MAX II CMOS FPGA architecture and a CMOS CPLD architecture.

The first AC power advantage that a MAX II device has is in the implementation of logic. A MAX II device uses four input Look-Up Tables (LUTs) to implement logic. Equations requiring more than four inputs are accomplished by cascading the LUTs. The CMOS product term is implemented by a series of cascaded CMOS gates. Therefore, even a 2-input function may cascade through an entire 80-input CMOS and gate or p-term. The MAX II device architecture implements the logic required by your function only. A two-input function consumes less power than a six-input function with only two inputs active, unlike an 80-input CMOS p-term that uses the same high power for a two-input function as a 40-input function. Because statistical analysis shows that typical applications have an average fan-in of 2.5, the MAX II device architecture has a clear dynamic power advantage. Figure 2 illustrates how the

MAX II architecture has a 65% advantage over competitive CPLD architectures at 50 MHz. All devices have the same core circuit implemented with no outputs switching and only a clock input toggling.

Figure 2. MAX II Core Logic & Routing Architecture Dynamic Power Advantage (1)
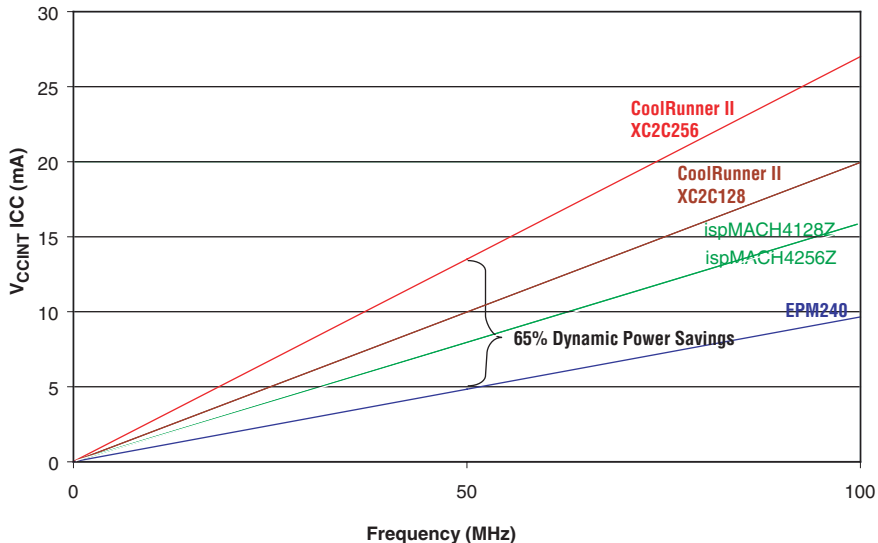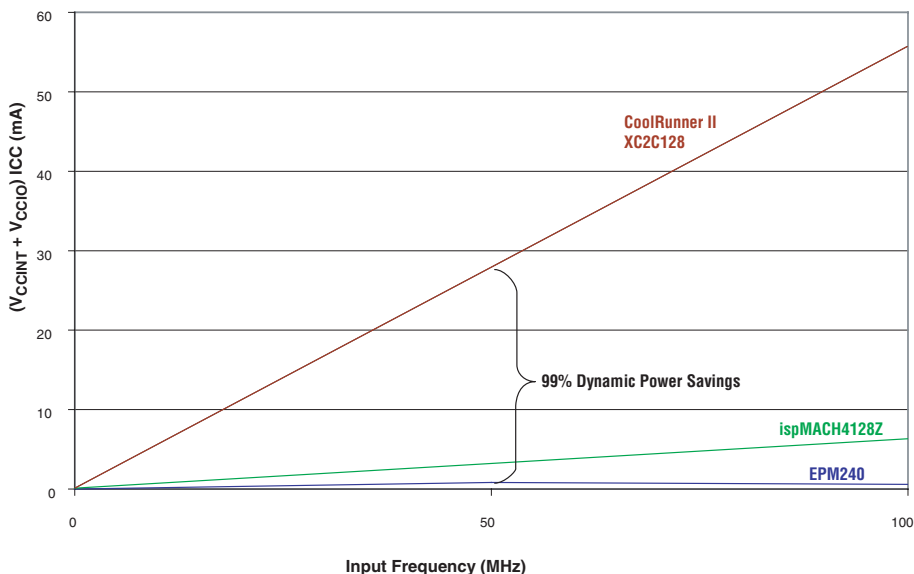

Note to Figure 2:
(1)   Dynamic power of eight 16-bit counters.

The routing of signals in the MAX II device architecture is quite different than typical CPLDs. Typical CPLDs have a central routing system that allows virtually every macrocell output or input pin to route to any macrocell input. This has several disadvantages in terms of power. Because every macrocell output or input pin goes everywhere, it has a very high capacitance. Even though most signals have a required fanout of two to four, they are still routed to literally hundreds of locations. This results in high capacitance and high dynamic power for all I/O pins and all macrocell outputs that feedback through the routing pool. The MAX II routing architecture is segmented. Each macrocell output connects to the routing network. The software assembles the minimum number of segments required to complete a desired net. By using the minimum route with no more span than required, the MAX II net capacitance is much lower than traditional CPLDs.

Figure 3 illustrates the dynamic power component of 16 inputs in a MAX II device and competing devices.

Figure 3. MAX II Routing Architecture Input Dynamic Power Advantage(1)

Note to Figure 3:
(1)   Dynamic power of 16 inputs switching.

The MAX II device offers 99% less dynamic power than traditional CPLD architectures with no special input gating circuits. MAX II offers dynamic power reduction on every input, regardless of the function, fanout, or placement.

CPLD architectures have only one way to place and connect macrocells. The MAX II architecture has many more possible variations. The Quartus® II software lets you select the best interconnect and placement method based on performance, power, or density. This is not possible with traditional CPLD routing architectures.

MAX II devices also have the advantage of a 1.8 V core. Even though the external V_{CCINT} is 3.3 V, the core operates at 1.8 V. Due to signal switching capacitance, the dynamic current is CV^2. Therefore, lowering VCC has a significant impact on the power consumed. This gives MAX II devices a

significant advantage over older process CPLDs that offer the advantage of a 3.3 V core voltage. Even with the same capacitance, MAX II offers 70% power reduction due to its lower core operating voltage.

True System Power

In most portable applications, the appliance is either running and satisfying a user need, or it is off, waiting to be turned on. Therefore, in most portable applications, being off takes care of the standby current reduction and so the key battery life improvement comes from decreasing the dynamic power consumed. PLDs with a low core voltage can mask the true power of the application.

The power consumed by the PLD is the $V_{CCINT*ICC}$, where ICC is the dynamic and static current of the PLD. The V_{CCINT} voltage is almost always derived from a Low Dropout (LDO) Regulator. The LDO takes the primary system voltage and generates the core voltage level. Therefore, the total power consumed by the PLD is $V_{CCINT*ICC}$ plus the power dissipated by the LDO. In a battery operated system, the power across the LDO is $(V_{BAT}-V_{CCINT})$*(ICC+ILDO), where ILDO is the DC bias current and AC regulation loss of the LDO regulator. The total power consumed by the portable system is calculated as:

$$V_{CCINIT} \times (ICC + ILDO) + (V_{BAT} - V_{CCINT}) \times (ICC + ILDO) = V_{BAT} \times (ICC + ILDO)$$

You must consider the total system power dissipation and not just the PLD power dissipation in isolation. Figure 4 illustrates the equivalent system power requirement for the MAX II device (EPM240) and the CoolRunner II device (XC2C128). The CoolRunner II device requires an additional LDO regulator. This figure shows the comparable system power curves using a 3.0 V lithium polymer battery and shows the total power usage of the battery. This figure also shows CoolRunner II's static power advantage, but it is quickly overcome at 5 MHz by the MAX II low dynamic power dissipation. MAX II devices offer 85% power savings at 50 MHz. The example designs have equal amounts of toggling core logic and toggling I/O pins. The sum of V_{CCINT} and V_{CCIO} power is shown. Note that the ispMACH4128Z V_{CCIO} power is not specified so the actual ispMACH4128Z power will be worse than shown. Output power required to drive board capacitance is not considered as it would be equal for all products.

Figure 4. Portable Appliance Example, Power Levels of Various CPLDs (1)
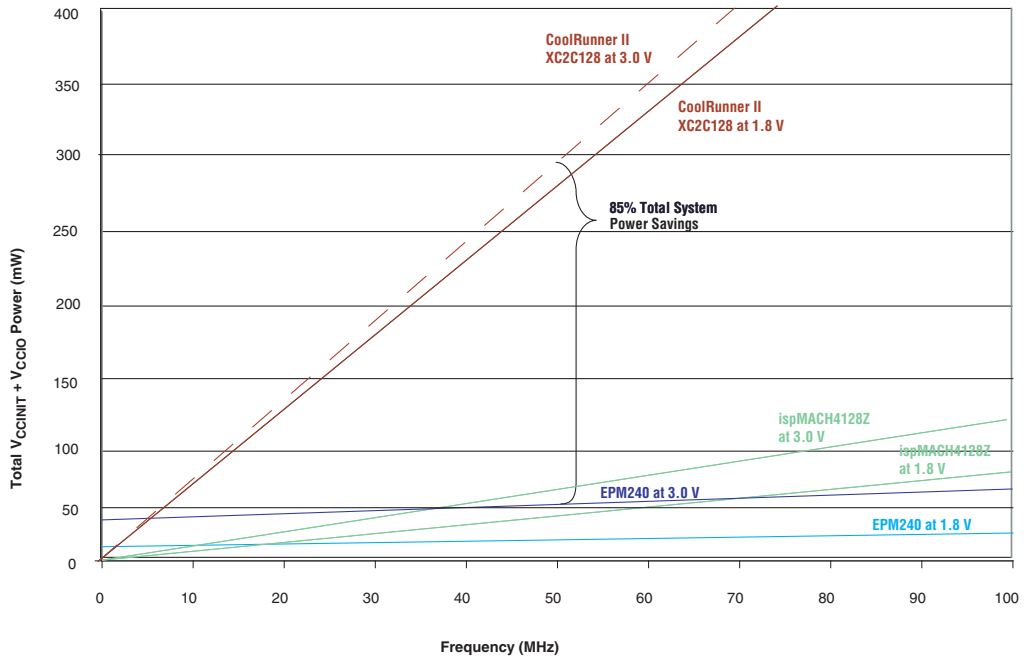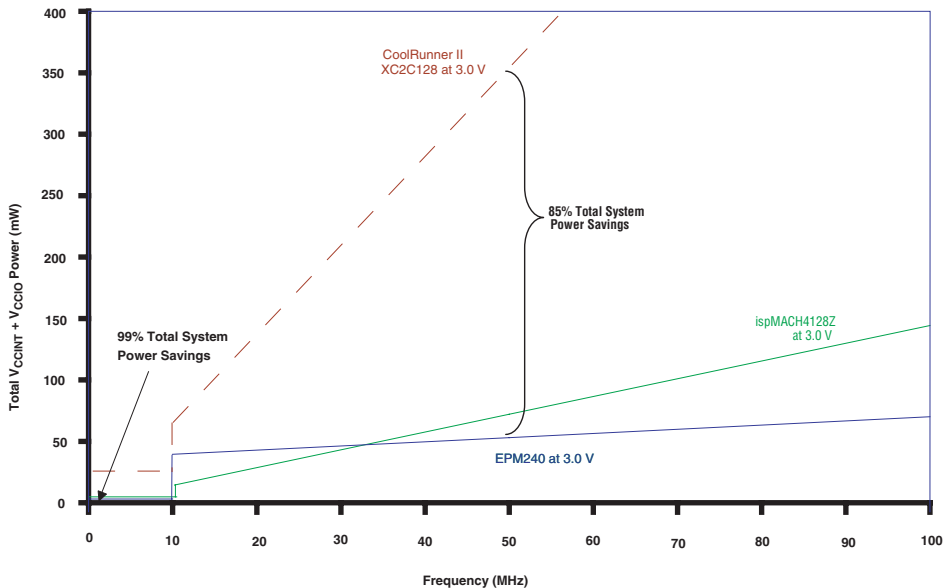

Note to Figure 4:
(1)   Portable application example with core logic and switching I/O.

Figure 5 shows the ability of the MAX II device to completely power-down due to its hot-socket, power-sequence flexibility and its single supply simplicity addressed earlier. In this example, the system is either running or stopped. The competitor device has eight I/O pins which are at VCC while the V_{CCIO} and V_{CCINT} are powered-down. This causes leakage current through the I/O, resulting in more power dissipation off than MAX II off. More than eight I/O pins at VCC results in a higher standby power on the CoolRunner II device. Multiple I/Os at VCC or GND has little effect on MAX II off power dissipation.

Figure 5. Portable Appliance Example, Power Levels with Power-Down Option for Various CPLDS (1)

Note to Figure 5:
(1)   Portable application example with V_{CCINT} and V_{CCIO} power down.

Using Power-Down Mode to Reduce MAX II Stand-by Power Dissipation

The circuit in Figure 6 shows how an Altera EPM570-T100 CPLD with an external P-Channel Metal Oxide Semiconductor Field-Effect Transistor (MOSFET), diode(s), and resistors are used to create a power-down system. The P-Channel MOSFET, or Field-Effect Transistor (FET), controls the power supply from the battery to the CPLD and any other selected components in the system. The cost of a MOSFET device can be less than $0.10 in high volume, and is always lower in cost than the low quiescent current LDO regulator required for 1.8 V core CPLD devices. The FET gate is controlled by the CPLD and the switches in the application. Pressing a switch enables the FET gate. The CPLD has a small embedded timer that monitors switching activity and system activity. Once a specified period of inactivity is detected, the FET is disabled, powering down the CPLD and other components on the same power node.

Figure 6. EPM570T100 Self Power-Down Circuit
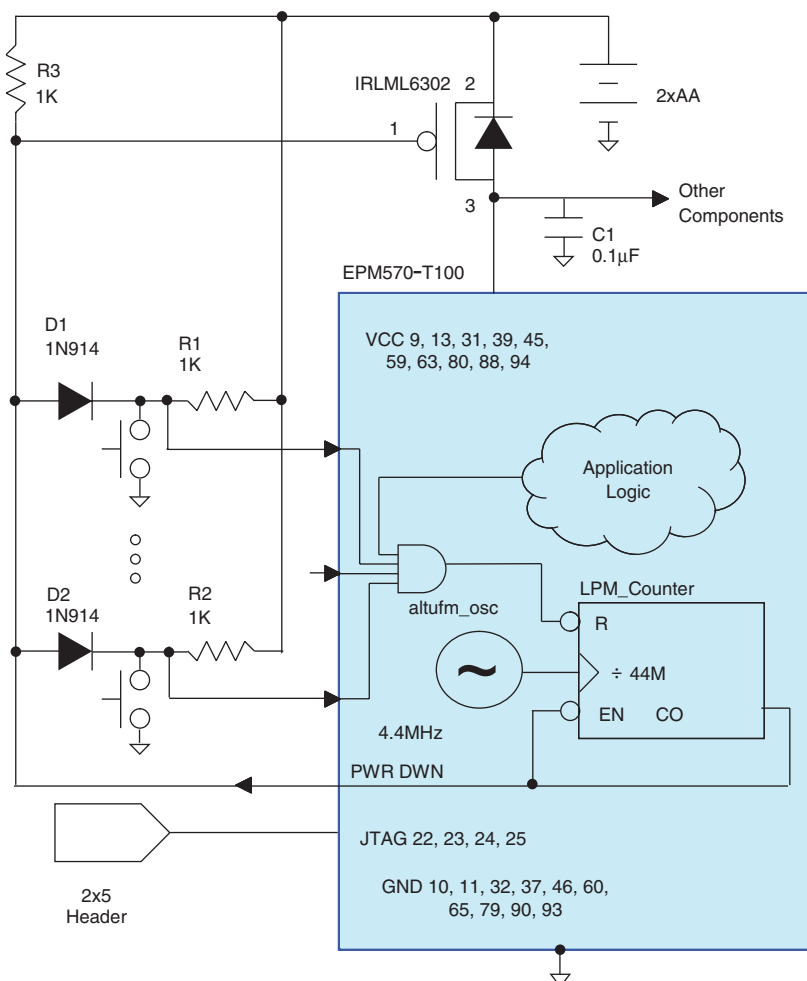
The FET is an IRLML6302 or equivalent. The source is connected to the + battery node and the drain to the VCC pins of the CPLD and any other components in the system to be powered down. The CPLD VCC pins are made up of V_{CCINT}, $V_{CCIO}1$ and $V_{CCIO}2$ type pins. The FET gate has a 1 K pull-up resistor, R3. When the power is off, the R3 pulls the gate to VCC, making the FET $V_{GS}=0$ V and shutting it off. When off, there is a leakage path to ground through the CPLD PWR_DWN pin. The EPM570-T100 has

hot-socket protection that limits the $I_{IOPIN} < 300$ µA dynamic and < 10 µA static. Therefore, even in the worst case, the FET is not turned on, because its minimum threshold is $V_{GS}=0.7$ V.

Pressing a switch turns on the FET, enabling a path through diode D1, a 1N914 diode, or 1N5818 Schottky diode equivalent, to the FET gate. Even with the 0.7 V drop across D1, the FET $V_{GS}=-2.3$ V easily turns it on. When the battery is discharged to 2.35 V, the lowest recommended operating voltage for the MAX II MultiVolt Core power system at $V_{GS}=-1.65$ V while the FET is still turned on. This powers up the CPLD within 100 µS.

Understanding the operation of the typical momentary switch is important to see how this circuit works. Even the best switch has a minimum on-time of about 3 ms. A typical user has a minimum press-and-release time of > 30 ms. Most switch specifications specify 3 ms as the minimum possible switch cycle time. With the relatively slow user response times, the CPLD device can power up the internal circuit, can reset and drive the `PWR_DWN` pin and the FET gate to a solid 0 V, long before the switch is released.

The circuit in the CPLD device is very simple. First, the internal 4.4 MHz ± 25% oscillator, `ALTUFM_OSC`, is used to drive an `LPM_counter` with a modulus of 44,000,000. The `LPM_counter` and `ALTUFM_OSC` are standard parameterized library macros generated by the Quartus II software. The counter is reset by any on switch or a low signal from the application logic. When the `LPM_counter` is reset, the Carry Out (CO) signal goes low and drives the `PWR_DWN` pin. The CO signal is inverted to enable the `LPM_counter` once the reset is removed.

After there are no switches depressed and there is no application logic activity, the `LPM_counter` counts to 44,000,000, or approximately 10 seconds before the CO signal goes high, thus disabling the counter and holding the CO pin high. This drives the `PWR_DWN` pin to VCC. Once the `PWR_DWN` pin reaches about 2.3 V, the FET turns off, powering down the CPLD which tri-states the `PWR_DWN` pin. Resistor R3 continues to pull the FET gate to VCC. The inactivity time-out can be set to any value by changing the counter modulus based on a 4.4MHz ± 25% internal oscillator. Power, ground, and JTAG pins are specified, but switch inputs and the `PWR_DWN` output can be any general purpose CPLD I/O pin.

The procedure for programming the EPM570-T100 using a download cable connected to JTAG pins through the manufacturer-defined 2x5 header requires depressing a switch before, during, and shortly after the configuration process to ensure the device is powered through the configuration process.

This complication is avoided by utilizing the pinout of the download cable connector shown in Figure 7. The download cable pins 2 and 10 are both GND. If only pin 10 is connected to the PCB GND, and pin 2 is connected to the PWR_DWN node, then when the download cable is connected the FET gate, it is shorted to GND, which keeps the device powered-up as long as the download cable is installed.

Figure 7. Implementation of Download Cable as Power-Up Enable for Configuration
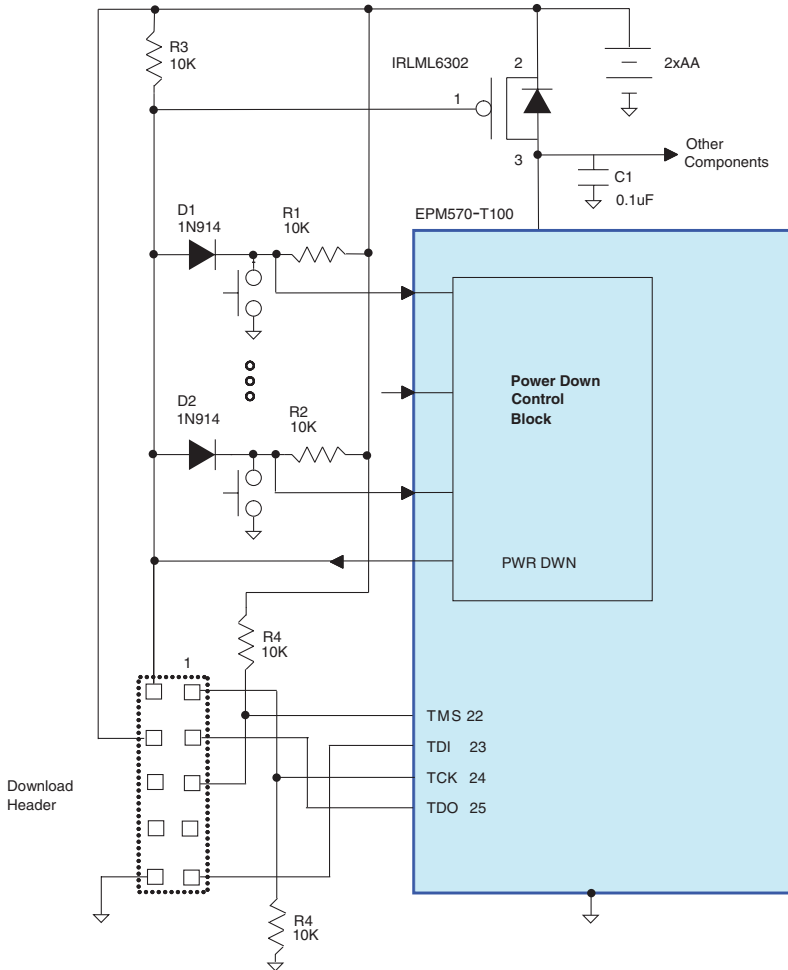
It is not necessary to have a diode for every switch in a system. Figure 8 shows how an NxM switch matrix can be efficiently used as a power-up detect with only N diodes.

In this example, only the rows are connected by diodes to the FET gate. Resistors R8 to R11 are added to give a path to ground for each column of switches. Pressing any switch pulls the FET gate low, turning on the CPLD. The CPLD power up is fast enough to allow scanning the switch matrix rows and columns to determine which switch was pressed long before the switch is released. The current draw through resistors R8 to R11 is very short during the scanning process, and the column signal is low in the waiting state to minimize supply current. Only Row 0-3 signals are used to reset the `LPM_counter` inactivity timer.

Figure 8. Efficient Wiring of Switch Matrix to Power-Down Circuit
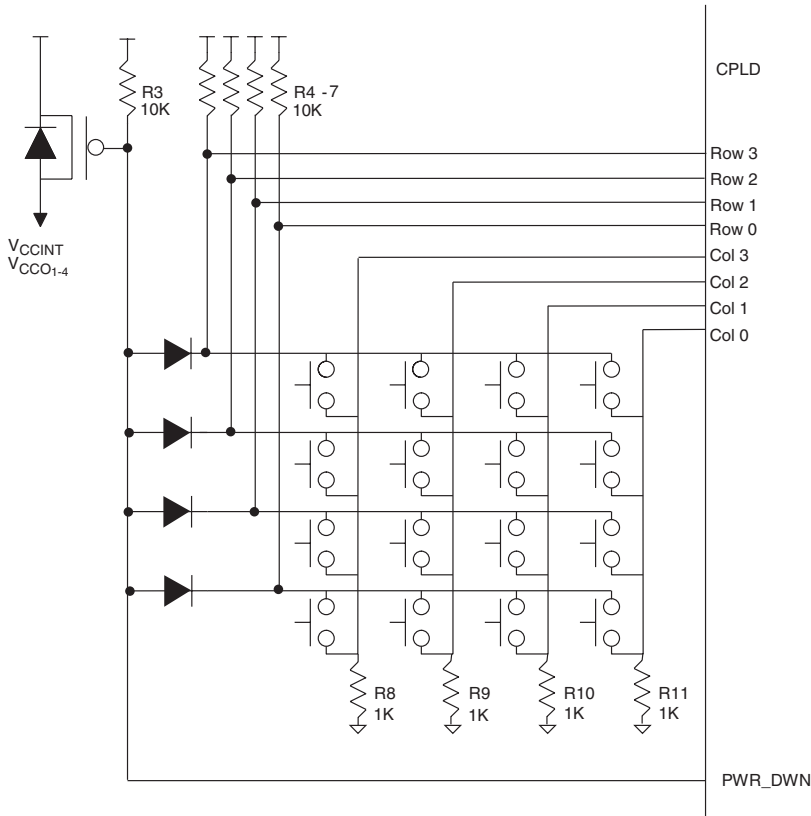
MAX II Advantages

The major advantages of using MAX II devices in portable battery powered applications are ease of use, lower cost, and lower power. MAX II devices are the easiest to use because of their integrated core voltage regulator, unrestricted power-up sequence, and excellent hot-socket characteristics. MAX II offers the lowest cost solution to portable system designers because it eliminates the need for using a core voltage regulator, a power-up oscillator, and external power sequence control circuits. Even when implementing a true power-down circuit, MAX II has the lowest cost, because MOSFET switches are much cheaper than zero-power digitally enabled LDO regulators. MAX II also offers more I/O per mm^2 of PCB area and more programmable logic gates per mm^2 of PCB than any other CPLD. Finally, MAX II offers the lowest dynamic power compared to any other CPLD or FPGA.

Conclusion

MAX II has a power advantage over other CPLDs and FPGAs. Too often, static power is used to judge the power advantage of one product over another. Although static power is important, there are many other aspects of power which are equally important. Many of the other power considerations addressed here have a much larger impact on portable appliance cost. Cost is nearly always more important than an abstract stand-by power specification. When standby power is required, the MAX II device can implement a true zero-power mode simply and cost effectively by turning itself off.

Additional Resources

For more information, see MAX II Power-Down Design at http://www.altera.com/support/examples/max/exm-power-down.html

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
literature@altera.com

I.S. EN ISO 9001