1. Stratix II GX Transceiver Block Overview

SIIGX52001-2.4

Introduction

Stratix® II GX devices combine highly advanced 6.375-Gigabits per second (Gbps) four-channel gigabit transceiver blocks with the industry's most advanced FPGA architecture. The Stratix II GX transceiver builds on the success of the Stratix GX family by offering higher data rate support and additional features that enable you to support a wide variety of standard and custom protocols. Each self-contained Stratix II GX gigabit transceiver block has a variety of embedded functions to implement commonly required tasks.

Building Blocks

Stratix II GX transceivers are structured into duplex four-channel groups called transceiver blocks. You can configure each channel within a transceiver block in either single-width or double-width mode. Single-width mode has an 8-bit/10-bit serializer/deserializer (SERDES) data path through the transceiver and supports data rates from 600 Mbps to 3.125 Gbps. Double-width mode has a 16-bit/20-bit SERDES data path through the transceiver and supports data rates from 1 Gbps to 6.375 Gbps. All blocks in the transceiver can operate in double-width mode, except deskew first-in first-out (FIFO), which is available only in single-width mode. The options for blocks available in the transceiver may differ depending on which mode (single or double) you use.

This documentation uses the terminology inter-transceiver block routing instead of inter-quad (IQ) routing, as seen in the Quartus II software.

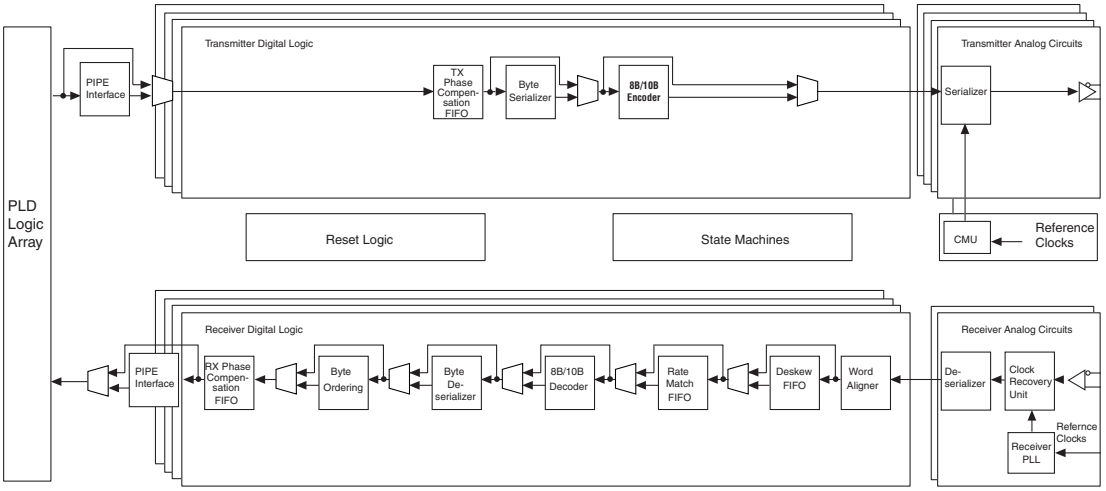
In addition to custom (Basic) modes, Stratix II GX transceivers support the following protocols:

- Physical Interface for PCI Express (PIPE) – single lane (×1), four lane (×4), and eight lane (×8)
- XAUI (10 Gigabit Attachment Unit Interface)
- GIGE (Gigabit Ethernet)
- SONET/SDH (Synchronous Optical NETwork) – OC-12, OC-48, and OC-96
- (OIF) CEI PHY Interface (Common Electrical I/O)
- Serial RapidIO (1.25 Gbps, 2.5 Gbps, and 3.125 Gbps)
- CPRI (Common Public Radio Interface)
- SDI (Serial Digital Interface) (HD-SDI and 3G-SDI)

Figure 1–1 shows a block diagram of the gigabit transceiver block in single-width mode. You enable or disable various optional modules based on the functional mode you select. The sections that follow Figure 1–1 give a brief description of each block.

For detailed information about each block, refer to the *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Device Handbook*.

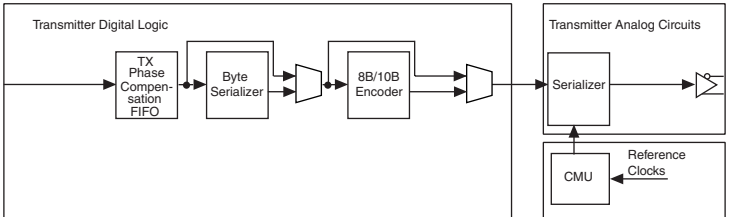
Figure 1–1. Stratix II GX Gigabit Transceiver Block Diagram



Transmitter Channel Overview

This section provides a brief description about the various components within the transmitter block (Figure 1–2). The modules are listed in order from the parallel logic array to the transmit buffer of the transmitter.

Figure 1–2. Stratix II GX Transmitter Block Diagram



Clock Multiplier Unit

Each gigabit transceiver block has a clock multiplier unit (CMU) to provide clocking flexibility and support a range of incoming data streams. Each CMU contains two transmitter phase-locked loops (PLLs) that generate the required clock frequencies based upon the synthesis of an input reference clock. Each transmitter PLL supports multiplication factors to allow the use of various input clock frequencies. Both transmitter PLLs are identical and support data ranges from 600 Mbps to 6.375 Gbps. However, each PLL can be configured to support different data rates. Each transmitter PLL drives up to four channels. In PIPE x8 mode, the transmitter PLL of the master transceiver block drives all eight channels. This CMU block is active in both single- and double-width modes and is powered down when not in use.

Phase Compensation FIFO Buffer

The transmitter data path has a dedicated phase compensation FIFO buffer that decouples phase variations between the FPGA and transceiver clock domains. This block is active in both single- and double-width modes and cannot be bypassed.

Byte Serializer

The byte serializer allows the programmable logic device (PLD) to run at half the rate of the transmit data path to allow the core to run at a lower frequency. Without the byte serializer, at the maximum data rate of 6.375 Gbps with a 20-bit serialization factor, the PLD-transceiver interface needs to run at 318.75 MHz. The PLD-transceiver interface can run at a maximum frequency of 250 MHz. With the byte serializer, the PLD-transceiver interface needs to run at 159.375 MHz. This block is available in both single- and double-width modes. In single-width mode, the PLD interface is either 16 or 20 bits when the byte serializer used. In double-width mode, using the byte serializer creates a PLD interface of 32 bits or 40 bits, depending on the serialization factor.

8B/10B Encoder

Many protocols use 8B/10B encoding. Stratix II GX devices have two dedicated 8B/10B encoders in each transmitter channel. This encoding technique ensures sufficient data transitions and a DC-balanced stream within the data signal for successful data recovery at the receiver. This block is available in single- and double-width modes. In single-width mode, one of the 8B/10B encoders is active. In double-width mode, both 8B/10B encoders are active and operate in a cascade mode. The 8B/10B encoder follows the IEEE 802.3 1998 edition standard for 8B/10B encoding.

Serializer

The serializer converts the incoming lower speed parallel signal from the transceiver's physical coding sublayer (PCS) to a high-speed serial signal on the transmit side. The serializer supports a variety of conversion factors, ensuring implementation flexibility. The serializer supports an 8- or 10-bit serialization factor in single-width mode and a 16- or 20-bit serialization factor in double-width mode. The serializer block also performs clock synthesis on the slow-speed clock for the parallel transmitter logic in the transceiver and PLD.

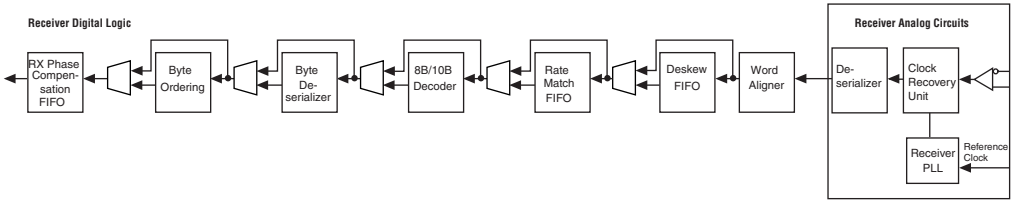
Transmitter Differential Output Buffers

The gigabit transceiver block differential output buffers support the 1.5-V PCML and 1.2-V PCML I/O standards and have a variety of features that improve system signal integrity. Programmable pre-emphasis helps compensate for high frequency losses. A variety of programmable voltage output differential (V_{OD}) settings allow noise margin tuning capabilities. Additionally, on-chip termination (OCT) provides the appropriate transmitter buffer termination for 100-, 120-, or 150-Ω transmission lines. The transmitter buffer circuit also contains a receiver-detect circuit for use with the PCI Express (PIPE) protocol to detect if a receiver is connected. The buffer can be tri-stated to reduce electromagnetic interference (EMI) and power consumption when not in use. In PIPE mode, the tri-state feature generates Electrical Idle.

Receiver Channel Overview

This section provides a brief description about the various components within the receiver block. The modules originate from the serial receiver buffer to the parallel FPGA interface (Figure 1–3).

Figure 1–3. Stratix II GX Receiver Block Diagram



Receiver Differential Input Buffers

Stratix II GX transceiver block differential input buffers support 1.5-V PCML and 1.2-V PCML I/O standards and have a variety of features that improve system signal integrity. Programmable equalization capabilities compensate for signal degradation across transmission mediums. Additionally, on-chip termination provides the appropriate receiver termination for 100-, 120-, or 150-Ω transmission lines. A signal detection block indicates if there is a valid signal at the receiver input.

Stratix II GX receiver input buffers also support the adaptive equalization (AEQ) capability to compensate for changing link characteristics.

Receiver PLL

The receiver PLL ramps the voltage controlled oscillator (VCO) to the frequency of the reference clock. Once that occurs, the clock recovery unit (CRU) controls the VCO. Each receiver channel in the transceiver has a dedicated receiver PLL that provides clocking flexibility and supports a range of data rates. These PLLs generate the required clock frequencies based upon the synthesis of an input reference clock.

Clock Recovery Unit

The Stratix II GX transceiver block CRU performs analog clock data recovery (CDR). The CRU recovers the embedded clock in the data stream to properly clock the incoming data. The recovered clock also clocks the reset of the receiver logic clock (`rx_digitalreset`) and is available in the PLD fabric.

Deserializer

The deserializer block converts the incoming data stream from a high-speed serial signal to a lower-speed parallel signal that can be processed in the FPGA logic array on the receive side. The deserializer supports a variety of conversion factors, ensuring implementation flexibility. The deserializer supports an 8- or 10-bit deserialization factor in the single-width mode and a 16- or 20-bit deserialization factor in double-width mode. The deserializer block also performs clock synthesis on the slow-speed clock from the CRU and forwards the recovered clock to the parallel receiver logic in the transceiver and for the PLD.

Word Aligner

The word aligner module contains a fully programmable pattern detector to identify specific patterns within the incoming data stream. The pattern detector includes recognition support for control code groups for 8B/10B encoded data and A1A2 or A1A1A2A2-type frame alignment patterns for scrambled data. Custom alignment patterns are also available. The word aligner can be bypassed in some functional modes.

In single-width mode, the following word-alignment options are available:

- Manual bit-slip mode
- Manual alignment to 7-, 10-, or 16-bit patterns
- Synchronization state machine that offers programmable hysteresis for synchronization.

In double-width mode, the following word-alignment options are available:

- Manual bit-slip mode
- Manual alignment to 7-, 8-, 10-, 16-, 20-, or 32-bit patterns

Channel Aligner (Deskew)

An embedded channel aligner aligns byte boundaries across multiple channels and synchronizes the data entering the logic array from the Gigabit transceiver block's four channels. The Stratix II GX channel aligner is optimized for a 10-Gigabit Ethernet XAUI four-channel implementation. The channel aligner includes the control circuitry and channel alignment character detection defined by the 10-Gigbit Attachment Unit Interface (XAUI) protocol.

This block is only available for the XAUI protocol and is disabled for all other protocols.

Rate Matcher

In CDR-based systems, the clock frequencies of the transmitting and receiving devices often do not match. This mismatch can cause the data to transmit at a rate slightly faster or slower than the receiving device can interpret. The Stratix II GX rate matcher resolves the frequency differences between the recovered clock and the FPGA logic array clock by inserting or deleting removable characters from the data stream, as defined by the transmission protocol, without compromising transmitted

data. The rate matcher block is available for single- and double-width Basic modes and for specific protocols—XAUI, Gigabit Ethernet (GIGE), and PCI Express (PIPE).

8B/10B Decoder

Various protocols use 8B/10B decoding. Stratix II GX devices have two dedicated 8B/10B decoders in each channel to support high data rates. This decoding technique ensures fast disparity and code group error detection. This block is available in single- and double-width modes. In single-width mode, only one of the 8B/10B decoders is active. In double-width mode, both 8B/10B decoders are active and operate in a cascade mode. The current running disparity can be sent to the PLD for each decoded code group. The 8B/10B decoder follows the IEEE 802.3 1998 edition standard for 8B/10B decoding.

Byte Deserializer

The byte deserializer widens the transceiver data path before the PLD interface to reduce the rate at which the received data must be clocked in the PLD logic. This byte deserializer block is available in both single- and double-width modes. In single-width mode, the PLD interface is either 16 or 20 bits when used. In double-width mode, using the byte deserializer creates a PLD interface of 32 or 40 bits, depending on your serialization factor.

Byte Ordering

Each receiver has an optional byte ordering block that is available in some functional modes when the byte deserializer is used. This block restores the expected word ordering if the byte deserialization of the data word does not match the expected word ordering after the byte deserializer block. This block is not available when the rate matcher is used (single- or double-width mode) because the rate matcher may alter the byte order by adding or deleting bytes. It is also not available when 8B/10B is used in single-width mode.

Receiver Phase Compensation FIFO Buffer

Each receiver data path has a dedicated phase compensation FIFO buffer that decouples phase variations between the FPGA and transceiver clock domains. This block is always used and cannot be bypassed.

PIPE Interface

The PIPE interface supports the PCI Express protocol. The PIPE interface simplifies and standardizes the back-end interface to the PCI Express physical layer. This block is automatically enabled in PIPE mode and is not available in any other mode.

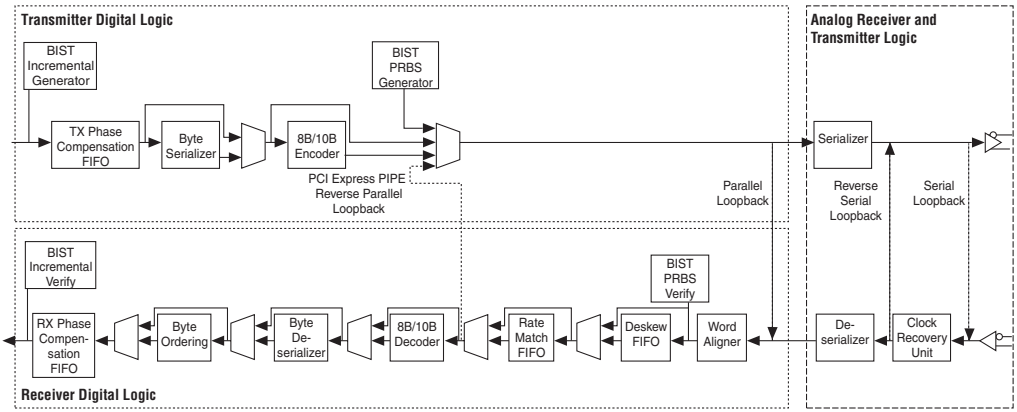
Loopback

There are four available loopback modes for diagnostic purposes. The following loopback modes are available:

- Serial loopback
- Reverse serial loopback
- Pre-CDR loopback
- Built-in self test (BIST) incremental test parallel loopback
- PCI Express (PIPE) reverse parallel loopback

Figure 1–4 shows the available loopback modes.

Figure 1–4. Loopback Modes



Built-In Self-Test

The gigabit transceiver block contains several features that simplify design verification. Embedded pattern generators and pattern verifiers provide a simple approach to board verification without the need to design additional logic in the PLD fabric. The BIST pseudo-random binary sequence (PRBS) and incremental pattern generators, along with their respective pattern verifiers, provide a full self-test path.

Reset and Power Down

Stratix II GX transceivers offer multiple reset signals to control separate ports of the transceiver channels and blocks. Each unused channel is automatically powered down to reduce power consumption. Additionally, there are dynamic power-down signals for each receiver and transmitter block.

Referenced Document

This chapter references the following document:

- *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Device Handbook.*

Document Revision History

Table 1–1 shows the revision history for this chapter.

Table 1–1. Document Revision History (Part 1 of 2)

Date and Document Version	Changes Made	Summary of Changes
October 2007, v2.4	Added note to "Receiver Differential Input Buffers" section.	—
	Updated bulleted list in"Building Blocks" and "Loopback" sections.	—
	Updated: • "Clock Multiplier Unit" • "Byte Serializer"	—
	Added "Referenced Document" section.	—
	Minor text edits.	—
August 2007 v2.3	Minor text edits.	—
February 2007 v2.2	Changed 622 Mbps to 600 Mbps in: • "Building Blocks" • "Clock Multiplier Unit"	—
	Changed 3.125 Gbps to 1 Gbps in "Building Blocks".	—
	Modified the following: • "Clock Multiplier Unit" • "Byte Serializer" • "8B/10B Encoder" • "Loopback"	—
	Updated Figure 1–3.	—

Table 1–1. Document Revision History (Part 2 of 2)

Date and Document Version	Changes Made	Summary of Changes
April 2006, v2.1	• Minor change to Figures 1–1 and 1–3.	—
February 2006, v2.0	• Updated “Building Blocks” section. • Updated “Word Aligner” section. • Updated “Byte Ordering” section. • Updated “Loopback” section. • Updated “Built-In Self-Test” section.	—
October 2005 v1.0	Added chapter to the *Stratix II GX Device Handbook*.	—