Serial Digital Interface Reference Design for Cyclone IV Devices

AN-641-1.2 Application Note

The Serial Digital Interface (SDI) reference design shows how you can transmit and receive video data using the Altera® SDI MegaCore® function and the Cyclone® IV GX video development board. This reference design uses three instances of the SDI MegaCore function. The triple-standard SDI MegaCore function comprises standard definition (SD-SDI), high definition (HD-SDI), and 3 gigabits per second (3G-SDI) video signal standards.

This application note describes how to use the serial digital interface with the Cyclone IV GX video development board for different variants. The Cyclone IV GX video development board consists of the Cyclone IV GX FPGA board that is available in the Cyclone IV GX FPGA development kit and an SDI high-speed mezzanine card (HSMC) that is purchased separately.

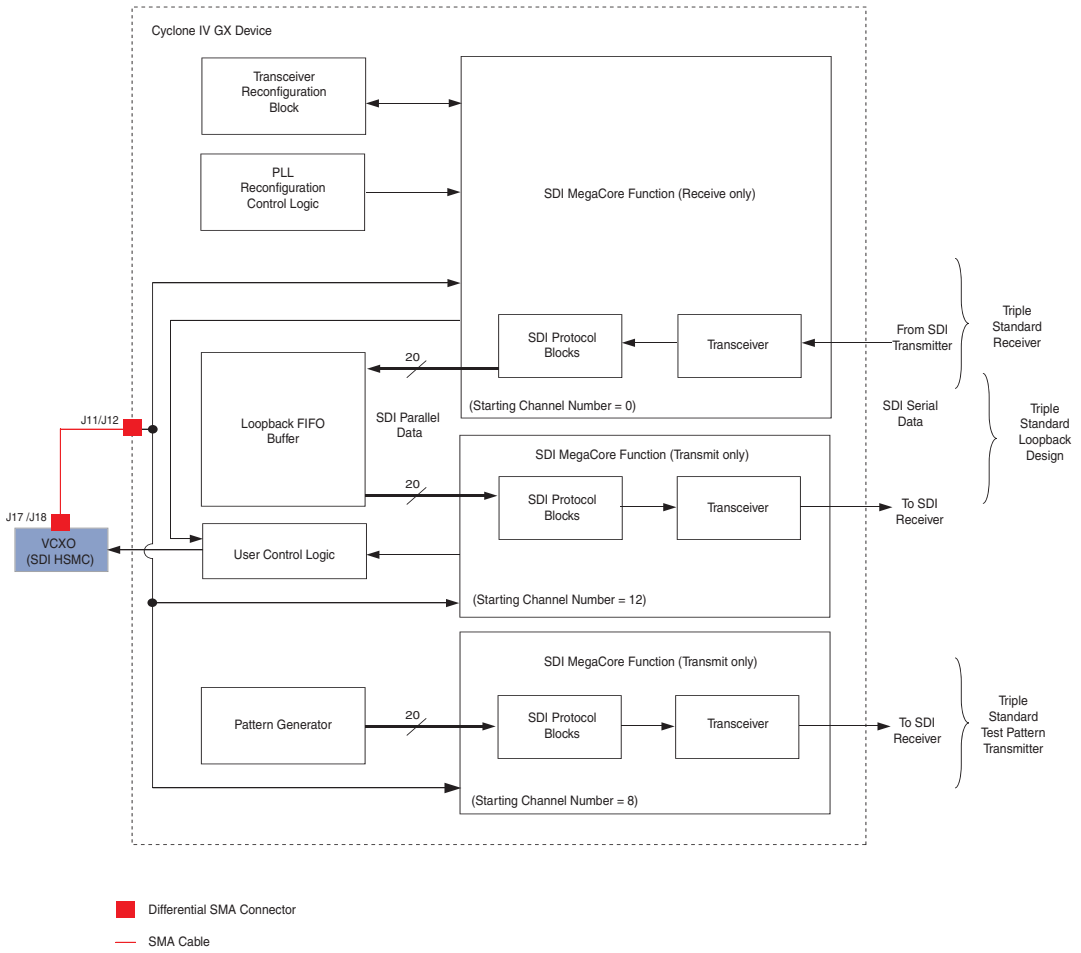
For more information about the Cyclone IV GX FPGA development kit, refer to the *Cyclone IV GX FPGA Development Kit User Guide*. For more information about the Cyclone IV GX FPGA development board, refer to the *Cyclone IV GX FPGA Development Board Reference Manual*; for more information about the SDI HSMC, refer to the *SDI HSMC Reference Manual*. For more information about the SDI MegaCore function, refer to the *Serial Digital Interface MegaCore Function User Guide* or contact your Altera representative.

101 Innovation Drive
San Jose, CA 95134
www.altera.com

Functional Description

The reference design provides a general platform to control, test, and monitor different speeds of the SDI operations. Figure 1 shows a high-level block diagram of the SDI reference design.

Figure 1. Block Diagram



The following sections describe the various elements of the block diagram.

Triple-Standard Receiver

The triple-standard SDI receiver MegaCore function provides SD-SDI, HD-SDI, and 3G-SDI receiver interfaces.

Triple-Standard Transmitter

The triple-standard SDI transmitter MegaCore function outputs a 2.970-Gbps 1080p, 1.485-Gbps 1080i, or 270-Mbps data stream. The transmitter takes its input from the pattern generator.

Triple-Standard Loopback

The triple-standard SDI MegaCore function provides SD-SDI, HD-SDI, and 3G-SDI interfaces, and demonstrates receiver-to-transmitter loopback. The received data is decoded, buffered, recoded, and then transmitted. The interface is configured for 2.970-Gbps, 1.485-Gbps or 270-Mbps rates.

Loopback FIFO Buffer

The decoded receiver data connects to the transmitter input through a FIFO buffer. When the receiver is locked, the receiver data is written to the FIFO buffer. When the FIFO buffer is half full, the transmitter starts reading, encoding, and transmitting the data.

Pattern Generator

The pattern generator IP core outputs a 2.970-Gbps 1080p, 1.485-Gbps 1080i or 270-Mbps test pattern. The test pattern can be a 100% color bar, a 75% amplitude color bar, or an SDI pathological checkfield frame.

Transceiver Reconfiguration Block

The transceiver reconfiguration block is an ALTGXB_RECONFIG instance that is required to cancel offsets and improve signal quality.

PLL Reconfiguration Control Logic

The reconfiguration control logic handles the reconfiguration of the receiver part of the duplex core and the separate receiver in the design.

The reconfiguration control logic comprises the following sub blocks:

- pll_reconfig_control

  This top-level design contains three blocks of dynamic partial reconfigurable I/O (DPRIO) in PLL reconfiguration mode.

- altpll_reconfig

  This block is an ALTPLL_RECONFIG instance that is required for the DPRIO. This megafunction reprograms the ALTGX transceivers in Cyclone devices only.

- ROMs

  The ROMs hold the ALTGX setting information for each of the video signal standards. Because the setup for SD-SDI is similar to 3G-SDI, only two settings are required: one ROM for SD-SDI and 3G-SDI, and one ROM for HD-SDI.

- PLL_reconfig_fsm

  The PLL reconfiguration finite state machine (FSM) block contains a state machine to control the ALTPLL_RECONFIG megafunction.

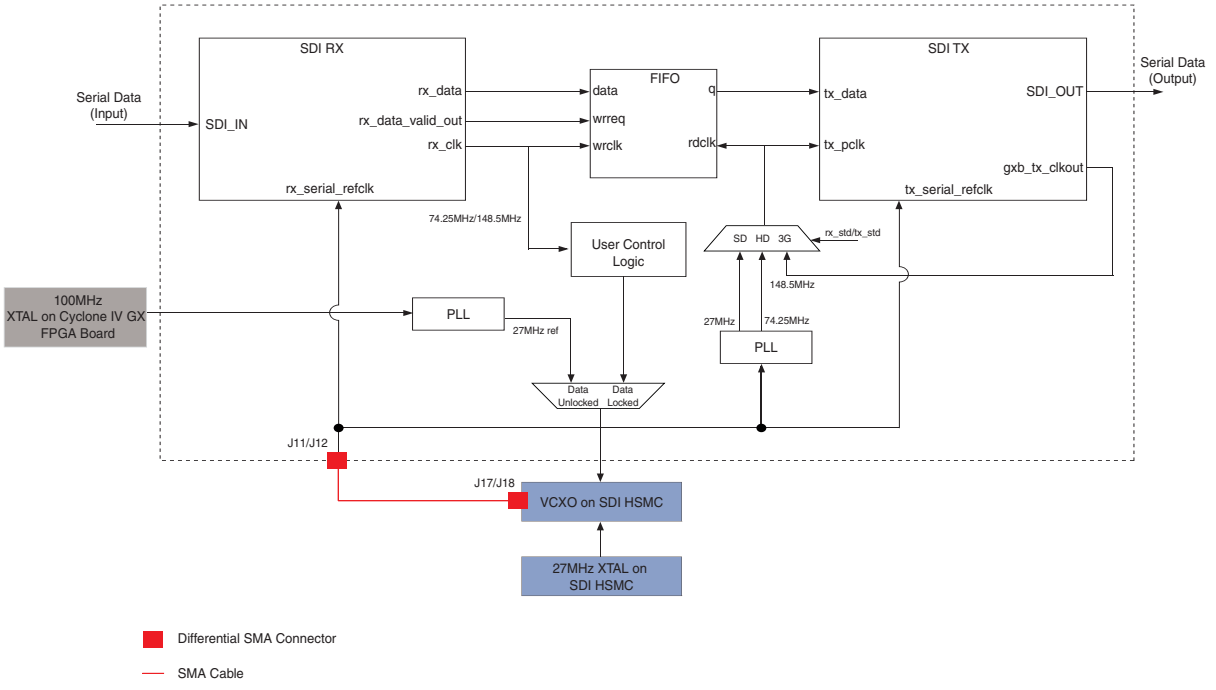
For more information about the ALTPLL_RECONFIG megafunction, refer to the *Phase-Locked Loop Reconfiguration (ALTPLL_RECONFIG) Megafunction User Guide*. For more information about DPRIO, refer to the DPRIO section in the *SDI MegaCore Function User Guide*, *Cyclone IV GX Device Handbook,* and *AN609: Implementing Dynamic Reconfiguration in Cyclone IV GX Devices*.

Voltage Controlled Crystal Oscillator

The VCXO device is a phase-locked loop (PLL) based synchronous clock generator (ICS810001) that is located on the SDI HSMC. This device contains two internal frequency multiplication stages cascaded in series. The first stage is a VCXO PLL that is optimized to provide reference clock jitter attenuation and to support the complex PLL multiplication ratios needed for video rate conversion. The second stage is a FemtoClock™ frequency multiplier that provides the low jitter, high frequency video output clock. The 148.5-MHz VCXO output clock connects to the `rx_serial_ref_clk` and `tx_serial_ref_clk` clocks of all the three SDI instances through the external SubMiniature version A (SMA) cables.

Figure 2 shows the block diagram of the parallel data loopback design.

Figure 2. Receiving the Parallel Data Loopback Design



Clock Input Differential SMA Connectors

Because of the the hardware limitation in the Cyclone IV GX video development board, the 148.5-MHz clock source from the HSMC feeds to `rx_serial_ref_clk` and `tx_serial_ref_clk` through external SMA cables. The SMA cables connect the SDI clock output (J17 and J18) from the HSMC to the clock input differential (J11 and J12). An external clock source from the clock input differential SMA connectors (J11 and J12) is applied to the receiver instance in this design.

☞ Altera recommends that you use the dedicated clock pin to feed the reference clock.

User Control Logic

The user control logic receives the clock data recovery (CDR) receiver clock, `rx_clk`, from the SDI receiver only and the SDI duplex instances, and then sends the receiver clock with the control bits to the VCXO device.

Getting Started

This section discusses the requirements and related procedures to demonstrate the SDI reference design with the Cyclone IV GX video development board. This section contains the following topics:

- Hardware and Software Requirements
- Hardware Setup
- Running the Reference Design

Hardware and Software Requirements

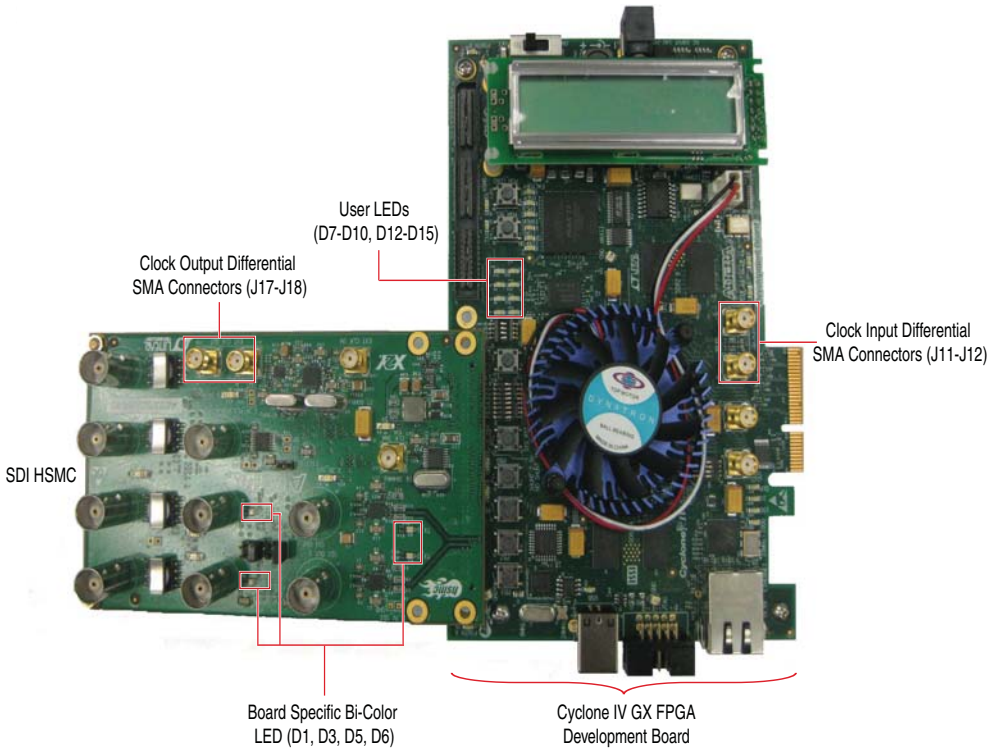
The demonstration requires the following hardware and software:

- Cyclone IV GX video development board—Cyclone IV GX FPGA development board and SDI HSMC
- SDI MegaCore function
- Quartus® II software, version 10.1 SP1
- Two SMA cables

Hardware Setup

Figure 3 shows how the Cyclone IV GX FPGA development board is connected to the SDI HSMC.

Figure 3. Hardware Setup



For more information about the Cyclone IV GX FPGA development board, refer to the *Cyclone IV GX FPGA Development Board Reference Manual*; for more information about the SDI HSMC, refer to the *SDI HSMC Reference Manual*.

Table 1 lists the function of each LED on the Cyclone IV GX FPGA development board.

Table 1. LEDs on Cyclone IV GX FPGA Development Board

LED	Description
D15	SDI IN 1 alignment lock
D14	SDI IN 1 TRS lock
D13	Not used. Reserved GND pin for dedicated clock. For more information about the reserved GND pin, refer to *Cyclone IV Device Family Pin Connection Guidelines*.
D12	SDI IN 1 frame lock
D10	SDI IN 1 received video signal standards
D9	[D9, D10] 00=SD-SDI, 01=HD-SDI, 11=3G-SDI

Table 1. LEDs on Cyclone IV GX FPGA Development Board

LED	Description
D8	Internal pattern generator video signal standards
D7	[D7, D8]: 00 = SD-SDI, 01 = HD-SDI, 11 = 3G-SDI

Table 2 lists the function of each user-defined dual in-line package (DIP) switch control (SW2). When the switch is in the OFF position, a logic 1 is selected. When the switch is in the ON position, a logic 0 is selected.

Table 2. SW2 DIP Switch Controls

USER_DIP	Description
7	Not used
6	
5	
4	
3	1= Select pathological SDI checkfield pattern
2	0= 100% color bar 1= 75% color bar
1	Change the internal pattern generator video signal standards
0	USER_DIP[1:0]: 00 = SD-SDI, 01 = HD-SDI, 11 = 3G-SDI

Table 3 lists the function of each board specific bi-color LED on the SDI HSMC.

Table 3. Board Specific Bi-Color LEDs on SDI HSMC

LED	Description
D1	SDI IN 2 receiving SDI signal in the following standards: ■ Green = 3G-SDI ■ Orange = HD-SDI ■ Red = SD-SDI
D3	SDI OUT 2 transmitting SDI signal in the following standards: ■ Green = 3G-SDI ■ Orange = HD-SDI ■ Red = SD-SDI
D5	SDI OUT 1 transmitting SDI signal in the following standards: ■ Green = 3G-SDI ■ Orange = HD-SDI ■ Red = SD-SDI
D6	SDI IN 1 receiving SDI signal in the following standards: ■ Green = 3G-SDI ■ Orange = HD-SDI ■ Red = SD-SDI

Table 4 lists the function of the reset button.

Table 4. Reset Button

Push Button	Description
S6	Resets the CPU or FPGA logic

Running the Reference Design

To run the reference design, follow these steps:

1. Set up the board connections. With the power to the board off, follow these steps:
   a. Connect the SDI HSMC to the FPGA development board. Refer to Figure 3 on page 6.
   b. Specify the following board settings located on the back of the FPGA development board:
      - DIP switch bank (SW1)
      - PCI Express DIP switch bank (SW4)
      - JTAG Control DIP switch (SW5)

      Match the board settings to the switch control settings in Table 5.
   c. Connect the FPGA development board (J4) to the power supply.

Table 5. SW DIP Switch Control Settings

Switch	Schematic Signal Name	Description	Default
SW1			
1	USER_FACTORY	ON: Loads the user file from the flash at power-up OFF: Loads the factory file from the flash at power-up	OFF
2	CLK125_EN	ON: Disables the 125 MHz oscillator OFF: Enables the 125 MHz oscillator	OFF
3	CLKA_EN	ON: Disables the 100 MHz programmable oscillator OFF: Enables the 100 MHz programmable oscillator	OFF
4	CLKA_SEL	ON: Drives the OSC source to the FPGA OFF: Drives the SMA input source to the FPGA	OFF
SW4			
1	PCIE_PRSNT2n_x1	ON: Enables x1 presence detect OFF: Disables x1 presence detect	ON
2	PCIE_PRSNT2n_x4	ON: Enables x4 presence detect OFF: Disables x4 presence detect	ON
3	—	—	—
4	USB_DISABLEn	ON: Disables embedded blaster OFF: Enables embedded blaster	ON

Table 5. SW DIP Switch Control Settings

Switch	Schematic Signal Name	Description	Default
SW5			
1	EPM2210_JTAG_EN	ON: Includes the MAX II CPLD EPM2210 System Controller in the JTAG chain OFF: Bypasses the MAX II CPLD EPM2210 System Controller	OFF
2	HSMA_JTAG_EN	ON: Includes the HSMA in the JTAG chain OFF: Bypasses the HSMA	OFF
3	HSMB_JTAG_EN	ON: Includes the HSMB in the JTAG chain OFF: Bypasses the HSMB	OFF
4	PCIE_JTAG_EN	ON: Includes the PCI Express in the JTAG chain OFF: Bypasses the PCI Express	OFF

2. Launch the Quartus II software and compile the reference design, as follows:
   d. On the File menu click **Open Project**, navigate to \<*directory*>**\c4gxsdi.qpf**, and click **Open**.
   e. On the Processing menu, click **Start Compilation**.
3. Download the **c4gxsdi.sof** file, as follows:
   f. Connect the USB-Blaster™ download cable to the board's USB Type-B Connector (J4).
   g. On the Tools menu, click **Programmer.** The **c4gxsdi.sof** file is automatically detected by the software during compilation and appears in the pop-up window**.**
   h. Click **Start** to download the Quartus II-generated file to the board. If the file does not appear in the pop-up window, click **Add File**, navigate to \<*directory*>**\c4gxsdi.sof**, and click **Open**.


You must reload the reference design each time you apply power to the board.

After you have set up the board, run the different variants described in the following sections.

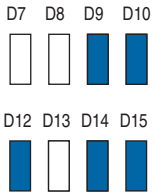
Parallel Loopback

To run the parallel loopback demonstration, follow these steps:

1. Connect an SDI signal generator to the receiver input of SDI IN 1(BNC J9).
2. Connect an SDI signal analyzer to the transmitter output of SDI OUT 2 (BNC J1).

3. The parallel loopback demonstration runs. The LEDs indicate the following conditions:
   - LED D9 and D10 illuminate when the receiver receives video signal standards.
   - LED D15 illuminates when the receiver is word aligned at port 1.
   - LED D14 illuminates when the received line format is stable at port 1.
   - LED D12 illuminates when the receiver frame format is stable at port 1.

Figure 4. Condition of LEDs for Parallel Loopback Demonstration



LEDs on the SDI HSMC indicate the following conditions:

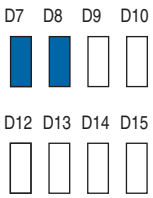
- LED D8 illuminates when the video signal standard for the receiver is detected at port 1.
- LED D12 illuminates when the video signal standard for the transmitter is detected at port 1.

Test Pattern Transmitter

To run the test pattern transmitter demonstration, follow these steps:

1. Connect an SDI signal analyzer to the transmitter output `SDI OUT 1` (BNC J8).
2. The test pattern demonstration runs. The LEDs indicate the following conditions:
   - LED D7 and D8 indicate the video signal standard for the internal pattern generator that transmits through port 1 in the transmitter. Refer to Figure 5.

Figure 5. Condition of LEDs for Test Pattern Transmitter Demonstration



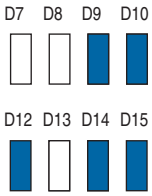
   - LED D9 on the SDI HSMC illuminates when the video signal standard for the transmitter is detected at port 1.
3. Check the result on the SDI signal analyzer.

Receiver Only

To run the receiver only demonstration, follow these steps:

1. Connect an SDI signal generator to the receiver input SDI IN 1 (BNC J9).
2. The receiver demonstration runs. The LEDs indicate the following conditions:
   - LED D9 and D10 illuminate when the receiver receives video signal standards.
   - LED D15 illuminates when the receiver is word aligned at port 1.
   - LED D14 illuminates when the received line format is stable at port 1.
   - LED D12 illuminates when the receiver frame format is stable at port 1.

Figure 6. Condition of LEDs for Receiver Only Demonstration



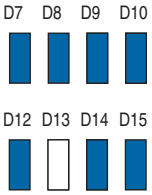
LED D8 on the SDI HSMC illuminates when the video signal standard for the receiver is detected at port 1.

Serial Loopback

To run the serial loopback demonstration, follow these steps:

1. Connect the transmitter output SDI OUT 1 (BNC J8) to the receiver input SDI IN 1 (BNC J9).
2. The serial loopback demonstration runs. The LEDs indicate the following conditions:
   - LED D7 and D8 indicate the video signal standard for the internal pattern generator at SDI IN 1.
   - LED D9 and D10 flash to indicate the video signal standard for the receiver.
   - LED D15 illuminates when the receiver is word aligned at port 1.
   - LED D14 illuminates when the received line format is stable at port 1.
   - LED D12 illuminates when the receiver frame format is stable at port 1.

Figure 7. Condition of LEDs for Serial Loopback Demonstration



LEDs on the SDI HSMC indicate the following conditions:

- LED D9 illuminates when the video signal standard for the transmitter is detected at port 1.
- LED D8 illuminates when the video signal standard for the receiver is detected at port 1.

Conclusion

This application note describes how to use the SDI reference design with the Cyclone IV GX FPGA board and SDI HSMC. You can use the different variants discussed to evaluate the SDI MegaCore function for integration into Altera FPGA designs.

Document Revision History

Table 6 lists the revision history for this document.

Table 6. Document Revision History

Date	Version	Changes
September 2011	1.2	■ Updated Figure 1, Figure 2, and Figure 3. ■ Updated "Clock Input Differential SMA Connectors" section. ■ Updated the design files.
March 2011	1.1	■ Updated Figure 1. ■ Updated "Clock Input Differential SMA Connectors" section. ■ Updated "Loopback FIFO Buffer" section.
March 2011	1.0	Initial Release.