3. TriMatrix Embedded Memory Blocks in Stratix IV Devices

SIV51003-3.3

This chapter describes the TriMatrix embedded memory blocks in Stratix® IV devices. TriMatrix embedded memory blocks provide three different sizes of embedded SRAM to efficiently address the needs of Stratix IV FPGA designs. TriMatrix memory includes 640-bit memory logic array blocks (MLABs), 9-Kbit M9K blocks, and 144-Kbit M144K blocks. MLABs have been optimized to implement filter delay lines, small FIFO buffers, and shift registers. You can use the M9K blocks for general purpose memory applications and the M144K blocks for processor code storage, packet buffering, and video frame buffering.

You can independently configure each embedded memory block to be a single- or dual-port RAM, FIFO buffer, ROM, or shift register using the Quartus® II MegaWizard™ Plug-In Manager. You can stitch together multiple blocks of the same type to produce larger memories with minimal timing penalty. TriMatrix memory provides up to 31,491 Kbits of embedded SRAM at up to 600 MHz operation.

This chapter contains the following sections:

Overview

Table 3–1 lists the features supported by the three sizes of TriMatrix memory.

Table 3–1. Summary of TriMatrix Memory Features (Part 1 of 2)

Feature	MLABs	M9K Blocks	M144K Blocks
Maximum performance	600 MHz	600 MHz	540 MHz
Total RAM bits (including parity bits)	640	9216	147,456
Configurations (depth × width)	64 × 8 64 × 9 64 × 10 32 × 16 32 × 18 32 × 20	8K × 1 4K × 2 2K × 4 1K × 8 1K × 9 512 × 16 512 × 18 256 × 32 256 × 36	16K × 8 16K × 9 8K × 16 8K × 18 4K × 32 4K × 36 2K × 64 2K × 72
Parity bits	Supported	Supported	Supported

Table 3–1. Summary of TriMatrix Memory Features (Part 2 of 2)

Feature	MLABs	M9K Blocks	M144K Blocks
Byte enable	Supported	Supported	Supported
Packed mode	—	Supported	Supported
Address clock enable	Supported	Supported	Supported
Single-port memory	Supported	Supported	Supported
Simple dual-port memory	Supported	Supported	Supported
True dual-port memory	—	Supported	Supported
Embedded shift register	Supported	Supported	Supported
ROM	Supported	Supported	Supported
FIFO buffer	Supported	Supported	Supported
Simple dual-port mixed width support	—	Supported	Supported
True dual-port mixed width support	—	Supported	Supported
Memory Initialization File (**.mif**)	Supported	Supported	Supported
Mixed clock mode	Supported	Supported	Supported
Power-up condition	Outputs cleared if registered, otherwise reads memory contents	Outputs cleared	Outputs cleared
Register clears	Output registers	Output registers	Output registers
Write/Read operation triggering	Write: Falling clock edges Read: Rising clock edges	Write and Read: Rising clock edges	Write and Read: Rising clock edges
Same-port read-during-write	Outputs set to **don't care**	Outputs set to **old data** or **new data**	Outputs set to **old data** or **new data**
Mixed-port read-during-write	Outputs set to **old data**, **new data**, or **don't care** *(1)*	Outputs set to **old data** or **don't care**	Outputs set to **old data** or **don't care**
ECC Support	Soft IP support using the Quartus II software	Soft IP support using the Quartus II software	Built-in support in ×64-wide SDP mode or soft IP support using the Quartus II software

Note to Table 3–1:

(1) The mixed-port read-during-write options of **new data** or **old data** are only supported for MLABs when you use both the read address registers and the output registers.

Table 3–2 lists the capacity and distribution of the TriMatrix memory blocks in each Stratix IV family member.

Table 3–2. TriMatrix Memory Capacity and Distribution in Stratix IV Devices (Part 1 of 2)

Device	MLABs	M9K Blocks	M144K Blocks	Total Dedicated RAM Bits (Dedicated Memory Blocks Only) (Kb)	Total RAM Bits (Including MLABs) (Kb)
EP4SE230	4,560	1,235	22	14,283	17,133
EP4SE360	7,072	1,248	48	18,144	22,564
EP4SE530	10,624	1,280	64	20,736	27,376
EP4SE820	16,261	1,610	60	23,130	33,294

Table 3–2. TriMatrix Memory Capacity and Distribution in Stratix IV Devices (Part 2 of 2)

Device	MLABs	M9K Blocks	M144K Blocks	Total Dedicated RAM Bits (Dedicated Memory Blocks Only) (Kb)	Total RAM Bits (Including MLABs) (Kb)
EP4SGX70	1,452	462	16	6,462	7,370
EP4SGX110	2,112	660	16	8,244	9,564
EP4SGX180	3,515	950	20	11,430	13,627
EP4SGX230	4,560	1,235	22	14,283	17,133
EP4SGX290	5,824	936	36	13,608	17,248
EP4SGX360	7,072	1,248	48	18,144	22,564
EP4SGX530	10,624	1,280	64	20,736	27,376
EP4S40G2	4,560	1,235	22	14,283	17,133
EP4S40G5	10,624	1280	64	20,736	27,376
EP4S100G2	4,560	1,235	22	14,283	17,133
EP4S100G3	5,824	936	36	13,608	17,248
EP4S100G4	7,072	1,248	48	18,144	22,564
EP4S100G5	10,624	1,280	64	20,736	27,376

TriMatrix Memory Block Types

While the M9K and M144K memory blocks are dedicated resources, the MLABs are dual-purpose blocks. They can be configured as regular logic array blocks (LABs) or as MLABs. Ten adaptive logic modules (ALMs) make up one MLAB. You can configure each ALM in an MLAB as either a 64 × 1 or a 32 × 2 block, resulting in a 64 × 10 or 32 × 20 simple dual-port SRAM block in a single MLAB.

Parity Bit Support

All TriMatrix memory blocks have built-in parity-bit support. The ninth bit associated with each byte can store a parity bit or serve as an additional data bit. No parity function is actually performed on the ninth bit.

Byte Enable Support

All TriMatrix memory blocks support byte enables that mask the input data so that only specific bytes of data are written. The unwritten bytes retain the previously written values. The write enable (`wren`) signals, along with the byte enable (`byteena`) signals, control the RAM blocks' write operations.

The default value for the byte enable signals is high (enabled), in which case writing is controlled only by the write enable signals. The byte enable registers have no clear port. When using parity bits on the M9K and M144K blocks, the byte enable controls all nine bits (eight bits of data plus one parity bit). When using parity bits on the MLAB, the byte-enable controls all 10 bits in the widest mode.

The MSB for the byteena signal corresponds to the MSB of the data bus and the LSB of the byteena signal corresponds to the LSB of the data bus. For example, if you use a RAM block in ×18 mode, with byteena = 01, data[8..0] is enabled, and data[17..9] id disabled. Similarly, if byteena = 11, both data[8..0] and data[17..9] are enabled. Byte enables are active high.

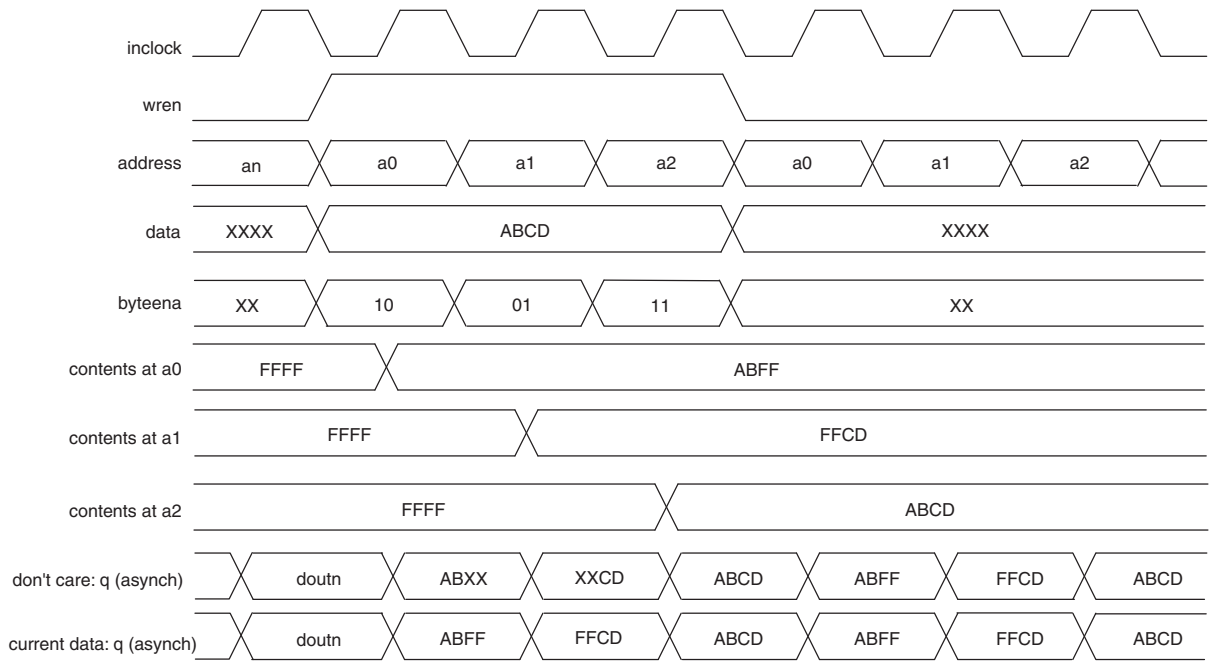
You cannot use the byte enable feature when using the error correction coding (ECC) feature on M144K blocks.

Byte enables are only supported for true dual-port memory configurations when both the PortA and PortB data widtByths of the individual M9K memory blocks are multiples of 8 or 9 bits. For example, if you implement a mixed data width memory configured with portA = 32 and portB = 8 as two separate 16 x 4 bit memories, you cannot use the byte enable feature.

Figure 3–1 shows how the write enable (wren) and byte enable (byteena) signals control the operations of the RAM blocks.

When a byte-enable bit is de-asserted during a write cycle, the corresponding data byte output can appear as either a "don't care" value or the current data at that location. The output value for the masked byte is controllable using the Quartus II software. When a byte-enable bit is asserted during a write cycle, the corresponding data byte output also depends on the setting chosen in the Quartus II software.

Figure 3–1. Byte Enable Functional Waveform



Packed Mode Support

Stratix IV M9K and M144K blocks support packed mode. The packed mode feature packs two independent single-port RAMs into one memory block. The Quartus II software automatically implements packed mode where appropriate by placing the physical RAM block into true dual-port mode and using the MSB of the address to distinguish between the two logical RAMs. The size of each independent single-port RAM must not exceed half of the target block size.

Address Clock Enable Support

All Stratix IV memory blocks support address clock enable, which holds the previous address value for as long as the signal is enabled (`addressstall = 1`). When the memory blocks are configured in dual-port mode, each port has its own independent address clock enable. The default value for the address clock enable signals is low (disabled).

Figure 3–2 shows an address clock enable block diagram. The address clock enable is referred to by the port name `addressstall`.

Figure 3–2. Address Clock Enable

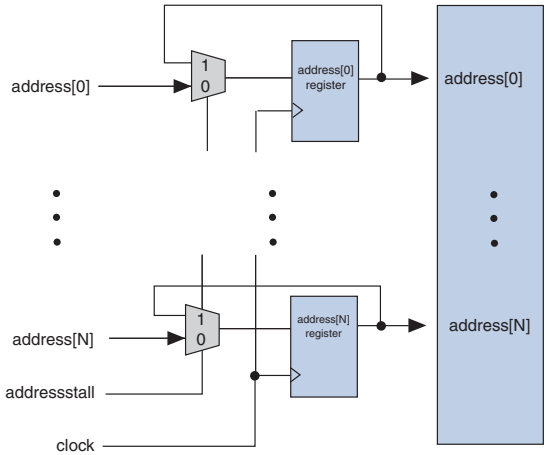


Figure 3–3 shows the address clock enable waveform during the read cycle.

Figure 3–3. Address Clock Enable During Read Cycle Waveform

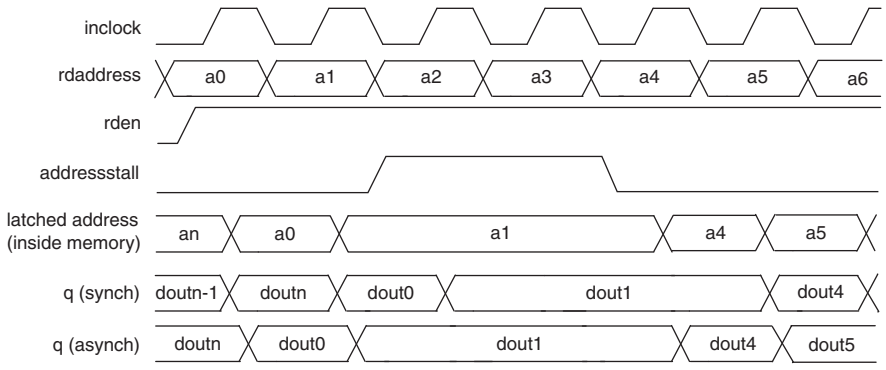
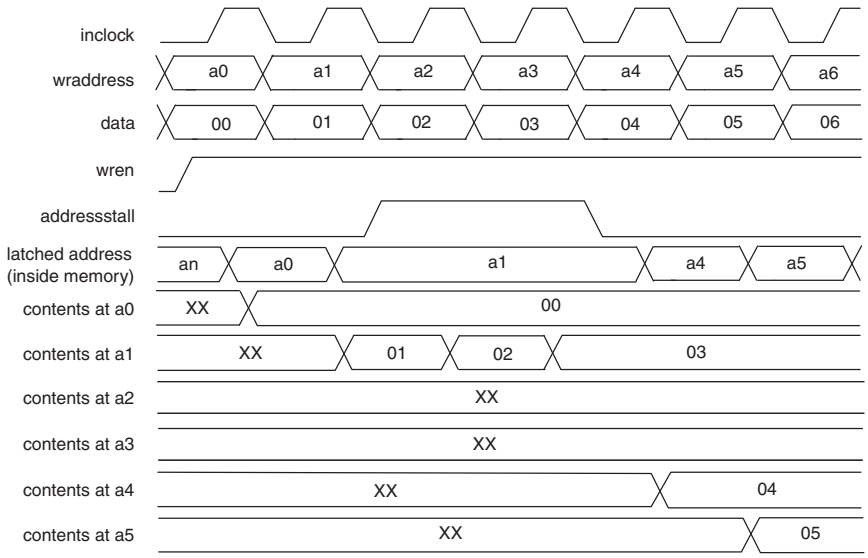


Figure 3–4 shows the address clock enable waveform during the write cycle.

Figure 3–4. Address Clock Enable During the Write Cycle Waveform



Mixed Width Support

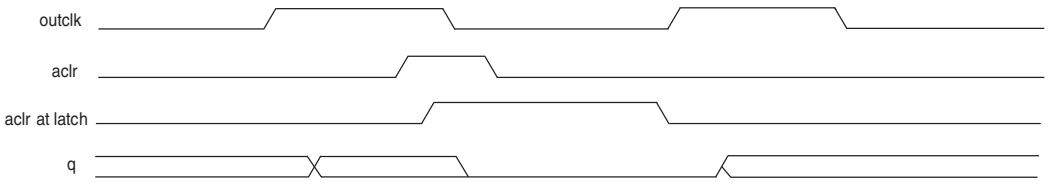
M9K and M144K memory blocks support mixed data widths inherently. MLABs can support mixed data widths through emulation using the Quartus II software. When using simple dual-port, true dual-port, or FIFO modes, mixed width support allows you to read and write different data widths to a memory block. For more information about the different widths supported per memory mode, refer to "Memory Modes" on page 3–9.

MLABs do not support mixed-width FIFO mode.

Asynchronous Clear

Stratix IV TriMatrix memory blocks support asynchronous clears on output latches and output registers. Therefore, if your RAM is not using output registers, you can still clear the RAM outputs using the output latch asynchronous clear. Figure 3–5 shows a waveform of the output latch asynchronous clear function.

Figure 3–5. Output Latch Asynchronous Clear Waveform



You can selectively enable asynchronous clears per logical memory using the Quartus II RAM MegaWizard Plug-In Manager.

For more information, refer to the *Internal Memory (RAM and ROM) User Guide*.

Error Correction Code (ECC) Support

Stratix IV M144K blocks have built-in support for error correction code (ECC) when in ×64-wide simple dual-port mode. ECC allows you to detect and correct data errors in the memory array. The M144K blocks have a single-error-correction double-error-detection (SECDED) implementation. SECDED can detect and fix a single bit error in a 64-bit word, or detect two bit errors in a 64-bit word. It cannot detect three or more errors.

The M144K ECC status is communicated using a three-bit status flag `eccstatus[2..0]`. The status flag can be either registered or unregistered. When registered, it uses the same clock and asynchronous clear signals as the output registers. When unregistered, it cannot be asynchronously cleared.

Table 3–3 lists the truth table for the ECC status flags.

Table 3–3. Truth Table for ECC Status Flags

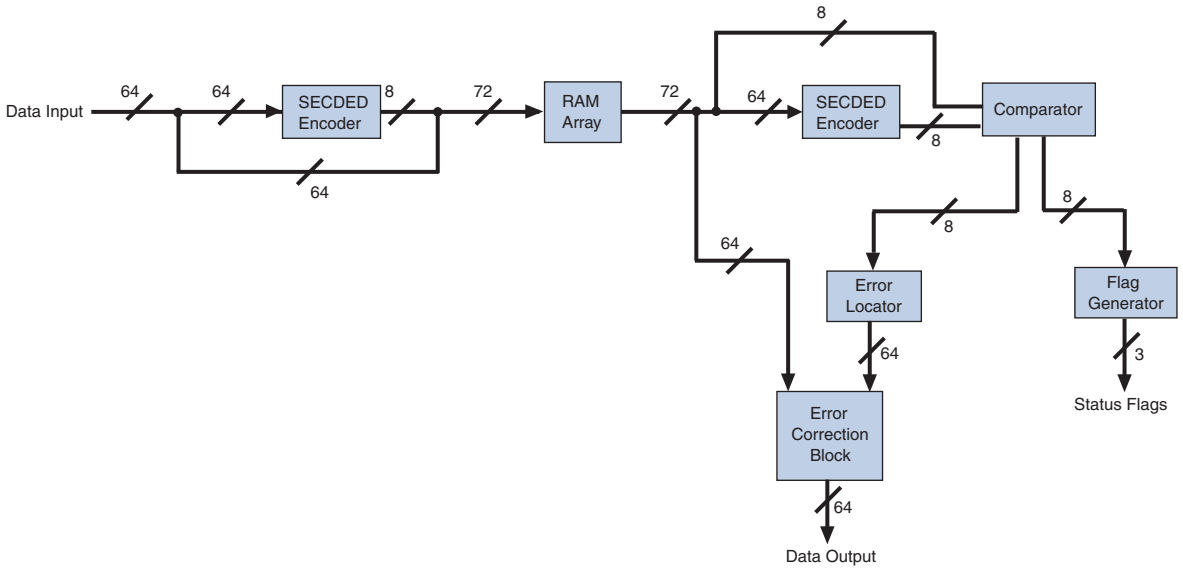
Status	eccstatus[2]	eccstatus[1]	eccstatus[0]
No error	0	0	0
Single error and fixed	0	1	1
Double error and no fix	1	0	1
Illegal	0	0	1
Illegal	0	1	0
Illegal	1	0	0
Illegal	1	1	X

You cannot use the byte enable feature when ECC is engaged.

Read-during-write “old data mode” is not supported when ECC is engaged.

Figure 3–6 shows a diagram of the ECC block of the M144K block.

Figure 3–6. ECC Block Diagram of the M144K Block



Memory Modes

Stratix IV TriMatrix memory blocks allow you to implement fully synchronous SRAM memory in multiple modes of operation. M9K and M144K blocks do not support asynchronous memory (unregistered inputs). MLABs support asynchronous (flow-through) read operations.

Depending on which TriMatrix memory block you target, you can use the following:

- "Single-Port RAM Mode" on page 3–10
- "Simple Dual-Port Mode" on page 3–11
- "True Dual-Port Mode" on page 3–14
- "Shift-Register Mode" on page 3–16
- "ROM Mode" on page 3–17
- "FIFO Mode" on page 3–17

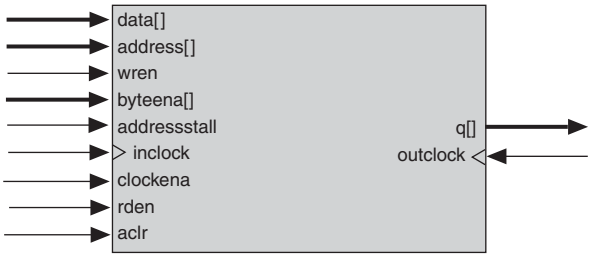
CAUTION

When using the memory blocks in ROM, single-port, simple dual-port, or true dual-port mode, you can corrupt the memory contents if you violate the setup or hold-time on any of the memory block input registers. This applies to both read and write operations.

Single-Port RAM Mode

All TriMatrix memory blocks support single-port mode. Single-port mode allows you to do either one-read or one-write operation at a time. Simultaneous reads and writes are not supported in single-port mode. Figure 3–7 shows the single-port RAM configuration.

Figure 3–7. Single-Port RAM ***(Note 1)***



Note to Figure 3–7:

(1) You can implement two single-port memory blocks in a single M9K or M144K block. For more information, refer to "Packed Mode Support" on page 3–5.

During a write operation, RAM output behavior is configurable. If you use the read-enable signal and perform a write operation with read enable de-activated, the RAM outputs retain the values they held during the most recent active read enable. If you activate read enable during a write operation, or if you are not using the read-enable signal at all, the RAM outputs either show the "new data" being written, the "old data" at that address, or a "don't care" value. To choose the desired behavior, set the read-during-write behavior to either **new data**, **old data**, or **don't care** in the RAM MegaWizard Plug-In Manager in the Quartus II software. For more information, refer to "Read-During-Write Behavior" on page 3–19.

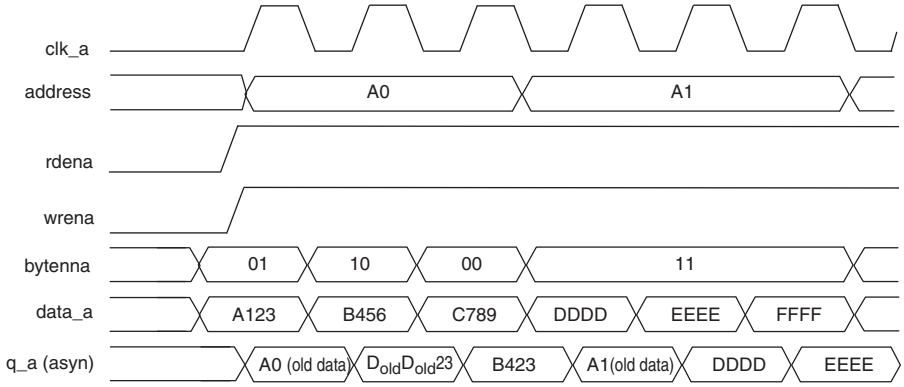
Table 3–4 lists the possible port width configurations for TriMatrix memory blocks in single-port mode.

Table 3–4. Port Width Configurations for MLABs, M9K, and M144K Blocks (Single-Port Mode)

	MLABs	M9K Blocks	M144K Blocks
Port Width Configurations	64 × 8 64 × 9 64 × 10 32 × 16 32 × 18 32 × 20	8K × 1 4K × 2 2K × 4 1K × 8 1K × 9 512 × 16 512 × 18 256 × 32 256 × 36	16K × 8 16K × 9 8K × 16 8K × 18 4K × 32 4K × 36 2K × 64 2K × 72

Figure 3–8 shows timing waveforms for read and write operations in single-port mode with unregistered outputs. Registering the RAM's outputs simply delays the q output by one clock cycle.

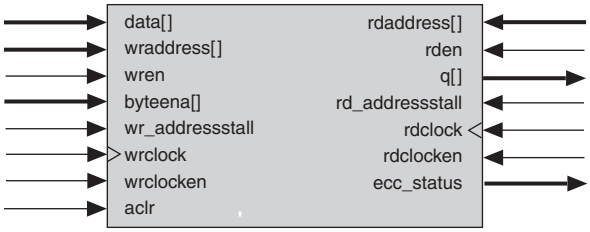
Figure 3–8. Timing Waveform for Read-Write Operations (Single-Port Mode)



Simple Dual-Port Mode

All TriMatrix memory blocks support simple dual-port mode. Simple dual-port mode allows you to perform one read and one write operation to different locations at the same time. Write operation happens on port A; read operation happens on port B. Figure 3–9 shows a simple dual-port configuration.

Figure 3–9. Stratix IV Simple Dual-Port Memory *(Note 1)*



Note to Figure 3–9:

(1) Simple dual-port RAM supports input/output clock mode in addition to read/write clock mode.

Simple dual-port mode supports different read and write data widths (mixed-width support). Table 3–5 lists the mixed width configurations for M9K blocks in simple dual-port mode. MLABs do not have native support for mixed-width operation. The Quartus II software implements mixed-width memories in MLABs by using more than one MLAB.

Table 3–5. M9K Block Mixed-Width Configurations (Simple Dual-Port Mode) (Part 1 of 2)

Read Port	Write Port								
	8K × 1	4K × 2	2K × 4	1K × 8	512 × 16	256 × 32	1K × 9	512 × 18	256 × 36
8K × 1	Y	Y	Y	Y	Y	Y	—	—	—
4K × 2	Y	Y	Y	Y	Y	Y	—	—	—
2K × 4	Y	Y	Y	Y	Y	Y	—	—	—

Table 3–5. M9K Block Mixed-Width Configurations (Simple Dual-Port Mode) (Part 2 of 2)

Read Port	Write Port								
	8K × 1	4K × 2	2K × 4	1K × 8	512 × 16	256 × 32	1K × 9	512 × 18	256 × 36
1K × 8	Y	Y	Y	Y	Y	Y	—	—	—
512 × 16	Y	Y	Y	Y	Y	Y	—	—	—
256 × 32	Y	Y	Y	Y	Y	Y	—	—	—
1K × 9	—	—	—	—	—	—	Y	Y	Y
512 × 18	—	—	—	—	—	—	Y	Y	Y
256 × 36	—	—	—	—	—	—	Y	Y	Y

Table 3–6 lists the mixed-width configurations for M144K blocks in simple dual-port mode.

Table 3–6. M144K Block Mixed-Width Configurations (Simple Dual-Port Mode)

Read Port	Write Port							
	16K × 8	8K × 16	4K × 32	2K × 64	16K × 9	8K × 18	4K × 36	2K × 72
16K × 8	Y	Y	Y	Y	—	—	—	—
8K × 16	Y	Y	Y	Y	—	—	—	—
4K × 32	Y	Y	Y	Y	—	—	—	—
2K × 64	Y	Y	Y	Y	—	—	—	—
16K × 9	—	—	—	—	Y	Y	Y	Y
8K × 18	—	—	—	—	Y	Y	Y	Y
4K × 36	—	—	—	—	Y	Y	Y	Y
2K × 72	—	—	—	—	Y	Y	Y	Y

In simple dual-port mode, M9K and M144K blocks support separate write-enable and read-enable signals. You can save power by keeping the read-enable signal low (inactive) when not reading. Read-during-write operations to the same address can either output a "don't care" value or "old data" value. To choose the desired behavior, set the read-during-write behavior to either **don't care** or **old data** in the RAM MegaWizard Plug-In Manager in the Quartus II software. For more information, refer to "Read-During-Write Behavior" on page 3–19.

MLABs only support a write-enable signal. For MLABs, you can set the same-port read-during-write behavior to **don't care** and the mixed-port read-during-write behavior to either **don't care** or **old data**. The available choices depend on the configuration of the MLAB. There is no "new data" option for MLABs.

Figure 3–10 shows timing waveforms for read and write operations in simple dual-port mode with unregistered outputs. Registering the RAM outputs simply delays the q output by one clock cycle.

Figure 3–10. Simple Dual-Port Timing Waveforms

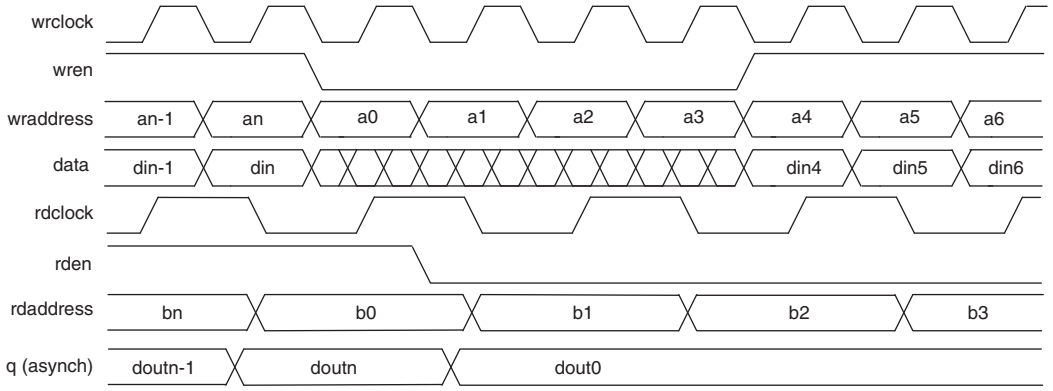
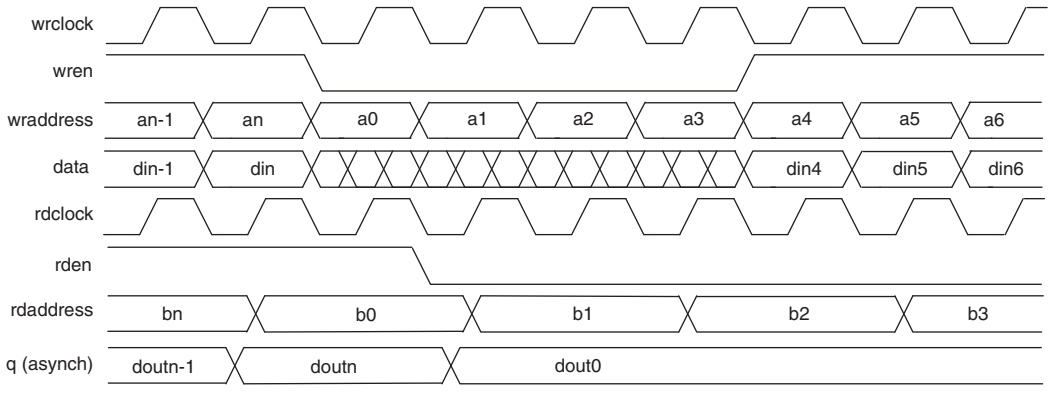


Figure 3–11 shows timing waveforms for read and write operations in mixed-port mode with unregistered outputs.

Figure 3–11. Mixed-Port Read-During-Write Timing Waveforms

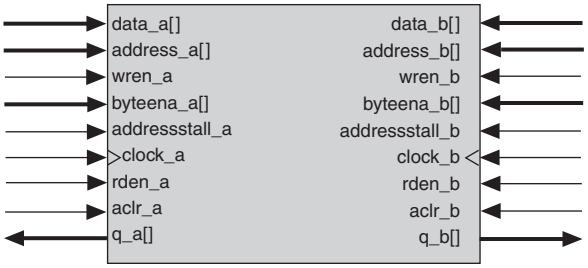


True Dual-Port Mode

Stratix IV M9K and M144K blocks support true dual-port mode. Sometimes called bi-directional dual-port, this mode allows you to perform any combination of two port operations: two reads, two writes, or one read and one write at two different clock frequencies.

Figure 3–12 shows the true dual-port RAM configuration.

Figure 3–12. Stratix IV True Dual-Port Memory ***(Note 1)***



Note to Figure 3–12:

(1) True dual-port memory supports input/output clock mode in addition to independent clock mode.

The widest bit configuration of the M9K and M144K blocks in true dual-port mode is as follows:

- M9K: 512 × 16-bit (or 512 ×18-bit with parity)
- M144K: 4K × 32-bit (or 4K ×36-bit with parity)

Wider configurations are unavailable because the number of output drivers is equivalent to the maximum bit width of the respective memory block. Because true dual-port RAM has outputs on two ports, its maximum width equals half of the total number of output drivers. Table 3–7 lists the possible M9K block mixed-port width configurations in true dual-port mode.

Table 3–7. M9K Block Mixed-Width Configuration (True Dual-Port Mode)

Read Port	Write Port						
	8K × 1	4K × 2	2K × 4	1K × 8	512 × 16	1K × 9	512 × 18
8K × 1	Y	Y	Y	Y	Y	—	—
4K × 2	Y	Y	Y	Y	Y	—	—
2K × 4	Y	Y	Y	Y	Y	—	—
1K × 8	Y	Y	Y	Y	Y	—	—
512 × 16	Y	Y	Y	Y	Y	—	—
1K × 9	—	—	—	—	—	Y	Y
512 × 18	—	—	—	—	—	Y	Y

Table 3–8 lists the possible M144K block mixed-port width configurations in true dual-port mode.

Table 3–8. M144K Block Mixed-Width Configurations (True Dual-Port Mode)

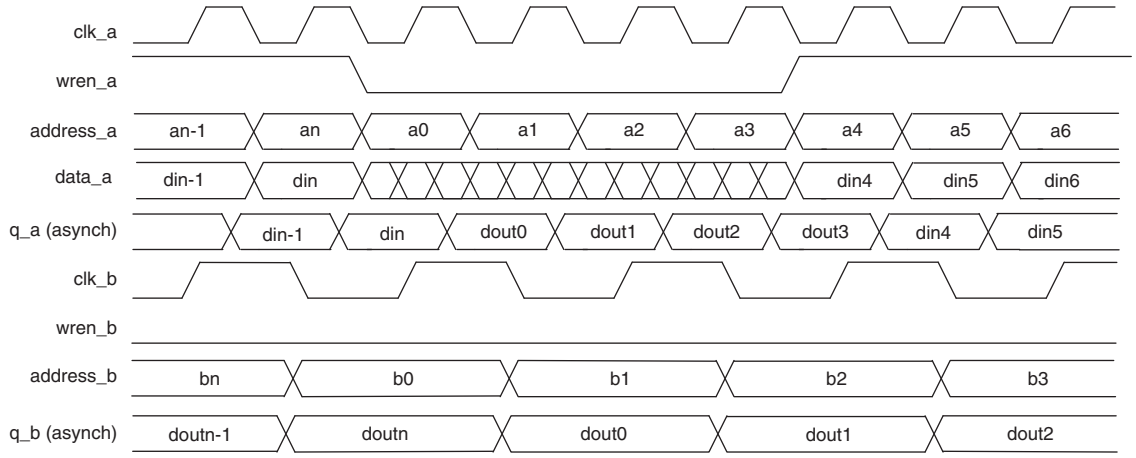
Read Port	Write Port					
	16K × 8	8K × 16	4K × 32	16K × 9	8K × 18	4K × 36
16K × 8	Y	Y	Y	—	—	—
8K × 16	Y	Y	Y	—	—	—
4K × 32	Y	Y	Y	—	—	—
16K × 9	—	—	—	Y	Y	Y
8K × 18	—	—	—	Y	Y	Y
4K × 36	—	—	—	Y	Y	Y

In true dual-port mode, M9K and M144K blocks support separate write-enable and read-enable signals. You can save power by keeping the read-enable signal low (inactive) when not reading. Read-during-write operations to the same address can either output "new data" at that location or "old data". To choose the desired behavior, set the read-during-write behavior to either **new data** or **old data** in the RAM MegaWizard Plug-In Manager in the Quartus II software. For more information, refer to "Read-During-Write Behavior" on page 3–19.

In true dual-port mode, you can access any memory location at any time from either port. When accessing the same memory location from both ports, you must avoid possible write conflicts. A write conflict happens when you attempt to write to the same address location from both ports at the same time. This results in unknown data being stored to that address location. No conflict resolution circuitry is built into the Stratix IV TriMatrix memory blocks. You must handle address conflicts external to the RAM block.

Figure 3–13 shows true dual-port timing waveforms for the write operation at port A and the read operation at port B, with the read-during-write behavior set to **new data**. Registering the RAM's outputs simply delays the `q` outputs by one clock cycle.

Figure 3–13. True Dual-Port Timing Waveform



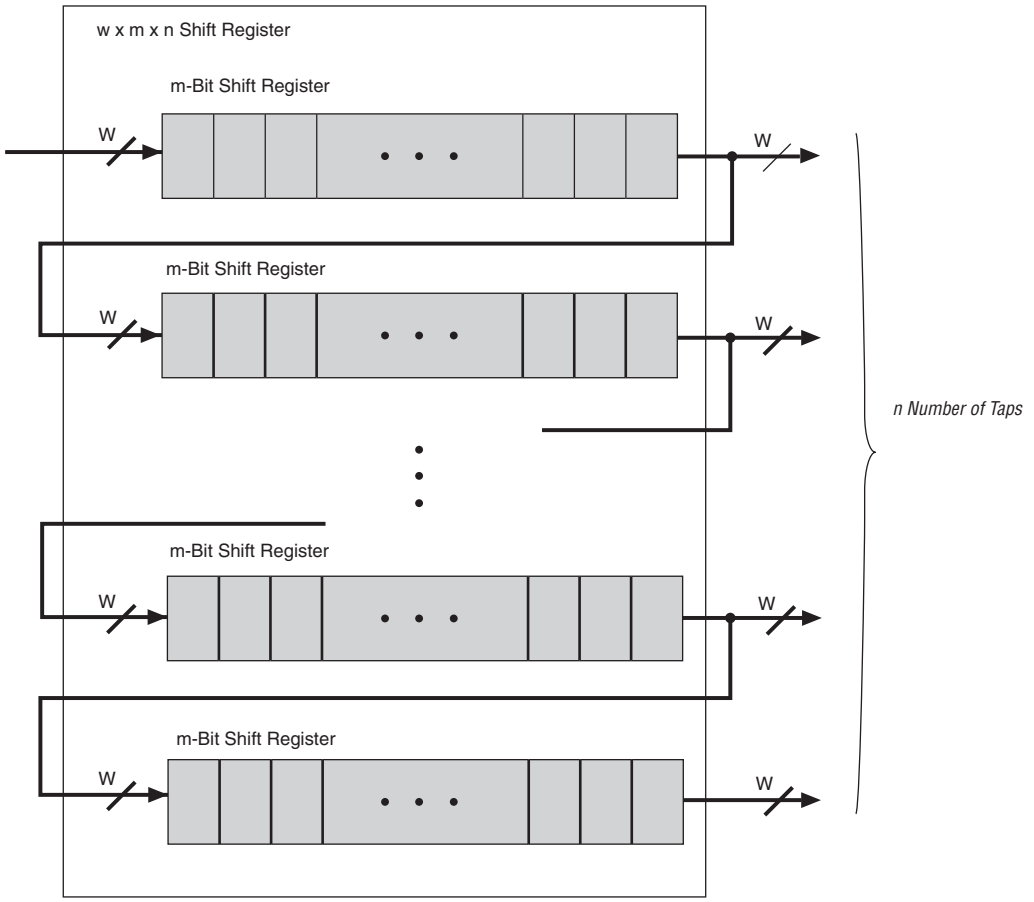
Shift-Register Mode

All Stratix IV memory blocks support shift register mode. Embedded memory block configurations can implement shift registers for digital signal processing (DSP) applications, such as finite impulse response (FIR) filters, pseudo-random number generators, multi-channel filtering, and auto- and cross-correlation functions. These and other DSP applications require local data storage, traditionally implemented with standard flipflops that quickly exhaust many logic cells for large shift registers. A more efficient alternative is to use embedded memory as a shift-register block, which saves logic cell and routing resources.

The size of a shift register (w × m × n) is determined by the input data width (w), the length of the taps (m), and the number of taps (n). You can cascade memory blocks to implement larger shift registers.

Figure 3–14 shows the TriMatrix memory block in shift-register mode.

Figure 3–14. Shift-Register Memory Configuration



ROM Mode

All Stratix IV TriMatrix memory blocks support ROM mode. A **.mif** file initializes the ROM contents of these blocks. The address lines of the ROM are registered on M9K and M144K blocks, but can be unregistered on MLABs. The outputs can be registered or unregistered. Output registers can be asynchronously cleared. The ROM read operation is identical to the read operation in the single-port RAM configuration.

FIFO Mode

All TriMatrix memory blocks support FIFO mode. MLABs are ideal for designs with many small, shallow FIFO buffers. To implement FIFO buffers in your design, use the Quartus II software FIFO MegaWizard Plug-In Manager. Both single- and dual-clock (asynchronous) FIFO buffers are supported.

For more information about implementing FIFO buffers, refer to the *SCFIFO and DCFIFO Megafunctions User Guide*.

MLABs do not support mixed-width FIFO mode.

Clocking Modes

Stratix IV TriMatrix memory blocks support the following clocking modes:

- "Independent Clock Mode" on page 3–18
- "Input/Output Clock Mode" on page 3–18
- "Read/Write Clock Mode" on page 3–18
- "Single Clock Mode" on page 3–18

CAUTION

Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

Table 3–9 lists which clocking mode/memory mode combinations are supported.

Table 3–9. TriMatrix Memory Clock Modes

Clocking Mode	True Dual-Port Mode	Simple Dual-Port Mode	Single-Port Mode	ROM Mode	FIFO Mode
Independent	Y	—	—	Y	—
Input/output	Y	Y	Y	Y	—
Read/write	—	Y	—	—	Y
Single clock	Y	Y	Y	Y	Y

Independent Clock Mode

Stratix IV TriMatrix memory blocks can implement independent clock mode for true dual-port memories. In this mode, a separate clock is available for each port (clock A and clock B). Clock A controls all registers on the port A side; clock B controls all registers on the port B side. Each port also supports independent clock enables for both port A and port B registers, respectively. Asynchronous clears are supported only for output latches and output registers on both ports.

Input/Output Clock Mode

Stratix IV TriMatrix memory blocks can implement input/output clock mode for true dual-port and simple dual-port memories. In this mode, an input clock controls all registers related to the data input to the memory block including data, address, byte enables, read enables, and write enables. An output clock controls the data output registers. Asynchronous clears are available on output latches and output registers only.

Read/Write Clock Mode

Stratix IV TriMatrix memory blocks can implement read/write clock mode for simple dual-port memories. In this mode, a write clock controls the data-input, write-address, and write-enable registers. Similarly, a read clock controls the data-output, read-address, and read-enable registers. The memory blocks support independent clock enables for both read and write clocks. Asynchronous clears are available on data output latches and registers only.

When using read/write clock mode, if you perform a simultaneous read/write to the same address location, the output read data is unknown. If you require the output data to be a known value, use either single-clock mode or input/output clock mode and choose the appropriate read-during-write behavior in the MegaWizard Plug-In Manager.

Single Clock Mode

Stratix IV TriMatrix memory blocks can implement single-clock mode for true dual-port, simple dual-port, and single-port memories. In this mode, a single clock, together with a clock enable, is used to control all registers of the memory block. Asynchronous clears are available on output latches and output registers only.

Design Considerations

This section describes guidelines for designing with TriMatrix memory blocks.

Selecting TriMatrix Memory Blocks

The Quartus II software automatically partitions user-defined memory into embedded memory blocks by taking into account both speed and size constraints placed on your design. For example, the Quartus II software may spread memory out across multiple memory blocks when resources are available to increase the performance of the design. You can manually assign memory to a specific block size using the RAM MegaWizard Plug-In Manager.

MLABs can implement single-port SRAM through emulation using the Quartus II software. Emulation results in minimal additional logic resources being used. Because of the dual-purpose architecture of the MLAB, it only has data input registers and output registers in the block. MLABs gain input address registers and additional data output registers from ALMs.

For more information about register packing, refer to the *Logic Array Blocks and Adaptive Logic Modules in Stratix IV Devices* chapter.

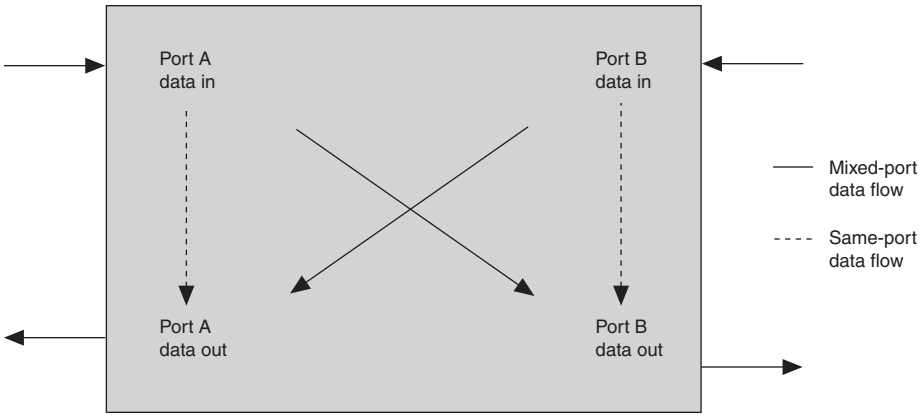
Conflict Resolution

When using memory blocks in true dual-port mode, it is possible to attempt two write operations to the same memory location (address). Because no conflict resolution circuitry is built into the memory blocks, this results in unknown data being written to that location. Therefore, you must implement conflict resolution logic external to the memory block to avoid address conflicts.

Read-During-Write Behavior

You can customize the read-during-write behavior of the Stratix IV TriMatrix memory blocks to suit your design needs. Two types of read-during-write operations are available: same port and mixed port. Figure 3–15 shows the difference between the two types.

Figure 3–15. Stratix IV Read-During-Write Data Flow

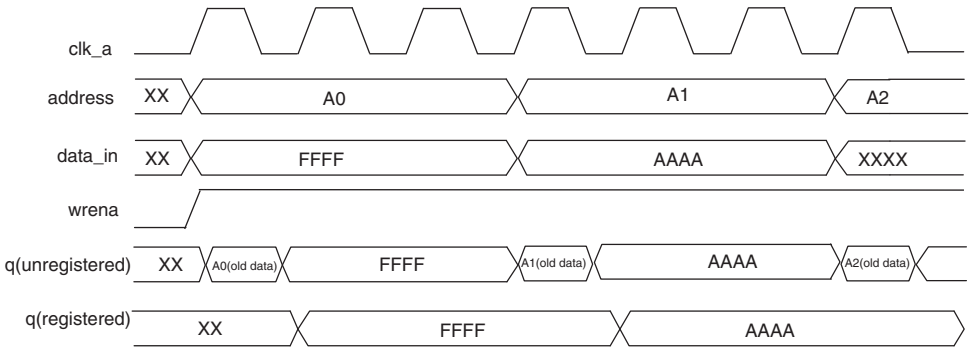


Same-Port Read-During-Write Mode

This mode applies to either a single-port RAM or the same port of a true dual-port RAM. For MLABs, the output of the MLABs can only be set to **don't care** in same-port read-during-write mode. In this mode, the output of the MLABs is unknown during a write cycle. There is a window near the falling edge of the clock during which the output is unknown. Prior to that window, "old data" is read out; after that window, "new data" is seen at the output.

Figure 3–16 shows sample functional waveforms of same-port read-during-write behavior in don't care mode for MLABs.

Figure 3–16. MLABs Same-Port Read-During Write: Don't Care Mode



For M9K and M144K memory blocks, three output choices are available in same-port read-during-write mode: "new data" (or flow-through) or "old data". In new data mode, the "new data" is available on the rising edge of the same clock cycle on which it was written. In old data mode, the RAM outputs reflect the "old data" at that address before the write operation proceeds. In don't care mode, the RAM outputs "unknown values" for a read-during-write operation.

Figure 3–17 shows sample functional waveforms of same-port read-during-write behavior in new data mode for M9K and M144K blocks.

Figure 3–17. M9K and M144K Blocks Same-Port Read-During-Write: New Data Mode

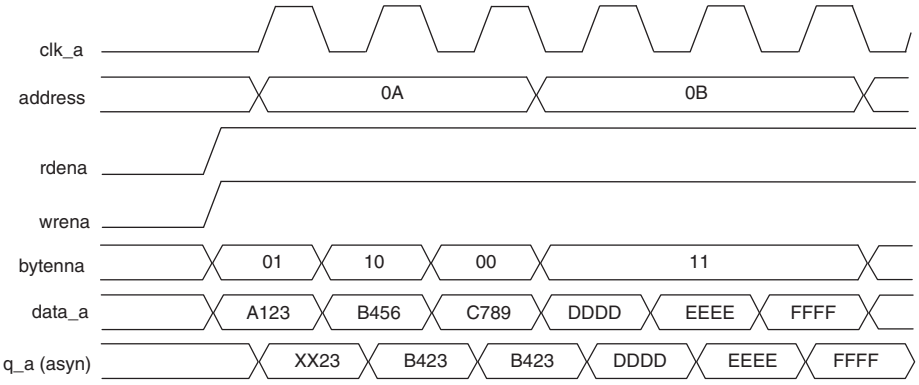
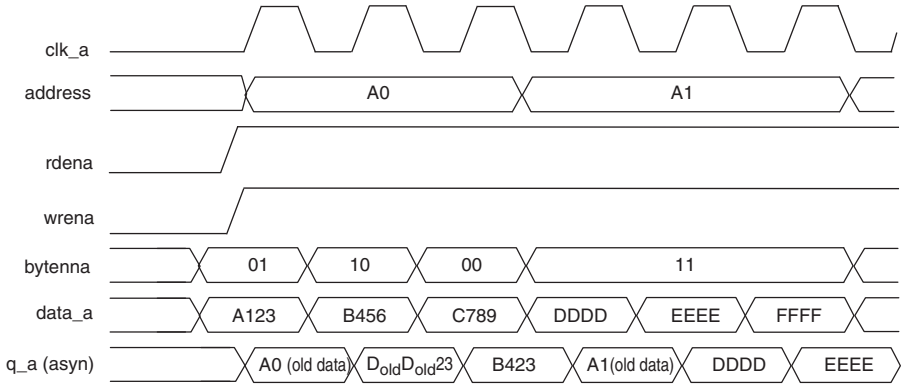


Figure 3–18 shows sample functional waveforms of same-port read-during-write behavior in old data mode for M9K and M144K blocks.

Figure 3–18. M9K and M144K Blocks Same-Port Read-During-Write: Old Data Mode



Mixed-Port Read-During-Write Mode

This mode applies to a RAM in simple or true dual-port mode that has one port reading from and the other port writing to the same address location with the same clock.

In this mode, you have two output choices if you use the output register: "old data," or "don't care". With MLABs, you also have the output register "new data." In old data mode, a read-during-write operation to different ports causes the RAM outputs to reflect the "old data" at that address location. In don't care mode, the same operation results in a "don't care" or "unknown" value on the RAM outputs.

Read-during-write behavior is controlled with the RAM MegaWizard Plug-In Manager. For more information, refer to the *Internal Memory (RAM and ROM) User Guide*.

Figure 3–19 shows a sample functional waveform of mixed-port read-during-write behavior for old data mode in MLABs.

Figure 3–19. MLABs Mixed-Port Read-During-Write: Old Data Mode

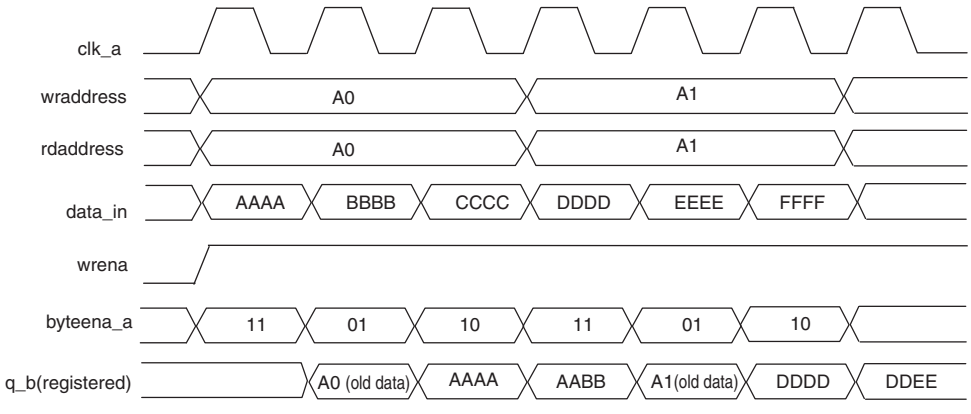


Figure 3–20 shows a sample functional waveform of mixed-port read-during-write behavior for don't care mode in MLABs.

Figure 3–20. MLABs Mixed-Port Read-During-Write: Don't Care Mode

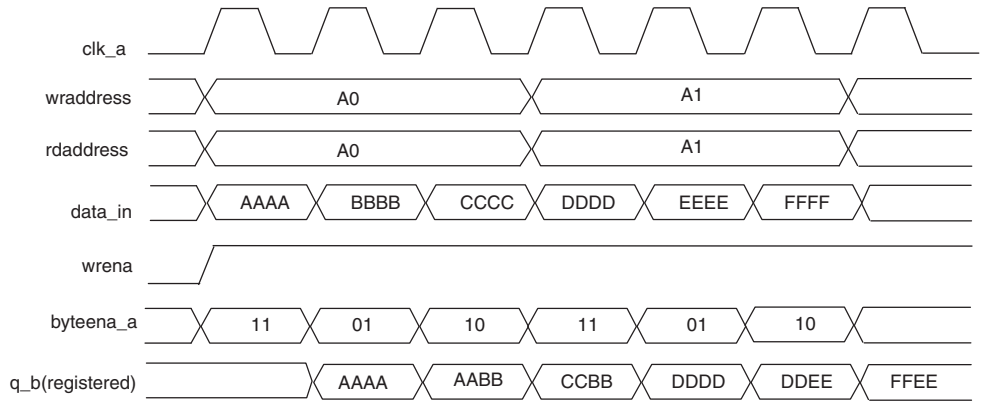


Figure 3–21 shows a sample functional waveform of mixed-port read-during-write behavior for old data mode in M9K and M144K blocks.

Figure 3–21. M9K and M144K Blocks Mixed-Port Read-During Write: Old Data Mode

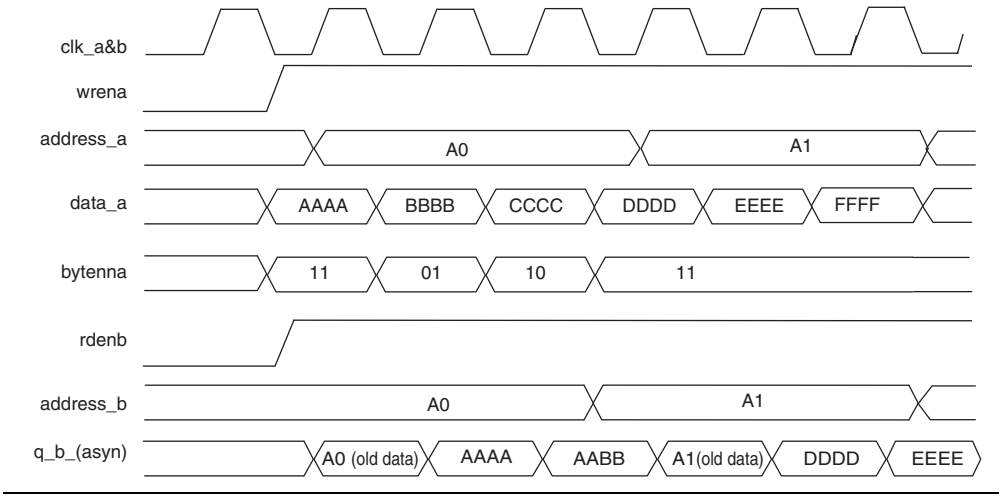
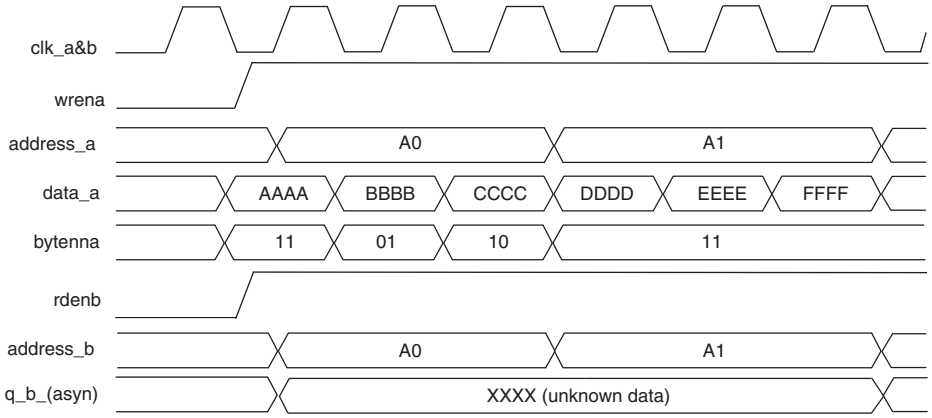


Figure 3–22 shows a sample functional waveform of mixed-port read-during-write behavior for don't care mode in M9K and M144K blocks.

Figure 3–22. M9K and M144K Blocks Mixed-Port Read-During Write: Don't Care Mode



Mixed-port read-during-write is not supported when two different clocks are used in a dual-port RAM. The output value is unknown during a dual-clock mixed-port read-during-write operation.

Power-Up Conditions and Memory Initialization

M9K memory cells are initialized to all zeros through a default **.mif** file in the Quartus II software. However, you may specify your own initialization of the memory cells through a defined **.mif** file. M144K memory cells are not initialized and; therefore, come up in an undefined state. This is to prevent the programming file from being too large. Again, you may specify your own initialization of the memory cells through a defined **.mif** file.

MLABs power up to zero if output registers are used and power up reading the memory contents if output registers are not used. You must take this into consideration when designing logic that might evaluate the initial power-up values of the MLAB memory block. For Stratix IV devices, the Quartus II software initializes the RAM cells to zero unless there is a **.mif** file specified.

As mentioned, all memory blocks support initialization using a **.mif** file. You can create **.mif** files in the Quartus II software and specify their use with the RAM MegaWizard Plug-In Manager when instantiating a memory in your design. Even if a memory is pre-initialized (for example, using a **.mif** file), it still powers up with its outputs cleared.

For more information about **.mif** files, refer to the *Internal Memory (RAM and ROM) User Guide* and the *Quartus II Handbook*.

Power Management

Stratix IV memory block clock-enables allow you to control clocking of each memory block to reduce AC power consumption. Use the read-enable signal to ensure that read operations only occur when you need them to. If your design does not need read-during-write, you can reduce your power consumption by de-asserting the read-enable signal during write operations, or any period when no memory operations occur.

The Quartus II software automatically places any unused memory blocks in low-power mode to reduce static power.

Document Revision History

Table 3–10 lists the revision history for this chapter.

Table 3–10. Document Revision History

Date	Version	Changes
December 2011	3.3	■ Updated the "Byte Enable Support" and "Mixed-Port Read-During-Write Mode" sections. ■ Updated Table 3–1.
February 2011	3.2	■ Updated the "Byte Enable Support" and "Power-Up Conditions and Memory Initialization" sections. ■ Applied new template. ■ Minor text edits.
March 2010	3.1	■ Updated the "Simple Dual-Port Mode", "Same-Port Read-During-Write Mode", and "Mixed-Port Read-During-Write Mode" sections. ■ Updated Figure 3–14. ■ Minor text edits.
November 2009	3.0	■ Updated Table 3–2. ■ Updated the "Simple Dual-Port Mode" section. ■ Minor text edits. ■ Updated graphics.
June 2009	2.3	■ Updated Table 3–1 and Figure 3–2. ■ Updated the "Introduction", "Byte Enable Support", "Mixed Width Support", "Asynchronous Clear", "Single-Port RAM", "Simple Dual-Port Mode", "True Dual-Port Mode", "FIFO Mode", and "Read/Write Clock Mode" sections. ■ Added introductory sentences to improve search ability. ■ Removed the Conclusion section. ■ Minor text edits.
April 2009	2.2	■ Updated Table 3–2.
March 2009	2.1	■ Updated Table 3–2. ■ Removed "Referenced Documents" section.
November 2008	2.0	Updated "Power-Up Conditions and Memory Initialization" on page 3–20
May 2008	1.0	Initial release.