3. Configuring Multiple Protocols and Data Rates in Stratix IV Devices

SIV52003-4.2

This chapter describes the procedure for merging; for example, when combining multiple protocols and data rates within a transceiver block. The instances you can combine include **Receiver Only** and **Transmitter and Receiver** channels as well as channels configured in Protocol Functional modes, channels using PLL cascade clocks, channels in multiple transceiver blocks, and channels with a Basic (PMA Direct) configuration. This chapter also offers several examples of sharing the clock multiplier unit phase-locked loops (CMU PLLs).

For information about the supported data rate range for the auxiliary transmit (ATX) PLL, refer to the "Transceiver Performance Specifications" section in the *DC and Switching Characteristics for Stratix IV Devices* chapter.

Overview

Each transceiver channel in a Stratix® IV GX and GT device can run at an independent data rate or in an independent protocol mode. Within each transceiver channel, the transmitter and receiver channels can run at different data rates. Each transceiver block consists of two CMU PLLs that provide clocks to all the transmitter channels within the transceiver block. Each receiver channel contains a dedicated clock data recovery (CDR) unit.

In addition to the CMU PLLs, the ATX PLLs are available to provide clocks to the transmitter channels that are configured for a specific data rate range.

This chapter includes the following sections:

Each transmitter channel has a local divider (/1, /2, or /4) that divides the high-speed clock output of the CMU PLL to provide high-speed serial and low-speed parallel clocks for its physical coding sublayer (PCS) and physical medium attachment (PMA) functional blocks.

You can configure the RX CDR present in the receiver channel to a distinct data rate and provide separate input reference clocks. Each receiver channel also contains a local divider that divides the high-speed clock output of the RX CDR and provides clocks for its PCS and PMA functional blocks. To enable transceiver channel settings, the Quartus® II software provides the ALTGX MegaWizard™ Plug-In Manager interface. The ALTGX MegaWizard Plug-In Manager allows you to instantiate a single transceiver channel or multiple transceiver channels in **Receiver and Transmitter**, **Receiver only**, and **Transmitter only** configurations.

Glossary of Terms

Table 3–1 lists the terms used in the chapter.

Table 3–1. Glossary of Terms Used in this Chapter

Configuration	Description
Regular Channels	This refers to the four transceiver channels in each transceiver block that contain PCS.
Basic (PMA Direct)	This refers to the Basic (PMA Direct) configuration that you can use for both regular and CMU channels. Basic (PMA Direct) mode has two variations, ×1 and ×N. The term "Basic (PMA Direct)" used in this chapter refers to both ×1 and ×N and to regular/CMU Channels. Any specific reference to ×1 and ×N or regular/CMU channels is stated explicitly.
Non-Basic (PMA Direct)	This term refers to all single channel non-bonded configurations (for example, GIGE, PCI Express® [PCIe] ×1) or bonded channel configurations that have PCS enabled (for example, Basic ×4 and ×8, XAUI, PCIe ×4 and ×8). Also, any reference to a channel in non-Basic (PMA Direct) mode indicates that the channel is a regular transceiver channel.
Basic (PMA Direct) ×1	A transceiver channel set up in this configuration uses the high-speed serial clock from the CMU PLL that is present within the same transceiver block. You can select this configuration by setting the **Which protocol you will be using?** option to **Basic (PMA Direct)** and the **Which sub protocol you will be using?** option to **none**.
Basic (PMA Direct) ×N	A transceiver channel set up in this configuration uses the ×N high-speed clock lines. You can select this configuration by setting the **Which protocol you will be using?** option to **Basic (PMA direct)** and the **Which sub protocol you will be using?** option to **×N**.

For more information about transceiver channel set up using a Basic (PMA Direct) ×N configuration, refer to the *Transceiver Clocking in Stratix IV Devices* chapter.

Creating Transceiver Channel Instances

The two ways you can instantiate multiple transceiver channels in the **General** screen of the ALTGX MegaWizard Plug-In Manager are:

- In the **What is the number of channels?** option, select the required value. This method creates all the transceiver channels with identical configurations. For an example, refer to "Combining Transceiver Instances in Multiple Transceiver Blocks" on page 3–13.
- In the **What is the number of channels?** option, select **1** and create a single channel transceiver instance. To instantiate additional transceiver channels with an identical configuration, select the created ALTGX instance multiple times. If you need additional transceiver channels with different configurations, create separate ALTGX megafunction instances with different settings and use them in your design.

When you create instances using the above methods, you can force the placement of up to four transceiver channels within the same transceiver block. Do this by assigning the `tx_dataout` and `rx_datain` ports of the channel instances to a single transceiver bank. If you do not assign pins to the `tx_dataout` and `rx_datain` ports, the Quartus II software chooses default pin assignments. When you compile the design, the Quartus II software combines multiple channel instances within the same transceiver block if the instances meet specific requirements. The following sections explain these requirements for different transceiver configurations.

General Requirements to Combine Channels

When you create multiple ALTGX instances, the Quartus II software requires that you to set identical values for the following parameters and signals to combine the ALTGX instances within the same transceiver block or in transceiver blocks on the same side of the device. The following sections describe these requirements.

Transmitter Buffer Voltage (V_{CCH})

The Stratix IV GX device provides you the option to select 1.4 V or 1.5 V for the V_{CCH} supply through the ALTGX MegaWizard Plug-In Manager. The Stratix IV GT device only allows 1.4 V for the V_{CCH} supply. To combine the channel instances within the same transceiver block, the Quartus II software requires that you to set the same V_{CCH} value in all the channel instances.

The data rate of the transmitter channel is limited based on the V_{CCH} value selected.

For the data rate restrictions, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

Transceiver Analog Power ($V_{CCA\_L/R}$)

The Stratix IV GX and GT device contains two different power supply pins, `VCCA_L` and `VCCA_R` that provide power to the PMA blocks in all the transceiver channels on the left and right sides of the device, respectively.

The Stratix IV GX and GT device provides you the option to select 2.5 V or 3.0 V for the VCCA_L/R supply through the ALTGX MegaWizard Plug-In Manager. The Stratix IV GT device only allows 3.3 V for the $V_{CCA\_L/R}$ supply. You must set the same VCCA_L/R value for all the transceiver channel instances to enable the Quartus II software to place them in the transceiver blocks on the same side of the device. For example, if you have two ALTGX instances that you would like to place on the left side transceiver banks GXBL0 and GXBL1, the VCCA_L/R values in the two ALTGX instances must be the same.

The data rate of the transceiver channel is limited based on the $V_{CCA\_L/R}$ value selected.

For the data rate restrictions, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

Control Signals

This section contains information about the gxb_powerdown, reconfig_fromgxb, and reconfig_togxb ports.

gxb_powerdown Port

The gxb_powerdown port is an optional port that you can enable in the ALTGX MegaWizard Plug-In Manager. If enabled, you must drive the gxb_powerdown port in the ALTGX instances from the same logic or the same input pin to enable the Quartus II software to assign them in the same transceiver block.

reconfig_fromgxb and reconfig_togxb Ports

In the ALTGX MegaWizard Plug-In Manager, the reconfig_fromgxb and reconfig_togxb ports are enabled if you select one of the following options in the **Reconfig** screen:

- Analog Controls (VOD, Pre-emphasis, Manual Equalization, and EyeQ)
- Enable Channel and Transmitter PLL reconfiguration
- Offset cancellation for receiver channels (always enabled if the configuration is **Transmitter and Receiver** or **Receiver only**)

To combine multiple instances within the same transceiver block:

- The reconfig_fromgxb ports must be enabled in each instance AND
- These ports must be connected to the same reconfig controller

For example, consider that you want to place a **Receiver only** and **Transmitter only** instance in the same transceiver block. For the **Receiver only** instance, the Quartus II software automatically enables the reconfig_fromgxb port. For the **Transmitter only** instance, you must select the options in the **Reconfig** screen (mentioned above) to enable the reconfig_fromgxb port. In the design, connect these ports from the **Transmitter only** and **Receiver only** instance to the same reconfig controller.

For more information about connecting these ports to the dynamic reconfiguration controller, refer to the "Connecting the ALTGX and ALTGX_RECONFIG Instances" section of the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Calibration Clock and Power Down

Each calibration block in a Stratix IV GX and GT device is shared by multiple transceiver blocks.

If your design uses multiple transceiver blocks, depending on the transceiver banks selected, you must connect the `cal_blk_clk` and `cal_blk_powerdown` ports of all channel instances to the same input pin or logic.

For more information about the calibration block and transceiver banks that are connected to a specific calibration block, refer to the "Calibration Blocks" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Asserting the `cal_blk_powerdown` port affects calibration on all transceiver channels connected to the calibration block.

Sharing CMU PLLs

When you create multiple transceiver channel instances using CMU PLLs and intend to combine these instances in the same transceiver block, the Quartus II software checks whether a single CMU PLL can be used to provide clock outputs for the transmitter side of the channel instances. If a single CMU PLL is not sufficient, the Quartus II software attempts to combine the channel instances using two CMU PLLs. Otherwise, the Quartus II software issues a Fitter error.

The following two sections describes the ALTGX instance requirements to enable the Quartus II software to share the CMU PLL.

Multiple Channels Sharing a CMU PLL

To enable the Quartus II software to share the same CMU PLL for multiple channels, the following parameters in the channel instantiations must be identical:

- "Base data rate" (the CMU PLL is configured for this data rate)
- CMU PLL bandwidth setting
- Reference clock frequency
- Input reference clock pin
- `pll_powerdown` port of the ALTGX instances must be driven from the same logic
- `GXB_TX_PLL_Reconfig_Group` assignment (refer to Table 3–14 on page 3–42)
- If the selected functional mode in one instance is (OIF) CEI Phy Interface or PCIe, the other instance must have the same functional mode to share the CMU PLL. For example, if you have two channels, one configured in Basic mode and the other configured in (OIF) CEI Phy Interface mode at the same data rate, the Quartus II software does not share the same PLL because the internal parameters for these two functional modes are different.

Each channel instance can have a different local divider setting. This is a useful option when you intend to run each channel within the transceiver block at different data rates that are derived from the same base data rate using the local divider values /1, /2, and /4. Example 1 shows this design configuration.

Example 1

Consider an example design with four instances of a **Receiver and Transmitter** configuration in the same transceiver block at various serial data rates. Assume that each instance contains a channel and is driven from the same clock source and has the same CMU PLL bandwidth settings. Table 3–2 lists the configuration for Example 1.

Table 3–2. Configuration for Example 1

User-Created Instance Name	ALTGX MegaWizard Plug-In Manager Settings		
	Number of Channels	Configuration	Effective Data Rate (Gbps)
inst0	1	Receiver and Transmitter	4.25
inst1	1	Receiver and Transmitter	2.125
inst2	1	Receiver and Transmitter	1.0625
inst3	1	Receiver and Transmitter	4.25

For Example 1, you can share a single CMU PLL for all four channels because:

- One CMU PLL can be configured to run at 4.25 Gbps.
- Each channel can divide the CMU PLL clock output using the local divider and achieve the required data rates of 4.25 Gbps, 2.125 Gbps, and 1.0625 Gbps. Because each receiver channel has a dedicated CDR, the receiver side in each instance can be set up for these three data rates without any restrictions.

To enable the Quartus II software to share a single CMU PLL for all four channels, set the values listed in Table 3–3 in the **General** screen of the ALTGX MegaWizard Plug-In Manager.

Table 3–3. ALTGX MegaWizard Plug-In Manager Settings for Example 1

Instance	General Screen Option	Setting (Gbps)
inst0	What is the effective data rate?	4.25
	Specify base data rate	4.25 (1)
inst1	What is the effective data rate?	2.125
	Specify base data rate	4.25 (1)
inst2	What is the effective data rate?	1.0625
	Specify base data rate	4.25 (1)

Table 3–3. ALTGX MegaWizard Plug-In Manager Settings for Example 1

Instance	General Screen Option	Setting (Gbps)
inst3	**What is the effective data rate?**	4.25
	Specify base data rate	4.25 (1)

Note to Table 3–3:

(1) The **Specify base data rate** option is 4.25 Gbps for all four instances. Given that the CMU PLL bandwidth setting and input reference clock are the same and that the `pll_powerdown` ports are driven from the same logic or pin, the Quartus II software shares a single CMU PLL that runs at 4.25 Gbps.

You can force the placement of the transceiver channels to a specific transceiver block by assigning pins to `tx_dataout` and `rx_datain`. Otherwise, the Quartus II software selects a transceiver bank.

Figure 3–1 and Figure 3–2 show the scenario before and after the Quartus II software combines the transceiver channel instances. Because the RX CDR is not shared between channels, only the CMU PLL is shown.

Each of the ALTGX instances has a `pll_powerdown` port. You must drive the `pll_powerdown` ports for all the instances from the same logic to enable the Quartus II software to share the same CMU PLL.

Figure 3–1. ALTGX Instances Before Compilation for Example 1

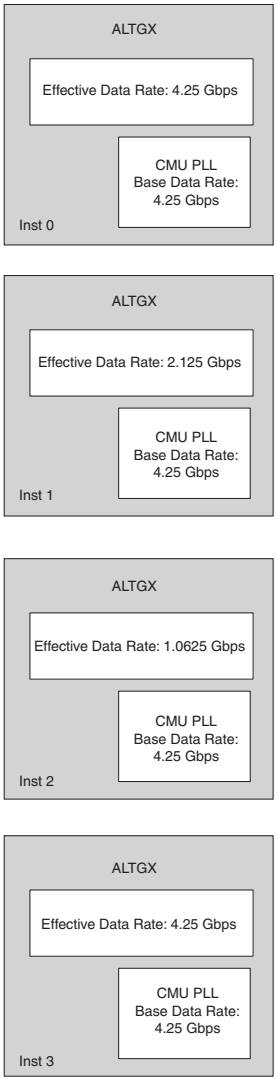
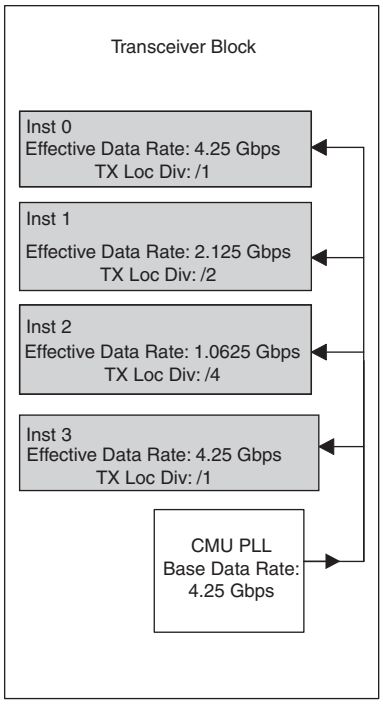


Figure 3–2 shows the scenario after the Quartus II software combines the transceiver channel instances.

Figure 3–2. Combined Instances after Compilation for Example 1



Example 2

Consider the example design listed in Table 3–4. When you have two instances with the same serial data rate but with different CMU PLL data rates, the Quartus II software creates a separate CMU PLL for the two instances.

Table 3–4. Configuration for Example 2

User-Created Instance Name	ALTGX MegaWizard Plug-In Manager Settings			
	Number of Channels	Configuration	Effective Data Rate (Gbps)	Base Data Rate (Gbps)
inst0	1	Receiver and Transmitter	2.5	2.5
inst1	1	Receiver and Transmitter	2.5	5
inst2	1	Receiver and Transmitter	1	1

Even though the effective data rate of inst1 is 2.5 Gbps (5 Gbps/2 = 2.5 Gbps), the same as inst0, when you compile the design, the Quartus II software requires two CMU PLLs to provide clocks for the transmitter side of the two instances because their base data rates are different. In this example, you have the third instance, inst2, that requires a third CMU PLL. Therefore, the Quartus II software cannot combine the above three instances within the same transceiver block.

Sharing ATX PLLs

The Quartus II software allows you to share the same ATX PLL for multiple transceiver instances if the following requirements are met:

- The ATX PLL bandwidth in both instances are the same
- If the selected functional mode in one instance is (OIF) CEI Phy Interface or PCIe, the other functional modes must be the same to share the ATX PLL. For example, if you have two channels, one configured in Basic mode and the other configured in (OIF) CEI Phy Interface mode at the same data rate, the Quartus II software does not share the same PLL because the internal parameters for these two functional modes are different.
- The base data rate and effective data rate values are the same.
- The `pll_powerdown` port in the instances are connected to the same logic.
- The instances are placed on the same side of the device.
- There is no contention on the ×N clock lines from the ATX PLL and the two instances.

For more information about ×N clocking, refer to the "Transmitter Channel Data Path Clocking" section in the *Transceiver Clocking in Stratix IV Devices* chapter.

Combining Receiver Only Channels

You can selectively use the receiver in the transceiver channel by selecting the **Receiver only** configuration in the **What is the Operating Mode?** option on the **General** screen of the ALTGX MegaWizard Plug-In Manager.

You can combine **Receiver only** channel instances of different configurations and data rates into the same transceiver block. Because each receiver channel contains its own dedicated CDR, each **Receiver only** instance (assuming one receiver channel per instance) can have a different data rate.

For the Quartus II software to combine the **Receiver only** instances within the same transceiver block, you must connect `gxb_powerdown` (if used) for all the channel instances to the same logic or input pin. For more information, refer to "General Requirements to Combine Channels" on page 3–3.

If your design contains a **Receiver only** instance, the Quartus II software disables all the settings for the unused transmitter channel present in the same physical transceiver channel. Therefore, the unused transmitter channel is always powered down in the hardware.

Combining Transmitter Channel and Receiver Channel Instances

You can create separate transmitter and receiver channel instances and assign the `tx_dataout` and `rx_datain` pins of the transmitter and receiver instances, respectively, to the same physical transceiver channel. This configuration is useful when you intend to run the transmitter and receiver channel at different serial data rates. To create separate transmitter and receiver channel instances, select the **Transmitter only** and **Receiver only** options in the operating mode (**General** screen) of the ALTGX MegaWizard Plug-In Manager.

Multiple Transmitter Channel and Receiver Channel Instances

The Quartus II software allows you to combine multiple **Transmitter only** and **Receiver only** channel instances within the same transceiver block. Based on the pin assignments, the Quartus II software combines the corresponding **Transmitter only** and **Receiver only** channels in the same physical channel. To enable the Quartus II software to combine the transmitter channel and receiver channel instances in the same transceiver block, follow the rules and requirements outlined in:

- "General Requirements to Combine Channels" on page 3–3
- "Multiple Channels Sharing a CMU PLL" on page 3–5
- "Combining Receiver Only Channels" on page 3–10

Example 3

Consider the example design listed in Table 3–5 with four ALTGX instances.

Table 3–5. Four ALTGX Instances for Example 3

Instance Name	Configuration	Serial Data Rate (Gbps)	Input Reference Clock Frequency (MHz)
`inst0`	**Transmitter only**	3.125	156.25
`inst1`	**Receiver only**	2.5	156.25
`inst2`	**Transmitter only**	1.25	125
`inst3`	**Receiver only**	2	125

After you create the above instances, if you force the placement of the instances, as listed in Table 3–6, the Quartus II software combines `inst0` and `inst1` to physical channel 0, and `inst2` and `inst3` to physical channel 1.

Table 3–6. Forced Placement of the Instances for Example 3

Instance Name	Physical Channel Pin Assignments in the Same Transceiver Block
`inst0`	TX pin of channel 0
`inst1`	RX pin of channel 0
`inst2`	TX pin of channel 1
`inst3`	RX pin of channel 1

Figure 3–3 and Figure 3–4 show the transceiver channel instances before and after compilation.

Figure 3–3. ALTGX Transceiver Channel Instances Before Compilation for Example 3

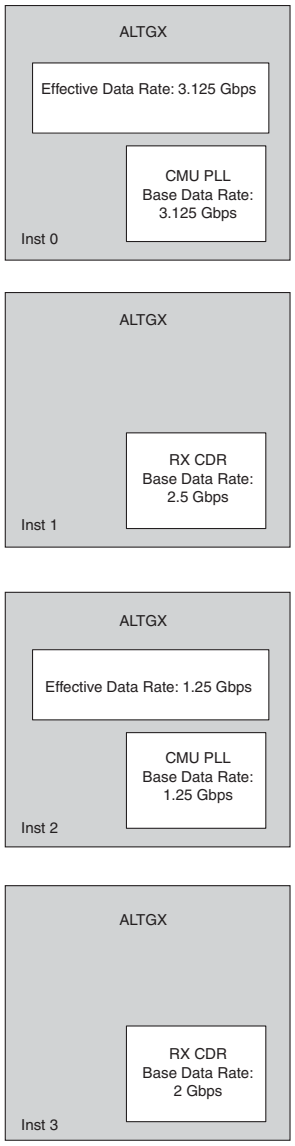
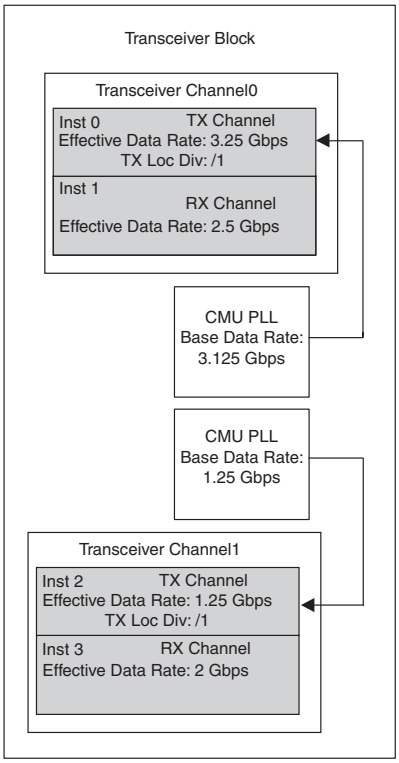


Figure 3–4 shows the transceiver channel instances after compilation.

Figure 3–4. Combined Transceiver Instances After Compilation for Example 3



Combining Transceiver Instances in Multiple Transceiver Blocks

The method to instantiate multiple transceiver channels using a single ALTGX instance is described in "Creating Transceiver Channel Instances" on page 3–3. The following section describes the method to instantiate multiple transceiver channels using multiple transceiver blocks.

When you create a transceiver instance that has more than four transceiver channels (assuming that the instance is created in non-Basic (PMA Direct) functional mode which requires regular channels), the Quartus II software attempts to combine the transceiver channels in multiple transceiver blocks. This is shown in the following examples.

Example 4

Consider the design example configuration listed in Table 3–7 with two ALTGX instances.

Table 3–7. Two ALTGX Instances for Example 4

Instance Name	Number of Transceiver Channels	Configuration	Serial Data Rate (Gbps)	Input Reference Clock (MHz)
inst0	7	Receiver and Transmitter	4.25	125 from refclk0
inst1	1	Receiver and Transmitter	4.25	125 from refclk0 (same as inst0)

In this case, assuming that all the required parameters specified in "Multiple Channels Sharing a CMU PLL" on page 3–5 are identical for inst0 and inst1, the Quartus II software fits inst0 and inst1 in two transceiver blocks.

Figure 3–5 and Figure 3–6 show the transceiver instances before and after compilation.

Figure 3–5. Transceiver Channel Instances Before Compilation for Example 4

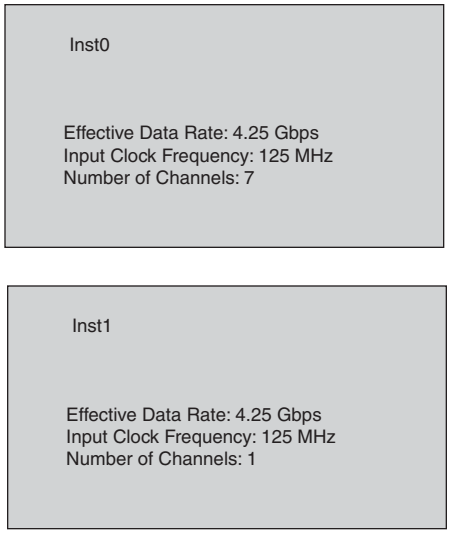
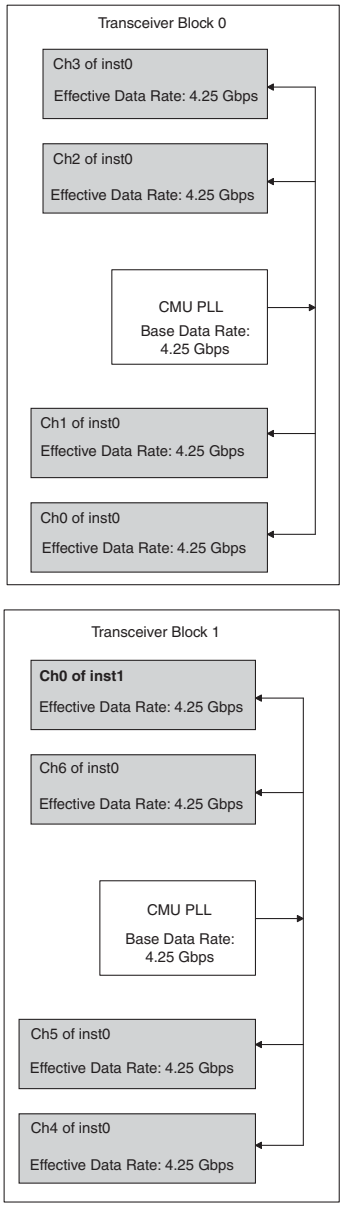


Figure 3–6 shows the transceiver instances after compilation.

Figure 3–6. Combined Transceiver Instances After Compilation for Example 4



You can force the placement of the transceiver channels in specific transceiver banks by assigning pins to the `tx_dataout` and `rx_datain` ports of `inst0` and `inst1`.

Even though `inst0` instantiates seven transceiver channels, the ALTGX MegaWizard Plug-In Manager provides only a one-bit wide `pll_inclk` port for `inst0`. In your design, provide only one clock input for the `pll_inclk` port. The Quartus II software uses two transceiver blocks to fit the seven channels and internally connects the input reference clock (connected to the `pll_inclk` port in your design) to the CMU PLLs of two transceiver blocks.

For inst1, the ALTGX MegaWizard Plug-In Manager provides a pll_inclk port. In this example, it is assumed that a single reference clock is provided for inst0 and inst1. Therefore, connect the pll_inclk port of inst0 and inst1 to the same input reference clock pin. This enables the Quartus II software to share a single CMU PLL in transceiver block 1 that has three channels of inst0 and one channel of inst1 (shown as ch4, ch5, and ch6 in transceiver block 1 in Figure 3–6).

For the RX CDRs in inst0, the ALTGX MegaWizard Plug-In Manager provides seven bits for the rx_cruclk port (if you do not select the **Train Receiver CDR from pll_inclk** option in the **PLL/Ports** screen). This allows separate input reference clocks to the RX CDRs of each channel.

Combining Transceiver Instances Using PLL Cascade Clocks

The Stratix IV GX and GT transceiver has the ability to cascade the output of the general purpose PLLs (PLL_L and PLL_R) to the CMU PLLs, ATX PLLs, and receiver CDRs. The left side PLLs can only be cascaded with the transceivers on the left side of the device. Similarly, the right side PLLs can only be cascaded with the transceivers on the right side of the device. Each side of the Stratix IV GX and GT device contains a PLL cascade clock network; a single line network that connects the PLL cascade clock to the transceiver block. This clock line is segmented to allow different PLL cascade clocks to drive the transceiver CMU PLLs, ATX PLLs, and RX CDRs. Within the same segment, only a single PLL_L/PLL_R can drive these transceiver PLLs/CDRs. Therefore, if you create two instances that use different PLLs for cascading, you cannot place these instances within the transceiver block.

The segmentation locations differ based on the device family.

For more information about using the PLL cascade clock and segmentation, refer to the "Dedicated Left and Right PLL Cascade Lines Network" section in the *Transceiver Clocking in Stratix IV Devices* chapter.

Combining Channels Configured in Protocol Functional Modes

This section describes how to combine channels for various protocol functional modes.

Combining Channels in Bonded Functional Modes

This section describes the combination requirements in the two variations of bonded functional modes using transceiver PCS blocks. The two bonded functional modes are:

- "Bonded ×4 Functional Mode"—Examples of bonded ×4 mode:
  - Basic mode with the sub protocol set to ×4
  - XAUI
  - PCIe mode with the sub protocol set to Gen1 ×4 or Gen2 ×4.
- "Bonded x8 Functional Mode" on page 3–20—Examples of bonded ×8 mode:
  - Basic mode with the sub protocol ×8
  - PCIe mode with the sub protocol ×8

Bonded ×4 Functional Mode

The combination requirements for Basic x4, Deterministic Latency ×4, and PCIe x4 functional modes (if you do not use the PCIe hard IP block) are similar.

In this mode, the transmitter channels are synchronized to reduce skew. The Quartus II software shares the control from physical transmitter channel 0 with the other transmitter channels in the transceiver block. Therefore, when you an create an instance in this mode, the logical transmit channel 0 (`tx_dataout[0]` in the instance) must be assigned by the physical channel location 0 in the transceiver block.

The central clock divider block in the `CMU0` channel forwards the high-speed serial and low-speed parallel clocks to the transmitter channels.

This clocking scheme is described in the "Bonded Channel Configurations" section of the *Transceiver Clocking in Stratix IV Devices* chapter.

Because you used the central clock divider, the are two restrictions on the channel combinations:

1. If you configure channels in bonded ×4 functional mode, the remaining transmitter channels (regular or CMU channels) within the transceiver block can be used only in Basic (PMA Direct) ×1 or ×N mode.

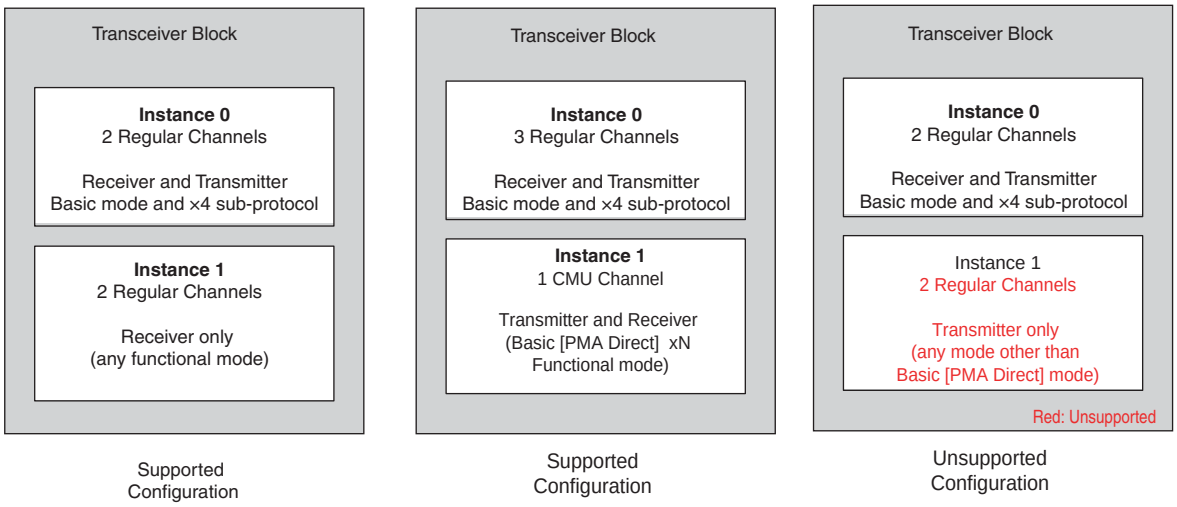
   

   If PCIe functional mode uses the PCIe hard IP block, the combination requirements are different. For more information, refer to "Combining Channels Using the PCIe hard IP Block with Other Channels" on page 3–24.

   The receiver channels are clocked independently. Therefore, you can configure the unused receiver channels within a transceiver block in any allowed configuration.

Figure 3–7 shows examples of supported and unsupported combinations.

Figure 3–7. Examples of Supported and Unsupported Configurations to Combine Instances in Basic ×4 Mode



The CMU0 PLL or CMU1 PLL can drive the central clock divider block in the CMU0 channel. In cases where you use CMU1 PLL for bonded ×4 mode, the Quartus II software does not allow you to use CMU0 PLL for any other configuration because part of the CMU0 channel (the central clock divider) is already used by the bonded ×4 functional mode.

Using the remaining channels in Basic (PMA Direct) ×1 or ×N mode depends on the following conditions.

1. If CMU1 PLL is available for clock generation, you can use the remaining transmitter channels in the transceiver block in Basic (PMA Direct) ×1 configuration.
2. If you want to configure the remaining transmitter channels at the same data rate as the bonded ×4 functional mode, you can configure the remaining transmitter channels in Basic (PMA Direct) ×1 mode. The requirements are specified in "Sharing CMU PLLs" on page 3–5 and "General Requirements to Combine Channels" on page 3–3.
3. If all the regular channels are configured in bonded ×4 functional mode, you can configure the transmitter side of the CMU0 channel in Basic (PMA Direct) ×N mode in single-width configuration only (double-width configuration is not supported). You can use the CMU1 channel in Basic (PMA Direct) ×N single-width or double-width configuration.

This only applies to the transmitter side and not the receiver side of the CMU channel.

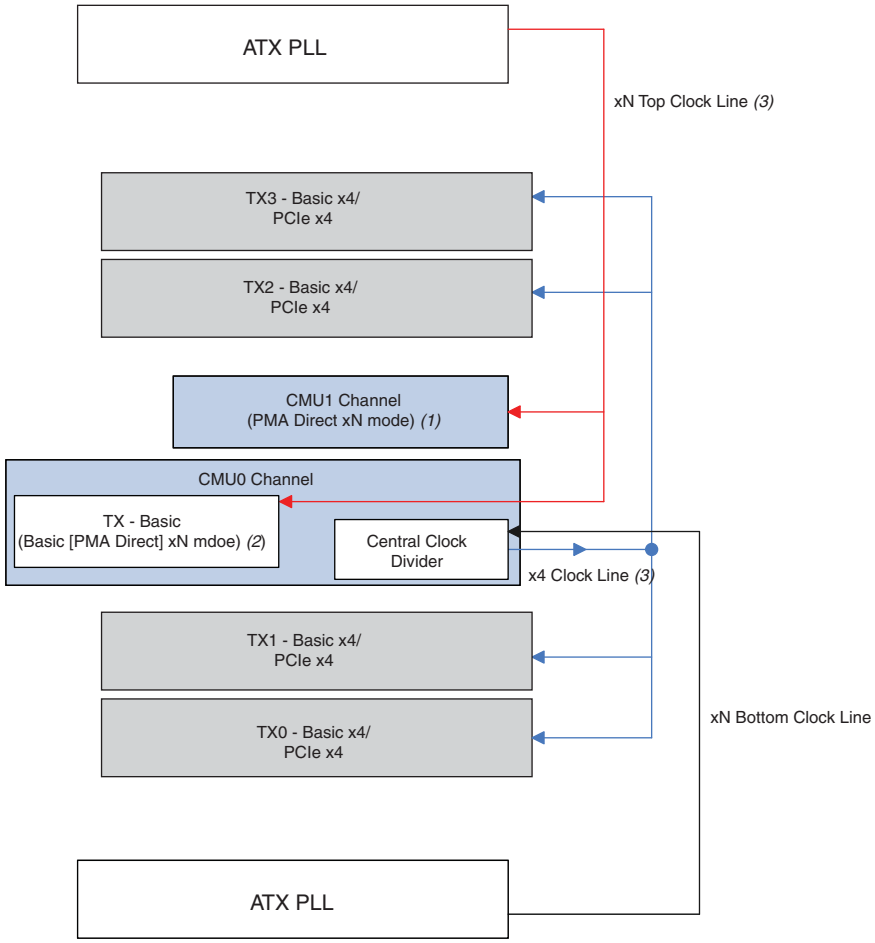
4. Using the receiver side of the CMU channels depends on whether you use `CMU1` PLL or `CMU0` PLL to generate clocks for the bonded ×4 functional mode. If the CMU PLL within the corresponding CMU channel is not available to perform CDR functionality, you cannot configure it as a receiver.
5. If you use ATX PLL to generate clocks for the ×4 bonded functional mode, you can use both the Transmitter and Receiver side of the `CMU0` and `CMU1` channels. You must satisfy the requirements specified in number 3.

Figure 3–8 shows a configuration in which all the transmitter channels in the transceiver block are used.

For XAUI, the option to select ATX PLL is not available.

Figure 3–8 shows the combination of Basic/PCIe x4 functional mode with Basic (PMA Direct) xN mode within the same transceiver block.

Figure 3–8. Basic ×4 Functional Mode Configuration when Combining Channels (4)



Notes to Figure 3–8:

(1) You can configure this channel in Basic (PMA Direct) single-width or double-width mode.
(2) You can configure this channel only in Basic (PMA Direct) single-width mode.
(3) The red lines represent the ×N top clock line, the blue lines represent the ×4 clock line, and the black line represents the ×N bottom clock line.
(4) To simplify the illustration, only the transmitter side is shown. PCIe ×4 refers to PCIe with the sub protocol set to **Gen1 x4** and **Gen2 x4**.

Bonded x8 Functional Mode

Bonded ×8 functional mode is similar to bonded ×4 functional mode except that the controls are shared from the physical channel 0 of the master transceiver block. The master is the lower of the two adjacent transceiver blocks selected for the ×8 configuration. Therefore, when you an create an instance in this mode, you must assign the logical transmit channel 0 (`tx_dataout[0]` in the instance to the physical channel location 0 in the master transceiver block.

There are specific transceiver blocks that can be paired as master-slave in the ×8 configuration.

The master is the adjacent lower transceiver block. For more information about location requirements, refer to the "Bonded Channel Configurations" section of the *Transceiver Clocking in Stratix IV Devices* chapter.

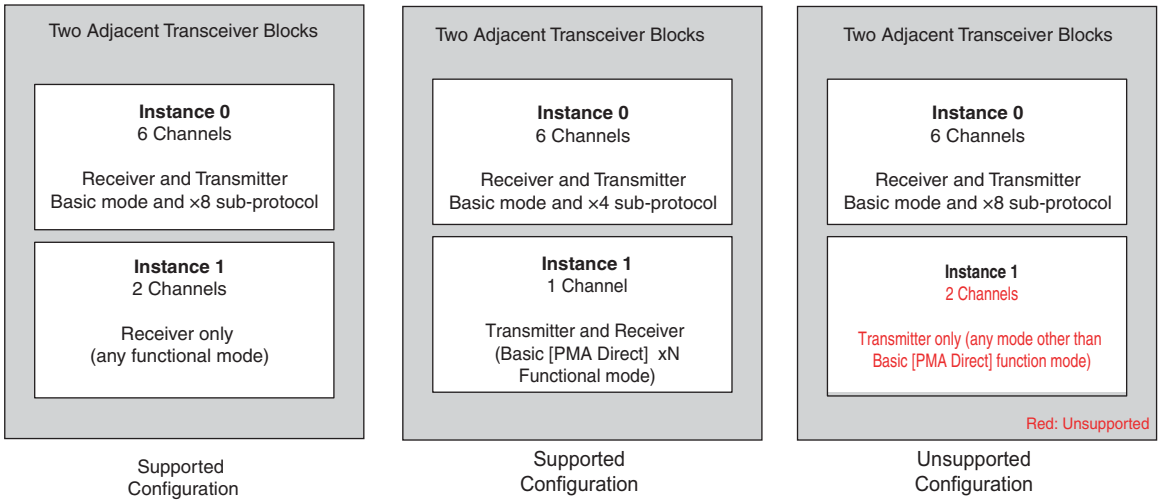
In Basic ×8 functional mode, you can select the number of channels to be less than 8 by setting the **What is the number of channels?** option on the **General** screen. In this instance, you can use the remaining transmitter channels only in Basic (PMA Direct) ×1 or ×N mode. In PCIe Gen1 ×8 and Gen2 ×8 functional modes, the number of regular channels used is always 8.

The number of remaining transmitter channels (CMU channels or regular channels) in the two transceiver blocks available for use in Basic (PMA Direct) ×1 or ×N mode depends on whether the ×8 functional mode uses CMU PLL or ATX PLL, as described below.

If PCIe functional mode uses the PCIe hard IP block, the combination requirements are different. For more information, refer to "Combining Channels Using the PCIe hard IP Block with Other Channels" on page 3–24.

Each receiver channel configured in Basic ×8 functional mode is clocked independently by the recovered clock from its receiver CDR. You can use the available receiver channels in any configuration. Figure 3–9 shows examples of supported and unsupported configuration in Basic ×8 mode.

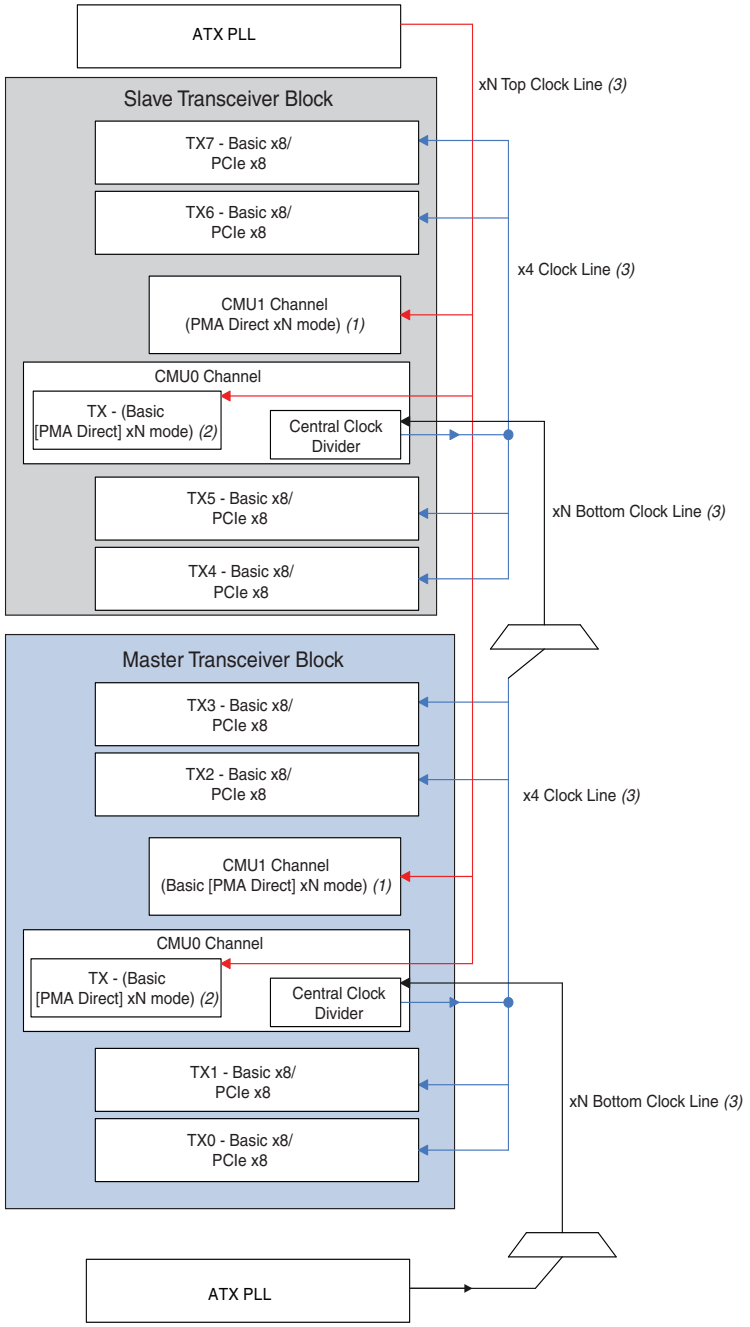
Figure 3–9. Examples of Supported and Unsupported Configurations to Combine Instances in Basic ×8 Mode



When the eight regular channels are used up in bonded ×8 functional mode:

- If the ATX PLL is used to generate clocks for the ×8 functional mode shown in Figure 3–10, you can use the four CMU channels (two from the master and slave transceiver block) in Basic (PMA Direct) ×N mode. Within Basic (PMA Direct) ×N mode, you can configure the `CMU0` channels in the master and slave transceiver block only in single-width mode (use the **single-width mode** option in the **General** screen). If a `CMU1` channel or regular channels are available for use, you can use them in Basic (PMA Direct) ×N mode in single-width or double-width configuration.

Figure 3–10. Basic ×8/PCIe ×8 Functional Mode Configuration when Combining Channels (ATX PLL) (4)



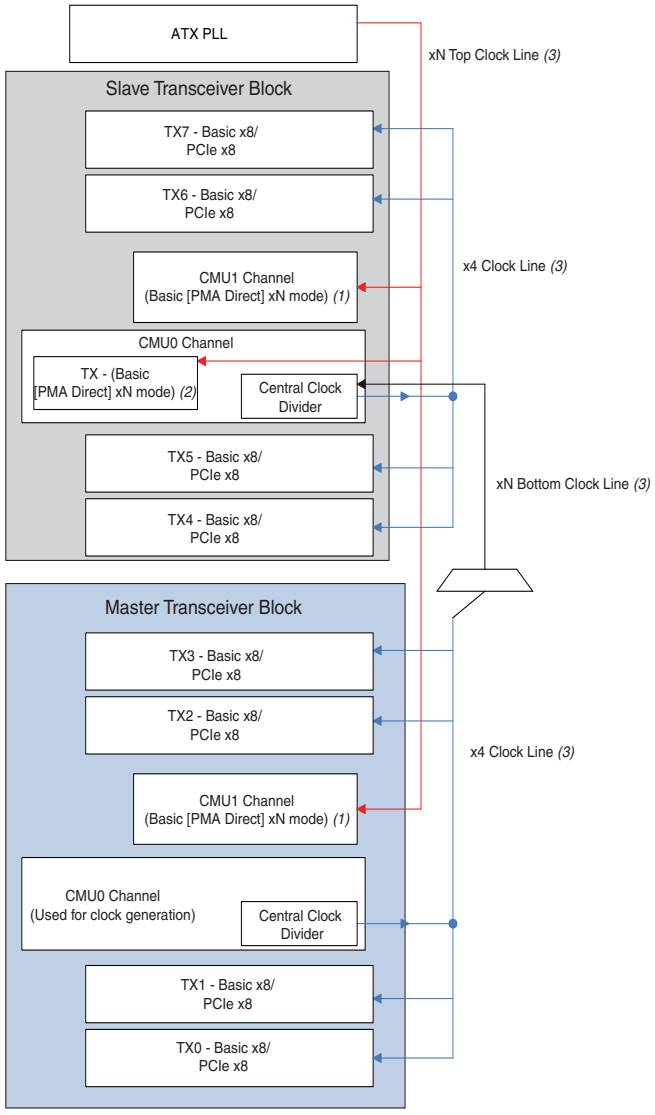
Notes to Figure 3–10:

(1) You can configure this channel in Basic (PMA Direct) single-width or double-width mode.
(2) You can configure this channel only in Basic (PMA Direct) single-width mode.
(3) The red lines represent the ×N top clock line, the blue lines represent the ×4 clock line, and the black line represents the ×N bottom clock line.
(4) To simplify the illustration, only the transmitter side is shown. PCIe ×8 refers to PCIe with the sub protocol set to **Gen1 ×8** and **Gen2 ×8**.

- If the CMU PLL is used to generate clocks for the ×8 bonded functional mode, you can use the `CMU0` channel in the slave transceiver block only in Basic (PMA Direct) ×N mode in the single-width configuration. You can use the `CMU1` channels in both the master and slave transceiver blocks in Basic (PMA Direct) ×N mode in single-width or double-width configuration.

Figure 3–11 shows the Basic ×8 functional mode configuration for these combination restrictions when using CMU PLL.

Figure 3–11. Basic ×8/PCIe ×8 Functional Mode Configuration when Combining Channels (CMU PLL) (4)



Notes to Figure 3–11:

(1) You can configure this channel in Basic (PMA Direct) single-width or double-width mode.
(2) You can configure this channel only in Basic (PMA Direct) single-width mode.
(3) The red lines represent the ×N top clock line, the blue lines represent the ×4 clock line, and the black line represents the ×N bottom clock line.
(4) To simplify the illustration, only the transmitter side is shown. PCIe ×8 refers to PCIe with the sub protocol set to **Gen1 ×8** and **Gen2 ×8**.

Combining Channels Configured in Deterministic Latency Mode

The ALTGX MegaWizard Plug-In Manager provides Deterministic Latency mode with two variations (×1 and ×4) to eliminate uncertainty in the transceiver data path. This functional mode provides the **Enable Phase Frequency Detector (PFD) feed back …** option in the **PLL/Ports** screen. If you select this option for ×1, the low-speed parallel clock from the transmitter serializer is fed back to the PFD input of the CMU PLL; for ×4, the output of the low-speed parallel clock from the central clock divider is provided as feed back.

For the ×1 variation, one CMU PLL is required for each transmitter channel in the instance. As a result, in ×1 mode, you can configure only two channels within the transceiver block in this mode. The restrictions for Deterministic Latency mode in ×4 mode are the same as that of the bonded x4 functional mode. For more information, refer to "Bonded ×4 Functional Mode" on page 3–17.

Combining Channels Using the PCIe hard IP Block with Other Channels

The Stratix IV GX and GT device contains an embedded PCIe hard IP block that performs the phyMAC, datalink, and transaction layer functionality specified by PCIe base specification 2.0. Each PCIe hard IP block is shared by two transceiver blocks. The **PCI Express Compiler Wizard** provides you the options to configure the PCIe hard IP block. When enabled, the transceiver channels associated with this block are also enabled.

There are restrictions on combining transceiver channels with different functional and/or protocol modes (for example, Basic mode) within two contiguous transceiver blocks with the channels that use the PCIe hard IP block. The restrictions depend on the number of channels used (×1 or ×4) and the number of virtual channels (VCs) selected in the PCI Express Compiler MegaWizard Plug-In Manager. Table 3–8 lists the restrictions.

When you use the PCIe hard IP block, there are placement restrictions on the locations of the transceiver channels.

For these channel placement restrictions, refer to the *PCI Express Compiler User Guide*.

Table 3–8. PCIe Hard IP Block Restrictions When Combining Transceiver Channels with Different Functional and/or Protocol Modes (Part 1 of 2) (1), (2), (7)

PCIe Configuration (PCIe hard IP Options Enabled in the PCI Express Compiler MegaWizard Plug-In Manager) (3)			Transceiver Block 0 (4)				Transceiver Block 1 (5)			
Link Width	Lane (Data Interface Width)	Virtual Channel (VC)	Ch0 (6)	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7
×1	64-bit	1	PCIe ×1	Avail.	Avail.	Avail.	Avail.	Avail.	Avail.	Avail.
		2	PCIe ×1	—	—	—	Avail.	Avail.	Avail.	Avail.
×4	64-bit	1	PCIe ×4				Avail.	Avail.	Avail.	Avail.
		2	PCIe ×4				Avail.	Avail.	Avail.	Avail.

Table 3–8. PCIe Hard IP Block Restrictions When Combining Transceiver Channels with Different Functional and/or Protocol Modes (Part 2 of 2) (1), (2), (7)

PCIe Configuration (PCIe hard IP Options Enabled in the PCI Express Compiler MegaWizard Plug-In Manager) (3)			Transceiver Block 0 (4)				Transceiver Block 1 (5)			
Link Width	Lane (Data Interface Width)	Virtual Channel (VC)	Ch0 (6)	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7
×4	128-bit	1	PCIe ×4				Avail.	Avail.	Avail.	Avail.
		2	PCIe ×4				—	—	Avail.	Avail.
×8	—	—	PCIe ×8							

Notes to Table 3–8:

(1) Avail. indicates that the channels can be used in other configurations.

(2) An em-dash (—) indicates that the channels are NOT available for use.

(3) The CMU PLL is used for the transmitter side of the channels in this table.

(4) Transceiver block 0—the master transceiver block that provides high-speed serial and low-speed parallel clocks in a PCIe ×4 or ×8 configuration.

(5) Transceiver block 1—the adjacent transceiver block that shares the same PCIe hard IP block with transceiver block 0.

(6) The physical channel 0 in the transceiver block. For more information about physical-to-logical channel mapping in PCIe functional mode, refer to the "×8 Channel Configuration" section in the *Transceiver Clocking in Stratix IV Devices* chapter.

(7) When you the use PCIe hard IP Block, you cannot configure the CMU channels within the transceiver block as transceiver channels.

For more information about the *PCI Express Compiler MegaCore functions* and hard IP implementation, refer to the *PCI Express Compiler User Guide.*

If you configure a transceiver channel in PCIe configuration and if an ATX PLL is used to provide clocks for the transmitter side of the channel, you can use the remaining transmitter channels within the same transceiver block only in Basic (PMA Direct) ×1 or ×N mode.

Combining Transceiver Channels in Basic (PMA Direct) Configurations

In this configuration, the transmitter and receiver PCS blocks of a transceiver channel are bypassed and the transceiver channel can run at a maximum of 6.5 Gbps.

For the data rate restrictions in Basic (PMA Direct) mode, refer to the "Transceiver Performance Specifications" section in the *DC and Switching Characteristics for Stratix IV Devices* chapter.

Using the Quartus II software, you can configure the two CMU channels and regular transceiver channels in Basic (PMA Direct) mode. The following sections describes the different scenarios for combining Basic (PMA Direct) mode with other transceiver configurations.

For information about the FPGA fabric-transceiver interface, refer to the "Non-Bonded Basic (PMA Direct) Mode Channel Configurations" section in the *Transceiver Clocking in Stratix IV Devices* chapter.

Combining Multiple Channels Configured in Basic (PMA Direct) ×1 Configurations

When you configure a transceiver channel in Basic (PMA Direct) ×1 configuration, the Quartus II software requires one of the two CMU PLLs within the same transceiver block to provide high-speed clocks to the transmitter side of the channel (you cannot use the ATX PLL). Therefore, within a transceiver block, you can only combine a maximum of five transceiver channels (using both the Transmitter and Receiver) configured in Basic (PMA Direct) ×1 mode (one CMU channel to perform the clock multiplication unit functionality).

You can configure the transmitter side of the CMU channel that uses its CMU PLL for clock generation in Basic (PMA Direct) x1 in single-width or double-width configuration, as shown in Figure 3–17 on page 3–32.

There are multiple ways you can combine channels in Basic (PMA Direct) ×1 mode within the same transceiver block:

- "Multiple Basic (PMA Direct) ×1 Configuration Instances with One Channel per Instance" on page 3–26
- "One Instance in a Basic (PMA Direct) ×1 Configuration with Multiple Transceiver Channels" on page 3–26
- "Combining Multiple Instances of Transmitter Only and Receiver Only Configurations in Basic (PMA Direct) ×1 Mode" on page 3–29
- "Combining Channels Configured in Basic (PMA Direct) ×1 with Non-Basic (PMA Direct) Modes" on page 3–29

Multiple Basic (PMA Direct) ×1 Configuration Instances with One Channel per Instance

If you create multiple instances of Basic (PMA Direct) ×1 with one channel per instance, you can combine them within the same transceiver block. To achieve this combination, refer to the requirements specified in "Multiple Channels Sharing a CMU PLL" on page 3–5 and "General Requirements to Combine Channels" on page 3–3. Note that one CMU PLL within the transceiver block must provide a high-speed clock for the transmitter side of the channels. Therefore, at least one CMU channel (that contains the CMU PLL) within the transceiver block must be available to generate high-speed serial and low-speed parallel clocks for the channels configured in this mode. You can also place the individual instances in this configuration in separate transceiver blocks. For this placement, the Quartus II software enables one CMU PLL per instance.

One Instance in a Basic (PMA Direct) ×1 Configuration with Multiple Transceiver Channels

In this case, if the number of channels selected in the instance is less than six, the Quartus II software, by default, combines these channels within the same transceiver block and uses one CMU PLL to provide the high-speed clocks. If the number of channels is six or more, the Quartus II software requires two transceiver blocks and two CMU PLLs, one from each transceiver block.

The following two examples show the combinations of channels under two different conditions.

Example 5

Consider a design example configuration with a Basic (PMA Direct) ×1 instance with the number of channels set to 7 in the ALTGX MegaWizard Plug-In Manager. With this setting, the ALTGX MegaWizard Plug-In Manager provides 7 bits of `gxb_powerdown`, `rx_analogreset`, and `pll_powerdown` ports.

In this case, the Quartus II software attempts to combine the five channels in the instance to one transceiver block and the remaining two channels to the second transceiver block, assuming that the `gxb_powerdown` and `pll_powerdown` ports for the five channels are driven from the same logic. Figure 3–12 and Figure 3–13 show the conditions before and after compilation.

Figure 3–12. Logical View of the Instance with Seven Channels Before Compilation for Example 5

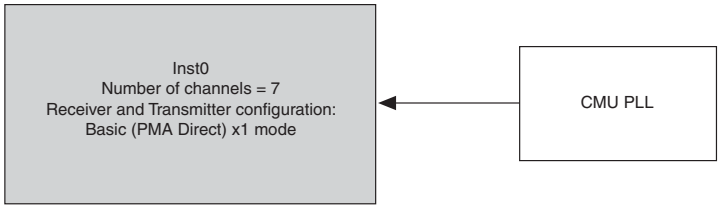
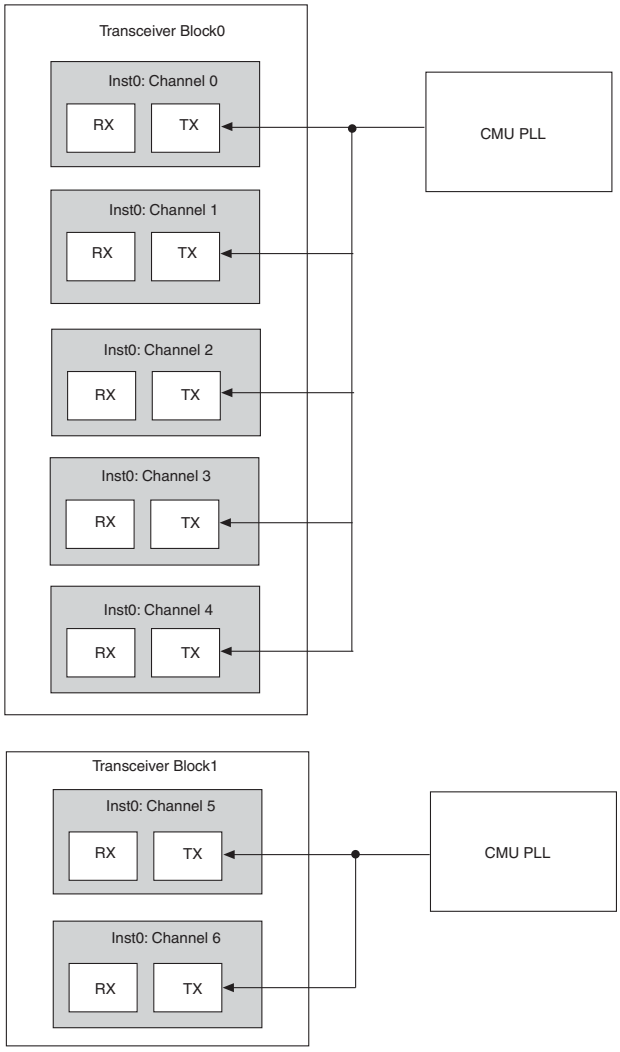


Figure 3–13 shows the conditions after compilation. In this example, the gxb_powerdown and pll_powerdown ports for channels 0 to 4 and channels 5 and 6 are driven from the same logic.

Figure 3–13. Combined Channels After Compilation for Example 5



If you connect each of the seven bits of the gxb_powerdown and pll_powerdown ports to different reset control logic, the Quartus II software requires seven transceiver blocks to combine the seven channels in the instance.

Combining Multiple Instances of Transmitter Only and Receiver Only Configurations in Basic (PMA Direct) ×1 Mode

The Quartus II software allows you to combine instances of **Transmitter Only** and **Receiver Only** configurations in Basic (PMA Direct) ×1 mode.

You can also combine **Transmitter Only** instances in non-Basic (PMA Direct) ×1 configuration (non-bonded only) and the **Receiver Only** instance in Basic (PMA Direct) configurations (and vice versa) in the same physical channel. The combination requirements of the instances in Basic (PMA Direct) ×1 configuration are similar to that of non-Basic (PMA Direct) configuration. For more information, refer to the "Combining Transmitter Channel and Receiver Channel Instances" on page 3–11.

Combining Channels Configured in Basic (PMA Direct) ×1 with Non-Basic (PMA Direct) Modes

You can combine a transceiver channel instance configured in Basic (PMA Direct) ×1 configuration with instances set up in non-Basic (PMA Direct) configurations (for example, GIGE and SDI within the same transceiver block).

If the CMU PLL configuration for the Basic (PMA Direct) ×1 configuration and the non-Basic (PMA Direct) configuration instances meet the requirements specified in "Multiple Channels Sharing a CMU PLL" on page 3–5 and "General Requirements to Combine Channels" on page 3–3, the Quartus II software uses a single CMU PLL for these two instances. In addition, to share the same CMU PLL between the two instances, you cannot enable the **channel reconfiguration** option in the instance setup in non-Basic (PMA Direct) configuration.

Example 6

Consider the example design listed in Table 3–9 for Basic (PMA Direct) ×1 and non-Basic (PMA Direct) configurations at the same data rate.

Table 3–9. Basic (PMA Direct) ×1 and Non-Basic (PMA Direct) Configurations at the Same Data Rate for Example 6

Instances	Configuration	CMU PLL Base Data Rate (Gbps)	Transmitter Channel Effective Data Rate (Gbps)	Input Reference Clock Frequency (MHz)
`inst0`	GIGE	1.25	1.25	125 (assume `refclk0`)
`inst1`	Basic (PMA Direct) ×1 (four channels)	1.25	1.25	Same as `inst0`

Figure 3–14 shows Basic (PMA Direct) ×1 and non-Basic (PMA Direct) configurations before compilation.

Figure 3–14. Logical View of the Instances in Basic (PMA Direct) ×1 and Non-Basic (PMA Direct) Configurations Before Compilation for Example 6

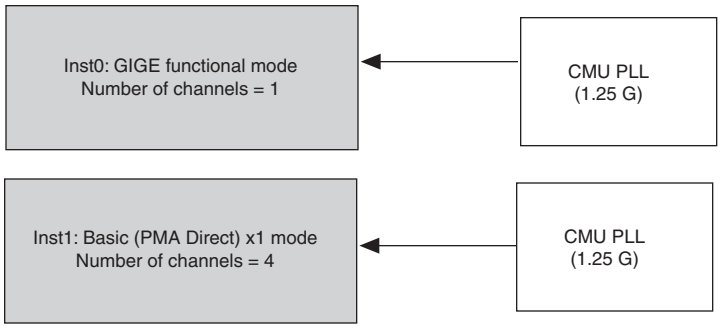
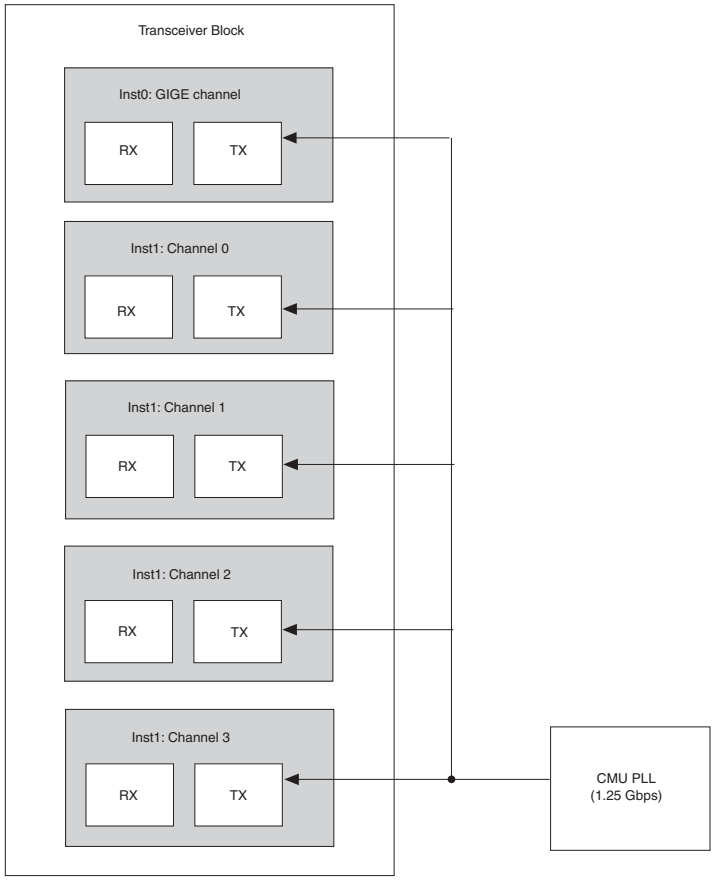


Figure 3–15 shows Basic (PMA Direct) ×1 and non-Basic (PMA Direct) configurations after compilation.

Figure 3–15. Combining Basic (PMA-Direct) ×1 and Non-Basic (PMA Direct) Configurations After Compilation for Example 6



Example 7

Consider the example design listed in Table 3–10 for Basic (PMA Direct) ×1 and non-Basic (PMA Direct) configurations at different data rates.

Table 3–10. Basic (PMA Direct) ×1 and Non-Basic (PMA Direct) Configurations at Different Data Rates for Example 7

Instances	Configuration	CMU PLL Base Data Rate (Gbps)	Transmitter Channel Effective Data Rate (Gbps)	Input Reference Clock Frequency (MHz)
`inst0`	GIGE	1.25	1.25	125 (assume `refclk0`)
`inst1`	Basic (PMA Direct) ×1 (three channels in **Receiver and Transmitter** configuration)	2	2	`refclk1`
inst2	Basic (PMA Direct) ×1 (one channel in **Transmitter Only** configuration)	2	2	refclk1

Figure 3–16 shows Basic (PMA Direct) ×1 and non-Basic (PMA Direct) configurations before compilation.

The data rate configurations of the two CMU PLLs are different.

Figure 3–16. Logical View of the Basic (PMA Direct) ×1 and Non-Basic (PMA Direct) Configurations Before Compilation for Example 7

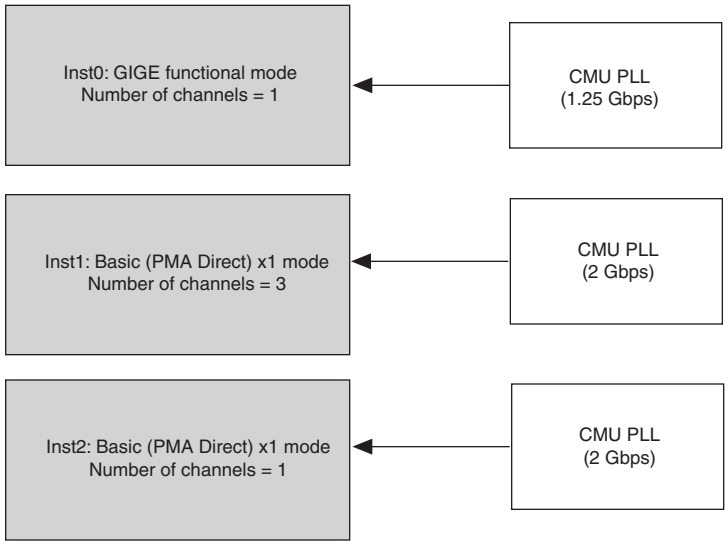
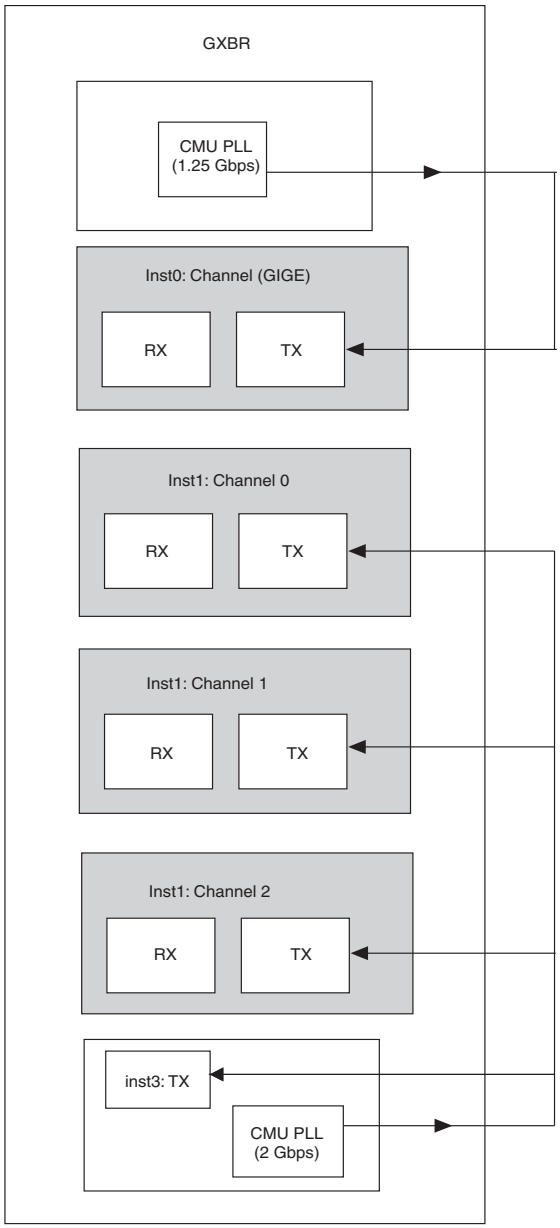


Figure 3–17 shows Basic (PMA Direct) ×1 and non-Basic (PMA Direct) configurations after compilation.

Figure 3–17. Combining Basic (PMA Direct) ×1 and Non-Basic (PMA Direct) Instances in a Transceiver Block After Compilation for Example 7



Key Observations

To combine the these instances, two CMU PLLs are required due to the different data rates. Therefore, two CMU channels must be available to enable their respective CMU PLLs. Note that `inst3` uses the transmit side of the CMU channel that uses the CMU PLL for clock generation.

Basic (PMA Direct) ×N Configurations

When you configure a transceiver channel in Basic (PMA Direct) ×N configuration, you can enable the Quartus II software to use the ×N lines to provide clocks to the transmitter channels, as shown in Figure 3–18.

The following are the possible sources driving the ×N clock lines:

- The `CMU0` central divider within the `CMU0` channel. Only the `CMU0` clock divider block can drive the ×N clock lines. Either the `CMU0` PLL or `CMU1` PLL can drive the central clock divider block.

  To understand the input clock connections to the central clock divider block, refer to the "CMU0 Channel" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

- The ATX PLL block.

Channel Placement in a Basic (PMA Direct) ×N Mode Instance

If you compile a design with a transceiver instance configured in Basic (PMA Direct) xN mode, the Quartus II software, by default, places these channels contiguously.

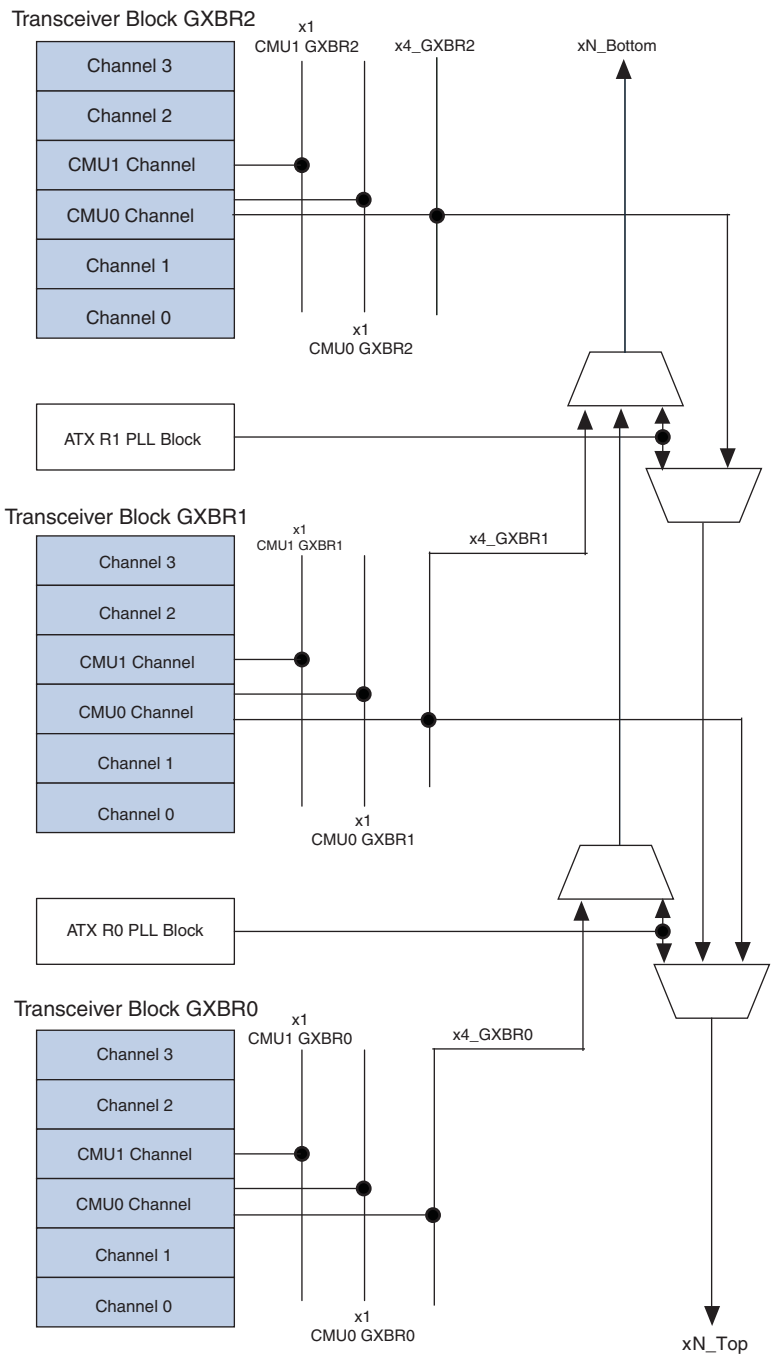
You can force the placement of the transceiver channels across multiple transceiver blocks on the same side of the device by assigning pins to the transmitter and receiver serial ports.

The logical channel 0 of the Basic (PMA Direct) ×N mode instance does not have to be assigned to the physical channel 0 of a transceiver block. The logical channel 0 of an instance with multiple channels is `tx_dataout[0]` or `rx_datain[0]`, which are the serial transmit and receive ports provided by the ALTGX MegaWizard Plug-In Manager. When you assign pins, you are not required to assign `tx_dataout[0]` to the location of physical channel 0 in the transceiver block to compile your design.

This is not the case if you have a PCIe ×4 configuration where `tx_dataout[0]` and `rx_datain[0]` must be assigned to physical channel 0 of the transceiver block.

Figure 3–18 shows the different drivers of the ×N_Top and ×N_Bottom clock lines.

Figure 3–18. The ×N_Top and ×N_Bottom Clock Line Connections



Examples of Combining Multiple Instances of Basic (PMA Direct) ×N Modes

The following section describes combining multiple transceiver channel instances in Basic (PMA Direct) ×N mode. Configuration examples include transceiver channels with different data rates, configurations in Basic (PMA Direct) ×N mode with non-Basic (PMA Direct) and ATX PLL, and unsupported configurations.

Example 8

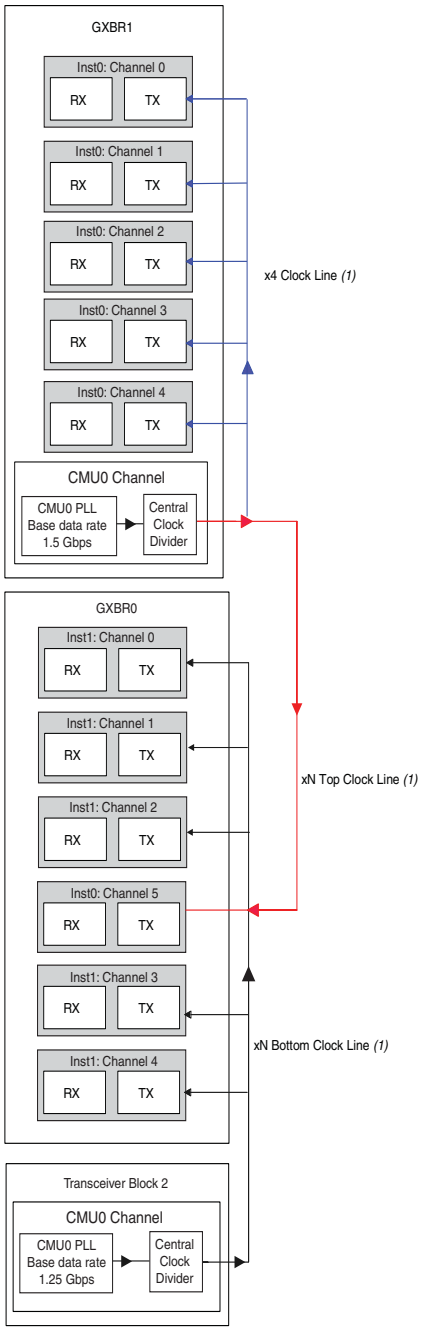
Consider the configuration for the two instances listed in Table 3–11 when combining transceiver channels in Basic (PMA Direct) ×N mode with different data rates.

Table 3–11. Combining Transceiver Channels in Basic (PMA Direct) ×N Configuration with Different Data Rates for Example 8

User Defined Instance Name	Number of Channels	Effective Data Rate (Gbps)	Configuration
`inst0`	6	1.5	**Receiver and transmitter**
`inst1`	5	1.25	**Receiver and transmitter**

You can place channels within a given instance non-contiguously, as shown in Figure 3–19.

Figure 3–19. Non-Contiguous Placements of Channels Using Different CMU PLLs for Example 8



Note to Figure 3–19:

(1) The red lines represent the ×N top clock line, the blue lines represent the ×4 clock line, and the black lines represent the ×N bottom clock line.

Key Observations

- Note that channel 5 in `inst0` is placed in transceiver block 1 and receives the high-speed clock through the `×N_Top` clock line.
- Some of the channels in transceiver block 1 receive their high-speed clock from the `×N_Bottom` clock line. Because the `×N_Top` and `×N_Bottom` lines are separate, this scenario is allowed. To understand the clock multiplexer on the ×N clock lines, refer to Figure 3–18 on page 3–34.

Combining Channels Configured in Basic (PMA Direct) ×N Configuration with Non-Basic (PMA Direct) Configurations

The Quartus II software only allows a combination of a transceiver channel instances configured in Basic (PMA Direct) ×N mode with instances in non-Basic (PMA Direct) configurations; for example, GIGE and SDI.

Example 9

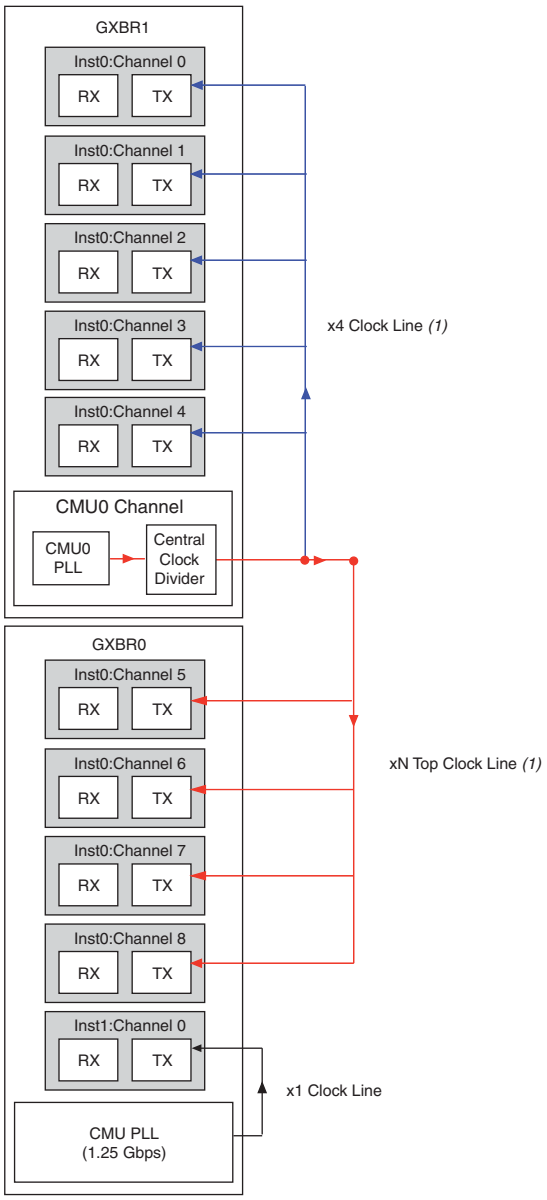
Consider the example design listed in Table 3–12 for the two instances when combining a Basic (PMA Direct) ×N configuration with a non-Basic (PMA Direct) configuration using a CMU PLL.

Table 3–12. Combining Basic (PMA Direct) ×N Configuration with Non-Basic (PMA Direct) Configuration Using CMU PLL for Example 9

User Defined Instance Name	Number of Channels	Effective Data Rate (Gbps)	Configuration	Functional Mode
`inst0`	9	1.5	Receiver and Transmitter	Basic (PMA Direct) ×N
`inst1`	1	1.25	Receiver and Transmitter	GIGE

You can place these two instances in two transceiver blocks, as shown in Figure 3–20.

Figure 3–20. Combining Basic (PMA Direct) ×N Configuration with Non-Basic (PMA Direct) Configuration Using CMU PLL in Two Transceiver Blocks For Example 9



Note to Figure 3–20:

(1) The red lines represent the ×N top clock line, the blue lines represent the ×4 clock line, and the black line represents the ×N bottom clock line.

Example 10

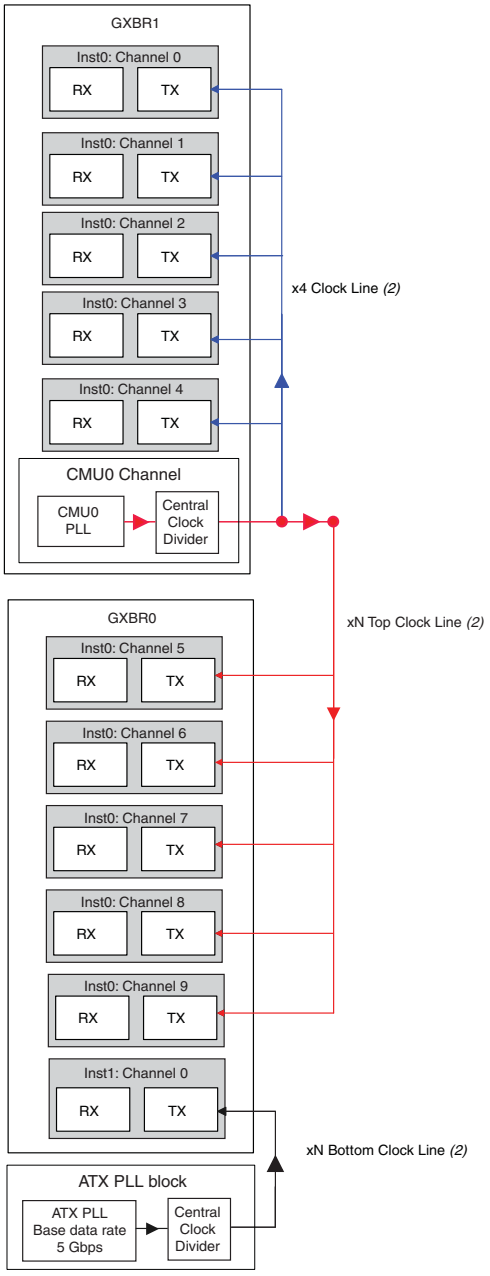
Consider the example design listed in Table 3–13 when combining a Basic (PMA Direct) ×N configuration with a non-Basic (PMA Direct) configuration using an ATX PLL.

Table 3–13. Combining Basic (PMA Direct) ×N Configuration with Non-Basic (PMA Direct) Configuration Using ATX PLL for Example 10

User Defined Instance Name	Number of Channels	Effective Data Rate (Gbps)	Configuration	Functional Mode
`inst0`	10	1.5	**Receiver and Transmitter**	Basic (PMA Direct) ×N configuration
`inst1`	1	5	**Receiver and Transmitter**	Basic mode (PCS+PMA) using ATX PLL

In this case, the ATX PLL provides the high-speed clock to the transmitter channel of `inst1`. Therefore, you can combine 10 channels of `inst0` and one channel of `inst1` in two transceiver blocks, as shown in Figure 3–21.

Figure 3–21. Combining Basic (PMA Direct) ×N Configuration with Non-Basic (PMA Direct) Configuration Using an ATX PLL for Example 10 (1)



Notes to Figure 3–21:

(1) The ATX PLL provides the high-speed clock to channel 0 of `inst1`.

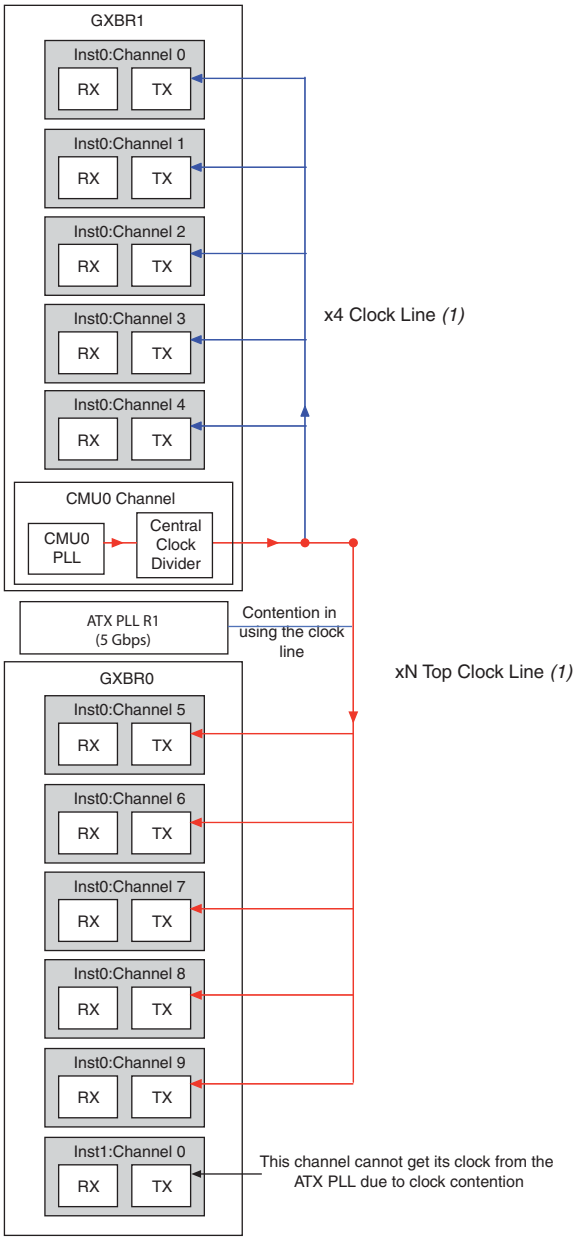
(2) The red lines represent the ×N top clock line, the blue lines represent the ×4 clock line, and the black line represents the ×N bottom clock line.

You can also combine channels configured in Basic (PMA Direct) ×N mode with bonded ×4 and ×8 functional modes. For example scenarios, refer to Figure 3–8 on page 3–19 and Figure 3–10 on page 3–22.

Example 11

Consider the unsupported placement design example shown Figure 3–22. The placement is unsupported because of the ×N_Top clock line contention between the ATX PLL and the CMU0 PLL in transceiver block 0.

Figure 3–22. Unsupported Placement Due to ×N Clock Line Contention for Example 11



Note to Figure 3–22:

(1) The red lines represent the ×N top clock line and the blue lines represent the ×4 clock line.

Combination Requirements When You Enable Channel Reconfiguration

You can configure a transmitter channel to:

- Switch to an alternate CMU PLL present within the same transceiver block.
- Switch to multiple TX PLLs (CMU or ATX PLLs) that are present outside the transceiver block.

For more information about setting up the transceiver to enable one of these three options, refer to the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

The section describes the combination requirements for an instance that is configured in one of the three options mentioned above with other instances.

Combination Requirements When You Enable the Use Alternate CMU PLL Option

If you create a transceiver instance by selecting the **use alternate CMU PLL** option, the Quartus II software uses two CMU PLLs. If you intend to combine other transmitter instances within the same transceiver block, the CMU PLLs must be shared between multiple instances. To enable the Quartus II software to share the CMU PLLs between these instances, you must:

1. Select the **user alternate CMU PLL** option in all the instances.
2. Set the same **PLL logical reference index** value for the similar PLLs between the two instances (similar PLLs are the ones that have the same data rate, input clock frequency, and bandwidth setting).
3. Create a **GXB TX PLL Reconfiguration** group setting in the assignment editor and assign the same value for both instances. This setting is required for all instances and channels controlled by the shared `ALT_GX_Reconfig`.

Table 3–14 lists the assignment for the first instance (Instance 1).

Table 3–14. Assignment for the First Instance—Instance 1

Assignment	Setting
To	`<provide the tx_dataout port name of first instance>`
Assignment Name	GXB TX PLL Reconfiguration group setting
Value	<any number>

Table 3–15 lists the assignment for the second instance (Instance 2).

Table 3–15. Assignment for the Second Instance—Instance 2

Assignment	Setting
To	`<provide the tx_dataout port name of second instance>`
Assignment Name	GXB TX PLL Reconfiguration group setting
Value	<same number as that of the first instance>

Ensure that the requirements specified in the "General Requirements to Combine Channels" on page 3–3 and "Sharing CMU PLLs" on page 3–5 sections are met.

Example 12 shows the requirements.

Example 12

Consider that you intend to run four channels within the transceiver block to switch between GIGE and SONET OC48 data rates. Assume that by default two channels run at GIGE data rates and the other two channels run at SONET OC48 data rates.

Assume that Instance1 with two channels running at GIGE data rate is created with the configuration, as listed in Table 3–16.

Table 3–16. Combining Requirements with the Use Alternate CMU PLL Option Enabled—Instance 1 for Example 12

PLL	Data Rate (Gbps)	Input Reference Clock (MHz)	PLL Logical Reference Index
Main PLL	1.25	125	0
Alternate PLL	2.488	155.5	1

Create Instance 2 with the following parameters to enable the Quartus II software to share CMU PLLs between the two instances.

Table 3–17 lists the required parameters to be set for Instance 2.

Table 3–17. Combining Requirements with the Use Alternate CMU PLL Option Enabled—Instance 2 for Example 12

PLL	Data Rate (Gbps)	Input Reference Clock (MHz)	PLL Logical Reference Index
Main PLL	2.488	155.5	1
Alternate PLL	1.25	125	0

Table 3–18 lists the assignment for the **GXB TX PLL Reconfiguration** group for Instance 1 when you compile the design.

Table 3–18. Assignment for the GXB TX PLL Reconfiguration Group for Instance 1

Assignment	Setting
To	`tx_dataout_instance1[0]` Note that the number of channels in this instance is 2. You can use any one of the channel port names within this instance for this assignment.
Assignment Name	GXB TX PLL Reconfiguration group setting
Value	6

Table 3–19 lists the assignment for the **GXB TX PLL Reconfiguration** group for Instance 2 when you compile the design.

Table 3–19. Assignment for the GXB TX PLL Reconfiguration Group for Instance 2

Assignment	Setting
To	`tx_dataout_instance2[1]` You can use any one of the channel port names within this Instance for this assignment.
Assignment Name	GXB TX PLL Reconfiguration group setting
Value	6

Key Observations

- The Main PLL in Instance 1 is configured for GIGE data rates because this is the data rate that you intend to run the first instance.
- The main PLL in Instance 2 is configured for SONET OC48 data rates because this is the data rate that you intend to run the second channel.
- Note that the PLL logical reference index values for similar PLLs in Instance 1 and Instance 2 are the same.
- The **GXB TX PLL Reconfiguration** group setting value for `tx_dataout` of Instance 1 and Instance 2 are the same.

Combination Requirements When You Use Multiple TX PLLs

This scenario describes transceiver configurations that have the **use additional CMU/ATX Transmitter PLLs from outside the transceiver block** option in the **reconfig screen** enabled.

If you create a transceiver instance using the above option and would like to share the CMU PLLs or ATX PLL with other instances, ensure that you have met the following requirements:

- Select the **use additional CMU/ATX Transmitter PLLs from outside the transceiver block** option in other instances.

  The number of additional PLLs selected (in the **How many additional PLLs are used** option) can be different between instances.

- The PLL logical reference index value of the similar PLLs that you intend to combine must be the same in all the instances considered.

  Similar PLLs are the ones that have the same data rate, input clock frequency, and bandwidth setting.

- Assign the same **GXB TX PLL Reconfiguration** group setting value for the `tx_dataout` ports of all the instances. This is explained in "Combination Requirements When You Enable the Use Alternate CMU PLL Option" on page 3–42.
- Ensure that the requirements specified in "General Requirements to Combine Channels" on page 3–3, "Sharing CMU PLLs" on page 3–5, and "Sharing ATX PLLs" on page 3–10 are met.

If you create an instance using the **use additional CMU/ATX Transmitter PLLs from outside the transceiver block** option and place your transmitter channels in one transceiver block (for example, QL1) and you use a CMU/ATX PLL from another transceiver block (for example, QL0), the channels (if used) in QL0 must be connected to the same reconfiguration controller as that of QL1. Example 13 shows an instance using multiple PLLs.

Example 13

Consider that the following 12-channel design is targeted for a THREE transceiver block per side device. The requirements for this design are:

1. Four transceiver channels to switch independently between four protocol data rates (SONET OC48, FC 2G, GIGE, and OTU1).
2. Four transceiver channels to operate in SONET OC48 data rate.
3. Four transceiver channels to operate in GIGE data rate.

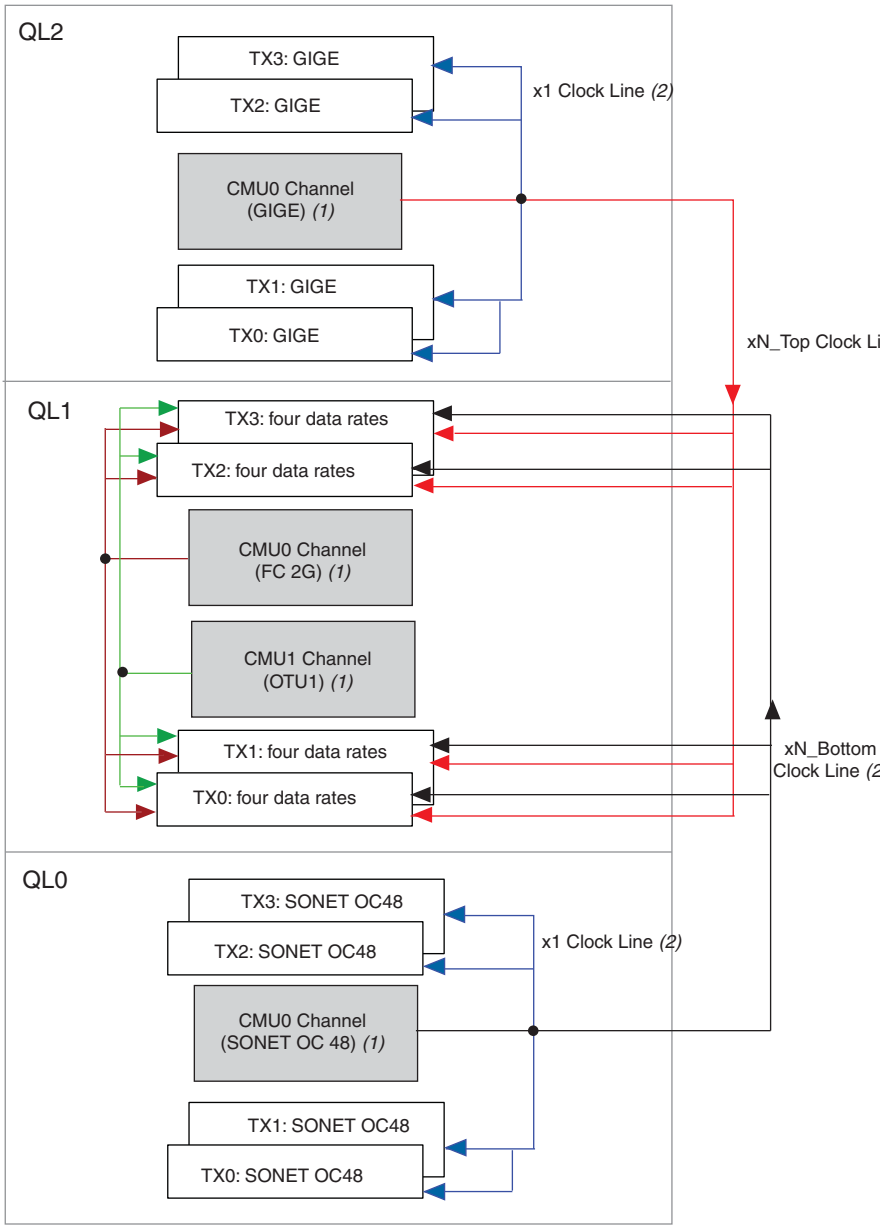
To implement step 1, you need four TX PLLs. Place the four channels in the middle transceiver block (QL1—the left side was chosen for illustration purposes), and provide one CMU PLL from QL0 for the SONET OC48 data rate and one CMU PLL from QL2 for the GIGE data rate. Use the two CMU PLLs from QL1 for the FC 2G and OTU1 data rates.

To implement step 2, note that the CMU PLL in QL0 already provides the SONET OC48 data rate. Therefore, use the four channels in QL0 to run the SONET OC48 data rate.

To implement step 3, note that the CMU PLL in QL2 already provides the GIGE data rate. Therefore, use the four channels in QL2 to run the GIGE data rate.

Figure 3–23 shows the configuration for Example 13.

Figure 3–23. Three Transceiver Block Configuration for Example 13



Notes to Figure 3–23:

(1) CMU channels are used for clock generation.

(2) The red lines represent the ×N top clock line, the blue lines represent the ×1 clock line, the black lines represent ×N bottom clock, the green lines represents the `CMU1` channel, and the brown lines represent the `CMU0` channel.

Create three Instances for steps 1, 2, and 3 with the following parameters:

Instance 1

- Select the **use additional CMU/ATX Transmitter PLLs from outside the transceiver block** option.
- Number of additional PLLs: **3** (Table 3–20)

Table 3–20. Instance 1 for Example 13

PLL	Data Rate	PLL Logical Reference Index
Main PLL	FC 2G	0
PLL1	OTU1	1
PLL2	GIGE	2
PLL3	SONET OC48	3

Instance 2

- Select the **use additional CMU/ATX Transmitter PLLs from outside the transceiver block** option.
- Number of additional PLLs: **0** (Table 3–21)

Table 3–21. Instance 2 for Example 13

PLL	Data Rate	PLL Logical Reference Index
Main PLL	SONET OC48	3

Instance 3

- Select the **use additional CMU/ATX Transmitter PLLs from outside the transceiver block** option.
- Number of additional PLLs: **0** (Table 3–22)

Table 3–22. Instance 3 for Example 13

PLL	Data Rate	PLL Logical Reference Index
Main PLL	GIGE	2

For more information, refer to "Combination Requirements When You Enable the Use Alternate CMU PLL Option" on page 3–42.

Combining Transceiver Channels When You Enable the Adaptive Equalization (AEQ) Feature

To enable the AEQ feature in a transceiver channel, select the **Enable Adaptive Equalization** option in the **Reconfig** screen of the ALTGX MegaWizard Plug-In Manager. When you select this option, the `aeq_fromgxb` and `aeq_togxb` ports are enabled.

For more information about initiating the AEQ feature, refer to the "Adaptive Equalization (AEQ)" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

This section describes the requirements to combine transceiver channels when you enable the AEQ feature.

You are not required to enable AEQ in all instances to combine them within the same transceiver block. When you instantiate the reconfiguration controller (ALTGX_Reconfig), the aeq_fromgxb and aeq_togxb ports available depend on the setting in the **what is the number of channels controlled by the reconfig controller** option. In configurations where AEQ is enabled on some of the transceiver channels that are connected to the same reconfiguration controller, the reconfiguration controller instance has additional aeq_fromgxb ports. To compile the design successfully, connect the unused aeq_fromgxb ports to 0. Example 14 shows the configuration.

Example 14

Consider that you have two ALTGX instances, Instance 1 and Instance 2 with one channel each. Assume that only Instance 1 has the **Enable adaptive equalization** option enabled.

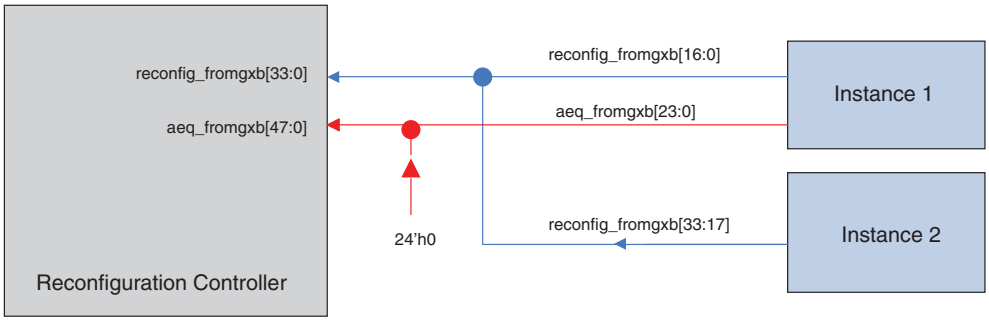
Because there are two instances, the starting channel numbers of Instance 1 and Instance 2 are spaced four apart (0 and 4, respectively).

In the ALTGX_Reconfig Instance, set the **what is the number of channels controlled by the reconfig controller** option to 8. The ALTGX_Reconfig Instance has 48 bits for the aeq_fromgxb port (24 bits per 4 channels). Instance 1 has the aeq_fromgxb[23:0] port because AEQ is enabled. Instance 2 does not have this port. Because Instance 1 has the starting channel number of 0, connect aeq_fromgxb of instance 1 to aeq_fromgxb[23:0] of the ALTGX_Reconfig Instance and tie aeq_fromgxb[47:24] to 0.

For more information about setting this parameter, refer to the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Figure 3–24 shows the required connection for the aeq_fromgxb port.

Figure 3–24. Required Connection for the aeq_fromgxb Port



The top 24 bits of aeq_fromgxb are tied to 0. This is because the logical channel address of Instance 1 starts at 4. Therefore, the top 24 bits of aeq_fromgxb corresponds to Instance 2.

Combination Requirements for Stratix IV Devices

Stratix IV GT devices allow configuring multiple protocols or data rates in the same transceiver block. For common protocols supported by both Stratix IV GX and GT devices, as well as for Basic functional mode at data rates between 2.488 Gbps and 8.5 Gbps, Stratix IV GT devices follow the same transceiver channel placement rules as Stratix IV GX devices.

Placement Rules for Transceiver Channels at 9.9 Gbps to 11.3 Gbps

You can use either the CMU PLL or the 10G ATX PLL to generate transceiver clocks for channels configured at data rates between 9.9 Gbps and 10.3125 Gbps.

If you use a 10G ATX PLL to generate transceiver clocks for any channel configured between 9.9 Gbps and 10.3125 Gbps within a transceiver block, the remaining channels in the same transceiver block must either be unused or must be configured at the same data rate and clocked by the same 10G ATX PLL.

If you use a CMU PLL to generate transceiver clocks for any channel configured between 8.5 Gbps and 11.3 Gbps within a transceiver block, the remaining channels in the same transceiver block may be configured at a different data rate and clocked by another CMU PLL or 6G ATX PLL. In this case, Stratix IV GT devices follow the same transceiver channel placement rules as Stratix IV GX devices.

Placing transceiver channels clocked by another PLL in the same transceiver block as a 10G channel can result in higher transmitter output jitter on the 10G channel. The amount of additional jitter is pending characterization.

Summary

The following is a summary for configuring multiple protocols and data rates in a transceiver block:

- You can run each transceiver channel at independent data rates or in independent protocol functional modes.
- Each transceiver block consists of two CMU PLLs that provide clocks to run the transmitter channels within the transceiver block.
- To enable the Quartus II software to combine multiple instances of transceiver channels within a transceiver block, follow the rules specified in "General Requirements to Combine Channels" on page 3–3 and "Sharing CMU PLLs" on page 3–5.
- You can reset each CMU PLL within a transceiver block using a `pll_powerdown` signal. For each transceiver instance, the ALTGX MegaWizard Plug-In Manager provides an option to select the `pll_powerdown` port. If you want to share the same CMU PLL between multiple transceiver channels, connect the `pll_powerdown` ports of the instances and drive the signal from the same logic.

- If you enable the PCIe hard IP block using the PCI Express Compiler, the Quartus II software has certain requirements for using the remaining transceiver channels within the transceiver block in the other configurations. For more information, refer to "Combining Channels Using the PCIe hard IP Block with Other Channels" on page 3–24.
- The Quartus II software supports two kinds of Basic (PMA Direct) configurations (×1 and ×N).
- If you use Basic (PMA Direct) ×1 configuration, you must use the CMU PLL within the same transceiver block.

Document Revision History

Table 3–23 lists the revision history for this chapter.

Table 3–23. Document Revision History (Part 1 of 2)

Date	Version	Changes
September 2012	4.2	Updated the "Overview" section to close FB #65273.
February 2011	4.1	■ Updated Table 3–15. ■ Updated the "Multiple Channels Sharing a CMU PLL", "Transmitter Buffer Voltage (VCCH)", "Transceiver Analog Power (VCCA_L/R)", "Calibration Clock and Power Down", "Combining Transceiver Instances Using PLL Cascade Clocks", "Combining Channels Using the PCIe hard IP Block with Other Channels", "Combination Requirements When You Enable the Use Alternate CMU PLL Option", and "Placement Rules for Transceiver Channels at 9.9 Gbps to 11.3 Gbps" sections. ■ Updated chapter title. ■ Applied new template. ■ Minor text edits.
November 2009	4.0	■ Added "Sharing ATX PLLs" on page 3–9, "Combination Requirements When Channel Reconfiguration is Enabled" on page 3–42, "Combining Transceiver Channels When the Adaptive Equalization (AEQ) is Enabled" on page 3–47, and "Combination Requirements for Stratix IV GT Devices" on page 3–49. ■ Added Figure 3–8, Figure 3–10, Figure 3–11, Figure 3–23, and Figure 3–24. ■ Updated all other sections. ■ Added Stratix IV GT information. ■ Updated graphics. ■ Minor text edits.
June 2009	3.1	■ Updated Table 3–7. ■ Minor text edits.
March 2009	3.0	■ Updated sections "Combining Channels Using the PCI Express Hard IP Block with Other Channels" on page 3–17, "Convention Used" on page 3–21, "PMA Direct Mode Restrictions" on page 3–22, "Multiple 'PMA Direct x1' Configuration Instances with One Channel per Instance" on page 3–22, "Combining Multiple Instances of TX Only and RX Only PMA-Direct x1 Configurations" on page 3–26, "Combining Transceiver Channels with PMA Direct Configuration" on page 3–21. ■ Updated Table 3–7. ■ Updated Figure 3–19.

Table 3–23. Document Revision History (Part 2 of 2)

Date	Version	Changes
November 2008	2.0	■ Updated "Transmitter Buffer Voltage (VCCH)" on page 3–2 ■ Added "reconfig_fromgxb and reconfig_togxb Ports" on page 3–3 ■ Updated Figure 3–7 ■ Added "Basic x8 Mode" on page 3–15 ■ Added Figure 3–8 ■ Updated Table 3–7
May 2008	1.0	Initial release.