Cyclone IV GX FPGA Development Board

Reference Manual

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Contents

Additional Information

1. Overview

This document describes the hardware features of the Cyclone® IV GX FPGA development board, including the detailed pin-out and component reference information required to create custom FPGA designs that interface with all components of the board.

General Description

The Cyclone IV GX FPGA development board provides a hardware platform for developing and prototyping low-power, high-volume, feature-rich designs as well as to demonstrate the Cyclone IV GX device's on-chip memory, embedded multipliers, and the Nios® II embedded soft processor. The board provides peripherals and memory interfaces to facilitate the development of the Cyclone IV GX FPGA designs.

For more information on the Cyclone IV device family, refer to the *Cyclone IV Device Handbook*.

Board Component Blocks

The board features the following major component blocks:

- Cyclone IV GX EP4CGX150DF31 FPGA in the 896-pin FineLine BGA (FBGA) package
  - 1.2-V core power
- MAX® II EPM2210GF256 CPLD in the 256-pin FBGA package
  - 1.8-V core power
- FPGA configuration circuitry
  - MAX II CPLD EPM2210 System Controller and flash fast passive parallel (FPP) configuration
  - Active serial configuration
  - On-board USB-Blaster™ for use with the Quartus® II Programmer
  - JTAG header for external USB-Blaster with the Quartus II Programmer
- On-Board ports
  - Embedded USB-Blaster
  - One gigabit Ethernet port
- Communication ports
  - PCI Express (PCIe) edge connector
  - 10/100/1000BASE-T Ethernet PHY with RJ-45 connector
  - Two High-Speed Mezzanine Card (HSMC) interfaces

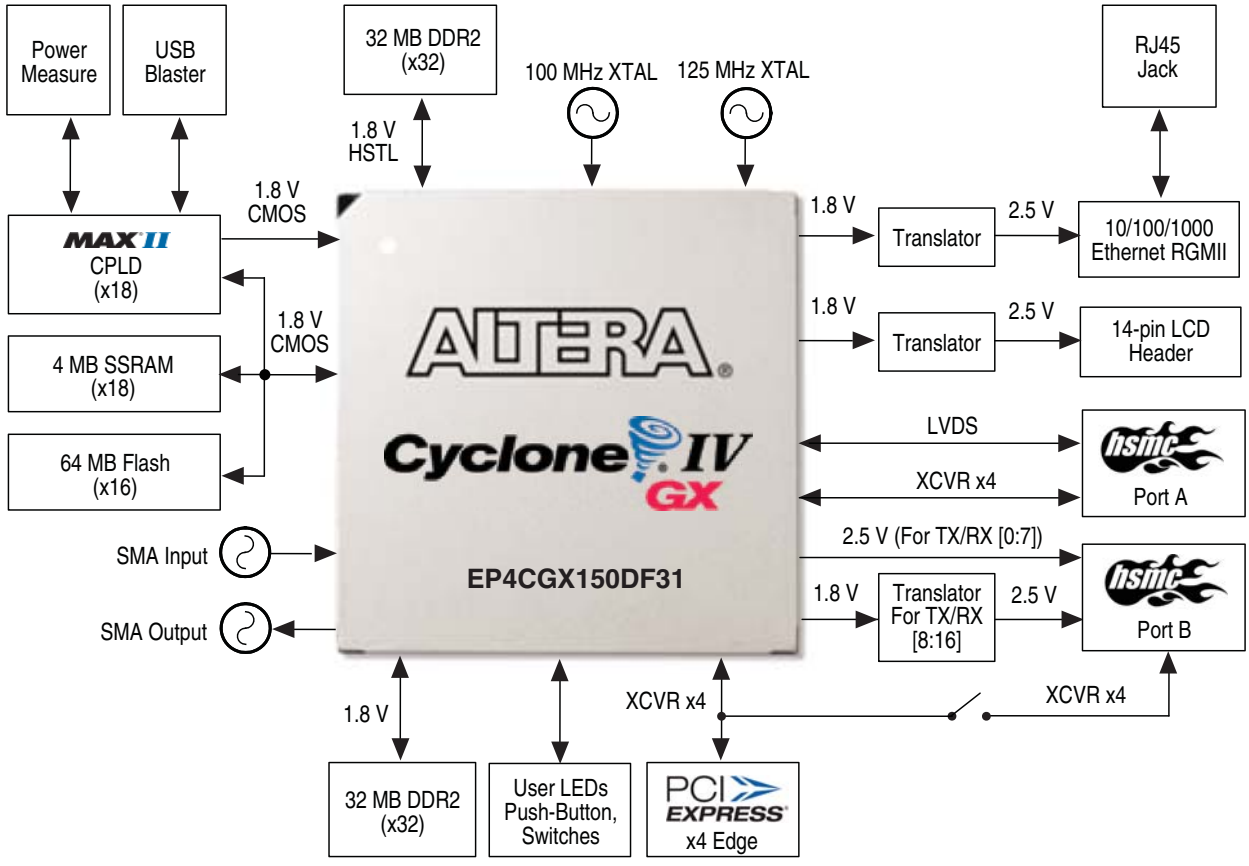
- On-Board memory
  - 4-MB (x16) Synchronous Static Random Access Memory (SSRAM)
  - Two 32-MB (x32) DDR2 SDRAM
  - 64-MB flash
- On-Board clocking circuitry
  - 50.000-MHz oscillator
  - 125.000-MHz oscillator
  - SMA clock input
  - SMA clock output
  - Programmable oscillator (default: 100.000-MHz)
- General user I/O
  - LEDs and display
    - Eight FPGA user LEDs
    - One configuration done LED
    - One error LED
    - Five Ethernet status LEDs
    - One USB status LED
    - One power status LED
    - Five configuration LEDs
    - A two-line 16-character LCD display
  - Push buttons
    - One CPU reset push button
    - One MAX II configuration reset push button
    - One program-load push button—configure the FPGA from flash memory
    - One program-select push button—select image to load from flash memory or serial configuration (EPCS) device
    - Four general user push buttons
  - DIP switches
    - Board settings DIP switch
    - JTAG chain select DIP switch
    - PCIe control DIP switch
    - Configuration settings DIP switch
    - User DIP switch

- Power supply
  - 16-V DC input
  - 2.5-mm barrel jack for DC power input
  - On/Off slide power switch
  - On-Board power measurement circuitry
  - 20-W per HSMC interface
- Mechanical
  - PCIe small form factor board
  - Bench-top operation

Development Board Block Diagram

Figure 1–1 shows the block diagram of the Cyclone IV GX FPGA development board.

Figure 1–1. Cyclone IV GX FPGA Development Board Block Diagram



Handling the Board

When handling the board, it is important to observe the following static discharge precaution:

Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

2. Board Components

Introduction

This chapter introduces the major components on the Cyclone IV GX FPGA development board. Figure 2–1 illustrates major component locations and Table 2–1 provides a brief description of all component features of the board.

A complete set of schematics, a physical layout database, and GERBER files for the development board reside in the Cyclone IV GX FPGA development kit documents directory.

For information about powering up the board and installing the demonstration software, refer to the *Cyclone IV GX FPGA Development Kit User Guide*.

This chapter consists of the following sections:

Board Overview

This section provides an overview of the Cyclone IV GX FPGA development board, including an annotated board image and component descriptions. Figure 2–1 provides an overview of the development board features.

Figure 2–1. Overview of the Cyclone IV GX FPGA Development Board Features

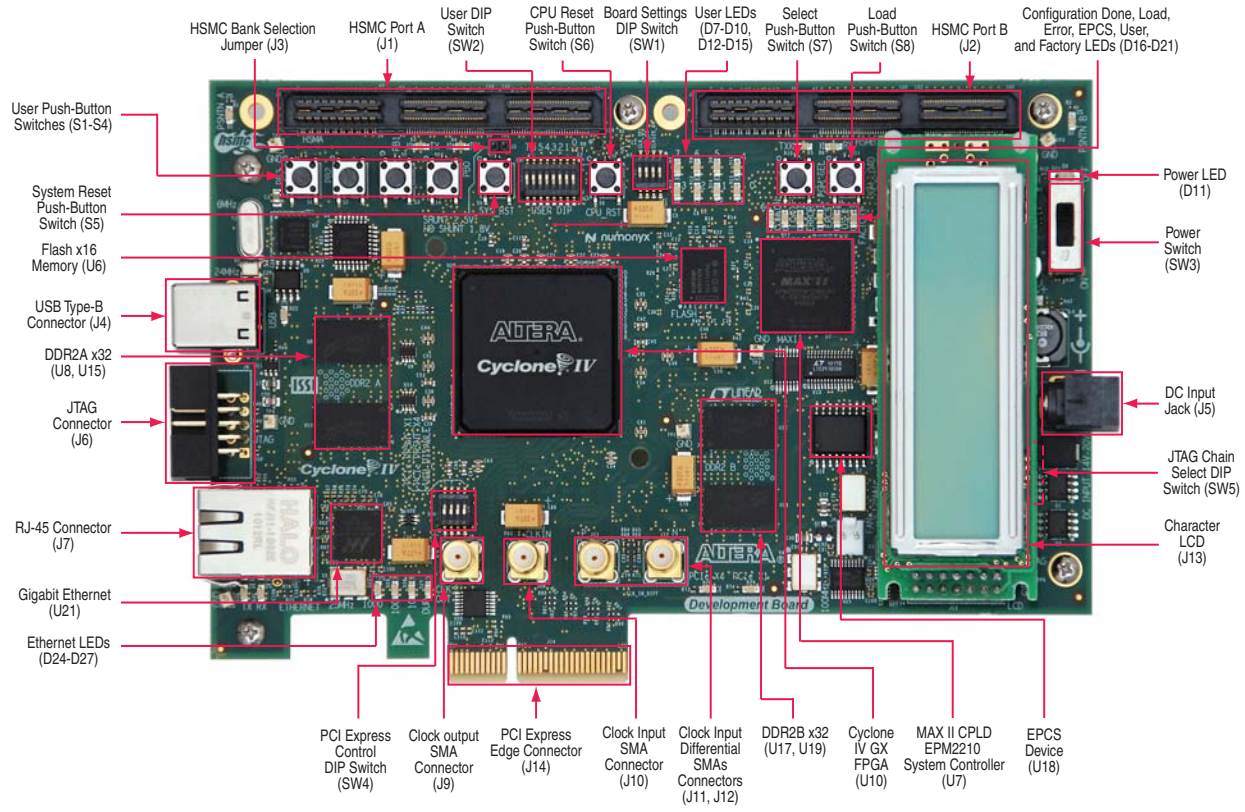


Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Cyclone IV GX FPGA Development Board Components (Part 1 of 3)

Board Reference	Type	Description
Featured Devices		
U10	FPGA	EP4CGX150DF31, 896-pin FBGA.
U7	CPLD	EPM2210GF256, 256-pin FBGA.
Configuration, Status, and Setup Elements		
J4	USB Type-B connector	Connects to the computer to enable embedded USB-Blaster JTAG.
J6	JTAG connector	Disables embedded blaster (for use with external USB-Blasters).
U18	EPCS128 serial configuration device	Flash memory device with a serial interface which stores configuration data for FPGA device that supports active serial configuration and reloads the data to the FPGA upon power-up or reconfiguration.

Table 2–1. Cyclone IV GX FPGA Development Board Components (Part 2 of 3)

Board Reference	Type	Description
D17	Load LED	Illuminates when the MAX II CPLD EPM2210 System Controller is actively configuring the FPGA.
D18	Error LED	Illuminates when the FPGA configuration from flash memory fails.
D24–D27, D30, D31	Ethernet LEDs	Shows the connection speed as well as transmit or receive activity.
D11	Power LED	Illuminates when 14-V – 20-V DC power is present.
D28	PCIe x4 LED	You can configure this LED to illuminate when PCIe is in x4 mode.
D29	PCIe x1 LED	You can configure these LEDs to illuminate when PCIe is in x1 mode.
SW4	PCIe DIP switch	Controls the PCIe lane width (connecting `prsnt` pins together on the PCIe edge connector) or disables the embedded USB-Blaster.
SW5	JTAG chain select DIP switch	Enables and disables devices in the JTAG chain. The switch is located under the character LCD.
SW1	Board settings DIP switch	Controls the Max II CPLD EPM2210 System Controller functions such as enabling the 125-MHz clock or programmable clock, as well as selection between the SMA clock input or the programmable clock for buffer multiplexer.
S5	System reset push button	Press to reset the MAX II CPLD EPM2210 System Controller.
S6	CPU reset push button	Press to reset the FPGA logic.
S7	Program select push button	Toggles the LEDs which selects the program image that loads either from the flash memory (FPP mode) or the EPCS device (active serial mode) to the FPGA.
S8	Program load push button	Configure the FGPA from flash memory based on the program select LEDs setting.
Clock Circuitry		
X2	125-MHz oscillator	125-MHz crystal oscillator for general use such as memories.
X3	50-MHz oscillator	50-MHz crystal oscillator for configuration purpose. This oscillator is located at the bottom of the board.
X5	25-MHz oscillator	25-MHz crystal oscillator for 10 Gigabit Ethernet. This oscillator is located at the bottom of the board.
Y2	6-MHz oscillator	6-MHz crystal oscillator for USB PHY. This oscillator is located at the bottom of the board.
X1	24-MHz oscillator	24-MHz crystal oscillator for USB PHY. This oscillator is located at the bottom of the board.
X4	Programmable oscillator	Programmable oscillator for PCIe or general use such as memories. Multiplexed with `CLKIN_SMA_P/N` signals based on `CLK_SEL` switch value.
J11, J12	Clock input SMA	Drive LVPECL-compatible clock input into the clock multiplexer buffer.
J10	Single-ended clock input	1.8-V single-ended clock input.
J9	Clock output SMA	Drives out 2.5-V CMOS clock output from the FPGA.

Table 2–1. Cyclone IV GX FPGA Development Board Components (Part 3 of 3)

Board Reference	Type	Description
General User Input/Output		
D7–D10, D12–D15	User LEDs	Eight user LEDs. Illuminates when driven low.
S1–S4	User push buttons	Four user push buttons. Driven low when pressed.
J13	Character LCD	Connector which interfaces to the provided 16 character × 2 line LCD module.
Memory Devices		
U44	SSRAM x18 memory	Standard synchronous RAM which provides a 72-Mbit (Mb) SSRAM port. This SSRAM is located at the bottom of the board.
U6	Flash x64 memory	Synchronous burst mode flash device which provides a 256-Mb non-volatile memory port.
U8, U15	DDR2 x32 SDRAM A	Two 16-bit memory device.
U17, U19	DDR2 x32 SDRAM B	Two 16-bit memory device.
Components Interfaces		
J7	RJ-45 connector	Provides 10/100/1000 BASE-T Ethernet connection via a Marvell 88E1111 PHY and the FPGA-based Altera Triple Speed Ethernet MegaCore function in RGMII mode.
U21	Gigabit Ethernet	A Marvell 88E1111 PHY device for 10/100/1000 BASE-T Ethernet connection. The device is an auto-negotiating Ethernet PHY with an RGMII interface to the FPGA.
J14	PCIe edge connector	Interfaces to a PCIe root port such as an appropriate PC motherboard. Made of gold-plated edge fingers for up to ×4 signaling in Gen1 mode.
J1	HSMC port A	Provides eight transceiver channels and 84 CMOS or 17 LVDS channels per the HSMC specification.
J2	HSMC port B	Provides eight transceiver channels and 84 CMOS channels per the HSMC specification.
Power Supply		
J5	DC input jack	Accepts a 16-V DC power supply. Do not use this input jack while the board is plugged into a PCIe slot.
SW3	Power switch	Switch to power on or off the board when power is supplied from the DC input jack.

Featured Device: Cyclone IV GX Device

The Cyclone IV GX FPGA development board features the Cyclone IV GX EP4CGX150DF31 device (U10) in a 896-pin FBGA package.

For more information about Cyclone IV device family, refer to the *Cyclone IV Device Handbook*.

Table 2–2 describes the features of the Cyclone IV GX EP4CGX150DF31 device.

Table 2–2. Cyclone IV GX EP4CGX150DF31 Device Features

Equivalent LEs	Embedded Memory (Kbits)	18-bit × 18-bit Multipliers	Transceivers	PLLs	User I/O	Package Type
149,760	6,480	360	8	8	475	896-pin FBGA

Table 2–3 lists the Cyclone IV GX device component reference and manufacturing information.

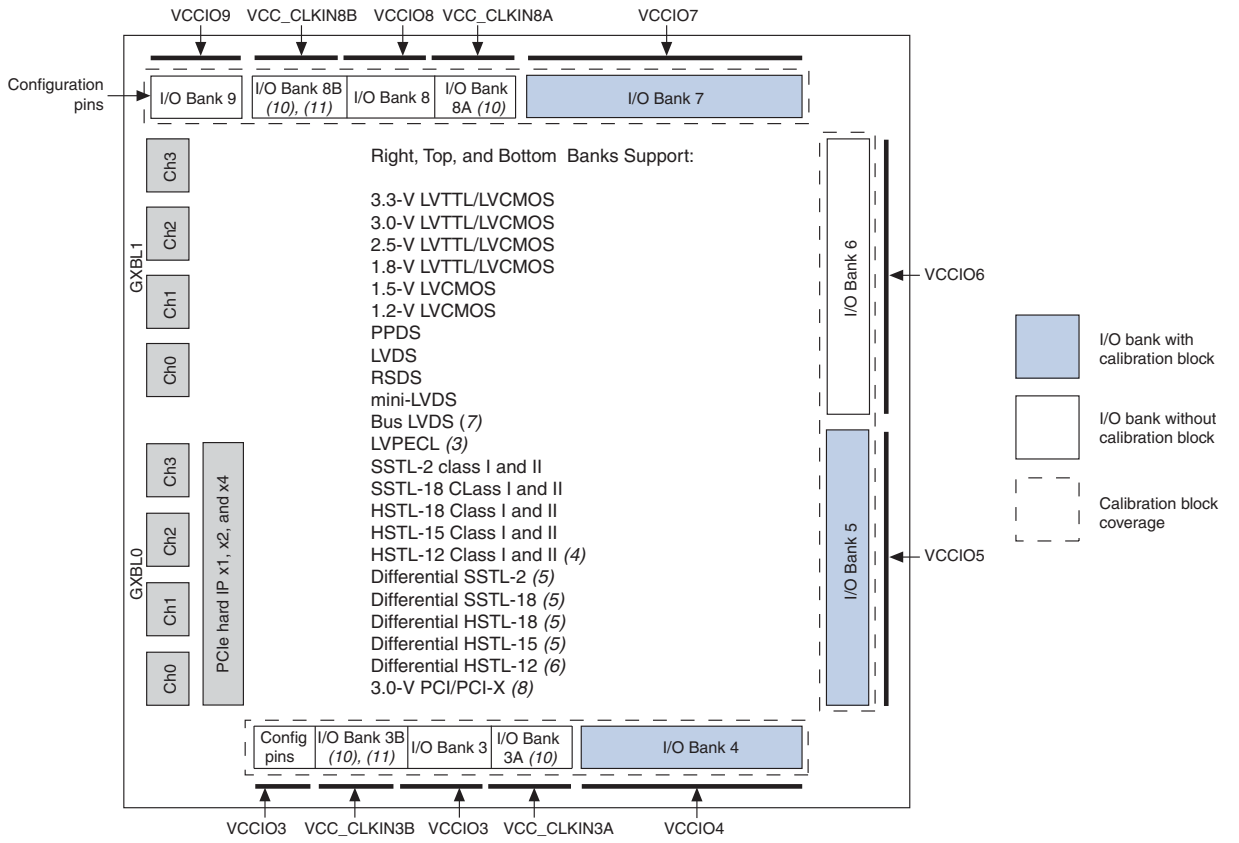
Table 2–3. Cyclone IV GX Device Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U10	FPGA, Cyclone IV GX, 896-pin FBGA package, lead-free.	Altera Corporation	EP4CGX150DF31	www.altera.com

I/O Resources

Figure 2–2 illustrates the bank organization and I/O count for the EP4CGX150DF31 device in the 896-pin FBGA package.

Figure 2–2. EP4CGX150DF31 Device I/O Bank Diagram *(1)*



Notes to Figure 2–2:

(1) This is a top view of the silicon die. For exact pin locations, refer to the pin list and the Quartus II software.

(2) True differential (PPDS, LVDS, mini-LVDS, and RSDS I/O standards) outputs are supported in row I/O banks 5 and 6 only. External resistors are needed for the differential outputs in column I/O banks.

(3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

(4) The HSTL-12 Class II is supported in column I/O banks 4, 7, and 8.

(5) The differential SSTL-18 and SSTL-2, differential HSTL-18, and HSTL-15 I/O standards are supported only on clock input pins and phase-locked loops (PLLs) output clock pins. PLL output clock pins do not support Class II interface type of differential SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards.

(6) The differential HSTL-12 I/O standard is only supported on clock input pins and PLL output clock pins. Differential HSTL-12 Class II is supported only in column I/O banks 4, 7, and 8.

(7) BLVDS output uses two single-ended outputs with the second output programmed as inverted. BLVDS input uses the LVDS input buffer.

(8) The PCI-X I/O standard does not meet the IV curve requirement at the linear region.

(9) The OCT block is located in the shaded banks 4, 5, and 7.

(10) The dedicated clock input I/O banks 3A, 3B, 8A, and 8B can be used either for HSSI input reference clock pins or clock input pins.

(11) Single-ended clock input support is available for dedicated clock input I/O banks 3B and 8B.

Table 2–4 lists the Cyclone IV GX device pin count and usage by function on the development board.

Table 2–4. Cyclone IV GX Device I/O Pin Count and Usage

Function	I/O Standard	I/O Count	Special Pins
Clocks or Oscillators	1.8-V CMOS	9	3 clock inputs, 1 clock input
DDR2A x32 (Top)	1.8-V SSTL	63	—
DDR2B x32 (Bottom)	1.8-V SSTL	63	—
Flash, SSRAM, MAX	1.8-V CMOS	55	—
Gigabit Ethernet	2.5-V CMOS (1)	16	—
User I/O (LEDs, Push buttons)	1.8-V	25	—
14-pin LCD	2.5-V CMOS (1)	11	—
HSMC Port A	2.5-V/1.8-V CMOS	103	—
HSMC Port B	2.5-V CMOS (1)	87	—
PCIe x4	2.5-V CMOS	7	—
PCIe (for HSMC port B transceiver multiplexer)	XCVR	16	—
Passive serial and active serial configuration	2.5-V CMOS	21	—
Device I/O Total:		476	

Note to Table 2–4:

(1) Translated from 1.8-V to 2.5-V using a bidirectional voltage translator.

MAX II CPLD EPM2210 System Controller

The board utilizes the EPM2210 System Controller, an Altera MAX II CPLD, for the following purposes:

- FPGA configuration from flash memory
- Power consumption monitoring
- Virtual JTAG interface for PC-based GUI
- Control registers for clocks
- Control registers for remote system update

Figure 2–3 illustrates the MAX II CPLD EPM2210 System Controller's functionality and external circuit connections as a block diagram.

Figure 2–3. MAX II CPLD EPM2210 System Controller Block Diagram

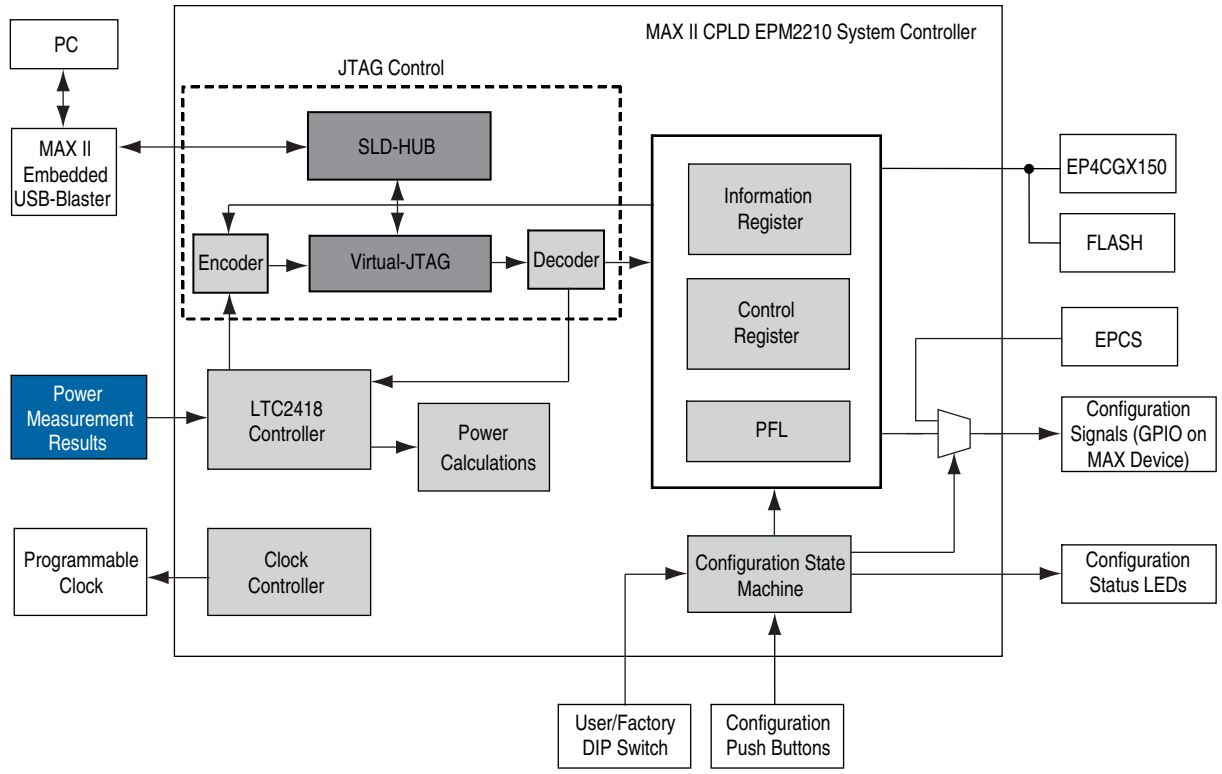


Table 2–5 lists the I/O signals present on the MAX II CPLD EPM2210 System Controller. The signal names and functions are relative to the MAX II device (U7).

Table 2–5. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 1 of 4)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	EP4CGX15BF14 Pin Number	Description
CLKA_EN	2.5-V	H3	—	125-MHz oscillator enable
CLKA_SDA		J1	—	125-MHz programming data
CLKA_SCL		H4	—	125-MHz programming clock
CLK125_EN		J2	—	125-MHz oscillator enable
CLKIN_50		H5	—	50-MHz oscillator
CLKIN_MAX_100		J5	—	MAX II clock input
FAN_CNTL		P2	—	Fan control

Table 2–5. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 2 of 4)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	EP4CGX15BF14 Pin Number	Description
FACTORY_CONFIGn	1.8-V	G12	—	Factory configuration enable
FLASH_ADVn		L13	F24	FSM bus flash memory address valid
FLASH_RESETn		M15	A28	FSM bus flash memory reset
FLASH_WEn		L12	C13	FSM bus flash memory write enable
FLASH_OEn		M16	F7	FSM bus flash memory output enable
FLASH_RDYBSYn		L11	B7	FSM bus flash memory ready
FLASH_CLK		L15	Y21	FSM bus flash memory clock
FLASH_CEn		K14	E25	FSM bus flash memory chip enable
FPGA_DATA0	2.5-V	D3	A3	FPGA data
FPGA_DATA1		L1	G9	FPGA data
FPGA_DATA2		J16	H9	FPGA data
FPGA_DATA3		J13	D1	FPGA data
FPGA_DATA4		H16	C2	FPGA data
FPGA_DATA5		H13	AE4	FPGA data
FPGA_DATA6		H15	AE5	FPGA data
FPGA_DATA7		H14	AE10	FPGA data
FPGA_DCLK		C2	B3	FPGA configuration clock
FPGA_CONF_DONE		E3	B1	FPGA configuration done
FPGA_STATUSn		C3	AJ1	FPGA configuration ready
FPGA_CONFIGn		E4	AB9	FPGA configuration active
JTAG_TCK		P3	F2	FPGA JTAG TCK
JTAG_TMS		N4	E1	FPGA JTAG TMS
JTAG_FPGA_TDO		L6	F1	FPGA JTAG TDO
JTAG_EPM2210_TDO		M5	E2	MAX II JTAG TDO

Table 2–5. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 3 of 4)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	EP4CGX15BF14 Pin Number	Description
FSM_A1	1.8-V	P7	AD6	FSM bus address
FSM_A2		R6	AK29	FSM bus address
FSM_A3		R5	AA21	FSM bus address
FSM_A4		R4	AG25	FSM bus address
FSM_A5		R3	AH5	FSM bus address
FSM_A6		M8	AH27	FSM bus address
FSM_A7		P6	AJ12	FSM bus address
FSM_A8		P8	AF16	FSM bus address
FSM_A9		R7	AH20	FSM bus address
FSM_A10		N6	AK23	FSM bus address
FSM_A11		P4	AH17	FSM bus address
FSM_A12		P5	AB21	FSM bus address
FSM_A13		N8	AF19	FSM bus address
FSM_A14		T6	AF12	FSM bus address
FSM_A15		N5	AG27	FSM bus address
FSM_A16		M6	AK26	FSM bus address
FSM_A17		N7	AH4	FSM bus address
FSM_A18		T5	AK3	FSM bus address
FSM_A19		R1	AH9	FSM bus address
FSM_A20		M7	AG6	FSM bus address
FSM_A21		T2	AK25	FSM bus address
FSM_A22		T7	AE21	FSM bus address
FSM_A23		T4	AA18	FSM bus address

Table 2–5. MAX II CPLD EPM2210 System Controller Device Pin-Out (Part 4 of 4)

Schematic Signal Name	I/O Standard	EPM2210 Pin Number	EP4CGX15BF14 Pin Number	Description
FSM_A24	1.8-V	R8	AK27	FSM bus address
FSM_A25		M9	AF21	FSM bus address
FSM_D0		E9	AK14	FSM bus data
FSM_D1		A9	AE6	FSM bus data
FSM_D2		E7	AG21	FSM bus data
FSM_D3		B7	AE9	FSM bus data
FSM_D4		A6	AK28	FSM bus data
FSM_D5		A8	AD23	FSM bus data
FSM_D6		C7	AG24	FSM bus data
FSM_D7		B6	AB22	FSM bus data
FSM_D8		E8	AE22	FSM bus data
FSM_D9		B8	AJ24	FSM bus data
FSM_D10		D8	Y19	FSM bus data
FSM_D11		D7	AH23	FSM bus data
FSM_D12		A7	AK22	FSM bus data
FSM_D13		C8	AH24	FSM bus data
FSM_D14		B5	Y18	FSM bus data
FSM_D15		A5	AJ13	FSM bus data
HSMA_PSNTn	2.5-V	G5	A25	HSMC port A present LED
HSMB_PSNTn		H2	C26	HSMC port B present LED
MAX_EPCS		G3	—	MAX II EPCS memory chip enable
MAX_ERROR		G2	—	FPGA configuration error LED
MAX_FACTORY		G4	—	FPGA factory configuration LED
MAX_USER		G1	—	FPGA user configuration LED
MAX_FAN	1.8-V	B1	—	FPGA fan LED
MAX_CSn		L16	B12	MAX II chip select
MAX_OEn		K13	G8	MAX II output enable
MAX_WEn		K15	A9	MAX II write enable
MSEL0	2.5-V	L2	AD7	FPGA MSEL0 configuration mode select
MSEL2		M1	AC7	FPGA MSEL2 configuration mode select
MSEL3		M2	AC8	FPGA MSEL3 configuration mode select
RESET_CONFIGn	1.8-V	G16	AF27	Force FPGA configuration push button
SENSE_CSn	2.5-V	F5	—	Power monitor chip select
SENSE_SCK		E1	—	Power monitor serial peripheral interface (SPI) clock
SENSE_SDI		F4	—	Power monitor SPI data in
SENSE_SDO		E2	—	Power monitor SPI data out
SYS_RESETn	1.8-V	J15	AF27	System reset push button
USER_FACTORY	2.5-V	N1	—	User reset push button

Table 2–6 lists the MAX II CPLD EPM2210 System Controller component reference and manufacturing information.

Table 2–6. MAX II CPLD EPM2210 System Controller Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U7	IC - MAX II CPLD EPM2210G 256FBGA -3 LF 1.8V VCCINT	Altera Corporation	EPM2210GF256C3N	www.altera.com

Configuration, Status, and Setup Elements

This section describes the board's configuration, status, and setup elements.

Configuration

This section describes the FPGA, flash memory, and MAX II CPLD EPM2210 System Controller device configuration methods supported by the Cyclone IV GX FPGA development board. The Cyclone IV GX FPGA development board supports the following configuration methods:

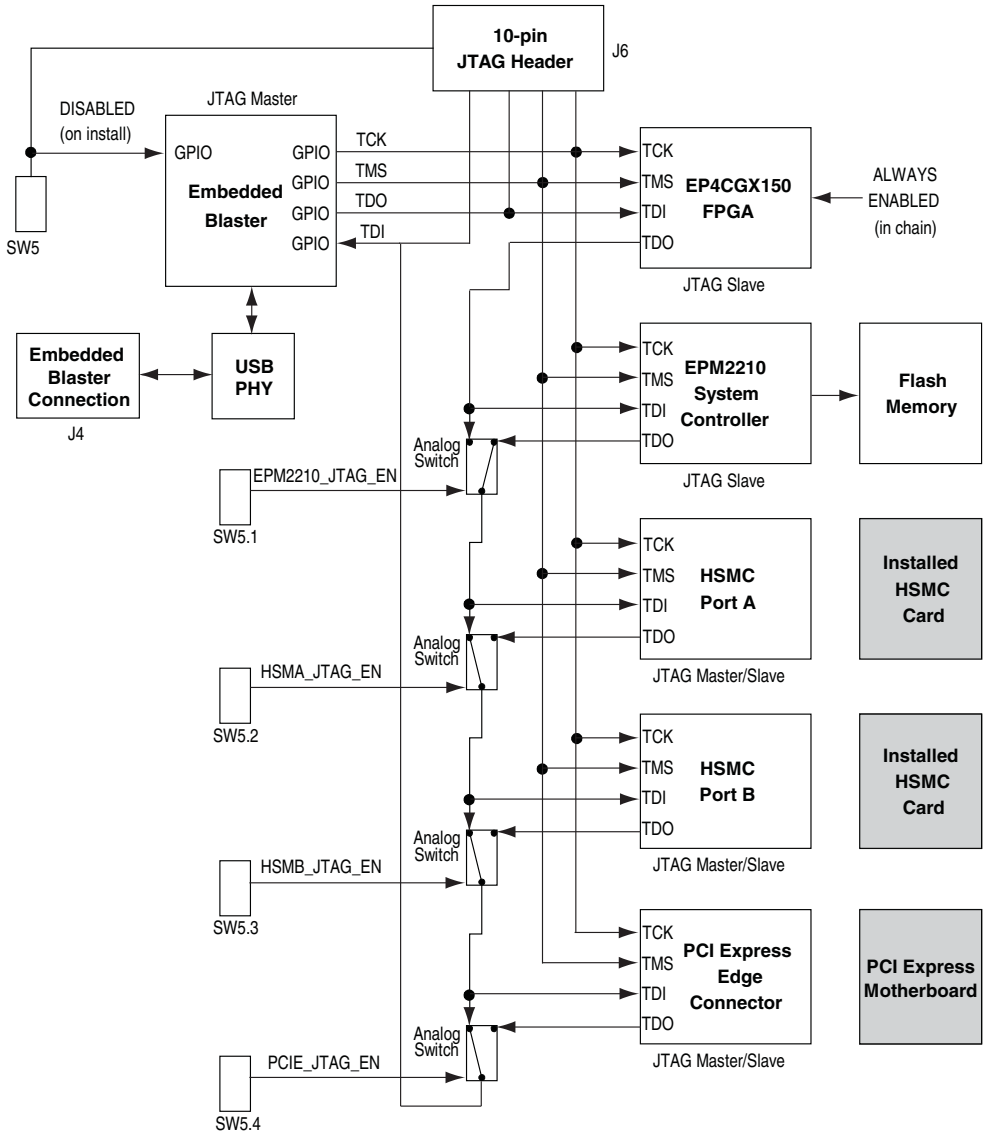
- Embedded USB-Blaster is the default method for configuring the FPGA at any time using the Quartus II Programmer in JTAG mode with the supplied USB cable.
- Flash memory download is used for storing FPGA images which the MAX II CPLD EPM2210 System Controller uses to configure the Cyclone IV GX device either on board power-up or after the program load push-button switch (S8) is pressed.
- External USB-Blaster for configuring the FPGA using an external USB-Blaster.
- Serial configuration (EPCS) device (U18) is used to store configuration data for FPGA device that supports active serial (AS) configuration and reloads the data to the FPGA upon reconfiguration. Use the program select push-button switch (S7) to select the configuration files to be loaded from either page 0 (factory location), page 1 (user location), or from the EPCS device.

FPGA Configuration over Embedded USB-Blaster

The USB-Blaster is implemented using a USB Type-B connector (J4), a FTDI USB 2.0 PHY device (U4), and an Altera MAX II CPLD (U7). This allows the configuration of the FPGA using a USB cable directly connected between the USB port on the board (J4) and a USB port of a PC running the Quartus II software. The JTAG chain is normally mastered by the embedded USB-Blaster found in the MAX II CPLD EPM2210 System Controller.

The embedded USB-Blaster is automatically disabled when an external USB-Blaster is connected to the JTAG chain. Figure 2–4 illustrates the JTAG chain.

Figure 2–4. JTAG Chain



The Cyclone IV GX FPGA is configured via JTAG using the MAX II configuration controller design (embedded blaster) as the primary configuration mode. The board includes a MAX II CPLD EPM2210 System Controller which interfaces directly to the Cyclone IV GX FPGA for configuration, LCD control, power monitor control, and other purposes. The MAX II CPLD EPM2210 System Controller contains the required state machine and control logic to determine the configuration source for the Cyclone IV GX FPGA.

Flash Memory Programming

Flash memory programming is possible through a variety of methods using the Cyclone IV GX device.

The default method is to use the factory design called the Board Update Portal. This design is an embedded web server, which serves the Board Update Portal web page. The web page allows you to select new FPGA designs including hardware, software, or both in an industry-standard S-Record File (**.flash**) and write the design to the user hardware page (page 1) of the flash memory over the network.

The secondary method is to use the pre-built parallel flash loader (PFL) design included in the development kit. The development board implements the Altera PFL megafunction for flash memory programming. The PFL megafunction is a block of logic that is programmed into an Altera programmable logic device (FPGA or CPLD). The PFL functions as a utility for writing to a compatible flash memory device. This prebuilt design contains the PFL megafunction that allows you to write either page 0, page 1, or other areas of flash memory over the USB interface using the Quartus II software. This method is used to restore the development board to its factory default settings.

Other methods to program the flash memory can be used as well, including the Nios® II processor.

For more information on the Nios II processor, refer to the Nios II Processor page of the Altera website.

FPGA Configuration from Flash Memory

On either power-up or by pressing the program load push-button switch (S8), the MAX II CPLD EPM2210 System Controller's PFL configures the FPGA from the flash memory hardware page 0 or 1 based on whether `USER` or `FACTORY` LED is illuminated. The PFL megafunction reads the data from the flash memory and loads to the FPGA using the FPP interface.

There are two pages reserved for the FPGA configuration data. The factory hardware (page 0) is loaded upon power-up if the board settings DIP switch (SW1) is set to '0'. Otherwise, the user hardware (page 1) is loaded. Pressing the program load push-button switch (S8) loads the FPGA with a hardware page based on the LED settings. Table 2–7 defines the hardware page that loads when the program load push-button switch (S8) is pressed.

Table 2–7. Program Load Push Button (S8) LED Settings *(1)*

USER LED	FACTORY LED	Design
OFF	ON	Factory hardware
ON	OFF	User hardware

Note to Table 2–7:

(1) ON indicates that the LED is illuminated while OFF indicates that the LED is not illuminated.

FPGA Configuration using External USB-Blaster

The JTAG programming header provides another method for configuring the FPGA using an external USB-Blaster device with the Quartus II Programmer running on a PC. The external USB-Blaster is connected to the board through the JTAG connector (J6). Figure 2–4 on page 2–13 illustrates the JTAG chain.

By default, the FPGA is the first device in the JTAG chain. To add the MAX II CPLD EPM2210 System Controller into the JTAG chain, set the JTAG chain select DIP switch (SW5) to '0'. Table 2–10 on page 2–17 summarizes the board settings DIP switch controls.

FPGA Configuration using EPCS Device

Active serial configuration can be performed using an Altera® EPCS device. During configuration, the FPGA is the master and the EPCS128 device is the slave. The configuration data is transferred to the FPGA on the `DATA0` pin at a rate of one bit per clock cycle. This configuration data is synchronized to the `DCLK` input.

Before you program the EPCS device, press the program select push button (S7) to select the AS configuration scheme. After programming the EPCS device, press the program load push button (S8) load the design from the EPCS device to the FPGA when you power up the board.

EPCS Programming

EPCS programming is possible through a variety of methods. One method to program the EPCS device is to use the Serial FlashLoader (SFL), a JTAG-based in-system programming solution for Altera serial configuration devices. The SFL is a bridge design for the FPGA that uses the JTAG connector (J6) to access the JTAG Indirect Configuration Device Programming File (**.jic**) and then uses the AS interface to program the EPCS device. Both the JTAG and AS interfaces are bridged together inside the SFL design.

Another method to program the EPCS device is to perform in-system programming through the AS programming header (J16).

Other methods to program the EPCS can be used as well, including the Nios II processor.

For more information on the following topics, refer to the respective documents:

Topic	Reference
Board Update Portal	*Cyclone IV GX Development Kit User Guide*
PFL Design	*Cyclone IV GX Development Kit User Guide*
PFL Megafunction	*AN 386: Using the Parallel Flash Loader with the Quartus II Software*
SFL Megafunction	*AN 370: Using the Serial FlashLoader with the Quartus II Software*
Managing and programming EPCS memory contents	*Nios II Flash Programmer User Guide*

Status Elements

The development board includes status LEDs. This section describes the status elements.

Table 2–8 lists the LED board references, names, and functional descriptions.

Table 2–8. Board-Specific LEDs

Board Reference	LED Name	Description
D1	PSNTN A	Green LED. Illuminates when the HSMC port A has a board or cable plugged-in such that pin 160 becomes grounded. Driven by the add-in card.
D2	PSNTN B	Green LED. Illuminates when the HSMC port B has a board or cable plugged-in such that pin 160 becomes grounded. Driven by the add-in card.
D11	POWER	Blue LED. Illuminates when 3.3-V power is active.
D16	FPGA_CONF_DONE	Green LED. Illuminates when the FPGA is successfully configured. Driven by the MAX II CPLD EPM2210 System Controller.
D17	FAN	Red LED. Illuminates when the FPGA needs to use the fan and heatsink. Driven by the MAX II CPLD.
D18	MAX_ERROR	Red LED. Illuminates when the MAX II CPLD EPM2210 System Controller fails to configure the FPGA. Driven by the MAX II CPLD EPM2210 System Controller.
D19, D20, D21	PROGRAM MAX_EPCS MAX_USER MAX_FACTORY	Green LEDs. Illuminates to show the LED sequence that determines which flash memory image is loaded to the FPGA. The image to be loaded depends on the selection of the three LEDs. Driven by the MAX II CPLD EPM2210 System Controller.
D22	USB	Green LED. Illuminates when the embedded USB-Blaster is in use to program the FPGA. Driven by the MAX II CPLD EPM2210 System Controller.
D24	1000	Green LED. Illuminates to indicate Ethernet linked at 1000 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D25	100	Green LED. Illuminates to indicate Ethernet linked at 100 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D26	10	Green LED. Illuminates to indicate Ethernet linked at 10 Mbps connection speed. Driven by the Marvell 88E1111 PHY.
D27	DUP	Green LED. Illuminates to indicate Ethernet in full-duplex operation. Driven by the Marvell 88E1111 PHY.
D28	PCIE_LED_X1	Green LED. Illuminates to indicate PCIe connection with channel width of ×1. Driven by the FPGA.
D29	PCIE_LED_X4	Green LED. Illuminates to indicate PCIe connection with channel width of ×4. Driven by the FPGA.
D30	ENET TX	Green LED. Illuminates to indicate Ethernet PHY transmit activity. Driven by the Marvell 88E1111 PHY.
D31	ENET RX	Green LED. Illuminates to indicate Ethernet PHY receive activity. Driven by the Marvell 88E1111 PHY.

Table 2–9 lists the board-specific LEDs component references and manufacturing information.

Table 2–9. Board-Specific LEDs Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D17, D18	Red LED	Lumex, Inc.	SML-LXT0805IW-TR	www.lumex.com
D1, D2, D11, D16, D19–D22, D24–D27, D30, D31	Green LEDs	Lumex, Inc.	SML-LXT0805GW-TR	www.lumex.com
D11	Blue LED	Lumex, Inc.	SML-LX1206USBC-TR	www.lumex.com

Setup Elements

The development board includes several different kinds of setup elements. This section describes the following setup elements:

- Board settings DIP switch
- JTAG chain select DIP switch
- PCIe control DIP switch
- Configuration push buttons
- System reset push button

Board Settings DIP Switch

The board settings DIP switch (S1) controls various features specific to the board and the MAX II CPLD EPM2210 System Controller logic design. Table 2–10 shows the switch controls and descriptions.

Table 2–10. Board Settings DIP Switch Controls

Board Reference	Schematic Signal Name	Description	Default (1)
SW1.1	USER_FACTORY	ON : Factory image OFF : User image	ON
SW1.2	CLK125_EN	ON : 125-MHz clock enabled OFF : 125-MHz clock disabled	ON
SW1.3	CLKA_EN	ON : On-Board oscillator enabled OFF : On-Board oscillator disabled	ON
SW1.4	CLKA_SEL	ON : 100-MHz oscillator input select OFF : SMA input select	ON

Note to Table 2–10:

(1) ON indicates a setting of '0' while OFF indicates a setting of '1'.

Table 2–11 lists the board settings DIP switch component reference and manufacturing information.

Table 2–11. Board Settings DIP Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
SW1	Four-position slide DIP switch	C & K Components	TDA04H0SB1	www.ck-components.com

JTAG Chain Select DIP Switch

The JTAG chain select DIP switch (SW5) controls the selection of devices in the JTAG chain. Table 2–10 shows the switch controls and descriptions.

Table 2–12. JTAG Chain Select DIP Switch Controls

Board Reference	Schematic Signal Name	Description	Default (1)
SW5.1	EPM2210_JTAG_EN	ON : Bypass Max II CPLD EPM2210 System Controller OFF : Max II CPLD EPM2210 System Controller in-chain	OFF
SW5.2	HSMA_JTAG_EN	ON : Bypass HSMC port A OFF : HSMC port A in-chain	OFF
SW5.3	HSMB_JTAG_EN	ON : Bypass HSMC port B OFF : HSMC port B in-chain	OFF
SW5.4	PCIE_JTAG_EN (2)	ON : Bypass PCIe OFF : PCIe in-chain	OFF

Notes to Table 2–12:

(1) ON indicates a setting of '0' while OFF indicates a setting of '1'.

(2) You are required to install the biderectional voltage translator analog device (part number ADG3304BRUZ) to chain the PCIe to the JTAG chain.

Table 2–11 lists the JTAG chain select DIP switch component reference and manufacturing information.

Table 2–13. JTAG Chain Select DIP Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
SW5	Four-position slide DIP switch	C & K Components	TDA04H0SB1	www.ck-components.com

PCIe Control DIP Switch

The PCIe control DIP switch (SW4) is provided to enable or disable the different configurations. Table 2–10 shows the switch controls and descriptions.

Table 2–14. PCIe Control DIP Switch Controls

Board Reference	Schematic Signal Name	Description	Default (1)
SW4.1	PCIE_PRSNT2n_x1	ON : Enable x1 presence detect OFF : Disable x1 presence detect	ON
SW4.2	PCIE_PRSNT2n_x4	ON : Enable x4 presence detect OFF : Disable x4 presence detect	ON
SW4.4	USB_DISABLE	ON : Embedded USB-Blaster disabled OFF : Embedded USB-Blaster enabled	OFF

Note to Table 2–14:

(1) ON indicates a setting of '0' while OFF indicates a setting of '1'.

Table 2–11 lists the PCIe control DIP switch component reference and manufacturing information.

Table 2–15. PCIe Control DIP Switch Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
SW4	Four-position slide DIP switch	C & K Components	TDA04H0SB1	www.ck-components.com

Configuration Settings

The MAX II CPLD EPM2210 System Controller controls the configuration settings. A configuration scheme is selected by driving the MSEL pins either high or low, as shown in Table 2–16.

Table 2–16. Configuration Settings (1)

Configuration Scheme	Setting				POR Delay
	MSEL3	MSEL2	MSEL1	MSEL0	
Active Serial—Enables active serial configuration with fast or standard power-on-reset delay.	1	1	0	1	Standard
Fast Passive Parallel—Enables FPP configuration with fast or standard power-on-reset delay.	0	0	0	1	Standard
JTAG—JTAG-based configuration	X (2)				—

Notes to Table 2–16:

(1) ON indicates a setting of '0' while OFF indicates a setting of '1'.

(2) X indicates does not care. The JTAG-based configuration takes precedence over other configuration schemes and therefore, the MSEL[] pin settings are ignored.

Configuration Push Buttons

The program load push button (S8), is an input to the MAX II CPLD EPM2210 System Controller. The push button forces a reconfiguration of the FPGA from flash memory. The location in the flash memory is based on the `board settings` DIP switch's position. Valid settings include `FACTORY` or `USER`.

The program select push button (S7), toggles the program LEDs (D3, D4) sequence. Refer to Table 2–8 on page 2–16 for the LED sequence definitions.

Table 2–17 lists the configuration push buttons component reference and manufacturing information.

Table 2–17. Configuration Push Buttons Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
S7, S8	Push buttons	Panasonic	EVQPAC07K	www.panasonic.com/industrial/

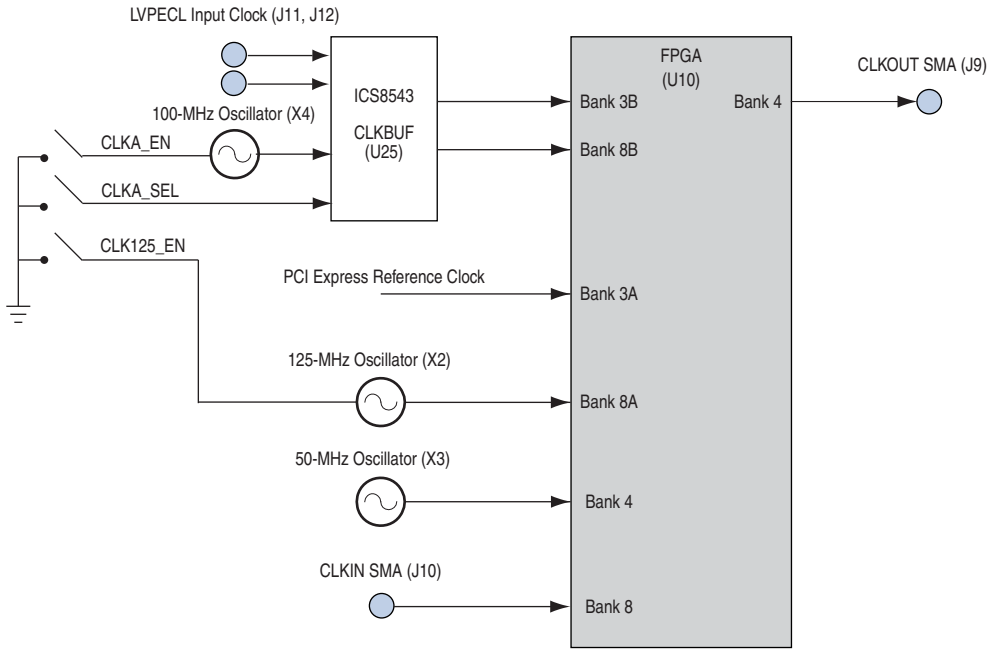
Clock Circuitry

The dedicated clock inputs are located on the top bank 8B and bottom bank 3B of the Cyclone IV GX device. An on-board programmable oscillator or a bench supply clock can be distributed to these dedicated clock inputs. The clock going to bank 3B is a dedicated clock input for 3G applications.

The non-dedicated clocks are located on banks 3A and 8A of the Cyclone IV GX device. The PCIe reference clock is on bank 3A while the 125-MHz clock is on bank 8A.

Figure 2–5 shows the Cyclone IV GX FPGA development board's transceiver clock structure.

Figure 2–5. Cyclone IV GX FPGA Development Board Transceiver Clock Structure



General User Input/Output

The development board includes several user I/O interfaces to the FPGA. This section describes the following I/O interfaces:

- User-defined push buttons
- User-defined LEDs
- User DIP switch
- Character LCD

User-Defined Push Buttons

The development board includes four user-defined push buttons, a CPU reset push button, and a system reset push button.

Board references S1, S2, S3, and S4 are push buttons that allow you to interact with the Cyclone IV GX device. When you press and hold the switch, the device pin is set to logic 0; when you release the switch, the device pin is set to logic 1. There is no board-specific function for these general user push buttons.

The system reset push button, `SYS_RESETn` (S5), resets the MAX II CPLD EPM2210 System Controller.

The CPU reset push button, `CPU_RESETn` (S6), resets the FPGA design loaded into the Cyclone IV GX device. This switch also acts as a regular I/O pin.

Table 2–18 lists the user-defined push button schematic signal names and their corresponding Cyclone IV GX device pin numbers.

Table 2–18. User-Defined Push Button Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
S4	User-defined push button. When the switch is pressed, a logic 0 is selected. When the switch is released, a logic 1 is selected.	USER_PB0	1.8-V	C12
S3		USER_PB1		D11
S2		USER_PB2		F4
S1		USER_PB3		D8
S5		SYS_RESETn		AF27
S6		CPU_RESETn		G20

Table 2–19 lists the user-defined push button component reference and the manufacturing information.

Table 2–19. User-Defined Push Button Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
S1–S6	Push button	Panasonic	EVQPAC07K	www.panasonic.com/industrial/

User-Defined LEDs

The development board includes general user-defined LEDs and HSMC user-defined LEDs. This section describes all user-defined LEDs. For information on board-specific or status LEDs, refer to "Status Elements" on page 2–16.

General User-Defined LEDs

Board references D7–D10 and D12–D15 are eight user-defined LEDs which allow status and debugging signals to be driven to the LEDs from the FPGA designs loaded into the Cyclone IV GX device. The LEDs illuminate when a logic 0 is driven, and turns off when a logic 1 is driven. There is no board-specific function for these LEDs.

Table 2–20 lists the user-defined LED schematic signal names and their corresponding Cyclone IV GX pin numbers.

Table 2–20. User-Defined LED Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
D15	User-defined LEDs. Driving a logic 0 on the I/O port turns the LED ON. Driving a logic 1 on the I/O port turns the LED OFF.	USER_LED0	2.5-V	E4
D14		USER_LED1		C7
D13		USER_LED2		A4
D12		USER_LED3		F6
D10		USER_LED4		D4
D9		USER_LED5		J9
D8		USER_LED6		D12
D7		USER_LED7		B6

Table 2–21 lists the user-defined LED component reference and the manufacturing information.

Table 2–21. User-Defined LED Component Reference and Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D7–D10, D12–D15	Green LEDs	Lumex, Inc.	SML-LXT0805GW-TR	www.lumex.com

HSMC User-Defined LEDs

The HSMC port A and B have two LEDs located nearby. There are no board-specific functions for the HSMC LEDs. However, the LEDs are labeled TX and RX, and are intended to display data flow to and from the connected HSMC cards. The LEDs are driven by the Cyclone IV GX device.

Table 2–22 lists the HSMC user-defined LED schematic signal names and their corresponding Cyclone IV GX pin numbers.

Table 2–22. HSMC User-Defined LED Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
D4	User-Defined LEDs. Labeled RX for HSMC Port A.	HSMA_RX_LED	2.5-V	C24
D3	User-Defined LEDs. Labeled TX for HSMC Port A.	HSMA_TX_LED		B25
D6	User-Defined LEDs. Labeled RX for HSMC Port B.	HSMB_RX_LED		C10
D5	User-Defined LEDs. Labeled TX for HSMC Port B.	HSMB_TX_LED		D25

Table 2–23 lists the HSMC user-defined LED component reference and the manufacturing information.

Table 2–23. HSMC User-Defined LED Component Reference and Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
D3–D6	Green LEDs	Lumex, Inc.	SML-LXT0805GW-TR	www.lumex.com

User-Defined DIP Switch

Board reference SW2 is an 8-pin DIP switch. The switch is user-defined, and is provided for additional FPGA input control. There is no board-specific function for this switch.

Table 2–24 lists the user-defined DIP switch schematic signal names and their corresponding Cyclone IV GX pin numbers.

Table 2–24. User-Defined DIP Switch Schematic Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
SW2.1	User-defined DIP switch connected to FPGA device. When the switch is in the OPEN or OFF position, a logic 1 is selected. When the switch is in the CLOSED or ON position, a logic 0 is selected.	USER_DIPSW0	2.5-V	A5
SW2.2		USER_DIPSW1		G15
SW2.3		USER_DIPSW2		E9
SW2.4		USER_DIPSW3		C8
SW2.5		USER_DIPSW4		C4
SW2.6		USER_DIPSW5		F14
SW2.7		USER_DIPSW6		G12
SW2.8		USER_DIPSW7		E7

Table 2–21 lists the user-defined LED component reference and the manufacturing information.

Table 2–25. User-Defined DIP Switch Component Reference and Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
SW2	Eight-Position DIP switch	C & K Components	TDA08H0SB1	www.ck-components.com

LCD

The development board contains a single 14-pin 0.1" pitch dual-row header that interfaces to a 16 character × 2 line Lumex LCD display. The LCD has a 14-pin receptacle that mounts directly to the board's 14-pin header, so it can be easily removed for access to components under the display. You can also use the header for debugging or other purposes.

Table 2–26 summarizes the LCD pin assignments. The signal names and directions are relative to the Cyclone IV GX FPGA.

Table 2–26. LCD Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
J13.4	LCD data or command select	LCD_D_Cn	2.5-V CMOS (1)	D5
J13.5	LCD write enable	LCD_WEn		E6
J13.6	LCD chip select	LCD_CSn		C3
J13.7	LCD data bus	LCD_DATA0		C15
J13.8	LCD data bus	LCD_DATA1		F9
J13.9	LCD data bus	LCD_DATA2		D7
J13.10	LCD data bus	LCD_DATA3		E21
J13.11	LCD data bus	LCD_DATA4		C27
J13.12	LCD data bus	LCD_DATA5		G13
J13.13	LCD data bus	LCD_DATA6		E10
J13.14	LCD data bus	LCD_DATA7		F16

Note to Table 2–26:

(1) All signals are translated from 1.8-V to 2.5-V using a dual/quad low-voltage level translators except for LCD_DATA4, which connects directly to the PLL4_CLKOUTn pin of the Cyclone IV GX FPGA.

Table 2–27 shows the LCD pin definitions, and is an excerpt from the Lumex data sheet.

For more information such as timing, character maps, interface guidelines, and other related documentation, visit www.lumex.com.

Table 2–27. LCD Pin Definitions and Functions

Pin Number	Symbol	Level	Function	
1	V_{DD}	—	Power supply	5 V
2	V_{SS}	—		GND (0 V)
3	V_0	—		For LCD drive
4	RS	H/L	Register select signal H: Data input L: Instruction input	
5	R/W	H/L	H: Data read (module to MPU) L: Data write (MPU to module)	
6	E	H, H to L	Enable	
7–14	DB0–DB7	H/L	Data bus, software selectable 4-bit or 8-bit mode	

The particular model used does not have a backlight and the LCD drive pin is not connected to the power pin for maximum pixel drive.

Table 2–28 lists the LCD component references and the manufacturing information.

Table 2–28. LCD Component References and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
J13	2×7 pin, 100 mil, vertical header	Samtec	TSM-107-07-G-D	www.samtec.com
	2×16 character display, 5×8 dot matrix	Lumex Inc.	LCM-S01602DSR/C	www.lumex.com

Components and Transceiver Interfaces

This section describes the development board's communication ports and interface cards relative to the Cyclone IV GX device. The development board supports the following communication ports:

- PCIe
- 10/100/1000 Ethernet
- HSMC

PCIe

The Cyclone IV GX FPGA development board fits entirely into a PC motherboard with a ×4 PCIe slot which can accommodate a short-form PCIe add-in card. The development board comes with a full height I/O bracket for its low profile form factor card. This interface uses the Cyclone IV GX device's PCIe hard IP block in ×4 lane configuration, saving logic resources for the user logic application.

For more information on using the PCIe hard IP block, refer to the *PCI Express Compiler User Guide*.

The PCIe interface supports a channel width of ×4 as well as the connection speed of Gen1 at 2.5 Gbps/lane.

The board's power can be sourced entirely from the PCIe edge connector when installed into a PC motherboard. Turn the power switch (SW3) to the ON position when you install the board into a PC motherboard. Although the board can also be powered by a laptop power supply for use on a lab bench, it is not recommended to use from both supplies at the same time. Ideal diode power sharing devices have been designed into this board to prevent damages or back-current from one supply to the other.

The PCIE_REFCLK_P and PCIE_REFCLK_N signals are a 100-MHz differential input that is driven from the PC motherboard onto this board through the PCIe edge connector. This signal connects directly to a Cyclone IV GX REFCLK input pin pair. This clock is terminated on the motherboard and therefore, no on-board termination is required. This clock can have spread-spectrum properties that change its period between 9.847 ps to 10.203 ps. The I/O standard is High-Speed Current Steering Logic (HCSL).

PCIe signals and HSMC Port B XCVR signals are muxed via resistors and capacitors. By default, the XCVR_RX_P and XCVR_RX_N channels of the FPGA are connected to the PCIE_RX_P and PCIE_RX_N signals, while the XCVR_TX_P and XCVR_TX_N channels are connected to the PCIE_TX_P and PCIE_TX_N signals.

Table 2–29 summarizes the PCIe pin assignments. The signal names and directions are relative to the Cyclone IV GX FPGA.

Table 2–29. PCIe Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
J14.A16	Add-in card transmit bus	PCIE_TX_P0	1.5-V PCML (2)	AB4 (1)
J14.A17	Add-in card transmit bus	PCIE_TX_N0		AB3 (1)
J14.A21	Add-in card transmit bus	PCIE_TX_P1		Y4 (1)
J14.A22	Add-in card transmit bus	PCIE_TX_N1		Y3 (1)
J14.A25	Add-in card transmit bus	PCIE_TX_P2		V4 (1)
J14.A26	Add-in card transmit bus	PCIE_TX_N2		V3 (1)
J14.A29	Add-in card transmit bus	PCIE_TX_P3		T4 (1)
J14.A30	Add-in card transmit bus	PCIE_TX_N3		T3 (1)
J14.B14	Add-in card receive bus	PCIE_RX_P0		AC2 (1)
J14.B15	Add-in card receive bus	PCIE_RX_N0		AC1 (1)
J14.B19	Add-in card receive bus	PCIE_RX_P1		AA2 (1)
J14.B20	Add-in card receive bus	PCIE_RX_N1		AA1 (1)
J14.B23	Add-in card receive bus	PCIE_RX_P2		W2 (1)
J14.B24	Add-in card receive bus	PCIE_RX_N2		W1 (1)
J14.B27	Add-in card receive bus	PCIE_RX_P3		U2 (1)
J14.B28	Add-in card receive bus	PCIE_RX_N3		U1 (1)
J14.A13	Motherboard reference clock	PCIE_REFCLK_P	HCSL	V15
J14.A14	Motherboard reference clock	PCIE_REFCLK_N		W15
J14.A11	Reset	PCIE_T_PERSTn	LVTTL	A7
J14.B5	SMB clock	PCIE_T_SMBCLK		F15
J14.B6	SMB data	PCIE_T_SMBDAT		E12
J14.B11	Wake signal	PCIE_WAKEn_R		—
J14.B17	x1 Present	PCIE_PRSNT2n_x1	—	—
J14.B31	x4 Present	PCIE_PRSNT2n_x4	—	—
J14.A5	Motherboard TCK	PCIE_JTAG_TCK	3.3-V	—
J14.A6	Motherboard TDI	PCIE_JTAG_TDI		—
J14.A7	Motherboard TDO	PCIE_JTAG_TDO		—
J14.A8	Motherboard TMS	PCIE_JTAG_TMS		—

Notes to Table 2–29:

(1) This signal is multiplexed with the signal on HSMC port B interface.

(2) The Quartus II version 10.1sp1 and newer only support an I/O standard of 1.5-V PCML for the PCI Express transmitter as stated in Altera's knowledge base webpage—solution ID rd12272010_575.

10/100/1000 Ethernet

A Marvell 88E1111 PHY device is used for 10/100/1000 BASE-T Ethernet connection. The device is an auto-negotiating Ethernet PHY with an RGMII interface to the FPGA. The MAC function must be provided in the FPGA for typical networking applications such the Altera Triple Speed Ethernet MegaCore design. The Marvell 88E1111 PHY uses 2.5-V and 1.1-V power rails and requires a 25-MHz reference clock driven from a dedicated oscillator. The device interfaces to a Halo Electronics HFJ11-1G02E model RJ45 with internal magnetics that can be used for driving copper lines with Ethernet traffic.

The PHY address on the management data input/output (MDIO) bus is 0b10010 = 0x12.

Figure 2–6 shows the RGMII interface between the FPGA (MAC) and Marvell 88E1111 PHY.

Figure 2–6. SGMII Interface between FPGA (MAC) and Marvell 88E1111 PHY

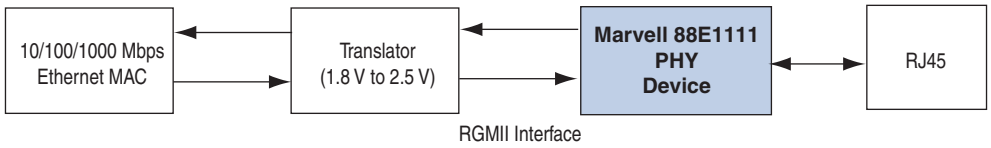


Table 2–30 lists the Ethernet PHY interface pin assignments.

Table 2–30. Ethernet PHY Pin Assignments, Signal Names and Functions

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
U21.11	RGMII TX data	ENET_T_TX_D0	1.8-V CMOS	G10
U21.12	RGMII TX data	ENET_T_TX_D1		E3
U21.13	RGMII TX data	ENET_T_TX_D2		D10
U21.14	RGMII TX data	ENET_T_TX_D3		B10
U21.8	RGMII TX clock	ENET_T_GTX_CLK		D9
U21.9	RGMII TX control	ENET_T_TX_EN		A27
U21.95	RGMII RX data	ENET_T_RX_D0		F5
U21.92	RGMII RX data	ENET_T_RX_D1		B9
U21.93	RGMII RX data	ENET_T_RX_D2		G14
U21.91	RGMII RX data	ENET_T_RX_D3		E13
U21.2	RGMII RX clock	ENET_T_RX_CLK		B15
U21.94	RGMII RX data valid	ENET_T_RX_DV		E15
U21.25	Management bus control	ENET_T_MDC		K21
U21.24	Management bus data	ENET_T_MDIO		G7
U21.23	Management bus interrupt	ENET_T_INTN		A11
U21.28	Device reset	ENET_T_RESETn		D6
U21.68	RX data active LED	ENET_LED_TX		—
U21.69	TX data active LED	ENET_LED_RX		—
U21.76	10 Mbps connection speed LED	ENET_LED_LINK10		—
U21.74	100 Mbps connection speed LED	ENET_LED_LINK100	1.8-V CMOS	—
U21.73	1000 Mbps connection speed LED	ENET_LED_LINK1000		—
U21.70	Duplex or collision LED	ENET_LED_DUPLEX		—

Table 2–31 lists the Ethernet PHY interface component reference and manufacturing information.

Table 2–31. Ethernet PHY Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U21	Ethernet PHY BASE-T device	Marvell Semiconductor	88E1111-B2-CAAIC000	www.marvell.com

Transceiver Connector (Optional)

The HSMC port B interface (J2) uses the same transceivers as the PCIe interface. A capacitor or resistor stuffing option is used to select the transceivers for either the PCIe or the HSMC port B interface. The default stuffing option is the PCIe interface.

Table 2–32 lists the capacitor or resistor stuffing option to enable either the PCIe interface or the HSMC port B interface. The multiplexer capacitors are 0.1 µF and the multiplexer resistors are 0 Ω.

Table 2–32. Multiplexer Location for PCIe Interface and HSMC Port B Interface

Selection	Multiplexer Location
PCIe interface	Populate C324, C326, C328, C330, C341, C343, C345, C347, R80, R81, R84, R86, R88, R89, R92, R96
HSMC port B interface	Populate C323, C325, C327, C329, C340, C342, C344, C346, R82, R83, R85, R87, R90, R91, R93, R97

High-Speed Mezzanine Cards

The development board contains two HSMC interfaces—port A and port B. The HSMC port A interface supports both single-ended and differential signaling while the HSMC port B interface only supports single-ended signaling. The HSMC interface also allows JTAG, SMB, clock outputs and inputs, as well as power for compatible HSMC cards. The HSMC is an Altera-developed open specification, which allows you to expand the functionality of the development board through the addition of daughtercards.

For more information about the HSMC specification such as signaling standards, signal integrity, compatible connectors, and mechanical information, refer to the *High Speed Mezzanine Card (HSMC) Specification* manual.

The HSMC connector has a total of 172 pins, including 120 signal pins, 39 power pins, and 13 ground pins. The ground pins are located between the two rows of signal and power pins, acting both as a shield and a reference. The HSMC host connector is based on the 0.5 mm-pitch QSH/QTH family of high-speed, board-to-board connectors from Samtec. There are three banks in this connector. Bank 1 has every third pin removed as done in the QSH-DP/QTH-DP series. Bank 2 and bank 3 have all the pins populated as done in the QSH/QTH series.

The HSMC port A interface has programmable bi-directional I/O pins that can be used as 2.5-V LVCMOS, which is 3.3-V LVTTL-compatible. These pins can also be used as various differential I/O standards including, but not limited to, LVDS, mini-LVDS, and RSDS with up to 17 full-duplex channels. The HSMC port B interface is translated from 1.8 V (on the FPGA) to 2.5 V (on the HSMC connector) using a bidirectional voltage translator.

As noted in the *High Speed Mezzanine Card (HSMC) Specification* manual, LVDS and single-ended I/O standards are only guaranteed to function when mixed according to either the generic single-ended pin-out or generic differential pin-out.

Table 2–33 lists the HSMC port A interface pin assignments, signal names, and functions.

Table 2–33. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
J1.17	Transceiver TX bit 3	HSMA_TX_P3	1.5 V	H4
J1.19	Transceiver TX bit 3n	HSMA_TX_N3		H3
J1.18	Transceiver RX bit 3	HSMA_RX_P3		J2
J1.20	Transceiver RX bit 3n	HSMA_RX_N3		J1
J1.21	Transceiver TX bit 2	HSMA_TX_P2		K4
J1.23	Transceiver TX bit 2n	HSMA_TX_N2		K3
J1.22	Transceiver RX bit 2	HSMA_RX_P2		L2
J1.24	Transceiver RX bit 2n	HSMA_RX_N2		L1
J1.25	Transceiver TX bit 1	HSMA_TX_P1		M4
J1.27	Transceiver TX bit 1n	HSMA_TX_N1		M3
J1.26	Transceiver RX bit 1	HSMA_RX_P1		N2
J1.28	Transceiver RX bit 1n	HSMA_RX_N1		N1
J1.29	Transceiver TX bit 0	HSMA_TX_P0		P4
J1.31	Transceiver TX bit 0n	HSMA_TX_N0		P3
J1.30	Transceiver RX bit 0	HSMA_RX_P0		R2
J1.32	Transceiver RX bit 0n	HSMA_RX_N0	2.5-V	R1
J1.33	Management serial data	HSMA_T_SDA		C25
J1.34	Management serial clock	HSMA_T_SCL		B24
J1.35	JTAG clock signal	JTAG_TCK		F2
J1.36	JTAG mode select signal	JTAG_TMS		E1
J1.37	JTAG data output	HSMA_JTAG_TDO		—
J1.38	JTAG data input	HSMA_JTAG_TDI	2.5-V	—
J1.39	Dedicated CMOS clock out	HSMA_CLK_OUT0		—
J1.40	Dedicated CMOS clock in	HSMA_CLK_IN0		—
J1.41	Dedicated CMOS I/O bit 0	HSMA_D0		AC27
J1.42	Dedicated CMOS I/O bit 1	HSMA_D1		Y27
J1.43	Dedicated CMOS I/O bit 2	HSMA_D2		AF30
J1.44	Dedicated CMOS I/O bit 3	HSMA_D3		AD27

Table 2–33. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
J1.47	LVDS TX bit 0 or CMOS bit 4	HSMA_TX_D_P0	LVDS or 2.5-V or 1.8-V	C29
J1.48	LVDS RX bit 0 or CMOS bit 5	HSMA_RX_D_P0		D29
J1.49	LVDS TX bit 0n or CMOS bit 6	HSMA_TX_D_N0		C30
J1.50	LVDS RX bit 0n or CMOS bit 7	HSMA_RX_D_N0		D30
J1.53	LVDS TX bit 1 or CMOS bit 8	HSMA_TX_D_P1		E27
J1.54	LVDS RX bit 1 or CMOS bit 9	HSMA_RX_D_P1		G26
J1.55	LVDS TX bit 1n or CMOS bit 10	HSMA_TX_D_N1		E28
J1.56	LVDS RX bit 1n or CMOS bit 11	HSMA_RX_D_N1		G27
J1.59	LVDS TX bit 2 or CMOS bit 12	HSMA_TX_D_P2		F26
J1.60	LVDS RX bit 2 or CMOS bit 13	HSMA_RX_D_P2		N24
J1.61	LVDS TX bit 2n or CMOS bit 14	HSMA_TX_D_N2		F27
J1.62	LVDS RX bit 2n or CMOS bit 15	HSMA_RX_D_N2		M25
J1.65	LVDS TX bit 3 or CMOS bit 16	HSMA_TX_D_P3		F30
J1.66	LVDS RX bit 3 or CMOS bit 17	HSMA_RX_D_P3		N25
J1.67	LVDS TX bit 3n or CMOS bit 18	HSMA_TX_D_N3		E30
J1.68	LVDS RX bit 3n or CMOS bit 19	HSMA_RX_D_N3		M26
J1.71	LVDS TX bit 4 or CMOS bit 20	HSMA_TX_D_P4		F28
J1.72	LVDS RX bit 4 or CMOS bit 21	HSMA_RX_D_P4		R24
J1.73	LVDS TX bit 4n or CMOS bit 22	HSMA_TX_D_N4		F29
J1.74	LVDS RX bit 4n or CMOS bit 23	HSMA_RX_D_N4		P25
J1.77	LVDS TX bit 5 or CMOS bit 24	HSMA_TX_D_P5		H30
J1.78	LVDS RX bit 5 or CMOS bit 25	HSMA_RX_D_P5		N27
J1.79	LVDS TX bit 5n or CMOS bit 26	HSMA_TX_D_N5		G30
J1.80	LVDS RX bit 5n or CMOS bit 27	HSMA_RX_D_N5		N28
J1.83	LVDS TX bit 6 or CMOS bit 28	HSMA_TX_D_P6		G28
J1.84	LVDS RX bit 6 or CMOS bit 29	HSMA_RX_D_P6		M29
J1.85	LVDS TX bit 6n or CMOS bit 30	HSMA_TX_D_N6		G29
J1.86	LVDS RX bit 6n or CMOS bit 31	HSMA_RX_D_N6		M30
J1.89	LVDS TX bit 7 or CMOS bit 32	HSMA_TX_D_P7		J29
J1.90	LVDS RX bit 7 or CMOS bit 33	HSMA_RX_D_P7		N29
J1.91	LVDS TX bit 7n or CMOS bit 34	HSMA_TX_D_N7		J30

Table 2–33. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
J1.92	LVDS RX bit 7n or CMOS bit 35	HSMA_RX_D_N7	LVDS or 2.5-V or 1.8-V	N30
J1.95	LVDS or CMOS clock out 1 or CMOS bit 36	HSMA_CLK_OUT_P1		P21
J1.96	LVDS or CMOS clock in 1 or CMOS bit 37	HSMA_CLK_IN_P1		T29
J1.97	LVDS or CMOS clock out 1 or CMOS bit 38	HSMA_CLK_OUT_N1		N21
J1.98	LVDS or CMOS clock in 1 or CMOS bit 39	HSMA_CLK_IN_N1		T30
J1.101	LVDS TX bit 8 or CMOS bit 40	HSMA_TX_D_P8		L30
J1.102	LVDS RX bit 8 or CMOS bit 41	HSMA_RX_D_P8		P27
J1.103	LVDS TX bit 8n or CMOS bit 42	HSMA_TX_D_N8		K30
J1.104	LVDS RX bit 8n or CMOS bit 43	HSMA_RX_D_N8		P28
J1.107	LVDS TX bit 9 or CMOS bit 44	HSMA_TX_D_P9		J28
J1.108	LVDS RX bit 9 or CMOS bit 45	HSMA_RX_D_P9		R30
J1.109	LVDS TX bit 9n or CMOS bit 46	HSMA_TX_D_N9		H28
J1.110	LVDS RX bit 9n or CMOS bit 47	HSMA_RX_D_N9		P30
J1.113	LVDS TX bit 10 or CMOS bit 48	HSMA_TX_D_P10		J27
J1.114	LVDS RX bit 10 or CMOS bit 49	HSMA_RX_D_P10		R27
J1.115	LVDS TX bit 10n or CMOS bit 50	HSMA_TX_D_N10		H27
J1.116	LVDS RX bit 10n or CMOS bit 51	HSMA_RX_D_N10		R28
J1.119	LVDS TX bit 11 or CMOS bit 52	HSMA_TX_D_P11		L27
J1.120	LVDS RX bit 11 or CMOS bit 53	HSMA_RX_D_P11		T28
J1.121	LVDS TX bit 11n or CMOS bit 54	HSMA_TX_D_N11		L28
J1.122	LVDS RX bit 11n or CMOS bit 55	HSMA_RX_D_N11		R29
J1.125	LVDS TX bit 12 or CMOS bit 56	HSMA_TX_D_P12		M27
J1.126	LVDS RX bit 12 or CMOS bit 57	HSMA_RX_D_P12		R25
J1.127	LVDS TX bit 12n or CMOS bit 58	HSMA_TX_D_N12		M28
J1.128	LVDS RX bit 12n or CMOS bit 59	HSMA_RX_D_N12		R26
J1.131	LVDS TX bit 13 or CMOS bit 60	HSMA_TX_D_P13		K26
J1.132	LVDS RX bit 13 or CMOS bit 61	HSMA_RX_D_P13		T26
J1.133	LVDS TX bit 13n or CMOS bit 62	HSMA_TX_D_N13		K27
J1.134	LVDS RX bit 13n or CMOS bit 63	HSMA_RX_D_N13		T27
J1.137	LVDS TX bit 14 or CMOS bit 64	HSMA_TX_D_P14		K25
J1.138	LVDS RX bit 14 or CMOS bit 65	HSMA_RX_D_P14		U25
J1.139	LVDS TX bit 14n or CMOS bit 66	HSMA_TX_D_N14		J26
J1.140	LVDS RX bit 14n or CMOS bit 67	HSMA_RX_D_N14		T25
J1.143	LVDS TX bit 15 or CMOS bit 68	HSMA_TX_D_P15		J25
J1.144	LVDS RX bit 15 or CMOS bit 69	HSMA_RX_D_P15		T23
J1.145	LVDS TX bit 15n or CMOS bit 70	HSMA_TX_D_N15		H25
J1.146	LVDS RX bit 15n or CMOS bit 71	HSMA_RX_D_N15		T24
J1.149	LVDS TX bit 16 or CMOS bit 72	HSMA_TX_D_P16		M21

Table 2–33. HSMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 4)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
J1.150	LVDS RX bit 16 or CMOS bit 73	HSMA_RX_D_P16	LVDS or 2.5-V or 1.8-V	U21
J1.151	LVDS TX bit 16n or CMOS bit 74	HSMA_TX_D_N16		M22
J1.152	LVDS RX bit 16n or CMOS bit 75	HSMA_RX_D_N16		T21
J1.155	LVDS or CMOS clock out 2 or CMOS bit 76	HSMA_CLK_OUT_P2		K28
J1.156	LVDS or CMOS clock in 2 or CMOS bit 77	HSMA_CLK_IN_P2		V29
J1.157	LVDS or CMOS clock out 2 or CMOS bit 78	HSMA_CLK_OUT_N2		K29
J1.158	LVDS or CMOS clock in 2 or CMOS bit 79	HSMA_CLK_IN_N2		V30
J1.160	HSMC Port A presence detect	HSMA_PSNTn	2.5-V	A25
D4	User LED to show RX data activity on HSMC Port A	HSMA_RX_LED		C24
D3	User LED to show TX data activity on HSMC Port A	HSMA_TX_LED		D25

Table 2–34 lists the HSMC port B interface pin assignments, signal names, and functions.

Table 2–34. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 5)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number	Other Connections
J2.17	Transceiver TX bit 3	HSMB_TX_P3	1.5-V	—	C329.1
J2.18	Transceiver RX bit 3	HSMB_RX_P3		—	R97.2
J2.19	Transceiver TX bit 3n	HSMB_TX_N3		—	C346.1
J2.20	Transceiver RX bit 3n	HSMB_RX_N3		—	R101.2
J2.21	Transceiver TX bit 2	HSMB_TX_P2		—	C327.1
J2.22	Transceiver RX bit 2	HSMB_RX_P2		—	R94.2
J2.23	Transceiver TX bit 2n	HSMB_TX_N2		—	C344.1
J2.24	Transceiver RX bit 2n	HSMB_RX_N2		—	R95.2
J2.25	Transceiver TX bit 1	HSMB_TX_P1		—	C325.1
J2.26	Transceiver RX bit 1	HSMB_RX_P1		—	R89.2
J2.27	Transceiver TX bit 1n	HSMB_TX_N1		—	C342.1
J2.28	Transceiver RX bit 1n	HSMB_RX_N1		—	R91.2
J2.29	Transceiver TX bit 0	HSMB_TX_P0		—	C323.1
J2.30	Transceiver RX bit 0	HSMB_RX_P0		—	R86.2
J2.31	Transceiver TX bit 0n	HSMB_TX_N0		—	C340.1
J2.32	Transceiver RX bit 0n	HSMB_RX_N0		—	R87.2
J2.33	Management serial data	HSMB_T_SDA	2.5-V	—	U39.1
J2.34	Management serial clock	HSMB_T_SCL		—	U39.8
J2.37	JTAG data output	HSMB_JTAG_TDO		—	U2.5
J2.38	JTAG data input	HSMB_JTAG_TDI		—	U1.9; U2.2

Table 2–34. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 5)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number	Other Connections
J2.39	Dedicated CMOS clock out	HSMB_CLK_OUT0	2.5-V	AA22	—
J2.40	Dedicated CMOS clock in	HSMB_CLK_IN0		—	U30.4
J2.41	Dedicated CMOS I/O bit 0	HSMB_D0		AH29	—
J2.42	Dedicated CMOS I/O bit 1	HSMB_D1		AE30	—
J2.43	Dedicated CMOS I/O bit 2	HSMB_D2		AD29	—
J2.44	Dedicated CMOS I/O bit 3	HSMB_D3		AG29	—
J2.47	CMOS bit 4	HSMB_TX_D_P0		AB28	—
J2.48	CMOS bit 5	HSMB_RX_D_P0		AB30	—
J2.49	CMOS bit 6	HSMB_TX_D_N0		AC30	—
J2.50	CMOS bit 7	HSMB_RX_D_N0		AA28	—
J2.53	CMOS bit 8	HSMB_TX_D_P1		Y28	—
J2.54	CMOS bit 9	HSMB_RX_D_P1		AA27	—
J2.55	CMOS bit 10	HSMB_TX_D_N1		AA26	—
J2.56	CMOS bit 11	HSMB_RX_D_N1		AD30	—
J2.59	CMOS bit 12	HSMB_TX_D_P2		AC28	—
J2.60	CMOS bit 13	HSMB_RX_D_P2		AB27	—
J2.61	CMOS bit 14	HSMB_TX_D_N2		AB26	—
J2.62	CMOS bit 15	HSMB_RX_D_N2		AB25	—
J2.65	CMOS bit 16	HSMB_TX_D_P3		AG30	—
J2.66	CMOS bit 17	HSMB_RX_D_P3		AE28	—
J2.67	CMOS bit 18	HSMB_TX_D_N3		V21	—
J2.68	CMOS bit 19	HSMB_RX_D_N3		AD26	—
J2.71	CMOS bit 20	HSMB_TX_D_P4		AF28	—
J2.72	CMOS bit 21	HSMB_RX_D_P4		AC25	—
J2.73	CMOS bit 22	HSMB_TX_D_N4		AE27	—
J2.74	CMOS bit 23	HSMB_RX_D_N4		AD25	—
J2.77	CMOS bit 24	HSMB_TX_D_P5		AE26	—
J2.78	CMOS bit 25	HSMB_RX_D_P5		AJ30	—
J2.79	CMOS bit 26	HSMB_TX_D_N5		AE25	—
J2.80	CMOS bit 27	HSMB_RX_D_N5		Y22	—
J2.83	CMOS bit 28	HSMB_T_TX_D_P6		—	U36.12
J2.84	CMOS bit 29	HSMB_T_RX_D_P6		—	U38.17
J2.85	CMOS bit 30	HSMB_T_TX_D_N6		—	U36.13
J2.86	CMOS bit 31	HSMB_T_RX_D_N6		—	U38.16
J2.89	CMOS bit 32	HSMB_T_TX_D_P7		—	U36.14
J2.90	CMOS bit 33	HSMB_T_RX_D_P7		—	U38.15
J2.91	CMOS bit 34	HSMB_T_TX_D_N7		—	U36.15
J2.92	CMOS bit 35	HSMB_T_RX_D_N7		—	U38.12

Table 2–34. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 5)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number	Other Connections
J2.95	CMOS clock out 1 or CMOS bit 36	HSMB_CLK_OUT_P1	2.5-V	AA25	—
J2.96	CMOS clock in 1 or CMOS bit 37	HSMB_CLK_IN_P1		W30	R167.1
J2.97	CMOS clock out 1 or CMOS bit 38	HSMB_CLK_OUT_N1		AH30	—
J2.98	CMOS clock in 1 or CMOS bit 39	HSMB_CLK_IN_N1		W29	R167.2
J2.101	CMOS bit 40	HSMB_T_TX_D_P8		—	U36.16
J2.102	CMOS bit 41	HSMB_T_RX_D_P8		—	U37.15
J2.103	CMOS bit 42	HSMB_T_TX_D_N8			U35.14
J2.104	CMOS bit 43	HSMB_T_RX_D_N8			U38.13
J2.107	CMOS bit 44	HSMB_T_TX_D_P9		—	U35.17
J2.108	CMOS bit 45	HSMB_T_RX_D_P9		—	U37.16
J2.109	CMOS bit 46	HSMB_TX_D_N9		AD28	—
J2.110	CMOS bit 47	HSMB_T_RX_D_N9			U37.17
J2.113	CMOS bit 48	HSMB_T_TX_D_P10		—	U36.17
J2.114	CMOS bit 49	HSMB_T_RX_D_P10			U37.18
J2.115	CMOS bit 50	HSMB_T_TX_D_N10			U35.18
J2.116	CMOS bit 51	HSMB_T_RX_D_N10		—	U38.14
J2.119	CMOS bit 52	HSMB_T_TX_D_P11		—	U29.13
J2.120	CMOS bit 53	HSMB_T_RX_D_P11		—	U37.19
J2.121	CMOS bit 54	HSMB_T_TX_D_N11		—	U29.14
J2.122	CMOS bit 55	HSMB_T_RX_D_N11		—	U37.14
J2.125	CMOS bit 56	HSMB_T_TX_D_P12		—	U36.19
J2.126	CMOS bit 57	HSMB_T_RX_D_P12		—	U37.13
J2.127	CMOS bit 58	HSMB_T_TX_D_N12		—	U29.15
J2.128	CMOS bit 59	HSMB_T_RX_D_N12		—	U38.18
J2.131	CMOS bit 60	HSMB_T_TX_D_P13		—	U29.16
J2.132	CMOS bit 61	HSMB_T_RX_D_P13		—	U29.12
J2.133	CMOS bit 62	HSMB_T_TX_D_N13		—	U35.19
J2.134	CMOS bit 63	HSMB_T_RX_D_N13		—	U29.17
J2.137	CMOS bit 64	HSMB_T_TX_D_P14		—	U35.13
J2.138	CMOS bit 65	HSMB_T_RX_D_P14		—	U28.15
J2.139	CMOS bit 66	HSMB_T_TX_D_N14		—	U35.16
J2.140	CMOS bit 67	HSMB_T_RX_D_N14		AF18	U38.19
J2.143	CMOS bit 68	HSMB_T_TX_D_P15		—	U35.15
J2.144	CMOS bit 69	HSMB_T_RX_D_P15		—	U28.16
J2.145	CMOS bit 70	HSMB_T_TX_D_N15		—	U28.19
J2.146	CMOS bit 71	HSMB_T_RX_D_N15		—	U28.17
J2.149	CMOS bit 72	HSMB_T_TX_D_P16		—	U35.12
J2.150	CMOS bit 73	HSMB_T_RX_D_P16		—	U28.18

Table 2–34. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 5)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number	Other Connections
J2.151	CMOS bit 74	HSMB_T_TX_D_N16	2.5-V	—	U36.18
J2.152	CMOS bit 75	HSMB_T_RX_D_N16		—	U37.12
J2.155	CMOS bit 76	HSMB_T_CLK_OUT_P2		—	U34.3
J2.156	CMOS bit 77	HSMBT_CLK_IN_P2		—	U33.4
J2.157	CMOS bit 78	HSMB_CLK_OUT_N2		Y25	—
J2.158	CMOS clock in 2 or CMOS bit 79	HSMB_CLK_IN_N2		V28	—
J2.160	HSMC Port B presence detect	HSMB_PSNTn		C26	U7.H2;R2.1
D6	User LED to show RX data activity on HSMC Port B	HSMB_RX_LED		C10	D6.2
D5	User LED to show TX data activity on HSMC Port B	HSMB_TX_LED		D25	D5.2
—	—	HSMAT_CLK_IN0		A15	U32.3
—	Dedicated CMOS clock in	HSMB_CLK_IN_P2	1.8-V	AG22	U33.3
—	Dedicated CMOS clock out	HSMB_CLK_OUT_P2		AG19	U34.4
—	—	HSMB_RX_D_N6		AE19	U38.5
—	—	HSMB_RX_D_N7		AJ25	U38.9
—	—	HSMB_RX_D_N8		Y20	U38.8
—	—	HSMB_RX_D_N9		AE17	U37.4
—	—	HSMB_RX_D_N10		AA20	U38.7
—	—	HSMB_RX_D_N11		AK19	U37.7
—	—	HSMB_RX_D_N12		AG20	U38.3
—	—	HSMB_RX_D_N13		AD10	U29.4
—	—	HSMB_RX_D_N14		AF18	U38.2
—	—	HSMB_RX_D_N15		AG3	U28.4
—	—	HSMB_RX_D_N16		AD16	U37.9
—	—	HSMB_RX_D_P6		AE20	U38.4
—	—	HSMB_RX_D_P7		AG23	U38.6
—	—	HSMB_RX_D_P8		AK20	U37.6
—	—	HSMB_RX_D_P9		AJ19	U37.5
—	—	HSMB_RX_D_P10		AE16	U37.3
—	—	HSMB_RX_D_P11		AG17	U37.2
—	—	HSMB_RX_D_P12		AG18	U37.8
—	—	HSMB_RX_D_P13		AG16	U29.9
—	—	HSMB_RX_D_P14		AH3	U28.6
—	—	HSMB_RX_D_P15		AK13	U28.5
—	Management serial data	HSMB_SCL		K22	U39.5
—	Management serial clock	HSMB_SDA		F10	U39.4

Table 2–34. HSMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 5 of 5)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number	Other Connections
—	—	HSMB_RX_D_P16	1.8-V	D3	U28.3
—	—	HSMB_TX_D_N6		AH28	U36.8
—	—	HSMB_TX_D_N7		AJ27	U36.6
—	—	HSMB_TX_D_N8		AH22	U35.7
—	—	HSMB_TX_D_N10		AH21	U35.3
—	—	HSMB_TX_D_N11		AF7	U29.7
—	—	HSMB_TX_D_N12		AF9	U29.6
—	—	HSMB_TX_D_N13		AJ21	U35.2
—	—	HSMB_TX_D_N14		AF22	U35.5
—	—	HSMB_TX_D_N15		AK6	U28.2
—	—	HSMB_TX_D_N16		AH25	U36.3
—	—	HSMB_TX_D_P6		AG28	U36.9
—	—	HSMB_TX_D_P7		AJ28	U36.7
—	—	HSMB_TX_D_P8		AG26	U36.5
—	—	HSMB_TX_D_P9		AJ22	U35.4
—	—	HSMB_TX_D_P10		AH26	U36.4
—	—	HSMB_TX_D_P11		AK21	U29.8
—	—	HSMB_TX_D_P12		AE23	U36.2
—	—	HSMB_TX_D_P13		AF10	U29.5
—	—	HSMB_TX_D_P14		AK24	U35.8
—	—	HSMB_TX_D_P15		AD22	U35.6
—	—	HSMB_TX_D_P16		AF25	U35.9
—	—	HSMBT_CLK_IN0		AJ16	U30.3

Table 2–35 lists the signals that multiplex between the PCIe and the HSMB transceivers.

Table 2–35. HSMC Port B Transceiver and PCIe Signals (Part 1 of 2)

HSMC Port B Transceiver Signal	PCIe Signal	Cyclone IV GX Device Pin Number
HSMB_RX_N0	XCVR_RX_N0	AC1
HSMB_RX_N1	XCVR_RX_N1	AA1
HSMB_RX_N2	XCVR_RX_N2	W1
HSMB_RX_N3	XCVR_RX_N3	U1
HSMB_RX_P0	XCVR_RX_P0	AC2
HSMB_RX_P1	XCVR_RX_P1	AA2
HSMB_RX_P2	XCVR_RX_P2	W2
HSMB_RX_P3	XCVR_RX_P3	U2
HSMB_TX_N0	XCVR_TX_N0	AB3

Table 2–35. HSMC Port B Transceiver and PCIe Signals (Part 2 of 2)

HSMC Port B Transceiver Signal	PCIe Signal	Cyclone IV GX Device Pin Number
HSMB_TX_N1	XCVR_TX_N1	Y3
HSMB_TX_N2	XCVR_TX_N2	V3
HSMB_TX_N3	XCVR_TX_N3	T3
HSMB_TX_P0	XCVR_TX_P0	AB4
HSMB_TX_P1	XCVR_TX_P1	Y4
HSMB_TX_P2	XCVR_TX_P2	V4
HSMB_TX_P3	XCVR_TX_P3	T4

Table 2–36 lists the HSMC connector component reference and manufacturing information.

Table 2–36. HSMC Connector Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
J1 and J2	HSMC, custom version of QSH-DP family high-speed socket.	Samtec	ASP-122953-01	www.samtec.com

Memory

This section describes the board's memory interface support and also their signal names, types, and connectivity relative to the Cyclone IV GX device. The board has the following memory interfaces:

- DDR2 SDRAM
- SSRAM
- Flash

DDR2 SDRAM

There are four DDR2 devices, providing 256 MB of memory for each on-board DDR2 SDRAM device. Each device interface has a 16-bit data bus, which can be configured to run individually or together as a 32-bit data bus.

Two DDR2 devices are pinned out to FPGA bank 3 and 4 (bottom port) while another two are pinned out to FPGA bank 7 and 8 (top port). These memory interfaces are designed to run at a maximum frequency of 167 MHz for a maximum theoretical bandwidth of over 10.6 Gbps. The internal bus in the FPGA is typically 2 or 4 times the width at full rate or half rate respectively. For example, a 167 MHz 16-bit interface becomes a 83.5 MHz 64-bit bus.

DDR2 SDRAM Top Port

The DDR2 SDRAM top port consists of two DDR2 devices (U8 and U15). Table 2–37 lists the DDR2 top port pin assignments, signal names, and its functions. The signal names and types are relative to the Cyclone IV GX device in terms of I/O setting and direction.

Table 2–37. DDR2 SDRAM Top Port Pin Assignments, Signal Names and Functions (Part 1 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
U8.R2, U15.R2	Address bus	DDR2A_A12	1.8-V SSTL Class I	F21
U8.P7, U15.P7	Address bus	DDR2A_A11		G18
U8.M2, U15.M2	Address bus	DDR2A_A10		C20
U8.P3, U15.P3	Address bus	DDR2A_A9		F20
U8.P8, U15.P8	Address bus	DDR2A_A8		K17
U8.P2, U15.P2	Address bus	DDR2A_A7		B22
U8.N7, U15.N7	Address bus	DDR2A_A6		F17
U8.N3, U15.N3	Address bus	DDR2A_A5		B21
U8.N8, U15.N8	Address bus	DDR2A_A4		F18
U8.N2, U15.N2	Address bus	DDR2A_A3		A21
U8.M7, U15.M7	Address bus	DDR2A_A2		D17
U8.M3, U15.M3	Address bus	DDR2A_A1		C19
U8.M8, U15.M8	Address bus	DDR2A_A0		D18
U8.L3, U15.L3	Bank address bus	DDR2A_BA1		B19
U8.L2, U15.L2	Bank address bus	DDR2A_BA0		A20
U8.K7, U15.K7	Row address select	DDR2A_RASn		B18
U8.L7, U15.L7	Column address select	DDR2A_CASn		A16
U8.L8, U15.L8	Chip select	DDR2A_CSn		D20
U8.K3, U15.K3	Write enable	DDR2A_WEn		A18
U8.K9, U15.K9	Termination enable	DDR2A_ODT		C17
U8.K2, U15.K2	Clock enable	DDR2A_CKE		A19
U8.J8, U15.J8	Clock P	DDR2A_CLK_P		D23
U8.K8, U15.K8	Clock N	DDR2A_CLK_N		C23
U8.G8,	Data bus byte lane 0	DDR2A_DQ0		G23
U8.G2	Data bus byte lane 0	DDR2A_DQ1		D28
U8.H7	Data bus byte lane 0	DDR2A_DQ2		G24
U8.H3	Data bus byte lane 0	DDR2A_DQ3		C28
U8.H1	Data bus byte lane 0	DDR2A_DQ4		H24
U8.H9	Data bus byte lane 0	DDR2A_DQ5		F23
U8.F1	Data bus byte lane 0	DDR2A_DQ6		B30
U8.F9	Data bus byte lane 0	DDR2A_DQ7		F22
U8.F3	Write mask byte lane 0	DDR2A_DM0		G22
U8.F7	Data strobe byte lane 0	DDR2A_DQS0		A29

Table 2–37. DDR2 SDRAM Top Port Pin Assignments, Signal Names and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
U8.C8	Data bus byte lane 1	DDR2A_DQ8	1.8-V SSTL Class I	D22
U8.C2	Data bus byte lane 1	DDR2A_DQ9		A26
U8.D7	Data bus byte lane 1	DDR2A_DQ10		E24
U8.D3	Data bus byte lane 1	DDR2A_DQ11		D26
U8.D1	Data bus byte lane 1	DDR2A_DQ12		B28
U8.D9	Data bus byte lane 1	DDR2A_DQ13		D21
U8.B1	Data bus byte lane 1	DDR2A_DQ14		B27
U8.B9	Data bus byte lane 1	DDR2A_DQ15		F19
U8.B3	Write mask byte lane 1	DDR2A_DM1		A24
U8.B7	Data strobe byte lane 1	DDR2A_DQS1		G17
U15.G8	Data bus byte lane 2	DDR2A_DQ16		E19
U15.G2	Data bus byte lane 2	DDR2A_DQ17		D19
U15.H7	Data bus byte lane 2	DDR2A_DQ18		C18
U15.H3	Data bus byte lane 2	DDR2A_DQ19		A17
U15.H1	Data bus byte lane 2	DDR2A_DQ20		A23
U15.H9	Data bus byte lane 2	DDR2A_DQ21		E18
U15.F1	Data bus byte lane 2	DDR2A_DQ22		C22
U15.F9	Data bus byte lane 2	DDR2A_DQ23		K18
U15.F3	Write mask byte lane 2	DDR2A_DM2		B16
U15.F7	Data strobe byte lane 2	DDR2A_DQS2		K19
U15.C8	Data bus byte lane 3	DDR2A_DQ24		A13
U15.C2	Data bus byte lane 3	DDR2A_DQ25		C14
U15.D7	Data bus byte lane 3	DDR2A_DQ26		A12
U15.D3	Data bus byte lane 3	DDR2A_DQ27		A14
U15.D1	Data bus byte lane 3	DDR2A_DQ28		D16
U15.D9	Data bus byte lane 3	DDR2A_DQ29		F13
U15.B1	Data bus byte lane 3	DDR2A_DQ30		D15
U15.B9	Data bus byte lane 3	DDR2A_DQ31		F12
U15.B3	Write mask byte lane 3	DDR2A_DM3		A8
U15.B7	Data strobe byte lane 3	DDR2A_DQS3		C16

DDR2 SDRAM Bottom Port

The DDR2 SDRAM bottom port consists of two DDR2 devices (U17 and U19). Table 2–38 lists the DDR2 bottom port pin assignments, signal names, and its functions. The signal names and types are relative to the Cyclone IV GX device in terms of I/O setting and direction.

Table 2–38. DDR2 SDRAM Bottom Port Pin Assignments, Signal Names and Functions (Part 1 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
U17.R2, U19.R2	Address bus	DDR2B_A12	1.8-V SSTL Class I	AB11
U17.P7, U19.P7	Address bus	DDR2B_A11		AE15
U17.M2, U19.M2	Address bus	DDR2B_A10		AH8
U17.P3, U19.P3	Address bus	DDR2B_A9		AG7
U17.P8, U19.P8	Address bus	DDR2B_A8		AA16
U17.P2, U19.P2	Address bus	DDR2B_A7		AG8
U17.N7, U19.N7	Address bus	DDR2B_A6		AH14
U17.N3, U19.N3	Address bus	DDR2B_A5		AK7
U17.N8, U19.N8	Address bus	DDR2B_A4		AG15
U17.N2, U19.N2	Address bus	DDR2B_A3		AH7
U17.M7, U19.M7	Address bus	DDR2B_A2		AB14
U17.M3, U19.M3	Address bus	DDR2B_A1		AK9
U17.M8, U19.M8	Address bus	DDR2B_A0		AG14
U17.L3, U19.L3	Bank address bus	DDR2B_BA1		AJ9
U17.L2, U19.L2	Bank address bus	DDR2B_BA0		AA12
U17.K7, U19.K7	Row address select	DDR2B_RASn		AG12
U17.L7, U19.L7	Column address select	DDR2B_CASn		AK10
U17.L8, U19.L8	Chip select	DDR2B_CSn		AK12
U17.K3, U19.K3	Write enable	DDR2B_WEn		AH10
U17.K9, U19.K9	Termination enable	DDR2B_ODT		AF13
U17.K2, U19.K2	Clock enable	DDR2B_CKE		AA13
U17.J8, U19.J8	Clock P	DDR2B_CLK_P		AF4
U17.K8, U19.K8	Clock N	DDR2B_CLK_N		AG4
U19.G8,	Data bus byte lane 0	DDR2B_DQ0		AG5
U19.G2	Data bus byte lane 0	DDR2B_DQ1		AJ3
U19.H7	Data bus byte lane 0	DDR2B_DQ2		AK4
U19.H3	Data bus byte lane 0	DDR2B_DQ3		AJ4
U19.H1	Data bus byte lane 0	DDR2B_DQ4		AH2
U19.H9	Data bus byte lane 0	DDR2B_DQ5		AH6
U19.F1	Data bus byte lane 0	DDR2B_DQ6		AF3
U19.F9	Data bus byte lane 0	DDR2B_DQ7		AK5
U19.F3	Write mask byte lane 0	DDR2B_DM0		AE3
U19.F7	Data strobe byte lane 0	DDR2B_DQS0		AD9

Table 2–38. DDR2 SDRAM Bottom Port Pin Assignments, Signal Names and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
U19.C8	Data bus byte lane 1	DDR2B_DQ8	1.8-V SSTL Class I	AJ10
U19.C2	Data bus byte lane 1	DDR2B_DQ9		AG9
U19.D7	Data bus byte lane 1	DDR2B_DQ10		AG13
U19.D3	Data bus byte lane 1	DDR2B_DQ11		AH11
U19.D1	Data bus byte lane 1	DDR2B_DQ12		AG10
U19.D9	Data bus byte lane 1	DDR2B_DQ13		AH12
U19.B1	Data bus byte lane 1	DDR2B_DQ14		AE12
U19.B9	Data bus byte lane 1	DDR2B_DQ15		AE13
U19.B3	Write mask byte lane 1	DDR2B_DM1		AJ6
U19.B7	Data strobe byte lane 1	DDR2B_DQS1		AH13
U17.G8	Data bus byte lane 2	DDR2B_DQ16		AA15
U17.G2	Data bus byte lane 2	DDR2B_DQ17		AK11
U17.H7	Data bus byte lane 2	DDR2B_DQ18		AH15
U17.H3	Data bus byte lane 2	DDR2B_DQ19		AE14
U17.H1	Data bus byte lane 2	DDR2B_DQ20		AK8
U17.H9	Data bus byte lane 2	DDR2B_DQ21		AH16
U17.F1	Data bus byte lane 2	DDR2B_DQ22		AJ7
U17.F9	Data bus byte lane 2	DDR2B_DQ23		AB16
U17.F3	Write mask byte lane 2	DDR2B_DM2		AH18
U17.F7	Data strobe byte lane 2	DDR2B_DQS2		AF15
U17.C8	Data bus byte lane 3	DDR2B_DQ24		AH18
U17.C2	Data bus byte lane 3	DDR2B_DQ25		AK17
U17.D7	Data bus byte lane 3	DDR2B_DQ26		AJ18
U17.D3	Data bus byte lane 3	DDR2B_DQ27		AK18
U17.D1	Data bus byte lane 3	DDR2B_DQ28		AK15
U17.D9	Data bus byte lane 3	DDR2B_DQ29		AE18
U17.B1	Data bus byte lane 3	DDR2B_DQ30		AJ15
U17.B9	Data bus byte lane 3	DDR2B_DQ31		AH19
U17.B3	Write mask byte lane 3	DDR2B_DM3		Y17
U17.B7	Data strobe P byte lane 3	DDR2B_DQS3		AA17

Table 2–39 lists the DDR2 component reference and manufacturing information.

Table 2–39. DDR2 Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U8, U15, U17, U19	16 M × 16-bit × 4 banks, 533Mbps, CL4	Micron	MT47H16M16BG-37E:B	www.micron.com

SSRAM

The SSRAM consists of a single standard synchronous SRAM device with a 100-TQFP package footprint. This device has 4 MB of memory with a 18-bit data bus but is implemented for non-linear burst mode using only a 16-bit data bus. The device speed is 200 MHz single-data-rate. There is no minimum speed for this device.

This device is part of the shared FSM bus which connects to the flash memory, SRAM, and MAX II CPLD EPM2210 System Controller.

Table 2–40 lists the SSRAM pin assignments, signal names, and functions. The signal names and types are relative to the Cyclone IV GX device in terms of I/O setting and direction.

Table 2–40. SSRAM Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
U44.46	Address bus	FSM_A1	1.8-V	AD6
U44.44	Address bus	FSM_A2		AK29
U44.42	Address bus	FSM_A3		AA21
U44.37	Address bus	FSM_A4		AG25
U44.36	Address bus	FSM_A5		AH5
U44.48	Address bus	FSM_A6		AH27
U44.43	Address bus	FSM_A7		AJ12
U44.49	Address bus	FSM_A8		AF16
U44.47	Address bus	FSM_A9		AH20
U44.39	Address bus	FSM_A10		AK23
U44.35	Address bus	FSM_A11		AH17
U44.34	Address bus	FSM_A12		AB21
U44.50	Address bus	FSM_A13		AF19
U44.45	Address bus	FSM_A14		AF12
U44.33	Address bus	FSM_A15		AG27
U44.32	Address bus	FSM_A16		AK26
U44.100	Address bus	FSM_A17		AH4
U44.80	Address bus	FSM_A18		AK3
U44.81	Address bus	FSM_A19		AH9
U44.99	Address bus	FSM_A20		AG6
U44.82	Address bus	FSM_A21		AK25
U44.23	Data bus	FSM_D0		AK14
U44.59	Data bus	FSM_D1		AE6
U44.22	Data bus	FSM_D2		AG21
U44.63	Data bus	FSM_D3		AE9
U44.68	Data bus	FSM_D4		AK28
U44.72	Data bus	FSM_D5		AD23
U44.12	Data bus	FSM_D6		AG24

Table 2–40. SSRAM Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
U44.9	Data bus	FSM_D7	1.8-V	AB22
U44.58	Data bus	FSM_D8		AE22
U44.62	Data bus	FSM_D9		AJ24
U44.19	Data bus	FSM_D10		Y19
U44.18	Data bus	FSM_D11		AH23
U44.69	Data bus	FSM_D12		AK22
U44.13	Data bus	FSM_D13		AH24
U44.8	Data bus	FSM_D14		Y18
U44.73	Data bus	FSM_D15		AJ13
U44.14	Flow Through or Pipeline mode; active low	SSRAM_FTn		Pulled low
U44.31	Linear Burst Order mode; active low	SSRAM_LBOn		Pulled low
U44.74	Ninth unused data bit for lower byte lane	SSRAM_DQP0		Pulled low
U44.24	Ninth unused data bit for upper byte lane	SSRAM_DQP1		Pulled low
U44.83	ADVn burst address counter advance enable; active low	SSRAM_ADVn		Pulled high
U44.84	Address strobe (Processor, Cache Controller); active low	SSRAM_ADSPn		Pulled high
U44.85	Address strobe (Processor, Cache Controller); active low	SSRAM_ADSCn		Pulled low
U44.86	Output enable; active low	SSRAM_Gn		G6
U44.87	Byte lane write enable	SSRAM_BWn		F8
U44.89	Clock	SSRAM_CLK		F11
U44.98	Chip enable 1	SSRAM_E1n		C6
U44.97	Chip enable 2	SSRAM_E2		Pulled high
U44.92	Chip enable 3	SSRAM_E3n		Pulled low
U44.93	Byte write enable for DQA Data I/Os; active low	SSRAM_BAn		D13
U44.94	Byte write enable for DQB Data I/Os; active low	SSRAM_BBn		D27
U44.64	Sleep enable	SSRAM_ZZ		Pulled low

Table 2–41 lists the SSRAM component reference and manufacturing information.

Table 2–41. SSRAM Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U44	Standard Synchronous Pipelined SCD, 2 M × 18, 200 MHz	GSI	GS832018GT-200V	www.gsitechnology.com

Flash

The flash interface consists of a single synchronous flash memory device, providing 64 MB of memory with a 16-bit data bus. This device is part of the shared FSM bus which connects to the flash memory, SRAM, LCD, and MAX II CPLD EPM2210 System Controller.

This 16-bit data memory interface can sustain burst read operations at up to 52 MHz for a throughput of 832 Mbps. The write performance is 125 µs for a single word and 440 µs for a 32-word buffer. The erase time is 400 ms for a 32 K parameter block and 1200 ms for a 128 K main block.

For more information about the flash memory map storage, refer to the *Cyclone IV GX Development Kit User Guide*.

Table 2–42 lists the flash pin assignments, signal names, and functions. The signal names and types are relative to the Cyclone IV GX device in terms of I/O setting and direction.

Table 2–42. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
U6.F6	Address valid	FLASH_ADVn	1.8-V	F24
U6.B4	Chip enable	FLASH_CEn		E25
U6.E6	Clock	FLASH_CLK		Y21
U6.F8	Output enable	FSM_OEn		F7
U6.F7	Ready	FLASH_RDYBSYn		B7
U6.D4	Reset	FLASH_RESETn		A28
U6.G8	Write enable	FSM_WEn		C13
U6.C6	Write protect	FLASH_WPn		Pulled high
U6.A1	Address bus	FSM_A1		AD6
U6.B1	Address bus	FSM_A2		AK29
U6.C1	Address bus	FSM_A3		AA21
U6.D1	Address bus	FSM_A4		AG25
U6.D2	Address bus	FSM_A5		AH5
U6.A2	Address bus	FSM_A6		AH27
U6.C2	Address bus	FSM_A7		AJ12
U6.A3	Address bus	FSM_A8		AF16
U6.B3	Address bus	FSM_A9		AH20
U6.C3	Address bus	FSM_A10		AK23
U6.D3	Address bus	FSM_A11		AH17
U6.C4	Address bus	FSM_A12		AB21
U6.A5	Address bus	FSM_A13		AF19
U6.B5	Address bus	FSM_A14		AF12
U6.C5	Address bus	FSM_A15		AG27

Table 2–42. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference	Description	Schematic Signal Name	I/O Standard	Cyclone IV GX Device Pin Number
U6.D7	Address bus	FSM_A16	1.8-V	AK26
U6.D8	Address bus	FSM_A17		AH4
U6.A7	Address bus	FSM_A18		AK3
U6.B7	Address bus	FSM_A19		AH9
U6.C7	Address bus	FSM_A20		AG6
U6.C8	Address bus	FSM_A21		AK25
U6.A8	Address bus	FSM_A22		AE21
U6.G1	Address bus	FSM_A23		AA18
U6.H8	Address bus	FSM_A24		AK27
U6.B6	Address bus	FSM_A25		AF21
U6.F2	Data bus	FSM_D0		AK14
U6.E2	Data bus	FSM_D1		AE6
U6.G3	Data bus	FSM_D2		AG21
U6.E4	Data bus	FSM_D3		AE9
U6.E5	Data bus	FSM_D4		AK28
U6.G5	Data bus	FSM_D5		AD23
U6.G6	Data bus	FSM_D6		AG24
U6.H7	Data bus	FSM_D7		AB22
U6.E1	Data bus	FSM_D8		AE22
U6.E3	Data bus	FSM_D9		AJ24
U6.F3	Data bus	FSM_D10		Y19
U6.F4	Data bus	FSM_D11		AH23
U6.F5	Data bus	FSM_D12		AK22
U6.H5	Data bus	FSM_D13		AH24
U6.G7	Data bus	FSM_D14		Y18
U6.E7	Data bus	FSM_D15		AJ13

Table 2–43 lists the flash component reference and manufacturing information.

Table 2–43. Flash Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U6	512-Mb synchronous flash	Numonyx	PC28F512P30BF	www.numonyx.com

Power Supply

The development board's power is provided through a laptop-style DC power input. The input voltage must be 16 V. The DC voltage is then stepped down to various power rails used by the components on the board.

An on-board multi-channel analog-to-digital converter (ADC) measures both the voltage and current for several specific board rails. The power utilization is displayed using a GUI that can graph power consumption versus time.

Power Distribution System

Figure 2–7 shows the power distribution system on the development board. The currents shown are conservative absolute maximum levels and reflects the regulator inefficiencies and sharing.

Figure 2–7. Power Distribution System

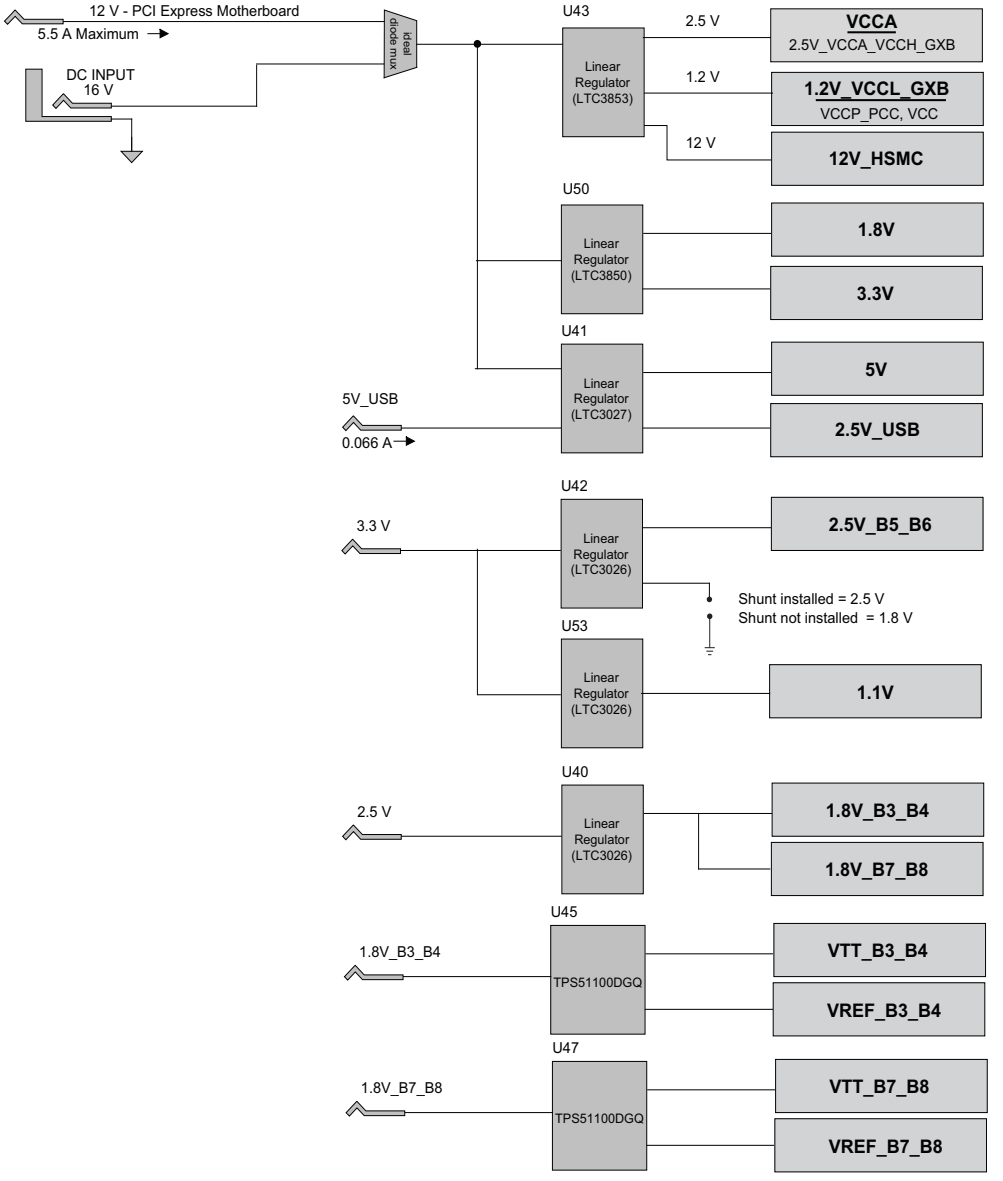


Table 2–44 lists the power supply component reference and manufacturing information.

Table 2–44. Power Supply Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
—	16-V power supply	EDAC Power Electronics	EA1060A	www.edac.com.tw

Power Measurement

There are eight power supply rails which have on-board voltage and current sense capabilities. The power supply rails are split from the primary supply plane by a low-value sense resistor for the 8-channel differential input 24-bit ADC device to measure voltage and current. A SPI bus connects the ADC device to the MAX II CPLD EPM2210 System Controller.

Figure 2–8 shows the block diagram for the power measurement circuitry.

Figure 2–8. Power Measurement Circuit

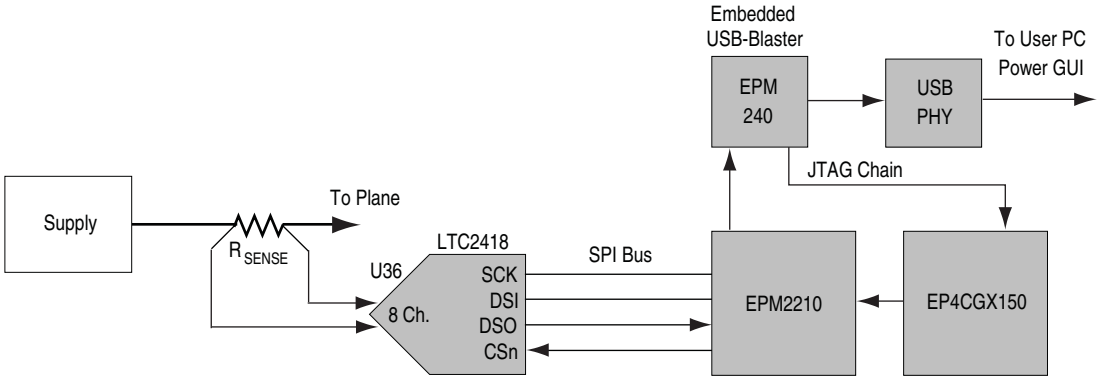


Table 2–45 lists the targeted rails. The schematic signal name column specifies the name of the rail being measured and the device pin column specifies the devices attached to the rail. If no subnet is named, the power is the total output power for that voltage.

Table 2–45. Power Rails Measurement Based on the Rail Selected in the Power GUI (Part 1 of 2)

Rail	Schematic Signal Name	Voltage (V)	Device Pin	Description
1	1.8V_B3_B4	1.8	VCCIO	1.8-V power to banks 3 and 4
2	1.8V_B7_B8	1.8	VCCIO	1.8-V power to banks 7and 8
3	2.5V_B5_B6	2.5 or 1.8	VCCIO	1.8-V or 2.5-V power to banks 5 and 6. Voltage selected by jumper J3. When J3 is shunted the voltage is 2.5 V and not shunted it is 1.8 V
4	VCCA	2.5	VCCA, VCC_CLKIN	PLL analog power
5	2.5V_VCCA_VCCH_GXB	2.5	VCCA_GXB, VCCH_GXB	Transceiver buffer power
6	1.2V_VCCL_GXB	1.2	VCCL_GXB	PMA auxiliary power

Table 2–45. Power Rails Measurement Based on the Rail Selected in the Power GUI (Part 2 of 2)

Rail	Schematic Signal Name	Voltage (V)	Device Pin	Description
7	VCCD_PLL	1.2	VCCD	PLL digital power
8	VCC	1,2	VCC	CORE

Table 2–46 lists the power measurement ADC component reference and manufacturing information.

Table 2–46. Power Measurement ADC Component Reference and Manufacturing Information

Board Reference	Description	Manufacturer	Manufacturing Part Number	Manufacturer Website
U13	8-channel differential input 24-bit ADC	Linear Technology	LTC2418	www.linear.com

Statement of China-RoHS Compliance

Table 2–47 lists hazardous substances included with the kit.

Table 2–47. Table of Hazardous Substances' Name and Concentration ***Notes (1), (2)***

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavalent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
Cyclone IV GX FPGA development board	X*	0	0	0	0	0
16-V power supply	0	0	0	0	0	0
Type A-B USB cable	0	0	0	0	0	0
User guide	0	0	0	0	0	0

Notes to Table 2–47:

(1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.

(2) X* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.

This chapter provides additional information about the document and Altera.

Document Revision History

The following table shows the revision history for this document.

Date	Version	Changes
August 2015	1.2	Added PHY address.
May 2013	1.1	■ Updated Table 2–18—The I/O standard for user push buttons is 1.8-V. ■ Updated the note in Table 2–26—All signals are translated from 1.8-V to 2.5-V using a dual/quad low-voltage level translators except for LCD_DATA4. ■ Updated Table 2–29—The I/O standard for PCI Express transmit and receive bus is 1.5-V PCML. ■ Updated Table 2–33—HSMA pin J1.44 connects to FPGA pin AD27. ■ Updated the document template.
December 2010	1.0	Initial release.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	The multimedia icon directs you to a related multimedia presentation.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.
	The feedback icon allows you to submit feedback to Altera about the document. Methods for collecting feedback vary as appropriate for each document.