Serial Digital Interface Reference Design for Stratix IV Devices

AN-600-1.2 Application Note

The Serial Digital Interface (SDI) reference design shows how you can transmit and receive video data using the Altera® SDI MegaCore® function and the Audio Video Development Kit, Stratix® IV GX Edition. This reference design uses three instances of a triple standard SDI MegaCore function. The triple standard SDI MegaCore function comprises standard definition (SD-SDI), high definition (HD-SDI), and 3 gigabits per second (3G-SDI) standards.

This application note describes how to use the SDI reference design with the Audio Video Development Kit, Stratix IV GX Edition for different variants. The Audio Video Development Kit, Stratix IV GX Edition consists of a Stratix IV GX FPGA development board and an SDI high-speed mezzanine card (HSMC).

For more information about the Audio Video Development Kit, Stratix IV GX Edition, refer to *Audio Video Development Kit, Stratix IV GX Edition User Guide*. For more information about the Stratix IV GX FPGA development board, refer to the *Stratix IV GX FPGA Development Board Reference Manual*; and for more information about the SDI HSMC, refer to *SDI HSMC Reference Manual*. For more information about the SDI MegaCore function, refer to *SDI MegaCore Function User Guide* or contact your Altera representative.

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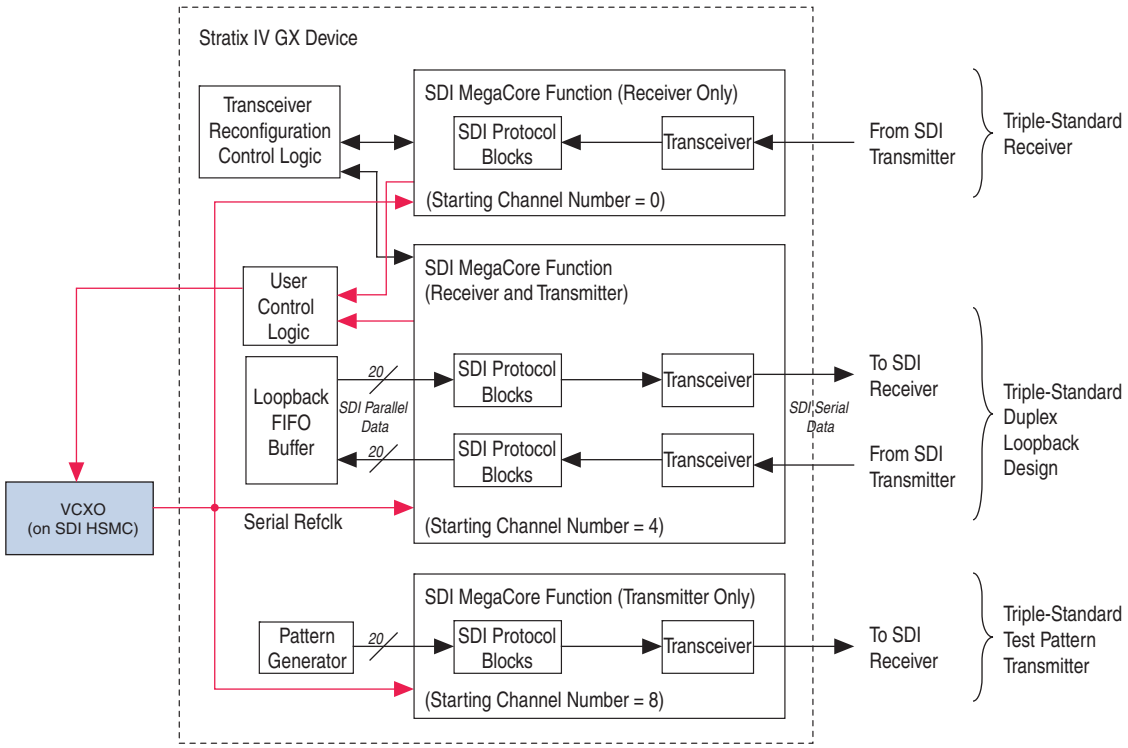
Functional Description

The reference design provides a general platform that enables you to control, test, and monitor different speeds of the SDI operations. Figure 1 shows a high-level block diagram of the SDI reference design.

Figure 1. High-Level Block Diagram of the SDI Reference Design



The following sections describe the various elements of the reference design.

Triple-Standard Receiver

The triple-standard SDI receiver MegaCore function provides an SD-SDI, HD-SDI, and 3G-SDI receiver interface.

Triple-Standard Transmitter

The triple-standard SDI transmitter MegaCore function outputs a 2.970-Gbps 1080p, 1.485-Gbps 1080i, or 270-Mbps data stream. The transmitter takes its input from the pattern generator.

Triple-Standard Duplex Loopback Design

The triple-standard SDI duplex MegaCore function provides a full-duplex, SD-SDI, HD-SDI, and 3G-SDI, and demonstrates receiver-to-transmitter loopback. The received data is decoded, buffered, recoded, and then transmitted. The interface is configured for 2.970-Gbps, 1.485-Gbps, or 270-Mbps rates.

Loopback FIFO Buffer

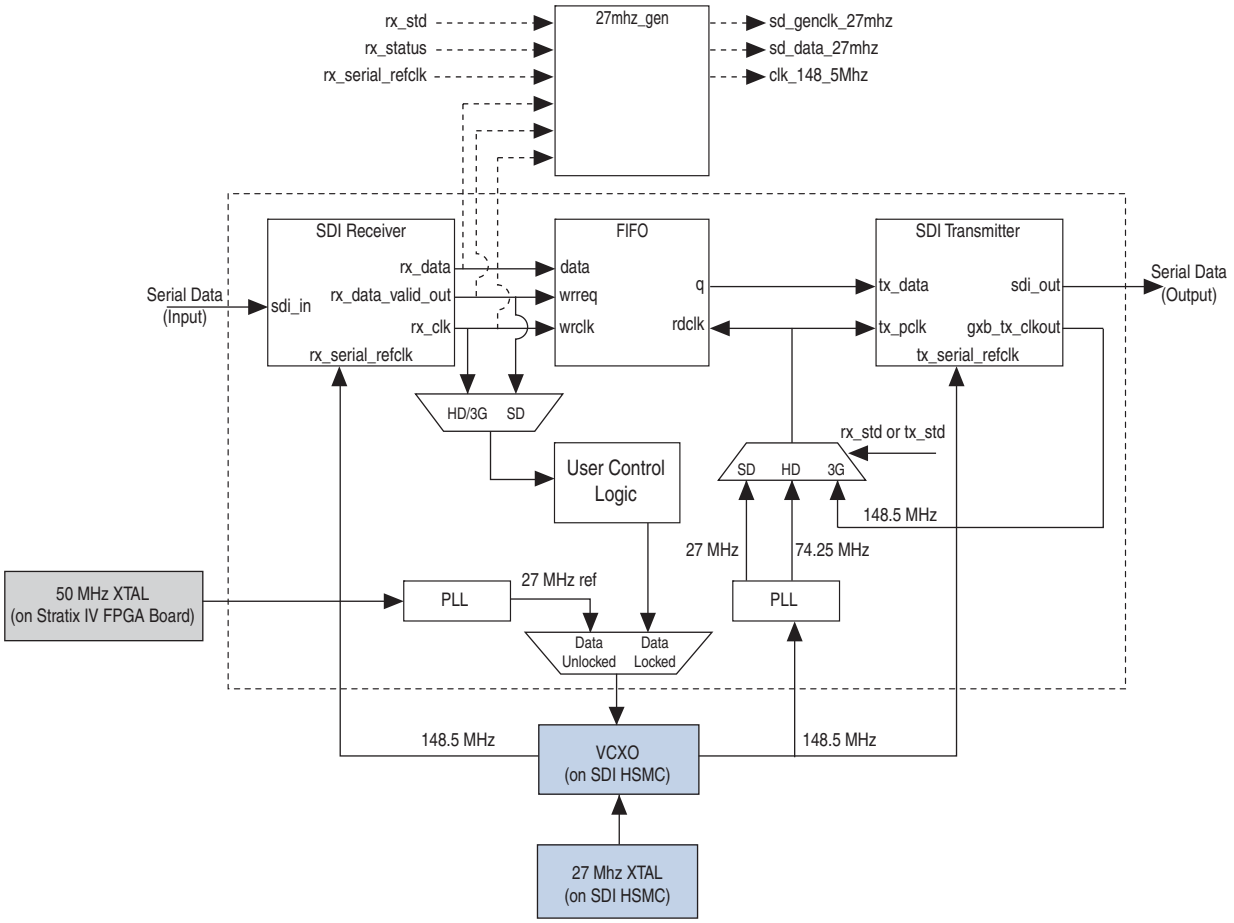
The receiver sends the decoded receiver data to the transmitter through a FIFO buffer. When the receiver is locked, the receiver data is written to the FIFO buffer. When the FIFO buffer is half full, the transmitter starts reading, encoding, and transmitting the data.

Voltage Controlled Crystal Oscillator (VCXO)

The VCXO device is a phase-locked loop (PLL) based synchronous clock generator (ICS810001) that is located on the SDI HSMC. This device contains two internal frequency multiplication stages that are cascaded in series. The first stage is a VCXO PLL that is optimized to provide reference clock jitter attenuation and support the complex PLL multiplication ratios needed for video rate conversion. The second stage is a FemtoClock™ frequency multiplier that provides the low jitter, high frequency video output clock. The 148.5-MHz VCXO output clock connects to the `rx_serial_ref_clk` and `tx_serial_ref_clk` clocks of all the three SDI instances.

Figure 2 shows the block diagram for the duplex loopback FIFO design and VXCO.

Figure 2. Block Diagram for Duplex Loopback FIFO Design and VXCO



Pattern Generator

The pattern generator outputs a 2.970-Gbps 1080p, 1.485-Gbps 1080i, or 270-Mbps test pattern. The test pattern can be a 100% color bar, a 75% amplitude color bar, or an SDI pathological checkfield frame.

Transceiver Reconfiguration Control Logic

The reconfiguration control logic block handles the reconfiguration of the receiver in the duplex core and the external receiver in the design.

The logic block comprises the following subblocks:

- Sdi_tr_reconfig_multi_siv

  This top-level design contains the arbitration logic for up to four receiver ports. This block also has a state machine to control the ALTGX_RECONFIG megafunction.

- Alt4gxb_gxb_reconfig

  This block is an ALTGX_RECONFIG instance that is required for the dynamic partial reconfigurable I/O (DPRIO). Only this ALTGX_RECONFIG instance reprograms the ALTGX transceivers.

- ROMs

  The ROMs hold the ALTGX setting information for each of the video standards. Four ROMs are included, which allows a maximum of four channels to be reconfigured.

- Sdi_mif_intercept

  This block intercepts the data read from the ROMs. If reprogramming to HD is requested, this block modifies the data read from the ROM before sending it to the ALTGX reconfiguration block. This block removes the need to have a ROM for the HD setup.

For more information about the ALTGX_RECONFIG instance, refer to the *Stratix IV Device Handbook*. For more information about DPRIO, refer to the DPRIO section in the *SDI MegaCore Function User Guide*, and *AN 587: DPRIO and Multiple Instances SDI Application*.

User Control Logic

This user control logic receives the CDR receiver clock, `rx_clk`, from the SDI receiver only and duplex instances, and then sends the receiver clock with the control bits to the VCXO device.

27mhz_gen

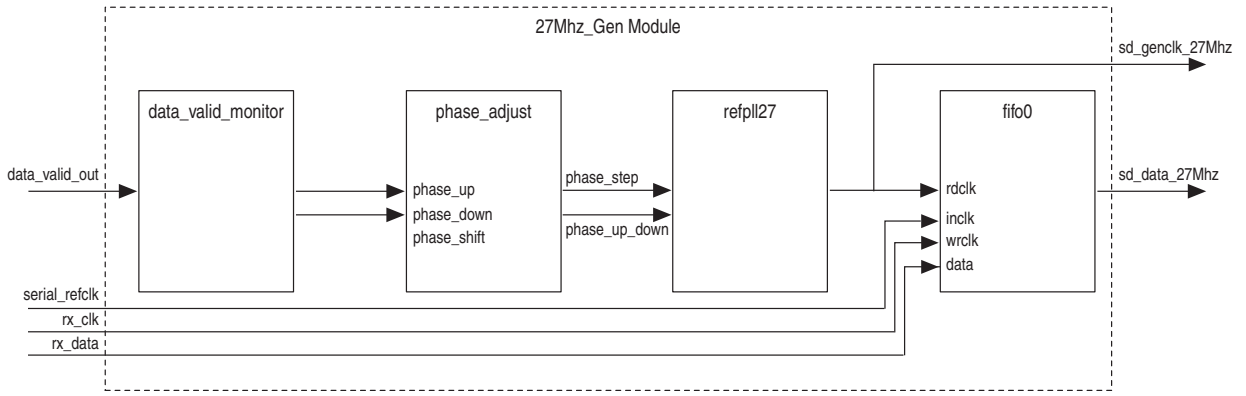
This module generates a 27-MHz parallel clock to receive the SD-SDI data. Use the `sd_genclk_27mhz` output clock to clock the `sd_data_27mhz` parallel data for SD-SDI.

The 27mhz_gen module consists of the following components:

- data_valid_monitor module—a user logic to control the pll
- phase_adjust module—module that controls the pll based `data_validout` signal
- `refpll27`—pll that generates `sd_genclock_27mhz` clock to clock the `sd_data_27mhz` data that comes from the FIFO buffer
- FIFO buffer

Figure 3 shows the block diagram of the 27mhz_gen module.

Figure 3. Block Diagram of the 27mhz_gen Module



Getting Started

This section discusses the requirements and related procedures to demonstrate the SDI reference design with the Stratix IV GX audio video development board. This section contains the following topics:

- Hardware and Software Requirements
- Hardware Setup
- Running the Reference Design
- Using the Reference Design

Hardware and Software Requirements

The demonstration requires the following hardware and software:

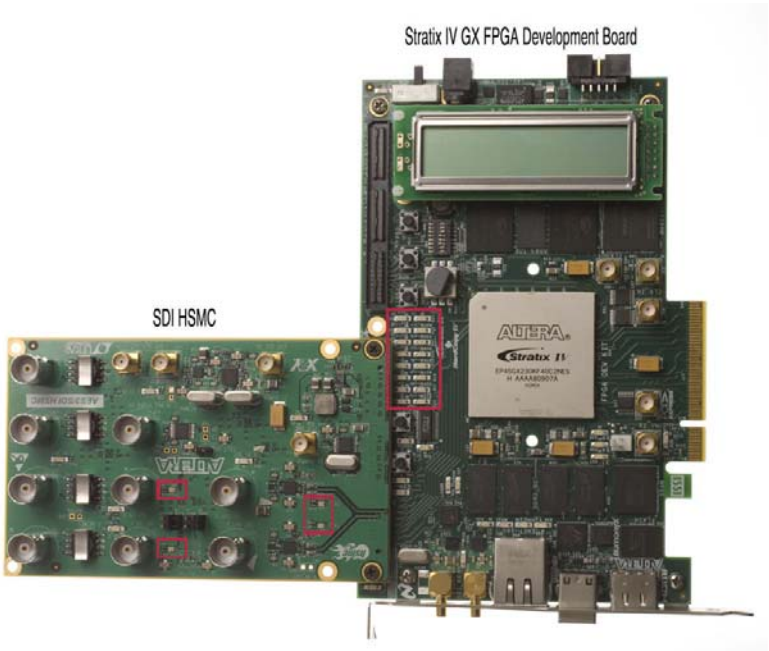
- Audio Video Development Kit, Stratix IV GX Edition—Stratix IV GX FPGA development board and SDI HSMC
- SDI MegaCore function
- Quartus® II software, version 10.0 SP1

To obtain the Audio Video Development Kit, Stratix IV GX Edition, contact your local Altera representative.

Hardware Setup

Figure 4 shows how the Stratix IV GX FPGA development board is connected to the SDI HSMC. The highlighted areas indicate the LEDs.

Figure 4. Stratix IV GX FPGA Development Board Connected to the SDI HSMC



The push button S2 functions as the CPU reset button. Table 1 describes the function of each LED on the Stratix IV GX FPGA development board.

Table 1. LEDs on Stratix IV GX FPGA Development Board (Part 1 of 2)

LED	Description
D6, D7	Internal pattern generator signal standard [D6, D7] : 00 = SD-SDI, 01 = HD-SDI, 11 = 3G-SDI
D8	Not used
D9	Not used
D10, D11	SDI IN2 received signal standard [D10, D11] : 00 = SD-SDI, 01 = HD-SDI, 11 = 3G-SDI
D12, D13	SDI IN1 received signal standard [D12, D13] : 00 = SD-SDI, 01 = HD-SDI, 11 = 3G-SDI
D16	SDI IN2 in reset
D17	SDI IN2 frame lock
D18	SDI IN2 TRS lock
D19	SDI IN2 alignment lock
D20	SDI IN1 in reset
D21	SDI IN1 frame lock

Table 1. LEDs on Stratix IV GX FPGA Development Board (Part 2 of 2)

LED	Description
D22	SDI IN1 TRS lock
D23	SDI IN1 alignment lock

Table 2 describes the function of each LED on the SDI HSMC.

Table 2. LEDs on SDI HSMC

DIP	Description
D1	SDI IN2 receiving SDI signal standard: Red = SD-SDI, Orange = HD-SDI, Green = 3G-SDI
D3	SDI OUT2 transmitting SDI signal standard: Red = SD-SDI, Orange = HD-SDI, Green = 3G-SDI
D5	SDI OUT1 transmitting SDI signal standard: Red = SD-SDI, Orange = HD-SDI, Green = 3G-SDI
D6	SDI IN1 receiving SDI signal standard: Red = SD-SDI, Orange = HD-SDI, Green = 3G-SDI

Table 3 describes the function of each dual in-line package (DIP) switch.

Table 3. SW3 DIP Switch

DIP Switch	Description
8, 7,6,5	Not used
4	1 = Select pathological SDI checkfield pattern
3	1= 100% color bar 0= 75% color bar
2, 1	Change pattern generator signal standard: 00 = SD-SDI, 01 = HD-SDI, 11 = 3G-SDI

Running the Reference Design

To run the reference design, you need to set up the board first. To set up the board, perform the following steps:

1. Set up the board connections.
   a. Connect the SDI HSMC to the HSMA port on the FPGA development board, refer to Figure 4 on page 6.
   b. Specify the board settings for the switch controls: DIP switch (SW4), PCI Express control DIP switch (SW5), and JTAG control DIP switch (SW6), located at the back of the FPGA development board. Match the settings to the switch control settings in Table 4.
   c. Connect the FPGA development board (J4) to the power supply.

Table 4. SW DIP Switch Control Settings (Part 1 of 2)

Switch	Schematic Signal Name	Description	Default
SW4			
1	MAX_DIP	Reserved	OFF
2	USB_DISABLEn	ON: Embedded USB-Blaster disable OFF: Embedded USB-Blaster enable	OFF
3	LCD_PWRMON	ON: LCD driven from the MAX II EPM2210 System Controller (power monitor) OFF: LCD driven from the FPGA (no power monitor)	ON
4	FAN_FORCE_ON	ON: Fan forced ON OFF: Fan controlled by the MAX1619 device	ON
5	CLK_SEL	ON: 100 MHz clock select OFF: SMA input clock select	ON
6	CLK_ENABLE	ON: On-board oscillator enable OFF: On-board oscillator disable	ON
7	S4VCCH_SEL	ON: 1.4 V (default) OFF: 1.5 V	ON
8	S4VCCA_SEL	ON: 3.3 V (default) OFF: 2.5 V	ON
SW5			
1	PCIE_PRSNT2n_x1	ON: Enable ×1 presence detect OFF: Disable ×1 presence detect	OFF
2	PCIE_PRSNT2n_x4	ON: Enable ×4 presence detect OFF: Disable ×4 presence detect	OFF
3	PCIE_PRSNT2n_x8	ON: Enable ×8 presence detect OFF: Disable ×8 presence detect	OFF
4	MAX_EN	Reserved	OFF

Table 4. SW DIP Switch Control Settings (Part 2 of 2)

Switch	Schematic Signal Name	Description	Default
SW6			
1	EPM2210_JTAG_EN	ON: Bypass MAX II CPLD EPM2210 System Controller OFF: MAX II CPLD EPM2210 System Controller in-chain	ON
2	HSMA_JTAG_EN	ON: Bypass HSMA OFF: HSMA in-chain	OFF
3	HSMB_JTAG_EN	ON: Bypass HSMB OFF: HSMB in-chain	ON
4	PCIE_JTAG_EN	ON: Bypass PCI Express OFF: Reserved	ON

2. Launch the Quartus II software.
   a. On the File menu, click **Open Project**, navigate to \<*directory*>**\s4gxsdi.qpf**, and click **Open**.
   b. On the Processing menu, click **Start Compilation**.
3. Download the Quartus II-generated SRAM Object File (**.sof**), \<*directory*>**\s4gxsdi.sof**.
   a. Connect the USB-Blaster™ download cable to the board's USB Type-B Connector (J7).
   b. On the Tools menu, click **Programmer** to download the \<*directory*>**\s4gxsdi.sof** to the board. The software automatically detects the file during compilation and it appears on the pop-up window. Click **Start** to download the file to the board. If the file does not appear in the pop-up window, click **Add File**, navigate to \<*directory*>**\a2gxsdi.sof**, and click **Open**.


This design is volatile. You must reload this design each time the board is powered on.

After you set up the board, you can run the different variants described in the following sections.

Parallel Loopback

To run the parallel loopback demonstration, follow these steps:

1. Connect an SDI signal generator to the receiver input of SDI IN2 (BNC J2).
2. Connect an SDI signal analyzer to the transmitter output of SDI OUT2 (BNC J1).
3. The parallel loopback demonstration runs. The LEDs indicate the following conditions:
   - LEDs D10 and D11 indicate the receiver signal standard.
   - LED D17 illuminates when the receiver frame format is stable at port 2.
   - LED D18 illuminates when the received line format is stable at port 2.

- LED D19 illuminates when the receiver word is aligned at port 2.

Figure 5 shows the conditions of the LEDs.

Figure 5. Condition of LEDs for Parallel Loopback Demonstration

Additionally, the LEDs on the SDI HSMC indicate the following conditions:

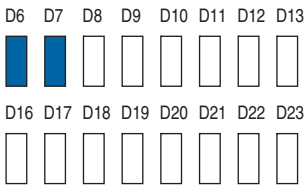
- LED D1 illuminates when the receiver signal standard is detected at port 2.
- LED D3 illuminates when the transmitter signal standard is detected at port 2.

Test Pattern Transmitter

To run the test pattern transmitter demonstration, follow these steps:

1. Connect an SDI signal analyzer to the transmitter output `SDI OUT1` (BNC J8). The LEDs indicate the following conditions:
   - LEDs D6 and D7 indicate the internal pattern generator signal standard, which transmits through port 1 in the transmitter, refer to Figure 6 on page 10.

Figure 6. Condition of LEDs for Test Pattern Transmitter Demonstration



   - LED D5, on the SDI HSMC, illuminates to indicate the transmitter signal standard at port 1.
2. Check the result on the SDI signal analyzer.

Receiver

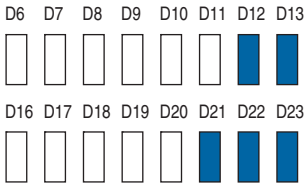
To run the receiver demonstration, follow these steps:

1. Connect an SDI signal generator to the receiver input of `SDI IN1` (BNC J9).

2. The receiver demonstration runs. The LEDs indicate the following conditions:
   - LEDs D12 and D13 indicate the receiver signal standard.
   - LED D21 illuminates when the receiver frame format is stable at port 1.
   - LED D22 illuminates when the received line format is stable at port 1.
   - LED D23 illuminates when the receiver word is aligned at port 1.

   Figure 7 shows the conditions of the LEDs.

Figure 7. Condition of LEDs for Receiver Demonstration



Additionally, LED D6 on the SDI HSMC illuminates when the receiver signal standard is detected at port 1.

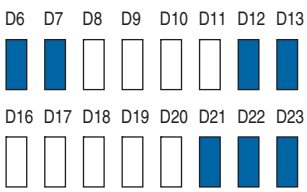
Serial Loopback

To run the serial loopback demonstration, follow these steps:

1. Connect transmitter output `SDI OUT1` (BNC J8) to receiver input `SDI IN1` (BNC J9).
2. The serial loopback demonstration runs. The LEDs indicate the following conditions:
   - LEDs D6 and D7 indicate the internal pattern generator signal standard, which transmits through port 1 of the transmitter.
   - LEDs D12 and D13 flash to indicate the receiver signal standard.
   - LED D21 illuminates when the receiver frame format is stable at port 1.
   - LED D22 illuminates when the received line format is stable at port 1.
   - LED D23 illuminates when the receiver word is aligned at port 1.

   Figure 8 shows the conditions of the LEDs.

Figure 8. Condition of LEDs for Test Pattern Transmitter Demonstration



Additionally, the LEDs on the SDI HSMC indicate the following conditions:

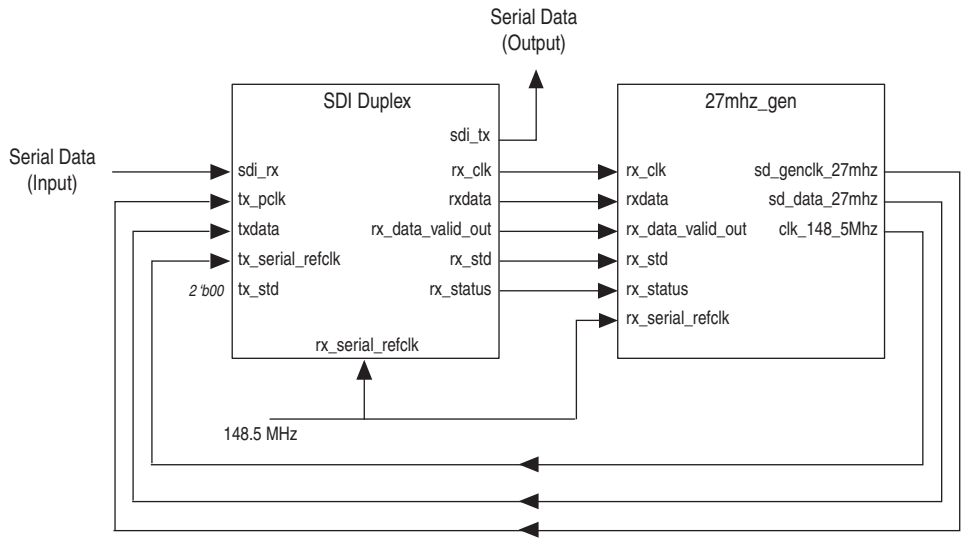
- LED D5 illuminates when the transmitter signal standard is detected at port 1.
- LED D6 illuminates when the receiver signal standard is detected at port 1.

Using the Reference Design

If you are using the SD-SDI standard, use the reference design with the 27mhz_gen module to generate the 27-MHz clock to receive the SD-SDI data.

Figure 9 shows how to use the 27mhz_gen module to generate a 27-MHz clean clock to receive SD-SDI parallel data. The 27-MHz clock and the SD-SDI parallel data from the 27mhz_gen module connects to the transmitter of SDI duplex instance, and transmits to a third party for monitoring.

Figure 9. Using 27mhz_gen Module with the Reference Design



If you are using the SD-SDI standard, type the following code to control the `GENERATE_SD_27MHZ_CLK` parameter:

```
GENERATE_SD_27MHZ_CLK =1'b1
```

If you are using a regular SDI operation, type the following code to control the `GENERATE_SD_27MHZ_CLK` parameter:

```
GENERATE_SD_27MHZ_CLK =1'b0
```

When compiling for a regular SDI operation, remove the back slash from the following line:

```
//define clk_148_p
```

Conclusion

This application note provides ways to use the SDI reference design with the Stratix IV GX FPGA development board and SDI HSMC. You can use the different variants discussed to evaluate the SDI MegaCore function for integration into Altera FPGA designs.

Document Revision History

Table 5 shows the revision history for this application note.

Table 5. Document Revision History

Date	Version	Changes
December 2010	1.2	■ Added information about the 27mhz_gen module. ■ Updated the design files.
July 2010	1.1	Updated Figure 2 on page 3 and the design files.
December 2009	1.0	Initial release.