Enhanced Configuration Devices

October 2007, Version 1.2 Errata Sheet

Introduction

This errata sheet provides updated information on enhanced configuration devices—EPC4, EPC8, and EPC16—which are used to configure SRAM-based programmable logic devices (PLDs). This document addresses known issues and includes methods to work around the issues.

Intel-Flash-Based EPC Device Protection

Altera performed a die-sub replacement for the EPC4, EPC8, and EPC16 devices with Intel flash. Intel flash devices do not have the lock bit protection feature to lock the flash for protection during power-up or power-down. The lock bit protection feature is used to prevent unintentional writes and ensure data retention.

For more information about the flash die change in the Altera® enhanced configuration devices, refer to *Process Change Notification PCN0506: Addition of Intel Flash Memory as Source for EPC4, EPC8 & EPC16 Enhanced Configuration Devices*.

In the absence of the lock bit protection feature in the EPC4, EPC8, and EPC16 devices with Intel flash, Altera recommends four methods to protect the Intel flash content in EPC4, EPC8, and EPC16 devices. Any method alone is sufficient to protect the flash. The methods are listed below in the order of descending protection level:

1. Using an RP# of less than 0.3 V on power-up and power-down for a minimum of 100 ns to a maximum 25 µs disables all control pins, making it impossible for a write to occur.
2. Using $V_{PP} < V_{PPLK,}$ where the maximum value of V_{PPLK} is 1 V, disables writes. $V_{PP} < V_{PPLK}$ means programming or writes cannot occur. V_{PP} is a programming supply voltage input pin on the Intel flash. V_{PP} is equivalent to the V_{CCW} pin on EPC16 devices.
3. Using a high CE# disables the chip. The requirement for a write is a low CE# and low WE#. A high CE# by itself prevents writes from occurring.
4. Using a high WE# prevents writes because a write only occurs when the WE# is low.

Performing all four methods simultaneously is the safest protection for the flash content.

The ideal power-up sequence is as follows:

1. Power up V_{CC}.
2. Maintain $V_{PP} < V_{PPLK}$ until V_{CC} is fully powered up.
3. Power up V_{PP}.
4. Drive RP# low during the entire power-up process. RP# must be released high within 25 µs after V_{PP} is powered up.

☞ CE# and WE# must be high for the entire power-up sequence.

The ideal power-down sequence is as follows:

1. Drive RP# low for 100 ns before power-down.
2. Power down $V_{PP} < V_{PPLK}$.
3. Power down V_{CC}.
4. Drive RP# low during the entire power-down process.

☞ CE# and WE# must be high for the entire power-down sequence.

The RP# pin is not internally connected to the controller. Therefore, an external loop-back connection between C-RP# and F-RP# must be made on the board even when you are not using the external flash interface. When using the external flash interface, connect the external device to the RP# pin with the loop back. Tri-state RP# at all times when the flash is not in use.

If an external power-up monitoring circuit is connected to the RP# pin with the loop-back, use the following guidelines to avoid contention on the RP# line:

- The power-up sequence on the 3.3-V supply should complete within 50 ms of power-up. The 3.3-V V_{CC} should reach the minimum V_{CC} before 50 ms and RP# should then be released.
- RP# should be driven low by the power-up monitoring circuit during power-up. After power-up, RP# should be tri-stated externally by the power-up monitoring circuit.

- If the preceding guidelines cannot be completed within 50 ms, then the OE pin must be driven low externally until RP# is ready to be released.

Set-Up Time Issue

The set-up time issue described here refers to the revision B silicon of the Altera enhanced configuration devices. The issue described in this errata sheet has now been corrected in the revision C silicon of this device. All revision C devices are fully backward compatible with the revision B devices. As of the date of this errata sheet, the EPC4, EPC8, and EPC16 devices in the 100-pin quad flat pack (QFP) package are shipped with revision C silicon.

The EPC16UC88 device has a special ordering code (EPC16UB88AA) to identify revision C silicon. The EPC16UC88 ordering code is used to deliver revision B silicon at this time. Once the transition from revision B to revision C silicon is complete, the EPC16UC88 ordering code will be used going forward to deliver revision C silicon, and the EPC16UC88AA ordering code will be made obsolete.

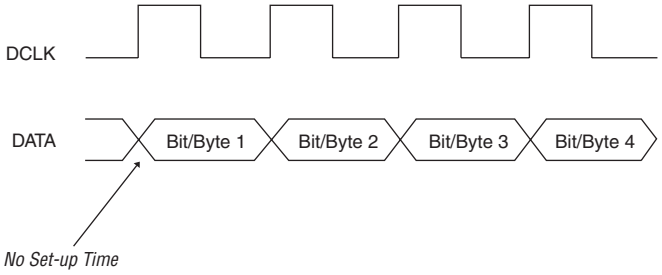
For identification purposes, the fourth character of the 11-character date code indicates the die revision. For a revision B component, this character will be a "B", and for a revision C component, this character will be a "C". For more information regarding the device marking, refer to customer advisories 9916 and 9707.

Customers who are using enhanced configuration devices and configuring one or more SRAM-based devices may encounter configuration device failure. This failure may be temperature- or voltage-dependent.

The problem is due to a set-up time violation of the DATA signal. The enhanced configuration device generates the DATA and DCLK signals so that they arrive at the PLD simultaneously.

The PLD requires a set-up time of 10 ns. However, since the DCLK and DATA signals transition simultaneously, the set-up time at the PLD is actually zero. Figure 1 shows the DATA and DCLK signals generated by enhanced configuration devices.

Figure 1. DATA and DCLK Signals Generated by Enhanced Configuration Devices

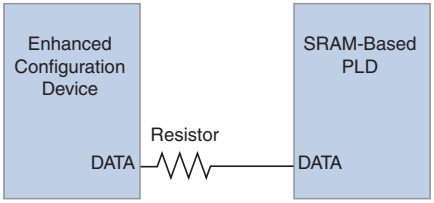


Design Guidelines

To achieve a successful configuration, required set-up time must be provided to the DATA signal or signals of SRAM-based devices. Depending on the layout of the board, there may already be sufficient set-up time at the PLD. Measure the DCLK to DATA relationship at the PLD. If the DATA changes prior to the rising edge of the DCLK signal more than the required set-up time (10 ns for all SRAM-based devices), then the board will configure correctly. If the set-up time parameter is not met, then the DATA signal must be delayed so that it changes after the DCLK transition (DATA latches on next rising edge of the clock). A delay of 10 ns is sufficient to provide the required set-up time for the DATA signal or signals. This delay between DCLK and DATA is measured at the PLD.

The delay is introduced by adding a resistor to the DATA path from the enhanced configuration devices to the SRAM-based PLDs, as shown in Figure 2.

Figure 2. Adding a Resistor to DATA Path

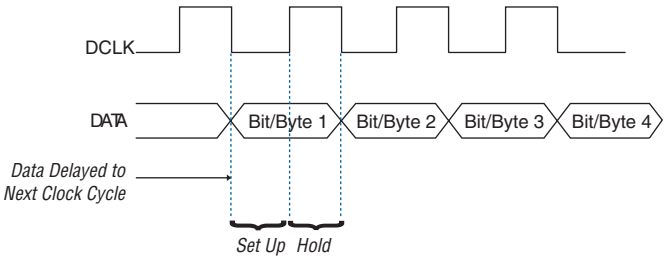


The delay is created by a resistor-capacitor network. The resistor is added to the circuit and the capacitance is provided by the board trace. The RC combination should be chosen such that the path delay is equal to 10 ns.

A typical combination would use a 100- to 200-Ω resistor with a trace length of four inches between the DATA pins of the enhanced configuration device and the PLD.

After inserting the delay, the DATA transition would shift to the right so that the first bit or byte of data would be latched on the second rising edge of DCLK, as shown in Figure 3. This shift meets the required set-up time for the DATA signal.

Figure 3. DATA Latches on Second Rising Edge of DCLK after DATA Path Delay



This technique enables existing enhanced configuration devices to configure PLDs. Future updated versions of enhanced configuration devices will be modified so that the DCLK and DATA signals arrive at the PLD to meet the required set-up time.

A board that is laid out with an in-line resistor will work with updated versions of enhanced configuration devices, but the maximum frequency for configuration would be limited to 33 MHz.

Contact Information

For more information, go to Altera's mySupport website at **www.altera.com/mysupport** and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 1 shows the revision history for this errata sheet.

Table 1. Enhanced Configuration Devices v1.2 Errata Sheet Revision History

Version	Date	Errata Summary
1.2	October 2007	Added section on "Intel-Flash-Based EPC Device Protection". Updated section on "Set-Up Time Issue".
1.1	December 2003	Addressed known issues and includes methods to work around the issues for enhanced configuration devices EPC4, EPC8, and EPC16.

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