1. PLLs in Stratix II and Stratix II GX Devices

SII52001-4.6

Introduction

Stratix® II and Stratix II GX device phase-locked loops (PLLs) provide robust clock management and synthesis for device clock management, external system clock management, and high-speed I/O interfaces. Stratix II devices have up to 12 PLLs, and Stratix II GX devices have up to 8 PLLs. Stratix II and Stratix II GX PLLs are highly versatile and can be used as a zero delay buffer, a jitter attenuator, low skew fan out buffer, or a frequency synthesizer.

Stratix II and Stratix II GX devices feature both enhanced PLLs and fast PLLs. Stratix II and Stratix II GX devices have up to four enhanced PLLs. Stratix II devices have up to eight fast PLLs and Stratix II GX devices have up to four PLLs. Both enhanced and fast PLLs are feature rich, supporting advanced capabilities such as clock switchover, reconfigurable phase shift, PLL reconfiguration, and reconfigurable bandwidth. PLLs can be used for general-purpose clock management, supporting multiplication, phase shifting, and programmable duty cycle. In addition, enhanced PLLs support external clock feedback mode, spread-spectrum clocking, and counter cascading. Fast PLLs offer high speed outputs to manage the high-speed differential I/O interfaces.

Stratix II and Stratix II GX devices also support a power-down mode where clock networks that are not being used can easily be turned off, reducing the overall power consumption of the device. In addition, Stratix II and Stratix II GX PLLs support dynamic selection of the PLL input clock from up to five possible sources, giving you the flexibility to choose from multiple (up to four) clock sources to feed the primary and secondary clock input ports.

The Altera® Quartus® II software enables the PLLs and their features without requiring any external devices.

Tables 1–1 and 1–2 show the PLLs available for each Stratix II and Stratix II GX device, respectively.

Table 1–1. Stratix II Device PLL Availability *Note (1)*

Device	Fast PLLs								Enhanced PLLs			
	1	2	3	4	7	8	9	10	5	6	11	12
EP2S15	✓	✓	✓	✓					✓	✓		
EP2S30	✓	✓	✓	✓					✓	✓		
EP2S60	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP2S90 *(2)*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP2S130 *(3)*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP2S180	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Notes for Table 1–1:

(1) The EP2S60 device in the 1,020-pin package contains 12 PLLs. EP2S60 devices in the 484-pin and 672-pin packages contain fast PLLs 1–4 and enhanced PLLs 5 and 6.

(2) EP2S90 devices in the 1020-pin and 1508-pin packages contain 12 PLLs. EP2S90 devices in the 484-pin and 780-pin packages contain fast PLLs 1–4 and enhanced PLLs 5 and 6.

(3) EP2S130 devices in the 1020-pin and 1508-pin packages contain 12 PLLs. The EP2S130 device in the 780-pin package contains fast PLLs 1–4 and enhanced PLLs 5 and 6.

Table 1–2. Stratix II GX Device PLL Availability *Note (1)*

Device	Fast PLLs								Enhanced PLLs			
	1	2	3 *(3)*	4 *(3)*	7	8	9 *(3)*	10 *(3)*	5	6	11	12
EP2SGX30 *(2)*	✓	✓							✓	✓		
EP2SGX60 *(2)*	✓	✓			✓	✓			✓	✓	✓	✓
EP2SGX90	✓	✓			✓	✓			✓	✓	✓	✓
EP2SGX130	✓	✓			✓	✓			✓	✓	✓	✓

Notes for Table 1–2:

(1) The global or regional clocks in a fast PLL's transceiver block can drive the fast PLL input. A pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

(2) EP2SGX30C and EP2SGX60C devices only have two fast PLLs (PLLs 1 and 2), but the connectivity from these two PLLs to the global and regional clock networks remains the same as shown in this table.

(3) PLLs 3, 4, 9, and 10 are not available in Stratix II GX devices. however, these PLLs are listed in Table 1–2 because the Stratix II GX PLL numbering scheme is consistent with Stratix and Stratix II devices.

Table 1–3 shows the enhanced PLL and fast PLL features in Stratix II and Stratix II GX devices.

Table 1–3. Stratix II and Stratix II GX PLL Features

Feature	Enhanced PLL	Fast PLL
Clock multiplication and division	*m*/(*n* × post-scale counter) *(1)*	*m*/(*n* × post-scale counter) *(2)*
Phase shift	Down to 125-ps increments *(3)*	Down to 125-ps increments *(3)*
Clock switchover	✓	✓ *(4)*
PLL reconfiguration	✓	✓
Reconfigurable bandwidth	✓	✓
Spread-spectrum clocking	✓	
Programmable duty cycle	✓	✓
Number of clock outputs per PLL *(5)*	6	4
Number of dedicated external clock outputs per PLL	Three differential or six single-ended	*(6)*
Number of feedback clock inputs per PLL	1 *(7)*	

Notes to Table 1–3:

(1) For enhanced PLLs, *m* and *n* range from 1 to 512 with 50% duty cycle. Post-scale counters range from 1 to 512 with 50% duty cycle. For non-50% duty-cycle clock outputs, post-scale counters range from 1 to 256.

(2) For fast PLLs, *n* can range from 1 to 4. The post-scale and *m* counters range from 1 to 32. For non-50% duty-cycle clock outputs, post-scale counters range from 1 to 16.

(3) The smallest phase shift is determined by the voltage controlled oscillator (VCO) period divided by eight. The supported phase-shift range is from 125 to 250 ps. Stratix II and Stratix II GX devices can shift all output frequencies in increments of at least 45°. Smaller degree increments are possible depending on the frequency and divide parameters. For non-50% duty cycle clock outputs post-scale counters range from 1 to 256.

(4) Stratix II and Stratix II GX fast PLLs only support manual clock switchover.

(5) The clock outputs can be driven to internal clock networks or to a pin.

(6) The PLL clock outputs of the fast PLLs can drive to any I/O pin to be used as an external clock output. For high-speed differential I/O pins, the device uses a data channel to generate the transmitter output clock (`txclkout`).

(7) If the design uses external feedback input pins, you will lose one (or two, if f_{BIN} is differential) dedicated output clock pin.

Figure 1–1 shows a top-level diagram of Stratix II device and PLL locations. Figure 1–2 shows a top-level diagram of Stratix II device and PLL locations. See "Clock Control Block" on page 1–86 for more detail on PLL connections to global and regional clocks networks.

Figure 1–1. Stratix II PLL Locations

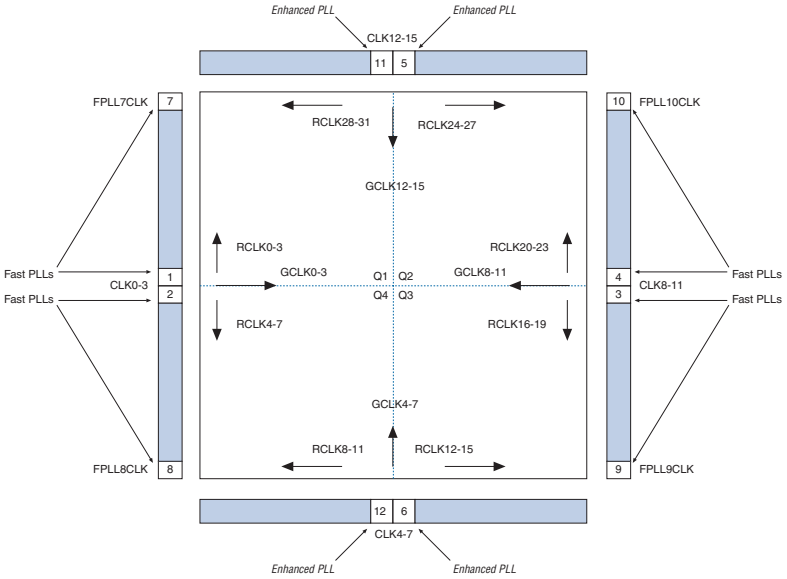
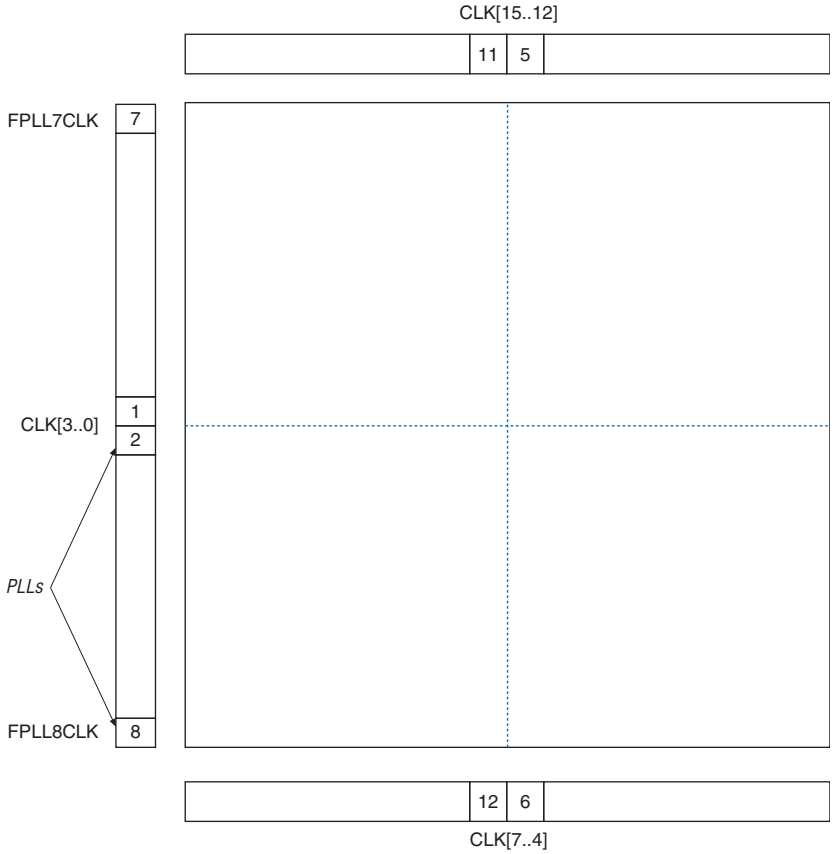


Figure 1–2. Stratix II GX PLL Locations



Enhanced PLLs

Stratix II and Stratix II GX devices contain up to four enhanced PLLs with advanced clock management features. The main goal of a PLL is to synchronize the phase and frequency of an internal and external clock to an input reference clock. There are a number of components that comprise a PLL to achieve this phase alignment.

Enhanced PLL Hardware Overview

Stratix II and Stratix II GX PLLs align the rising edge of the reference input clock to a feedback clock using the phase-frequency detector (PFD). The falling edges are determined by the duty-cycle specifications. The PFD produces an up or down signal that determines whether the VCO needs to operate at a higher or lower frequency.

The PFD output is applied to the charge pump and loop filter, which produces a control voltage for setting the VCO frequency. If the PFD produces an up signal, then the VCO frequency increases. A down signal decreases the VCO frequency. The PFD outputs these up and down signals to a charge pump. If the charge pump receives an up signal, current is driven into the loop filter. Conversely, if it receives a down signal, current is drawn from the loop filter.

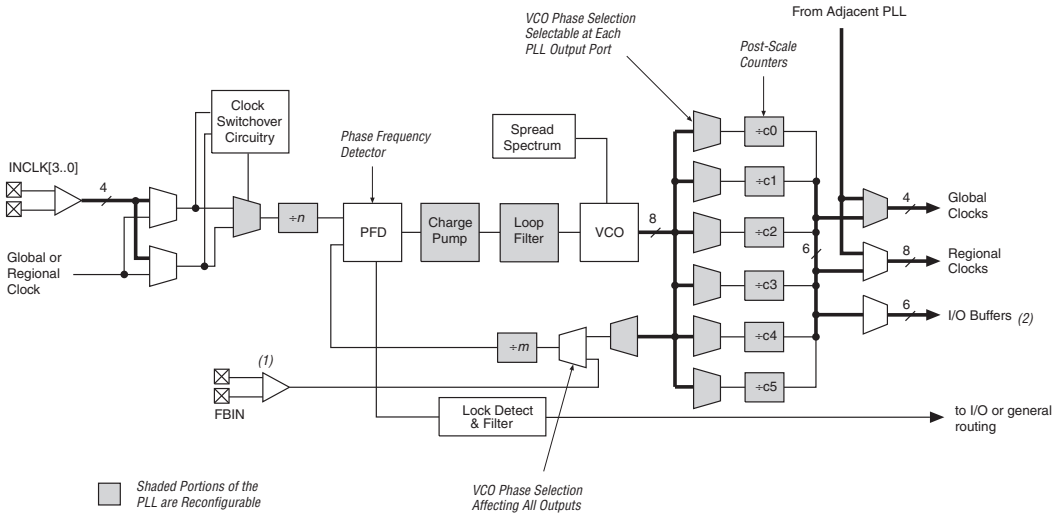
The loop filter converts these up and down signals to a voltage that is used to bias the VCO. The loop filter also removes glitches from the charge pump and prevents voltage over-shoot, which filters the jitter on the VCO.

The voltage from the loop filter determines how fast the VCO operates. The VCO is implemented as a four-stage differential ring oscillator. A divide counter (*m*) is inserted in the feedback loop to increase the VCO frequency above the input reference frequency. VCO frequency (f_{VCO}) is equal to (*m*) times the input reference clock (f_{REF}). The input reference clock (f_{REF}) to the PFD is equal to the input clock (f_{IN}) divided by the pre-scale counter (*n*). Therefore, the feedback clock (f_{FB}) applied to one input of the PFD is locked to the f_{REF} that is applied to the other input of the PFD.

The VCO output can feed up to six post-scale counters (`C0`, `C1`, `C2`, `C3`, `C4`, and `C5`). These post-scale counters allow a number of harmonically related frequencies to be produced within the PLL.

Figure 1–3 shows a simplified block diagram of the major components of the Stratix II and Stratix II GX enhanced PLL. Figure 1–4 shows the enhanced PLL's outputs and dedicated clock outputs.

Figure 1–3. Stratix II and Stratix II GX Enhanced PLL



Notes to Figure 1–3:

(1) Each clock source can come from any of the four clock pins located on the same side of the device as the PLL.

(2) PLLs 5, 6, 11, and 12 each have six single-ended dedicated clock outputs or three differential dedicated clock outputs.

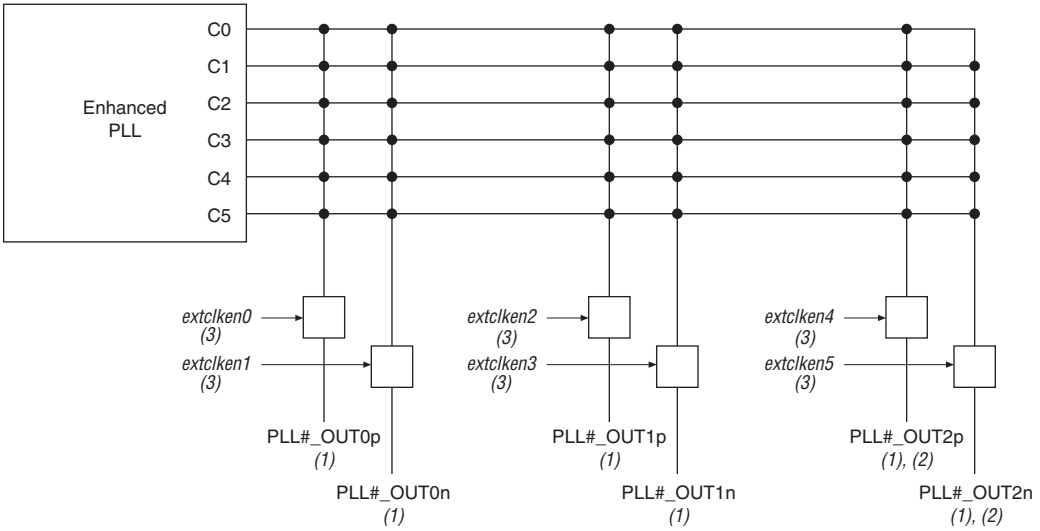
(3) If the design uses external feedback input pins, you will lose one (or two, if f_{BIN} is differential) dedicated output clock pin. Every Stratix II and Stratix II GX device has at least two enhanced PLLs with one single-ended or differential external feedback input per PLL.

(4) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

External Clock Outputs

Enhanced PLLs 5, 6, 11, and 12 each support up to six single-ended clock outputs (or three differential pairs). See Figure 1–4.

Figure 1–4. External Clock Outputs for Enhanced PLLs 5, 6, 11 and 12



Notes to Figure 1–4:

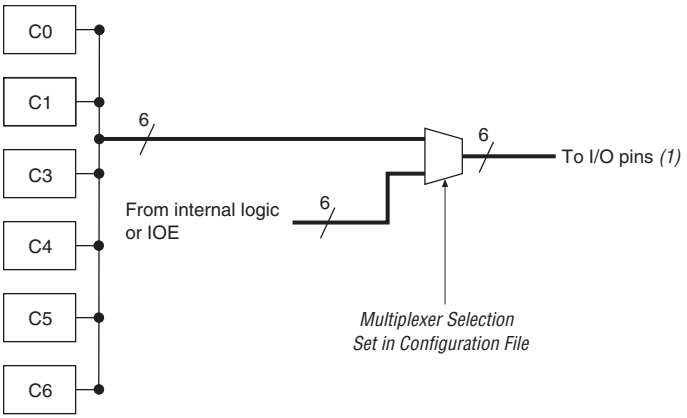
(1) These clock output pins can be fed by any one of the `C[5..0]` counters.

(2) These clock output pins are used as either external clock outputs or for external feedback. If the design uses external feedback input pins, you will lose one (or two, if f_{BIN} is differential) dedicated output clock pin.

(3) These external clock enable signals are available only when using the `altclkctrl` megafunction.

Any of the six output counters `C[5..0]` can feed the dedicated external clock outputs, as shown in Figure 1–5. Therefore, one counter or frequency can drive all output pins available from a given PLL. The dedicated output clock pins (`PLL_OUT`) from each enhanced PLL are powered by a separate power pin (e.g., `VCC_PLL5_OUT`, `VCC_PLL6_OUT`, etc.), reducing the overall output jitter by providing improved isolation from switching I/O pins.

Figure 1–5. External Clock Output Connectivity to PLL Output Counters for Enhanced PLLs 5, 6, 11 and 12 Note (1)



Note to Figure 1–5:

(1) The design can use each external clock output pin as a general-purpose output pin from the logic array. These pins are multiplexed with I/O element (IOE) outputs.

Each pin of a single-ended output pair can either be in phase or 180° out of phase. The Quartus II software places the NOT gate in the design into the IOE to implement 180° phase with respect to the other pin in the pair. The clock output pin pairs support the same I/O standards as standard output pins (in the top and bottom banks) as well as LVDS, LVPECL, differential HSTL, and differential SSTL. See Table 1–6, in the "Enhanced PLL Pins" section on page 1–12 to determine which I/O standards the enhanced PLL clock pins support.

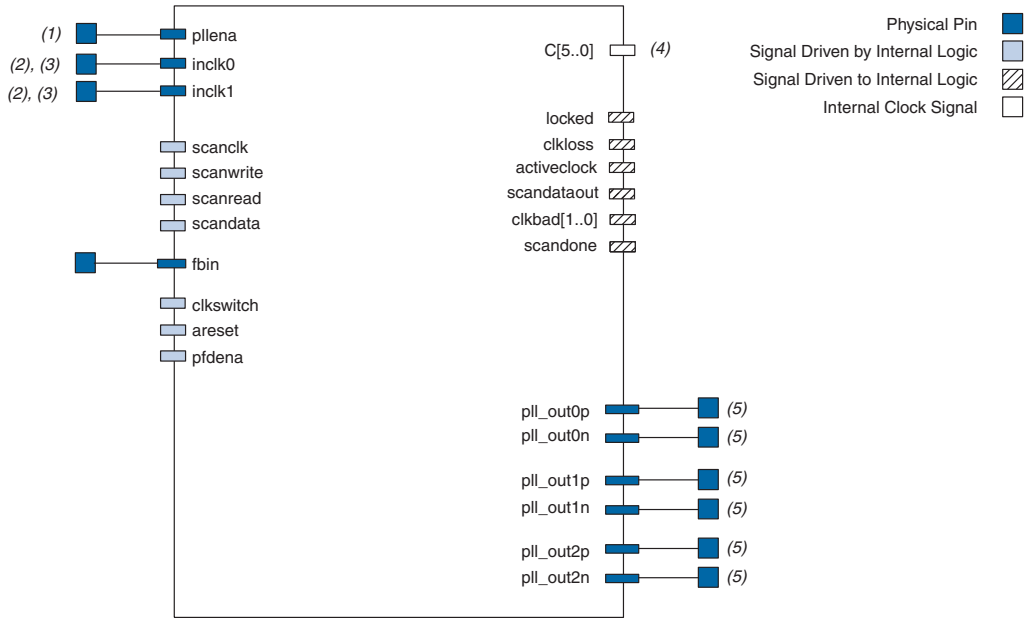
When in single-ended or differential mode, one power pin supports six single-ended or three differential outputs. Both outputs use the same I/O standard in single-ended mode to maintain performance. You can also use the external clock output pins as user output pins if external enhanced PLL clocking is not needed.

The enhanced PLL can also drive out to any regular I/O pin through the global or regional clock network.

Enhanced PLL Software Overview

Stratix II and Stratix II GX enhanced PLLs are enabled in the Quartus II software by using the `altpll` megafunction. Figure 1–6 shows the available ports (as they are named in the Quartus II `altpll` megafunction) of the Stratix II and Stratix II GX enhanced PLL.

Figure 1–6. Enhanced PLL Ports



Notes to Figure 1–6:

(1) Enhanced and fast PLLs share this input pin.
(2) These are either single-ended or differential pins.
(3) The primary and secondary clock input can be fed from any one of four clock pins located on the same side of the device as the PLL.
(4) Can drive to the global or regional clock networks or the dedicated external clock output pins.
(5) These dedicated output clocks are fed by the `C[5..0]` counters.

Tables 1–4 and 1–5 describe all the enhanced PLL ports.

Table 1–4. Enhanced PLL Input Signals (Part 1 of 2)

Port	Description	Source	Destination
`inclk0`	Primary clock input to the PLL.	Pin or another PLL	*n* counter
`inclk1`	Secondary clock input to the PLL.	Pin or another PLL	*n* counter
`fbin`	External feedback input to the PLL.	Pin	PFD
`pllena`	Enable pin for enabling or disabling all or a set of PLLs. Active high.	Pin	General PLL control signal
`clkswitch`	Switch-over signal used to initiate external clock switch-over control. Active high.	Logic array	PLL switch-over circuit

Table 1–4. Enhanced PLL Input Signals (Part 2 of 2)

Port	Description	Source	Destination
areset	Signal used to reset the PLL which resynchronizes all the counter outputs. Active high.	Logic array	General PLL control signal
pfdena	Enables the outputs from the phase frequency detector. Active high.	Logic array	PFD
scanclk	Serial clock signal for the real-time PLL reconfiguration feature.	Logic array	Reconfiguration circuit
scandata	Serial input data stream for the real-time PLL reconfiguration feature.	Logic array	Reconfiguration circuit
scanwrite	Enables writing the data in the scan chain into the PLL. Active high.	Logic array	Reconfiguration circuit
scanread	Enables scan data to be written into the scan chain. Active high.	Logic array	Reconfiguration circuit

Table 1–5. Enhanced PLL Output Signals (Part 1 of 2)

Port	Description	Source	Destination
c[5..0]	PLL output counters driving regional, global or external clocks.	PLL counter	Internal or external clock
pll_out [2..0]p pll_out [2..0]n	These are three differential or six single-ended external clock output pins fed from the C[5..0] PLL counters, and every output can be driven by any counter. *p* and *n* are the positive (*p*) and negative (*n*) pins for differential pins.	PLL counter	Pin(s)
clkloss	Signal indicating the switch-over circuit detected a switch-over condition.	PLL switch-over circuit	Logic array
clkbad[1..0]	Signals indicating which reference clock is no longer toggling. clkbad1 indicates inclk1 status, clkbad0 indicates inclk0 status. 1= good; 0=bad	PLL switch-over circuit	Logic array
locked	Lock or gated lock output from lock detect circuit. Active high.	PLL lock detect	Logic array
activeclock	Signal to indicate which clock (0 = inclk0 or 1 = inclk1) is driving the PLL. If this signal is low, inclk0 drives the PLL, If this signal is high, inclk1 drives the PLL	PLL clock multiplexer	Logic array

Table 1–5. Enhanced PLL Output Signals (Part 2 of 2)			
Port	**Description**	**Source**	**Destination**
scandataout	Output of the last shift register in the scan chain.	PLL scan chain	Logic array
scandone	Signal indicating when the PLL has completed reconfiguration. 1 to 0 transition indicates that the PLL has been reconfigured.	PLL scan chain	Logic array

Enhanced PLL Pins

Table 1–6 lists the I/O standards support by the enhanced PLL clock outputs.

Table 1–6. I/O Standards Supported for Enhanced PLL Pins (Part 1 of 2) Note (1)			
I/O Standard	**Input**		**Output**
	INCLK	**FBIN**	**EXTCLK**
LVTTL	✓	✓	✓
LVCMOS	✓	✓	✓
2.5 V	✓	✓	✓
1.8 V	✓	✓	✓
1.5 V	✓	✓	✓
3.3-V PCI	✓	✓	✓
3.3-V PCI-X	✓	✓	✓
SSTL-2 Class I	✓	✓	✓
SSTL-2 Class II	✓	✓	✓
SSTL-18 Class I	✓	✓	✓
SSTL-18 Class II	✓	✓	✓
1.8-V HSTL Class I	✓	✓	✓
1.8-V HSTL Class II	✓	✓	✓
1.5-V HSTL Class I	✓	✓	✓
1.5-V HSTL Class II	✓	✓	✓
1.2-V HSTL Class I	✓	✓	✓
1.2-V HSTL Class II	✓	✓	✓

Table 1–6. I/O Standards Supported for Enhanced PLL Pins (Part 2 of 2) *Note (1)*

I/O Standard	Input		Output
	INCLK	FBIN	EXTCLK
Differential SSTL-2 Class I	✓	✓	✓
Differential SSTL-2 Class II	✓	✓	✓
Differential SSTL-18 Class I	✓	✓	✓
Differential SSTL-18 Class II	✓	✓	✓
1.8-V differential HSTL Class I	✓	✓	✓
1.8-V differential HSTL Class II	✓	✓	✓
1.5-V differential HSTL Class I	✓	✓	✓
1.5-V differential HSTL Class II	✓	✓	✓
LVDS	✓	✓	✓
HyperTransport technology			
Differential LVPECL	✓	✓	✓

Note to Table 1–6:
(1) The enhanced PLL external clock output bank does not allow a mixture of both single-ended and differential I/O standards.

Table 1–7 shows the physical pins and their purpose for the Stratix II and Stratix II GX enhanced PLLs. For `inclk` port connections to pins see "Clock Control Block" on page 1–86.

Table 1–7. Stratix II and Stratix II GX Enhanced PLL Pins (Part 1 of 3) *Note (1)*

Pin	Description
CLK4p/n	Single-ended or differential pins that can drive the `inclk` port for PLLs 6 or 12.
CLK5p/n	Single-ended or differential pins that can drive the `inclk` port for PLLs 6 or 12.
CLK6p/n	Single-ended or differential pins that can drive the `inclk` port for PLLs 6 or 12.
CLK7p/n	Single-ended or differential pins that can drive the `inclk` port for PLLs 6 or 12.
CLK12p/n	Single-ended or differential pins that can drive the `inclk` port for PLLs 5 or 11.
CLK13p/n	Single-ended or differential pins that can drive the `inclk` port for PLLs 5 or 11.
CLK14p/n	Single-ended or differential pins that can drive the `inclk` port for PLLs 5 or 11.
CLK15p/n	Single-ended or differential pins that can drive the `inclk` port for PLLs 5 or 11.
PLL5_FBp/n	Single-ended or differential pins that can drive the `fbin` port for PLL 5.

Table 1–7. Stratix II and Stratix II GX Enhanced PLL Pins (Part 2 of 3) *Note (1)*

Pin	Description
PLL6_FBp/n	Single-ended or differential pins that can drive the fbin port for PLL 6.
PLL11_FBp/n	Single-ended or differential pins that can drive the fbin port for PLL 11.
PLL12_FBp/n	Single-ended or differential pins that can drive the fbin port for PLL 12.
PLL_ENA	Dedicated input pin that drives the pllena port of all or a set of PLLs. If you do not use this pin, connect it to ground.
PLL5_OUT[2..0]p/n	Single-ended or differential pins driven by C[5..0] ports from PLL 5.
PLL6_OUT[2..0]p/n	Single-ended or differential pins driven by C[5..0] ports from PLL 6.
PLL11_OUT[2..0]p/n	Single-ended or differential pins driven by C[5..0] ports from PLL 11.
PLL12_OUT[2..0]p/n	Single-ended or differential pins driven by C[5..0] ports from PLL 12.
VCCA_PLL5	Analog power for PLL 5. You must connect this pin to 1.2 V, even if the PLL is not used.
GNDA_PLL5	Analog ground for PLL 5. You can connect this pin to the GND plane on the board.
VCCA_PLL6	Analog power for PLL 6. You must connect this pin to 1.2 V, even if the PLL is not used.
GNDA_PLL6	Analog ground for PLL 6. You can connect this pin to the GND plane on the board.
VCCA_PLL11	Analog power for PLL 11. You must connect this pin to 1.2 V, even if the PLL is not used.
GNDA_PLL11	Analog ground for PLL 11. You can connect this pin to the GND plane on the board.
VCCA_PLL12	Analog power for PLL 12. You must connect this pin to 1.2 V, even if the PLL is not used.
GNDA_PLL12	Analog ground for PLL 12. You can connect this pin to the GND plane on the board.
VCCD_PLL	Digital power for PLLs. You must connect this pin to 1.2 V, even if the PLL is not used.
VCC_PLL5_OUT	External clock output V_{CCIO} power for PLL5_OUT0p, PLL5_OUT0n, PLL5_OUT1p, PLL5_OUT1n, PLL5_OUT2p, and PLL5_OUT2n outputs from PLL 5.
VCC_PLL6_OUT	External clock output V_{CCIO} power for PLL6_OUT0p, PLL6_OUT0n, PLL6_OUT1p, PLL6_OUT1n and PLL6_OUT2p, PLL6_OUT2n outputs from PLL 6.
VCC_PLL11_OUT	External clock output V_{CCIO} power for PLL11_OUT0p, PLL11_OUT0n, PLL11_OUT1p, PLL11_OUT1n and PLL11_OUT2p, PLL11_OUT2n outputs from PLL 11.

Table 1–7. Stratix II and Stratix II GX Enhanced PLL Pins (Part 3 of 3) Note (1)	
Pin	**Description**
VCC_PLL12_OUT	External clock output V_{CCIO} power for PLL12_OUT0p, PLL12_OUT0n, PLL12_OUT1p, PLL12_OUT1n and PLL12_OUT2p, PLL12_OUT2n outputs from PLL 12.

Note to Table 1–7:
(1) The negative leg pins (CLKn, PLL_FBn, and PLL_OUTn) are only required with differential signaling.

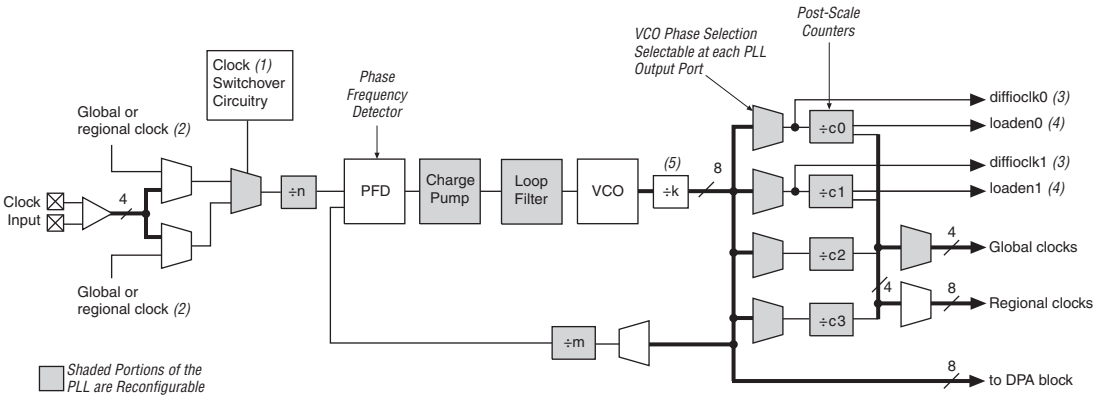
Fast PLLs

Stratix II devices contain up to eight fast PLLs and Stratix II GX devices contain up to four fast PLLs. Fast PLLs have high-speed differential I/O interface capability along with general-purpose features.

Fast PLL Hardware Overview

Figure 1–7 shows a diagram of the fast PLL.

Figure 1–7. Stratix II and Stratix II GX Fast PLL Block Diagram



Notes to Figure 1–7:
(1) Stratix II and Stratix II GX fast PLLs only support manual clock switchover.
(2) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.
(3) In high-speed differential I/O support mode, this high-speed PLL clock feeds the SERDES. Stratix II devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.
(4) This signal is a high-speed differential I/O support SERDES control signal.
(5) If the design enables this ÷2 counter, then the device can use a VCO frequency range of 150 to 520 MHz.

External Clock Outputs

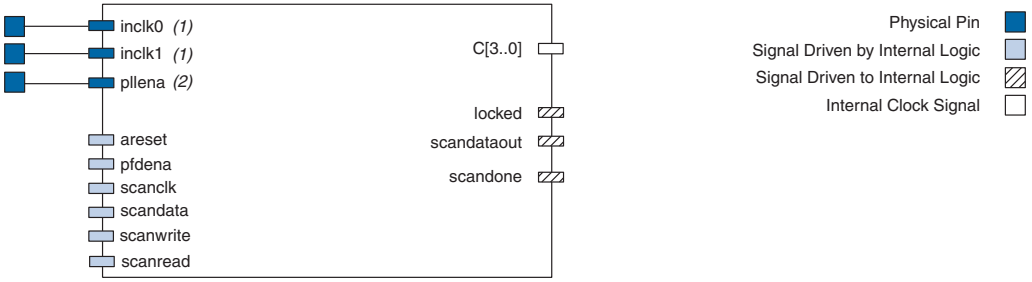
Each fast PLL supports differential or single-ended outputs for source-synchronous transmitters or for general-purpose external clocks. There are no dedicated external clock output pins. The fast PLL global or regional outputs can drive any I/O pin as an external clock output pin. The I/O standards supported by any particular bank determines what standards are possible for an external clock output driven by the fast PLL in that bank.

For more information, see the *Selectable I/O Standards in Stratix II and Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* (or the *Stratix II Device Handbook*).

Fast PLL Software Overview

Stratix II and Stratix II GX fast PLLs are enabled in the Quartus II software by using the `altpll` megafunction. Figure 1–8 shows the available ports (as they are named in the Quartus II `altpll` megafunction) of the Stratix II or Stratix II GX fast PLL.

Figure 1–8. Stratix II and Stratix II GX Fast PLL Ports and Physical Destinations



Notes to Figure 1–8:
(1) This input pin is either single-ended or differential.
(2) This input pin is shared by all enhanced and fast PLLs.

Tables 1–8 and 1–9 show the description of all fast PLL ports.

Table 1–8. Fast PLL Input Signals (Part 1 of 2)

Name	Description	Source	Destination
`inclk0`	Primary clock input to the fast PLL.	Pin or another PLL	*n* counter
`inclk1`	Secondary clock input to the fast PLL.	Pin or another PLL	*n* counter

Table 1–8. Fast PLL Input Signals (Part 2 of 2)

Name	Description	Source	Destination
pllena	Enable pin for enabling or disabling all or a set of PLLs. Active high.	Pin	PLL control signal
clkswitch	Switch-over signal used to initiate external clock switch-over control. Active high.	Logic array	Reconfiguration circuit
areset	Enables the up/down outputs from the phase-frequency detector. Active high.	Logic array	PLL control signal
pfdena	Enables the up/down outputs from the phase-frequency detector. Active high.	Logic array	PFD
scanclk	Serial clock signal for the real-time PLL control feature.	Logic array	Reconfiguration circuit
scandata	Serial input data stream for the real-time PLL control feature.	Logic array	Reconfiguration circuit
scanwrite	Enables writing the data in the scan chain into the PLL Active high.	Logic array	Reconfiguration circuit
scanread	Enables scan data to be written into the scan chain Active high.	Logic array	Reconfiguration circuit

Table 1–9. Fast PLL Output Signals

Name	Description	Source	Destination
c[3..0]	PLL outputs driving regional or global clock.	PLL counter	Internal clock
locked	Lock or gated lock output from lock detect circuit. Active high.	PLL lock detect	Logic array
scandataout	Output of the last shift register in the scan chain.	PLL scan chain	Logic array
scandone	Signal indicating when the PLL has completed reconfiguration. 1 to 0 transition indicates the PLL has been reconfigured.	PLL scan chain	Logic array

Fast PLL Pins

Table 1–10 shows the I/O standards supported by the fast PLL input pins.

Table 1–10. I/O Standards Supported for Stratix II and Stratix II GX Fast PLL Pins

I/O Standard	INCLK
LVTTL	✓
LVCMOS	✓
2.5 V	✓
1.8 V	✓
1.5 V	✓
3.3-V PCI	
3.3-V PCI-X	
SSTL-2 Class I	✓
SSTL-2 Class II	✓
SSTL-18 Class I	✓
SSTL-18 Class II	✓
1.8-V HSTL Class I	✓
1.8-V HSTL Class II	✓
1.5-V HSTL Class I	✓
1.5-V HSTL Class II	✓
Differential SSTL-2 Class I	
Differential SSTL-2 Class II	
Differential SSTL-18 Class I	
Differential SSTL-18 Class II	
1.8-V differential HSTL Class I	
1.8-V differential HSTL Class II	
1.5-V differential HSTL Class I	
1.5-V differential HSTL Class II	
LVDS	✓
HyperTransport technology	✓
Differential LVPECL	

Table 1–11 shows the physical pins and their purpose for the fast PLLs. For inclk port connections to pins, see "Clocking" on page 1–62.

Table 1–11. Fast PLL Pins (Part 1 of 2) *Note (1)*

Pin	Description
CLK0p/n	Single-ended or differential pins that can drive the inclk port for PLLs 1, 2, 7 or 8.
CLK1p/n	Single-ended or differential pins that can drive the inclk port for PLLs 1, 2, 7 or 8.
CLK2p/n	Single-ended or differential pins that can drive the inclk port for PLLs 1, 2, 7 or 8.
CLK3p/n	Single-ended or differential pins that can drive the inclk port for PLLs 1, 2, 7 or 8.
CLK8p/n	Single-ended or differential pins that can drive the inclk port for PLLs 3, 4, 9 or 10.
CLK9p/n	Single-ended or differential pins that can drive the inclk port for PLLs 3, 4, 9 or 10.
CLK10p/n	Single-ended or differential pins that can drive the inclk port for PLLs 3, 4, 9 or 10.
CLK11p/n	Single-ended or differential pins that can drive the inclk port for PLLs 3, 4, 9 or 10.
FPLL7CLKp/n	Single-ended or differential pins that can drive the inclk port for PLL 7.
FPLL8CLKp/n	Single-ended or differential pins that can drive the inclk port for PLL 8.
FPLL9CLKp/n	Single-ended or differential pins that can drive the inclk port for PLL 9.
FPLL10CLKp/n	Single-ended or differential pins that can drive the inclk port for PLL 10.
PLL_ENA	Dedicated input pin that drives the pllena port of all or a set of PLLs. If you do not use this pin, connect it to GND.
VCCD_PLL	Digital power for PLLs. You must connect this pin to 1.2 V, even if the PLL is not used.
VCCA_PLL1	Analog power for PLL 1. You must connect this pin to 1.2 V, even if the PLL is not used.
GNDA_PLL1	Analog ground for PLL 1. Your can connect this pin to the GND plane on the board.
VCCA_PLL2	Analog power for PLL 2. You must connect this pin to 1.2 V, even if the PLL is not used.
GNDA_PLL2	Analog ground for PLL 2. You can connect this pin to the GND plane on the board.
VCCA_PLL3	Analog power for PLL 3. You must connect this pin to 1.2 V, even if the PLL is not used.
GNDA_PLL3	Analog ground for PLL 3. You can connect this pin to the GND plane on the board.
VCCA_PLL4	Analog power for PLL 4. You must connect this pin to 1.2 V, even if the PLL is not used.
GNDA_PLL4	Analog ground for PLL 4. You can connect this pin to the GND plane on the board.
GNDA_PLL7	Analog ground for PLL 7. You can connect this pin to the GND plane on the board.
VCCA_PLL8	Analog power for PLL 8. You must connect this pin to 1.2 V, even if the PLL is not used.
GNDA_PLL8	Analog ground for PLL 8. You can connect this pin to the GND plane on the board.
VCCA_PLL9	Analog power for PLL 9. You must connect this pin to 1.2 V, even if the PLL is not used.
GNDA_PLL9	Analog ground for PLL 9. You can connect this pin to the GND plane on the board.
VCCA_PLL10	Analog power for PLL 10. You must connect this pin to 1.2 V, even if the PLL is not used.

Table 1–11. Fast PLL Pins (Part 2 of 2) Note (1)	
Pin	**Description**
GNDA_PLL10	Analog ground for PLL 10. You can connect this pin to the GND plane on the board.

Note to Table 1–11:
(1) The negative leg pins (CLKn and FPLL_CLKn) are only required with differential signaling.

Clock Feedback Modes

Stratix II and Stratix II GX PLLs support up to five different clock feedback modes. Each mode allows clock multiplication and division, phase shifting, and programmable duty cycle. Each PLL must be driven by one of its own dedicated clock input pins for proper clock compensation. The clock input pin connections for each PLL are listed in Table 1–20 on page 1–70.

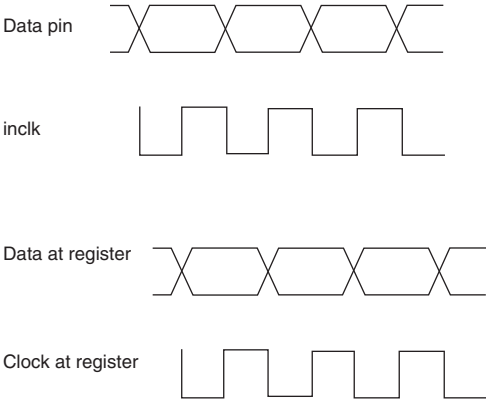
Table 1–12 shows which modes are supported by which PLL type.

Table 1–12. Clock Feedback Mode Availability		
Clock Feedback Mode	**Mode Available in**	
	Enhanced PLLs	**Fast PLLs**
Source synchronous mode	Yes	Yes
No compensation mode	Yes	Yes
Normal mode	Yes	Yes
Zero delay buffer mode	Yes	No
External feedback mode	Yes	No

Source-Synchronous Mode

If data and clock arrive at the same time at the input pins, they are guaranteed to keep the same phase relationship at the clock and data ports of any IOE input register. Figure 1–9 shows an example waveform of the clock and data in this mode. This mode is recommended for source-synchronous data transfers. Data and clock signals at the IOE experience similar buffer delays as long as the same I/O standard is used.

Figure 1–9. Phase Relationship Between Clock and Data in Source-Synchronous Mode



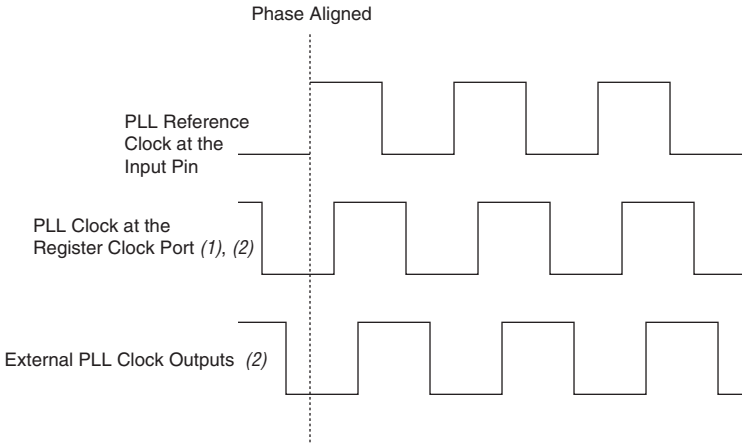
In source-synchronous mode, enhanced PLLs compensate for clock delay to the top and bottom IO registers and fast PLLs compensate for clock delay to the side IO registers. While implementing source-synchronous receivers in these IO banks, use the corresponding PLL type for best matching between clock and data delays (from input pins to register ports).

Set the input pin to the register delay chain within the IOE to zero in the Quartus II software for all data pins clocked by a source-synchronous mode PLL.

No Compensation Mode

In this mode, the PLL does not compensate for any clock networks. This provides better jitter performance because the clock feedback into the PFD does not pass through as much circuitry. Both the PLL internal and external clock outputs are phase shifted with respect to the PLL clock input. Figure 1–10 shows an example waveform of the PLL clocks' phase relationship in this mode.

Figure 1–10. Phase Relationship between PLL Clocks in No Compensation Mode

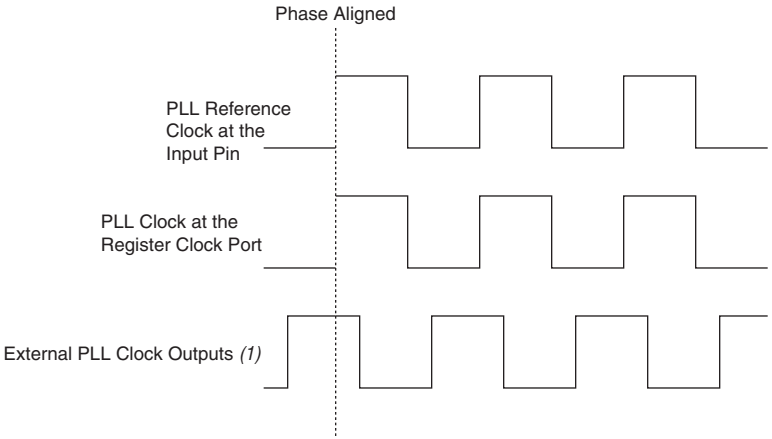


Notes to Figure 1–10.
(1) Internal clocks fed by the PLL are phase-aligned to each other.
(2) The PLL clock outputs can lead or lag the PLL input clocks.

Normal Mode

An internal clock in normal mode is phase-aligned to the input clock pin. The external clock output pin will have a phase delay relative to the clock input pin if connected in this mode. In normal mode, the delay introduced by the GCLK or RCLK network is fully compensated. Figure 1–11 shows an example waveform of the PLL clocks' phase relationship in this mode.

Figure 1–11. Phase Relationship Between PLL Clocks in Normal Mode

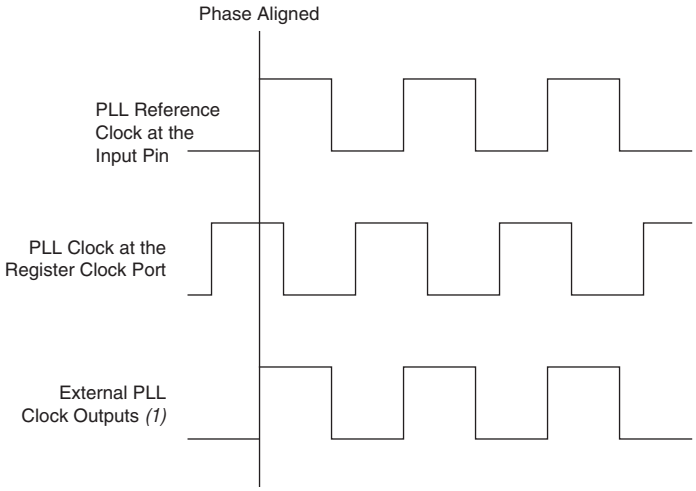


Note to Figure 1–11:
(1) The external clock output can lead or lag the PLL internal clock signals.

Zero Delay Buffer Mode

In the zero delay buffer mode, the external clock output pin is phase-aligned with the clock input pin for zero delay through the device. Figure 1–12 shows an example waveform of the PLL clocks' phase relationship in this mode. When using this mode, Altera requires that you use the same I/O standard on the input clock, and output clocks. When using single-ended I/O standards, the `inclk` port of the PLL must be fed by the dedicated `CLKp` input pin.

Figure 1–12. Phase Relationship Between PLL Clocks in Zero Delay Buffer Mode

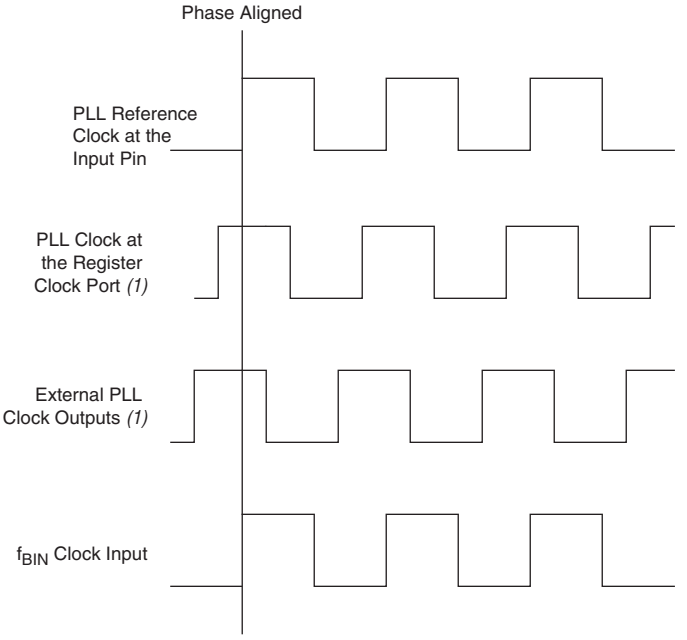


Note to Figure 1–12:
(1) The internal PLL clock output can lead or lag the external PLL clock outputs.

External Feedback Mode

In the external feedback mode, the external feedback input pin, `fbin`, is phase-aligned with the clock input pin, (see Figure 1–13). Aligning these clocks allows you to remove clock delay and skew between devices. This mode is possible on all enhanced PLLs. PLLs 5, 6, 11, and 12 support feedback for one of the dedicated external outputs, either one single-ended or one differential pair. In this mode, one *C* counter feeds back to the PLL `fbin` input, becoming part of the feedback loop. In this mode, you will be using one of the dedicated external clock outputs (two if a differential I/O standard is used) as the PLL `fbin` input pin. When using this mode, Altera requires that you use the same I/O standard on the input clock, feedback input, and output clocks. When using single-ended I/O standards, the `inclk` port of the PLL must be fed by the dedicated `CLKp` input pin.

Figure 1–13. Phase Relationship Between PLL Clocks in External Feedback Mode



Note to Figure 1–13:
(1) The PLL clock outputs can lead or lag the f_{BIN} clock input.

Hardware Features

Stratix II and Stratix II GX PLLs support a number of features for general-purpose clock management. This section discusses clock multiplication and division implementation, phase-shifting implementations and programmable duty cycles. Table 1–13 shows which feature is available in which type of Stratix II or Stratix II GX PLL.

Table 1–13. Stratix II and Stratix II GX PLL Hardware Features (Part 1 of 2)

Hardware Features	Availability	
	Enhanced PLL	Fast PLL
Clock multiplication and division	*m* (*n* × post-scale counter)	*m* (*n* × post-scale counter)
m counter value	Ranges from 1 through 512	Ranges from 1 through 32
n counter value	Ranges from 1 through 512	Ranges from 1 through 4
Post-scale counter values	Ranges from 1 through 512 *(1)*	Ranges from 1 through 32 *(2)*

Table 1–13. Stratix II and Stratix II GX PLL Hardware Features (Part 2 of 2)		
Hardware Features	Availability	
	Enhanced PLL	Fast PLL
Phase shift	Down to 125-ps increments *(3)*	Down to 125-ps increments *(3)*
Programmable duty cycle	Yes	Yes

Notes to Table 1–13:

(1) Post-scale counters range from 1 through 512 if the output clock uses a 50% duty cycle. For any output clocks using a non-50% duty cycle, the post-scale counters range from 1 through 256.

(2) Post-scale counters range from 1 through 32 if the output clock uses a 50% duty cycle. For any output clocks using a non-50% duty cycle, the post-scale counters range from 1 through 16.

(3) The smallest phase shift is determined by the VCO period divided by 8. For degree increments, the Stratix II device can shift all output frequencies in increments of at least 45°. Smaller degree increments are possible depending on the frequency and divide parameters.

Clock Multiplication and Division

Each Stratix II PLL provides clock synthesis for PLL output ports using $m/(n \times$ post-scale counter) scaling factors. The input clock is divided by a pre-scale factor, n, and is then multiplied by the m feedback factor. The control loop drives the VCO to match f_{IN} (m/n). Each output port has a unique post-scale counter that divides down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets its frequency specifications. For example, if output frequencies required from one PLL are 33 and 66 MHz, then the Quartus II software sets the VCO to 660 MHz (the least common multiple of 33 and 66 MHz within the VCO range). Then, the post-scale counters scale down the VCO frequency for each output port.

There is one pre-scale counter, n, and one multiply counter, m, per PLL, with a range of 1 to 512 for both m and n in enhanced PLLs. For fast PLLs, m ranges from 1 to 32 while n ranges from 1 to 4. There are six generic post-scale counters in enhanced PLLs that can feed regional clocks, global clocks, or external clock outputs, all ranging from 1 to 512 with a 50% duty cycle setting for each PLL. The post-scale counters range from 1 to 256 with any non-50% duty cycle setting. In fast PLLs, there are four post-scale counters (`C0`, `C1`, `C2`, `C3`) for the regional and global clock output ports. All post-scale counters range from 1 to 32 with a 50% duty cycle setting. For non-50% duty cycle clock outputs, the post-scale counters range from 1 to 16. If the design uses a high-speed I/O interface, you can connect the dedicated `dffioclk` clock output port to allow the high-speed VCO frequency to drive the serializer/deserializer (SERDES).

The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered into the `altpll` megafunction.

Phase-Shift Implementation

Phase shift is used to implement a robust solution for clock delays in Stratix II and Stratix II GX devices. Phase shift is implemented by using a combination of the VCO phase output and the counter starting time. The VCO phase output and counter starting time is the most accurate method of inserting delays, since it is purely based on counter settings, which are independent of process, voltage, and temperature.

Stratix II and Stratix II GX PLLs do not support programmable delay elements because these delay elements require considerable area on the die and are sensitive to process, voltage, and temperature.

You can phase shift the output clocks from the Stratix II or Stratix II GX enhanced PLL in either:

- Fine resolution using VCO phase taps
- Coarse resolution using counter starting time

The VCO phase tap and counter starting time is implemented by allowing any of the output counters (`C[5..0]` or `m`) to use any of the eight phases of the VCO as the reference clock. This allows you to adjust the delay time with a fine resolution. The minimum delay time that you can insert using this method is defined by:

$$\Phi_{fine} = \frac{1}{8} T_{VCO} = \frac{1}{8 f_{VCO}} = \frac{N}{8 M f_{REF}}$$

where f_{REF} is input reference clock frequency.

For example, if f_{REF} is 100 MHz, *n* is 1, and *m* is 8, then f_{VCO} is 800 MHz and Φ_{fINE} equals 156.25 ps. This phase shift is defined by the PLL operating frequency, which is governed by the reference clock frequency and the counter settings.

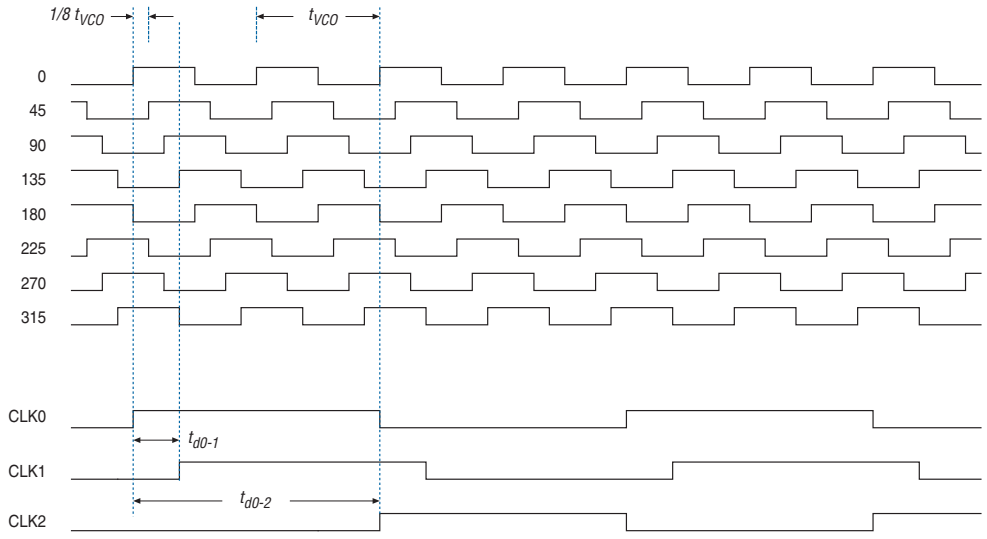
You can also delay the start of the counters for a predetermined number of counter clocks. You can express phase shift as:

$$\Phi_{coarse} = \frac{C - 1}{f_{Vco}} = \frac{(C - 1)N}{M f_{REF}}$$

where *C* is the count value set for the counter delay time, (this is the initial setting in the PLL usage section of the compilation report in the Quartus II software). If the initial value is 1, C – 1 = 0° phase shift.

Figure 1–14 shows an example of phase shift insertion using the fine resolution using VCO phase taps method. The eight phases from the VCO are shown and labeled for reference. For this example, `CLK0` is based off the 0phase from the VCO and has the *C* value for the counter set to one. The `CLK1` signal is divided by four, two VCO clocks for high time and two VCO clocks for low time. `CLK1` is based off the 135° phase tap from the VCO and also has the *C* value for the counter set to one. The `CLK1` signal is also divided by 4. In this case, the two clocks are offset by 3 Φ_{FINE}. `CLK2` is based off the `0phase` from the VCO but has the *C* value for the counter set to three. This creates a delay of 2 Φ_{COARSE}, (two complete VCO periods).

Figure 1–14. Delay Insertion Using VCO Phase Output and Counter Delay Time



You can use the coarse and fine phase shifts as described above to implement clock delays in Stratix II and Stratix II GX devices. The phase-shift parameters are set in the Quartus II software.

Programmable Duty Cycle

The programmable duty cycle allows enhanced and fast PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each enhanced and fast PLL post-scale counter `C[]`. The duty cycle setting is achieved by a low and high time count setting for the post-scale counters. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices. The post-scale counter value determines the precision of the duty cycle. The precision is defined by 50% divided by the post-scale counter value. The closest value to 100% is not achievable for a given counter value. For example, if the `C0` counter is ten, then steps of 5% are possible for duty cycle choices between 5 to 90%.

If the device uses external feedback, you must set the duty cycle for the counter driving the `fbin` pin to 50%. Combining the programmable duty cycle with programmable phase shift allows the generation of precise non-overlapping clocks.

Advanced Clear and Enable Control

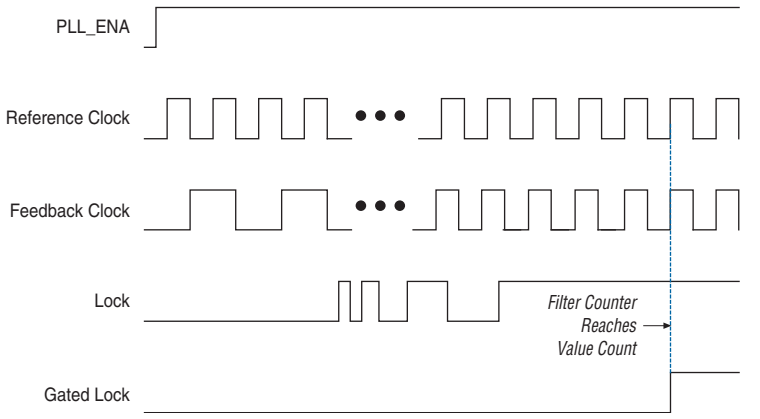
There are several control signals for clearing and enabling PLLs and their outputs. You can use these signals to control PLL resynchronization and gate PLL output clocks for low-power applications.

Enhanced Lock Detect Circuit

The lock output indicates that the PLL has locked onto the reference clock. Without any additional circuitry, the lock signal may toggle as the PLL begins tracking the reference clock. You may need to gate the lock signal for use as a system control. Either a gated lock signal or an ungated lock signal from the locked port can drive the logic array or an output pin. The Stratix II and Stratix II GX enhanced and fast PLLs include a programmable counter that holds the lock signal low for a user-selected number of input clock transitions. This allows the PLL to lock before enabling the lock signal. You can use the Quartus II software to set the 20-bit counter value.

Figure 1–15 shows the timing waveform for the lock and gated lock signals.

Figure 1–15. Timing Waveform for Lock and Gated Lock Signals



The device resets and enables both the counter and the PLL simultaneously when the `pllena` signal is asserted or the `areset` signal is de-asserted. Enhanced PLLs and fast PLLs support this feature. To ensure correct circuit operation, and to ensure that the output clocks have the correct phase relationship with respect to the input clock, Altera recommends that the input clock be running before the Stratix II device is finished configuring.

PLL_ENA

The PLL_ENA pin is a dedicated pin that enables or disables all PLLs on the Stratix II or Stratix II GX device. When the PLL_ENA pin is low, the clock output ports are driven low and all the PLLs go out of lock. When the PLL_ENA pin goes high again, the PLLs relock and resynchronize to the input clocks. You can choose which PLLs are controlled by the `pllena` signal by connecting the `pllena` input port of the `altpll` megafunction to the common PLL_ENA input pin.

Also, whenever the PLL loses lock for any reason (be it excessive `inclk` jitter, clock switchover, PLL reconfiguration, power supply noise, etc.), the PLL must be reset with the `areset` signal to guarantee correct phase relationship between the PLL output clocks. If the phase relationship between the input clock versus output clock, and between different output clocks from the PLL is not important in your design, the PLL need not be reset.

The level of the VCCSEL pin selects the PLL_ENA input buffer power. Therefore, if VCCSEL is high, the PLL_ENA pin's 1.8/1.5-V input buffer is powered by V_{CCIO} of the bank that PLL_ENA resides in. If VCCSEL is low (GND), the PLL_ENA pin's 3.3/2.5-V input buffer is powered by V_{CCPD}.

For more information about the VCCSEL pin, refer to the *Configuring Stratix II and Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* (or the *Stratix II Device Handbook)*.

pfdena

The pfdena signals control the phase frequency detector (PFD) output with a programmable gate. If you disable the PFD, the VCO operates at its last set value of control voltage and frequency with some long-term drift to a lower frequency. The system continues running when the PLL goes out of lock or the input clock is disabled. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. You can either use your own control signal or clkloss or gated locked status signals, to trigger pfdena.

areset

The areset signal is the reset or resynchronization input for each PLL. The device input pins or internal logic can drive these input signals. When driven high, the PLL counters reset, clearing the PLL output and placing the PLL out of lock. The VCO is set back to its nominal setting (~700 MHz). When driven low again, the PLL will resynchronize to its input as it relocks. If the target VCO frequency is below this nominal frequency, then the output frequency starts at a higher value than desired as the PLL locks.

The areset signal should be asserted every time the PLL loses lock to guarantee correct phase relationship between the PLL input clock and output clocks. Users should include the areset signal in designs if any of the following conditions are true:

- PLL reconfiguration or clock switchover enabled in the design.
- Phase relationships between the PLL input clock and output clocks need to be maintained after a loss of lock condition.
- If the input clock to the PLL is not toggling or is unstable upon power up, assert the areset signal after the input clock is toggling, making sure to stay within the input jitter specification.

Altera recommends that you use the areset and locked signals in your designs to control and observe the status of your PLL.

clkena

If the system cannot tolerate the higher output frequencies when using pfdena higher value, the clkena signals can disable the output clocks until the PLL locks. The clkena signals control the regional, global, and external clock outputs. The clkena signals are registered on the falling edge of the counter output clock to enable or disable the clock without glitches. See Figure 1–56 in the "Clock Control Block" section on page 1–86 of this document for more information about the clkena signals.

Advanced Features

Stratix II and Stratix II GX PLLs offer a variety of advanced features, such as counter cascading, clock switchover, PLL reconfiguration, reconfigurable bandwidth, and spread-spectrum clocking. Table 1–14 shows which advanced features are available in which type of Stratix II or Stratix II GX PLL.

Table 1–14. Stratix II and Stratix II GX PLL Advanced Features

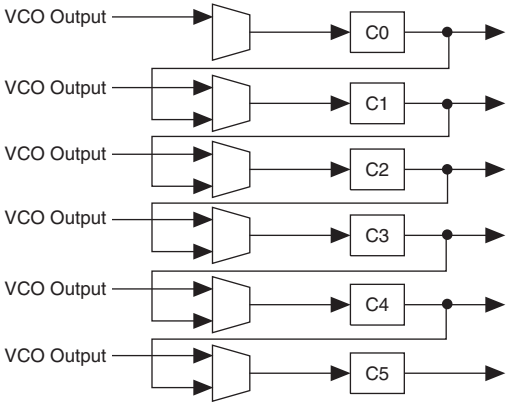
Advanced Feature	Availability	
	Enhanced PLLs	Fast PLLs *(1)*
Counter cascading	✓	
Clock switchover	✓	✓
PLL reconfiguration	✓	✓
Reconfigurable bandwidth	✓	✓
Spread-spectrum clocking	✓	

Note to Table 1–14:
(1) Stratix II and Stratix II GX fast PLLs only support manual clock switchover, not automatic clock switchover.

Counter Cascading

The Stratix II and Stratix II GX enhanced PLL supports counter cascading to create post-scale counters larger than 512. This is implemented by feeding the output of one counter into the input of the next counter in a cascade chain, as shown in Figure 1–16.

Figure 1–16. Counter Cascading



When cascading counters to implement a larger division of the high-frequency VCO clock, the cascaded counters behave as one counter with the product of the individual counter settings. For example, if C0 = 4 and C1 = 2, then the cascaded value is C0 × C1 = 8.

The Stratix II and Stratix II GX fast PLLs does not support counter cascading.

Counter cascading is set in the configuration file, meaning they can not be cascaded using PLL reconfiguration.

Clock Switchover

The clock switchover feature allows the PLL to switch between two reference input clocks. Use this feature for clock redundancy or for a dual clock domain application such as in a system that turns on the redundant clock if the primary clock stops running. The design can perform clock switchover automatically, when the clock is no longer toggling, or based on a user control signal, `clkswitch`.

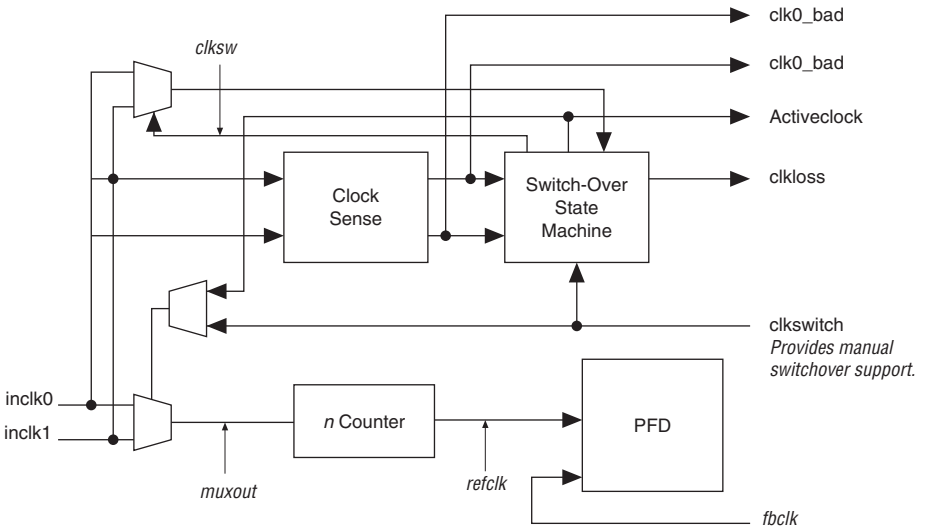
Enhanced PLLs support both automatic and manual switchover, while fast PLLs only support manual switchover.

Automatic Clock Switchover

Stratix II and Stratix II GX device PLLs support a fully configurable clock switchover capability. Figure 1–17 shows the block diagram of the switch-over circuit built into the enhanced PLL. When the primary clock signal is not present, the clock sense block automatically switches from

the primary to the secondary clock for PLL reference. The design sends out the clk0_bad, clk1_bad, and the clk_loss signals from the PLL to implement a custom switchover circuit.

Figure 1–17. Automatic Clock Switchover Circuit Block Diagram



There are two possible ways to use the clock switchover feature.

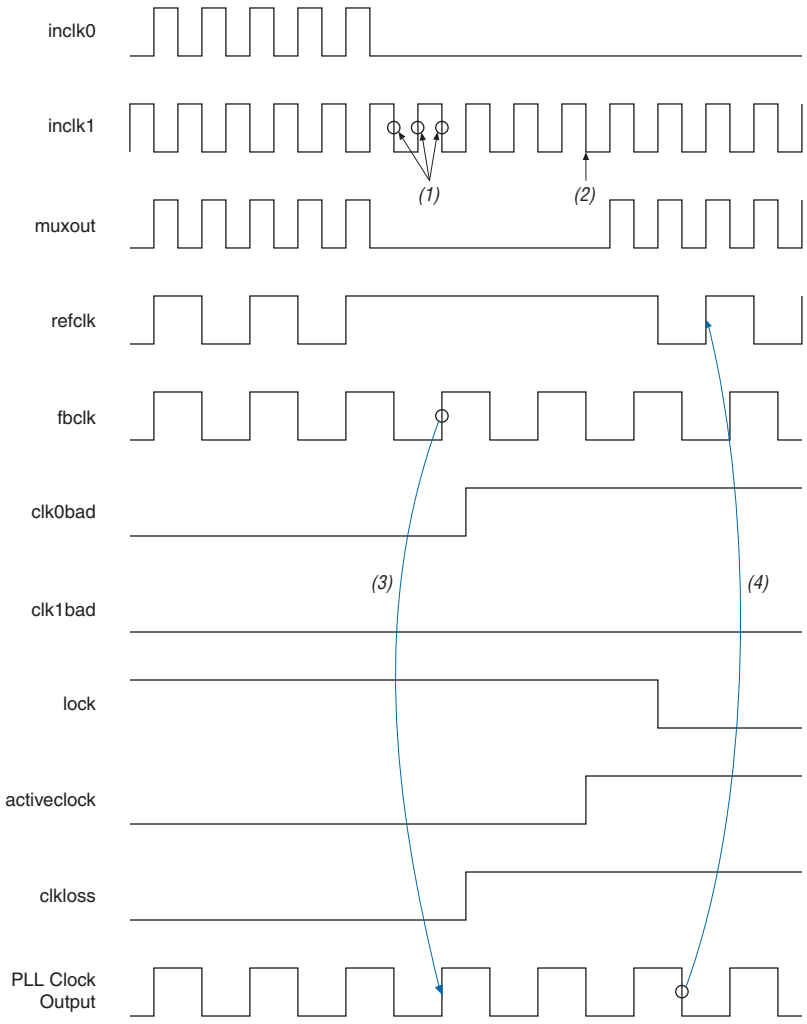
- Use the switchover circuitry for switching from a primary to secondary input of the same frequency. For example, in applications that require a redundant clock with the same frequency as the primary clock, the switchover state machine generates a signal that controls the multiplexer select input shown on the bottom of Figure 1–17. In this case, the secondary clock becomes the reference clock for the PLL. This automatic switchover feature only works for switching from the primary to secondary clock.

- Use the CLKSWITCH input for user- or system-controlled switch conditions. This is possible for same-frequency switchover or to switch between inputs of different frequencies. For example, if inclk0 is 66 MHz and inclk1 is 100 MHz, you must control the switchover because the automatic clock-sense circuitry cannot monitor primary and secondary clock frequencies with a frequency difference of more than 20%. This feature is useful when clock sources can originate from multiple cards on the backplane, requiring a system-controlled switchover between frequencies of operation. You should choose the secondary clock frequency so the

VCO operates within the recommended range of 500 to 1,000 MHz. You should also set the *m* and *n* counters accordingly to keep the VCO operating frequency in the recommended range.

Figure 1–18 shows an example waveform of the switchover feature when using the automatic `clkloss` detection. Here, the `inclk0` signal gets stuck low. After the `inclk0` signal is stuck at low for approximately two clock cycles, the clock sense circuitry drives the `clk0_bad` signal high. Also, because the reference clock signal is not toggling, the `clk_loss` signal goes low, indicating a switch condition. Then, the switchover state machine controls the multiplexer through the `clksw` signal to switch to the secondary clock.

Figure 1–18. Automatic Switchover Upon Clock Loss Detection

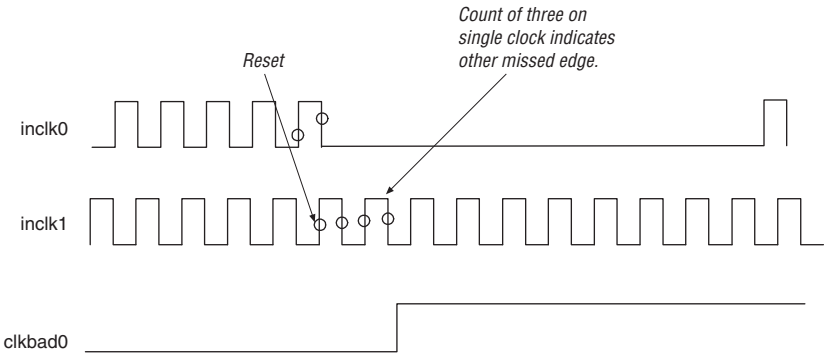


Notes to Figure 1–18:

(1) The number of clock edges before allowing switchover is determined by the counter setting.
(2) Switchover is enabled on the falling edge of INCLK1.
(3) The rising edge of FBCLK causes the VCO frequency to decrease.
(4) The rising edge of REFCLK starts the PLL lock process again, and the VCO frequency increases.

The switch-over state machine has two counters that count the edges of the primary and the secondary clocks; counter0 counts the number of inclk0 edges and counter1 counts the number of inclk1 edges. The counters get reset to zero when the count values reach 1, 1; 1, 2; 2, 1; or 2, 2 for inclock0 and inclock1, respectively. For example, if counter0 counts two edges, its count is set to two and if counter1 counts two edges before the counter0 sees another edge, they are both reset to 0. If for some reason one of the counters counts to three, it means the other clock missed an edge. The clkbad0 or clkbad1 signal goes high, and the switchover circuitry signals a switch condition. See Figure 1–19.

Figure 1–19. Clock-Edge Detection for Switchover



Manual Override

When using automatic switchover, you can switch input clocks by using the manual override feature with the clkswitch input.

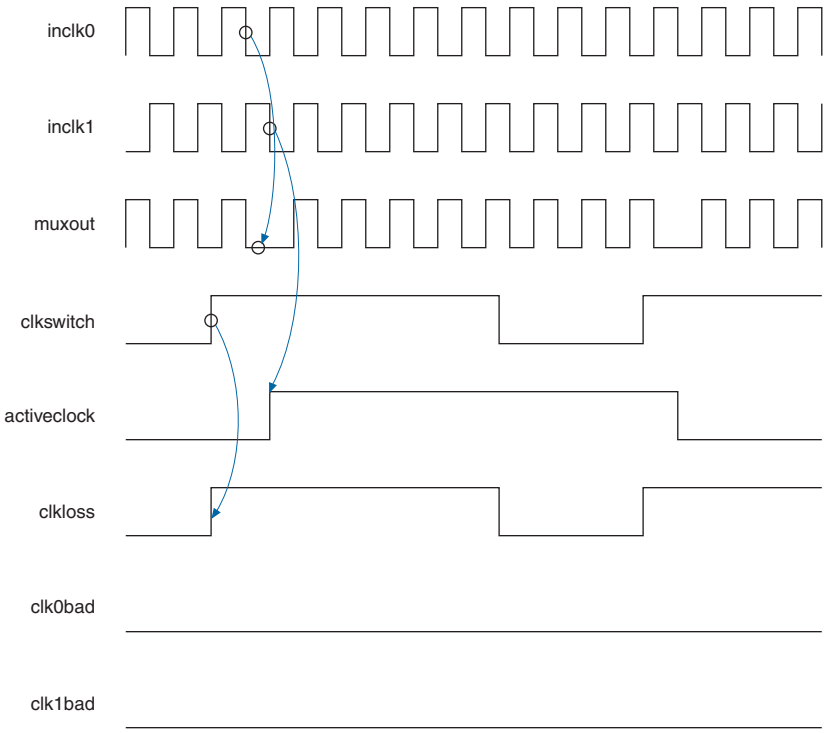
The manual override feature available in automatic clock switchover is different from manual clock switchover.

Figure 1–20 shows an example of a waveform illustrating the switchover feature when controlled by clkswitch. In this case, both clock sources are functional and inclk0 is selected as the primary clock. clkswitch goes high, which starts the switchover sequence. On the falling edge of inclk0, the counter's reference clock, muxout, is gated off to prevent any clock glitching. On the falling edge of inclk1, the reference clock multiplexer switches from inclk0 to inclk1 as the PLL reference and the activeclock signal changes to indicate which clock is selected as primary and which is secondary.

The clkloss signal mirrors the clkswitch signal and activeclock mirrors clksw in this mode. Since both clocks are still functional during the manual switch, neither clk_bad signal goes high. Since the

switchover circuit is edge-sensitive, the falling edge of the clkswitch signal does not cause the circuit to switch back from inclk1 to inclk0. When the clkswitch signal goes high again, the process repeats. clkswitch and automatic switch only work if the clock being switched to is available. If the clock is not available, the state machine waits until the clock is available.

Figure 1–20. Clock Switchover Using the CLKSWITCH Control *Note (1)*

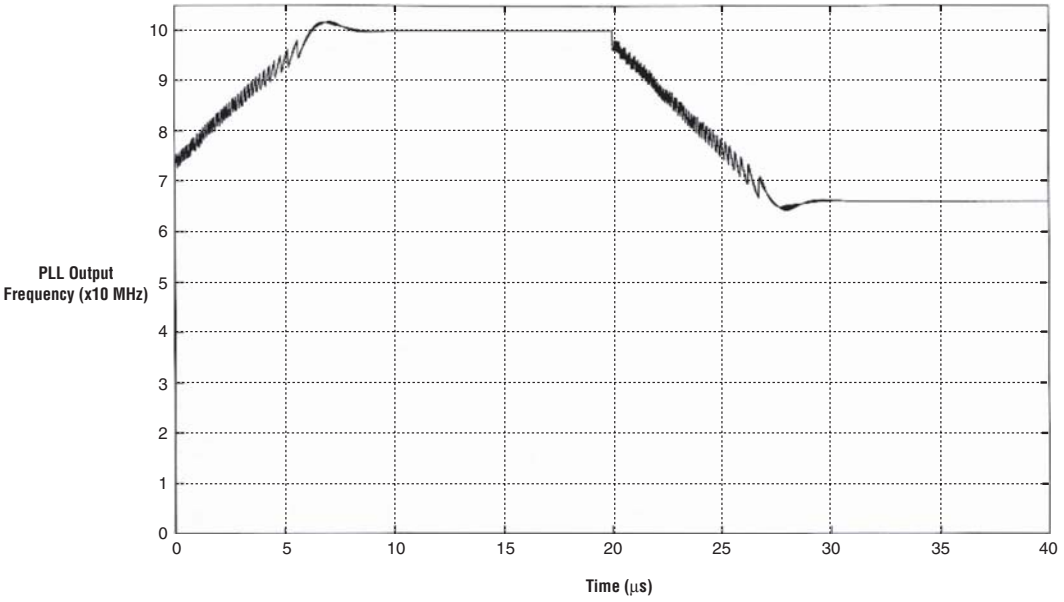


Note to Figure 1–20:

(1) Both inclk0 and inclk1 must be running when the clkswitch signal goes high to initiate a manual clock switchover event. Failing to meet this requirement causes the clock switchover to not function properly.

Figure 1–21 shows a simulation of using switchover for two different reference frequencies. In this example simulation, the reference clock is either 100 or 66 MHz. The PLL begins with f_{IN} = 100 MHz and is allowed to lock. At 20 µs, the clock is switched to the secondary clock, which is at 66 MHz.

Figure 1–21. Switchover Simulation *Note (1)*



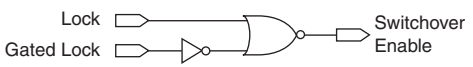
Note to Figure 1–21:

(1) This simulation was performed under the following conditions: the *n* counter is set to 2, the *m* counter is set to 16, and the output counter is set to 8. Therefore, the VCO operates at 800 MHz for the 100-MHz input references and at 528 MHz for the 66-MHz reference input.

Lock Signal-Based Switchover

The lock circuitry can initiate the automatic switchover. This is useful for cases where the input clock is still clocking, but its characteristics have changed so that the PLL is not locked to it. The switchover enable is based on both the gated and ungated lock signals. If the ungated lock is low, the switchover is not enabled until the gated lock has reached its terminal count. You must activate the switchover enable if the gated lock is high, but the ungated lock goes low. The switchover timing for this mode is similar to the waveform shown in Figure 1–20 for `clkswitch` control, except the switchover enable replaces `clkswitch`. Figure 1–17 shows the switchover enable circuit when controlled by lock and gated lock.

Figure 1–22. Switchover Enable Circuit



Manual Clock Switchover

Stratix II and Stratix II GX enhanced and fast PLLs support manual switchover, where the `clkswitch` signal controls whether `inclk0` or `inclk1` is the input clock to the PLL. If `clkswitch` is low, then `inclk0` is selected; if `clkswitch` is high, then `inclk1` is selected. Figure 1–23 shows the block diagram of the manual switchover circuit in fast PLLs. The block diagram of the manual switchover circuit in enhanced PLLs is shown in Figure 1–23.

Figure 1–23. Manual Clock Switchover Circuitry in Fast PLLs

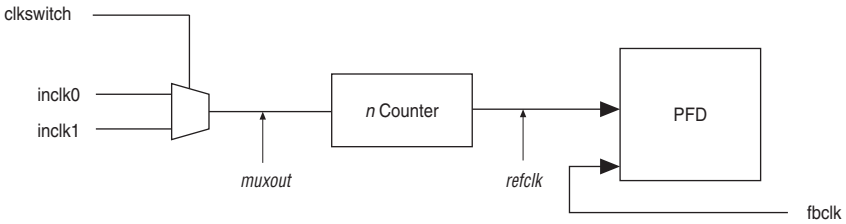
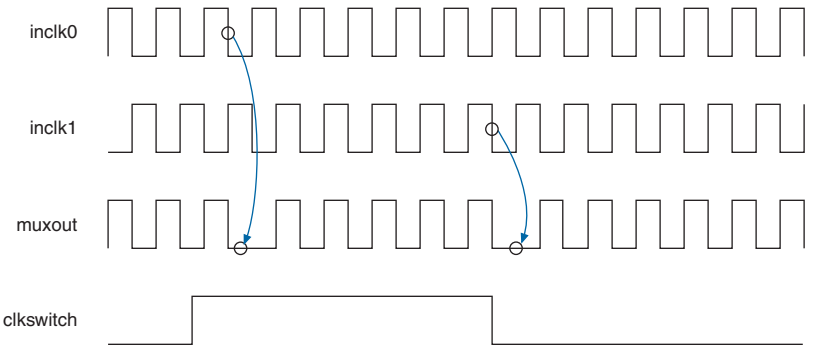


Figure 1–24 shows an example of a waveform illustrating the switchover feature when controlled by `clkswitch`. In this case, both clock sources are functional and `inclk0` is selected as the primary clock. `clkswitch` goes high, which starts the switch-over sequence. On the falling edge of `inclk0`, the counter's reference clock, `muxout`, is gated off to prevent any clock glitching. On the rising edge of `inclk1`, the reference clock multiplex switches from `inclk0` to `inclk1` as the PLL reference. When the `clkswitch` signal goes low, the process repeats, causing the circuit to switch back from `inclk1` to `inclk0`.

Figure 1–24. Manual Switchover *Note (1)*



Note to Figure 1–24:

(1) Both `inclk0` and `inclk1` must be running when the `clkswitch` signal goes high to initiate a manual clock switchover event. Failing to meet this requirement causes the clock switchover to not function properly.

Software Support

Table 1–15 summarizes the signals used for clock switchover.

Table 1–15. altpll Megafunction Clock Switchover Signals (Part 1 of 2)

Port	Description	Source	Destination
inclk0	Reference `clk0` to the PLL.	I/O pin	Clock switchover circuit
inclk1	Reference `clk1` to the PLL.	I/O pin	Clock switchover circuit
clkbad0 *(1)*	Signal indicating that `inclk0` is no longer toggling.	Clock switchover circuit	Logic array
clkbad1 *(1)*	Signal indicating that `inclk1` is no longer toggling.	Clock switchover circuit	Logic array
clkswitch	Switchover signal used to initiate clock switchover asynchronously. When used in manual switchover, clkswitch is used as a select signal between inclk0 and inclk1 `clswitch = 0 inclk0` is selected and vice versa.	Logic array or I/O pin	Clock switchover circuit
clkloss *(1)*	Signal indicating that the switchover circuit detected a switch condition.	Clock switchover circuit	Logic array
locked	Signal indicating that the PLL has lost lock.	PLL	Clock switchover circuit

Table 1–15. altpll Megafunction Clock Switchover Signals (Part 2 of 2)

Port	Description	Source	Destination
activeclock *(1)*	Signal to indicate which clock (0 = `inclk0`, 1= `inclk1`) is driving the PLL.	PLL	Logic array

Note for Table 1–15:
(1) These ports are only available for enhanced PLLs and in auto mode and when using automatic switchover.

All the switchover ports shown in Table 1–15 are supported in the `altpll` megafunction in the Quartus II software. The `altpll` megafunction supports two methods for clock switchover:

- When selecting an enhanced PLL, you can enable both the automatic and the manual switchover, making all the clock switchover ports available.
- When selecting a fast PLL, you can use only enable the manual clock switchover option to select between `inclk0` or `inclk1`. The `clkloss`, `activeclock` and the `clkbad0`, and `clkbad1` signals are not available when manual switchover is selected.

If the primary and secondary clock frequencies are different, the Quartus II software selects the proper parameters to keep the VCO within the recommended frequency range.

For more information about PLL software support in the Quartus II software, see the *altpll Megafunction User Guide*.

Guidelines

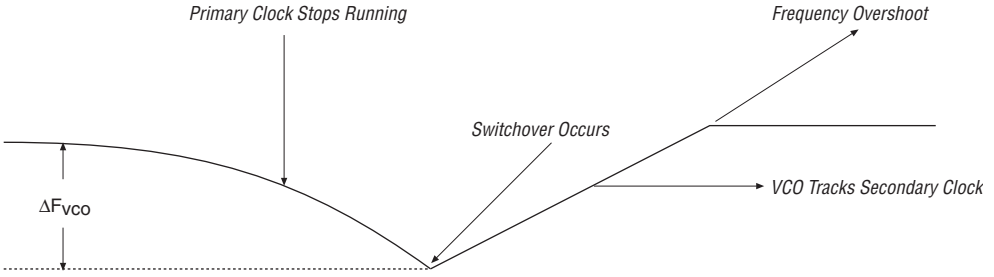
Use the following guidelines to design with clock switchover in PLLs.

- When using automatic switchover, the `clkswitch` signal has a minimum pulse width based on the two reference clock periods. The `CLKSWITCH` pulse width must be greater than or equal to the period of the current reference clock (t_{from_clk}) multiplied by two plus the rounded-up version of the ratio of the two reference clock periods. For example, if t_{to_clk} is equal to t_{from_clk}, then the `CLKSWITCH` pulse width should be at least three times the period of the clock pulse.

$$t_{CLKSWITCHCHmin} \geq t_{from\_clk} \times [2 + int_{round\_up} (t_{to\_clk} \div t_{from\_clk})]$$

- Applications that require a clock switchover feature and a small frequency drift should use a low-bandwidth PLL. The low-bandwidth PLL reacts slower than a high-bandwidth PLL to reference input clock changes. When the switchover happens, a low-bandwidth PLL propagates the stopping of the clock to the output slower than a high-bandwidth PLL. A low-bandwidth PLL filters out jitter on the reference clock. However, be aware that the low-bandwidth PLL also increases lock time.
- Stratix II and Stratix II GX device PLLs can use both the automatic clock switchover and the `clkswitch` input simultaneously. Therefore, the switchover circuitry can automatically switch from the primary to the secondary clock. Once the primary clock stabilizes again, the `clkswitch` signal can switch back to the primary clock. During switchover, the `PLL_VCO` continues to run and slows down, generating frequency drift on the PLL outputs. The `clkswitch` signal controls switchover with its rising edge only.
- If the clock switchover event is glitch-free, after the switch occurs, there is still a finite resynchronization period to lock onto a new clock as the VCO ramps up. The exact amount of time it takes for the PLL to relock is dependent on the PLL configuration. Use the PLL programmable bandwidth feature to adjust the relock time.
- If the phase relationship between the input clock to the PLL and output clock from the PLL is important in your design, assert `areset` for 10ns after performing a clock switchover. Wait for the locked signal (or gated lock) to go high before re-enabling the output clocks from the PLL.
- Figure 1–25 shows how the VCO frequency gradually decreases when the primary clock is lost and then increases as the VCO locks on to the secondary clock. After the VCO locks on to the secondary clock, some overshoot can occur (an over-frequency condition) in the VCO frequency.

Figure 1–25. VCO Switchover Operating Frequency



- Disable the system during switchover if it is not tolerant to frequency variations during the PLL resynchronization period. There are two ways to disable the system. First, the system may require some time to stop before switchover occurs. The switchover circuitry includes an optional five-bit counter to delay when the reference clock is switched. You have the option to control the time-out setting on this counter (up to 32 cycles of latency) before the clock source switches. You can use these cycles for disaster recovery. The clock output frequency varies slightly during those 32 cycles since the VCO can still drift without an input clock. Programmable bandwidth can control the PLL response to limit drift during this 32 cycle period.
- A second option available is the ability to use the PFD enable signal (`pfdena`) along with user-defined control logic. In this case you can use `clk0_bad` and `clk1_bad` status signals to turn off the PFD so the VCO maintains its last frequency. You can also use the state machine to switch over to the secondary clock. Upon re-enabling the PFD, output clock enable signals (`clkena`) can disable clock outputs during the switchover and resynchronization period. Once the lock indication is stable, the system can re-enable the output clock(s).

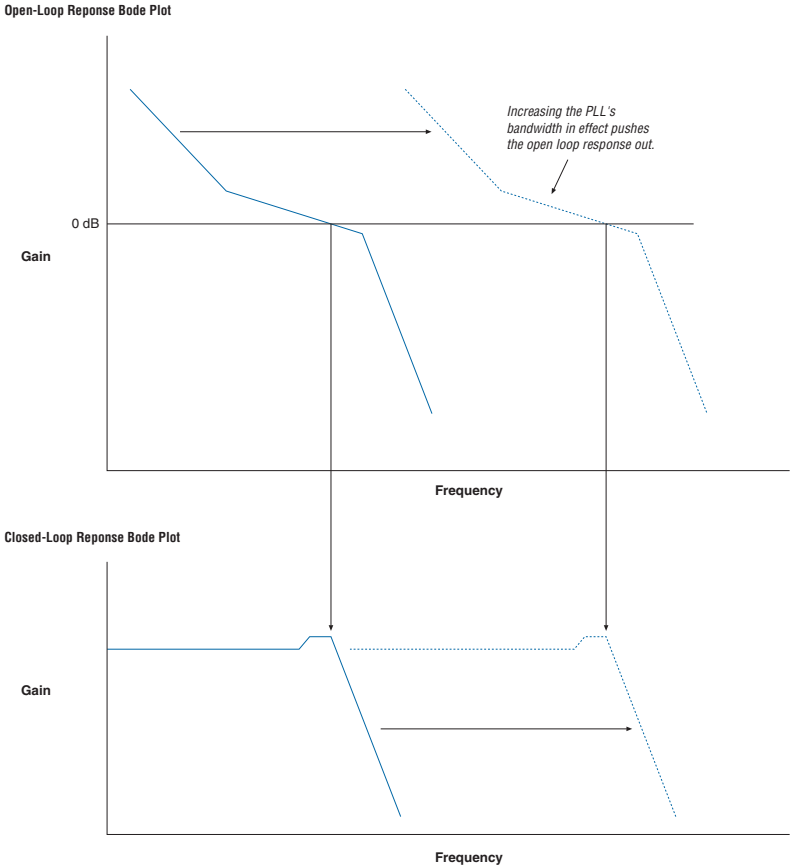
Reconfigurable Bandwidth

Stratix II and Stratix II GX enhanced and fast PLLs provide advanced control of the PLL bandwidth using the PLL loop's programmable characteristics, including loop filter and charge pump.

Background

PLL bandwidth is the measure of the PLL's ability to track the input clock and jitter. The closed-loop gain 3-dB frequency in the PLL determines the PLL bandwidth. The bandwidth is approximately the unity gain point for open loop PLL response. As Figure 1–26 shows, these points correspond to approximately the same frequency.

Figure 1–26. Open- and Closed-Loop Response Bode Plots



A high-bandwidth PLL provides a fast lock time and tracks jitter on the reference clock source, passing it through to the PLL output. A low-bandwidth PLL filters out reference clock, but increases lock time. Stratix II and Stratix II GX enhanced and fast PLLs allow you to control the bandwidth over a finite range to customize the PLL characteristics for a particular application. The programmable bandwidth feature in Stratix II and Stratix II GX PLLs benefits applications requiring clock switchover (e.g., TDMA frequency hopping wireless, and redundant clocking).

The bandwidth and stability of such a system is determined by the charge pump current, the loop filter resistor value, the high-frequency capacitor value (in the loop filter), and the *m*-counter value. You can use the Quartus II software to control these factors and to set the bandwidth to the desired value within a given range.

You can set the bandwidth to the appropriate value to balance the need for jitter filtering and lock time. Figures 1–27 and 1–28 show the output of a low- and high-bandwidth PLL, respectively, as it locks onto the input clock.

Figure 1–27. Low-Bandwidth PLL Lock Time

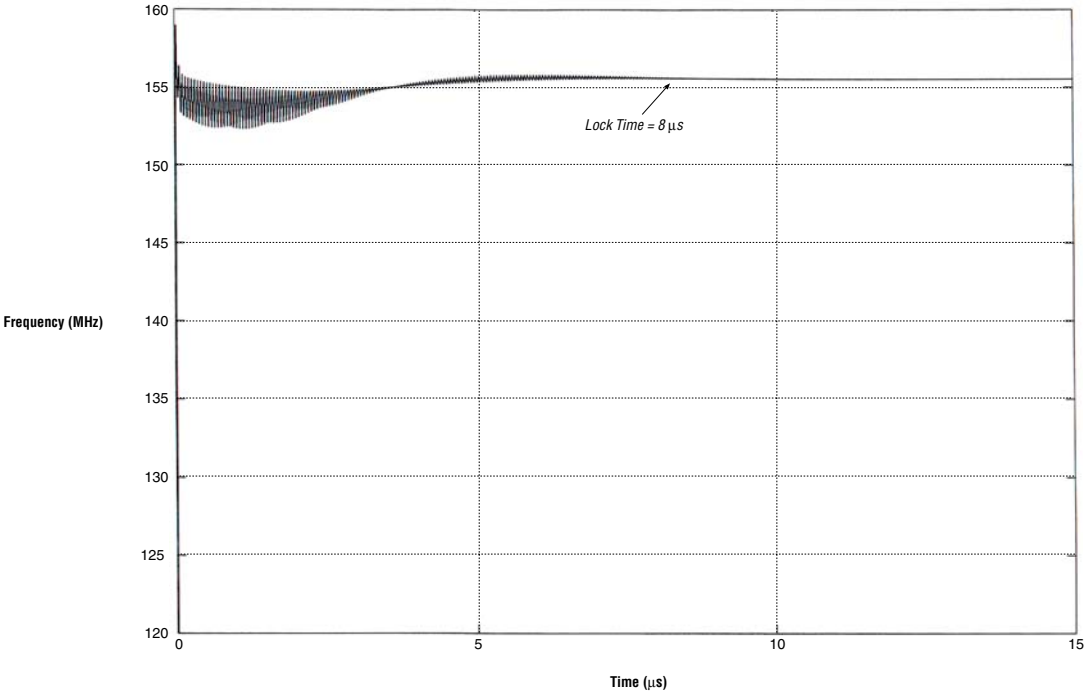
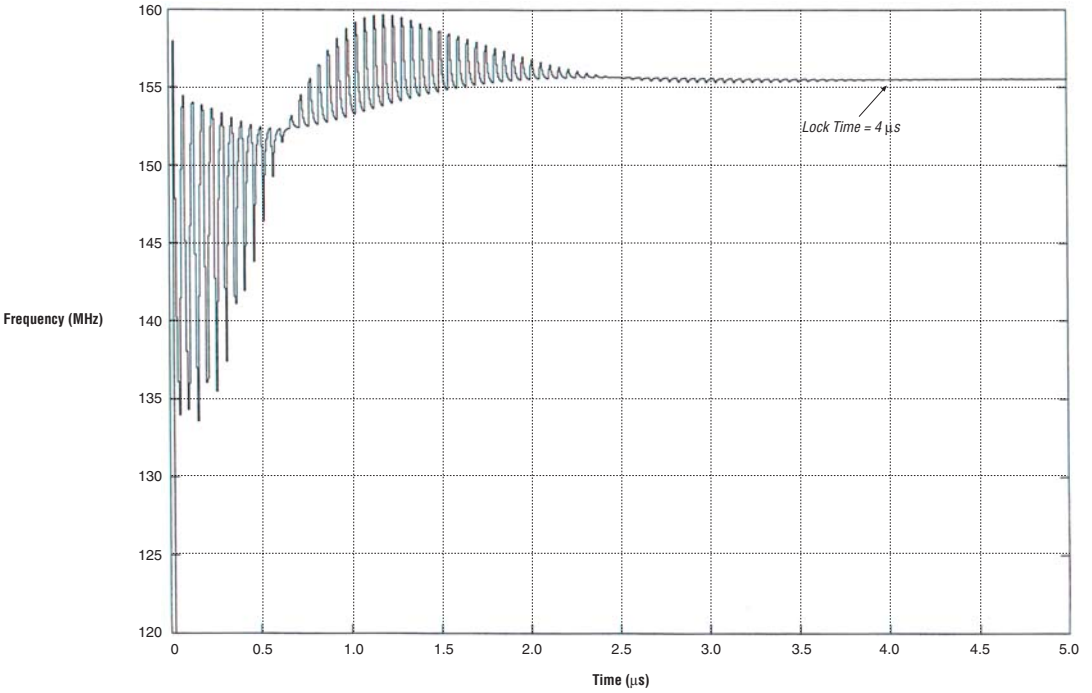


Figure 1–28. High-Bandwidth PLL Lock Time



A high-bandwidth PLL can benefit a system that has two cascaded PLLs. If the first PLL uses spread spectrum (as user-induced jitter), the second PLL can track the jitter that is feeding it by using a high-bandwidth setting. A low-bandwidth PLL can, in this case, lose lock due to the spread-spectrum-induced jitter on the input clock.

A low-bandwidth PLL benefits a system using clock switchover. When the clock switchover happens, the PLL input temporarily stops. A low-bandwidth PLL would react more slowly to changes to its input clock and take longer to drift to a lower frequency (caused by the input stopping) than a high-bandwidth PLL. Figures 1–29 and 1–30 demonstrate this property. The two plots show the effects of clock switchover with a low- or high-bandwidth PLL. When the clock switchover happens, the output of the low-bandwidth PLL (see Figure 1–29) drifts to a lower frequency more slowly than the high-bandwidth PLL output (see Figure 1–30).

Figure 1–29. Effect of Low Bandwidth on Clock Switchover

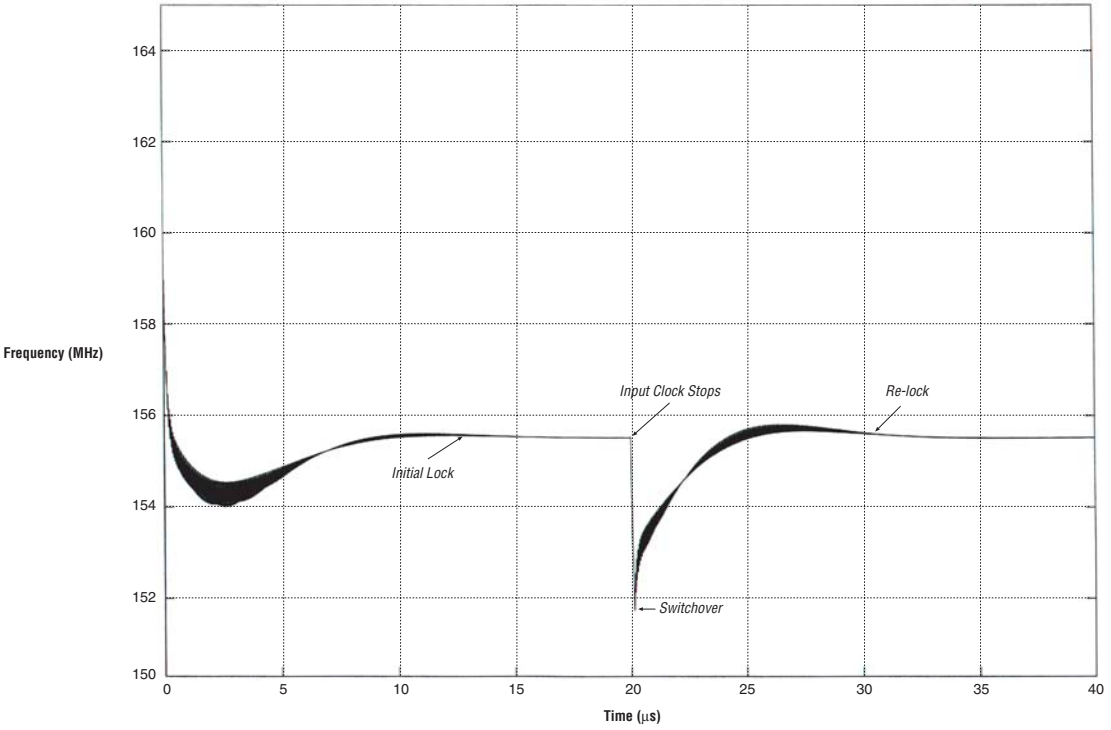
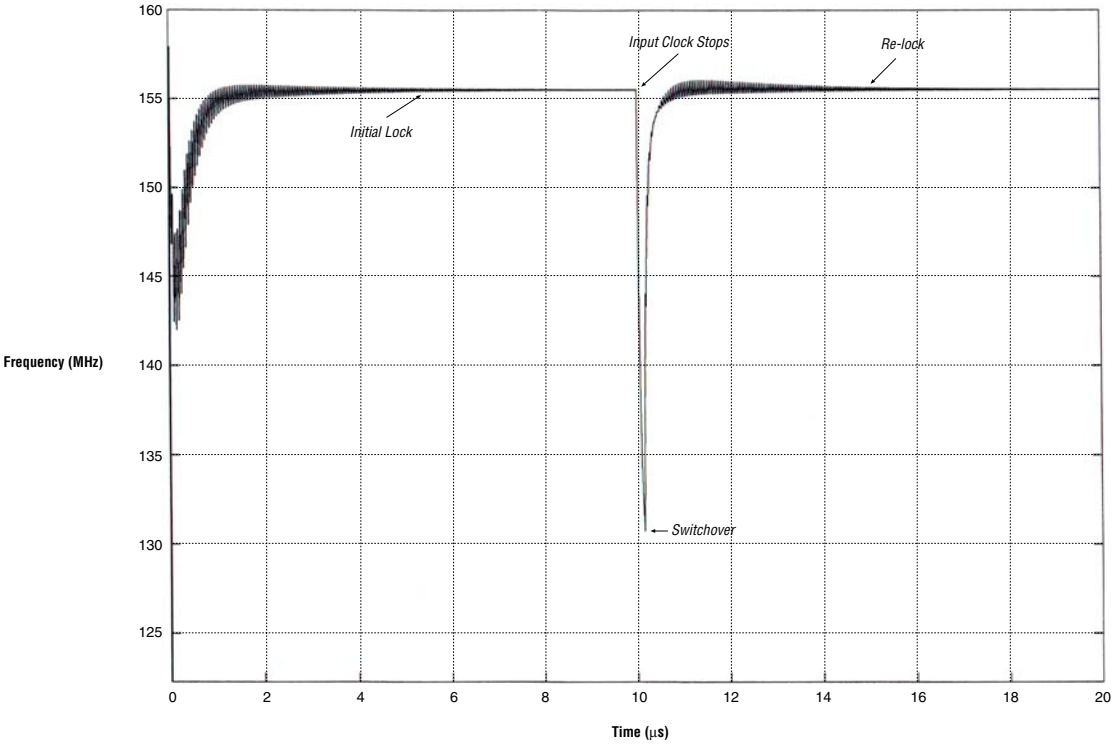


Figure 1–30. Effect of High Bandwidth on Clock Switchover



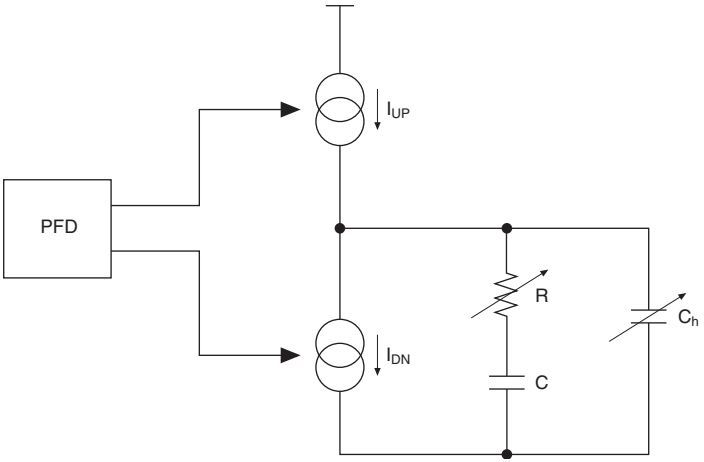
Implementation

Traditionally, external components such as the VCO or loop filter control a PLL's bandwidth. Most loop filters are made up of passive components such as resistors and capacitors that take up unnecessary board space and increase cost. With Stratix II and Stratix II GX PLLs, all the components are contained within the device to increase performance and decrease cost.

Stratix II and Stratix II GX device PLLs implement reconfigurable bandwidth by giving you control of the charge pump current and loop filter resistor (R) and high-frequency capacitor C_H values (see Table 1–16). The Stratix II and Stratix II GX device enhanced PLL bandwidth ranges from 130 kHz to 16.9 MHz. The Stratix II and Stratix II GX device fast PLL bandwidth ranges from 1.16 to 28 MHz.

The charge pump current directly affects the PLL bandwidth. The higher the charge pump current, the higher the PLL bandwidth. You can choose from a fixed set of values for the charge pump current. Figure 1–31 shows the loop filter and the components that can be set through the Quartus II software. The components are the loop filter resistor, R, and the high frequency capacitor, C_H, and the charge pump current, I_{UP} or I_{DN}.

Figure 1–31. Loop Filter Programmable Components



Software Support

The Quartus II software provides two levels of bandwidth control.

Megafunction-Based Bandwidth Setting

The first level of programmable bandwidth allows you to enter a value for the desired bandwidth directly into the Quartus II software using the `altpll` megafunction. You can also set the bandwidth parameter in the `altpll` megafunction to the desired bandwidth. The Quartus II software selects the best bandwidth parameters available to match your bandwidth request. If the individual bandwidth setting request is not available, the Quartus II software selects the closest achievable value.

Advanced Bandwidth Setting

An advanced level of control is also possible using advanced loop filter parameters. You can dynamically change the charge pump current, loop filter resistor value, and the loop filter (high frequency) capacitor value.

The parameters for these changes are: `charge_pump_current`, `loop_filter_r`, and `loop_filter_c`. Each parameter supports the specific range of values listed in Table 1–16.

Table 1–16. Advanced Loop Filter Parameters

Parameter	Values
Resistor values (kΩ)	*(1)*
High-frequency capacitance values (pF)	*(1)*
Charge pump current settings (µA)	*(1)*

Note to Table 1–16:
(1) For more information, see *AN 367: Implementing PLL Reconfiguration in Stratix II Devices*.

For more information about Quartus II software support of reconfigurable bandwidth, see the *Design Example: Dynamic PLL Reconfiguration* section in volume 3, Verification, of the *Quartus II Development Software Handbook*.

PLL Reconfiguration

PLLs use several divide counters and different VCO phase taps to perform frequency synthesis and phase shifts. In Stratix II and Stratix II GX enhanced and fast PLLs, the counter value and phase are configurable in real time. In addition, you can change the loop filter and charge pump components, which affect the PLL bandwidth, on the fly. You can control these PLL components to update the output clock frequency, PLL bandwidth, and phase-shift variation in real time, without the need to reconfigure the entire FPGA.

For more information about PLL reconfiguration, see *AN 367: Implementing PLL Reconfiguration in Stratix II Devices*.

Spread-Spectrum Clocking

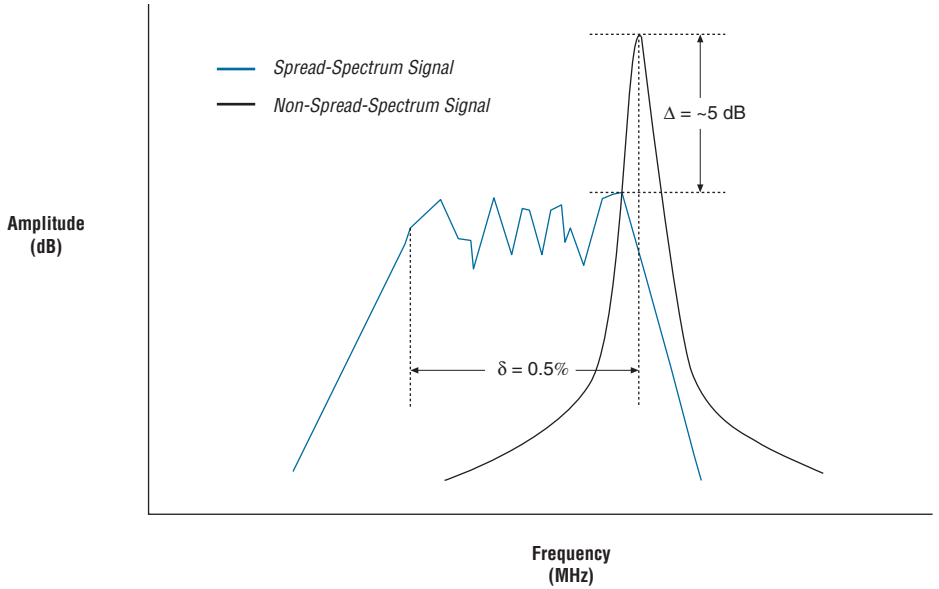
Digital clocks are square waves with short rise times and a 50% duty cycle. These high-speed clocks concentrate a significant amount of energy in a narrow bandwidth at the target frequency and at the higher frequency harmonics. This results in high energy peaks and increased electromagnetic interference (EMI). The radiated noise from the energy peaks travels in free air and, if not minimized, can lead to corrupted data and intermittent system errors, which can jeopardize system reliability.

Traditional methods for limiting EMI include shielding, filtering, and multi-layer printed circuit boards (PCBs). However, these methods significantly increase the overall system cost and sometimes are not

enough to meet EMI compliance. Spread-spectrum technology provides you with a simple and effective technique for reducing EMI without additional cost and the trouble of re-designing a board.

Spread-spectrum technology modulates the target frequency over a small range. For example, if a 100-MHz signal has a 0.5% down-spread modulation, then the frequency is swept from 99.5 to 100 MHz. Figure 1–32 gives a graphical representation of the energy present in a spread-spectrum signal vs. a non-spread spectrum-signal. It is apparent that instead of concentrating the energy at the target frequency, the energy is re-distributed across a wider band of frequencies, which reduces peak energy. Not only is there a reduction in the fundamental peak EMI components, but there is also a reduction in EMI of the higher order harmonics. Since some regulations focus on peak EMI emissions, rather than average EMI emissions, spread-spectrum technology is a valuable method of EMI reduction.

Figure 1–32. Spread-Spectrum Signal Energy Versus Non-Spread-Spectrum Signal Energy



Spread-spectrum technology would benefit a design with high EMI emissions and/or strict EMI requirements. Device-generated EMI is dependent on frequency and output voltage swing amplitude and edge rate. For example, a design using LVDS already has low EMI emissions

because of the low-voltage swing. The differential LVDS signal also allows for EMI rejection within the signal. Therefore, this situation may not require spread-spectrum technology.

Spread-spectrum clocking is only supported in Stratix II enhanced PLLs, not fast PLLs.

Implementation

Stratix II and Stratix II GX device enhanced PLLs feature spread-spectrum technology to reduce the EMIs emitted from the device. The enhanced PLL provides approximately 0.5% down spread using a triangular, also known as linear, modulation profile. The modulation frequency is programmable and ranges from approximately 30 kHz to 150 kHz. The spread percentage is based on the clock input to the PLL and the *m* and *n* settings. Spread-spectrum technology reduces the peak energy by four to six dB at the target frequency. However, this number is dependent on bandwidth and the *m* and *n* counter values and can vary from design to design.

Spread percentage, also known as modulation width, is defined as the percentage that the design modulates the target frequency. A negative (–) percentage indicates a down spread, a positive (+) percentage indicates an up spread, and a (±) indicates a center spread. Modulation frequency is the frequency of the spreading signal, or how fast the signal sweeps from the minimum to the maximum frequency. Down-spread modulation shifts the target frequency down by half the spread percentage, centering the modulated waveforms on a new target frequency.

The *m* and *n* counter values are toggled at the same time between two fixed values. The loop filter then slowly changes the VCO frequency to provide the spreading effect, which results in a triangular modulation. An additional spread-spectrum counter (shown in Figure 1–33) sets the modulation frequency. Figure 1–33 shows how spread-spectrum technology is implemented in the Stratix II and Stratix II GX device enhanced PLL.

Figure 1–33. Stratix II and Stratix II GX Spread-Spectrum Circuit Block Diagram

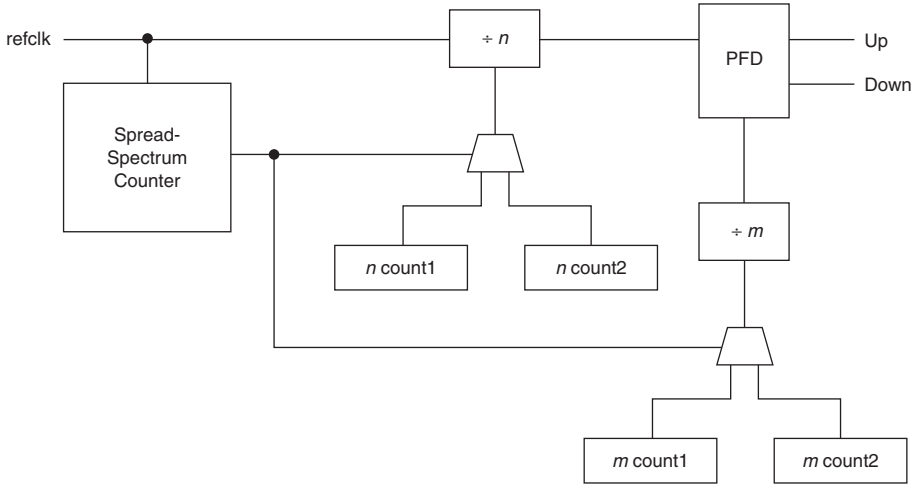


Figure 1–34 shows a VCO frequency waveform when toggling between different counter values. Since the enhanced PLL switches between two different m and n values, the result is a straight line between two frequencies, which gives a linear modulation. The magnitude of modulation is determined by the ratio of two m/n sets. The percent spread is determined by:

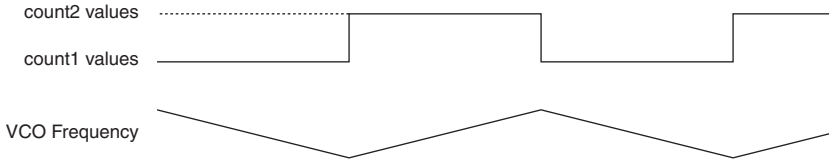
$$\text{percent spread} = (f_{VCOmax} - f_{VCOmin})/f_{VCOmax} = 1\ [(m_2 \times n_1)/(m_1 \times n_2)].$$

The maximum and minimum VCO frequency is defined as:

$$f_{VCOmax} = (m_1/n_1) \times f_{REF}$$

$$f_{VCOmin} = (m_2/n_2) \times f_{REF}$$

Figure 1–34. VCO Frequency Modulation Waveform



Software Support

You can enter the desired down-spread percentage and modulation frequency in the `altpll` megafunction through the Quartus II software. Alternatively, the `downspread` parameter in the `altpll` megafunction can be set to the desired down-spread percentage. Timing analysis ensures the design operates at the maximum spread frequency and meets all timing requirements.

For more information about PLL software support in the Quartus II software, see the *altpll Megafunction User Guide*.

Guidelines

If the design cascades PLLs, the source (upstream) PLL should have a low-bandwidth setting, while the destination (downstream) PLL should have a high-bandwidth setting. The upstream PLL must have a low-bandwidth setting because a PLL does not generate jitter higher than its bandwidth. The downstream PLL must have a high bandwidth setting to track the jitter. The design must use the spread-spectrum feature in a low-bandwidth PLL, and, therefore, the Quartus II software automatically sets the spread-spectrum PLL bandwidth to low.

If the programmable or reconfigurable bandwidth features are used, then you cannot use spread spectrum.

Stratix II and Stratix II GX devices can accept a spread-spectrum input with typical modulation frequencies. However, the device cannot automatically detect that the input is a spread-spectrum signal. Instead, the input signal looks like deterministic jitter at the input of the downstream PLL.

Spread spectrum can have a minor effect on the output clock by increasing the period jitter. Period jitter is the deviation of a clock's cycle time from its previous cycle position. Period jitter measures the variation of the clock output transition from its ideal position over consecutive edges.

With down-spread modulation, the peak of the modulated waveform is the actual target frequency. Therefore, the system never exceeds the maximum clock speed. To maintain reliable communication, the entire system and subsystem should use the Stratix II and Stratix II GX device as the clock source. Communication could fail if the Stratix II or Stratix II GX logic array is clocked by the spread-spectrum clock, but the data it receives from another device is not clocked by the spread spectrum.

Since spread spectrum affects the *m* counter values, all spread-spectrum PLL outputs are effected. Therefore, if only one spread-spectrum signal is needed, the clock signal should use a separate PLL without other outputs from that PLL.

No special considerations are needed when using spread spectrum with the clock switchover feature. This is because the clock switchover feature does not affect the *m* and *n* counter values, which are the counter values switching when using spread spectrum.

Board Layout

The enhanced and fast PLL circuits in Stratix II and Stratix II GX devices contain analog components embedded in a digital device. These analog components have separate power and ground pins to minimize noise generated by the digital components. Stratix II and Stratix II GX enhanced and fast PLLs use separate V_{CC} and ground pins to isolate circuitry and improve noise resistance.

V_{CCA} and GNDA

Each enhanced and fast PLL uses separate V_{CC} and ground pin pairs for their analog circuitry. The analog circuit power and ground pin for each PLL is called VCCA_PLL<*PLL number*> and GNDA_PLL<*PLL number*>. Connect the V_{CCA} power pin to a 1.2-V power supply, even if you do not use the PLL. Isolate the power connected to V_{CCA} from the power to the rest of the Stratix II or Stratix II GX device or any other digital device on the board. You can use one of three different methods of isolating the V_{CCA} pin: separate V_{CCA} power planes, a partitioned V_{CCA} island within the V_{CCINT} plane, and thick V_{CCA} traces.

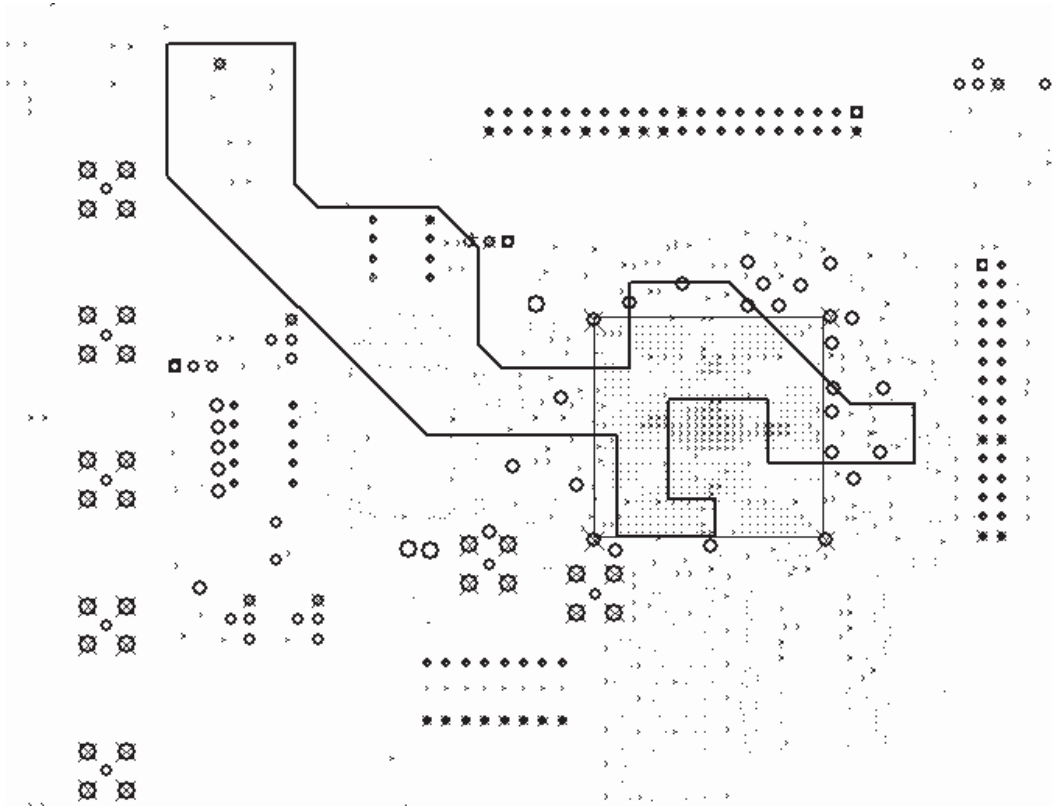
Separate V_{CCA} Power Plane

A mixed signal system is already partitioned into analog and digital sections, each with its own power planes on the board. To isolate the V_{CCA} pin using a separate V_{CCA} power plane, connect the V_{CCA} pin to the analog 1.2-V power plane.

Partitioned V_{CCA} Island Within V_{CCINT} Plane

Fully digital systems do not have a separate analog power plane on the board. Since it is expensive to add new planes to the board, you can create islands for VCCA_PLL. Figure 1–35 shows an example board layout with an analog power island. The dielectric boundary that creates the island should be 25 mils thick. Figure 1–36 shows a partitioned plane within V_{CCINT} for V_{CCA}.

Figure 1–35. V_{CCINT} Plane Partitioned for V_{CCA} Island

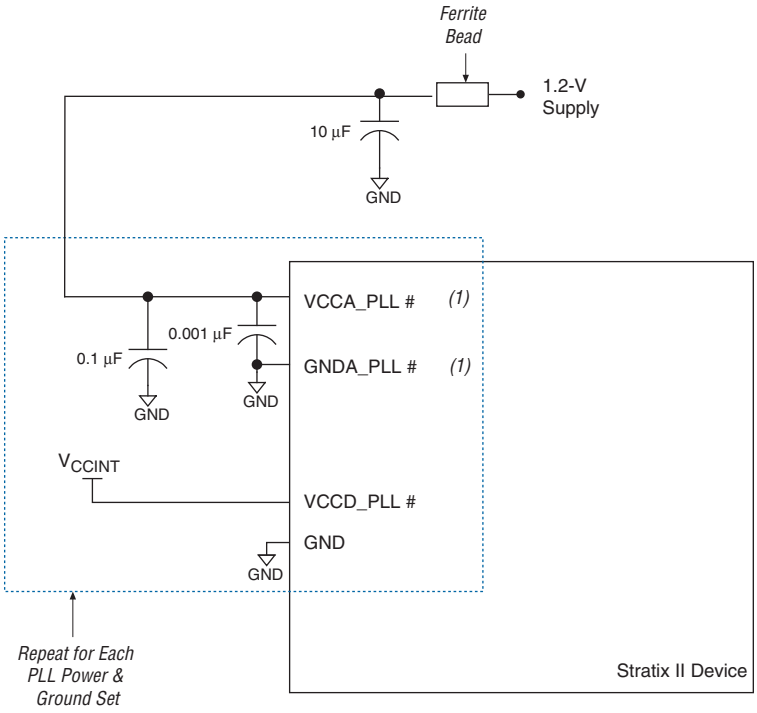


Thick V_{CCA} Trace

Because of board constraints, you may not be able to partition a V_{CCA} island. Instead, run a thick trace from the power supply to each V_{CCA} pin. The traces should be at least 20 mils thick.

In each of these three cases, you should filter each VCCA_PLL pin with a decoupling circuit, as shown in Figure 1–36. Place a ferrite bead that exhibits high impedance at frequencies of 50 MHz or higher and a 10-µF tantalum parallel capacitor where the power enters the board. Decouple each VCCA_PLL pin with a 0.1-µF and 0.001-µF parallel combination of ceramic capacitors located as close as possible to the Stratix II or Stratix II GX device. You can connect the GNDA_PLL pins directly to the same ground plane as the device's digital ground.

Figure 1–36. PLL Power Schematic for Stratix II and Stratix II GX PLLs



Note to Figure 1–36
(1) Applies to PLLs 1 through 12.

V_{CCD}

The digital power and ground pins are labeled VCCD_PLL<*PLL number*> and GND. The VCCD pin supplies the power for the digital circuitry in the PLL. Connect these VCCD pins to the quietest digital supply on the board. In most systems, this is the digital 1.2-V supply supplied to the device's V_{CCINT} pins. Connect the VCCD pins to a power supply even if you do not use the PLL. When connecting the V_{CCD} pins to V_{CCINT}, you do not need any filtering or isolation. You can connect the GND pins directly to the same ground plane as the device's digital ground. See Figure 1–36.

External Clock Output Power

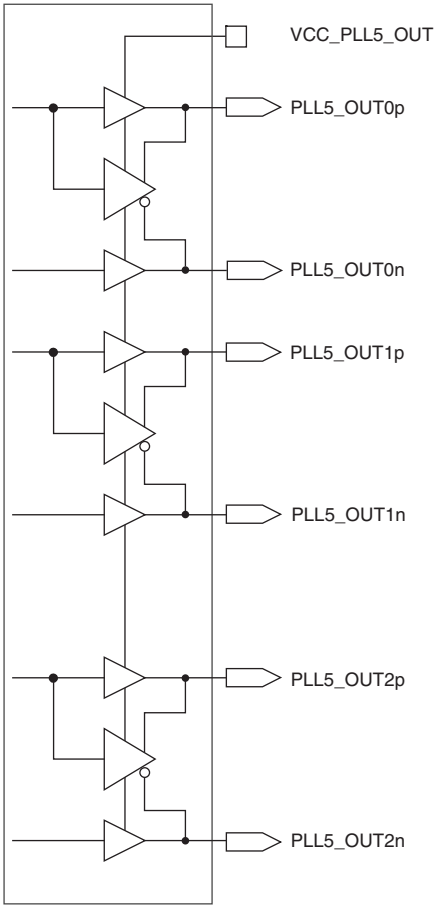
Enhanced PLLs 5, 6, 11, and 12 also have isolated power pins for their dedicated external clock outputs (VCC_PLL5_OUT, VCC_PLL6_OUT, VCC_PLL11_OUT and VCC_PLL12_OUT, respectively). Since the

dedicated external clock outputs from a particular enhanced PLL are powered by separate power pins, they are less susceptible to noise. They also reduce the overall jitter of the output clock by providing improved isolation from switching I/O pins.

I/O pins that reside in PLL banks 9 through 12 are powered by the VCC_PLL<*5, 6, 11, or 12*>_OUT pins, respectively. The EP2S60F484, EP2S60F780, EP2S90H484, EP2S90F780, and EP2S130F780 devices do not support PLLs 11 and 12. Therefore, any I/O pins that reside in bank 11 are powered by the VCCIO3 pin, and any I/O pins that reside in bank 12 are powered by the VCCIO8 pin.

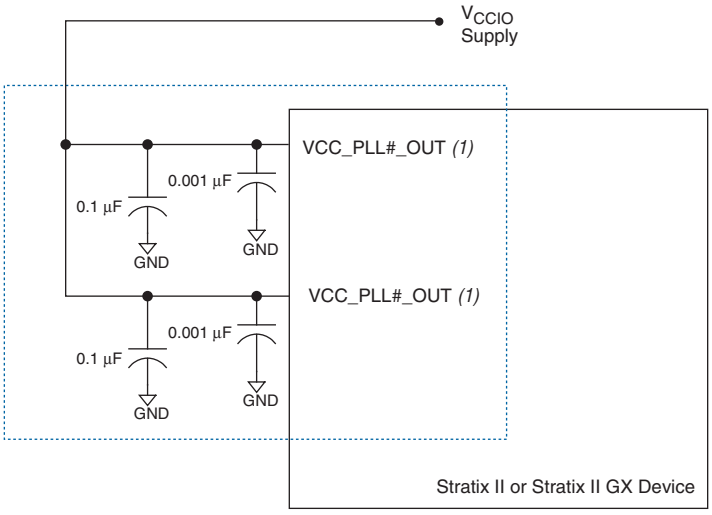
The VCC_PLL_OUT pins can by powered by 3.3, 2.5, 1.8, or 1.5 V, depending on the I/O standard for the clock output from a particular enhanced PLL, as shown in Figure 1–37.

Figure 1–37. External Clock Output Pin Association with Output Power



Filter each isolated power pin with a decoupling circuit shown in Figure 1–38. Decouple the isolated power pins with parallel combination of 0.1- and 0.001-µF ceramic capacitors located as close as possible to the Stratix II or Stratix II GX device.

Figure 1–38. Stratix II and Stratix II GX PLL External Clock Output Power Ball Connection *Note (1)*



Note to Figure 1–38:
(1) Applies only to enhanced PLLs 5, 6, 11, and 12.

Guidelines

Use the following guidelines for optimal jitter performance on the external clock outputs from enhanced PLLs 5, 6, 11, and 12. If all outputs are running at the same frequency, these guidelines are not necessary to improve performance.

- Use phase shift to ensure edges are not coincident on all the clock outputs.
- Use phase shift to skew clock edges with respect to each other for best jitter performance.

If you cannot drive multiple clocks of different frequencies and phase shifts or isolate banks, you should control the drive capability on the lower-frequency clock. Reducing how much current the output buffer has to supply can reduce the noise. Minimize capacitive load on the slower frequency output and configure the output buffer to lower current strength. The higher-frequency output should have an improved performance, but this may degrade the performance of your lower-frequency clock output.

PLL Specifications

See the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook* (or the *Stratix II Device Handbook*) for information about PLL timing specifications

Clocking

Stratix II and Stratix II GX devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock-management solution.

Global and Hierarchical Clocking

Stratix II and Stratix II GX devices provide 16 dedicated global clock networks and 32 regional clock networks. These clocks are organized into a hierarchical clock structure that allows for 24 unique clock sources per device quadrant with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains within the entire Stratix II or Stratix II GX device. Table 1–17 lists the clock resources available on Stratix II devices.

There are 16 dedicated clock pins (`CLK[15..0]`) on Stratix II and Stratix II GX devices to drive either the global or regional clock networks. Four clock pins drive each side of the Stratix II device, as shown in Figures 1–39 and 1–40**.** Enhanced and fast PLL outputs can also drive the global and regional clock networks.

Table 1–17. Clock Resource Availability in Stratix II and Stratix II GX Devices (Part 1 of 2)

Description	Stratix II Device Availability	Stratix II GX Device Availability
Number of clock input pins	24	12
Number of global clock networks	16	16
Number of regional clock networks	32	32
Global clock input sources	Clock input pins, PLL outputs, logic array	Clock input pins, PLL outputs, logic array, inter-transceiver clocks
Regional clock input sources	Clock input pins, PLL outputs, logic array	Clock input pins, PLL outputs, logic array, inter-transceiver clocks
Number of unique clock sources in a quadrant	24 (16 global clocks and 8 regional clocks)	24 (16 GCLK and 8 RCLK clocks)
Number of unique clock sources in the entire device	48 (16 global clocks and 32 regional clocks)	48 (16 GCLK and 32 RCLK clocks)

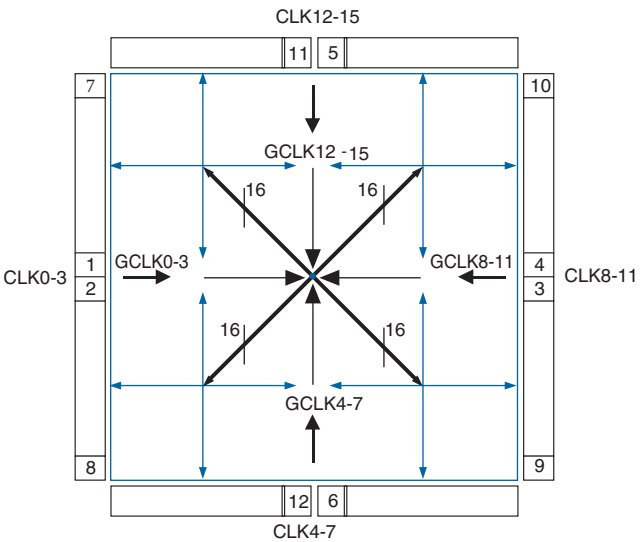
Table 1–17. Clock Resource Availability in Stratix II and Stratix II GX Devices (Part 2 of 2)

Description	Stratix II Device Availability	Stratix II GX Device Availability
Power-down mode	Global clock networks, regional clock networks, dual-regional clock region	GCLK, RCLK networks, dual-regional clock region
Clocking regions for high fan-out applications	Quadrant region, dual-regional, entire device via global clock or regional clock networks	Quadrant region, dual-regional, entire device via GCLK or RCLK networks

Global Clock Network

Global clocks drive throughout the entire device, feeding all device quadrants. All resources within the device IOEs, adaptive logic modules (ALMs), digital signal processing (DSP) blocks, and all memory blocks can use the global clock networks as clock sources. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed by an external pin. Internal logic can also drive the global clock networks for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 1–39 shows the 16 dedicated CLK pins driving global clock networks.

Figure 1–39. Global Clocking *Note (1)*



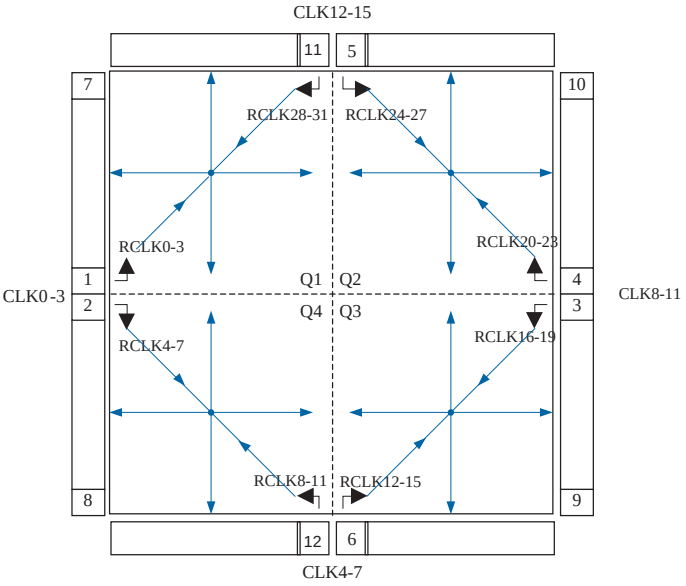
Note to Figure 1–39:

(1) Stratix II GX devices do not have PLLs 3, 4, 9, and 10 or clock pins 8, 9, 10, and 11.

Regional Clock Network

Eight regional clock networks within each quadrant of the Stratix II and Stratix II GX device are driven by the dedicated `CLK[15..0]` input pins or from PLL outputs. The regional clock networks only pertain to the quadrant they drive into. The regional clock networks provide the lowest clock delay and skew for logic contained within a single quadrant. Internal logic can also drive the regional clock networks for internally generated regional clocks and asynchronous clears, clock enables, or other control signals with large fanout.The `CLK` clock pins symmetrically drive the RCLK networks within a particular quadrant, as shown in Figure 1–40. Refer to Table 1–18 on page 1–67 and Table 1–19 on page 1–68 for RCLK connections from `CLK` pins and PLLs.

Figure 1–40. Regional Clocking *Note (1)*

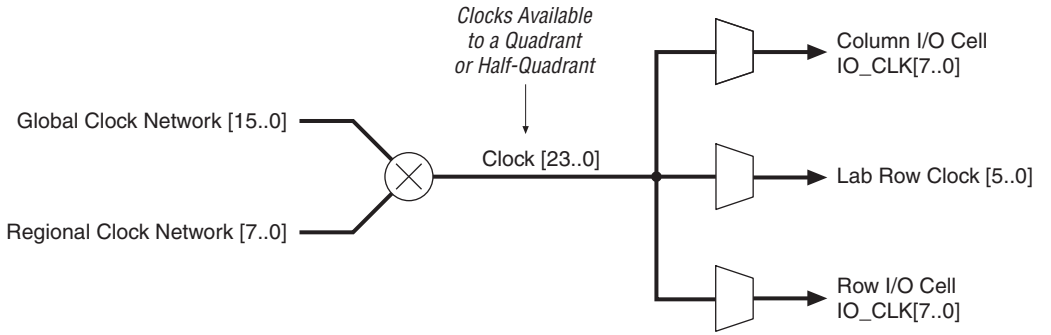


Note to Figure 1–40:
(1) Stratix II GX devices do not have PLLs 3, 4, 9, and 10 or clock pins 8, 9, 10, and 11.

Clock Sources Per Region

Each Stratix II and Stratix II GX device has 16 global clock networks and 32 regional clock networks that provide 48 unique clock domains for the entire device. There are 24 unique clocks available in each quadrant (16 global clocks and 8 regional clocks) as the input resources for registers (see Figure 1–41).

Figure 1–41. Hierarchical Clock Networks Per Quadrant



Stratix II and Stratix II GX clock networks provide three different clocking regions:

- Entire device clock region
- Quadrant clock region
- Dual-regional clock region

These clock network options provide more flexibility for routing signals that have high fan-out to improve the interface timing. By having various sized clock regions, it is possible to prioritize the number of registers the network can reach versus the total delay of the network.

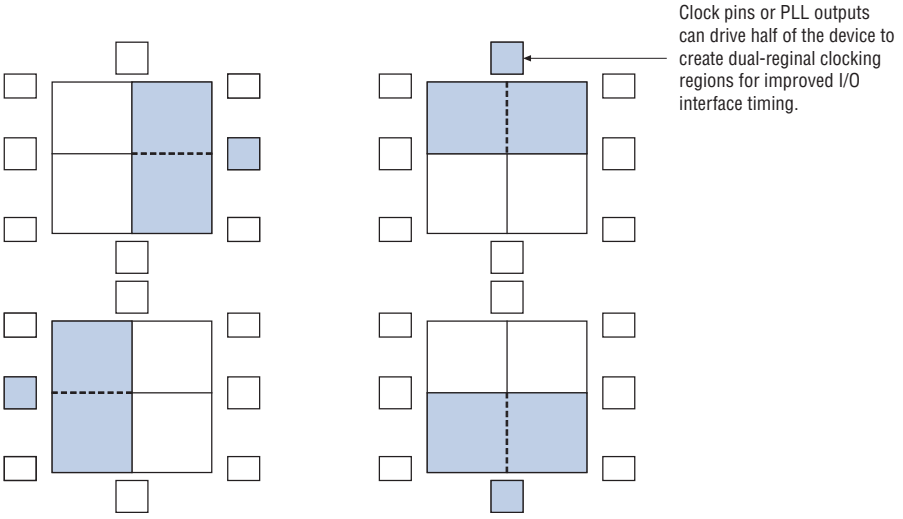
In the first clock scheme, a source (not necessarily a clock signal) drives a global clock network that can be routed through the entire device. This has the maximum delay for a low skew high fan-out signal but allows the signal to reach every block within the device. This is a good option for routing global resets or clear signals.

In the second clock scheme, a source drives a single-quadrant region. This represents the fastest, low-skew, high-fan-out signal-routing resource within a quadrant. The limitation to this resource is that it only covers a single quadrant.

In the third clock scheme, a single source (clock pin or PLL output) can generate a dual-regional clock by driving two regional clock network lines (one from each quadrant). This allows logic that spans multiple quadrants to utilize the same low-skew clock. The routing of this signal on an entire side has approximately the same speed as in a quadrant clock region. The internal logic-array routing that can drive a regional clock also supports this feature. This means internal logic can drive a

dual-regional clock network. Corner fast PLL outputs only span one quadrant and hence cannot form a dual-regional clock network. Figure 1–42 shows this feature pictorially.

Figure 1–42. Stratix II and Stratix II GX Dual-Regional Clock Region



The 16 clock input pins, enhanced or fast PLL outputs, and internal logic array can be the clock input sources to drive onto either global or regional clock networks. The CLKn pins also drive the global clock network as shown in Table 1–22 on page 1–72. Tables 1–18 and 1–19 for the connectivity between CLK pins as well as the global and regional clock networks.

Clock Inputs

The clock input pins CLK[15..0] are also used for high fan-out control signals, such as asynchronous clears, presets, clock enables, or protocol signals such as TRDY and IRDY for PCI through global or regional clock networks.

Internal Logic Array

Each global and regional clock network can also be driven by logic-array routing to enable internal logic to drive a high fan-out, low-skew signal.

PLL Outputs

All clock networks can be driven by the PLL counter outputs.

Table 1–18 shows the connection of the clock pins to the global clock resources. The reason for the higher level of connectivity is to support user controllable global clock multiplexing.

Table 1–18. Clock Input Pin Connectivity to Global Clock Networks

Clock Resource	CLK(p) (Pin)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
GCLK0	✓	✓														
GCLK1	✓	✓														
GCLK2			✓	✓												
GCLK3			✓	✓												
GCLK4					✓	✓										
GCLK5					✓	✓										
GCLK6							✓	✓								
GCLK7							✓	✓								
GCLK8											✓ (1)	✓ (1)				
GCLK9											✓ (1)	✓ (1)				
GCLK10									✓ (1)	✓ (1)						
GCLK11									✓ (1)	✓ (1)						
GCLK12															✓	✓
GCLK13															✓	✓
GCLK14													✓	✓		
GCLK15													✓	✓		

Note to Table 1–18:

(1) Clock pins 8, 9, 10, and 11 are not available in Stratix II GX devices. Therefore, these connections do not exist in Stratix II GX devices.

Table 1–19 summarizes the connectivity between the clock pins and the regional clock networks. Here, each clock pin can drive two regional clock networks, facilitating stitching of the clock networks to support the ability to drive two quadrants with the same clock or signal.

Table 1–19. Clock Input Pin Connectivity to Regional Clock Networks (Part 1 of 2)

Clock Resource	CLK(p) (Pin)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RCLK0	✓															
RCLK1		✓														
RCLK2			✓													
RCLK3				✓												
RCLK4	✓															
RCLK5		✓														
RCLK6			✓													
RCLK7				✓												
RCLK8					✓											
RCLK9						✓										
RCLK10							✓									
RCLK11								✓								
RCLK12					✓											
RCLK13						✓										
RCLK14							✓									
RCLK15								✓								
RCLK16											✓ (1)					
RCLK17												✓ (1)				
RCLK18									✓ (1)							
RCLK19										✓ (1)						
RCLK20											✓ (1)					
RCLK21												✓ (1)				
RCLK22									✓ (1)							

Table 1–19. Clock Input Pin Connectivity to Regional Clock Networks (Part 2 of 2)

Clock Resource	CLK(p) (Pin)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RCLK23										✓ (1)						
RCLK24															✓	
RCLK25																✓
RCLK26													✓			
RCLK27														✓		
RCLK28															✓	
RCLK29																✓
RCLK30													✓			
RCLK31														✓		

Note to Table 1–19:

(1) Clock pins 8, 9, 10, and 11 are not available in Stratix II GX devices. Therefore, these connections do not exist in Stratix II GX devices.

Clock Input Connections

Four CLK pins drive each enhanced PLL. You can use any of the pins for clock switchover inputs into the PLL. The CLK pins are the primary clock source for clock switchover, which is controlled in the Quartus II software. Enhanced PLLs 5, 6, 11, and 12 also have feedback input pins, as shown in Table 1–20.

Input clocks for fast PLLs 1, 2, 3, and 4 come from CLK pins. A multiplexer chooses one of two possible CLK pins to drive each PLL. This multiplexer is not a clock switchover multiplexer and is only used for clock input connectivity.

Either an FPLLCLK input pin or a CLK pin can drive the fast PLLs in the corners (7, 8, 9, and 10) when used for general-purpose applications. CLK pins cannot drive these fast PLLs in high-speed differential I/O mode.

Tables 1–20 and 1–21 show which PLLs are available in each Stratix II and Stratix II GX device, respectively, and which input clock pin drives which PLLs.

Table 1–20. Stratix II Device PLLs and PLL Clock Pin Drivers (Part 1 of 2)

Input Pin	All Devices						EP2S60 to EP2S180 Devices					
	Fast PLLs				Enhanced PLLs		Fast PLLs				Enhanced PLLs	
	1	2	3	4	5	6	7	8	9	10	11	12
CLK0	✓	✓					✓ (1)	✓ (1)				
CLK1 (2)	✓	✓					✓ (1)	✓ (1)				
CLK2	✓	✓					✓ (1)	✓ (1)				
CLK3 (2)	✓	✓					✓ (1)	✓ (1)				
CLK4						✓						✓
CLK5						✓						✓
CLK6						✓						✓
CLK7						✓						✓
CLK8			✓	✓					✓ (1)	✓ (1)		
CLK9 (2)			✓	✓					✓ (1)	✓ (1)		
CLK10			✓	✓					✓ (1)	✓ (1)		
CLK11 (2)			✓	✓					✓ (1)	✓ (1)		
CLK12					✓						✓	
CLK13					✓						✓	
CLK14					✓						✓	
CLK15					✓						✓	
PLL5_FB					✓							
PLL6_FB						✓						
PLL11_FB											✓	
PLL12_FB												✓
PLL_ENA	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
FPLL7CLK (2)							✓					
FPLL8CLK (2)								✓				
FPLL9CLK (2)									✓			

Table 1–20. Stratix II Device PLLs and PLL Clock Pin Drivers (Part 2 of 2)

Input Pin	All Devices						EP2S60 to EP2S180 Devices					
	Fast PLLs				Enhanced PLLs		Fast PLLs				Enhanced PLLs	
	1	2	3	4	5	6	7	8	9	10	11	12
FPLL10CLK *(2)*										✓		

Notes to Table 1–20:
(1) Clock connection is available. For more information about the maximum frequency, contact Altera Applications.
(2) This is a dedicated high-speed clock input. For more information about the maximum frequency, contact Altera Applications.

Table 1–21. Stratix II GX Device PLLs and PLL Clock Pin Drivers (Part 1 of 2)

Input Pin	All Devices						EP2SGX60 to EP2SGX130 Devices					
	Fast PLLs				Enhanced PLLs		Fast PLLs				Enhanced PLLs	
	1	2	3 *(1)*	4 *(1)*	5	6	7	8	9 *(1)*	10 *(1)*	11	12
CLK0	✓	✓					✓*(2)*	✓*(2)*				
CLK1 *(2)*	✓	✓					✓*(2)*	✓*(2)*				
CLK2	✓	✓					✓*(2)*	✓*(2)*				
CLK3 *(2)*	✓	✓					✓*(2)*	✓*(2)*				
CLK4						✓						✓
CLK5						✓						✓
CLK6						✓						✓
CLK7						✓						✓
CLK8 *(4)*												
CLK9 *(3)*, *(4)*												
CLK10 *(4)*												
CLK11 *(3)*, *(4)*												
CLK12					✓						✓	
CLK13					✓						✓	
CLK14					✓						✓	
CLK15					✓						✓	
PLL5_FB					✓							
PLL6_FB						✓						
PLL11_FB											✓	

Table 1–21. Stratix II GX Device PLLs and PLL Clock Pin Drivers (Part 2 of 2)

Input Pin	All Devices						EP2SGX60 to EP2SGX130 Devices					
	Fast PLLs				Enhanced PLLs		Fast PLLs				Enhanced PLLs	
	1	2	3 *(1)*	4 *(1)*	5	6	7	8	9 *(1)*	10 *(1)*	11	12
PLL12_FB												✓
PLL_ENA	✓	✓			✓	✓	✓	✓			✓	✓
FPLL7CLK *(3)*							✓					
FPLL8CLK *(3)*								✓				
FPLL9CLK *(3)*												
FPLL10CLK *(3)*												

Notes to Table 1–21:

(1) PLLs 3, 4, 9, and 10 are not available in Stratix II GX devices.
(2) Clock connection is available. For more information about the maximum frequency, contact Altera Applications.
(3) This is a dedicated high-speed clock input. For more information about the maximum frequency, contact Altera Applications.
(4) Input pins `CLK[11..8]` are not available in Stratix II GX devices.

CLK(n) Pin Connectivity to Global Clock Networks

In Stratix II and Stratix II GX devices, the `clk(n)` pins can also feed the global clock network. Table 1–22 shows the `clk(n)` pin connectivity to global clock networks.

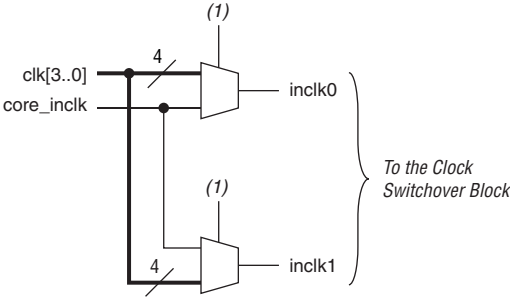
Table 1–22. CLK(n) Pin Connectivity to Global Clock Network

Clock Resource	CLK(n) pin							
	4	5	6	7	12	13	14	15
GCLK4	✓							
GCLK5		✓						
GCLK6			✓					
GCLK7				✓				
GCLK12							✓	
GCLK13								✓
GCLK14					✓			
GCLK15						✓		

Clock Source Control For Enhanced PLLs

The clock input multiplexer for enhanced PLLs is shown in Figure 1–43. This block allows selection of the PLL clock reference from several different sources. The clock source to an enhanced PLL can come from any one of four clock input pins `CLK[3..0]`, or from a logic-array clock, provided the logic array clock is driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block, provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL. The clock input pin connections to the respective enhanced PLLs are shown in Table 1–20 above. The multiplexer select lines are set in the configuration file only. Once programmed, this block cannot be changed without loading a new configuration file. The Quartus II software automatically sets the multiplexer select signals depending on the clock sources that a user selects in the design.

Figure 1–43. Enhanced PLL Clock Input Multiplex Logic



Note to Figure 1–43:

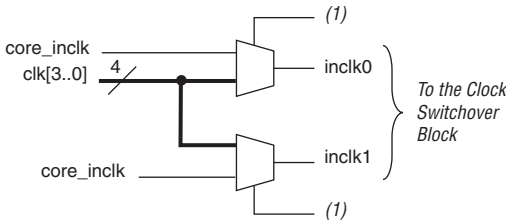
(1) The input clock multiplexing is controlled through a configuration file only and cannot be dynamically controlled in user mode.

Clock Source Control for Fast PLLs

Each center fast PLL has five clock input sources, four from clock input pins, and one from a logic array signal, provided the logic array signal is driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block, provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL. When using clock input pins as the clock source, you can perform manual clock switchover among the input clock sources.

The clock input multiplexer control signals for performing clock switchover are from core signals. Figure 1–44 shows the clock input multiplexer control circuit for a center fast PLL.

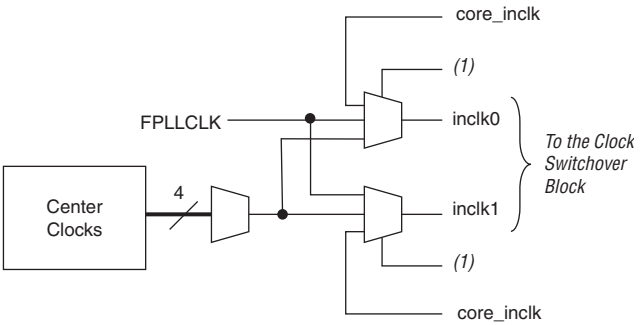
Figure 1–44. Center Fast PLL Clock Input Multiplexer Control



Note to Figure 1–44:
(1) The input clock multiplexing is controlled through a configuration file only and cannot be dynamically controlled in user mode.

Each corner fast PLL has three clock input sources, one from a dedicated corner clock input pin, one from a center clock input pin, and one from a logic array clock, provided the logic array signal is driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block, provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL. Figure 1–45 shows a block diagram showing the clock input multiplexer control circuit for a corner fast PLL. Only the corner FPLLCLK pin is fully compensated.

Figure 1–45. Corner Fast PLL Clock Input Multiplexer Control



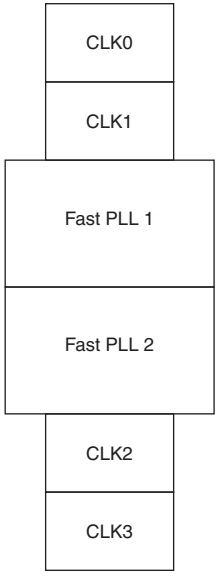
Note to Figure 1–45:
(1) The input clock multiplexing is controlled through a configuration file only and cannot be dynamically controlled in user mode.

Delay Compensation for Fast PLLs

Each center fast PLL can be fed by any one of four possible input clock pins. Among the four clock input signals, only two are fully compensated, i.e., the clock delay to the fast PLL matches the delay in the data input path when used in the LVDS receiver mode. The two clock inputs that match the data input path are located right next to the fast PLL. The two clock inputs that do not match the data input path are located next to the neighboring fast PLL. Figure 1–46 shows the above description for the left-side center fast PLL pair. If the PLL is used in non-LVDS modes, then any of the four dedicated clock inputs can be used and are compensated.

Fast PLL 1 and PLL 2 can choose among `CLK[3..0]` as the clock input source. However, for fast PLL 1, only `CLK0` and `CLK1` have their delay matched to the data input path delay when used in the LVDS receiver mode operation. The delay from `CLK2` or `CLK3` to fast PLL 1 does not match the data input delay. For fast PLL 2, only `CLK2` and `CLK3` have their delay matched to the data input path delay in LVDS receiver mode operation. The delay from `CLK0` or `CLK1` to fast PLL 2 does not match the data input delay. The same arrangement applies to the right side center fast PLL pair. For corner fast PLLs, only the corner `FPLLCLK` pins are fully compensated. For LVDS receiver operation, it is recommended to use the delay compensated clock pins only.

Figure 1–46. Delay Compensated Clock Input Pins for Center Fast PLL Pair



Clock Output Connections

Enhanced PLLs have outputs for eight regional clock outputs and four global clock outputs. There is line sharing between clock pins, global and regional clock networks and all PLL outputs. See Tables 1–18 through 1–23 and Figures 1–47 through 1–53 to validate your clocking scheme. The Quartus II software automatically maps to regional and global clocks to avoid any restrictions. Enhanced PLLs 5, 6, 11, and 12 drive out to single-ended pins as shown in Table 1–23.

You can connect each fast PLL 1, 2, 3, or 4 output (`C0`, `C1`, `C2`, and `C3`) to either a global or a regional clock. There is line sharing between clock pins, `FPLLCLK` pins, global and regional clock networks, and all PLL outputs. The Quartus II software will automatically map to regional and global clocks to avoid any restrictions.

Figure 1–47 shows the clock input and output connections from the enhanced PLLs.

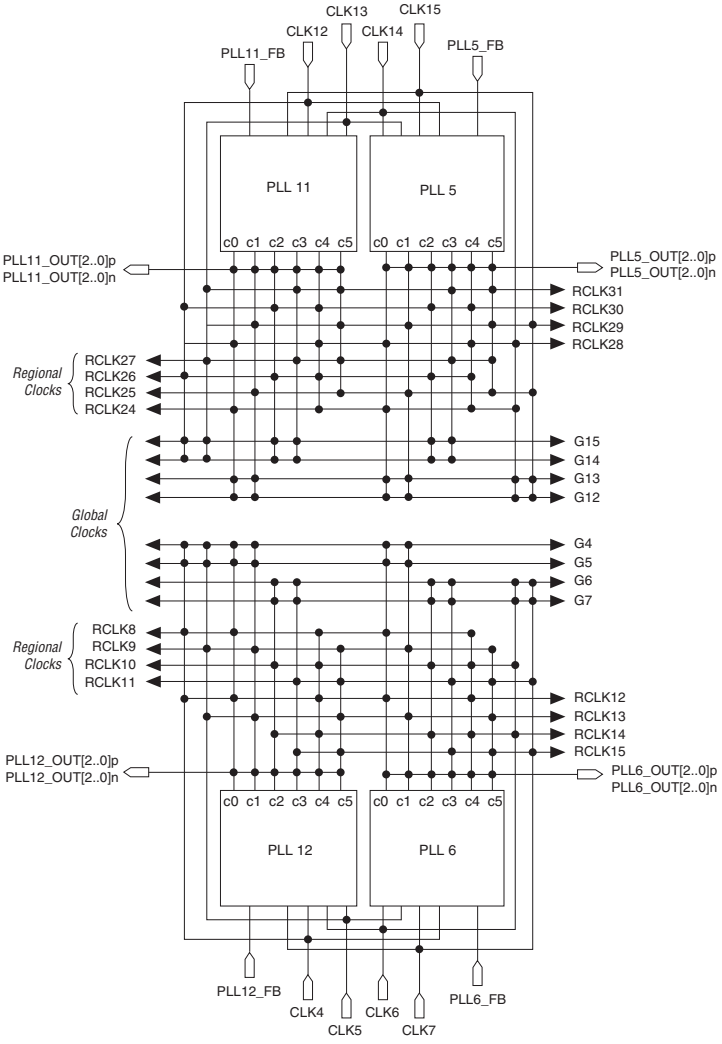
EP2S15, EP2S30, and EP2SGX30 devices have only two enhanced PLLs (5, 6), but the connectivity from these two PLLs to the global or regional clock networks remains the same.

The EP2S60 device in the 1,020-pin package contains 12 PLLs. EP2S60 devices in the 484-pin and 672-pin packages contain fast PLLs 1–4 and enhanced PLLs 5 and 6.

EP2S90 devices in the 1020-pin and 1508-pin packages contain 12 PLLs. EP2S90 devices in the 484-pin and 780-pin packages contain fast PLLs 1–4 and enhanced PLLs 5 and 6.

EP2S130 devices in the 1020-pin and 1508-pin packages contain 12 PLLs. The EP2S130 device in the 780-pin package contains fast PLLs 1–4 and enhanced PLLs 5 and 6.

Figure 1–47. Stratix II and Stratix II GX Top and Bottom Enhanced PLLs, Clock Pin and Logic Array Signal Connectivity to Global and Regional Clock Networks *Notes (1) and (2)*



Notes to Figure 1–47:

(1) The redundant connection dots facilitate stitching of the clock networks to support the ability to drive two quadrants with the same clock.

(2) The enhanced PLLs can also be driven through the global or regional clock networks. The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block, provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

Tables 1–23 and 1–24 show the global and regional clocks that the PLL outputs drive.

Table 1–23. Stratix II Global and Regional Clock Outputs From PLLs (Part 1 of 3)

Clock Network	PLL Number and Type											
	EP2S15 through EP2S30 Devices						EP2S60 through EP2S180 Devices					
	Fast PLLs				Enhanced PLLs		Fast PLLs				Enhanced PLLs	
	1	2	3	4	5	6	7	8	9	10	11	12
GCLK0	✓	✓					✓	✓				
GCLK1	✓	✓					✓	✓				
GCLK2	✓	✓					✓	✓				
GCLK3	✓	✓					✓	✓				
GCLK4						✓						✓
GCLK5						✓						✓
GCLK6						✓						✓
GCLK7						✓						✓
GCLK8			✓	✓					✓	✓		
GCLK9			✓	✓					✓	✓		
GCLK10			✓	✓					✓	✓		
GCLK11			✓	✓					✓	✓		
GCLK12					✓						✓	
GCLK13					✓						✓	
GCLK14					✓						✓	
GCLK15					✓						✓	
RCLK0	✓	✓					✓					
RCLK1	✓	✓					✓					
RCLK2	✓	✓					✓					
RCLK3	✓	✓					✓					
RCLK4	✓	✓						✓				
RCLK5	✓	✓						✓				
RCLK6	✓	✓						✓				
RCLK7	✓	✓						✓				
RCLK8						✓						✓
RCLK9						✓						✓

Table 1–23. Stratix II Global and Regional Clock Outputs From PLLs (Part 2 of 3)

Clock Network	PLL Number and Type											
	EP2S15 through EP2S30 Devices						EP2S60 through EP2S180 Devices					
	Fast PLLs				Enhanced PLLs		Fast PLLs				Enhanced PLLs	
	1	2	3	4	5	6	7	8	9	10	11	12
RCLK10						✓						✓
RCLK11						✓						✓
RCLK12						✓						✓
RCLK13						✓						✓
RCLK14						✓						✓
RCLK15						✓						✓
RCLK16			✓	✓					✓			
RCLK17			✓	✓					✓			
RCLK18			✓	✓					✓			
RCLK19			✓	✓					✓			
RCLK20			✓	✓						✓		
RCLK21			✓	✓						✓		
RCLK22			✓	✓						✓		
RCLK23			✓	✓						✓		
RCLK24					✓						✓	
RCLK25					✓						✓	
RCLK26					✓						✓	
RCLK27					✓						✓	
RCLK28					✓						✓	
RCLK29					✓						✓	
RCLK30					✓						✓	
RCLK31					✓						✓	
External Clock Output												
PLL5_OUT[3..0]p/n					✓							
PLL6_OUT[3..0]p/n						✓						

Table 1–23. Stratix II Global and Regional Clock Outputs From PLLs (Part 3 of 3)

Clock Network	PLL Number and Type											
	EP2S15 through EP2S30 Devices						EP2S60 through EP2S180 Devices					
	Fast PLLs				Enhanced PLLs		Fast PLLs				Enhanced PLLs	
	1	2	3	4	5	6	7	8	9	10	11	12
PLL11_OUT[3..0]p/n											✓	
PLL12_OUT[3..0]p/n												✓

Table 1–24. Stratix II GX Global and Regional Clock Outputs From PLLs (Part 1 of 3)

Clock Network	PLL Number and Type											
	EP2SGX30 Devices						EP2SGX60 through EP2SGX130 Devices *Notes (2)*, *(3)*, and *(4)*					
	Fast PLLs				Enhanced PLLs		Fast PLLs				Enhanced PLLs	
	1	2	3 *(1)*	4 *(1)*	5	6	7	8	9 *(1)*	10 *(1)*	11	12
GCLK0	✓	✓					✓	✓				
GCLK1	✓	✓					✓	✓				
GCLK2	✓	✓					✓	✓				
GCLK3	✓	✓					✓	✓				
GCLK4						✓						✓
GCLK5						✓						✓
GCLK6						✓						✓
GCLK7						✓						✓
GCLK8												
GCLK9												
GCLK10												
GCLK11												
GCLK12					✓						✓	
GCLK13					✓						✓	
GCLK14					✓						✓	
GCLK15					✓						✓	

Table 1–24. Stratix II GX Global and Regional Clock Outputs From PLLs (Part 2 of 3)

Clock Network	PLL Number and Type											
	EP2SGX30 Devices						EP2SGX60 through EP2SGX130 Devices *Notes (2), (3), and (4)*					
	Fast PLLs				Enhanced PLLs		Fast PLLs				Enhanced PLLs	
	1	2	3 *(1)*	4 *(1)*	5	6	7	8	9 *(1)*	10 *(1)*	11	12
RCLK0	✓	✓					✓					
RCLK1	✓	✓					✓					
RCLK2	✓	✓					✓					
RCLK3	✓	✓					✓					
RCLK4	✓	✓						✓				
RCLK5	✓	✓						✓				
RCLK6	✓	✓						✓				
RCLK7	✓	✓						✓				
RCLK8						✓						✓
RCLK9						✓						✓
RCLK10						✓						✓
RCLK11						✓						✓
RCLK12						✓						✓
RCLK13						✓						✓
RCLK14						✓						✓
RCLK15						✓						✓
RCLK16												
RCLK17												
RCLK18												
RCLK19												
RCLK20												
RCLK21												
RCLK22												
RCLK23												
RCLK24					✓						✓	
RCLK25					✓						✓	
RCLK26					✓						✓	
RCLK27					✓						✓	

Table 1–24. Stratix II GX Global and Regional Clock Outputs From PLLs (Part 3 of 3)

Clock Network	PLL Number and Type											
	EP2SGX30 Devices						EP2SGX60 through EP2SGX130 Devices *Notes (2)*, *(3)*, and *(4)*					
	Fast PLLs				Enhanced PLLs		Fast PLLs				Enhanced PLLs	
	1	2	3 *(1)*	4 *(1)*	5	6	7	8	9 *(1)*	10 *(1)*	11	12
RCLK28					✓						✓	
RCLK29					✓						✓	
RCLK30					✓						✓	
RCLK31					✓						✓	
External Clock Output												
PLL5_OUT[3..0]p/n					✓							
PLL6_OUT[3..0]p/n						✓						
PLL11_OUT[3..0]p/n											✓	
PLL12_OUT[3..0]p/n												✓

Notes to Table 1–24:

(1) PLLs 3, 4, 9, and 10 are not available in Stratix II GX devices.

(2) The EP2S60 device in the 1,020-pin package contains 12 PLLs. EP2S60 devices in the 484-pin and 672-pin packages contain fast PLLs 1–4 and enhanced PLLs 5 and 6.

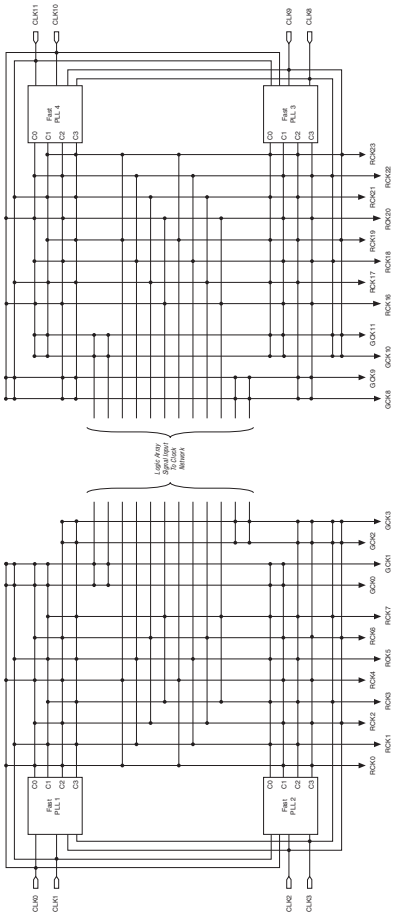
(3) EP2S90 devices in the 1020-pin and 1508-pin packages contain 12 PLLs. EP2S90 devices in the 484-pin and 780-pin packages contain fast PLLs 1–4 and enhanced PLLs 5 and 6.

(4) EP2S130 devices in the 1020-pin and 1508-pin packages contain 12 PLLs. The EP2S130 device in the 780-pin package contains fast PLLs 1–4 and enhanced PLLs 5 and 6.

The fast PLLs also drive high-speed SERDES clocks for differential I/O interfacing. For information about these FPLLCLK pins, contact Altera Applications.

Figures 1–48 through 1–51 show the global and regional clock input and output connections from the Stratix II fast PLLs.

Figure 1–48. Stratix II Center Fast PLLs, Clock Pin and Logic Array Signal Connectivity to Global and Regional Clock Networks *Notes (1) and (2)*

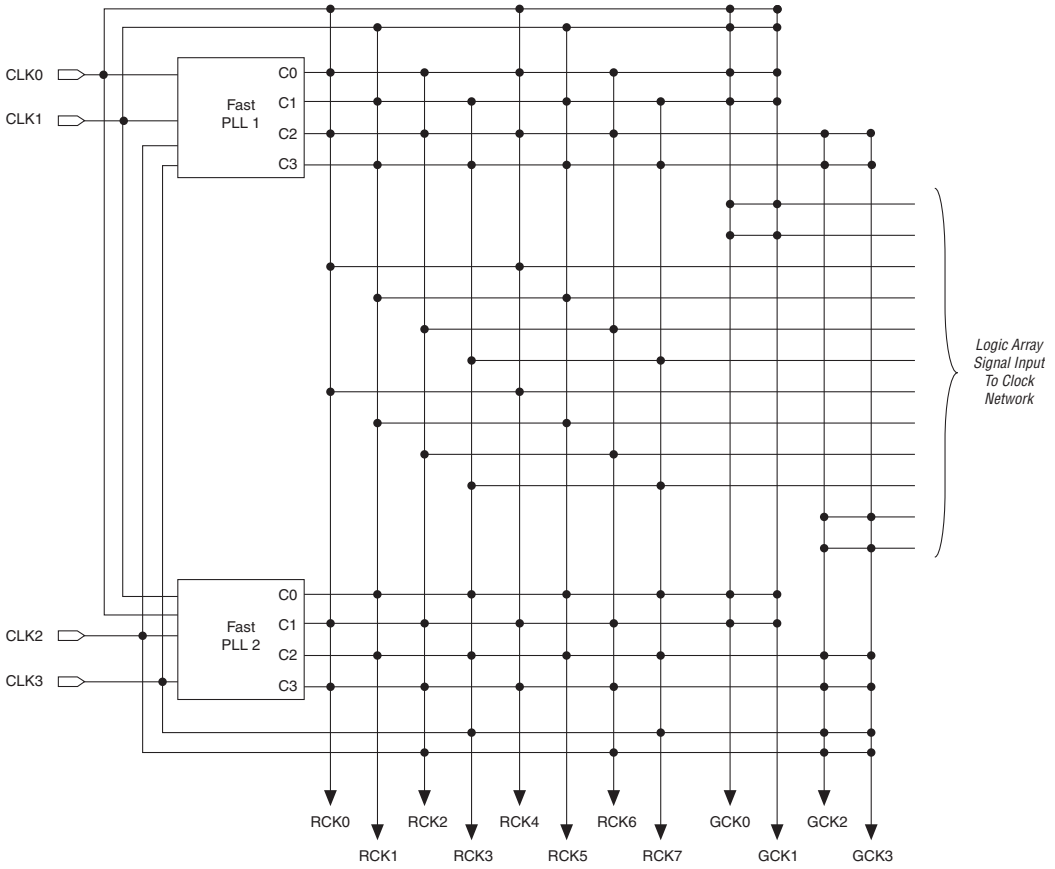


Notes to Figure 1–48:

(1) The redundant connection dots facilitate stitching of the clock networks to support the ability to drive two quadrants with the same clock.

(2) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block, provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

Figure 1–49. Stratix II GX Center Fast PLLs, Clock Pin and Logic Array Signal Connectivity to Global and Regional Clock Networks *Notes (1) and (2)*

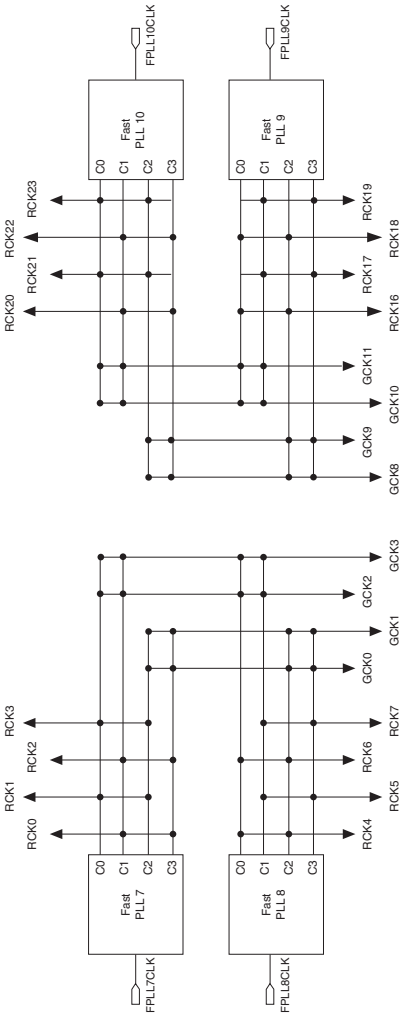


Notes to Figure 1–49:

(1) The redundant connection dots facilitate stitching of the clock networks to support the ability to drive two quadrants with the same clock.

(2) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block, provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

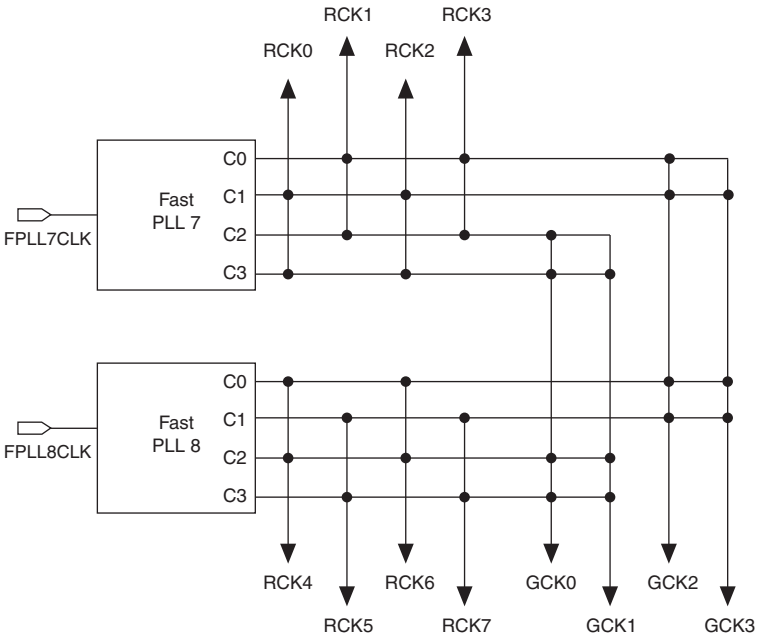
Figure 1–50. Stratix II Corner Fast PLLs, Clock Pin and Logic Array Signal Connectivity to Global and Regional Clock Networks *Note (1)*



Note to Figure 1–50:

(1) The corner FPLLs can also be driven through the global or regional clock networks. The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block, provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

Figure 1–51. Stratix II GX Corner Fast PLLs, Clock Pin and Logic Array Signal Connectivity to Global and Regional Clock Networks *Note (1)*



Note to Figure 1–51:

(1) The corner FPLLs can also be driven through the global or regional clock networks. The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block, provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

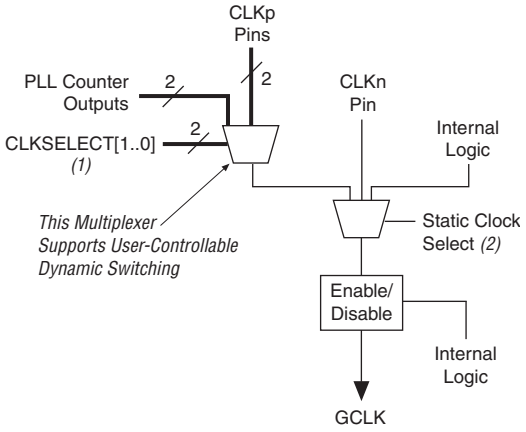
Clock Control Block

Each global and regional clock has its own clock control block. The control block has two functions:

- Clock source selection (dynamic selection for global clocks)
- Clock power-down (dynamic clock enable or disable)

Figures 1–52 and 1–53 show the global clock and regional clock select blocks, respectively.

Figure 1–52. Stratix II Global Clock Control Block

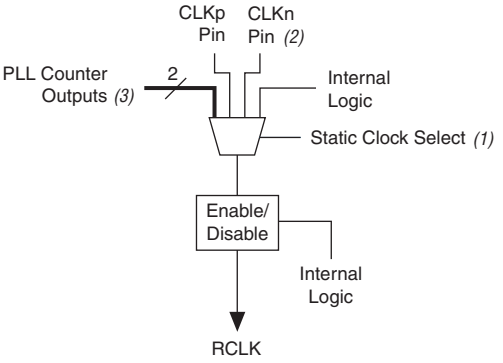


Notes to Figure 1–52:

(1) These clock select signals can only be dynamically controlled through internal logic when the device is operating in user mode.

(2) These clock select signals can only be set through a configuration file and cannot be dynamically controlled during user-mode operation.

Figure 1–53. Regional Clock Control Block



Notes to Figure 1–53:

(1) These clock select signals can only be dynamically controlled through a configuration file and cannot be dynamically controlled during user-mode operation.

(2) Only the CLK*n* pins on the top and bottom for the device feed to regional clock select blocks.

For the global clock select block, the clock source selection can be controlled either statically or dynamically. You have the option to statically select the clock source in configuration file generated by the Quartus II software, or you can control the selection dynamically by using internal logic to drive the multiplexer select inputs. When selecting statically, the clock source can be set to any of the inputs to the select multiplexer. When selecting the clock source dynamically, you can either select two PLL outputs (such as CLK0 or CLK1), or a combination of clock pins or PLL outputs.

When using the altclkctrl megafunction to implement clock source (dynamics) selection, the inputs from the clock pins feed the inclock[0..1] ports of the multiplexer, while the PLL outputs feed the inclock[2..3] ports. You can choose from among these inputs using the CLKSELECT[1..0] signal.

For the regional clock select block, the clock source selection can only be controlled statically using configuration bits. Any of the inputs to the clock select multiplexer can be set as the clock source.

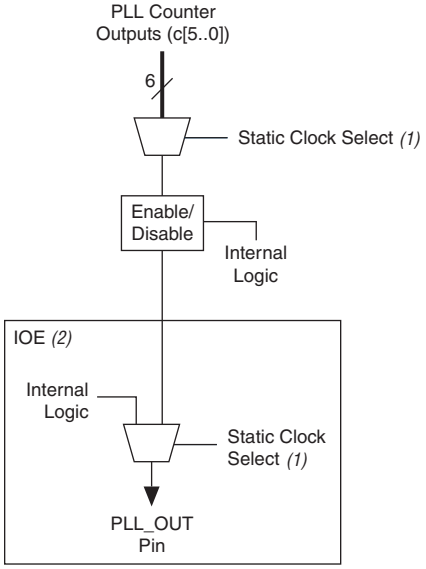
The Stratix II and Stratix II GX clock networks can be disabled (powered down) by both static and dynamic approaches. When a clock net is powered down, all the logic fed by the clock net is in an off-state, thereby reducing the overall power consumption of the device.

The global and regional clock networks that are not used are automatically powered down through configuration bit settings in the configuration file (SRAM Object File (**.sof**) or Programmer Object File (**.pof**)) generated by the Quartus II software.

The dynamic clock enable or disable feature allows the internal logic to control power up or down synchronously on GCLK and RCLK nets, including dual-regional clock regions. This function is independent of the PLL and is applied directly on the clock network, as shown in Figure 1–52 on page 1–87 and Figure 1–53 on page 1–88.

The input clock sources and the clkena signals for the global and regional clock network multiplexers can be set through the Quartus II software using the altclkctrl megafunction. The dedicated external clock output pins can also be enabled or disabled using the altclkctrl megafunction. Figure 1–54 shows the external PLL output clock control block.

Figure 1–54. Stratix II External PLL Output Clock Control Block



Notes to Figure 1–54:

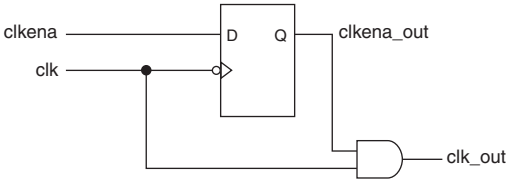
(1) These clock select signals can only be set through a configuration file and cannot be dynamically controlled during user mode operation.

(2) The clock control block feeds to a multiplexer within the PLL_OUT pin's IOE. The PLL_OUT pin is a dual-purpose pin. Therefore, this multiplexer selects either an internal signal or the output of the clock control block.

clkena Signals

Figure 1–55 shows how clkena is implemented.

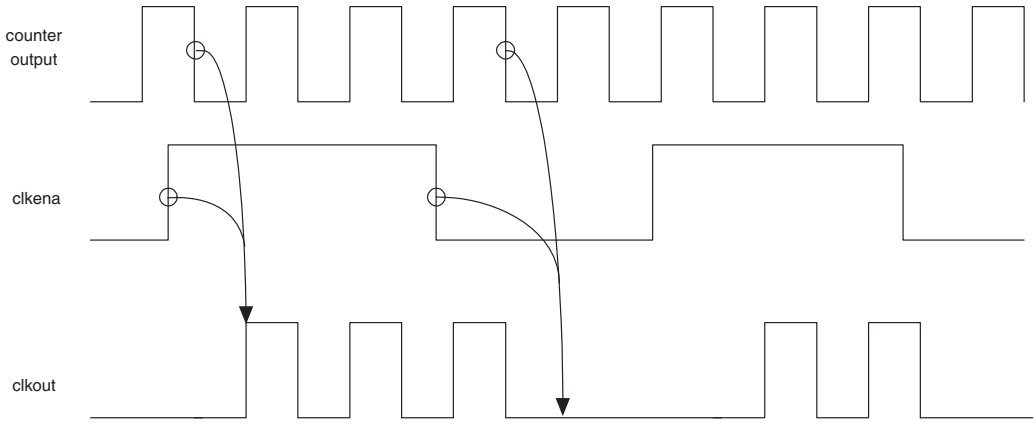
Figure 1–55. clkena Implementation



In Stratix II devices, the clkena signals are supported at the clock network level. This allows you to gate off the clock even when a PLL is not being used.

The clkena signals can also be used to control the dedicated external clocks from enhanced PLLs. Upon re-enabling, the PLL does not need a resynchronization or relock period unless the PLL is using external feedback mode. Figure 1–56 shows the waveform example for a clock output enable. clkena is synchronous to the falling edge of the counter output.

Figure 1–56. Clkena Signals



Note to Figure 1–56

(1) The clkena signals can be used to enable or disable the global and regional networks or the PLL_OUT pins.

The PLL can remain locked independent of the `clkena` signals since the loop-related counters are not affected. This feature is useful for applications that require a low power or sleep mode. Upon re-enabling, the PLL does not need a resynchronization or relock period. The `clkena` signal can also disable clock outputs if the system is not tolerant to frequency overshoot during resynchronization.

Conclusion

Stratix II and Stratix II GX device enhanced and fast PLLs provide you with complete control of device clocks and system timing. These PLLs are capable of offering flexible system-level clock management that was previously only available in discrete PLL devices. The embedded PLLs meet and exceed the features offered by these high-end discrete devices, reducing the need for other timing devices in the system.

Referenced Documents

This chapter references the following documents:

- *altpll Megafunction User Guide*
- *AN 367: Implementing PLL Reconfiguration in Stratix II Devices*
- *Configuring Stratix II and Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* (or the *Stratix II Device Handbook)*
- *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook* (or the *Stratix II Device Handbook*)
- *Selectable I/O Standards in Stratix II and Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* (or the *Stratix II Device Handbook*)
- Verification, volume 3 of the *Quartus II Development Software Handbook*

Document Revision History

Table 1–25 shows the revision history for this chapter.

Table 1–25. Document Revision History (Part 1 of 2)

Date and Document Version	Changes Made	Summary of Changes
July 2009, v4.6	• Updated "Manual Override", "Manual Clock Switchover", and "Spread-Spectrum Clocking" sections. • Updated notes to Figure 1–20 and Figure 1–24.	• Both `inclk0` and `inclk1` must be running when the `clkswitch` signal goes high to initiate a manual clock switchover. • Updated the spread spectrum modulation frequency from (100 kHz–500 kHz) to (30 kHz–150 kHz).
January 2008, v4.5	Updated "External Clock Outputs" section.	—
	Added the "Referenced Documents" section.	—
	Minor text edits.	—
No change	For the *Stratix II GX Device Handbook* only: Formerly chapter 6. The chapter number changed due to the addition of the *Stratix II GX Dynamic Reconfiguration* chapter. No content change.	—
May 2007, v4.4	Updated Table 7–6.	—
	Updated notes to: • Figure 7–7 • Figure 7–47 • Figure 7–48 • Figure 7–49 • Figure 7–50 • Figure 7–51	—
	Updated the "Clock Source Control For Enhanced PLLs" section.	—
	Updated the "Clock Source Control for Fast PLLs" section.	—
February 2007 v4.3	Added "Document Revision History" section to this chapter.	—
	Deleted paragraph beginning with "The Stratix II GX PLLs have the ability..." in the "Enhanced Lock Detect Circuit" section.	—
April 2006, v4.2	Chapter updated as part of the *Stratix II Device Handbook* update.	—
No change	Formerly chapter 5. Chapter number change only due to chapter addition to Section I in February 2006; no content change.	—

Table 1–25. Document Revision History (Part 2 of 2)

Date and Document Version	Changes Made	Summary of Changes
December 2005, v4.1	Chapter updated as part of the *Stratix II Device Handbook* update.	—
October 2005 v4.0	Added chapter to the *Stratix II GX Device Handbook*.	—