ADI Parallel Port SDRAM Controller Reference Design

June 2005, Version 1.3 Application Note 334

Introduction

The ADI parallel port SDRAM controller reference design connects SDRAM to the parallel port of an Analog Devices Incorporated (ADI) ADSP-2126x Sharc DSP device and is implemented in Altera® FPGAs and CPLDs.

Altera supplies the reference design as Verilog HDL source code. The reference design includes a testbench that allows you to test the Verilog HDL source code.

The purpose of this reference design is to demonstrate that Altera devices provide a low cost SDRAM interface for ADI Sharc DSP devices.

Background

The ADI Parallel Port

The SDRAM controller supports the 8-bit mode of the ADSP-2126x parallel port in which the 16 most significant bits (MSBs) of the address are available on `AD[15:0]` during address latch enable (ALE) cycles. The eight least significant bits (LSBs) of the address (byte address) are available on `AD[15:8]` during read and write cycles. A single byte of data is available on `AD[7:0]` during read and write cycles. ALE cycles occur only when the 16 MSBs of the address change. Parallel port transfers are always four bytes (one word) starting at byte address `b'xxxxxx00`.

The parallel port has no provision for a slave to insert wait states.

Performance Requirements

The DSP core clock `CCLK` has a maximum frequency of 200 MHz. The length of the parallel port read and write cycles is programmable between 2 and 31 `CCLK` periods. There is always one `CCLK` period between each byte read or write in a word. Thus, a sustained burst of byte reads or writes with minimum cycle timing is equivalent to `CCLK`/3 or 66 megabit per second (Mbps). The memory controller supports operation at 66 Mbps.

Critical Timing Areas

A number of critical timing paths are identified in the parallel-port interface. Figure 2 shows an ALE cycle and a single read cycle.

Figure 1. Read Cycle Timing

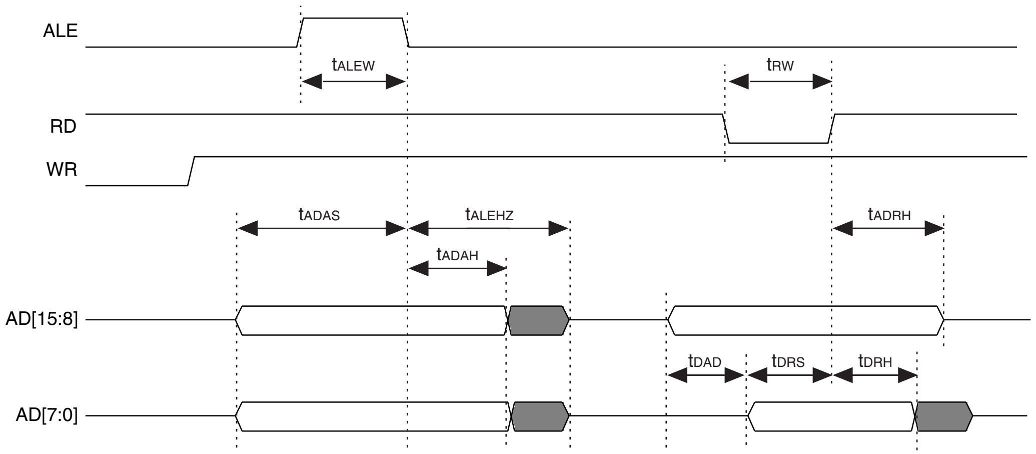


Table 1 shows the minimum read cycle timing parameters for 66-Mbps operation.

Table 1. Minimum Read Cycle Timing Parameters for 66 Mbps

Parameter	Time (ns)
t_{ALEW}	8
t_{RW}	8
t_{DAD}	9
t_{DRS}	3.3

The ALE strobe is asynchronous with a guaranteed maximum width, t_{ALEW}, of 8 ns. Read and write strobes are asynchronous. For 66 Mbps they have a guaranteed minimum width, t_{RW}, of 8 ns. The minimum period for which read and write strobes is de-asserted is not specified but is assumed to be approximately one `CCLK` period or 5 ns. To use the strobes synchronously, a local clock in excess of 400 MHz is required to double sample the negation of the read and write strobes between each byte.

If the strobes are used asynchronously, only 5.78 ns is available for the output enable during read cycles. To select read data from the byte address, 10ns (t_{DAD}) is available.

If the rising edge of each read strobe is used as a clock for the next read data, 13 ns (3 × CCLK period – t_{DAD}) is available as the t_{CO} for selection of the next read data byte.

SDRAM Requirements

SDRAM requires initialization, periodic refresh, page open, and page close (precharge) cycles in addition to read and write cycles. The lack of a wait mechanism on the parallel port requires that all access to SDRAM by the parallel port complete in the same fixed number of cycles. Refresh and page operations must not interfere with data accesses.

Refresh and page open and close operations are scheduled in software by the DSP and initiated through a register set within the SDRAM controller. This is acceptable as the DSP is expected to be running an algorithm in a regular well-timed execution loop with a priori knowledge of what data movements are required (allowing the correct page to be opened for reading or writing) and when the data is required (allowing refreshes to be scheduled). Initialization is a once only operation following reset and is also initiated through the register set.

Resource Requirements

Table 2 shows resource requirements and their advantages and disadvantages.

Table 2. Resource Requirements

Family	Advantage	Disadvantage	Macrocells /LEs
MAX® II	Slowest speed grade is sufficient. Instant on.	–	266
MAX	Instant on.	Requires the fastest speed grade.	234
Cyclone™	Slowest speed grade is sufficient. Space in smallest device to integrate system glue logic.	Requires configuration.	265

Supported Devices

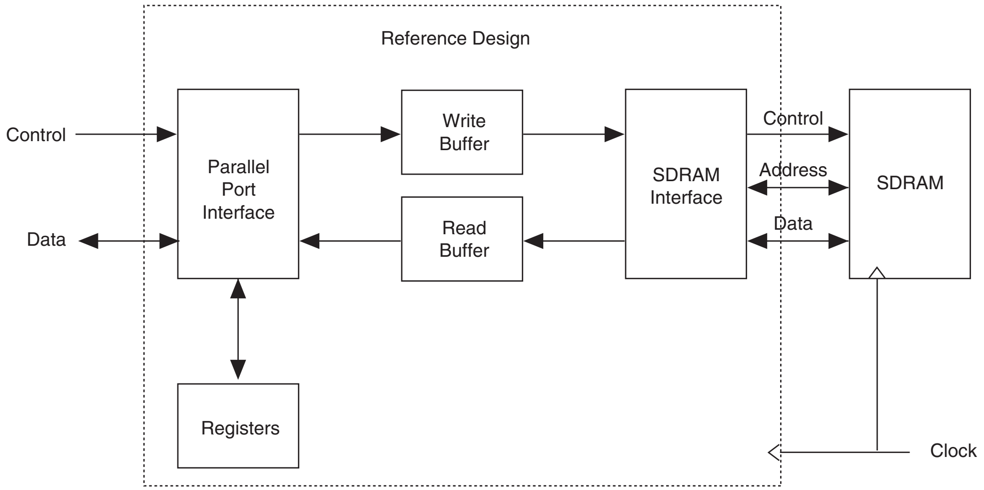
The SDRAM controller supports 128-Mbit byte-wide SDRAM, e.g., Micron MT48LC16M8A2.

☞ The reference design can be modified to support other memory sizes.

Functional Description

Figure 2 shows the block diagram.

Figure 2. Block Diagram



Registers

SDRAM controller registered are accessed in the highest 256 bytes of the parallel port address space selected by an ALE cycle with `AD[15:0]` = `0xffff`. Table 3 shows the SDRAM controller register memory map. All registers are write only.

Table 3. SDRAM Controller Registers

Register	Address	Description
`INIT`	0xffff00	The SDRAM will be initialized by a parallel port write to the INIT register.
`REFRESH`	0xffff04	A parallel port write to the REFRESH register will cause a burst of 8 auto refresh cycles to be performed.
`OPEN_READ`	0xffff08	A bank opens for reading by performing a parallel port write to the OPEN_READ register. The data written to the register will specify the row address, bank address and starting column address bits for the location to be accessed by subsequent read operations.
`OPEN_WRITE`	0xffff0c	A bankopens for writing by performing a parallel port write to the controllers OPEN_WRITE register. The data written to the register will specify the row address, bank address and starting column address bits for the location to be accessed by subsequent write operations.

Table 3. SDRAM Controller Registers		
Register	**Address**	**Description**
POWER_DOWN	0xffff10	A parallel port write to the POWER_DOWN register will put the SDRAM into power down mode.
POWER_UP	0xffff14	A parallel port write to the POWER_UP register will put the SDRAM into idle mode redy for a page to be opened for reading or writing.

Table 3 shows the bit fields for the OPEN_READ and OPEN_WRITE registers..

Table 4. OPEN_READ and OPEN_WRITE Register Format	
Bits	**Description**
31:24	Unused—write 0
23:12	Row address
11:10	Bank address
9:0	Column address

Operation

This sections describes the following operations

- Initialization
- Refresh
- Write accesses
- Read accesses
- Power down

Initialization

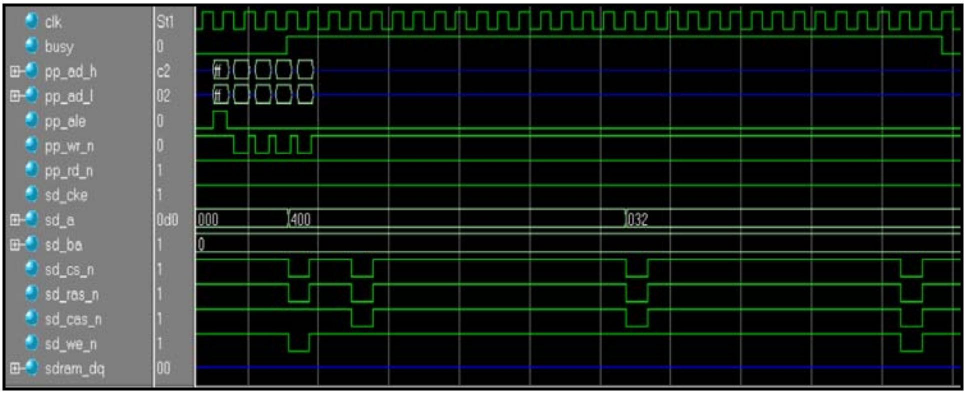
A parallel port write to the INIT register causes the SDRAM controller to perform the following operations:

- precharge all
- two auto refresh cycles
- load mode register

The BUSY output of the SDRAM controller asserts whilst these operations are being performed (see Figure 3).

No other accesses are allowed to the SDRAM controller whilst BUSY is asserted.

Figure 3. SDRAM Initialization

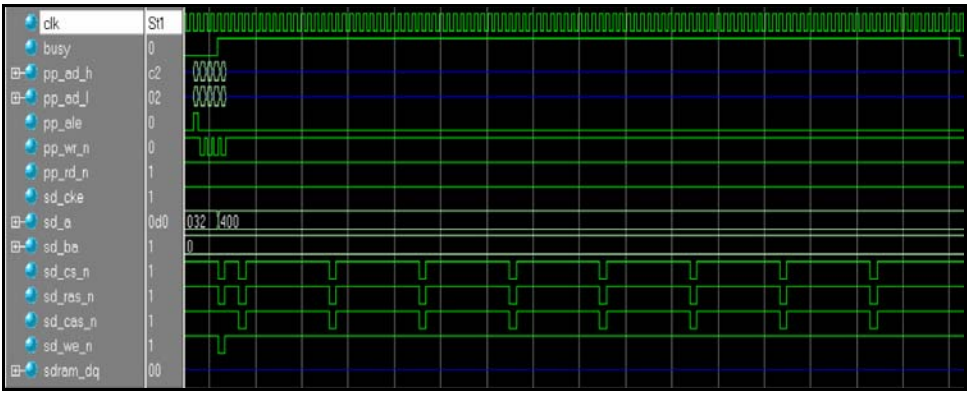


Refresh

A parallel port write to the REFRESH register causes a precharge all command to be issued to the SDRAM followed by a burst of eight auto-refresh commands. The BUSY output of the SDRAM controller is asserted whilst the refreshes are being performed (see Figure 4).

No other accesses are allowed to the SDRAM controller whilst BUSY is asserted.

Figure 4. SDRAM Refresh Burst



Write Accesses

Writing to the OPEN_WRITE register causes a precharge all command to be issued to the SDRAM followed by an active command for all banks at the specified row address. When an SDRAM bank has been opened for writing, write data is pipelined through the controller, which gives the appearance of operating at the parallel ports maximum rate of 66 Mbps. Write access are allowed to random bank or column addresses (see Figures 5 and 6).

Figure 5. SDRAM Write Bank Opening

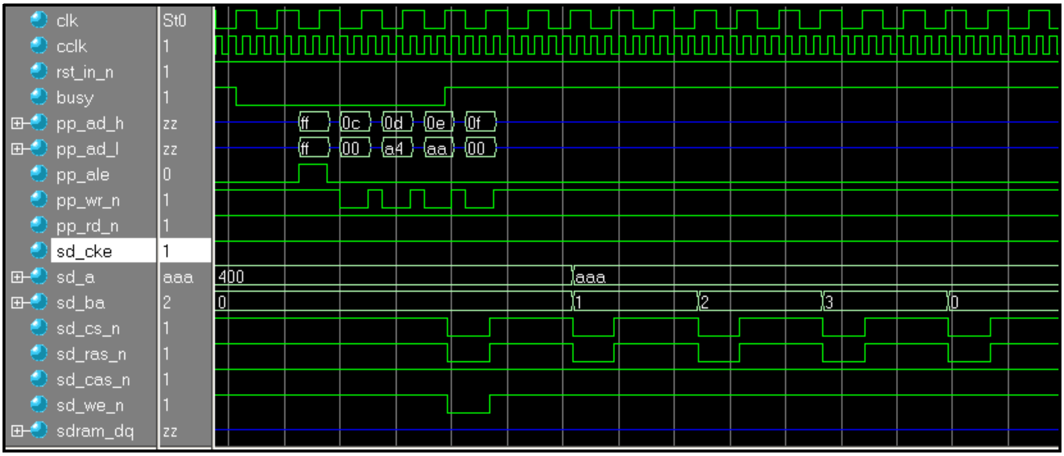
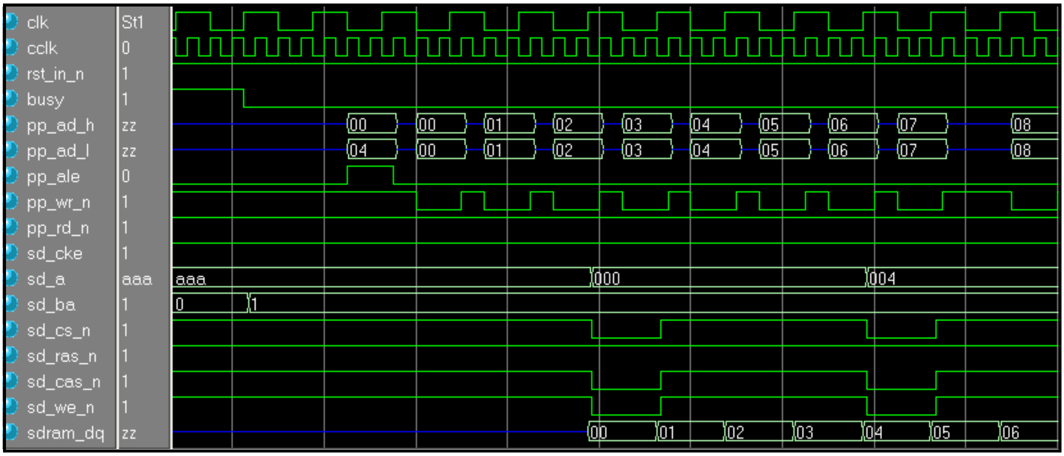


Figure 6. SDRAM Write Cycles



Read Accesses

Writing to the OPEN_READ register causes a precharge all command to be issued to the SDRAM followed by an active command for all four banks at the specified row address. When an SDRAM bank has been opened for reading, the SDRAM exhibits latency from issuing of each read command to the required data being returned. To remove the effect of this latency, the controller prefetches data and imposes strict rules on read access patterns allowed via the parallel port. Opening a bank for reading causes data to be prefetched from the SDRAM, starting at bank or column address specified, into an internal buffer. Each subsequent read returns the prefetched data to the parallel port and prefetch new data for a further read. Thus, data is always read from successive locations in all banks, wrapping around from the end of bank3 to the start of bank0, regardless of the byte address on AD[15:8] (see Figures 7 and 8).

Figure 7. SDRAM Read Bank Opening & Prefetch

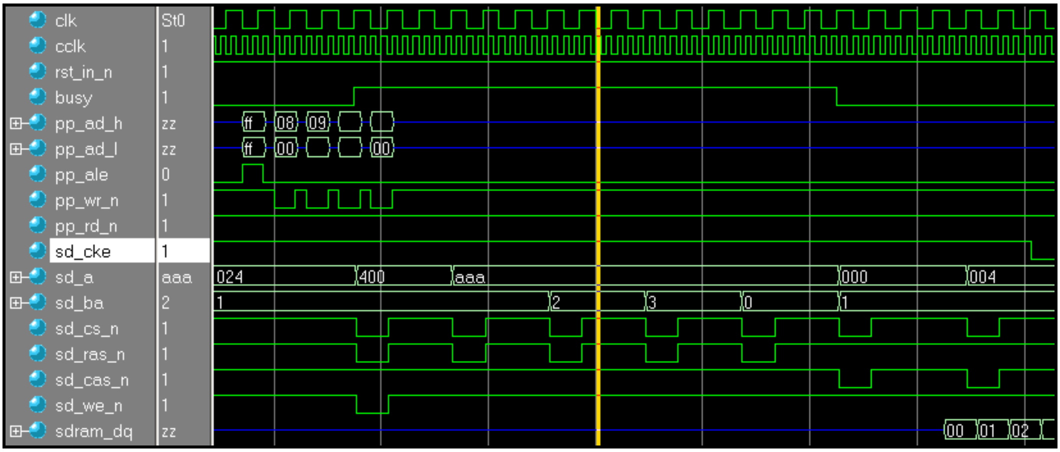
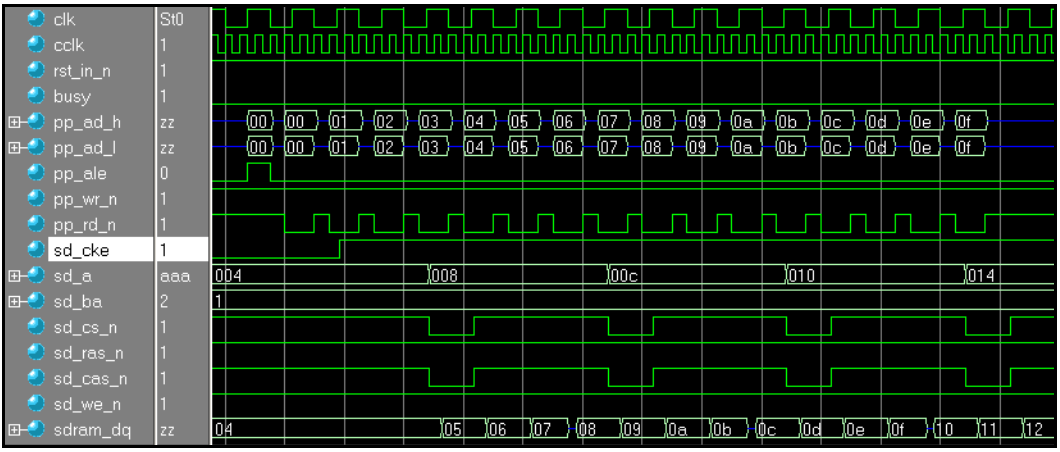


Figure 8. SDRAM Read Cycles & Prefetch

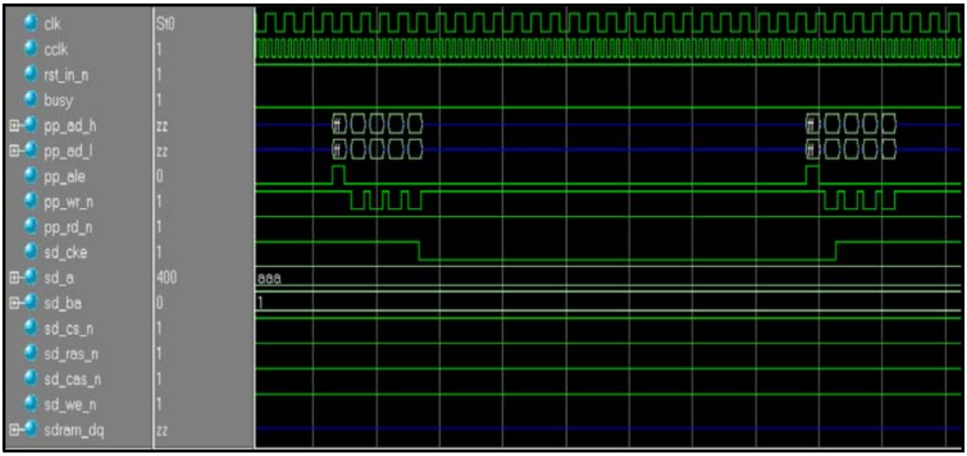


Power Down

The SDRAM may be powered down by a performing a parallel port write to the `POWER_DOWN` register. The SDRAM must be powered up again (by writing to the `POWER_UP` register) for refresh at the scheduled interval. The SDRAM clock enable (`CKE`) is driven low to put the device into power down mode. If the SDRAM was previously open for reading or writing, issue a refresh burst before the power down.

The SDRAM must be powered up (by writing to the `POWER_UP` register) before further operations take place. Attempting to write to the SDRAM whilst in power down results in loss of data. Attempting to read returns undefined data. Figure 5 shows power down and power up.

Figure 9. Power Down & Power Up



Getting Started

This section involves the following steps:

1. "Software Requirements".
2. "Install the Design".

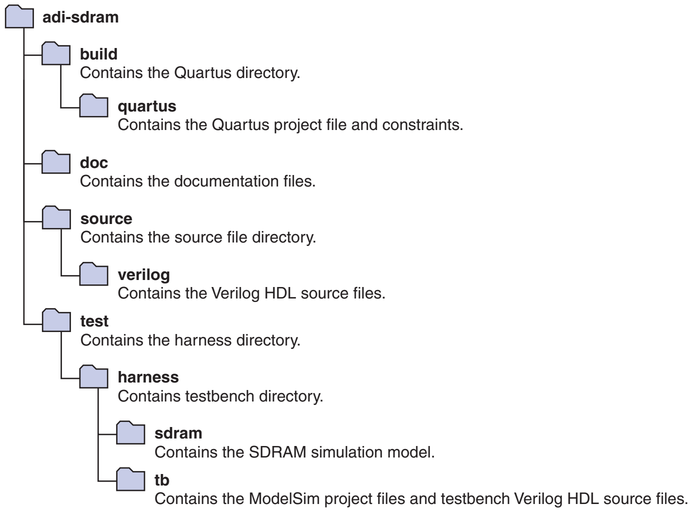
Software Requirements

The reference design requires the Quartus® II software version 4.2, or higher.

Install the Design

To install the reference design, run the **.exe** and follow the installation instructions. Figure 10 shows the directory structure.

Figure 10. Directory Structure



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