AN 597: Getting Started Flow for Board Designs

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This application note provides an overview of the Altera® FPGA design flow.

Introduction

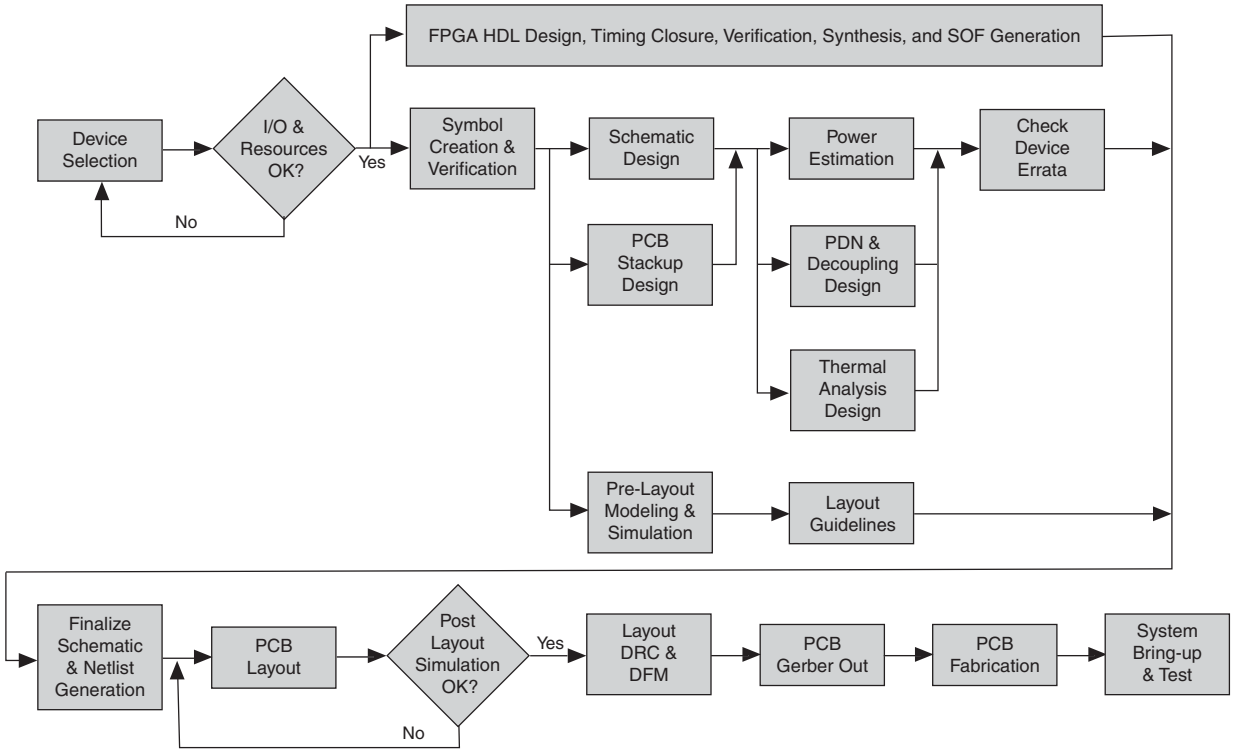
In many system designs, the typical design flow begins with a Marketing Requirements Document (MRD) that specifies both the high-level business justifications and the technical requirements of the product to be developed. After the document is approved, the responsible engineering team uses it to produce a more detailed technical Product Requirements Document (PRD). The PRD typically specifies the architectural implementation of the product and may even specify certain key components required in the design implementation. Detailed design specifications are generated by the design engineers from this PRD.

An FPGA is a key component that is frequently used in complex system designs because of its programmable nature and integrated high-speed transceivers. Because of this flexibility, FPGAs have become central to the system, allowing designers to easily bridge different technologies and drive high-speed backplanes. However, because of its flexible nature, designing with FPGAs can also present a challenge if the designer is not fully familiar with the FPGA design process. This document presents a quick overview of the Altera FPGA board design flow and provides links to relevant additional information to ensure a successful and robust FPGA implementation.

FPGA Design Flow

Figure 1 shows the typical design flow using an Altera FPGA device. The following sections describe each relevant step in the FPGA design process. Where applicable, links to related information are provided for further guidance.

Figure 1. FPGA System Design Flow



Device Selection

The typical FPGA design process begins with selecting the Altera FPGA device that best meets the system's requirements, such as the number of I/O pins, LVDS channels, clock and PLL resources, amount of integrated RAM, DSP blocks, number of transceivers, and so forth. When a device is selected that delivers the resources and performance required, schematic and FPGA HDL design can proceed.

For information about device features and resources to aid with device selection, refer to the Altera Product Selector.

Schematic Symbol Creation

Schematic capture begins with the creation of the FPGA symbol. Due to the programmable nature of most I/O pins in the FPGA, careful pin planning at this stage helps lessen layout complexity and reduce layer count. Use the following conventions and the checklist in "User I/Os" on page 4 to create the schematic symbol:

- Consider the system level floorplanning of the interconnected devices on the board and assign pins that minimize signal crossings in the layout stage
- Give programmable I/O pins names that reflect their intended function for better schematic readability
- Name dedicated pins such as configuration and power pins according to their dedicated function

- Compile the final pin assignments in Altera's Quartus® II design compiler software to ensure the pin assignments meet the device requirements and I/O placement rules

For the complete Altera FPGA device family pin-out files to help with the schematic symbol creation, refer to the Pin-Out Files for Altera Devices web page.

Users of Cadence's Capture schematic tool can download the premade Altera schematic symbol libraries from the Cadence Capture CIS and Allegro PCB Symbols and Footprints web page.

Schematic Design

When a verified symbol is complete, the schematic capture connects all FPGA pins to their respective interfaces according to their usage requirements.

Refer to the Altera Pin Connection Guidelines for the device selected to ensure that any specific Altera recommendations or requirements are met.

Use the appropriate Device Schematic Review Worksheet to verify your schematic connections and ensure that all Altera guidelines are correctly followed.

Altera FPGA pins can be divided into the following categories.

Configuration and JTAG Pins

Because FPGAs are SRAM-based devices, they require configuration data to be reloaded each time the device powers up. These pins are used to program the FPGA with Quartus II-generated configuration data. Some configuration pins are dedicated for this purpose, while others can also be used as user I/O pins after device configuration is complete. For flexibility, Altera devices support a wide variety of configuration modes to satisfy the application requirement. Select one or more configuration modes based on the design requirements.

For information about configuring Altera FPGA devices, refer to the Configuration Center web page.

For detailed information about each configuration mode, refer to the *Configuration Handbook*.

For additional training on configuring Altera FPGA devices, refer to the *Configuring Altera FPGAs* online training course.

In addition to the configuration pins, Altera devices provide dedicated JTAG pins that are always available for device programming and debugging, regardless of the configuration mode selected. Always connect the JTAG pins to a 10-pin JTAG header so device programming and the SignalTap II Embedded Logic Analyzer debugging tool can be used with any of the available Altera download cables.

For more information about the SignalTap II Embedded Logic Analyzer, refer to the *Design Debugging Using the SignalTap II Embedded Logic Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

For more information about Altera's download cables, refer to the following documents:

- *ByteBlaster II Download Cable User Guide*
- *USB-Blaster Download Cable User Guide*
- *EthernetBlaster Communications Cable User Guide*

Clock and PLL Inputs

Clocking within the FPGA is divided into regions. For example, in Stratix IV devices, the clock regions are driven by Global Clock (GCLK) networks, Regional Clock (RCLK) networks, and PLL outputs. The dedicated clock input pins provide the external clock sources to these GCLK and RCLK networks and PLLs within the device. Because of the fixed location of the dedicated clock input pins and PLLs, not all clock pins can drive all regions of the device and PLL resources. As a result, clock pin assignments must consider internal clocking and PLL resources that are available to the pin.

For detailed information about Clocking and PLL resources, refer to the *Clock Networks and PLLs* chapter of the respective device handbook on the Literature and Technical Documentation web page.

User I/Os

I/O pins are designed to support a wide range of industry I/O standards, allowing the flexibility to easily interface with different technologies. I/O pins are arranged in groups around the device called *I/O banks*. Depending on the device, these I/O pins may provide added features such as dynamic On-Chip Termination (OCT), programmable current strength, programmable slew rate, and programmable delay for easy interfacing flexibility, improved signal integrity, and timing controls without external components. However, because an I/O bank is restricted to a single I/O power (V_{CCIO}) and reference voltage (V_{REF}) within the bank, mixing I/O standards with different V_{CCIO} or V_{REF} voltages in the same bank is not allowed. As a result, careful pin planning must be done to optimize pin and bank usage.

Use the following checklist for making I/O pin assignments:

- ☐ Select a suitable signaling type and I/O standard for each I/O pin
- ☐ Ensure that the appropriate I/O standard is supported in the targeted I/O bank
- ☐ Place I/O pins that share the same voltage level in the same I/O bank
- ☐ Verify that all output signals in each I/O bank drive out at the I/O bank's V_{CCIO} voltage level
- ☐ Verify that all voltage-referenced signals in each I/O bank use the I/O bank's V_{REF} voltage level
- ☐ Check I/O bank support for LVDS features
- ☐ Use the dedicated DQ/DQS pins and DQ groups for memory interfaces
- ☐ Validate the pin assignments in the Quartus II software

For more information about user I/O pins, supported I/O standards, OCT, and other I/O features, refer to the *I/O Interface* chapter of the appropriate device handbook on the Literature and Technical Documentation web page.

For more information about using I/O pins for memory interfacing, refer to the following links:

- External Memory Solutions Center web page
- *External Memory Interfaces Handbook*
- External Memory Interfaces Design Examples web page

High-Speed Transceivers

High-speed transceiver pins are the multi-gigabit serial links used for implementing high-speed interfaces such as PCI Express, SATA, 10G Ethernet, XAUI, Serial RapidIO, and many others. Successful serial interface designs that use these pins require a good understanding of high-speed design techniques to minimize I/O jitter and maximize transceiver eye openings. For guidelines specific to transceiver design, refer to the transceiver section of the device handbook for your selected device.

For general board design guidelines related to high-speed transceivers, refer to the "Gigahertz Channel Design Considerations" section of the Board Design Resource Center web page.

For additional gigabit channel design guidelines, refer to the Gigabit Channel Design Guidelines web cast.

For a list of supported transceiver protocols by device family, refer to the Transceiver Protocols web page.

Power Supplies

Power supply pins provide power to the digital and analog blocks that comprise the core, I/O, PLLs, and transceivers. The analog PLL and transceiver's power rails are sensitive to noise and must be carefully isolated and decoupled to minimize noise impact on performance. Power rail isolation can be defined in both the PCB stackup design and the layout of the board. For more information about decoupling, refer to "Power Design and Decoupling".

PCB Stackup Design

In parallel with the schematic capture process, the PCB stackup design is usually specified by working closely with the PCB fabrication vendor. Most PCB vendors freely provide the detailed stackup design to fit the engineering requirements. A typical stackup usually specifies the PCB and dielectric material, the number of layers (signal, power, and ground), the ordering of the layers within the stackup, the trace geometry and impedance control requirements, the PCB board paneling to maximize boards per panel, and the finished board thickness. Having a final PCB stackup design early is useful for performing pre-layout signal integrity simulations that can be used to derive the layout design rules required for the PCB layout designers.

For more information about PCB stackup considerations, refer to the "PCB and Stackup Design Considerations" section on Altera's Board Design Resource Center web page.

Power Design and Decoupling

A challenging part of designing with FPGAs is the implementation of the power distribution and decoupling network. Because the power requirements of an FPGA can vary significantly depending on the FPGA design, the optimum decoupling depends on the actual current draw of each rail of the FPGA. The strategy for determining the optimum FPGA decoupling starts with an estimation of the device's power requirements and using the Frequency Domain Target Impedance Method (FDTIM) to realize the decoupling network for the device.

Use the Altera PowerPlay Early Power Estimator (EPE) tool and the PowerPlay Power Analyzer tool in the Quartus II software to obtain an accurate estimate of power throughout the FPGA design process.

Use the Altera Power Distribution Network (PDN) Design Tool to determine the decoupling requirements.

For more information about using the PDN tool and FDTIM methodology, refer to the following links:

- *Power Distribution Network Design for Stratix III and Stratix IV FPGAs (OPDN1100)* online training course
- "Power Distribution Network (PDN) Design" section on the Board Design Resource Center web page
- *AN 574: Printed Circuit Board (PCB) Power Delivery Network (PDN) Design Methodology*

Thermal Management

In addition to power estimation, the EPE tool also estimates die junction temperature (Tj) based on the expected system ambient temperature (Ta) and junction-to-ambient thermal resistance (θja). Using the EPE tool, you can determine the heat sink or airflow required to maintain the FPGA's junction temperature at safe operating conditions.

For more information about thermal management, refer to the "Power Dissipation and Thermal Management" section on the Board Design Resource Center web page.

Users of the Mentor Graphics® FloTHERM thermal modeling software tool can download FloTHERM device thermal models from the "Thermal Models" section on the Board Design Resource Center web page.

Pre-Layout Simulation

To verify the signal integrity of critical routes in the system, Altera provides complete IBIS and HSPICE I/O buffer models to allow system designers to perform hypothetical scenarios for the signal integrity simulations. This can be useful for determining termination requirements, crosstalk effects, length constraints, and other layout design rules for critical nets.

For a list of available IBIS and HSPICE I/O buffer models, refer to the following web pages:

- Altera IBIS Models
- SPICE Models for Altera Devices

Layout Design

The layout design is the process of translating the schematic design into the physical representation of the board. A common practice is to provide the layout designer with a detailed document that specifies all the physical requirements required for the board's layout. This document usually contains the detailed board dimensions, the stackup information with layer construction (which was done previously in collaboration with the PCB vendor), all necessary design rules derived from the pre-layout simulations to meet signal integrity, and any design rules that are necessary to meet board manufacturing requirements. When the layout designer has reviewed and understood these requirements, layout begins with the component symbol (or footprint) creation, detailed component placement, and design rule entry into the layout design tool.

To aid in the rules creation for the sensitive gigabit transceiver channel routing, Altera provides the following application notes:

- *AN 529: Via Optimization Techniques for High-Speed Channel Designs*
- *AN 530: Optimizing Impedance Discontinuity Caused by Surface Mount Pads for High-Speed Channel Designs*

For information about Altera's packaging information for device footprint creation, refer to the *Altera Device Package Information Data Sheet*.

Users of Cadence's Allegro PCB layout tool can download the premade Altera Allegro symbol libraries from the Cadence Capture CIS and Allegro PCB Symbols and Footprints web page.

Post-Layout Simulation

When the critical routes of the layout design have been completed, Altera recommends you perform a post-layout extraction and simulation on those critical nets to validate their expected signal integrity behavior. Similar to the pre-layout simulation already discussed, the post-layout simulation can use the device IBIS and HSPICE I/O buffer models along with the extracted layout S-parameter data to generate a simulation deck. When the post-layout simulation confirms proper signal integrity behavior, the layout can be finalized and released for final checking and generation of Gerber files for the PCB.

Conclusion

FPGAs are commonly used in complex system designs due to their high integration and flexibility. However, this flexibility can present unique challenges in the system design process. This application note provides an overview of the Altera FPGA design flow to help familiarize you with the Altera FPGA design process. Links to additional information are provided throughout the document to help you successfully design with Altera FPGA devices.

Document Revision History

Table 1 shows the revision history for this application note.

Table 1. Document Revision History

Date	Version	Changes Made
March 2010	1.1	Added link to Device Schematic Review Worksheets in "Schematic Design".
March 2010	1.0	Initial release.

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