Combining Multiple Configuration Schemes

AN-656-1.0 Application Note

This application note describes how to configure Altera® FPGAs using multiple configuration schemes on the same board.

Combining JTAG configuration with passive serial (PS) or active serial (AS) configuration on your board is useful in the prototyping environment because it allows multiple methods to configure your FPGA. For example, if your production environment calls for PS configuration using a configuration device, you must reprogram your configuration device every time you wanted to test a design change in your FPGA. If you include the FPGA in the same JTAG chain as the configuration device, the FPGA can be reconfigured using JTAG without having to reprogram the configuration device.

In this application note, the generic term "download cable" includes the Altera USB-Blaster™, EthernetBlaster II, EthernetBlaster, and ByteBlaster™ II download cables. The generic term "FPGA" includes Arria® series, Cyclone® series, and Stratix® series devices.

In this application note, the figures show the configuration interface connections only.

For more information about pull-up resistor values or other pins on the configuration devices, refer to the Configuration Devices page.

For more information about pull-up resistor values, V_{CC} values, or other pins on FPGA, refer to the configuration chapter in the appropriate device handbook.

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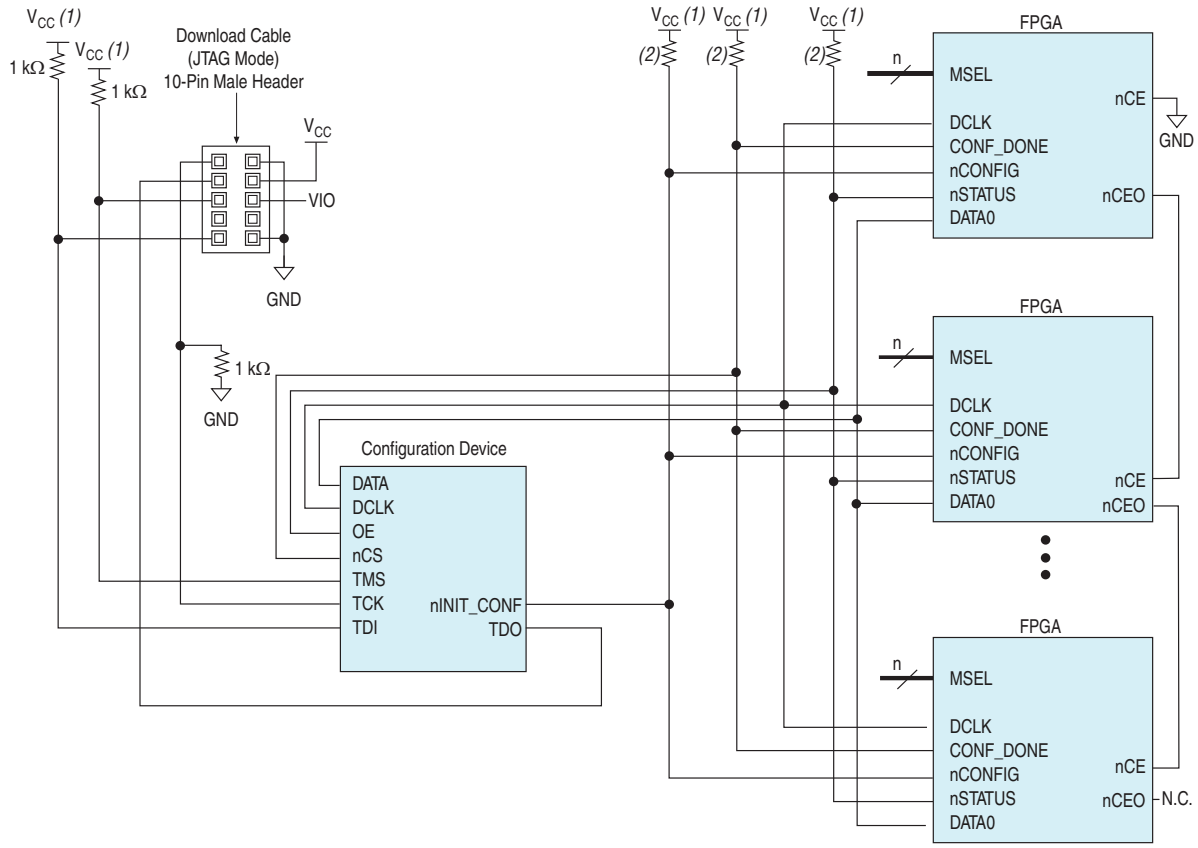
Passive Serial and JTAG

Figure 1 shows the configuration interface connections when you are using a download cable to JTAG program a configuration device and using the configuration device to configure the FPGAs. In Figure 1, multiple FPGAs are daisy-chained together and the MSEL pins should be set to select PS as the configuration mode.

Figure 1. JTAG Programming of a Configuration Device with PS Configuration of FPGA Using a Configuration Device



Notes to Figure 1:

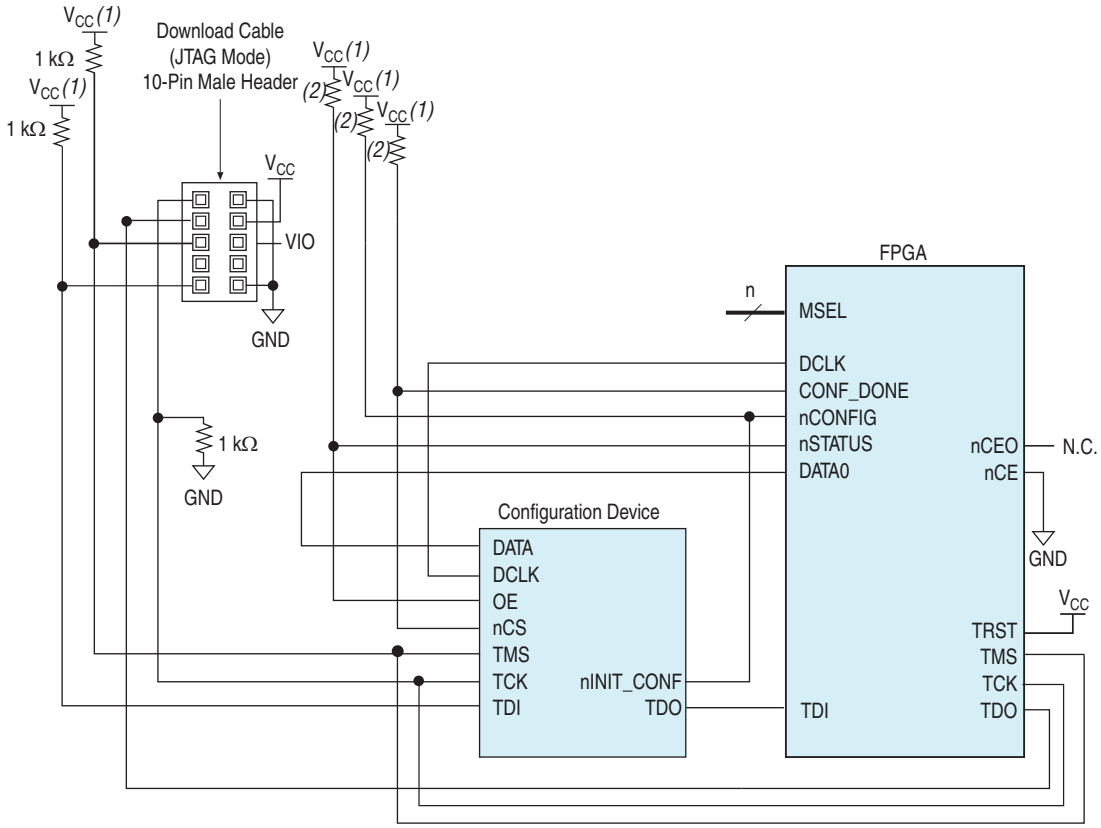
(1) Connect V_{CC} to the same supply voltage as the configuration device.

(2) If you use the internal pull-up resistors of the configuration device, do not use external pull-up resistors on these pins.

Figure 2 shows the configuration interface connections when the configuration device and the FPGA are in the same JTAG chain. Ensure the TDO signal drives out enough amount of high voltage to meet the next device's TDI minimum high-level input voltage (V_{IH}). The TDO output drives out the voltage of the I/O bank's V_{CCIO} where it resides. For example, if the TDO pin resides in an I/O bank whose V_{CCIO} is set to 3.3 V, the TDO pin drives out 3.3 V. The download cable is used to JTAG program the configuration device and the FPGA. The configuration device is used to configure the FPGA. Set the MSEL pins to select PS as the configuration mode.

If there is a configuration device on board, after power up, allow the FPGA to finish configuration before attempting JTAG configuration.

Figure 2. JTAG Programming of a Configuration Device and FPGA with PS Configuration of FPGA Using a Configuration Device



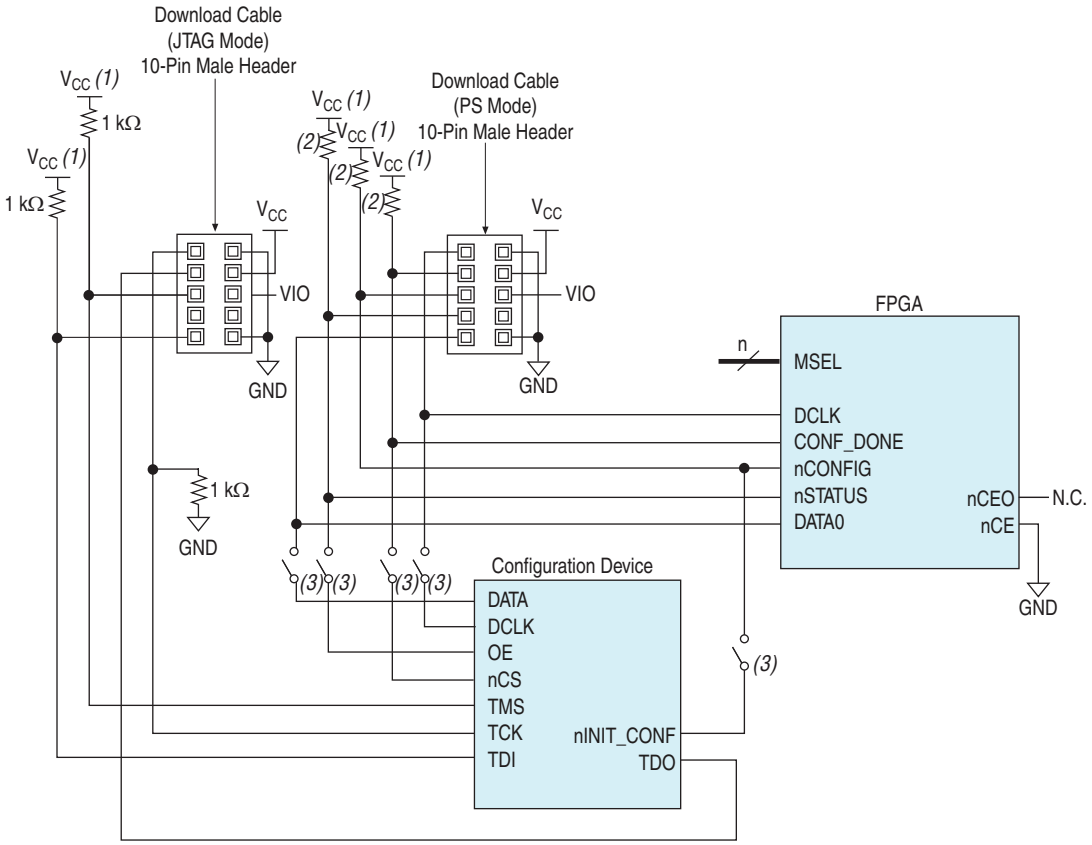
Notes to Figure 2:

(1) Connect V_{CC} to the same supply voltage as the configuration device.

(2) If you use the internal pull-up resistors of the configuration device, do not use external pull-up resistors on these pins.

You can use the download cables in different modes such as the JTAG mode or PS mode. In each mode, the header of the download cable connects to different pins on the FPGA. Therefore, two separate 10-pin headers are required on your board in order to support two different modes of the download cable. Figure 3 shows a schematic with two download cables. A download cable is used in JTAG mode to JTAG program the configuration device. The second download cable is used in PS mode to configure the FPGA using PS configuration. Set the MSEL pins to select PS as the configuration mode.

Figure 3. JTAG Programming of Configuration Device with PS Configuration of FPGA Using a Configuration Device and Download Cable



Notes to Figure 3:

(1) Connect V_{CC} to the same supply voltage as the configuration device.

(2) If you use the internal pull-up resistors of the configuration device, do not use external pull-up resistors on these pins.

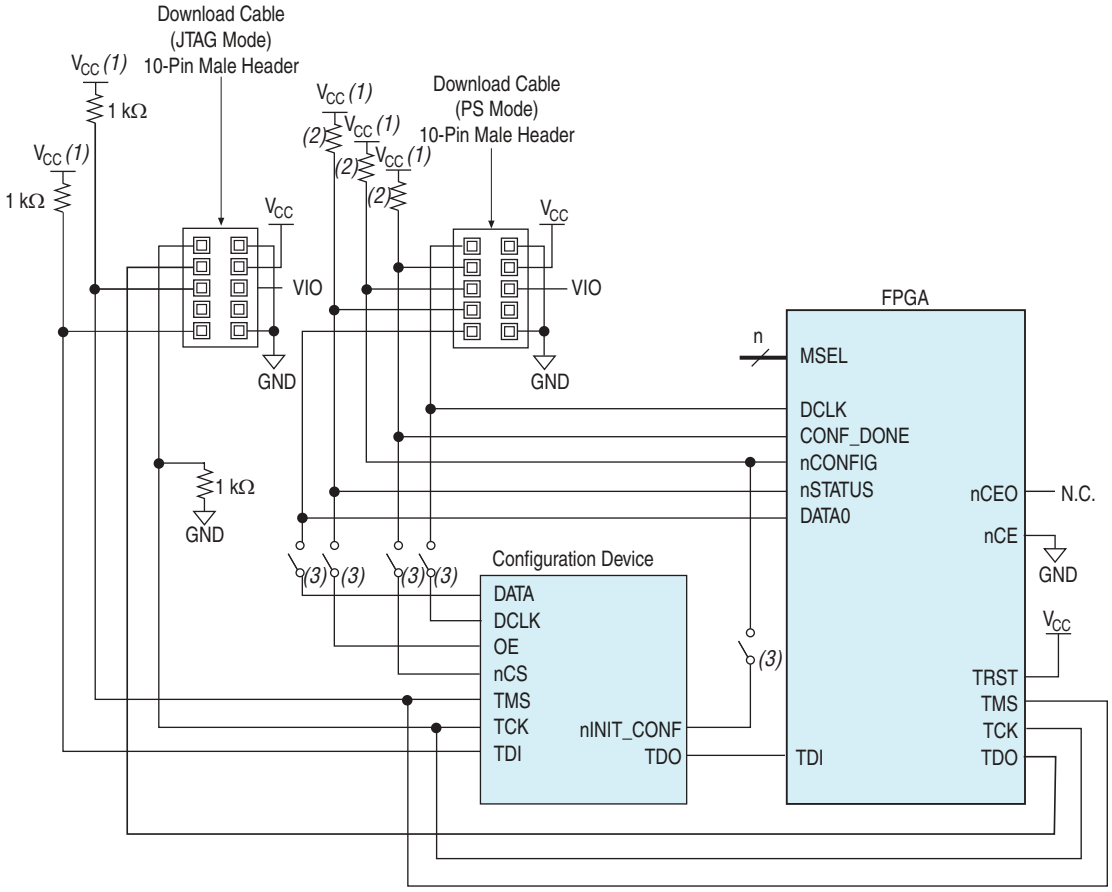
(3) To configure the FPGA with a download cable, you should either remove the configuration device from its socket or place a switch on the five common signals between the download cable and the configuration device.

You should not attempt PS configuration with a download cable while a configuration device is connected to an FPGA.

If you configure the FPGA using the download cable while the configuration device is connected to the FPGA, the low signals driven on the nSTATUS and CONF_DONE pins will pull the OE and nCS pins of the configuration device low. This will reset the configuration device and cause the configuration device to try to configure the FPGA.

Figure 4 shows a schematic that allows configuration of the FPGA with either a PS mode download cable or JTAG mode download cable. In addition, you can configure the FPGA using the configuration device. A download cable is used in JTAG mode to JTAG program the configuration device and FPGA. In Figure 4, the configuration device and FPGA are in the same JTAG chain. Ensure the TDO signal drives out enough amount of high voltage to meet the next device's TDI minimum V_{IH}. The TDO output drives out the voltage of the I/O bank's V_{CCIO} where it resides. The second download cable is used in PS mode to configure the FPGA using PS configuration. Set the MSEL pins to select PS as the configuration mode.

Figure 4. Combining JTAG Programming of Configuration Device and FPGA with PS Configuration of FPGA Using a Configuration Device and Download Cable



Notes to Figure 4:

(1) Connect V_{CC} to the same supply voltage as the configuration device.

(2) If you use the internal pull-up resistors of the configuration device, do not use external pull-up resistors on these pins.

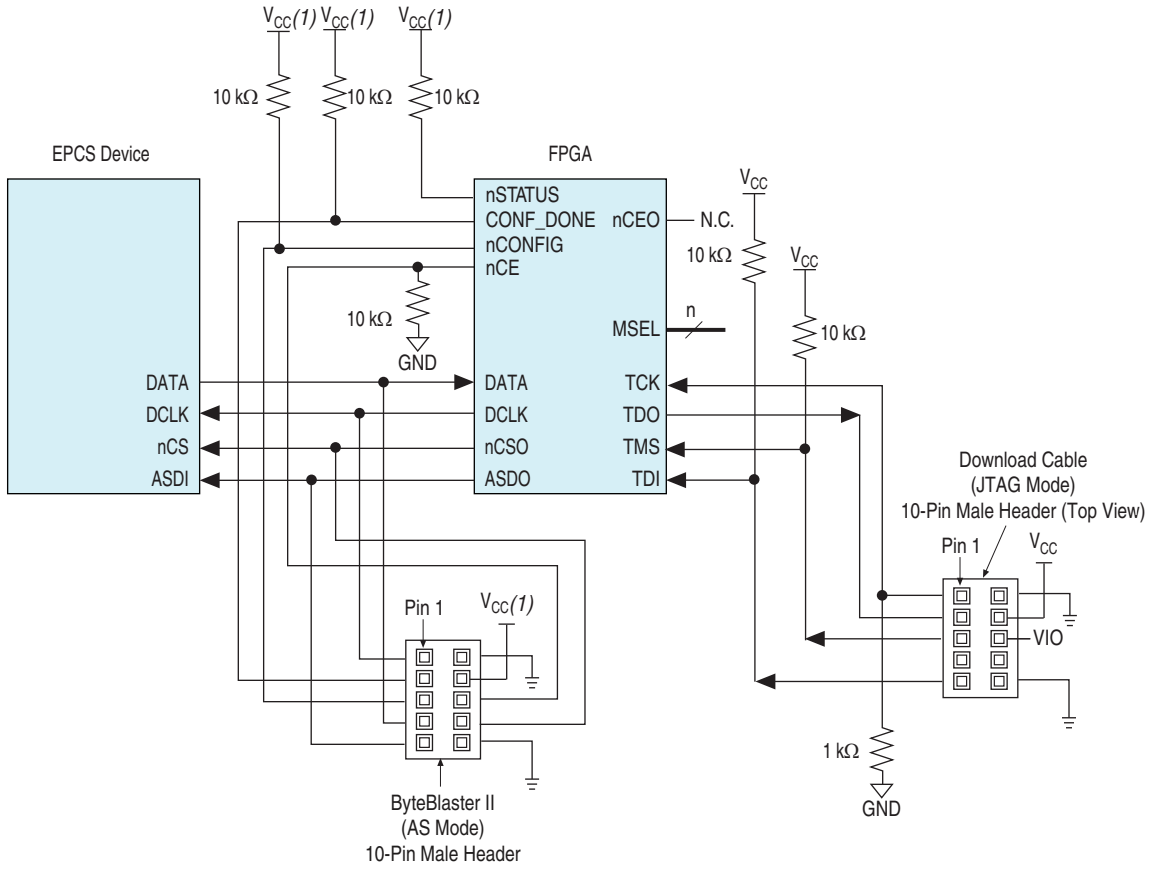
(3) To configure the FPGA with a download cable, you should either remove the configuration device from its socket or place a switch on the five common signals between the download cable and the configuration device.

You can use Figure 1 on page 2 and Figure 4 for fast passive parallel (FPP) mode with an exception—connect DATA[7..0] from the configuration device to the FPGAs that support FPP configuration. You must set the MSEL pins accordingly.

Active Serial and JTAG

For devices that support AS configuration, you can combine AS configuration with JTAG-based configuration (Figure 5). This setup uses two 10-pin download cable headers on the board. A download cable is used in JTAG mode to configure the FPGA directly using the JTAG interface. The second download cable is used in AS mode to program the serial configuration (EPCS) device in system using the AS programming interface. Set the MSEL pins to select AS as the configuration mode. If you configure the device using both schemes simultaneously, JTAG configuration takes precedence and terminates AS configuration.

Figure 5. Combining JTAG Programming of Configuration Device and FPGA with AS Configuration of FPGA Using a Configuration Device and Download Cable



Note to Figure 5:

(1) Connect V_{CC} to 3.3 V.

Document Revision History

Table 1 lists the revision history for this document.

Table 1. Document Revision History

Date	Version	Changes
January 2012	1.0	Initial release.