Using the Nios II Configuration Controller Reference Designs

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Introduction

This application note describes configuration controller reference designs for Nios® II systems using Altera® Stratix® II, Cyclone® II, and Cyclone III FPGAs. The note describes how to use the reference designs with four different Altera development boards, provides steps to port the reference designs to other boards, and offers suggestions for modifying the reference designs to support more complex systems.

A configuration controller helps accomplish the following tasks:

- Intelligently configure FPGAs from a flash memory device on system power-up
- Utilize a single flash memory device to store hardware configuration data as well as embedded software instructions and data
- Provide flash partitions for multiple hardware images
- Provide a mechanism for users to reset the board to a known working hardware image
- Facilitate in-the-field upgrades by responding to reconfiguration requests from a Nios II processor residing on the FPGA

Many modern embedded systems use flash memory to store processor configuration information and program data for the system processor. Systems also use flash memory to store FPGA hardware configuration data. The use of flash memory for both processor memory and FPGA configuration data typically requires an intelligent configuration controller, particularly for systems with soft embedded processors such as the Altera Nios II processor.

The Altera development boards running reference designs discussed in this application note contain a programmable configuration controller that provides a stable platform for managing system configuration and reset in embedded systems. The controller provides instant-on configuration control—enabling system configuration or reconfiguration in a minimal amount of time. Table 1 identifies the device where the configuration controller is implemented for each solution discussed in this application note.

Table 1. Configuration Controller Location

Board/Kit	Configuration Controller Device
Nios Development Board, Stratix II Edition	Altera EPM7256AE non-volatile MAX® 7000
Nios Development Board, Cyclone II Edition	Altera EPM7256AE non-volatile MAX 7000
Cyclone III FPGA Starter Board Nios II Embedded Evaluation Kit, Cyclone III Edition	Altera EP3C25 Cyclone III
Cyclone III 3C120 Development Board Altera Embedded System Development Kit, Cyclone III Edition	Altera EPM2210 non-volatile MAX II

For more information about the development boards referenced in this application note, refer to the following documents:

- *Nios Development Board Cyclone II Edition Reference Manual*
- *Nios Development Board Stratix II Edition Reference Manual*
- *Cyclone III FPGA Starter Board Reference Manual*
- *Cyclone III 3C120 Development Board Reference Manual*

For more information about the Nios II embedded processor, refer to the following documents:

- *Nios II Processor Reference Handbook*
- *Nios II Software Developer's Handbook*

Configuration Controller for Stratix II Devices

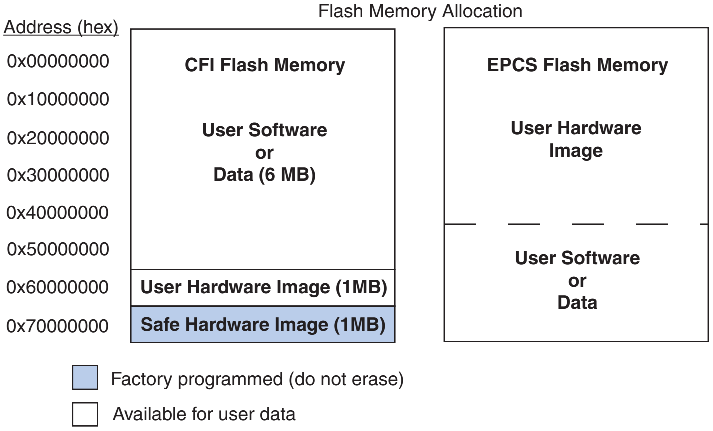
This section discusses the following configuration controller topics:

- "Flash Images on the Nios Development Board, Stratix II Edition" on page 2
- "Configuration Controller Boot Sequence for Stratix II Devices" on page 3
- "Configuration Controller Hardware for Stratix II Devices" on page 4
- "Configuration Controller Reference Designs for Stratix II Devices" on page 6

Flash Images on the Nios Development Board, Stratix II Edition

The Nios Development Board, Stratix II Edition includes an Altera EPCS64 serial configuration device as well as 8-bit wide Common Flash Interface (CFI) flash memory. The CFI flash memory on the board is partitioned into three sections (refer to Figure 1).

Figure 1. Nios Development Board Flash Partition



The first section is used for general programming or data storage. The other two sections—user and safe image—store FPGA hardware configurations. The user image typically contains a hardware design that is under development or testing. The safe (factory programmed) image typically contains a working, default hardware image.

The EPCS64 flash memory is divided into two sections with a floating section boundary. The section boundary between the user hardware and user software/data sections is determined by the size of the user hardware section.

The configuration controller loads the EPCS user, CFI user, or the CFI safe image into the Stratix II device. By observing the behavior illustrated in the Figure 2 flowchart, the configuration controller determines which image to load.

Configuration Controller Boot Sequence for Stratix II Devices

When the Nios Development Board, Stratix II Edition initially powers-on, the configuration controller is idle until it detects the power-on reset. Upon detecting power-on reset, the controller attempts to load the EPCS user image into the FPGA.

If configuration of the serial user flash image is successful, the controller continually blinks the User LED, tri-states all of its flash interface pins, and remains idle until a reset, reconfiguration, or safe image request is detected.

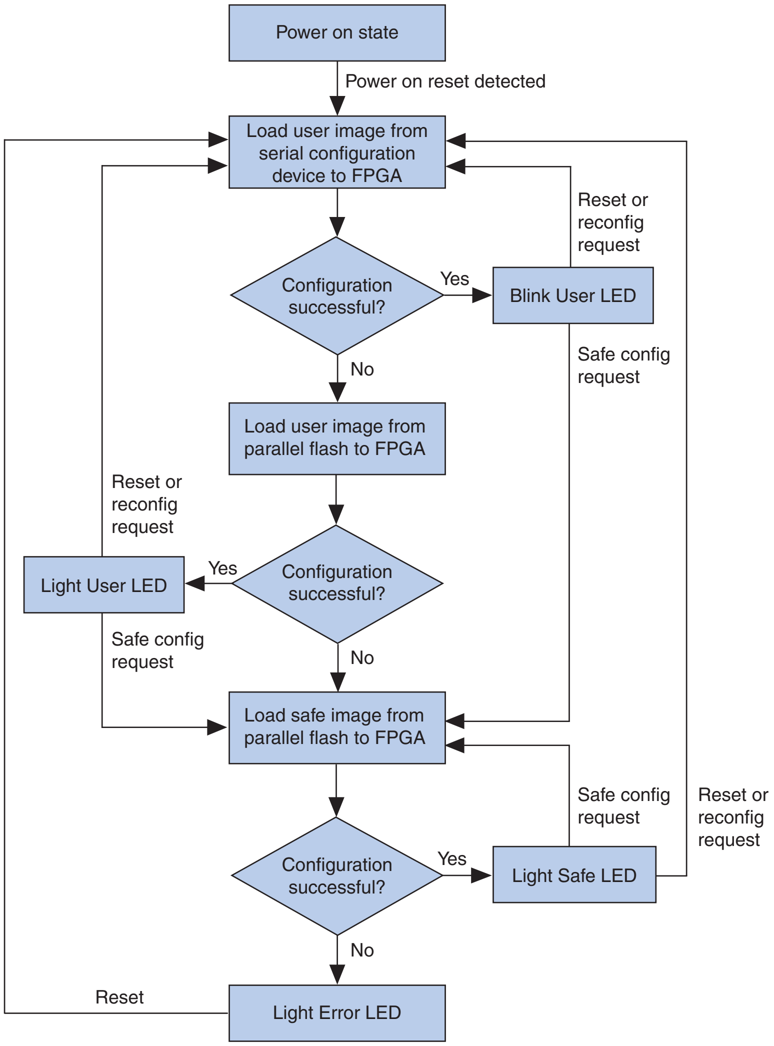
If configuration of the serial user flash image fails, the controller attempts to program the user image from the 8-bit parallel flash into the Stratix II device. If the controller successfully programs the user image into the Stratix II device, the User LED illuminates and the controller remains idle until a reset, reconfiguration request, or safe image reset is detected.

If configuration of the parallel user flash image fails, the controller attempts to program the safe image from the 8-bit flash into the Stratix II device. If the controller successfully programs the safe image into the Stratix II device, the Safe LED illuminates and the controller remains idle until a reset, reconfiguration, or safe image request is detected.

If an error occurs while programming the safe image to the device, the controller illuminates the Error LED and remains in an error state. The controller only exits the error state when a reset or power-on reset request is detected.

Figure 2 shows the configuration controller boot sequence for Stratix II and Cyclone II devices.

Figure 2. Stratix II and Cyclone II Configuration Controller Boot Sequence Flowchart


Power on state
Power on reset detected
Load user image from serial configuration device to FPGA
Reset or reconfig request
Configuration successful?
Yes
Blink User LED
No
Safe config request
Load user image from parallel flash to FPGA
Reset or reconfig request
Light User LED
Yes
Configuration successful?
Safe config request
No
Load safe image from parallel flash to FPGA
Safe config request
Reset or reconfig request
Configuration successful?
Yes
Light Safe LED
No
Reset
Light Error LED

For more information about the configuration process and the flash structure of the Nios Development Board, Stratix II Edition, refer to the *Nios Development Board Stratix II Edition Reference Manual*.

Configuration Controller Hardware for Stratix II Devices

You can program Stratix II FPGAs in a number of different modes; however, when programming a Stratix II device via an external configuration controller, Altera recommends programming the device in fast passive parallel (FPP) mode. When in FPP mode, the external configuration controller generates a configuration clock for the Stratix II device and presents an 8-bit configuration data word to the Stratix II device on each configuration clock cycle.

For more information about the FPP configuration capabilities of Stratix II devices, refer to the *Configuring Stratix II and Stratix II GX Devices* chapter of the *Stratix II Device Handbook*.

The configuration controller reference design included with the Nios II Embedded Design Suite (EDS) uses an EPM7256AE device to generate the configuration clock for the Stratix II device, as well as generate the address and control signals necessary to pull configuration data out of flash memory. Figure 3 shows a block diagram of the configuration controller reference design for Stratix II devices.

Figure 3. Development Board Configuration Controller for Stratix II Devices

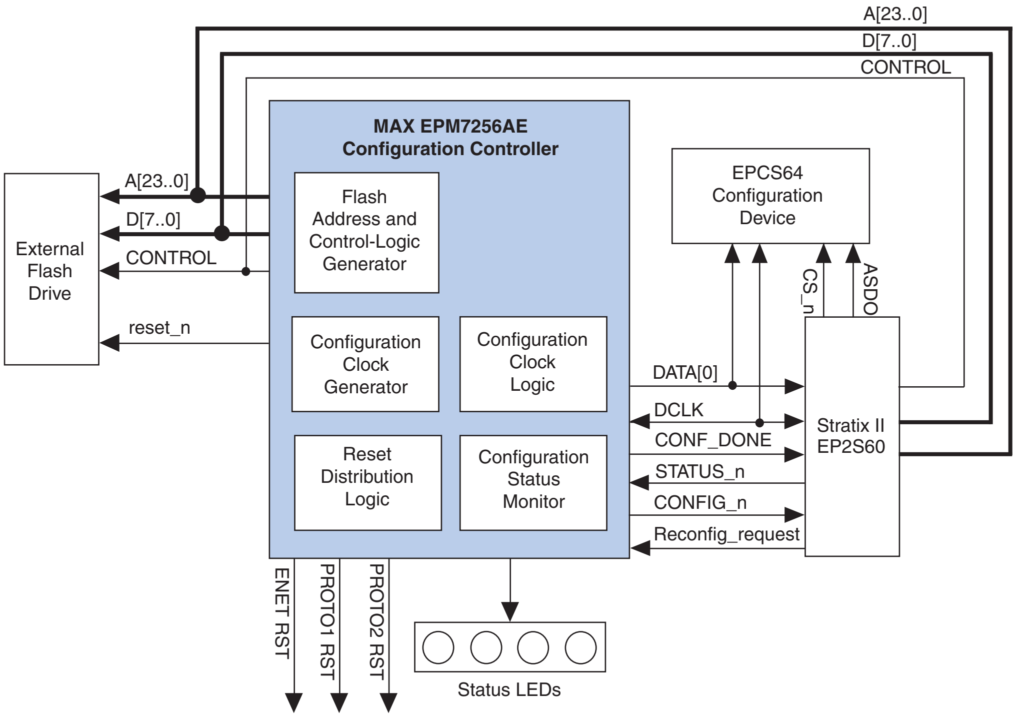


Figure 3 depicts the configuration controller as the five conceptual sub-blocks described in the following sections.

Flash Address and Control Logic Generator

The flash address and control logic block generates the address signals to send to the CFI flash device. The logic initiates configuration from either the user or factory image based on inputs from the control logic, and then increments the CFI flash address bus until the appropriate number of configuration bytes transfer, or an error is detected. After a successful configuration, the CFI flash address and control pins of the EPM7256AE device are tri-stated so that the flash can be accessed by the Nios II embedded processor running in the Stratix II device.

Configuration Clock Generator

The configuration clock generator drives the `DCLK` input signal of the Stratix II device. The clock is derived from the 50 MHz oscillator on the development board. The reference design divides the oscillator by 16 to create a 3.125MHz configuration clock. The clock is also used to time the address and control signals of the CFI flash device.

Reset Distribution Logic

The configuration controller also delivers reset signals to other devices on the development board. A board level reset is issued to the Ethernet device, the flash device, and the two board-prototype headers under the following conditions:

- A power-on reset occurs.
- A reconfiguration request from the processor arrives.
- The Force Safe button is pressed.

Configuration Control Logic

To control the configuration flow, the configuration control logic monitors the various board reset sources as well as the Stratix II device configuration status signals. This logic block drives the MSEL pins on the Stratix II device to set the configuration mode based on the flow chart shown in Figure 2 on page 4. The logic manages the loading of the user or factory images based on the status of the Stratix II devices `STATUS_n` and `CONF_DONE` signals. The configuration control logic initiates a new configuration if a `reset_n` is detected, the Force Safe button is pressed, or the Nios II processor residing in the Stratix II device issues a `Reconfiguration_request`.

Configuration Status Monitor

The Nios Development Board, Stratix II Edition contains four LEDs that indicate the configuration status of the processor. Different LEDs illuminate depending on which image is loaded into the Stratix II device or if an error occurs during configuration.

Configuration Controller Reference Designs for Stratix II Devices

The Nios II EDS provides a configuration controller reference design for the EP2S60 device. If you have installed the Nios II EDS, you can find the source code and Quartus® II project files for the reference design in the <*Nios II EDS install path*>**/examples/config_controller/niosII_stratixII_2s60_rohs** directory.

Table 2 provides a description of each of the source files used in the configuration controller design.

Table 2. Stratix II Configuration Controller Files

File Name	Description
config_controller.tdf	Top-level design. Contains control logic and instantiations of the lower-level files, namely, **address_counter.tdf**, **dclk_divider.tdf**, and **reset_counter.tdf**.
address_counter.tdf	Counter used to generate address bus for flash device access.
dclk_divider.tdf	Clock divider used to generate `DCLK` from the board oscillator.
reset_counter.tdf	Used to debounce reset switch inputs.

Configuration Controller for Cyclone II Devices

This section discusses the following configuration controller topics:

- "Flash Image on the Nios Development Board, Cyclone II Edition" on page 7
- "Configuration Controller Boot Sequence for Cyclone II Devices" on page 7

- "Configuration Controller Hardware for Cyclone II Devices" on page 7
- "Configuration Controller Reference Designs for Cyclone II Devices" on page 8

Flash Image on the Nios Development Board, Cyclone II Edition

The flash image on the Nios Development Board, Cyclone II Edition also contains a user and safe (factory programmed) image in CFI flash, as well as a user hardware image in an EPCS64 serial configuration device.

Configuration Controller Boot Sequence for Cyclone II Devices

When the Nios Development Board, Cyclone II Edition initially powers-on, the configuration controller is idle until it detects the power-on reset. Upon detecting power-on reset, the controller attempts to load the EPCS user image into the FPGA.

If configuration of the serial user flash image is successful, the controller continuously blinks the User LED, tri-states all of its flash interface pins, and remains idle until a reset, reconfiguration, or safe image request is detected.

If configuration of the serial user flash image fails, the controller attempts to program the user image from the 8-bit parallel flash into the Cyclone II device. If the controller successfully programs the user image into the Cyclone II device, the User LED illuminates and the controller remains idle until a reset, reconfiguration request, or safe image reset is detected.

If configuration of the parallel user image fails, the controller attempts to program the safe image from the 8-bit flash into the Cyclone II device. If the controller successfully programs the safe image into the Stratix II device, the Safe LED illuminates and the controller remains idle until a reset, reconfiguration, or safe image request is detected.

If an error occurs while programming the safe image to the device, the controller illuminates the Error LED and remains in an error state. The controller only exits the error state when a reset or power-on reset is detected.

Figure 2 on page 4 shows the configuration controller boot sequence for Stratix II and Cyclone II devices.

For more information about the configuration process and the flash structure of the Nios Development Board, Cyclone II Edition, refer to the *Nios Development Board Cyclone II Edition Reference Manual*.

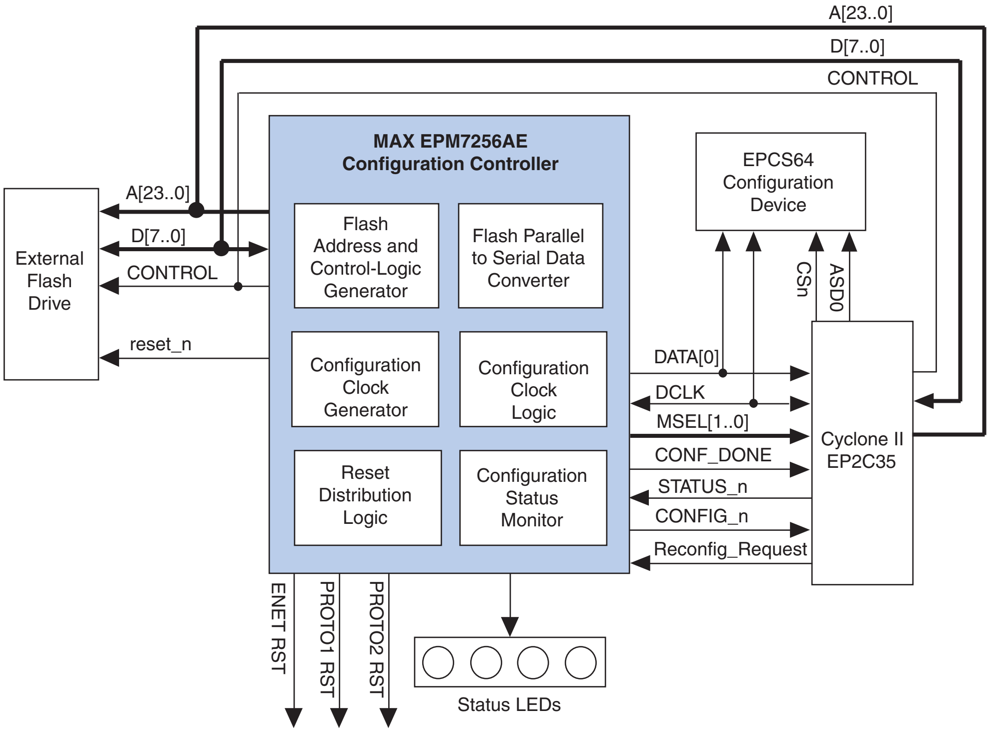
Configuration Controller Hardware for Cyclone II Devices

You program Cyclone II FPGAs serially via either a download cable, a serial configuration device, or in passive serial (PS) mode using an external configuration controller. The configuration controller reference design demonstrates the flexibility of using a single CPLD as a configuration controller for two different Altera device families. In the case of the Nios Development Board, Cyclone II Edition, the configuration controller has been modified to enable programming the Cyclone II device in PS mode using an 8-bit flash as the configuration source as well as from an Altera serial configuration device.

For more information about the configuration capabilities of Cyclone II devices, refer to the *Configuring Cyclone II Devices* chapter of the *Cyclone II Device Handbook*.

The configuration controller reference design included with the Nios Development Board, Cyclone II Edition uses a MAX 7256AE device to generate the configuration clock for the Cyclone II device as well as generate the address and control signals necessary to pull configuration data out of flash memory and convert it to serial data for the Cyclone II device. Figure 4 shows a block diagram of the configuration controller reference design for Cyclone II devices.

Figure 4. Development Board Configuration Controller for Cyclone II Devices


A[23..0]
D[7..0]
CONTROL
MAX EPM7256AE Configuration Controller
Flash Address and Control-Logic Generator
Flash Parallel to Serial Data Converter
Configuration Clock Generator
Configuration Clock Logic
Reset Distribution Logic
Configuration Status Monitor
EPCS64 Configuration Device
External Flash Drive
A[23..0]
D[7..0]
CONTROL
reset_n
CSn
ASD0
DATA[0]
DCLK
MSEL[1..0]
CONF_DONE
STATUS_n
CONFIG_n
Reconfig_Request
Cyclone II EP2C35
ENET RST
PROTO1 RST
PROTO2 RST
Status LEDs

The main differences between the Cyclone II edition and Stratix II edition development board's configuration controllers are that the Cyclone II edition includes a parallel to serial converter block and control logic block modifications. The parallel to serial block reads an 8-bit word from the flash image every 8 `DCLK` cycles and shifts the word out to the `DATA0` input of the Cyclone II device on every `DCLK` cycle.

Configuration Controller Reference Designs for Cyclone II Devices

The Nios II EDS provides a configuration controller reference design for the Cyclone II EP2C35 device. If you have installed the Nios II EDS, you can find the source code and Quartus II project files for the reference designs in the <*Nios II EDS install path*>**/examples/config_controller/niosII_cycloneII_2c35** directory.

Table 3 provides a description of each of the source files used in the configuration controller design.

Table 3. Cyclone II Configuration Controller Files

File Name	Description
config_controller.tdf	Top-level design. Contains control logic and instantiations of the lower-level files, namely, **address_counter.tdf**, **dclk_divider.tdf**, **reset_counter.tdf**, **data_bit_counter.tdf**, **shift_register.tdf**.
address_counter.tdf	Counter used to generate address bus for flash access.
dclk_divider.tdf	Clock divider used to generate `DCLK` from the board oscillator.
reset_counter.tdf	Used to debounce reset switch inputs.
data_bit_counter.tdf	Used to determine when a word should be loaded into the shift register.
shift_register.tdf	Shifts a configuration bit out to the `DATA0` line each `DCLK` cycle.

Configuration Controller for Cyclone III Devices

This section discusses the following configuration controller topics:

- "Flash Image on the Nios II Embedded Evaluation Kit, Cyclone III Edition" on page 9
- "Configuration Controller Hardware for the Nios II Embedded Evaluation Kit, Cyclone III Edition" on page 10
- "Configuration Controller Boot Sequence for the Nios II Embedded Evaluation Kit, Cyclone III Edition" on page 10
- "Flash Image on the Altera Embedded Systems Development Kit, Cyclone III Edition" on page 11
- "Configuration Controller Hardware for the Altera Embedded Systems Development Kit, Cyclone III Edition" on page 12
- "MAX II Register Interface on the Altera Embedded Systems Development Kit, Cyclone III Edition" on page 13
- "Configuration Controller Boot Sequence for the Altera Embedded Systems Development Kit, Cyclone III Edition" on page 16

Flash Image on the Nios II Embedded Evaluation Kit, Cyclone III Edition

The flash image on the Nios II Embedded Evaluation Kit, Cyclone III Edition contains one factory-programmed image in CFI flash memory. The factory image is the application selector utility. Use the application selector utility to load user designs into CFI flash memory.

Configuration Controller Hardware for the Nios II Embedded Evaluation Kit, Cyclone III Edition

The configuration controller on the Nios II Embedded Evaluation Kit, Cyclone III Edition board is not a separate chip; it resides in the Cyclone III device. You can configure the Cyclone III FPGA using either a serial or parallel interface. Configure the Cyclone_III FPGA serially via a download cable, a serial configuration device, or an external configuration controller. Configure the Cyclone_III FPGA over a parallel interface either passively via an external controller, or actively by reading from a parallel flash memory device. The Nios II Embedded Evaluation Kit, Cyclone III Edition uses the active parallel (AP) configuration method.

The Cyclone III device contains a hard-coded remote update block that allows logic in the FPGA to control reconfiguration. The application selector utility uses this block to reconfigure the FPGA with user designs.

For more information about the remote update block, refer to the *Remote Update Circuitry Megafunction User Guide* and the *Cyclone III Remote Update Controller Core* chapter in volume 5 of the *Quartus II Handbook*.

For more information about the configuration capabilities of Cyclone III devices, refer to the *Configuring Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

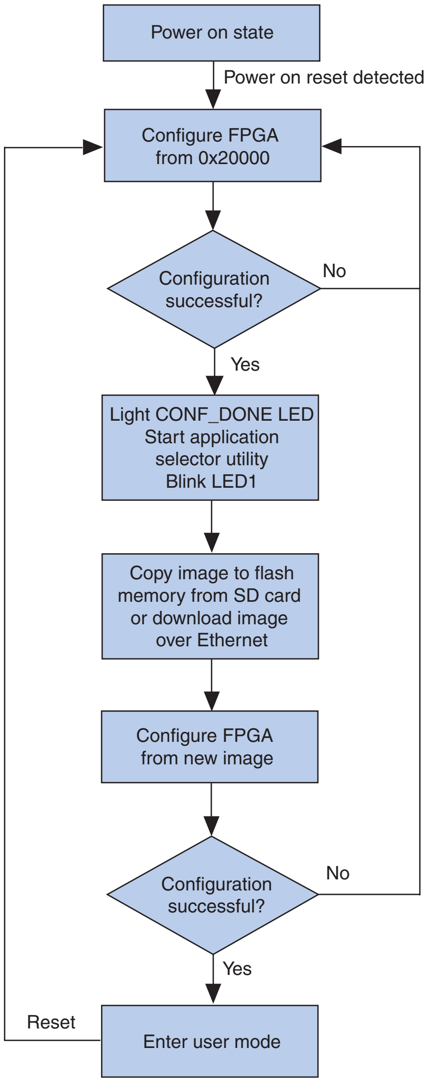
Configuration Controller Boot Sequence for the Nios II Embedded Evaluation Kit, Cyclone III Edition

When the Nios II Embedded Evaluation Kit, Cyclone III Edition initially powers on, the configuration controller attempts to configure the Cyclone III FPGA from the CFI flash memory starting at offset 0x20000. Offset 0x20000 is the location of the application selector utility factory image. If configuration is successful, the controller illuminates the CONF_DONE LED. After the application selector utility starts up, LED1 blinks continuously.

Once the application selector utility boots, you can load a user image using either the GUI displayed on the touch screen LCD, or over Ethernet by connecting to the board's web server with a web browser.

Figure 5 shows the configuration controller boot sequence flowchart for the Nios II Embedded Evaluation Kit, Cyclone III Edition.

Figure 5. Nios II Embedded Evaluation Kit, Cyclone III Edition Configuration Controller Boot Sequence Flowchart


Power on state
Power on reset detected
Configure FPGA from 0x20000
Configuration successful?
No
Yes
Light CONF_DONE LED Start application selector utility Blink LED1
Copy image to flash memory from SD card or download image over Ethernet
Configure FPGA from new image
Configuration successful?
No
Yes
Reset
Enter user mode

For more information about the configuration process, the application selector utility, and the flash structure of Nios II Embedded Evaluation Kit, Cyclone III Edition, refer to the *Nios II Embedded Evaluation Kit, Cyclone III Edition User Guide*.

Flash Image on the Altera Embedded Systems Development Kit, Cyclone III Edition

The flash image on the Altera Embedded Systems Development Kit, Cyclone III Edition contains one factory-programmed image in CFI flash memory. The factory image is the application selector utility. Use the application selector utility to load user designs into CFI flash memory.

Configuration Controller Hardware for the Altera Embedded Systems Development Kit, Cyclone III Edition

You can configure the Cyclone III FPGA using either a serial or parallel interface. Configure the Cyclone_III FPGA serially via a download cable, a serial configuration device, or an external configuration controller. Configure the Cyclone_III FPGA over a parallel interface either passively via an external controller, or actively by reading from a parallel flash memory device. The Altera Embedded Systems Development Kit, Cyclone III Edition uses the passive serial (PS) configuration method in combination with a configuration controller that reads configuration data from a parallel flash device, then serializes the data in the PS format.

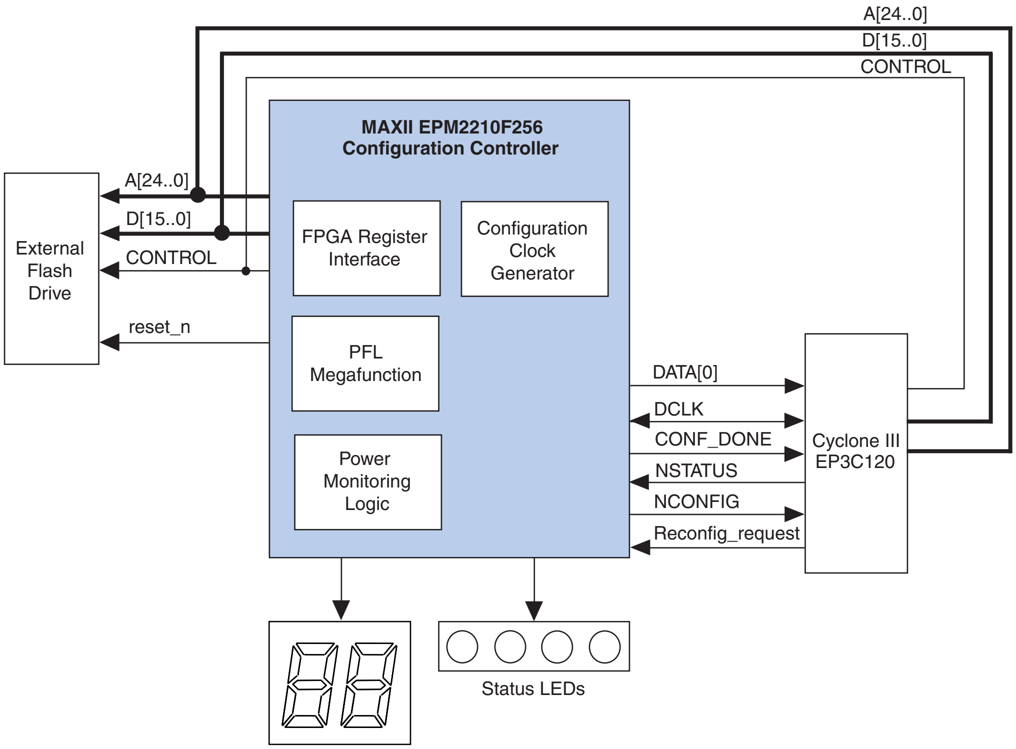
For more information about the configuration capabilities of Cyclone III devices, refer to the *Configuring Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

The configuration controller reference design included with the Altera Embedded Systems Development Kit, Cyclone III Edition, uses a MAXII EPM2210F256 device to generate the configuration clock for the Cyclone III device as well as generate the address and control signals necessary to pull configuration data out of flash memory and convert it to serial data for the Cyclone III device.

☞ Switch bank SW1 switch 5 (SW1.5), labeled MAX0, must be in the open (1) position to enable FPGA configuration from flash memory using the configuration controller. Putting SW1.5 in the closed (0) position disables the configuration controller in the MAXII CPLD.

Figure 6 shows a block diagram of the configuration controller reference design for the Altera Embedded Systems Development Kit, Cyclone III Edition.

Figure 6. Development Board Configuration Controller for the Altera Embedded Systems Development Kit, Cyclone III Edition



The configuration controller for the Cyclone III edition differs considerably from the Cyclone II and Stratix II configuration controllers. The Cyclone III configuration controller uses the Parallel Flash Loader (PFL) megafunction to manage the configuration process.

For more information about the PFL megafunction, refer to *AN 386: Using the MAX II Parallel Flash Loader with the Quartus II Software*.

In addition to the PFL megafunction, the Cyclone III configuration controller contains a register interface that allows external logic to control the configuration process. In the Altera Embedded Systems Development Kit, Cyclone III Edition, the Nios II processor in the factory image is connected to the configuration controller's register interface, which allows the Nios II to control FPGA reconfiguration.

MAX II Register Interface on the Altera Embedded Systems Development Kit, Cyclone III Edition

The register map for the MAX II interface contains four 32-bit registers. There are no byte enables for writing, so treat all accesses as 32-bit DWORD transactions. Table 4 shows the register names and default reset values for the register map.

Table 4. MAX II Register Map

DWORD	Register Name	Default Reset Value
0x0	IDR1	0x1338BEEF
0x4	Regfile 1	0x00000000
0x8	Regfile 2	0x0E787FC0
0xC	IDR2	0xDEADBEEF

Press the CPU_RESET button or either configuration button to restore the default reset values.

For configuration, the only register of interest is the Regfile 2 register. Regfile 2 is a 32-bit register serving many purposes in a single 32-bit DWORD. Regfile 2 is typically accessed as a read/modify/write function when writing a bit or number of bits. Table 5 and the following paragraphs show the field names and descriptions for the Regfile 2 register.

Table 5. Regfile 2 Register Description

	31 … 25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Reserved	OMR	RSO	RSR				RSS				DSO	DAW	OCRE	E125	E50	PSO	PSR			PSS			SRST	URST	MRST
Read / Write	R	RW	RW	RW				R				RW	RW	RW	RW	RW	RW	RW			R			W	W	W
Reset Value	0000111	0	0	1111				SW4				1	1	1	1	1	1	111			SW5			-	-	-

MRST—MAX Reset (bit 0)

The MRST field is only local to the MAX II CPLD internals. This field is write-only. Writing a zero causes a short reset pulse to occur. You cannot hold the device in reset via software control. Writing a one to the MRST field has no effect.

URST—User Reset (bit 1)

The URST field resets the MAX II CPLD and the Cyclone III FPGA with board net CPU_RESET. This field is write-only. Writing a zero causes a short reset pulse to occur. This pulse drives the MAX reset and the board reset low. You cannot hold the device in reset via software control. If the FPGA uses CPU_RESET as a reset input, the device's logic resets as well. Writing a one to the URST field has no effect.

SRST—System Reset (bit 2)

The SRST field resets the MAX II CPLD and reloads the Cyclone III FPGA with configuration data. This field is write-only.

PSS—Page Select Switch (bits 5:3)

The PSS field shows the current position of the PGM CONFIG SELECT rotary switch (SW5). This field is read-only. When PSO = 1, the PSS field value determines the image to load from flash memory into the FPGA.

PSR—Page Select Register (bits 8:6)

When PSO = 0, the PSR field value determines the image to load from flash memory into the FPGA. This field is readable and writable.

PSO—Page Select Software Override (bit 9)

The PSO field indicates the field to use to determine the image to load into the FPGA. When PSO = 0, the PSR field determines the image to load. When PSO = 1, the PSS field determines the image to load.

E50—50 MHz Oscillator Enable (bit 10)

The E50 field controls the 50-MHz oscillator that drives to the FPGA. This field is readable and writable. A zero disables the oscillator. A one enables the oscillator. You must write the OCRE bit low before the E50 field actively drives the oscillator's enable pin. Do not disable the oscillator used in the Nios II design responsible for interfacing to the MAX II CPLD.

E125—125 MHz Oscillator Enable (bit 11)

The E125 field controls the 125-MHz oscillator that drives to the FPGA. This field is readable and writable. A zero disables the oscillator. A one enables the oscillator. You must write the OCRE bit low before the E125 field actively drives the oscillator's enable pin. Do not disable the oscillator used in the Nios II design responsible for interfacing to the MAX II CPLD.

OCRE—Oscillator Control Register Enable (bit 12)

The OCRE field gates usage of the E50 and E125 fields. A zero enables the E50 and E125 field values to drive the oscillator's enable pin. A one drives both oscillator enable pins regardless of the E50 and E125 field values.

DAW—Display Amps/Watts (bit 13)

When DSO = 0, the DAW field controls the power display format. A zero displays power in mW. A one displays current in mA. When DSO = 1, the DAW field has no effect.

DSO—Display Select Software Override (bit 14)

The DSO field gates usage of the DAW field. When DSO = 1, the display mode is chosen through DIP switch SW1.1, which is the default behavior. When DSO = 0, the switch has no effect; the DAW field controls the display.

RSS—Rotary Select Switch (bits 18:15)

The RSS field shows the current position of the POWER SELECT rotary switch (SW4). This field is read-only. When RSO = 1, the RSS field value determines which power rail the MAX II CPLD's power monitoring function monitors.

RSR—Rotary Switch Register (bits 22:19)

When RSO = 0, the RSR field value determines which power rail the MAX II CPLD's power monitoring function monitors. This field is readable and writable.

RSO—Rotary Switch Software Override (bit 23)

The RSO field indicates the field to use to determine the power rail to monitor. When RSO = 0, the RSR field determines the power rail to monitor. When RSO = 1, the RSS field determines the power rail to monitor.

OMR—Graphics Display Mode (bit 24)

The OMR field determines whether the graphics LCD is in 8080 mode or 68000 mode. A zero selects 8080 mode. A one selects 68000 mode.

Configuration Controller Boot Sequence for the Altera Embedded Systems Development Kit, Cyclone III Edition

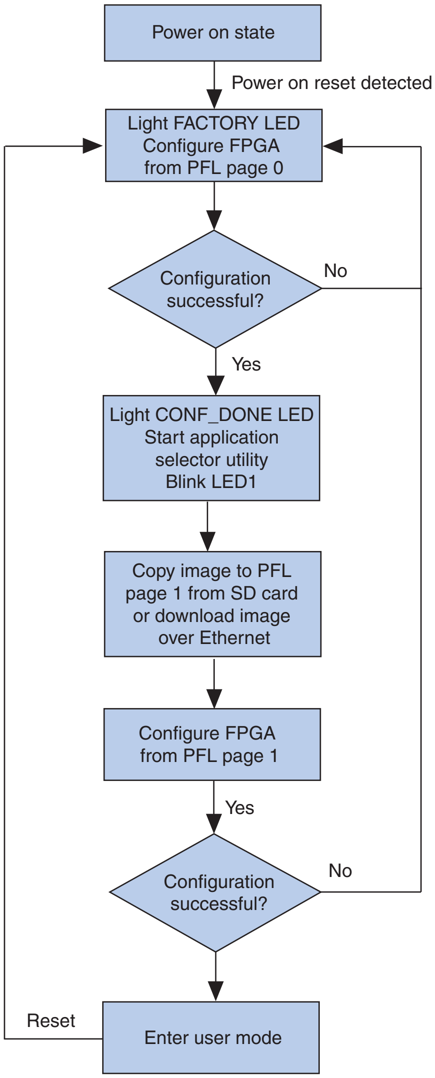
When the Altera Embedded Systems Development Kit, Cyclone III Edition board initially powers-on, the configuration controller is idle until it detects the power-on reset. Upon detecting power-on reset, the controller attempts to configure the FPGA from the image located at page 0. Page 0 contains the application selector utility factory image. The illumination of the FACTORY LED indicates that the factory image is configuring the FPGA.

If configuration is successful, the controller illuminates the CONF_DONE LED. After the application selector utility starts up, LED1 blinks continuously.

Once the application selector utility boots, load a user image using either the GUI displayed on the touch screen LCD, or over Ethernet by connecting to the board's web server with a web browser. After the user image is loaded into flash memory, the application selector utility uses the register interface attached to the PFL megafunction in the configuration controller to force the controller to reconfigure the Cyclone III FPGA with the new image.

Figure 7 shows the configuration controller boot sequence flowchart for the Altera Embedded Systems Development Kit, Cyclone III Edition.

Figure 7. Altera Embedded Systems Development Kit, Cyclone III Edition Configuration Controller Boot Sequence Flowchart



For more information about the configuration process, the application selector utility and the flash structure of Altera Embedded Systems Development Kit, Cyclone III Edition, refer to the *Altera Embedded Systems Development Kit, Cyclone III Edition User Guide* that comes on the *Altera Embedded Systems Development Kit, Cyclone III Edition CD* available on the Altera Embedded Systems Development Kit, Cyclone III Edition page of the Altera website.

For information about the configuration and JTAG-related board switch settings, refer to the *Cyclone III 3C120 Development Board Reference Manual*.

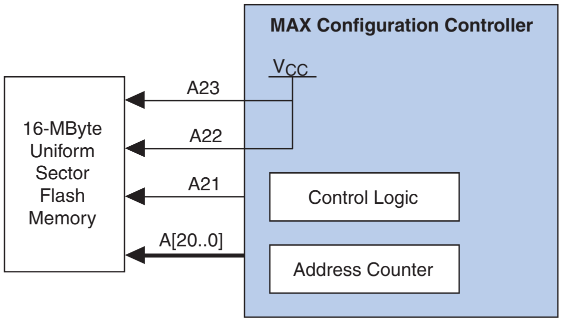
Porting the Configuration Controller Reference Designs to Other Boards

You can easily adapt the configuration controller reference design included with Nios II development kits to work on other boards that contain a CPLD and an Altera FPGA. In general, the only required modification is to match the Nios development board configuration controller to the type of flash image present on your board.

The flash image contained on the Nios development board is an 8-bit-wide, 16-MByte flash image, which requires 24 address lines. Other size flashes may require a different number of address bits. In this case, you need to modify the configuration controller source code such that the address bus width matches the address width of your flash.

If you are using a different size flash, you also need to modify the location of the user and safe images within the configuration controller. The configuration controller for the Stratix II development board wires the upper two address bits (namely, bits 23 and 22) to the 16-MByte flash and to 1 (or V_{CC}), and uses address bit 21 to select between the user and safe images. Figure 8 shows the 16-MByte flash connection.

Figure 8. 8-Bit Wide, 16-MByte Uniform Sector Flash Connection

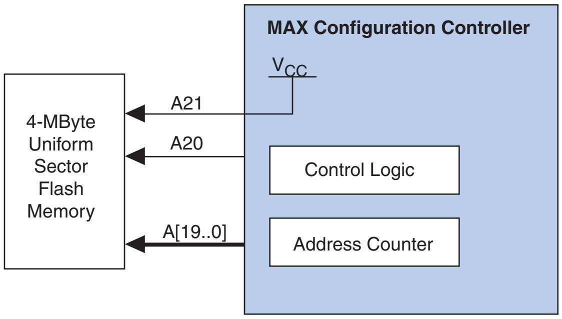

MAX Configuration Controller
VCC
A23
A22
A21
A[20..0]
16-MByte Uniform Sector Flash Memory
Control Logic
Address Counter

Note to Figure 8:

(1) This figure assumes that the configuration target is an EP2C35 device. Other size devices may have different configuration file sizes requiring different address mapping.

If you are using a 4-MByte flash, change the address bus width from [23..0] to [21..0] and wire address bit 21 of the configuration controller address bus to 1 (or V_{CC}); then continue to use bit 20 to select between the user and safe image. Figure 9 shows the 4-MByte flash connection.

Figure 9. 8-Bit Wide, 4-MByte Uniform Sector Flash Connection

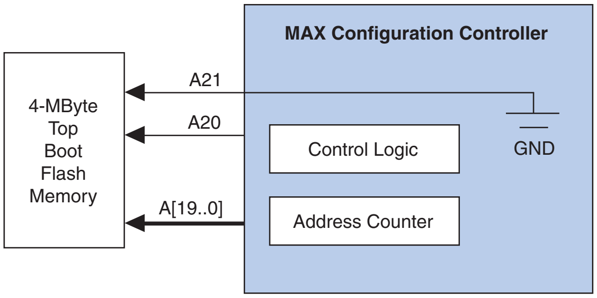

MAX Configuration Controller
V_{CC}
4-MByte Uniform Sector Flash Memory
A21
A20
A[19..0]
Control Logic
Address Counter

Note to Figure 9:

(1) This figure assumes that the configuration target is an EP2C35 device. Other size devices may have different configuration file sizes requiring different address mapping.

If you are using a top boot sector flash, you also need to make modifications to the source code. The flash used in the Nios II development kits is a uniform sector flash; therefore, it is generally advisable to leave the lower sections of a uniform sector flash for the host processor and the upper sections for data storage. However, a top boot sector flash generally reserves the upper sections as processor boot code. In this case, it is better to store the hardware configuration data in a lower section of the flash. This type of flash requires that the upper address bit (bit 21) of the flash is tied to 0 (or GND), and bit 20 is used to select the user or safe image. Figure 10 shows the top boot sector flash connection.

Figure 10. 8-Bit-Wide, 4-MByte Top Boot Sector Flash Connection



Note to Figure 10:

(1) This figure assumes that the configuration target is an EP2C35 device. Other size devices may have different configuration file sizes requiring different address mapping.

Modifying the Reference Design to Support a Variety of System and Configuration Requirements

In addition to accommodating different flash types, you can modify the configuration controller reference design to support many different types of systems and configuration requirements. For example, you can use a MAX device to create configuration controllers that can perform the following tasks:

- "Selecting from Multiple Flash Images" on page 20
- "Upgrading Hardware Images via an Ethernet Link" on page 21

- "Configuring Multiple Devices" on page 21

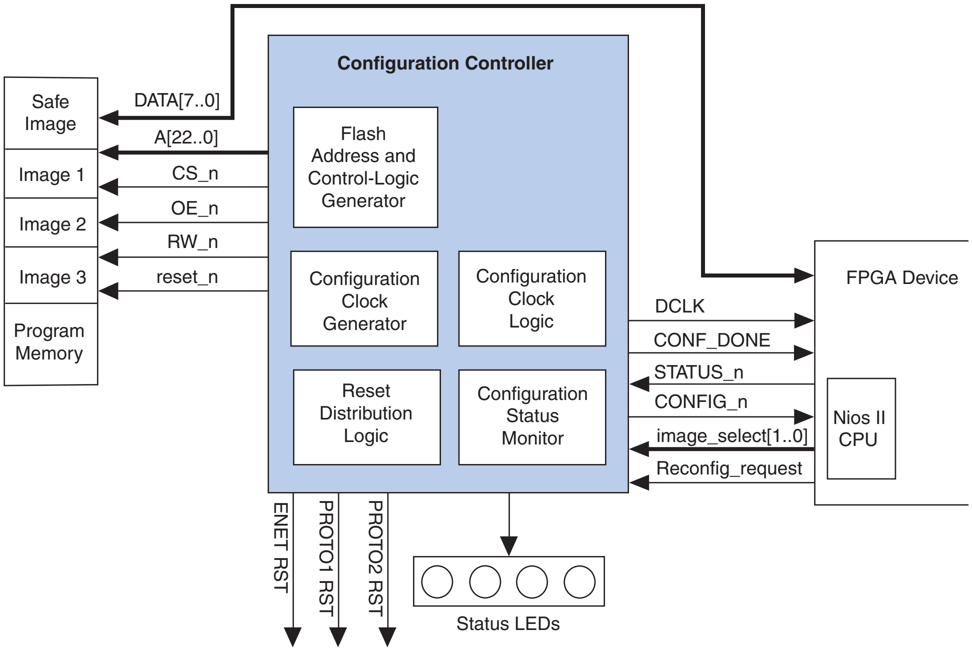
Selecting from Multiple Flash Images

The configuration controller reference designs that ship with Altera development kits are designed to first attempt to program the user image into the targeted FPGA. If the user image configuration attempt fails, the reference design attempts to program the safe image.

The concept of a priority image-selection design can easily be extended to include a number of user images to chose from to program the FPGA. Figure 11 shows an example configuration controller that offers priority image selection. The Figure 11 controller design is virtually identical to the Figure 3 controller design. However, the Figure 11 controller has a 2-bit `image_select[1..0]` bus used to select one of four user images stored in flash memory. The 2-bit `image_select[1..0]` bus is driven by an external source—such as a Nios II embedded processor—running in the target device. To load a new image into the target device, the Nios II processor (or external source) writes out the desired configuration image number to the `image_select[1..0]` bus and issues a reconfiguration request.

An alternative solution is to reserve a flash memory location that contains a hardware image number. In this scenario, the processor writes to the desired flash configuration number. When a reset or reconfiguration request occurs, the configuration controller reads the image number location from flash and proceeds to load the indicated image into the target device.

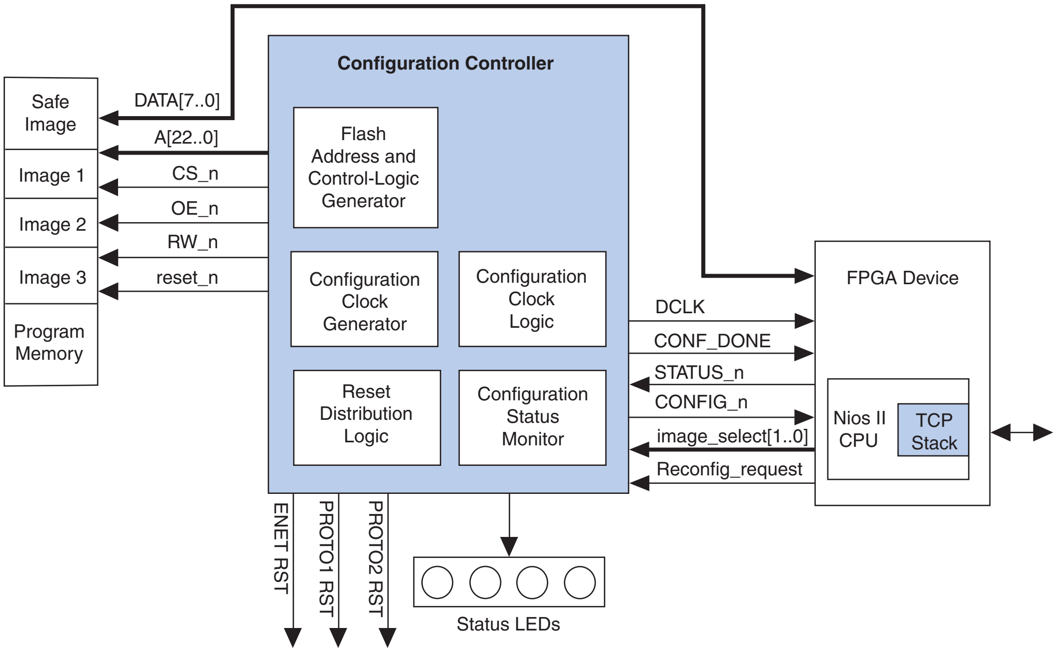
Figure 11. Image Select Capability



Upgrading Hardware Images via an Ethernet Link

The configuration controller that ships with Altera development kits supports upgrading the hardware image over an Ethernet link. Upgrading can occur when a Nios II embedded processor equipped with a transmission control protocol (TCP) stack is running in the target FPGA. In this scenario, the Nios II processor receives a programming file via an Ethernet link, and then stores the programming file into flash memory. When the flash file upgrade completes, the Nios II processor issues a reconfiguration request, which downloads the new hardware image into the target device. Figure 12 shows an example system that can automatically be reconfigured via an Ethernet link.

Figure 12. Ethernet Reconfigurable System



The Nios Embedded Evaluation Kit, Cyclone III Edition and the Altera Embedded Systems Development Kit, Cyclone III Edition include an application selector utility as their factory design. The application selector utility is capable of remote update using Ethernet.

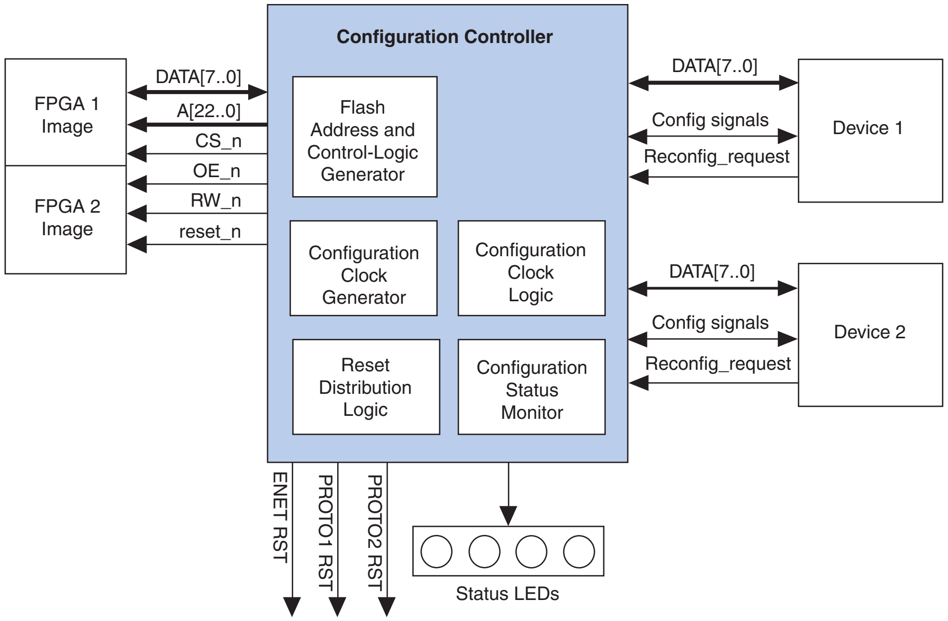
Configuring Multiple Devices

Configuring multiple FPGAs is another application that demonstrates the flexibility of a CPLD-based configuration controller. There are a number of different configuration scenarios that exist when multiple FPGAs reside on the same board, including:

- Multiple identical FPGAs
- Multiple FPGAs from the same vendor with different hardware images
- Multiple FPGAs from different vendors

Figure 13 illustrates a configuration controller that can configure multiple FPGAs where each FPGA requires a different configuration file. The Figure 13 controller can program different device family devices from either the same vendor or different vendors. In this scenario, the flash memory contains two configuration images for two target FPGAs. The Figure 13 controller logic programs one device at a time.

Figure 13. Multiple Device Configuration



Conclusion

The use of flash memory to store hardware configuration data for FPGAs located in an embedded system typically requires an intelligent configuration controller. Many of Altera's development boards contain a programmable configuration controller that provides a stable platform for managing system configuration and reset in embedded systems.

You can port the Nios II configuration controller reference designs to other boards, as well as modify the designs to support more complex systems and configuration requirements.

Because the Altera MAX family CPLDs are ideally-suited for use as board-level configuration controllers, configuration controllers on Altera development boards utilize Altera MAX CPLDs.

The programmable nature of MAX CPLDs allows you to use the same device in a variety of different systems. Because the MAX device supports both local and remote configuration updates, a MAX-based configuration controller is particularly useful in systems with embedded processors—such as the Nios II embedded processor.

Document Revision History

Table 6 shows the revision history for this document.

Table 6. Document Revision History

Date and Revision	Changes Made	Summary of Changes
March 2009 v1.2	Added coverage for the Nios II Embedded Evaluation Kit, Cyclone III Edition using the Cyclone III FPGA Starter Board and the Altera Embedded System Development Kit, Cyclone III Edition using the Cyclone III 3C120 Development Board.	Cyclone III
July 2006 v1.1	Updated application note to cover Stratix II and Cyclone II, rather than Stratix and Cyclone.	Stratix II, Cyclone II
March 2004 v1.0	Initial Release.	—

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